COTS Components Radiation Test Activity and Results at MSSL

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Abstract—this paper reports a full radiation test results for two popular commercial off the shelf (COTS) devices ADC128S102 and DAC121S101, targeted for use in MSSL's VIS instrument on ESA's EUCLID mission. The tests include total ionization dose (TID) and single event effect (SEE). The TID test shows both devices have passed 30krad test limit. Single event latch-up (SEL) has been observed at both devices at LET of 60 MeV.cm².mg⁻¹ or below.

Index Terms-COTS, SEE, TID, ADC, DAC, MSSL, EUCLID

I. INTRODUCTION

MSSL has a long established history in making scientific instrument for major space agency in the world like

ESA, NASA. Program like Hindo/EIS instrument on Solar-B, PEACE instrument on Cluster have won MSSL world reputation.

In recently years, as the narrowing choice of flight qualified parts and their staggering price, MSSL moves to upscreen some COTS devices. This proves to be very fruitful in reducing cost and improves the instrument performance.

This paper will report the full radiation test results of two widely used TI devices: ADC128S102 and DAC121S101.

Both have a space grade rad-hard version (QML part) commercially available. The version under test is the industry grade. It is vocally confirmed from a TI engineer that the QML counterpart applies a rad-hardening design to improve the radiation performance.

This paper will describe the test setup and report the test results.

II. TEST SETUP

A. Test Facilities

1) TID

ALTER TECHNOLOGY(ATN)[1], as the MSSL COTS devices upscreening program industry partner, provides the TID test facility. Their RADLAB gamma radiation laboratory is based on a Cobalt-60 source placed into a Gammabeam X200 irradiator. This Cobalt-60 source has 1.17 and 1.33 MeV energies and 403TBq (10894Ci) certified on 2013, Jan 28th. The facility can meet the requirements by MSSL and applicable standards such as ECSS, MIL-STD or ASTM. The dose rate can be adjusted to customer needs within a wide

range, including standard and low window rates specified in ESCC 22900[5].

2) SEE

The heavy ion test is done by HIREX ENGINEERING, now part of ATN. The facility selected is RADEF[2] at JYFL, University of Jyvaskyla, Finland. The facility includes a special beam line dedicated to irradiation studies of semiconductor devices. It consists of a vacuum chamber including component movement apparatus and the necessary diagnostic equipment required for the beam quality and intensity analysis.

The available beam sources are listed in Table I.

TABLE I

Ion	LET ^{SRIM} at surface [MeV.cm ² .mg ⁻¹]	Range ^{SR™} [µm]	Beam energy [MeV]
20 Ne ⁺⁶	3.63	146	186
$^{40}Ar^{+12}$	10.2	118	372
⁵⁶ Fe ¹⁵⁺	18.5	97	523
82 Kr ²²⁺	32.1	94	768
131 Xe ³⁵⁺	60.0	89	1217

The data is quoted from the RADEF test report [3][4].

B. Test Setup and standards

1) Abbreviations and units

Table II lists all the abbreviations used in this document. Unless otherwise noted, by default, all LET values are in MeV.cm2.mg-1, all cross-sections in cm2/device and total dose is rad in silicon(Si).

Abbreviations	Definitions
ADC	Analog to Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DUT	Device Under Test
LET	Linear Energy Transfer
SEE	Single Event Effect
SEFI	Single Event Function Interrupt
SEL	Single Event Latchup
SET	Single Event Transient
SEU	Single Event Upset
TID	Total Ionization Dose

2) TID

The test plan is prepared by ATN in conformance with ECSS22900[5] and MSSL requirements. The mission requirement of total dose is 5krad including the design margin of 2. To maximize the confidence, the test at ALTER is extended to 30krad. The dose rate in plan is 360 rad/h, which falls into "Low rate" window according to ECSS22900 definition.

The bias circuit and configuration is defined as close to the real circuit as possible and also close to the datasheet test

The research was carried out at the Mullard Space Science Laboratory, University College London, as part of the EUCLID VIS flight instrument development project.

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circuit so that the selected electric parameters can be monitored and compared to the datasheet value. The ECSS22900 calls for a worst-case bias condition to be used, which is difficult to determine without an evaluation phase.

The test procedure follows ECSS22900 Fig. 1 flow chart for qualification and lot acceptance testing.

Table III shows the detail irradiation steps. TABLE III

1	IRRADIATION EVALUATION TEST STEPS						
STEPS	1	2	3	4	5	6	7
PROCESS	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad	Irrad
Dose[krad(Si)]	2.5	2.5	5	10	10	-	-
Cumulative Dose [krad(Si)]	2.5	5	10	20	30	-	-
Dose Rate [rad(Si)/h]	360	360	360	360	360	-	-
Exposure Time (h)	6.9	6.9	13.9	27.8	41.7	24	168
Temperature (°C)	25	25	25	25	25	25	85

The real dose rate may vary slightly at each test.

3) SEE

The test plan is prepared by ATN in conformance with ECSS25100[6] and MSSL requirements. The mission requirement of SEE is if the device shows a threshold LET above 60MeV, it can be considered as immune to SEE in space. If it is below, SEE analysis shall be performed. Below 15MeV, the proton induced sensitivity analysis shall be conducted as well.

Heavy ions listed in Table I will be used in the test. To test beyond the LET of 60MeV, the EUT can be tilted with respect to the beam axis. At Xenon source, tilt of 30° can provide effective LET of 70MeV and 45° for 85MeV.

The test covers SET, SEU, SEFI and SEL. The SET/SEU/SEFI is all soft errors and their consequences are considered not severe for this application. SEL has the potential of destructive and permanent damage to the device. So it is closely watched and carefully examined in the test.

SET/SEU/SEFI test will be performed up to 100 events or ions fluence reaches 1E6 ions/cm2. SEL will be performed up to 100 events or 1E7 ions/cm2. If device is found sensitive to Xe, additional test will be performed at Kr.

Fig. 1 shows the principle of the heavy ion test system. The test mother board includes the voltage and current monitoring and the latch-up management of the DUT power supplies.

A SEL event is detected when corresponding DUT current exceeds a given threshold current within a few microseconds; it is then followed by a DUT power reset after a given off time.

A SET event is detected when the DUT output is above or below the expected value plus or minus a given threshold.

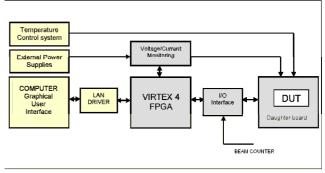


Fig. 1 SEE heavy ion test setup

The bias condition is set at close to real operation or predicted worst case condition. ADC128S102 is clocked at 16MHz and DAC121S101 is clocked at 30MHz. Both chips are mounted on a single PCB and configured in such way that the DAC output feeds into the ADC input. Each PCB contains three chains shown in Fig. 2. Only one device (the ADC or the DAC) is exposed to radiation source at each test. The other is covered.

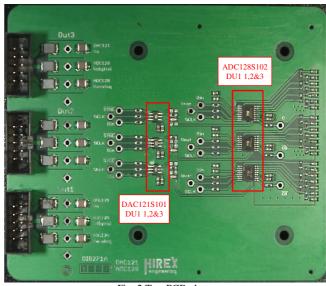


Fig. 2 Test PCB photo

The top cover of the device is removed to expose the die direct to the radiation source before the test.

III. TEST RESULTS

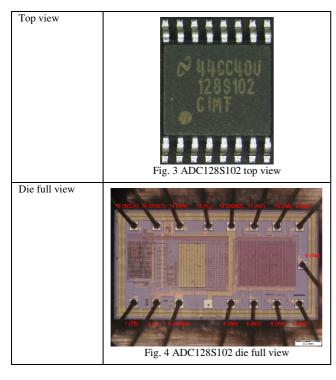
A. ADC128S102

The ADC128S102 from TI is a low-power, eight-channel CMOS12-bit analogue to digital converter. The converter is based on successive-approximation register(SAR) architecture with an internal track-and-hold circuit.

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1) Device description

Item	Description
Part type	ADC128S102
Manufacturer	Texas Instruments
Part number	ADC128S102CIMT/NOPB
Date code	1414
Package	TSSOP-16
Top marking	logo 44CC40U 128S02 CIMT
Bottom marking	-
Die dimensions	891µm x 1649µm



2) TID[7]

The electrical parameters and bias condition for the test is listed in Table V.

	ELECT	RICAL MEASUR	TABLE V EMENTS TEST CONDITION	N AND I	LIMITS	
N°	SYMBOL	TEST	CONDITIONS	LIN	AITS	UNIT
			$(T_{AMB} = 22 \pm 3^{\circ}C)$	MIN	MAX	
1	INL	Integral Non	$V_A = V_D = +3.0V$	-	±1	LSB
2	INL	Linearity	$V_{\rm A} = V_{\rm D} = +5.0 V$	-	±1.2	LSB
3	DNL	Differential	$V_{\rm A} = V_{\rm D} = +3.0 V$	-0.7	+0.9	LSB
4	DNL	Non Linearity	$V_{\rm A} = V_{\rm D} = +5.0 V$	-0.9	+1.5	LSB
5	V	Offset Error	$V_{\rm A} = V_{\rm D} = +3.0 V$	-	±2.3	LSB
6	V _{OFF}	Oliset Erior	$V_{\rm A} = V_{\rm D} = +5.0 V$	-	±2.3	LSB
7	FSE	Full Scale	$V_{\rm A} = V_{\rm D} = +3.0 V$	-	±2.0	LSB
8	132	Error	$V_{\rm A} = V_{\rm D} = +5.0 V$	-	±2.0	LSB
9	I _{DCL}	Analog Input DC Leakage Current		-	±1	μΑ
10	I_{IN}	Digital Input Current	$VIN = 0V \text{ or } V_D$	-	±1	μΑ
11		Total Supply Current	$V_A = V_D = +2.7V \text{ to}$ +3.6V, $f_{SAMPLE} = 1MSPS, f_{IN} =$ 40KHz $V_A = V_D = +4.75V \text{ to}$	-	1.5	mA
11	T .T	Normal Mode (CS low)	$V_A = V_D = +4.75V$ to +5.25V, $f_{SAMPLE} = 1MSPS$, $f_{IN} = 40KHz$ $V_A = V_D = +2.7V$ to	-	3.1	mA
12	I _A +I _D	I _A +I _D Total Supply Current Shutdown Mode (CS high)	+3.6V, $f_{SAMPLE} = 1MSPS$, $f_{IN} = 40KHz$	-	1.0	μΑ
12			$V_{A} = V_{D} = +4.75V \text{ to}$ +5.25V, $f_{SAMPLE} = 1MSPS, f_{IN} =$ 40KHz	-	1.4	μΑ

1. AGND = DGND = 0V, f_{SCLK} = 8MHz to 16MHz, f_{SAMPLE} = 500Ksps to 1MSPS, C_L = 50pF, unless otherwise noted in table III.

5 biased, 5 unbiased and 1 control unit are under the test. Does rate was adjusted to 207.54rad/h and test stopped at 30krad.

Results

The results show all the parameters being monitored during the irradiation process are well within the datasheet limit up to the maximum test level. See Table VI for the summary: TABLE VI

SUMMARY OF THE IRRADIATION TEST RESULTS								
	0 krad	2.5 krad	5 krad	10 krad	20 krad	30 krad	ANN 24h	ANN 168h
INL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
DNL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
VOFF	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
FSE	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IDCL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IIN	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
IA+ID	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS

However there are some parameters showing some sensitivity after 10krad. The most affected parameter is the Total Supply Current Shutdown Mode (Ia+Id), only for biased irradiated samples. The trend profile differences with different bias voltage. See Fig. 5 and Fig. 6

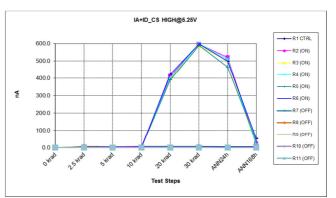


Fig. 5 IA+ID at CS high at V_A=V_D=+5.25V parameter shifts during irradiation process.

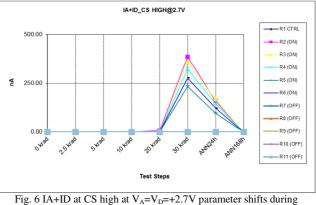


Fig. 6 IA+ID at CS high at $V_A = V_D = +2.7 V$ parameter shifts during irradiation process.

During the annealing process the affected parameter tends to recover its initial values.

3) SEE[3] SEL test runs For SEL test condition (VA=VD=+3.6V), DUT case temperature was set to 50°C and SEL detection threshold for each DUT was 80mA for VA and 50mA for VD.

SEL have been observed on VA only and measured SEL currents are about 180mA. In addition step current increase has been recorded but significantly below 80mA.

No SEL was observed with Krypton (tilt= 45° and Effective LET=45MeV).

When tested in the SEL test mode but at room temperature, few SEL has been observed on VA as well as some step currents with Xenon (LET=60MeV).

SEL cross-section for each sample is shown in Fig. 7.

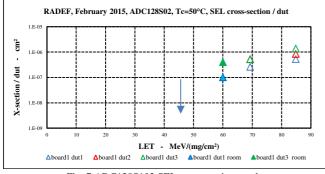


Fig. 7 ADC128S102 SEL cross-section results

SET test runs

SET cross-section for each sample is shown in Fig. 8.

With krypton (LET=32MeV) and higher LETs, when a step current occurred, sample might enter a SEFI mode error (permanent errors) or not and the step current as well as the SEFI mode were cured by a manual power reset. No SET event is found at Ar (LET=10.2 MeV) and lower LET.

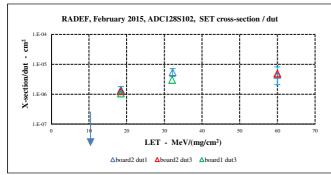
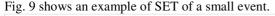
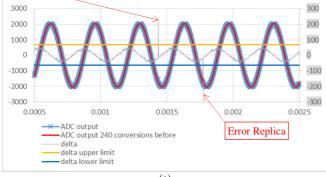


Fig. 8 ADC128S102 SET cross-section results



Error detection run022, dut3, SET event stamped 13827.150505380



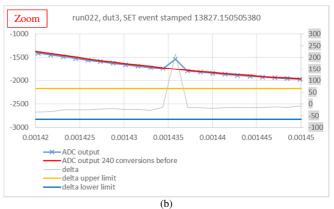


Fig. 9 A small SET event is captured. (a) is the full view. (b) is the zoom-in of the event, which shows it is a single conversion error.

SEE test results an	e summarized in	Table VII.
	TABLE VII	

	SUMMARY OF THE SEE TEST RESULTS							
Eff. LET	LET SEL SET		STEP CURRENT	SEFI				
MeV. cm ² .mg ⁻¹	cm ²	cm ²	cm ²	cm ²				
3.6	N/T	FREE	FREE	FREE				
6.5	N/T	FREE	FREE	FREE				
10.2	N/T	FREE	FREE	FREE				
18.5	N/T	1.40E-06	FREE	FREE				
32.1	N/T	5.40E-06	1.04E-07	1.04E-07				
45	FREE	N/T	N/T	N/T				
60	1.67E-07	4.50E-06	4.55E-07	4.55E-07				
69.3	4.31E-07	N/T	N/T	N/T				
84.9	9.12E-07	N/T	N/T	N/T				

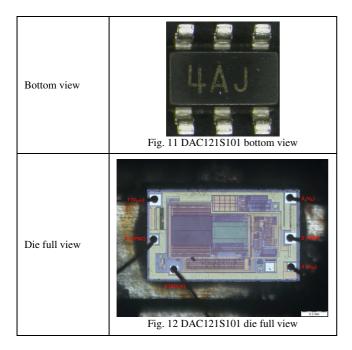
B. DAC121S101

The TI DAC121S101 is a very low-power, precision, general purpose, 12-bit voltage-output digital to analogue converter. The automotive grade version is used in test.

1) Device description

TABLE VIII	
DAC121S101 DEVICE DETAILS	

Item	Description		
Part type	DAC121S101		
Manufacturer	Texas Instruments		
Part number	DAC121S101QCMK/NOPB		
Date code	1440		
Package	SOT-6		
Top marking	X61Q		
Bottom marking	4AJ		
Die dimensions	749µm x 1233µm		
Top view	Fig. 10 DAC121S101 top view		



2) TID[8]

The electrical parameters and bias condition for the test is listed in Table IX.

ELECTRICAL MEASUREMENTS TEST CONDITION AND LIMITS								
N°	SWADOL	TECT	CONDITIONS		LIN			
N°	SYMBOL	TEST	$(T_{AMB} = 2$	2±3°C)	MIN	MAX	UNIT	
1	INL	Integral Non Linearity	Over Decim 48 to 4047	Over Decimal codes 48 to 4047		±8	LSB	
2	DNL	Differential Non Linearity	$V_{\rm A} = 2.7 V t$	o 5.5V	-0.7	+1.0	LSB	
3	ZE	Zero Code Error	$I_{\rm OUT}=0$		-	+15	mV	
4	FSE	Full Scale Error	$I_{\rm OUT}=0$		-	-1.0	%FSR	
5			$V_A = 3V, I_0$ 10µA	_{UT} =	2.990	-	v	
6	FSO	Full Scale Output	$V_A = 3V, I_{OI}$ 100 μA $V_A = 5V, I_{OI}$ 10 μA	UT =	2.985	-	v	
7	r3U	(Note 2)		_{UT} =	4.985	-	v	
8			$V_A = 5V, I_0$ 100µA	_{UT} =	4.985	-	v	
9	I _{A1}		Normal Mode	V _A = 5.5V	-	270	μΑ	
10	\mathbf{I}_{A1}		$f_{SCLK} = 20MHz$	V _A = 3.6V	-	197	μΑ	
11	T		Normal Mode	V _A = 5.5V	-	230	μΑ	
12	I _{A2}		f _{SCLK} = 10MHz	V _A = 3.6V	-	175	μΑ	
13	т		Normal Mode	V _A = 5.5V	-	190	μΑ	
14	I_{A3}	Supply Current (output unloaded)	$f_{SCLK} = 0$	V _A = 3.6V	-	160	μΑ	
15	I _{A4}	(Note 2)	All PD Modes	V _A = 5.0V	-	60	μΑ	
16	1 _{A4}		f _{SCLK} = 20MHz	V _A = 3.0V	-	30	μΑ	
17	I _{A5}		All PD Modes	V _A = 5.0V	-	40	μΑ	
18	145		$f_{SCLK} = 10MHz$	V _A = 3.0V	-	20	μΑ	
19	L		All PD Modes	V _A = 5.0V	-	1.0	μΑ	
20	I _{A6}		$f_{SCLK} = 0$	V _A = 3.0V	-	1.0	μΑ	

	I ADLE IA	
FIECTRICAL	MEASUREMENTS TEST CONDITION AND LIMITS	

N STMBOL TEST $(T_{AMB} = 22\pm 3^{\circ}C)$ MIN MAX 21 ts Output Voltage settling Time (Note 2) 00Fh to FF0h code change, R ₁ = ∞ - 15 μs	N°	SYMBOL	TEST	CONDITIONS	LIMITS		UNIT
21 t _s settling Time change, - 15 μs	IN	STNIBOL	IESI	$(T_{AMB} = 22 \pm 3^{\circ}C)$	MIN MAX		
	21	ts	settling Time	change,	-	15	μs

1. $V_A = +2.7V$ to +5.5V, $R_L =$ unload, $C_L = 200$ pF to GND, $f_{SCLK} = 30$ MHz, input code range 48 to 4047, unless otherwise noted in Table IV.

 These limits and test conditions are from the manufacturer's QML data sheet as there are no limit values specified in the Automotive Grade data sheet. This test should be considered for information purposes only. Components tested may exceed these limits but should not be deemed failures.

5 biased, 5 unbiased and 1 control unit are under the test. Does rate was adjusted to 212.7rad/h and test stopped at 30krad.

<u>Results</u>

The results show that some parameters are affected slightly by the irradiation process.

ZE@2.7V, ZE@5.5V, IA2@(3.6V,10MHz), IA3@(3.6V,0MHz), IA4@(3V,20MHz,1k), IA4@(3V,20MHz,100k), IA4@(3V,20MHz,100k), IA4@(3V,20MHz,Hi-Z),

IA5@(3V,10MHz,1k),

IA5@(3V,10MHz,100k),

IA5@(3V,10Mhz,Hi-Z), and IA6 are the most affected parameters.

In all cases, the deviation was more significant in the biased parts than in the unbiased ones.

These parameters all return to their initial values during the annealing process.

Full results are summarized in Table X.

TABLE X SUMMARY OF THE IRRADIATION TEST RESULTS

	SUMMARY OF THE IRRADIATION TEST RESULTS							
	0 krad	2.5 krad	5 krad	10 Krad	20 krad	30 krad	ANN 24h	ANN 168h
INL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
DNL	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
ZE	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
FSE	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
FSO	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I _{A1}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I _{A2}	See note1	See note1	See note1	See note1	See note1	See note1	See note1	See note1
I _{A3}	See note1	See note1	See note1	See note1	See note1	See note1	See note1	See note1
I _{A4}	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
I _{A5}	See note1	See note1	See note1	See note1	See note1	See note1	See note1	See note1
I _{A6}	PASS	PASS	PASS	PASS	PASS	See note1	See note1	PASS
ts	PASS	PASS	PASS	PASS	PASS	PASS	PASS	PASS
Note 1:								

Note 1:

These parameters shows values slightly higher than the maximum limit set by the manufacturer datasheet but all within the limit set by the military spec 5962-07226, which is the spec for the QML equivalent of this COTS device under test. Therefore we conclude the affected parameters are acceptable.

Fig. 13, Fig. 14 and Fig. 15 show some affected parameters at particular configuration.

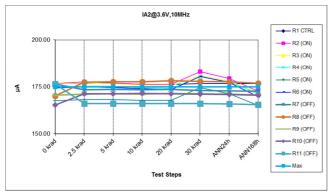


Fig. 13 IA2 at +3.6V and 10MHz shifts during irradiation process.

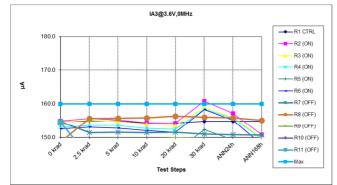


Fig. 14 IA3 at +3.6V and 0MHz shifts during irradiation process.

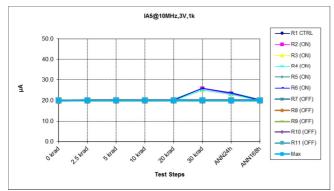


Fig. 15 IA5 at +3.6V and 10MHz with 1k load shifts during irradiation process.

3) SEE[4]

SEL test runs

For SEL test condition (Va=3.6V), DUT case temperature was set to 50°C and SEL detection threshold for each DUT was 50mA.

SEL have been observed as low as Kr (TILT=45°, EFF. LET=45MeV). When case temperature is reduced to 25°C, the number of SEL events significantly drops. SEL currents are between 51mA and 200mA. In addition step current increase has been recorded below 50mA. These step currents are cured by a next SEL event which triggers a power reset.

Then part of the SEL events counted could be step current increases with a current value higher than 50mA.

SEL cross-section for each sample is shown in Fig. 16.

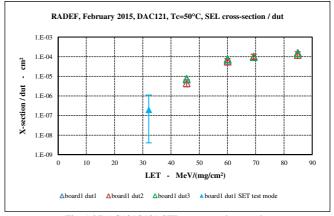


Fig. 16 DAC121S101 SEL cross-section results

SET test runs

For SET test condition (Va=+2.7V), DUT case temperature was set to 25°C. SET cross-section for each sample is calculated and shown in Fig. 17.

With Krypton (LET=32 MeV) and higher LETs, when a step current occurred, sample might enter a SEFI mode error (permanent errors) or not and the step current as well as the SEFI mode will be cured either by an SEL or by a manual power reset. No SET event is found at Fe(LET=18.5MeV) and lower LET.

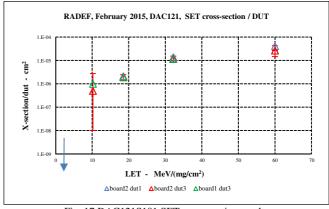
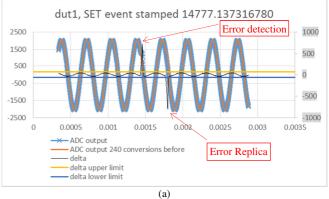
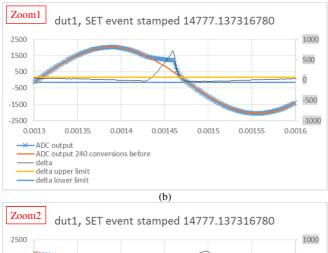
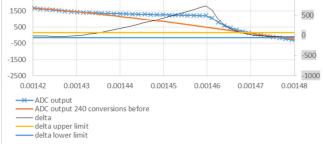


Fig. 17 DAC121S101 SET cross-section results

Fig. 18 shows an example of SET of a large event.







(c)
Fig. 18 A large SET event with a duration of about 200µs is captured.
(a) shows the full view. (b) and (c) are two zooms of the event which shows that many successive conversions are affected.

SEE test results are summarized in Table XI . TABLE XI

SUMMARY OF THE SEE TEST RESULTS							
Eff. LET	SEL SET		STEP CURRENT	SEFI			
MeV. cm ² .mg ⁻¹	cm ²	cm ²	cm ²	cm ²			
3.6	N/T	FREE	N/T	N/T			
6.5	N/T	FREE	FREE	FREE			
10.2	N/T	FREE	FREE	FREE			
18.5	N/T	2.10E-06	FREE	FREE			
32.1	2.02E-07	1.40E-05	6.12E-07	8.16E-07			
45.5	6.80E-06	N/T	N/T	N/T			
60	6.42E-05	4.10E-05	1.64E-06	1.64E-06			
69.3	9.50E-05	N/T	N/T	N/T			
84.9	1.57E-04	N/T	N/T	N/T			

IV. SUMMARY

Both devices pass 30krad TID test with very minor parameter shifts. In the SEE test, both devices show radiation softness with both SEL and SET events captured at LET at or below 60 MeV.cm2.mg-1.

It is recommended to use the ADC in house-keeping circuit or other uncritical circuit where a loss of data due to single transient events are acceptable. The data from one technology demonstration mission using this commercial ADC as a housekeeping function in low earth orbit (~500km polar synchronization orbit) has demonstrated that the number of error data due to SET events will increase as the device ages or TID accumulates. For critical function, it is recommended to use its QML version, which has implemented rad-hardening design.

A useful strategy for DAC to overcome SET impacts is to regularly refresh its data register. Besides add a low pass filter or buffer amplifier at its output to filter the unwanted pulse induced by the SET.

For both devices, the SEL cross-section should be taken into account with the mission environment. When necessary, a latch-up protection circuit should be added to ensure the device safety.

V. FUTURE WORKS

More COTS parts like EL7457, AD8065 and DG612 are going through the radiation screening under EUCLID program. Their results will be published later on.

REFERENCES

- RadLab at ALTER TECHNOLOGY(Spain), webpage: <u>http://www.altertechnology.com/atn/en/radiation/total-ionizing-dose-tests-924.htm.</u>
- [2] RADEF, JYFL, University of JYVASKYLA, webpage: https://www.jyu.fi/fysiikka/en/research/accelerator/radef
- [3] Single event effects test report for ADC128S102, internal report, HIREX.
- [4] Single event effects test report for DAC121S101, internal report, HIREX.
- [5] ESCC 22900 "Total dose steady-state irradiation test method", issue 4, October 2010.
- [6] ESCC 25100 "Single event effects test method and guidelines", issue 2, October 2014.
- [7] ADC128S102 Total ionization dose test report, internal report, ALTER TECHNOLOGY.
- [8] DAC121S101 Total ionization dose test report, internal report, ALTER TECHNOLOGY.