# InAs/GaAs Quantum-Dot Lasers Monolithically Grown on on-axis Silicon (001)


Manyu Dang
*Department of Electronic and Electrical Engineering*
*University College London*London
WC1E 7JE, UK
manyu.dang.16@ucl.ac.uk

Mingchu Tang
*Department of Electronic and Electrical Engineering*
*University College London*
London WC1E 7JE, UK
mingchu.tang.11@ucl.ac.uk

JunJie Yang
*Department of Electronic and Electrical Engineering*
*University College London*
London WC1E 7JE, UK
junjie.yang.13@ucl.ac.uk

Alwyn Seeds
*Department of Electronic and Electrical Engineering*
*University College London*
London WC1E 7JE, UK
a.seeds@ucl.ac.uk

Siming Chen
*Department of Electronic and Electrical Engineering*
*University College London*
London WC1E 7JE, UK
siming.chen@ucl.ac.uk

Huiyun Liu
*Department of Electronic and Electrical Engineering)*
*University College London*
London WC1E 7JE, UK
huiyun.liu@ucl.ac.uk



***Abstract*—Inversion boundaries (IBs) are charged planer defects that arise from the growth of polar III–V materials on non-polar Si (001) substrate. This paper demonstrates a novel technique to achieve all-MBE grown, IB-free GaAs on on-axis Si (001) substrates by employing periodic Si single-atomic-height steps to re-distribute the nucleation of IBs and promote IB self-annihilation in the subsequent GaAs growth. Furthermore, an electronically pumped quantum-dot (QD) laser has been demonstrated on this IB-free GaAs/Si platform with a maximum operating temperature of 120 °C. These results could be a significant step towards the monolithic integration of III-V materials and devices with mature CMOS technology.**



**Keywords— Si photonics, inversion boundaries, on-axis Si (001)**


## I. Introduction

Accumulated by the rapid development of the internet of things, cloud engineering and ever-growing data traffic, Si photonics is emerging as the essential technology for next-generation data centers and communication systems. As Si photonics shows its potentiality of integrating optical components with well-established integrated circuits utilizing developed CMOS fabrication technology [1,2]. To circumvent the inferior light emitting nature from group IV materials, integrating direct bandgap III/V materials as the reliable, high-efficiency light source on the Si platform offers a promising approach for the Si photonics [3,4]. Among mainstream integration methods, including heterogenous integration (wafer bonding and flip-flop bonding technique) and monolithic integration, the latter approach is more attractive for low-cost, high-yield and large-scale production [5].

However, the monolithic integration of III-V materials on Si is challenging due to the large material dissimilarities between III-V materials and Si. Lattice mismatch, different thermal expansion coefficients and contrary polarities between III-V materials and Si substrate lead to a series of growth defects such as threading dislocations (TDs), respectivily, thermal cracks, and inversion boundaries (IBs) [6,7]. These growth defects undermine the quality of crystal and form non-radiative recombination centers, which dramatically hinder the laser performance. IBs originate at the interface when growing polar III-V materials directly on non-polar Si (001) substate. Every Si single-atomic-height (*S*) step triggers the formation of IBs, while the Si double-atomic-step (*D*) steps prevent this formation [6,9].

Intensive research has been done to eradicate IBs. The conventional method to prevent IBs utilizes the Si oriented substrate with various offcut angles from 4°-7° toward [110] or [111] plane for creating stable Si *D* steps [10]. However, offcut substrates are incompatible with the standard COMS fabrication process, which strictly demands nominal on-axis (001) Si substrates. Other approaches have been developed to eliminate IBs include using patterned Si substrate,template-assisted selective epitaxy, III-V nano-ridge engineering and high-temperature annealed Si substrate under a hydrogen ambiance by using metal organic chemical vapor deposition (MOCVD) [11-14]. But the complicated substrate pre-treatments and hydrogen source are not feasible for the solid-source molecular beam epitaxy (MBE) growth, which is a favorable growth technique for growing high-quality QD laser.

## II. Experimental Detail and Result Discussion

Firstly, a 200 nm Si buffer layer was grown on the deoxidized on-axis Si (001) substrate with random miscut angle 0.15°± 0.1° toward [110] orientation. This Si buffer consisted of a 100 nm of Si layer annealed at 900 °C followed by 5 periods of 20 nm Si layers annealed at 1200 °C. In the subsequent GaAs growth, a three-step growth method was employed, a 250 nm GaAs nucleation layer was first grown at a low temperature (LT) of 350 °C on the Si buffer. Then another 250 nm GaAs layer was deposited at a mid-temperature (MT) of 420 °C, followed by a 500 nm GaAs layer was grown at a high temperature (HT) of 580 °C to complete this IB-free buffer growth. The atomic force microscopy (AFM) results show the surface morphology of the original deoxidized Si substrate and the Si buffer layer. Randomly distributed Si steps appear on the deoxidized Si surface (Fig.1a) to neutralize the elastic energy of different stress domains. By contrast, periodic Si steps are formed on the Si buffer layer,

as shown in Fig.1 b,c. The height of each step is ~0.13nm (Fig.1 d), proving these periodic steps are Si *S* steps.

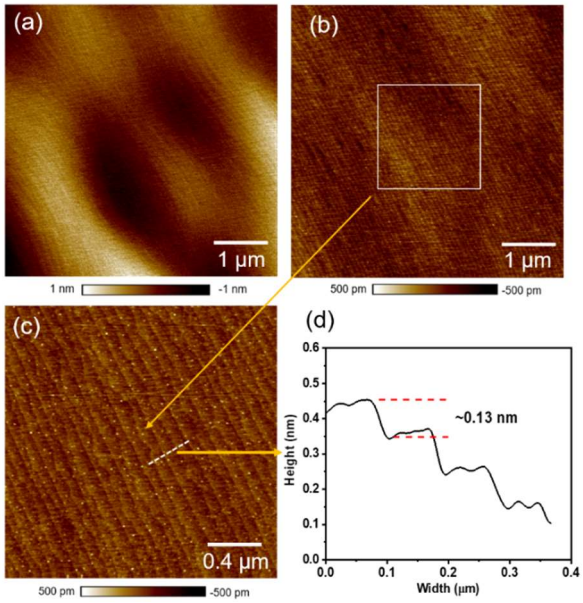


**Fig.1.** 5 μm × 5 μm AFM images illustrate the surface morphology of Si surface. a, Si surface after 30 min deoxidation. b, Surface of 200 nm Si buffer layer. c, 2 μm × 2 μm AFM image of Si buffer layer surface showing alternating *S* step pairs. d, Height measurement of each step on the surface of 200 nm Si buffer.

To further study the mechanism of the IB annihilation, a cross-sectional transmission electron microscope (TEM) measurement was performed to examine the cross-sectional structural properties of GaAs-on-Si heteroepitaxy. In Fig.2 a,b IBs are randomly nucleated at the interface between Si and GaAs and propagate freely within the crystal structures. During the subsequent growth of GaAs layers, the growth temperature is gradually ramped to enhance the probability of intersecting of IBs as shown in the Fig.2 a,b. Even though some of IBs can be self-annihilated during the growth procedure, the remaining IBs still propagate freely in three dimensions and penetrate the whole structure. As for the sample with annealed Si buffer, the nucleation of IBs resembles the underlying Si steps. As a result, periodic {110} IBs are observed in Fig. 2c,d. During the temperature ramping process in the subsequent GaAs growth, the kick of IBs into higher index planes such as {111} and {112} planes promotes self-annihilation of IBs within about 500nm GaAs growth .

Based on this IB-free GaAs/Si (001) platform, a broad-area InAs/GaAs QDs laser structure has been fabricated with low threshold current density ($J_{th}$) of 83.3 A cm$^{-2}$ and high operating temperature up to 120 °C under a pulsed mode. The slope efficiency of the single-facet emission of 0.13 W A$^{-1}$ at 20°C remains stable as temperature increased. The characteristic temperature ($T_0$) is calculated as ~55 K between 20 and 100 °C.

## III. Conclusion

In conclusion, we demonstrate a novel approach by employing the periodic *S* Si step and temperature-varying growth technique to achieve IB-free GaAs grown on on-axis Si (001) substrates. Based on this IB-free GaAs/Si (001) platform, an InAs/GaAs QD laser is fabricated with low $J_{th}$ of 83.3 A cm$^{-2}$ and a maximum operating temperature of 120 °C .This approach simplifies growth requirements for high-quality IBs free platform and is a huge milestone for the monolithic integration of III-V polar material on on-axis (001) substrate.

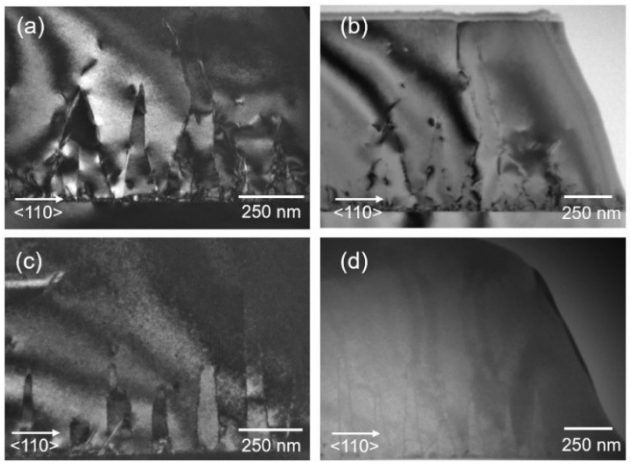


**Fig.2.** Cross-sectional TEM measurements with view direction of [110] of IBs propagation and annihilation. a, dark field image of the sample without annealed Si buffer, b, bright field image of the sample without annealed Si buffer, c, dark field image of the sample with annealed Si buffer, d, bright field image of the sample with annealed Si buffer.

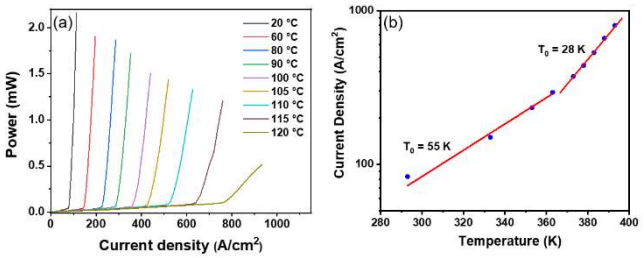


**Fig.3.** a, temperature dependent light–current (*L–I*) curves of the InAs QD laser up to 120 °C. b, Temperature dependence of the $J_{th}$ showing the characteristic temperature $T_0$ of the laser sample.

## References


[1] S. Chen *et al.*, "Electrically pumped continuous-wave III–V quantum dot lasers on silicon"*Nat. Photonics*, vol. 10, no. 5, pp. 307–311, 2016.
[2] Wu, S. Chen, A. Seeds, H. Liu, J. Phys. D: Appl. Phys. 2015, 48,363001.
[3] D. Liang, J. E. Bowers, Nat. Photonics 2010, 4, 511.
[4] H. Liu, T. Wang, Q. Jiang, R. Hogg, F. Tutu, F. Pozzi, A. Seeds, Nat.Photonics 2011, 5, 416.
[5] M. Tang *et al.*, "Integration of III-V lasers on Si for Si photonics," *Progress in Quantum Electronics*. 2019.
[6] B. Kunert, Y. Mols, M. Baryshniskova, N. Waldron, A. Schulze, R. Langer, Semicond. Sci. Technol. 2018, 33, 093002.
[7] V. Yang, M. Groenert, C. Leitz, A. Pitera, M. Currie, E. A. Fitzgerald, J. Appl. Phys. 2003, 93, 3859.
[8] M. Tang, S. Chen, J. Wu, Q. Jiang, V. G. Dorogan, M. Benamara, A. Seeds, H. Liu, Opt. Express 2014, 22, 11528.
[9] H. Kroemer, J. Cryst. Growth 1987, 81, 193.
[10] R. Fischer, W. T. Masselink, J. Klem, T. Henderson, T. C. McGlinn, M. V. Klein, andJ. Washburn, J. Appl. Phys. 58(1), 374–381 (1985).
[11] Wang, Z., Tian, B., Pantouvaki, M. et al. Room-temperature InP distributed feedback laser array directly grown on silicon. Nature Photon 9, 837–842 (2015).
[12] S. Chen, M. Liao, M. Tang, J. Wu, M. Martin, T. Baron, A. Seeds, H. Liu, Opt. Express 2017, 25, 4632.
[13] A. J. Bain, A. Ostendorf, J.-M. Nunzi, D. L. Andrews, K. Moselund, H. Schmid, P. Staudinger, G. Villares, M. Sousa, B. Mayer, S. Mauthe,Proc. SPIE 2018, 10672, 106722U.
[14] B. Kunert, W. Guo, Y. Mols, R. Langer, K. Barla, ECS Trans. 2016, 75,409.