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Microwave Properties of 2D CMOS Compatible Co-Planar Waveguides Made from Phosphorus Dopant Monolayers in Silicon

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Low-dimensional microwave interconnects have important applications for nanoscale electronics, from complementary metal–oxide-semiconductor (CMOS) to silicon quantum technologies. Graphene is naturally nanoscale and has already demonstrated attractive electronic properties, however its application to electronics is limited by available fabrication techniques and CMOS incompatibility. Here, the characteristics of transmission lines made from silicon doped with phosphorus are investigated using phosphine monolayer doping. S-parameter measurements are performed between 4–26 GHz from room temperature down to 4.5 K. At 20 GHz, the measured monolayer transmission line characteristics consist of an attenuation constant of 40 dB mm^{-1} and a characteristic impedance of 600 Ω. The results indicate that Si:P monolayers are a viable candidate for microwave transmission and that they have a.c. properties similar to graphene, with the additional benefit of extremely precise, reliable, stable, and inherently CMOS compatible fabrication.

1. Introduction

Recent progress toward the scaling of silicon transistors down to single-atom devices [1] has motivated the requirement for nanoscale interconnects.[2] Conventional metals have limitations as they approach nanoscale dimensions due to resistivity scaling from surface and grain boundary scattering effects, and the difficulties in extending lithography techniques to sub-100 nm.[3] Favorable microwave properties have been shown for both macroscopic mono-layer graphene sheets[4–9] and carbon nano-tubes (CNTs),[10–14] leading to the development of theoretical models for nanoscale transmission lines in graphene.[15–22] Despite this, progress in the integration of graphene and CNTs into practical technologies has been hindered by processing issues: they oxidize easily in air which degrades their electrical properties,[23] they are contaminated by silicon limiting their complementary metal–oxide–semiconductor (CMOS) compatibility[24] and they cannot yet be reliably fabricated and placed with nanometer precision. Here we examine the use of atomically sharp, metallic phosphorus δ-doped silicon for low-dimensional interconnects. We show that the microwave properties of such micron-scale 2D sheets are comparable with graphene, with all the additional advantages brought by nanoscale processing, high stability and CMOS compatibility. The results motivate further study of the properties at the nanoscale.

Delta-layers are very thin buried layers of substitutional dopants within a semiconductor host lattice. They are often produced by a very short pulse of the dopant source during molecular beam epitaxy (MBE) growth.[25–27] In the case of phosphorus doping of silicon, they may also be fabricated using phosphine (PH_3) dosing of a clean silicon surface followed by low temperature MBE overgrowth.[27,28] Nanoscale wires fabricated with this method have been shown to maintain ohmic behavior even when the width is reduced down to almost the single atom scale.[27]

Research into phosphine doping has been strongly motivated by its use for atomically precise placement of single donors as silicon-based quantum bits (qubits).[29] For interfacing with the qubits, the same doping technique has been used for the fabrication of islands, on the scale of single atoms, for single electron transistors (commonly used in the low-frequency qubit initialization and readout),[1] and for creating electrical gates which have been shown to successfully control the quantum state with nanosecond accuracy using excitation signals up to 13 GHz.[30] Microwaves, and the high frequency alternating magnetic field they produce, are crucial for control of the qubit spins. In recent devices, waveguides are typically made from aluminum.[31] Replacing these aluminum components with δ-layer interconnects could enable individual qubit addressability and create a simplified fabrication procedure for both the qubit and its low- and high-frequency control architecture.

Graphene is well known to have excellent low frequency electrical properties, and Si:P monolayers are just as attractive. Large area graphene sheets are usually grown with chemical

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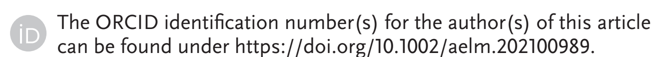
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vapor deposition (CVD)[32] with sheet resistances in the order of $R_S \approx 0.5$–15 kΩ □$^{-1}$ depending on the exact processing conditions, whilst in Si:P δ-doped layers, $R_S \approx 0.18$–1 kΩ □$^{-1}$ can be regularly achieved.[33] The sheet resistance, $R_S = 1/(n_{2D}e\mu)$, is inversely proportional to the 2D carrier density, n_{2D}, and the carrier mobility μ, and while graphene typically exhibits higher mobilities, Si:P monolayers have higher carrier densities. The electron mobility in CVD graphene[32] can be within the range 800–16000 cm^2 V^{-1} s^{-1} (although higher mobilities have been found with suspended exfoliated graphene,[32] the upper limit is far smaller when incorporated into a device), whereas with Si:P δ-layers $\mu \approx 100$ cm^2 V^{-1} s^{-1}.[34] The electron density of graphene[35] is limited to approximately two orders of magnitude lower than maximally doped Si:P δ-layers, for which[36] $n_{2D} \approx 1 \times 10^{14}$ cm^{-2}. Additionally, the kinetic inductance must be considered for low dimension, high mobility transmission lines, as dominance of the inductance can induce parasitic plasmonics resonances. The reduced mobility of the Si:P δ-doped layers, compared to graphene, is beneficial in this respect, where they can be used at much higher frequency without suffering from these parasitic plasmonic effects. Indeed, it is found that the kinetic inductance is negligible below frequencies when $\tau\omega \approx 0.1$, where τ is the momentum scattering time, which for Si:P δ-doped layers is ≈870 GHz. In this study, which investigates the transmission line properties in the range of 5–25 GHz, the influence of kinetic conductance effects can be neglected.

In order to assess the suitability of δ-doped Si:P layers for use as microwave transmission lines, we have studied phosphorus doped silicon monolayers prepared using two different silicon epitaxy recipes. These recipes produce variable confinement, mobility, and carrier concentration and thus provide insight into the role of these parameters on microwave transmission performance. The two different Si:P δ-layers investigated here were both doped at a phosphorus density of 0.35 ML, and then overgrown using either a constant low temperature epitaxy recipe (labeled P_{LTE}) or using an additional reduced temperature "locking layer" stage during the first few monolayers of epitaxial growth (labeled P_{LL}). The "locking layer" suppresses phosphorus surface segregation and increases the layer confinement, which comes at the expense of a lower carrier concentration and mobility.[37,38]

Each monolayer was processed into six coplanar waveguides (CPWs) with lengths l between 200–2000 µm, as seen in **Figure 1**. An additional "open" structure was fabricated on each monolayer constructed of the contact and probing pads. These are marked on Figure 1 as the structure components outside the area marked by the dotted vertical lines separated by CPW length l. An image of the "open" structure can be seen in Figure 2b. The cross-sectional geometry (defined by the signal line width, w, and the signal–ground distance, g, which are marked on Figure 1 was consistent for all CPWs.

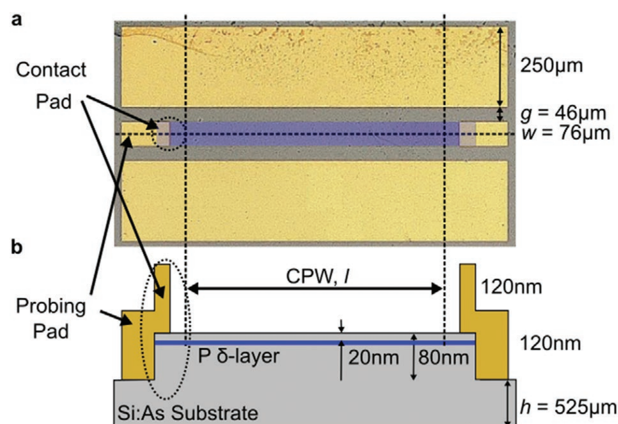

Figure 1. a) Plan view optical micrograph and b) cross-section diagram showing the experimental structure for the δ-layer co-planar waveguides. The CPW (between the vertical dashed lines) is formed of a δ-layer signal line and gold ground planes, and is terminated with contact and probing pads. In (a) the δ-layer is shadowed blue, and is represented as a blue line in (b). The bilayer contact pad (circled) is formed of a 100 µm section of δ-layer and a gold top contact with a 50 µm overlap forming a capacitive contact. An additional edge contact is formed to the probing pad, as seen in (b). The horizontal dashed line in (a) specifies the longitudinal slice in (b). The substrate height, h, and CPW length, l, are not shown to scale in (b). The geometry of the CPW is defined by the signal line width, w, the signal-ground distance, g, and the signal line length, l. The CPW and contact geometry for all the CPWs is equivalent—only the signal line doping layer and signal line lengths are different.

2. Experimental Section

2.1. Fabrication and DC Transport

The samples studied here were (001) oriented Si:P δ-layers, with a nominal phosphorus dopant areal density of 2.35×10^{14} cm^{-2}, or 0.35 monolayers (ML). Both samples were fabricated on a 2×9 mm^2 Si(001) die, with an active δ-layer area of 2×5 mm^2. The substrate was arsenic bulk-doped Si(001) with a thickness of 525 µm, resistivity of 14.95 Ω cm, corresponding to a background donor concentration of 3×10^{14} cm^{-3}, The P_{LTE} and P_{LL} δ-layers were fabricated by exposing an atomically clean Si(001) surface to PH_3 gas at room temperature. Following this saturating PH_3 dose, the samples were annealed at 350 °C to activate substitutional incorporation of the dopant atoms into the surface atomic layer, and then overgrown with 20 nm of intrinsic silicon using low temperature (250 °C) MBE and a deposition rate of 1.0 ML min^{-1}. The P_{LL} sample had a modified silicon overgrowth process, where a 10 ML room temperature, silicon "locking layer" was grown first, followed by a 15 s, 500 °C rapid thermal anneal, and then growth of the remaining 18.6 nm of silicon at a sample temperature of 250 °C. The "locking layer" step was introduced to improve the confinement of the phosphorus dopants and remove the segregation tail which extended from the δ-layer toward to the surface in the P_{LTE} sample, as seen in **Figure 2**. The 500 °C anneal improved the crystallinity of the locking layer region but cannot completely remove defects introduced by the growth of the locking layer. The expected DC transport properties were taken from Hall bars measurements at 1.8 K on δ-layers fabricated using the same process specifications. The P_{LTE} sample had a DC R_S of ≈670 Ω □$^{-1}$ and carrier density of $n_{2D} = 2.35 \times 10^{14}$ cm^{-2}, indicating full activation of the saturation phosphorous layer. The carrier mobility was $\mu = 40$ cm^2 V^{-1} s^{-1} giving a scattering time $\tau = 7.2$ fs. Dopant profiles from SIMS measurements are shown in Figure 2. It can be seen that the layers had expected

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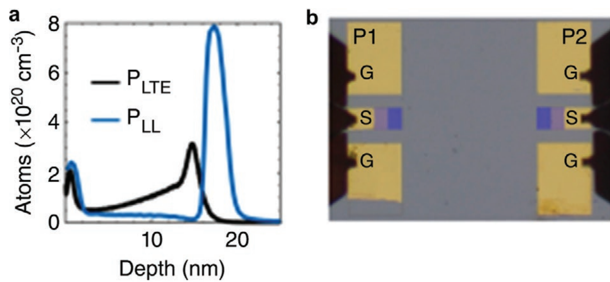

Figure 2. a) Secondary-ion mass spectrometry profiles of the phosphorous dopant densities of the doped monolayers. b) Micrograph of the ground–signal–ground (GSG) on-wafer probing for S-parameter measurements with the probes landed on a "open" reflect structure. Ports 1 and 2 are identified within the photo. The open structure is formed of the probing pads and the bilayer contact pads, as detailed in Figure 1. As before, the presence of a δ-layer is indicated by the blue shading.

full width half maximum thicknesses of 2.5 and 2.5 nm for the P_{LTE} and P_{LL} respectively. The P_{LTE} δ-layer had a 20 nm segregation tail that reached all the way to the silicon surface.

2.2. S-Parameter Measurements

The S-parameters of the δ-layers were obtained using an on-wafer two-port measurement between 4–26 GHz. To enable S-parameter measurements of the δ-layers, characterization structures were fabricated onto the sample, where the δ-layer was isolated within a CPW signal line. The signal line was contacted to probing pads to facilitate ground–signal–ground probing. The probing pad dimensions of the structure were chosen for a 50 Ω characteristic impedance to minimize reflections at the network analyzer port. The contact pads were both capacitively coupled and edge contacted to the δ-layer, using a 100 μm^2 overlap of the two metal sheets. Figure 2 shows the probing configuration on the "open" standard. In total, six characterization structures were fabricated on each sample with δ-layer CPWs of lengths 200, 400, 600, 800, 1000, 2000 μm and an "open" reflect standard. The structures were defined using photolithography. Reactive ion etching was used to complete an 80 nm etch to pattern the signal lines out of the δ-layer sheet, before evaporation processing techniques were used to deposit the metal probing and contact pads. A 100 nm gold layer was used to contact the δ-layers and to fabricate the ground planes with a 20 nm titanium adhesive layer. A hydrofluric acid etch was completed to remove the native silicon oxide layer before metal deposition.

S-parameters were measured at 4.5 K using a Lakeshore TTPX Cryogenic probe station combined with a Keysight N9918A Field Fox Analyzer and GGB 100 μm-pitch probes in an optically isolated environment. A thru-reflect-line calibration technique, using a Cascade Impedance Standard Substrate calibration substrate, was used to move the measurement reference plane to the probe tips.[39] An input power level of −15 dBm was used to prevent heating within the structures. The S-parameter data had been smoothed using a moving median method across ten data points for clarity due to a small oscillating background noise from the probe station.

2.3. Conversion of S-Parameters to γ and Z_C

The bilayer contacts required to access the embedded δ-doped layer prevented the implementation of standardized on-wafer calibration techniques.[40] Two techniques were used to analytically extract γ[41] and Z_C[23] of the δ-doped layers from the S-parameter measurements. A broadband continuous measurement was chosen to be used to extract γ from two similar uniform transmission lines of varying length. An equivalent technique was not available for extracting Z_C so instead the CPW measurements was de-embedded using a consistent "open" structure, formed of the two contact pad structures. This was a less rigorous technique as it had a higher dependence on continuity between the contact structures across the measured CPWs and coupling between the contact pads. Thus, it was not suitable for extracting the more sensitive γ value, particularly at high frequencies where the edge contact dominated. For γ, the S-parameters were converted into T-parameters (wave cascade matrices). The characterization structure T-parameters T_{CS} can be modeled in the form seen in Equation (1), where T_A and T_B represent at the contact pads at port 1 and 2, respectively and T_{CPW} represents the δ-layer CPW.

$$T_{CS} = T_A T_{CPW} T_B \tag{1}$$

By taking two uniform characterization structures of different CPW lengths l_1 and l_2, the T-parameters can be written as shown in Equation (2), where l_1 is the shorter line length. Using Equation (2), the eigenvalues of $T = T_{CPW_2} T_{CPW_1}^{-1}$ can be calculated and γ obtained.[41] For both samples, the δ-layer characterization structure with CPW length 200 μm was used as CPW_1.

$$T_{CPW_1} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix},\ T_{CPW_2} = \begin{bmatrix} e^{-\gamma(l_2-l_1)} & 0 \\ 0 & e^{-\gamma(l_2-l_1)} \end{bmatrix} \tag{2}$$

To find Z_C, the S-parameters were converted into Y-parameters (admittance matrices). In the low frequency approximation, the characterization structure Y_{CS} can be written as seen in Equation (3), where Y_{OPEN} is a structure formed of the probing and contact pads only, as seen in Figure 2b

$$Y_{CS} = Y_{CPW} + Y_{OPEN} \tag{3}$$

As Y_{CS} and Y_{OPEN} were known through measurements of the characterization and "open" structures, Y_{CPW} can be found through a simple subtraction. Through further conversion from Y-parameters to ABCD-parameters, which were of the form seen in Equation (4), Z_C can be determined through $Z_C = \sqrt{B/C}$. Conversions between the different electrical parameters can be found here.[42]

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma l) & Z_C \sinh(\gamma l) \\ \frac{1}{Z_C}\sinh(\gamma l) & \cosh(\gamma l) \end{bmatrix} \tag{4}$$

For reference, **Figure 3** shows γ extracted using the Y_{OPEN} calibration technique. In α there was a modified dependency at the higher frequencies, with a negative trend for both

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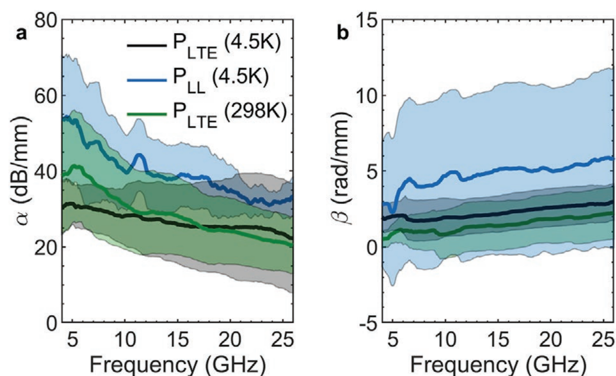

Figure 3. a) Attenuation and b) phase constant values shown for the two monolayers as extracted using the Y_{OPEN} technique, previously only used to extract Z_C. This fails at high frequencies due to high variability in the edge contact between the CPWs on each monolayer.

monolayers. The change in β was primarily in the magnitude with the P_{LTE} data showing a consistent v_p between extraction techniques. The greatest variance between γ extraction techniques was found for the P_{LL} monolayer CPWs, consistent with the higher confinement of the monolayer decreasing the size of the edge contact and reducing the size of the capacitive contact.

3. Results

3.1. S-Parameter Measurements

We characterized the CPWs at microwave frequencies by measuring the scattering parameters (S-parameters, S_{ij}) at 4.5 and 300 K using a probe station and a vector network analyzer. The S-parameters of the P_{LTE} CPWs at 4.5 K are shown in **Figure 4**. The reflection S_{11} and transmission S_{21} coefficients are the ratios of the output signal amplitude at the measurement port j to the input amplitude at the excited port i. The S-parameters show that there is a significant difference in microwave transmission through the δ-layer compared to the "open" structure. The S_{11} values are 0.5 dB lower than the "open" structure indicating

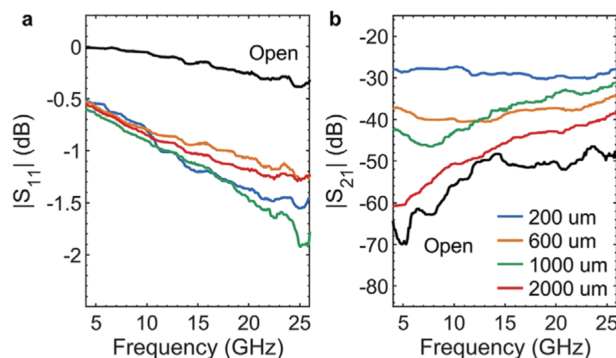

Figure 4. The S-parameters for the P_{LTE} Si:P δ-doped monolayer co-planar waveguides measured at 4.5 K of different lengths (see legend) and an "open" structure as a function of frequency. a) Magnitude of S_{11} and b) magnitude of S_{21}.

that the inclusion of the δ-layer induces a lower reflection at the port. S_{21} is a measure of the signal transmission along the δ-layer, and is observed to decrease in magnitude as the line length increases, approaching the lowest measured value for the "open" structure. This is evidence that the δ-layer is responsible for supporting propagation of the electromagnetic wave.

3.2. Transmission Characteristics

A transmission line can be defined by two characteristic parameters: the propagation constant $\gamma = \alpha + i\beta$ and the characteristic impedance Z_C. Both of the parameters are independent of the line length, but have a dependence on the CPW cross-sectional geometry. The parameters have been extracted from the experimental S-parameters (see Section 2.3) where the techniques used were selected to optimize the removal of the influence of the probing/contact pad. The resulting values of α, β, and Z_C averaged over multiple CPWs of different line length for each monolayer type are shown in **Figure 5**a–c. The shaded area indicates the standard deviation of the results for the different line lengths. Note that the extraction of γ involves the logarithm of a complex number which is sensitive to errors within the S-parameters, and produces correlations in the uncertainty in α and β. The fractional errors in α and β are therefore larger than for Z_C. The logarithm also produces a 2π wrapping in β which was manually removed by ensuring that β tends to zero at $\omega = 0$. The noise in S_{21} is not surprising as low dB measurements suffer from the logarithm. The lower amplitude noise in the S_{11} measurements however, is somewhat larger than expected, and is likely systematic, originating in the probe tips placement (see Section 2.2). In addition to the 4.5 K measurements, Figure 5 also includes data from the P_{LTE} monolayer sample at room temperature—we save the discussion of this for Section 3.4.

The standard deviations for each monolayer type shown in Figure 5 are dominated by variations in the fabrication of each CPW, especially the contacts. Although the analysis techniques that convert the S-parameters into the propagation and impedance characteristics are intended to remove the effect of contacts, they require that the contacts are identical between CPWs of the same monolayer type, which can produce some limitations. For example, the higher magnitude in α for the P_{LL} monolayer indicates that the P_{LL} has a less reliable resistive edge contact, likely due to the reduced thickness of the dopant layer.

The complex propagation constant for a transmission line comprises a real part (the attenuation constant) and an imaginary part (the phase constant). The attenuation constant α is the fractional decrease in signal amplitude along the transmission line per unit length, with an ideal lossless transmission line having $\alpha = 0$. The phase constant is defined as $\beta = \omega / v_p$, where $\omega = 2\pi f$ is the angular frequency and v_p is the propagating phase velocity. Assuming a thin planar CPW structure, that is, negligible thickness for both the ground planes and the signal line and a geometry where all the metallic layers sit within the same horizontal plane, $v_p = c/\sqrt{\varepsilon_{eff}}$. ε_{eff} is the effective relative dielectric permittivity of a CPW, which is given by[43]

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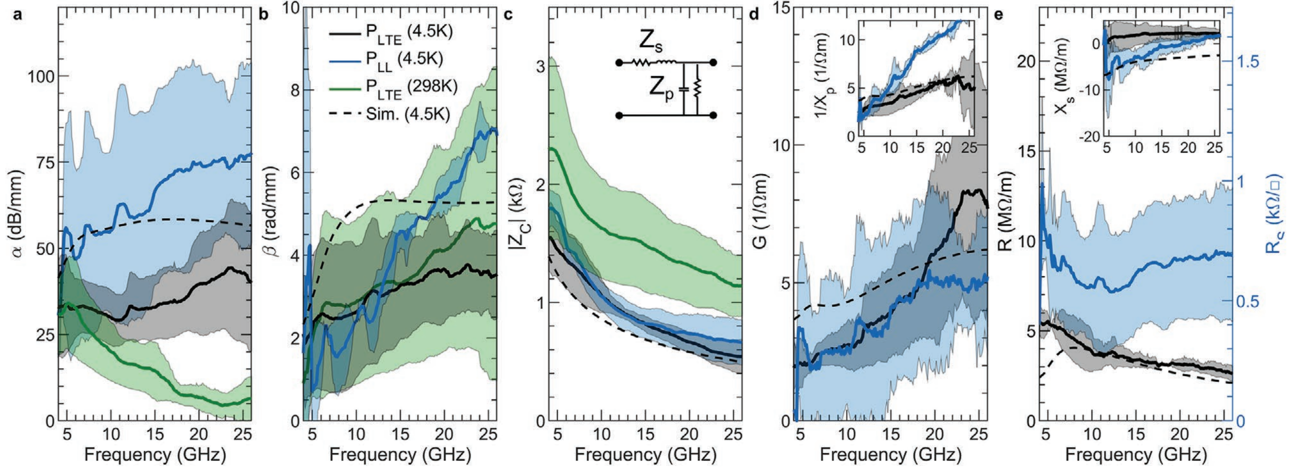

Figure 5. Characteristic transmission line properties for the different layer materials; P_{LTE} (black) and P_{LL} (blue) measured at 4.5 K and for P_{LTE} at room temperature (green). The properties shown are the a) power attenuation constant α and b) phase constant β, c) the characteristic impedance Z_C. An EM planar simulation (as described in the text) of the P_{LTE} structure is shown in each as a dashed line. The inset in (c) is the lumped element model for a transmission line. d) Main panel: $Re(1/Z_p) = Re(\gamma/Z_C) = G$, inset: $Im(1/Z_p) = Im(\gamma/Z_C) = 1/X_p$. e) Main panel $Re(Z_s) = Re(\gamma Z_C) = R$, inset $Im(Z_s) = Im(=\gamma Z_C) = X_s$. The secondary axis for (e) shows the sheet resistance R_s. The error bars represent a single standard deviation of the parameters extracted from the set of multi-length lines for each monolayer.

$$\varepsilon_{\mathrm{eff}} = 1+\frac{(\varepsilon_R-1)}{2}\frac{K(k_1)}{K(k'_1)}\frac{K(k'_0)}{K(k_0)} \tag{5}$$

where K is the complete elliptic integral of the first kind, $k_0 = (1 + 2g/w)^{-1}$, $k_1 = \sinh(\pi w/4h)/\sinh(\pi(w + 2g)/4h)$, $k' = \sqrt{1-k^2}$, $\varepsilon_R = 11.7$ is the expected silicon permittivity at 4.5 K, and c is the speed of light. If $h \gg w$, $w + 2g$, as in our case (Figure 1), then $k_1 \approx k_0$ hence $\varepsilon_{\mathrm{eff}} \approx (\varepsilon_R + 1)/2 = 6.2$. Therefore, we expect $v_p = c/\sqrt{\varepsilon_{\mathrm{eff}}} = 12.0\times10^7\ \mathrm{m\ s^{-1}}$ for a CPW mounted on silicon, which displays reasonable agreement with the extracted value from the gradient of the P_{LTE} transmission line, $v_p \approx (9.2\pm0.2)\times10^7\ \mathrm{m\ s^{-1}}$.

The Z_C of a transmission line is defined as the input impedance the line would have if it were of infinite length. The cross-sectional geometry of the probing pads and CPW were designed for $Z_C = 50\ \Omega$ assuming a low loss line. This design allows characterization of the unknown δ-layer impedance when it is incorporated as the signal line. The magnitude of Z_C is shown in Figure 5c for the P_{LTE} and P_{LL} δ-layer CPWs. Both monolayers show Z_C of a similar magnitude and a simple montonically decreasing dependence on applied frequency. The lower characteristic impedances at high frequencies (approaching closer to the desired 50 Ω) indicate lower port reflections, and easier incorporation of δ-layer CPWs into a device design if they are intended for higher frequency operation.

In addition to the actual transmission measurements, microwave transmission in a P_{LTE} δ-layer transmission line was also successfully simulated using Sonnet Software Inc's planar electromagnetic simulator.[44] The results of this calculation are shown as dashed lines in Figure 5. In this simulation we took the experimental DC R_S 670 Ω □$^{-1}$ (see Section 2.1) and an estimated substrate resistivity of 1000 Ω cm.[45] The simulation produces frequency dependent S-parameters that can be analyzed in the same way as the experiment to extract Z_C and γ. There is an excellent match with the experimental results for Z_C with the simulated results sitting comfortably within twice the standard deviation of the measured data, with the results for α and β showing the correct trends and magnitudes.

3.3. Lumped Element Model

In order to further understand the results for γ and Z_C we consider a lumped element circuit model formed of a series complex impedance per unit length Z_s and parallel complex leakage per unit length Z_p, arranged as depicted in Figure 5c. In this model, the line losses are contributed by $Re(Z_s) = R \approx R_S/w$, the resistance per unit length of the metallic signal line and $Re(1/R_p) = G \approx 1/gR_{SS}$, the parallel leakage conductance per unit length. Here, R_{SS} is the resistivity of the substrate, that is, G arises from the imaginary part of the dielectric response of the substrate. The dimensions w and g are defined in Figure 1. In an ideal line, $R \approx G \approx 0$. Furthermore, it is expected that $Im(1/Z_p) = 1/X_p = \omega C$ is the electrostatic capacitance, and that $Im(Z_s) = X_s = \omega L$ is the mutual inductance, where both reactances are predominantly defined by the CPW geometry per unit length. From this model

$$Z_s = R + i\omega L = \gamma Z_C \tag{6}$$

$$1/Z_p = G + i\omega C = \gamma/Z_C \tag{7}$$

The lumped element model is valid when the transmission line dimensions are much smaller than $\lambda_0/\sqrt{\varepsilon_{\mathrm{eff}}}$ where λ_0 is the free-space wavelength. From the prior estimated value of $\varepsilon_{\mathrm{eff}} = 6.2$, we state that the lumped element model is reasonable for our CPWs when $f \ll 60$ GHz.

From Equations (6) and (7), it is trivial to find the real and imaginary parts of Z_s and $1/Z_p$ from γ and Z_C in order to obtain R, G, X_s, and $1/X_p$, as shown in Figure 5d,e. Figure 5e shows that the P_{LTE} has a DC $R_S = wR \approx 500\ \Omega$ □$^{-1}$ in good agreement with typical DC single dose Si:P δ-layer values from elsewhere.[33]

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The P_{LL} sample has larger experimental sheet resistances above 700 $\Omega\,\square^{-1}$. This can be attributed to the room temperature "locking layer" fabrication step, where the higher confinement of the doping increases the ionized impurity scattering probability. In addition, the encapsulating "locking layer" was grown at room temperature to suppress thermal segregation of the donors, thus we would expect lower carrier activation, and higher density of crystal defects which can serve as additional scattering centers. In Figure 5d, despite the high substrate resistance expected at 4.5 K as the impurities freeze out, there is still a significant dielectric loss for both monolayers types, with G increasing monotonically with frequency. The agreement between the simulation and the P_{LTE} data here, not only in the absolute magnitudes of the values but also the general trends is remarkable, with the simulation replicating the loss trends within the monolayer CPW at microwave frequencies.

As mentioned before, C and L are expected to be primarily geometry dependent and thus to be similar between the two monolayers. Within the thin planar CPW approximation, which assumes a simplified geometry,[43] simple equations can be obtained for the capacitance and inductance per unit length as

$$C_E = 4\varepsilon_{eff}\,\varepsilon_0 \frac{K(k_0)}{K(k'_0)} \tag{8}$$

$$L_M = \frac{\mu_0}{4}\frac{K(k'_0)}{K(k_0)} = \frac{\varepsilon_{eff}}{c^2 C_E} = \frac{1}{v_p^2 C_E} \tag{9}$$

producing C_E = 160 pF m^{-1} and L_M = 440 nH m^{-1}. From the inset figure in Figure 5d, assuming that $Im(1/Z_p) = 1/X_p = \omega C$ we extract for the P_{LL} sample $C = (83 \pm 3)$pF m^{-1}, which gives $\omega C = 5.2\ \Omega^{-1}$ m^{-1} at 10 GHz. The extracted C value for the P_{LL} monolayer is in reasonable agreement with the theoretical C_E (within a factor of two), and that for the P_{LTE} sample is within a factor of four. We take this to be an indication of the size of the uncertainty in the fabrication/measurement, perhaps because the theoretical K term produces a smaller geometrical contribution to C_E than found in the experimental CPW structure. The thin planar CPW approximation assumes that $t \ll \delta_S$ and that the ground planes and signal lines are within the same plane, which would produce a reduced electromagnetic geometry, and hence a smaller K. At 20 GHz we would expect $Im(Z_s) = X_s = \omega L_M$ to be on the order of 0.01 M Ωm which is much smaller than the axis scale of the Figure 5e inset. This indicates the presence of an unexpected reactance that is large compared to ωL_M of the CPW. Furthermore, the X_s data is both negative and inversely proportional to ω, which implies it could originate from either a stray series capacitance or perhaps, an inductive coupling between the measurements ports in parallel with the relatively high impedance CPW. Given that the EM simulation also shows the same effect, it seems likely that this is due to the inductive coupling. The coupling is a geometric effect due to the short CPW lengths where the pairs of probing pads are relatively close together. The stray reactance appears larger for the P_{LL} monolayer, presumably due to the higher R_S of the monolayer and a reduced L_M term from the increased geometrical confinement.

3.4. Room Temperature Measurements

The CPW characteristics described above were measured at 4.5 K as this approaches the working regime of silicon-based single atom devices. We also replicated the study at room temperature, to assess the versatility of δ-layers for application to CMOS technologies. Figure 5a–c includes the characteristic parameters of the P_{LTE} δ-layer CPWs under room temperature. The room temperature P_{LTE} CPW has the highest Z_C and the lowest α. At higher temperatures, the resistance of a metal is expected to increase due to damping from phonon scattering leading to a higher Z_C values. As discussed in the Section 2.1, the substrate is heavily doped with the higher temperatures producing an increase in carrier concentration through both donor ionization and intrinsic thermal carrier generation, leading to an almost metallic regime at room temperatures. At higher frequencies, eddy currents will be induced within the substrate, reducing R_{SS} producing the negative dependence of the attenuation constant on the frequency seen in Figure 5a. It is useful to note that the P_{LTE} monolayer at room temperature shows contrasting error behavior to the P_{LL} sample, with the smallest, and largest standard deviations in α, and β, respectively. This corroborates our conclusion that variation of the thickness of the metallic layer within the contact is the primary contribution to the deviations. At room temperatures, the ionization of the donors induces an extended monolayer thickness and thus a larger edge contact, and higher variations in the reduced capacitive contact.

The influence of the substrate upon the propagation characteristics of the monolayer transmission lines could be reduced by incorporating commercial silicon-on-insulator CMOS wafers which have an insulating layer of SiO_2 which isolates the metallic layer from the doped substrate suppressing leakage into the dielectric. Electromagnetic simulations at room temperature have indicated a 14% reduction in α for the inclusion of a 5 µm SiO_2 layer directly below the phosphorous monolayer.

4. Discussion

We are not aware of any experimental values for γ and Z_C reported for graphene, even though experiments similar to those presented here have been performed at room temperature. This is presumably due to the limited sizes of graphene flakes available, with CPW dimensions on the order of 20–100 µm making it difficult to assess the transmission line parameters. Instead, the S-parameters are matched to an extended equivalent lumped element model and a R_S extracted, with R_S values of 910 $\Omega\,\square^{-1}$[5] and 250 $\Omega\,\square^{-1}$.[8] The R_S values demonstrated here for Si:P δ-layer CPWs compare favorably with these graphene values. Additionally, we have shown that Si:P δ-doped layers fabricated using phosphine doping and molecular beam epitaxy support electromagnetic transmission at microwave frequencies at both 4.5 K and room temperatures. The excellent agreement between the simulation and the experiment suggests that simple material and geometrical parameters can be used to predict the transmission properties, at least for micron-scale CPWs. The δ-layers have transmission characteristics that suggest promising suitability for application as interconnects with microwave transmission capabilities. The differentiation between the transmission characteristics of the phosphine δ-layer CPWs shows preferable behavior for the monolayer fabricated without a "locking layer," due to the higher mobilites and carrier concentrations within the P_{LTE}

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monolayer. Next steps look toward implementing δ-layers within practical technologies. Standard planar electromagnetic simulations have shown to be a good match to measured data, meaning we can design and optimize future geometries and studies of nanoscale interconnects. Further work would benefit from a more consistent contacting structure, independent of thickness and dopant variations in the monolayer such as a palladium silicide contact[46] or a series of vias.[47] The delta-doped layers have electrical characteristics similar to graphene which has been extensively investigated for low-dimension interconnects. We propose δ-doped layers as an alternative to graphene for nanoscale interconnects as they are supported by advanced fabrication techniques that can produce deterministically positioned nano-structures, exhibit a resistivity unaffected by nanoscale geometries, and are CMOS compatible.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

G.C., S.K.C., and P.H.A. proposed the experiments. G.C. performed the S-parameter measurements with assistance from H.V. G.C., H.V., P.H.A., and B.N.M. analyzed the data. T.J.Z.S. and N.J.C. fabricated and provided the samples. G.C., T.J.Z.S., S.K.C, P.H.A., and B.N.M. wrote the paper.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

delta-doped layer, microwaves, phosphorus, silicon, transmission line

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