A Multi-Channel Stimulator With High-Resolution Time-to-Current Conversion for Vagal-Cardiac Neuromodulation

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***Abstract*—This paper presents a low power integrated multi-channel stimulator for a cardiac neuroprosthesis designed to restore the parasympathetic control after heart transplantation. The proposed stimulator is based on time-to-current conversion. It replaces the conventional current mode digital-to-analog converter (DAC) that uses tens of microamps for biasing, with a novel capacitor time-based DAC (CT-DAC) offering about 10-bit current amplitude resolution with a bias current of only 250 nA. A stimulator chip was designed in a 0.18 µm CMOS high-voltage (HV) technology. It consists of 16 independent channels, each capable of delivering up to 550 µA stimulus current with a HV output stage that can be operated up to 20 V. The stimulator chip performance was evaluated using both RC equivalent load and a microelectrode array in saline solution. It is power efficient, provides high-resolution current amplitude stimulation, and has good charge balance. The design is suitable for multi-channel neural stimulation applications.**

***Index Terms*—Digital-to-analog converter (DAC), heart transplant, high voltage neural stimulator, implantable devices, time-to-current converter, vagus nerve stimulation.**

I. Introduction

Every year over 3000 heart transplantation surgeries are conducted worldwide. Surgery is the last resort for a patient who is at the end-stage of heart failure. Because of the complexity involved during the surgery, denervation is inevitable and causes the transplanted heart to function without any parasympathetic control. By innervating the sinoatrial and atrioventricular nodes, the parasympathetic control functions to slow the heart rate and relax the heart [1]. Parasympathetic control is facilitated by the vagus nerve for cardiac activity modulation; denervation means this connection is lost between the patient's vagus nerve and the donor heart which is only controlled by the circulation catecholamines. Therefore, even though heart transplantation can extend the life expectancy of patients, health-related problems remain due to cardiac denervation. Related chronotropic incompetence not only affects the exercise capacity and health-related quality of life but also leads to long-term complications.

To re-bridge this neural link, a cardiac neuroprosthesis is required as shown in the conceptual diagram in Fig. 1. Here, an active regenerative electrode with a multi-channel stimulator chip for artificial vagus control is proposed. The regenerative neural interface is designed to provide guided nerve regeneration [2], [3]. Once the nerve is regenerated, the neuroprosthesis could facilitate cardiac-vagal re-connection by providing multi-site stimulation. With both the re-connection of the vagus nerve and 'grafting' of the electrode stimulation capability, the parasympathetic control would be reinstated.

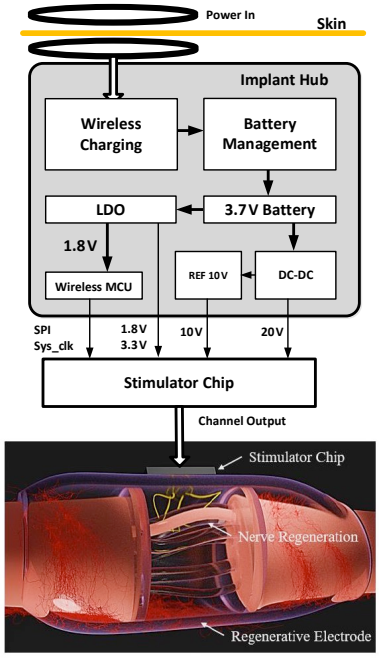

Fig. 1. Concept of cardiac neuroprosthesis with a regenerative active electrode array for vagal-cardiac reconnection.

The entire system consists of an implant hub providing power and communication to the active site where the stimulator chip is located, as shown in Fig. 1. This paper focuses on the design of the neural stimulator chip. A simple time-to-current digital-to-analog (DAC)-based stimulator is proposed. The stimulator has a time-to-current conversion rate of 74.2 nA per DAC clock cycle, controlled by a 15 MHz timing clock achieving about 10-bit DAC resolution. With four current scaling options, it can

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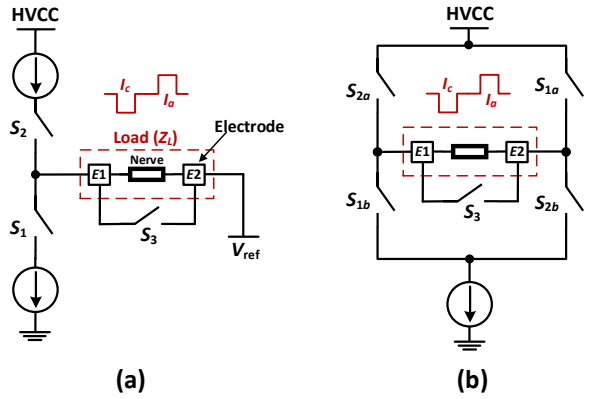

Fig. 2. Stimulator output stage topologies for generating biphasic current pulses (I_a and I_c). (a) Using a source-sink current driver pair. (b) Using a single current driver with an H-bridge.

output a maximum stimulus current (I_{stim}) of 550 µA from a 20 V high-voltage (HV) supply. The DAC uses only 250 nA biasing current. The total power consumption during biphasic stimulation is dynamic but the static power is only 23.3 µW.

The proposed 16-channel time-to-current stimulator design provides high resolution stimulus currents with independent channel control. It is also power efficient and scalable for multi-channel stimulation. The rest of the paper is organized as follows. Section II outlines the stimulator design considerations and Section III describes the circuit details of the various system blocks. Section IV presents measured results from the fabricated stimulator chip implemented in a 0.18 µm CMOS HV technology, including testing with a cardiac microelectrode array in saline solution. Concluding remarks are drawn in Section V. The paper expands on the preliminary design reported in [4].

II. Stimulator Design Considerations

A conventional constant current neural stimulator fundamentally consists of a programmable current driver. It delivers current pulses between a pair of electrodes connected to the targeted nerve where neural responses are elicited by a stimulus current ranging from tens of microamperes (µA) to tens of milliamperes (mA) [5]. Numerous integrated stimulator designs have been reported; they typically comprise of two main parts:

(i) A DAC to generate the desired current amplitude. This often uses a current mirror-based DAC (I-DAC) whose output current is multiplied/mirrored to the output stage for biphasic stimulation [6].

(ii) An output stage that connects to the electrodes for stimulation. There are two common approaches to generate biphasic current stimulation [7]; either a source-sink current driver pair [8] as shown in Fig. 2(a), or a single current driver with an H-bridge [9] as in Fig. 2(b).

An implantable stimulator must account for the following two design considerations [10]:

1) Low Power Consumption – Over the years, with an increasing demand for spatial resolution in neural interface microsystems, the number of electrodes has been increasing while the size of each electrode has been significantly

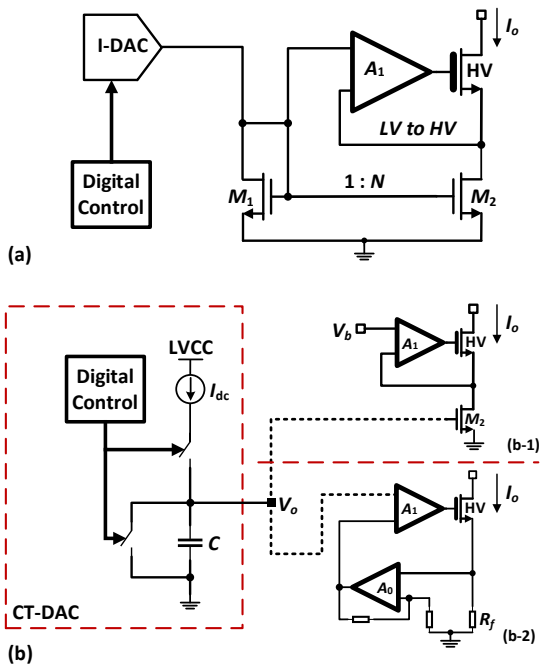

Fig. 3. (a) Conventional stimulator based on I-DAC. (b) Proposed time-to-current converter stimulator topology using CT-DAC; (b-1) Design option 1, (b-2) Design option 2.

decreasing. This leads to unavoidable high load impedances (in the region of tens of kΩ) that the stimulator must drive [11]. Hence, the output stage of the stimulator is often designed with HV transistors or low-voltage (LV) transistor stacks [12], [13] to provide enough voltage compliance. Given the strict power constraints imposed on implantable devices, state-of-the-art neural integrated stimulators are required to drive multiple channels and operate power-efficiently. For example, using dynamic HV supplies [14] or merging the I-DAC directly into a HV output stage at the expense of chip area [15], [16].

Although the HV output stage other requires unavoidable high-power consumption, power optimization can be achieved in the LV stage. A conventional high-resolution I-DAC design, for example, a 10-bit I-DAC with a 250 nA LSB would consume up to 256 µA. In addition, the transistors in the layout must be scaled up from the minimum size transistor by a maximum of 1024. Allocating one DAC per stimulator channel in a multi-channel design is challenging. Thus, for multi-channel stimulators either DAC sharing is adopted [6] or multiple low-resolution (≤8-bit) DACs are often employed [14], [17]-[21] and calibration may be required to achieve good DAC performance [22].

2) Charge Balance – For safe stimulation a balanced biphasic current pulse is required; the total charge injected by the cathodic current phase must equal to the total charge removed by the anodic current phase. Any excess residual charge which builds up on the neural interface would potentially not only cause electrolysis at the electrodes but also damage the tissue [23].

Using the single current driver (which requires only one HV transistor) with an H-bridge [Fig. 2(b)] to generate biphasic current pulses provides good current matching characteristics and is simple to implement. However, for multi-channel

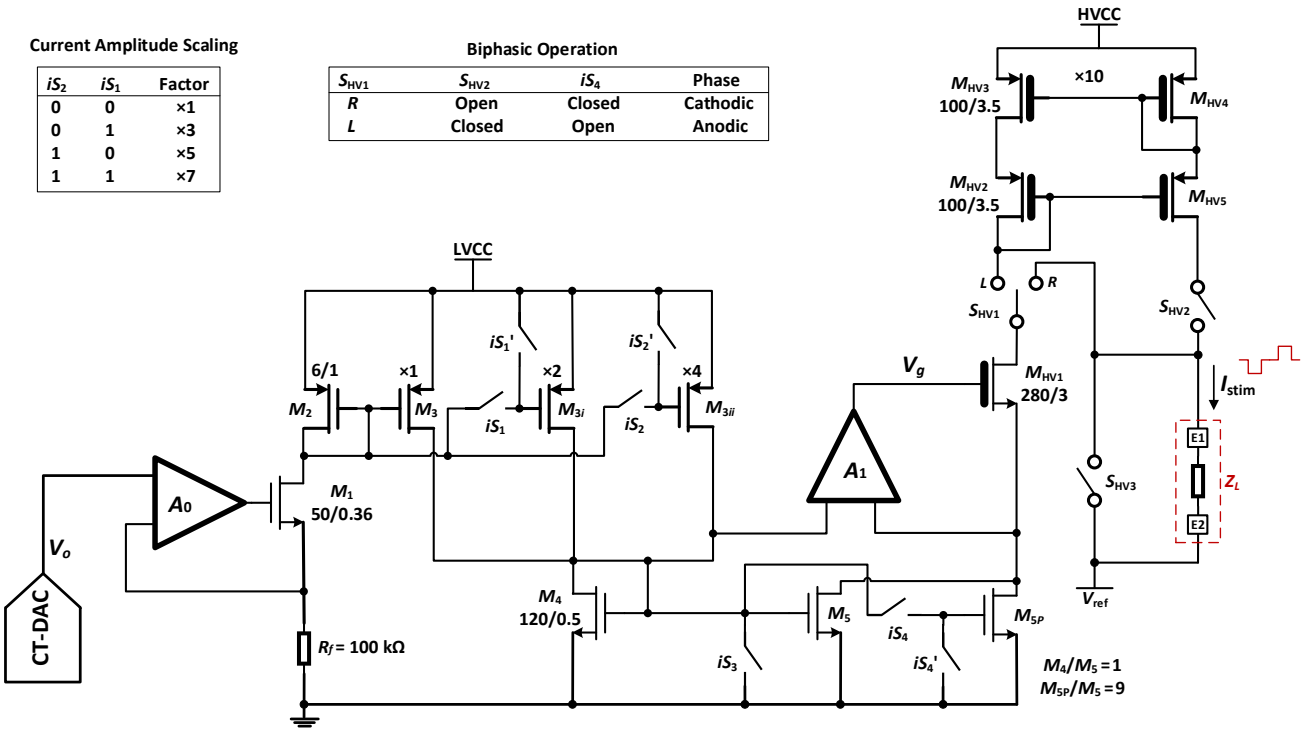

Fig. 4. The output stage of the neural stimulator. M_{HV} transistors and S_{HV} switches are high voltage. All other devices are low voltage.

stimulation in order to reduce electric crosstalk, time multiplexing [24] or power isolation [25] is required.

The source-sink topology [Fig. 2(a)] is more suitable for driving multiple channels, but it suffers from CMOS fabrication induced current mismatches which limit the resolution of the DAC. Electrode discharging is often required to remove any residual charge by either actively sending extra short-burst current pulses or temporarily passively shorting the electrodes together [facilitated by switch S_3 in Fig. 2(a) and (b)] after each biphasic pulse for better charge balancing [26].

III. Stimulator Design

A. Voltage-to-Current Converter

The proposed design employs a new DAC principle that is power efficient, simple to implement and scalable for multi-channel stimulators. In the conventional design shown in Fig. 3(a), from a I-DAC a desired current amplitude is generated and then scaled up by the current mirror (LV transistors M_1 and M_2) to generate I_o. For HV operation, a cascode HV transistor under the bias control of opamp A_1 is added. This active feedback clamps the drain voltage of M_2, and not only provides reliable current mirroring and high output impedance, but also couples the LV MOS to the HV MOS to drive a large impedance load.

An alternative is shown in Fig. 3(b). By controlling the charging period of a capacitor, the desired voltage, previously supplied by a conventional I-DAC with multiple current branches, can instead be generated by simply charging the capacitor with a small constant dc current (I_{dc}), hence implementing a capacitor-charge time-based DAC (CT-DAC). In the CT-DAC, the relationship between charging time and voltage developed across the capacitor is essentially linear. The time-to-current control can be quite simple if the voltage-to-current conversion also has a linear relationship.

There are several options to couple the output voltage (V_o) of the CT-DAC to the stimulator output stage:

(i) As shown in Fig. 3(b-1) by directly using the output voltage from the CT-DAC to bias, for example, the gate of transistor M_2 offers a more power efficient design than Fig. 3(a). If M_2 is biased in the triode region, the circuit is effectively a voltage-to-current converter with a linear transfer function of $I = V_b/R_{M_2}$, where V_b is a fixed bias voltage and R_{M_2} is the equivalent resistance of M_2 which varies according to the output voltage V_o of the CT-DAC. The non-linearity of the MOS resistor M_2 is an inaccuracy requiring extra compensation [27].

(ii) A method to implement a voltage-to-current converter with better linearity is shown in Fig. 3(b-2) [4]. It uses a fixed-value resistor R_f instead of MOS resistor and applies the CT-DAC voltage to the active feedback opamp A_1. This option has a linear output current transfer function:

$$I_o = V_o \frac{g_{m_{\mathrm{HV}}} A_{ol}}{1 + g_{m_{\mathrm{HV}}} A_{ol} G R_f} \approx \frac{V_o}{G R_f} \qquad (1)$$

where $g_{m_{\mathrm{HV}}}$ is the transconductance of the HV transistor, A_{ol} is the open loop gain of A_1 and G is the gain of the non-inverting amplifier using opamp A_0. With the non-inverting amplification, the clamped source voltage of the HV transistor can be G times smaller than V_o, offering higher voltage compliance but at the expense of power consumption due to the added opamps to drive the HV transistor.

(iii) An improved implementation is shown in Fig. 4. By placing the voltage-to-current converter on the LV side, the source of transistor M_1 can be clamped at higher voltage levels

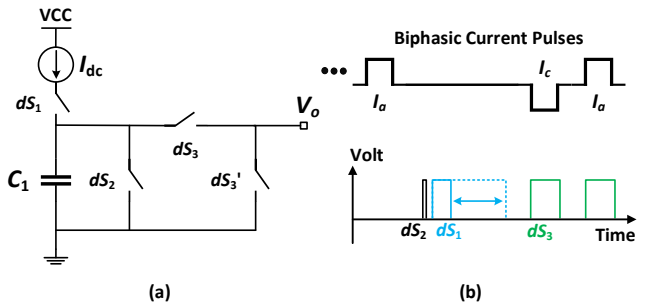

Fig. 5. (a) One capacitor implementation of CT-DAC. (b) Switch timing diagram.

[compared to Fig. 3(b-2)], providing a wider dynamic range for the CT-DAC. A simple feedback loop has a wider bandwidth and moderate power consumption. R_f can be large (e.g., 100 kΩ) for low-power operation. The drain current of M_1 can be scaled by different factors with the intermediate stage ($M_2, M_3, M_{3i}, M_{3ii}$) according to the 'current amplitude scaling' table in Fig. 4.

To generate the cathodic phase of a biphasic pulse, the HV switch S_{HV1} is connected to position R, and transistors M_5 and M_{5P} (with iS_4 closed) provide the cathodic current (S_{HV2} is open). The current flows from the common return electrode $E2$ to electrode $E1$. For the anodic phase, S_{HV2} is closed, S_{HV1} is changed to position L, and the HV PMOS current mirror ($M_{\mathrm{HV2}} - M_{\mathrm{HV5}}$) provides the anodic current from $E1$ to $E2$. In the anodic phase, the gate of M_{5P} is grounded (by switching on iS_4'), and the drain current of M_{HV1} is equal to that of M_4. It is scaled up by a factor of 10 by the $M_{\mathrm{HV2}} - M_{\mathrm{HV5}}$ current mirror. This is used to save power in the M_{HV1} branch during the anodic phase. To discharge the electrodes in the discharge phase, S_{HV3}, iS_3 and iS_4' are closed.

As an example, for a maximum cathodic current of 500 µA, with a scaling factor of ×70 (M_2 to $M_3/M_{3i}/M_{3ii}$ times M_4 to M_5/M_{5P}), M_1 is required to conduct a drain current of 7.15 µA. It is sized to account for the maximum voltage provided by opamp A_0 (<1.8 V) to provide 715 mV across R_f = 100 kΩ. The same consideration applies to the sizing of M_{HV1}; it is required to support 500 µA under a limited gate-to-source voltage. Voltage V_g provided by A_1 is limited by the available 3.3 V supply. The source voltage of M_{HV1} is determined by the sizing of M_5 and M_{5P}. Other considerations in relation to the sizing of the transistor include the available voltage, voltage compliance and layout area. The HV transistor dimensions are labeled in Fig. 4. Note that the maximum stimulator output current is also determined by the maximum output voltage (V_o) provided by the CT-DAC.

B. Time-to-Voltage Converter

The basic CT-DAC circuit implementation is shown in Fig. 5(a) [4] with the corresponding digital control timing diagram in Fig. 5(b). There are two issues with this implementation:

(i) For asymmetrical biphasic pulses (beneficial for stimulation efficacy [19]), the charge on the capacitor in the CT-DAC must be recharged during the interphase delay. For short interphase delays this may be difficult.

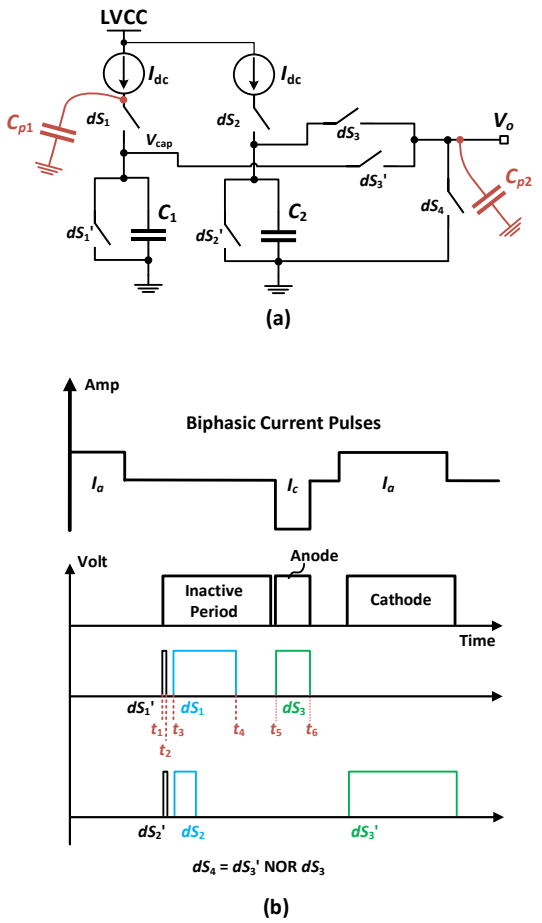

Fig. 6. (a) Implementation of improved CT-DAC with two capacitors. (b) Switch timing diagram.

(ii) The voltage-to-current converter in Fig. 3(b-2) used in [4] may need its input reset to ground (depends on its bandwidth) by closing dS_3' during the pulse interphase delay. Hence, charge sharing between the CT-DAC capacitor and the input parasitic capacitance of opamp A_1 happens twice, resulting in different V_o for a supposedly equal biphasic current output, lowering the bit resolution.

An improved CT-DAC design is shown in Fig. 6(a). It uses two capacitors that can be charged to different voltage levels for asymmetrical biphasic current outputs with the same dc current I_{dc}. Fig. 6(b) shows the timing control diagram. After dS_1' and dS_2' reset capacitors C_1 and C_2, they can be charged to different voltages according to the ON times of dS_1 (T_{dS_1}) and dS_2 (T_{dS_2}) during the inactive period. Then dS_3 and dS_3' select which voltage is applied to opamp A_0. The overall digital system operates under a 1 MHz master clock, and the charging period is controlled by another CT-DAC clock. In this design, the capacitor was 25 pF and the charging current I_{dc} was 250 nA. This is the total bias current required for the CT-DAC. The voltage developed across each capacitor is given by:

$$V_o = I_{\mathrm{dc}}\left(T_{dS_i}/C_i\right). \qquad (2)$$

For example, consider a 15 MHz CT-DAC clock with a 10-bit current amplitude counter. In each clock cycle the capacitor

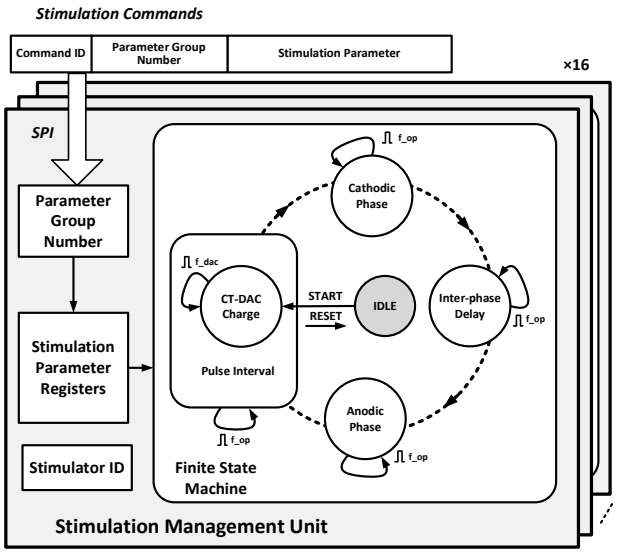

Fig. 7. The digital control for stimulator multi-channel management.

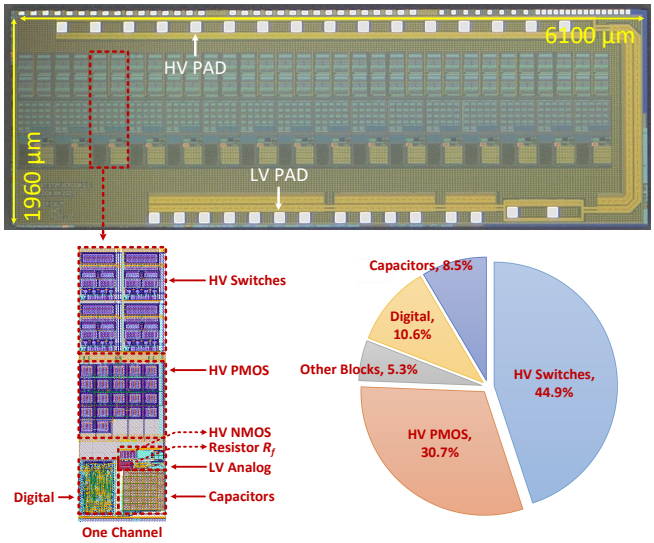

Fig. 8. Stimulator chip microphotograph and details of a single channel. The layout area breakdown is also shown. 'Other blocks' include the low-voltage analog circuits, feedback resistor R_f and HV NMOS M_{HV1}.

charges up by 667 µV, leading to a maximum output voltage V_o of 682 mV. For $R_f = 100$ kΩ, the drain current of M_1 is 6.82 µA, and with a scaling factor of ×70 yields a maximum stimulator output current of 478 µA. This translates to an LSB output current of 66.7 nA per CT-DAC clock cycle (the other 3 scaling factors shown in Fig. 4 provide different LSB output current values). In addition, other CT-DAC clock frequencies can be used leading to different LSB values, hence simple adjustment of the current resolution.

Charge injection and charge sharing will affect the voltage developed on the capacitor (V_{cap}) in the CT-DAC. This can be examined using the timing diagram in Fig. 6(b):

(i) Before t_1, $dS_1{}'$ and dS_1 are open, and the parasitic capacitor C_{p1} shown in Fig. 6(a) is charged to LVCC.

(ii) From t_1 to t_2, $dS_1{}'$ resets the voltage on C_1 to ground and opens at t_2. As $dS_1{}'$ opens, the charge injection ΔQ from $dS_1{}'$ is transferred to C_1. It is approximately:

$$\Delta Q \approx \frac{1}{2}\left[W_n L_n C_{\mathrm{ox}}\left(V_{\mathrm{control}} - V_{\mathrm{in}} - V_{thn}\right) - W_p L_p C_{\mathrm{ox}}\left(V_{\mathrm{in}} - \left|V_{thp}\right|\right)\right] \quad (3)$$

where V_{control} is the control signal applied to the gate of the switch, V_{in} is the input signal to the switch, and the other symbols are the conventional notations for a standard CMOS transmission gate switch. As shown, ΔQ is V_{in} dependent; in simulation, when V_{in} of $dS_1{}'$ is 0 V at t_2, $\Delta Q_{dS_1{}'} = 3.5$ fC. This charge injection will be the same for all the CT-DAC charging cycles.

(iii) As dS_1 closes at t_3, charge sharing happens between C_1 and the parasitic capacitor C_{p1}. Hence, prior to any current charging, there will be an initial voltage on C_1 due to $\Delta Q_{dS_1{}'}$, and the stored charge on C_{p1}. The initial voltage is constant for all the charging cycles, and in simulation, this voltage was around 2.5 mV ($C_1 = 25$ pF).

(iv) As dS_1 opens after the charging of the CT-DAC is completed at t_4, its charge injection ΔQ_{dS_1} is transferred to C_1. From (3) it can be seen that a net-zero ΔQ occurs at $V_{q0} = V_{\mathrm{control}}/2$ ideally, and as V_{in} moves away from V_{q0} (which from simulation was around 0.5 V) ΔQ_{dS_1} increases. Hence, in any CT-DAC operation, one equivalent LSB charge on C_1 must be larger than 3.5 fC, which is the worst-case for ΔQ_{dS_1} when $V_{\mathrm{in}} = 0$ V. This is the only critical charge injection that must be accounted for in the design. Using a 15 MHz CT-DAC clock, a charging current of 250 nA for 10-bit resolution causes a LSB charge of 16.7 fC (4.76 times 3.5 fC). The value of C_1 is dictated by the maximum CT-DAC output voltage for 10-bit resolution.

(v) When dS_3 closes at t_5, charge sharing happens between capacitors C_1 and parasitic capacitor C_{p2}. As dS_4 always resets C_{p2} to ground, and the final CT-DAC output is $V_o = C_1 V_{\mathrm{cap}}/(C_1 + C_{p2})$. This does not affect the CT-DAC resolution because C_{p2} is the same for each stimulator channel. Mismatches, for example, between C_1 and C_2 can be minimized by careful layout design.

(vi) When dS_3 opens at t_6, its charge injection is no longer relevant. Subsequently a new cycle can begin.

The charge on capacitors C_1 and C_2 must ideally be held constant after dS_1 or dS_2 have been turned off to the end of its corresponding pulse duration (when dS_3 or $dS_3{}'$ turn off); see Fig. 6(b). Charge leakage should be considered. A 15 MHz CT-DAC of 10-bit resolution, results in a 68.2 µs inactive period. For a pulse width of 100 µs, when holding one LSB of charge the worst case is losing half the LSB on C_2 (at the end of the anodic phase) over 268 µs. This results in a maximum allowable leakage current of $Q_{\mathrm{LSB}}/t = 0.5(16.7\ \mathrm{fC}/268\ \mu\mathrm{s}) \approx 31.2$ pA for a 250 nA CT-DAC charging current.

C. Stimulator Digital Control

For the targeted application requiring multi-channel stimulation, 16 stimulators were implemented on chip. Each stimulator is identified with a dedicated hardwired stimulator ID. The stimulators can operate individually, or several stimulators can be grouped together using the stimulator ID for synchronized stimulation.

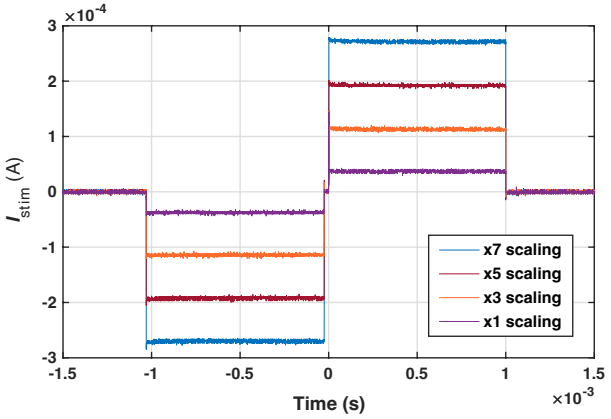

Fig. 9. Biphasic stimulator output current (I_{stim}) with a 2 kΩ resistor load for different scaling factors.

Stimulation parameters are sent to all the stimulators via a single serial peripheral interface (SPI). Each SPI command frame is headed with a parameter group number and a command ID. Stimulators are firstly assigned to a group, and those with the matching group number operate with the set parameters, e.g., stimulator with ID-1, ID-5 and ID-13 can be grouped into stimulator group 1 and operate in parallel (the stimulation parameters of group 1 are sent by the SPI).

The stimulation management logic in each stimulator stores the parameters to specific registers according to the command ID to set the biphasic current amplitudes, pulse width, interphase delay, pulse interval and amplitude scaling factors. Once all the parameters are received, the finite-state machine (FSM) leaves the idle state to start periodic operations as illustrated in Fig. 7. The states in the FSM are controlled by cascaded counters.

IV. Measured Results

The stimulator chip was implemented in XFAB 0.18 µm HV CMOS technology. The overall chip size is 1960 µm × 6100 µm, and each stimulator channel occupies an area of 350 µm × 1100 µm. The design uses the available 45 V HV MOS. The 3 HV switches (350 µm × 410 µm in total) and the 4 HV PMOS (350 µm × 280 µm in total) occupy the largest area. The two capacitors in the CT-DAC occupy an area of 165 µm × 165 µm in total. The other blocks include the low-voltage analog circuits, feedback resistor R_f and NMOS HV M_{HV1}. The chip microphotograph is shown in Fig. 8 with the percentage area breakdown shown in the pie chart.

A. Chip Performance

For chip performance tests, the stimulator was first connected to a resistor load of 2 kΩ and the voltage across it provided the stimulator output current. The CT-DAC clock was set to 15 MHz. The selected stimulator channel was set to output half the maximum output current (amplitude counter set to 512) with a symmetrical pulse width of 1000 µs each phase, an interphase delay of 25 µs and a pulse frequency of 100 Hz.

The biphasic output current for different scaling factors is shown in Fig. 9. The measured output current with ×1 scaling was 38 µA, resulting in a time-to-current conversion rate of 74.2 nA per clock, slightly higher than the design value (based on the 15 MHz DAC counter clock) of 66.7 nA per clock due to process variations. Other scaling factors were measured to be ×3.1, ×5.2 and ×7.3, providing a maximum output current of 554.3 µA at full range with the largest scaling factor.

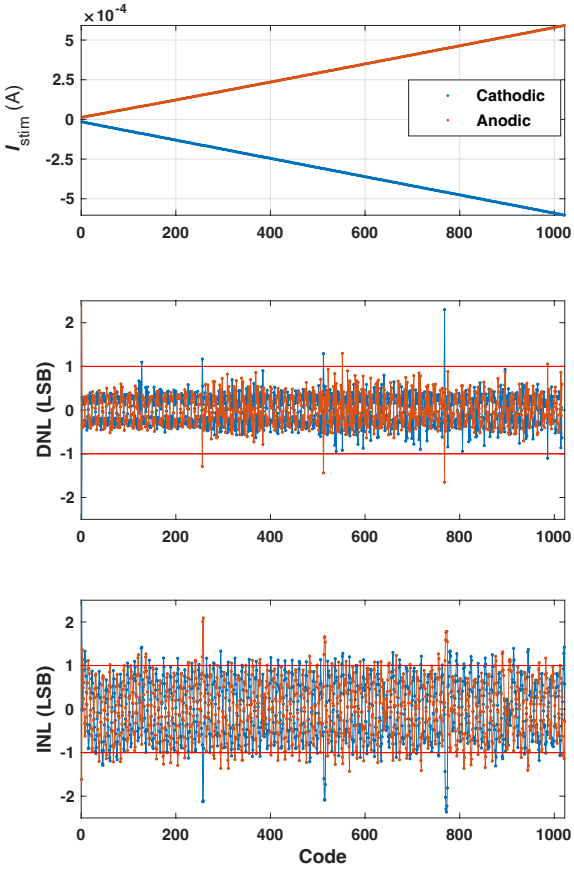

Fig. 10. The measured stimulator cathodic and anodic currents and their DNL and INL plots over a 10-bit digital sweep.

The other important parameter in this design is the bit resolution provided by the CT-DAC implementation. It was measured over a 10-bit digital sweep. The DNL and INL of the CT-DAC was extrapolated from the measured voltage across the 2 kΩ resistor load. The measured cathodic and anodic currents together with the DNL and INL plots are shown in Fig. 10.

It is important to investigate the mismatch between the cathodic and anodic currents due to process variations. The measurements in Fig. 9 were repeated for each channel and the current mismatches are plotted in Fig. 11. On average the cathodic and anodic current mismatch is 3.86%. This will lead to charge imbalance examined in the next section.

B. Charge Balancing and Experiments With Electrodes in Saline

For charge balancing evaluation, a RC electrode model (R_x = 100 kΩ and C_x = 100 nF in parallel and R_i = 2 kΩ in series) was connected in series with a sensing resistor R_s = 100 Ω. Due to imbalanced biphasic pulses, residual charge ΔQ_r remains on capacitor C_x. Without any intervention,

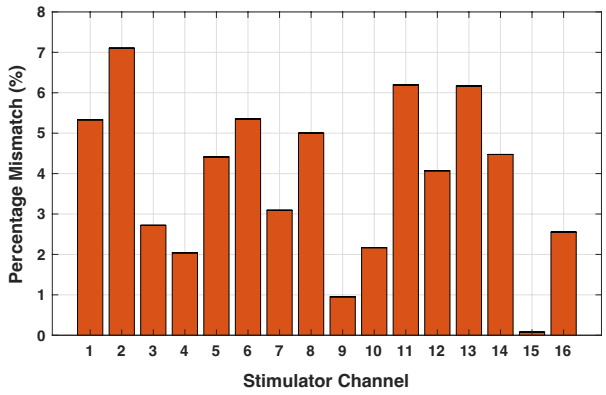

Fig. 11. Mismatch of the cathodic and anodic currents in each of the 16 independent channels in one stimulator chip. The amplitude of the cathodic and anodic currents was set to 200 µA.

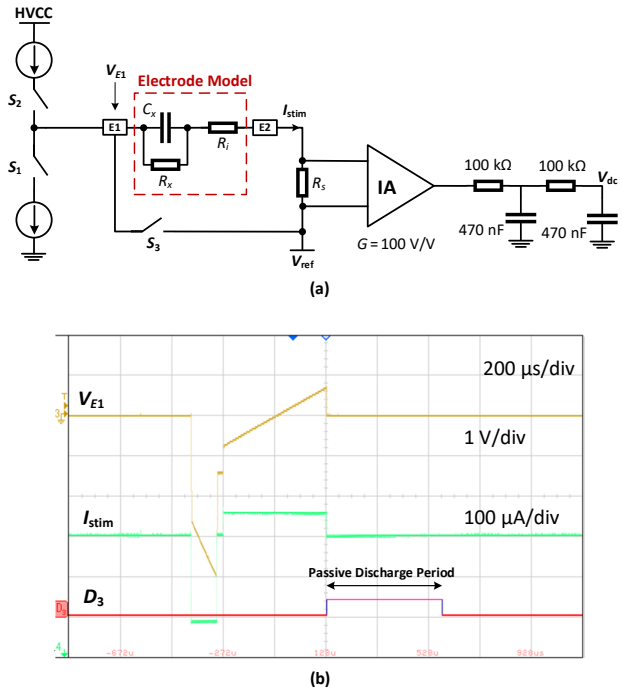

Fig. 12. (a) Setup for the residual dc measurements using the RC electrode model with passive discharge. (b) Voltage and current oscillograms of the asymmetrical biphasic stimulus pulses with the discharge switch timing. V_{E1} measured with a gain of 6. The stimulation pulse repetition rate was 100 Hz. D_3 is the digital pulse defining the passive discharge period when S_3 closes.

ΔQ_r naturally discharges through R_x with a time constant $R_x C_x$ at the pulse frequency.

Passive discharge is a simple but effective method to provide a low impedance discharge path for quicker ΔQ_r removal. By closing switch S_3 in Fig. 12(a) (see S_{HV3} in Fig. 4), the combination of R_{on}, R_s and R_i where $R_{on} \approx 750\ \Omega$ is the on resistance of S_3, provides a shorter discharging time constant. The effectiveness of passive discharge can be application and electrode impedance dependent. In the targeted application (chronic vagus nerve stimulation), the recommended stimulation threshold is below 20 nC for a pulse width of 100 µs and a frequency of 1 Hz [28]. The recommended safety limit for the equivalent residual dc current should be less than 100 nA [29]. Considering the above, the biphasic current pulse

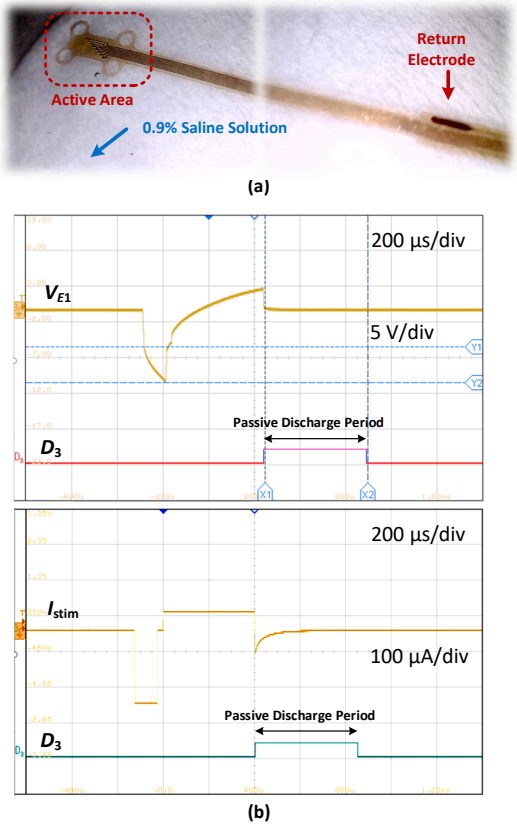

Fig. 13. (a) Microelectrode array immersed in saline solution. (b) Voltage and current oscillograms of the asymmetrical biphasic stimulus pulses with the discharge switch timing. V_{E1} measured with a gain of 6. Identical anodic and cathodic currents were used to those in Fig. 12.

parameters were set as follows: cathodic current 200 µA, pulse width 100 µs, interphase delay 25 µs, anodic current 50 µA, pulse width 400 µs. The pulse frequency was set to 100 Hz instead of 1 Hz to better illustrate the charge balancing condition.

The stimulation channel used in the charge balancing test was number 8 in Fig. 11. From Fig. 12(a) the residual current error, $i_{dc} = V_{dc}/R_s$, can register the current mismatches from the stimulator. Prior to the insertion of a passive discharge period, the measured ΔQ_r ($i_{dc} = 95.1$ nA, $t = 10$ ms) was 951 pC. By inserting a passive discharge period of 450 µs after each completed biphasic cycle as shown in Fig. 12(b), 79.3% of the ΔQ_r should be removed (the passive discharge path had a RC time constant of 285 µs). The measured reduction with passive discharge was 74% corresponding to a residual ΔQ_r of 248 pC or residual i_{dc} of 24.8 nA. Note that the remaining ΔQ_r will continue to discharge through R_x until the next biphasic cycle; this would provide an additional residual error reduction.

The stimulator chip was also tested with a gold polyimide thin film electrode array in saline solution. The electrode array for vagus nerve stimulation is of the type shown in Fig. 13(a). It has eight 80 µm diameter circular gold contacts on the active area and a long track extending to the back side where the larger return electrode is located. The entire electrode array was immersed in 0.9% saline solution; one active contact and the return electrode were connected to the '*E*1' and '*E*2' terminals shown in Fig. 12(a). The same asymmetric biphasic current in the RC electrode model experiment was used. The resulting

Table I. Comparison with other stimulator designs.

Reference	**This work**	[12]	[13]	[16]	[22]	[25]	[26]
Technology	HV 0.18 µm	65 nm LP	LV 0.18 µm	HV 0.35 µm	LV 0.18µm	HV 0.6 µm	LV 0.18 µm
Stimulation channels	16	4	16	1	8	2	1
Maximum current	0.55 mA	2 mA	3 mA	5.12 mA	0.25 mA	1 mA	1 mA
Output stage	Source-sink	H-bridge	Source-sink	Source-sink	Source-sink	H-bridge (chopped pulses)	H-bridge
DAC design	Independent CT-DAC	Independent I-DAC	I-DAC sharing	Independent I-DAC	Independent I-DAC	I-DAC sharing	I-DAC
DAC resolution	~10-bit	8-bit	4-bit	9-bit	8-bit	8-bit	5-bit
Charge balance strategy	Passive discharge	N/A	Passive discharge	Active discharge	Passive discharge & calibration	Passive discharge	Passive discharge & Anodic modulation
Residual current (i_{dc}) or voltage (V_{E1})	3.9 nA*[1]	N/A	3.42 nA*[2]	±20 mV	2 – 5 nA*[3]	5.5 nA*[4]	±20 mV*[5]
Static power**	23.3 µW	104 µW	N/A	31.8 µW	N/A	N/A	<0.59 mW
Voltage compliance	18.2 V	±11 V	±6 V	22 V	3.3 V	12 V	12.3 V
Stimulator channel area	0.385 mm^2	0.36 mm^2	0.08 mm^2	1.88 mm^2	0.064 mm^2	<10 mm^2	0.11 mm^2

*[1] Injected charge 20 nC, asymmetrical 1:4 ratio, passive discharge time 0.45 ms.
*[2] Charge error 1.056 nC, symmetrical pulses, passive discharge time 5.56 ms.
*[3] Injected charge 18.75 nC, symmetrical pulses at 0.5/1 kHz, passive discharge between pulses (calibrated I-DAC).
*[4] Injected charge 200 nC, symmetrical pulses at 1 kHz, passive discharge between pulses.
*[5] Injected charge 100 nC, symmetrical pulses at 1 kHz, anodic modulation and passive discharge between pulses.
** Static power consumption when the stimulator is in idle state.

electrode voltage and stimulus current characteristics are shown in Fig. 13(b). With passive discharge the measured residual ΔQ_r was 39 pC, equivalent to a residual i_{dc} of 3.9 nA (at 100 Hz pulse frequency), i.e., a 96% charge reduction. It is well below the <100 nA safety limit [29].

C. Power Management

The power supplies and reference voltages were generated as shown in Fig. 1. HVCC was 20 V using a boost dc-dc converter IC (LM27313) from a 3.7 V battery. LVCC (1.8 V) and the 3.3 V supply for the amplifier A_1 in Fig. 4 used standard LDOs. The 10 V reference voltage (V_{ref}) was derived from HVCC using MAX6043. The measured voltage output compliance of the stimulator was 18.2 V.

The total power consumption of the LM27313, LDOs and MAX6043 is 43 mW. The total power consumption of the CT-DAC (using 250 nA charging current per branch during the charging periods), and opmaps A_0 and A_1 in the stimulator chip is 23.3 µW. The power consumption of the rest of the stimulator circuits (see Fig. 4) is dynamically set depending on the required stimulus current.

For the digital functions, the stimulator is controlled by an FPGA (Digilent Cmod S7). The FPGA receives commands from a PC via UART communication. It also provides the SPI commands, the 1 MHz clock for the chip operation and the 15 MHz clock for CT-DAC charging.

D. Comparison and Discussion

Table I compares the stimulator in this work with other integrated neural stimulators. The CT-DAC principle provides a new alternative to the conventional I-DAC. It offers high resolution with simple layout requirements, and good power efficiency. Unlike most of the stimulators in Table I which have <8-bit I-DACs, the stimulator in this work achieves about 10-bit resolution while operating in a power efficient manner.

In terms of silicon area, the design in [15], [16] use HV transistors to form the I-DAC at the output stage. Although requiring lower static power consumption, a large silicon area is required. The LV design in [22] with a 3.3 V output stage occupies 0.064 mm^2 but can only be used with low impedance electrodes. Although not in Table I, for a direct comparison, the stimulator in [30] with an 11-bit I-DAC implemented using the same technology consumes 576 µA (at maximum I-DAC output) whereas the CT-DAC design (including the voltage-to-current conversion and intermediate mirroring stage) consumes about 69 µA. The I-DAC in [30] occupies 0.11 mm^2 compared to 0.027 mm^2 used by the CT-DAC with much less layout effort.

The CT-DAC design defines a Q_{LSB} for charging that is 4.76 times the worst-case switch charge injection ΔQ_{ds_1} as described in Section III-B. This margin required 25 pF capacitors [C_1, C_2 in Fig. 6(a)]. Minimizing ΔQ_{ds_1} in future designs could reduce the capacitor size significantly. In addition, these MIM capacitors use only the two top metal layers in the six metal CMOS technology employed. In future layout optimization, the capacitors could be placed on top of the other circuits to reduce silicon area [4].

The maximum stimulus current value has been chosen for the targeted application. In the proposed design scaling up the output current is easily accomplished either by reducing the feedback resistor R_f or increasing the scaling factor.

Passive discharge was shown to be effective in the intended application. Asymmetrical pulses, which lead to worse charge balancing compared to symmetrical pulses, were tested. Results showed a residual current of 3.9 nA which is comparable to other work and is well below the safety limit (<100 nA). Potential calibration measures can be employed to improve charge balancing at the expense of reduced CT-DAC bit resolution.

V. Conclusion

A 16-channel vagus nerve stimulator using a novel time-to-current based design has been presented. Using a small constant dc current of 250 nA, the proposed CT-DAC can provide biphasic stimulus currents of up to 550 μA with about 10-bit resolution. The stimulator is power efficient, dissipating a static power of 23.3 μW. It has an output voltage compliance of 18.2 V. A dc residual current of 3.9 nA was recorded with a microelectrode array in saline solution. The novel design is simple, accurate, and its architecture is scalable for multi-channel stimulator applications.

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