Variable Switching Point Model Predictive Control for DC-Link Voltage Regulation of Back-to-Back Converters

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***Abstract*—In this paper, a novel control method for back-to-back converters used in grid-to-motor connections is explored. To increase the robustness of low DC-link capacitances, a control method based on variable switching point model predictive control is proposed. While previous model predictive control methods for the back-to-back converter selected a certain switching state to fulfill all control goals, we use the switching time in addition to the switching state in order to minimise deviations from the target voltage. Choosing a variable switching point provides an additional degree of freedom to the control framework and allows the system to cope with the large number of control variables. In this case, the variable switching point is used to minimize the effects of low DC-link capacitances on the system. This can either be achieved by selecting a switching point that yields low DC-link capacitor charging or by selecting a switching point that aims to keep the DC-link voltage close to the reference. The proposed method is verified through numerical simulations and hardware-in-the-loop (HIL) experiments and compared to existing approaches. The results show that it is possible to control the DC-link using only the switching point of the converter.**

Keywords*— *Back-to-back Converter, Model Predictive Control, Variable Switching Point, DC-link control, Capacitor Minimization

I. Introduction

Back-to-back converters are a popular AC-DC-AC topology that is mainly used to establish connections between grids or linking renewable energy systems such as wind energy to the grid [1]. Several model predictive control schemes for the back-to-back converter have been proposed in [1]. A quasi-centralised control [2] approach can be employed to control DC-Link voltage in addition to grid side and load side. A quasi-centralized Model Predictive Control (MPC) system, for example, computes the reference quantities dynamically by utilizing load-side power estimation rather than PI-controllers. The concept of quasi-centralized MPC can be further extended to centralized model predictive control (CMPC) [3]–[5]. This approach summarizes the whole system model into one single cost function, allowing evaluation of the influence of all possible switching combinations on all the states and including effects of both sides of the converter at the same time. While [3] presented a continuous control set MPC algorithm, where the output can take any possible value, the algorithm presented in [4] instead focuses on a finite control set algorithm which only allows outputs that can be produced by the converter. The approach in [4] focuses on finite control set MPC which is achieved by linearizing the DC-link voltage. Based on the findings of [4], a variant of CMPC which is robust to low DC-link capacitances has been introduced in [5]. At each sampling point, model predictive control methods aim to estimate the optimal switching state for the next sampling instant. While conventional MPC applies this switching state for the complete next sampling interval, Variable Switching Point (VSP) MPC [6]–[14] allows to switching between two states anywhere between the current sampling step and the next one using an implicit modulator. VSPMPC has been introduced for power electronics in [9]. The main advantage of VSPMPC is that the switching point is an additional degree of freedom in the algorithm which may allow further increases in the performance of the system. Based on those findings, the concept has been extended to other topologies such as the three-level neutral point clamped converter [7], the four-switch three-phase inverter [6] and the quasi Z-source inverter [8]. An experimental evaluation of VSPMPC can be found in [10]. One problem of the proposed method is that the variable switching point has to be implemented with an implicit modulator that again has a finite sampling time. Thus, the ideal switching time computed by the algorithm might be impossible to implement on the given modulator and the best candidate of the solutions within the limit of the modulator has to be computed instead. The algorithm presented in [11]–[14], examines several candidate combinations for duty-cycle and phase shift of a dual-active bridge converter. This allows the optimal result out of all the available candidate solutions to be obtained, however since the system has two degrees of freedom, the computational complexity will increase using this method. A method to limit the number of candidates in cases where the solution is close to that at the previous time instant has therefore been suggested in [11]. In [12], [13] the proposed algorithm is extended to achieve multiple objectives such as control of the output voltage and the transformer current simultaneously. Stability analysis with guidelines for the application of the algorithm has been presented in [14].

In this paper, we introduce a VSPMPC scheme for the back-to-back converter that was originally described in [15]. In this approach, CMPC, as a basic control scheme, is used due to its

simplicity, and the additional degree of freedom offered by the VSP approach is used to achieve another control goal and to increase the overall robustness of low DC-link capacitances.

II. System Model

The system consists of a 2 level back-to-back converter that connects a three-phase AC-grid to a three-phase load [4]. A circuit diagram of the system can be seen in Fig. 1.

A. Converter Dynamics

The output voltages are denoted as $\vec{u}_l^{\text{abc}}$ on the load side and $\vec{u}_n^{\text{abc}}$ on the grid side, respectively. The switching states are denoted as $\vec{S}_n^{\text{abc}} \in \{0,1\}^3$ on the grid side, and $\vec{S}_l^{\text{abc}} \in \{0,1\}^3$ on the load side and are the input of the system. The values of $\vec{S}_n^{\text{abc}}$ and $\vec{S}_l^{\text{abc}}$ depend on the switching state of the corresponding MOSFET in Fig. 1. If $G_{i,j}$ is open and $\overline{G}_{i,j}$ is closed for $i \in \{\text{n,l}\}$ and $j \in \{\text{a,b,c}\}$ then $S_i^{\text{j}} = 0$, and if $G_{i,j}$ is closed and $\overline{G}_{i,j}$ is open then $S_i^{\text{j}} = 1$. The relationship between switching states and the converter output voltage is given by the following equation:

$$\vec{u}_i^{\text{abc}} = \frac{1}{3} V_{\text{dc}} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \vec{S}_i^{\text{abc}} = \mathbf{T}_{\text{V}} \vec{S}_i^{\text{abc}} \tag{1}$$

for $i = \{l, n\}$. V_{dc} denotes the voltage at the DC-link of the converter. Its dynamics are given by:

$$\dot{V}_{\text{dc}} = \frac{1}{C} \left((\vec{i}_n^{\text{abc}})^T \vec{S}_n^{\text{abc}} - (\vec{i}_l^{\text{abc}})^T \vec{S}_l^{\text{abc}} \right), \tag{2}$$

where $\vec{i}_n^{\text{abc}}$ is the grid side current, $\vec{i}_l^{\text{abc}}$ the load side current, and C is the DC-link capacitance.

B. Grid Side Dynamics

The dynamics of the grid side can be expressed as below:

$$\dot{\vec{i}}_n^{\text{abc}} = -\frac{R_n}{L_n} \vec{i}_n^{\text{abc}} - \frac{1}{L_n} \vec{u}_n^{\text{abc}} + \frac{1}{L_n} \vec{e}^{\text{abc}}, \tag{3}$$

where $\vec{u}_n^{\text{abc}}$ is the voltage applied to the grid side and $\vec{e}^{\text{abc}}$ the grid side source voltage. By invoking the (power invariant) Clark-Transformation as shown below all quantities $\vec{x}^{\alpha\beta} = (x^\alpha, x^\beta)^\top$ in the $\alpha\beta$ frame are derived from the original values $\vec{x}^{\text{abc}}$ measured in the abc- frame:

$$\vec{x}^{\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \vec{x}^{\text{abc}} = \mathbf{T}_C \vec{x}^{\text{abc}}. \tag{4}$$

To control the power flow, we then look into the active power P and reactive power Q on the grid side according to instantaneous power theory [1]:

$$P_n = e_n^\alpha i_n^\alpha + e_n^\beta i_n^\beta, \quad Q_n = e_n^\alpha i_n^\beta - e_n^\beta i_n^\alpha, \tag{5}$$

which results from a complex multiplication of $\vec{i}^{\alpha\beta}$ and $\vec{e}^{\alpha\beta}$. The grid-side input $\mathbf{u}_g$ state space variables $\mathbf{x}_g$ and output $\mathbf{y}_g$ are defined as:

$$\mathbf{u}_g = \vec{S}_n^{\text{abc}}, \tag{6}$$
$$\mathbf{x}_g = \vec{i}_n^{\text{abc}}, \tag{7}$$
$$\mathbf{y}_g = \begin{bmatrix} P & Q \end{bmatrix}^T. \tag{8}$$

C. Load Side Dynamics

The load side dynamics can be described by a linear system of equations [2]:

$$\dot{\vec{i}}_l^{\text{abc}} = -\frac{R_l}{L_l} \vec{i}_l^{\text{abc}} - \frac{1}{L_l} \vec{u}_l^{\text{abc}} + \frac{1}{L_l} \vec{v}_l^{\text{abc}}. \tag{9}$$

For the load side, $\vec{i}_l^{\text{abc}}$ is the current in abc- coordinates, $\vec{u}_l^{\text{abc}}$ is the voltage applied to the load side and $\vec{v}_l$ the load side voltage source. As with the grid-side, the load-side input $\mathbf{u}_l$ state space variables $\mathbf{x}_l$ and output $\mathbf{y}_l$ are defined as:

$$\mathbf{u}_l = \vec{S}_l^{\text{abc}}, \tag{10}$$
$$\mathbf{x}_l = \vec{i}_l^{\text{abc}}, \tag{11}$$
$$\mathbf{y}_l = \vec{i}_l^{\alpha\beta}. \tag{12}$$

D. Linearized System Model

Combining the grid side, load side, and linearized DC-link dynamics, the system variables can be formulated as follows:

$$\mathbf{u} = \begin{bmatrix} (\vec{S}_l^{\text{abc}})^T & (\vec{S}_n^{\text{abc}})^T \end{bmatrix}^T \in \{0,1\}^6, \tag{13a}$$
$$\mathbf{x} = \begin{bmatrix} (\vec{i}_l^{\text{abc}})^T & V_{\text{dc}} & (\vec{i}_n^{\text{abc}})^T \end{bmatrix}^T \in \mathbb{R}^7, \tag{13b}$$
$$\mathbf{y} = \begin{bmatrix} (\vec{i}_l^{\alpha\beta})^T & V_{\text{dc}} & P & Q \end{bmatrix}^T \in \mathbb{R}^5. \tag{13c}$$

Including the DC-link voltage yields a nonlinear system model since its behavior depends on the switching state as can be seen from (2):

$$\dot{V}_{dc} = \frac{1}{C} \mathbf{x}_l^T \mathbf{u}_l - \frac{1}{C} \mathbf{x}_g^T \mathbf{u}_g, \tag{14}$$

In order to obtain the input-output relationship of the system we summarize the differential equations given in (2), (3), and (9) to a single differential equation system [4]:

$$\dot{\mathbf{x}} = \begin{pmatrix} \frac{R_n}{L_n} \mathbf{x}_l - \frac{1}{L_n} \mathbf{T}_{\text{V}} \mathbf{u}_l + \frac{1}{L_n} \vec{e}^{\text{abc}} \\ \frac{1}{C} \mathbf{x}_l^T \mathbf{u}_l - \frac{1}{C} \mathbf{x}_g^T \mathbf{u}_g \\ -\frac{R_l}{L_l} \mathbf{x}_g - \frac{1}{L_l} \mathbf{T}_{\text{V}} \mathbf{u}_g + \frac{1}{L_l} \vec{v}_l \end{pmatrix}, \tag{15a}$$
$$= \mathbf{f}(\mathbf{x}, \mathbf{u}). \tag{15b}$$

The output $\mathbf{y}$ is defined in $\alpha\beta$ coordinates or can be derived from quantities that are formulated in $\alpha\beta$ coordinates. However the state $\mathbf{x}$ is formulated in abc- coordinates, and therefore, the relationship between $\mathbf{x}$ and $\mathbf{y}$ can be obtained by performing a coordinate transform using the Clarke transform matrix $\mathbf{T}_C$ and inserting the relationship given in (5) [4]:

$$\mathbf{y} = \begin{bmatrix} \mathbf{T}_C & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & 1 & \mathbf{0} \\ \mathbf{0} & \mathbf{0} & \begin{bmatrix} e_n^\alpha & e_n^\beta \\ -e_n^\beta & e_n^\alpha \end{bmatrix} \mathbf{T}_C \end{bmatrix} \mathbf{x} = \mathbf{C}\mathbf{x}. \tag{16}$$

Due to the nonlinear behaviour of the DC-link shown in Eq. (2), the system model is described by a nonlinear differential equation (15b). To avoid the increase in computational complexity which is arising from the use of a nonlinear system model, the controller is designed using on a linearized approach [4].
The linearizations of the nonlinear input-output relationships of the system are computed during the online stage at the current

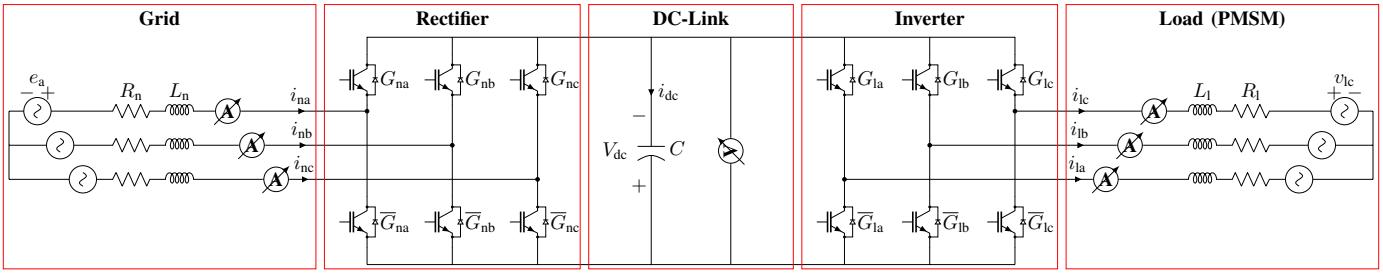


Fig. 1. Block diagram of a 2L back-to-back system consisting of the line (grid) side, the rectifier, the DC-link, the inverter, and the load side [4].

time t_0. This yields the linearization point $\mathbf{x}_0 = \mathbf{x}(t_0)$ and $\mathbf{u}_0 = \mathbf{u}(t_0)$:

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}_0, \mathbf{u}_0) + \frac{\partial \mathbf{f}}{\partial \mathbf{x}}\Big|_{\substack{\mathbf{x}_0 \\ \mathbf{u}_0}} (\mathbf{x} - \mathbf{x}_0) + \frac{\partial \mathbf{f}}{\partial \mathbf{u}}\Big|_{\substack{\mathbf{x}_0 \\ \mathbf{u}_0}} (\mathbf{u} - \mathbf{u}_0). \quad (17)$$

A linearized system model can be constructed by inserting the system model into the linearization formula (17). For the given back-to-back system, the gradients $\frac{\partial \mathbf{f}}{\partial \mathbf{x}}$ and $\frac{\partial \mathbf{f}}{\partial \mathbf{u}}$ are given as:

$$\frac{\partial \mathbf{f}}{\partial \mathbf{u}} = \begin{bmatrix} \frac{1}{L_n}\mathbf{I} & \mathbf{0} \\ \mathbf{0} & \frac{1}{L_l}\mathbf{I} \end{bmatrix}, \mathbf{S}_{\text{VEC},i} = \begin{bmatrix} 2S_i^a - S_i^b - S_i^c \\ -S_i^a + 2S_i^b - S_i^c \\ -S_i^a - S_i^b + 2S_i^c \end{bmatrix} \quad (18)$$

$$\frac{\partial \mathbf{f}}{\partial \mathbf{x}} = \begin{bmatrix} -\frac{R_n}{L_n}\mathbf{I} & -\frac{\mathbf{S}_{\text{VEC},n}}{3L_n} & \mathbf{0} \\ \frac{1}{C}\vec{S}_n^T & 0 & -\frac{1}{C}\vec{S}_l^T \\ \mathbf{0} & \frac{\mathbf{S}_{\text{VEC},l}}{3L_l} & -\frac{R_l}{L_l}\mathbf{I} \end{bmatrix}, \quad (19)$$

with $i \in \{n, l\}$. Inserting the system model into the linearization formula (17) enables the set up of the linearized system model:

$$\mathbf{F} = \frac{\partial \mathbf{f}}{\partial \mathbf{x}}\Big|_{\substack{\mathbf{x}_0 \\ \mathbf{u}_0}}, \quad \mathbf{G} = \frac{\partial \mathbf{f}}{\partial \mathbf{u}}\Big|_{\substack{\mathbf{x}_0 \\ \mathbf{u}_0}}, \quad (20a)$$

$$\mathbf{h} = \mathbf{f}(\mathbf{x}_0, \mathbf{u}_0) - \frac{\partial \mathbf{f}}{\partial \mathbf{x}}\Big|_{\substack{\mathbf{x}_0 \\ \mathbf{u}_0}} \mathbf{x}_0 - \frac{\partial \mathbf{f}}{\partial \mathbf{u}}\Big|_{\substack{\mathbf{x}_0 \\ \mathbf{u}_0}} \mathbf{u}_0. \quad (20b)$$

Applying (20) to (17) yields the well-known linear system model:

$$\dot{\mathbf{x}} = \mathbf{F}\mathbf{x} + \mathbf{G}\mathbf{u} + \mathbf{h}. \quad (21)$$

Having defined the system differential equation, the next step is to design a controller that computes an optimal input $\mathbf{u}(t)$ which ensures that the system follows a desired reference trajectory $\mathbf{y}^{\text{ref}}(t)$.

III. Proposed Control Framework

As depicted in Figure 1, a centralized control approach, consisting of a predictive current control [16] to control the load side, and a predictive power control [17] to control the grid side, is utilised in this study. This control approach is summarized in figure 2. The controller is defined in three steps: first, the reference output $\mathbf{y}^{\text{ref}}(t)$ is defined. Secondly, the prediction model and extrapolation is introduced and finally the cost function is formulated.

A. Reference Trajectories

In this paper the reference outputs are defined as follows [2]:

1) $(\vec{i}_l^{\,\alpha\beta})^{\text{ref}}$ is computed from the reference speed ω_l^{ref} of the Permanent Magnet Synchronous Machine (PMSM)-load, see e.g. [2].
2) With the known asymptotic DC-link reference being $V_{dc,\infty}^{\text{ref}}$ we define the instantaneous DC-link reference V_{dc}^{ref} as
$$V_{dc}^{\text{ref}} = V_{dc} + \frac{V_{dc,\infty}^{\text{ref}} - V_{dc}}{N_s}, \quad (22)$$
where N_s is the number of steps we assume the DC-link voltage should require to reach $V_{dc,\infty}^{\text{ref}}$ [2].
3) The reference reactive power Q^{ref} is chosen as $Q^{\text{ref}} = 0$. The reference active power P^{ref} is computed using load side power estimation [2]:
$$i_{l(dc)} = \|i_l^{\alpha\beta}\|^2 \cdot R_l / V_{dc}^{\text{ref}}, \quad (23)$$
$$i_{(dc)}^{\text{ref}} = \frac{C}{N_s T_{CTRL}}(V_{dc}^{\text{ref}} - V_{dc}), \quad (24)$$
$$i_{n(dc)}^{\text{ref}} = i_{dc}^{\text{ref}} + i_{l(dc)}, \quad (25)$$
$$P^{\text{ref}} = \frac{3A^2}{4R_l} - \sqrt{\frac{9A^4}{16R_l^2} - \frac{3A^2}{2R_l} i_{l(dc)}^{\text{ref}} \cdot V_{dc}^{\text{ref}}},$$
where A is the maximum amplitude of the grid voltage $\vec{e}$.

Similar to $\mathbf{y}$, the reference output vector is defined as:

$$\mathbf{y}^{\text{ref}} = \begin{bmatrix} \left((\vec{i}_l^{\,\alpha\beta})^{\text{ref}}\right)^T & V_{dc}^{\text{ref}} & Q^{\text{ref}} & P^{\text{ref}} \end{bmatrix}^T. \quad (26)$$

B. Extrapolation of State-Space Variables

To evaluate the performance of a candidate solution, the output trajectory is extrapolated over the next sampling step under the assumption the given candidate solution is used as input. The extrapolation is based on an explicit Euler discretization:

$$\dot{\mathbf{x}} \approx \frac{\mathbf{x}(t + T_i) - \mathbf{x}(t)}{T_i}, \quad (27)$$

utilizing T_i as a suitably small time interval. In this paper, we use only $T_i \leq T_{CTRL}$ where T_{CTRL} is the sampling time of the model predictive controller. In the following we denote the discretized state-space vector as $\mathbf{x}[k] = \mathbf{x}(t)$ and

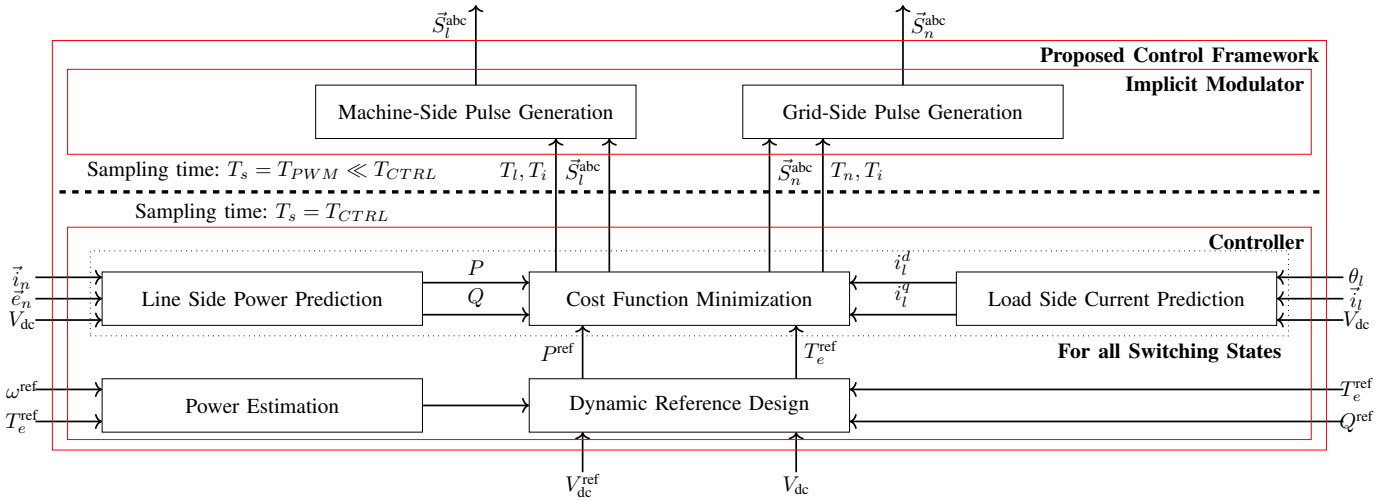


Fig. 2. The proposed controller, consisting of the known centralized MPC controller which is extended by computing the switching time, and the implicit modulator which uses the information of the switching state and switching time to generate a pulse signal. To do so, the sampling frequency of the modulator is chosen to be higher than the sampling frequency of the controller. With a centralized approach, T_i will be used to generate both pulses. For a decentralized approach, T_n and T_l will be given to the rectifier and inverter side respectively.

$\mathbf{x}[k+1] = \mathbf{x}(t+T_{CTRL})$. Applying (21) to (27) we obtain the extrapolation model for this paper:

$$\mathbf{x}[k+1] = \mathbf{A}_{T_{CTRL}}\mathbf{x}[k] + \mathbf{B}_{T_{CTRL}}\mathbf{u}[k] + \mathbf{n}_{T_{CTRL}}, \quad (28)$$

$$\mathbf{A}_{T_{CTRL}} = \mathbf{I} + T_{CTRL}\mathbf{F}, \quad (29)$$

$$\mathbf{B}_{T_{CTRL}} = T_{CTRL}\mathbf{G}, \quad (30)$$

$$\mathbf{n}_{T_{CTRL}} = T_{CTRL}\mathbf{h}. \quad (31)$$

Furthermore, using (16) the output $\mathbf{y}[k+1]$ at the next sampling step:

$$\mathbf{y}[k+1] = \mathbf{C}\mathbf{x}[k+1]. \quad (32)$$

The fundamental principle of variable switching point MPC is to switch between the present input $\mathbf{u}[k-1]$ and the next one $\mathbf{u}[k]$ at an arbitrary point in between kT_{CTRL} and $(k+1)T_{CTRL}$. The sampling time of the controller is limited by the clock frequency of the hardware on which it runs. However, it may be possible to distribute the computational tasks of the controller onto different hardware platforms with different sampling frequencies and employ different programming languages. To reduce computational requirements, the main control algorithm can be implemented on a slower microcontroller while the implicit modulator can be implemented as a simple counter on a faster field programmable gate array, allowing two discretizations of different resolutions. The signal generation of variable switching point MPC is visualized in Fig. 3. This can be modeled by applying the extrapolation formula (29) twice as follows:

1) First the current time switching state $\mathbf{u}_i[k-1]$ is applied until the switching point T_i is reached:
$$\mathbf{x}(t+T_i) = \mathbf{A}_{T_i}\mathbf{x}(t) + \mathbf{B}_{T_i}\mathbf{u}[k-1] + \mathbf{n}_{T_i}. \quad (33)$$
2) After that the next switching state $\mathbf{u}[k]$ is applied for the remainder of the sampling interval $T_{CTRL} - T_i =: \Delta T$:
$$\mathbf{x}(t+T_{CTRL}) = \mathbf{A}_{\Delta T}\mathbf{x}(t) + \mathbf{B}_{\Delta T}\mathbf{u}[k] + \mathbf{n}_{\Delta T},$$

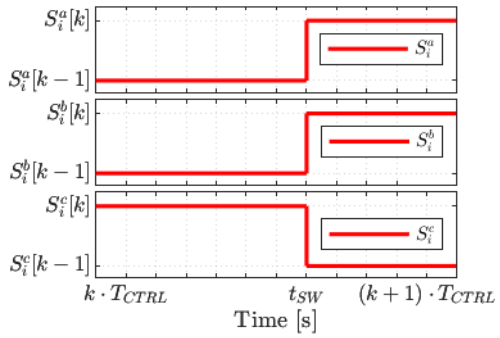


Fig. 3. Signal generation for Variable Switching Point MPC. Contrary to regular finite control set MPC, switching between two states happens between the sampling point k and $k+1$. The index i represents machine side ($i = m$) and grid side ($i = n$) in this case.

Combining the two extrapolations yields the prediction model for variable switching point MPC:

$$\mathbf{x}[k+1](\mathbf{u}[k], T_i) = \mathbf{A}(T_i)\mathbf{x}[k] + \mathbf{B}(T_i)\mathbf{u}[k] + \mathbf{n}(T_i). \quad (34)$$

Equation (34) summarizes the prediction model used in this paper. Contrary to the standard prediction model (29), the parameters $\mathbf{A}(T_i)$, $\mathbf{B}(T_i)$ and $\mathbf{n}(T_i)$ now depend on the switching point T_i. They are defined as:

$$\mathbf{A}(T_i) = (\mathbf{I} + (T_{CTRL} - T_i)\mathbf{F})^2 \quad (35a)$$

$$\mathbf{B}(T_i) = (T_{CTRL} - T_i)\mathbf{G} \quad (35b)$$

$$\mathbf{n}(T_i) = T_i\,(\mathbf{I} + (T_{CTRL} - T_i)\mathbf{F})\,(\mathbf{G}\mathbf{u}[k-1] + \mathbf{n}) + (T_{CTRL} - T_i)\mathbf{n}. \quad (35c)$$

C. Cost Function Formulation

The objective is to determine the input $\mathbf{u}[k]$ and switching point T_i that will produce the desired output trajectory $\mathbf{y}^{\text{ref}}$ as

closely as possible. This can be achieved by minimizing the following cost function:

$$J(\mathbf{u}[k], T_i) = \|\mathbf{y}[k+1](\mathbf{u}[k], T_i) - \mathbf{y}^{\text{ref}}\|_2^2. \tag{36}$$

In the case of a decentralized approach, the cost function is split in to two parts, one for the machine side and one for the grid side. Each can be solved independently from the other:

$$\begin{aligned} J(\mathbf{u}_l[k], T_l) &= \|\mathbf{y}_l[k+1](\mathbf{u}_l[k], T_l) - \mathbf{y}_l^{\text{ref}}\|_2^2, & (37)\\ J(\mathbf{u}_g[k], T_g) &= \|\mathbf{y}_g[k+1](\mathbf{u}_g[k], T_g) - \mathbf{y}_g^{\text{ref}}\|_2^2. & (38) \end{aligned}$$

In addition to the definition of the cost function (36), it is necessary to take further physical constraints of the system into account:

- The switching state $\mathbf{u}[k]$ must be a valid state of the converter: $\mathbf{u}[k] \in \{0,1\}^6$.
- The switching time must be positive and smaller than the sampling time T_{CTRL} since after T_{CTRL} the cost function J will be evaluated again: $0 \leq T_i \leq T_{CTRL}$.

Taking these two constraints into account allows the optimization problem to be formulated:

$$\begin{aligned} \mathbf{u}^{\text{opt}}[k], T_i^{\text{opt}} &= \arg\min J & (39)\\ &\quad \text{s.t.} \quad \mathbf{u}[k] \in \{0,1\}^6, 0 \leq T_i \leq T_{CTRL}. \end{aligned}$$

In case of a decentralized approach, the same cost function can be used however it will be split in two independent cost functions:

$$\begin{aligned} \mathbf{u}_l^{\text{opt}}[k], T_l^{\text{opt}} &= \arg\min J_l & (40)\\ &\quad \text{s.t.} \quad \mathbf{u}_l[k] \in \{0,1\}^3, 0 \leq T_l \leq T_{CTRL}.\\ \mathbf{u}_g^{\text{opt}}[k], T_g^{\text{opt}} &= \arg\min J_g & (41)\\ &\quad \text{s.t.} \quad \mathbf{u}_g[k] \in \{0,1\}^3, 0 \leq T_g \leq T_{CTRL}. \end{aligned}$$

This will decrease the accuracy of the solution however it will also benefit from reduced computational complexity.

IV. Solution to the Optimization Problem

The optimization problem consists of two variables: T_i and $\mathbf{u}[k]$. While T_i is a continuous quantity, $\mathbf{u}[k]$ can only take one of $2^6 = 64$ allowed states. To reduce the computational complexity the optimization process is split into two parts:

1) First, the switching point T_i is optimized for each of the 64 switching candidates by solving a continuous optimization problem.
2) In the second step, the best switching state candidate is computed by comparing the cost function values obtained for the 64 optimal switching times.

In this paper two methods to obtain the switching point are presented:

- Choosing the T_i that minimizes the required DC-link charging, using the formula introduced in [18]. This approach is presented in section IV-A.
- Minimising the DC-link voltage error using an analytic solution. This approach will be presented in section IV-B.

A. VSP-scheme to minimize DC-link charging

The required DC-link capacitance is related to the charging and discharging of the DC-link capacitance [19]. Since all current that is not flowing from the machine side to the grid side or vice versa is charging the DC-link capacitor, the DC-link voltage is used instead as cost function to obtain the switching state in the following. A formula estimating the charge change of the DC-link $C_{\text{req, approx}}$ is given as [5]:

$$\begin{aligned} \Delta\tilde{\mathcal{Q}}_{\text{r}} &= \frac{3}{4} T_{CTRL} \left(\mathbf{x}_l[k]^T \mathbf{u}_{1l}[k-1] + \mathbf{x}_l[k+1]^T \mathbf{u}_l[k] \right),\\ \Delta\tilde{\mathcal{Q}}_{\text{i}} &= \frac{3}{4} T_{CTRL} \left(\mathbf{x}_n[k]^T \mathbf{u}_n[k-1] + \mathbf{x}_n[k+1]^T \mathbf{u}_n[k] \right). \end{aligned}$$

$$C_{\text{req, approx}} = \frac{\Delta\tilde{\mathcal{Q}}_{\text{r}} - \Delta\tilde{\mathcal{Q}}_{\text{i}}}{V_{\text{dc}}^{\text{ref}}} = \frac{\tilde{\mathcal{Q}}}{V_{\text{dc}}^{\text{ref}}}. \tag{42}$$

To achieve a small DC-link capacitance, $C_{\text{req, approx}}$ must be kept as small as possible. For this reason we define a reference for the required capacity as $C_{\text{req, approx}}^{\text{ref}} = 0$. This allows us to apply the formula that yields the switching point as presented in [20]. Therefore we define the extrapolation of the charge with the current input as $\tilde{\mathcal{Q}}_0$:

$$\tilde{\mathcal{Q}}_0 = \tilde{\mathcal{Q}}\Big|_{\mathbf{u}_n[k]=\mathbf{u}_n[k-1], \mathbf{u}_l[k]=\mathbf{u}_l[k-1]}. \tag{43}$$

Furthermore we define:

$$m_Q = \frac{\tilde{\mathcal{Q}}_0}{T_{CTRL}} \quad m_Z = \frac{\tilde{\mathcal{Q}}}{T_{CTRL}}. \tag{44}$$

as the mean gradients of the charge exchange during the sampling interval. The switching time T_i determined in [20] can then be expressed as:

$$T_i^{\text{opt}} = \frac{V_{\text{dc}}^{\text{ref}} - V_{\text{dc}} - C \cdot \tilde{\mathcal{Q}}}{C\,(m_Q - m_Z)}. \tag{45}$$

For the decentralized approach, the charge on one of the sides are minimized to compute each switching time respectively:

$$\begin{aligned} T_n^{\text{opt}} &= \frac{-T_{CTRL}\Delta\tilde{\mathcal{Q}}_{\text{r}}}{\tilde{\mathcal{Q}}_0 - \Delta\mathcal{Q}_{\text{r}}} & (46)\\ T_l^{\text{opt}} &= \frac{-T_{CTRL}\Delta\tilde{\mathcal{Q}}_{\text{i}}}{\tilde{\mathcal{Q}}_0 - \Delta\mathcal{Q}_{\text{i}}} & (47) \end{aligned}$$

B. VSP-scheme to minimize DC-link voltage errors

Equation (45) gives an expression for the switching point under the assumption that the slope of $C_{\text{req, approx}}$ is constant over the whole time interval. Since this is only an approximation we present a second approach in which the optimal switching point is chosen as the point which provides the best reference tracking of the DC-link voltage:

$$T_i^{\text{opt}} = \arg\min \|V_{\text{dc}}[k+1](T_i) - V_{\text{dc}}^{\text{ref}}\|_2^2. \tag{48}$$

The optimization problem in the above equation can be reformulated by computing $V_{\text{dc}}[k+1]$ using the fourth row (indicated with subscript 4) of the prediction model (34):

$$T_i^{\text{opt}} = \arg\min \|\mathbf{A}_{4,:}(T_i)\mathbf{x}[k] + \mathbf{B}_{4,:}(T_i)\mathbf{u}[k-1] + \mathbf{n}_4(T_i) - V_{\text{dc}}^{\text{ref}}\|_2^2. \tag{49}$$

For the decentralized approach, the optimization problem is split into the grid side and machine side, as with the linear approach:

$$\begin{aligned} V_{\mathrm{dc},n}(T_n) &= \mathbf{A}_{4,5:7}(T_n)\mathbf{x}_n[k] + \mathbf{B}_{4,4:6}(T_n)\mathbf{u}_g[k-1] + \mathbf{n}_4(T_n) \\ T_n^{\mathrm{opt}} &= \arg\min \|V_{\mathrm{dc},l}(T_n) - V_{\mathrm{dc}}^{\mathrm{ref}}\|_2^2 \quad (50) \\ V_{\mathrm{dc},l}(T_l) &= \mathbf{A}_{4,1:3}(T_l)\mathbf{x}_l[k] + \mathbf{B}_{4,1:3}(T_l)\mathbf{u}_l[k-1] + \mathbf{n}_4(T_l) \\ T_l^{\mathrm{opt}} &= \arg\min \|V_{\mathrm{dc},l}(T_l) - V_{\mathrm{dc}}^{\mathrm{ref}}\|_2^2. \quad (51) \end{aligned}$$

The solution is then obtained by using the well-known equation $\|\mathbf{a}\|_2^2 = \mathbf{a}^T\mathbf{a}$, deriving the result with respect to T_i and setting the derivative to zero:

$$\frac{\partial}{\partial T_i}\|V_{\mathrm{dc}}[k+1](T_i) - V_{\mathrm{dc}}^{\mathrm{ref}}\|_2^2 \stackrel{!}{=} 0. \quad (52)$$

Simplifying the resulting expressions yields a quadratic equation for T_i:

$$\begin{aligned} a &= -\mathbf{F}_{4,:}\mathbf{F}\mathbf{x}[k] - \mathbf{F}_{4,:}\mathbf{G}\mathbf{u}[k-1] - \mathbf{F}_{4,:}\mathbf{h} \quad (53a) \\ b &= \mathbf{F}_{4,:}\mathbf{x}[k] + \mathbf{G}_{4,:}\mathbf{u}[k-1] + h_4 + T_{CTRL}\mathbf{F}_{4,:}\mathbf{F}\mathbf{x}[k] \\ &\quad + \mathbf{F}_{4,:}\mathbf{G}\mathbf{u}[k-1] + \mathbf{F}_{4,:}\mathbf{h} - \mathbf{G}_{4,:}\mathbf{u}[k] - h_4 \quad (53b) \\ c &= V_{\mathrm{dc}} + T_{CTRL}\mathbf{F}_{4,:}\mathbf{x}[k] + T_{CTRL}\mathbf{G}_{4,:}\mathbf{u}[k] + \\ &\quad + T_{CTRL}h_4 - V_{\mathrm{dc}}^{\mathrm{ref}} \quad (53c) \\ 0 &\stackrel{!}{=} aT_i^2 + bT_i + c. \quad (53d) \end{aligned}$$

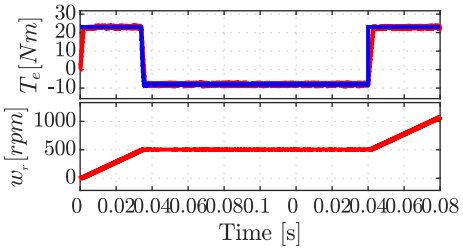
The solution of (53) for T_i can be found with the standard solution for quadratic equations. Since there can be more than one solution, the only remaining step is to determine how to select T_i^{opt}:

1) If there is no solution, set $T_i^{\mathrm{opt}} = 0$.
2) If there is a single solution which is a maximum, choose $T_i^{\mathrm{opt}} = 0$.
3) If there is a single solution that is a minimum, choose T_i^{opt} as this minimum.
4) If there are two solutions, set T_i^{opt} as the minimum.

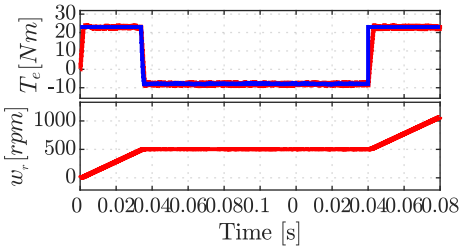
When the switching point is found, the second part of the cost function is solved. The simulation showed that in some cases it might be beneficial to only set the grid side switching point $T_{n,i}$ to T_i^{opt} while setting the machine side switching time as $T_{m,i} = 0$ at all times. This will be thoroughly discussed in the next section. The solution can be found e.g. with an exhaustive search or a sphere decoder [4]. To generate the input signal of the converter, it is necessary to add a modulator that works with a higher sampling frequency T_{PWM} than the controller T_{CTRL}.

V. Simulation and HIL Results

The properties of the proposed framework are examined using numerical and real-time simulations. Therefore, a back-to-back converter with a DC-link voltage reference $V_{\mathrm{dc},\infty}^{\mathrm{ref}}$ =550 V was examined. For the grid side a peak voltage of $\vec{e}_n^{\mathrm{abc}} =$ 250 V, a frequency of $\omega_n = 100\pi$ Hz, a resistance $R_n =$ 0.156 Ω and inductance of $L_n = 0.019$ H were chosen. The simulated machine side data was a PMSM with $R_s = 0.1379$ Ω, $L_s = 0.019$ H, $\psi_{pm} = 0.426\,75$ Wb and $N_p = 3$. The sampling time of the controller was $T_{CTRL} = 50$ µs. The

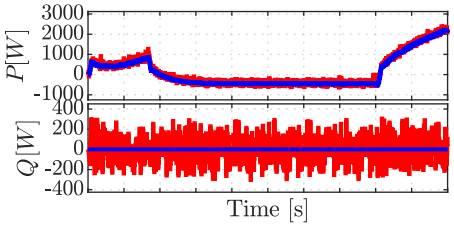


(a) Centralized MPC, $\lambda_C = 0$, C =3100 µF.

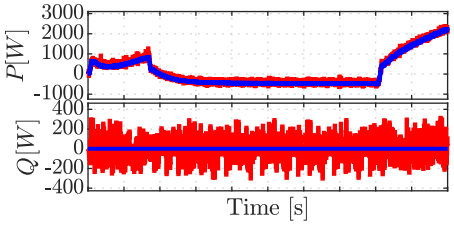


(b) Proposed Variable Switching Point MPC.

Fig. 4. Machine-side torque and speed transient data comparison. The top plots of both subfigures show the machine torque where the blue curve is the reference and the red curve shows the actual value from the machine. The lower plot shows the speed during that time for centralised MPC and the proposed method, respectively.

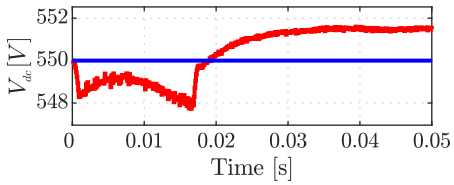


(a) Centralized MPC, $\lambda_C = 0$, C =3100 µF.

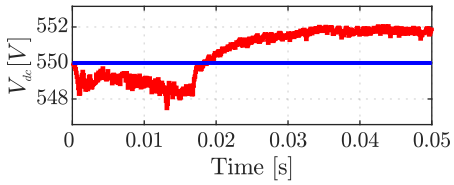


(b) Proposed Variable Switching Point MPC.

Fig. 5. Grid side active and reactive power transient data comparison. The top subfigure shows the transients of the active power on the grid side. The blue curve denotes the reference quantity while the red curve shows the actual value from the simulation. The lower plot gives the reactive power on the grid side. The blue curve shows the reference of the transient of the grid side while the red curve shows the actual value obtained during the simulation.



(a) Centralized MPC, $\lambda_C = 0$, C =3100 µF.



(b) Proposed Variable Switching Point MPC.

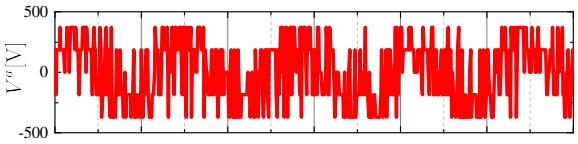
Fig. 6. DC-link voltage transient data comparison. The blue curve shows the reference value which the controller aims to follow during the simulation. The red curve gives the actual value of the system.

sampling time of the modulator was chosen as T_{PWM} = 5 µs. To verify the functionality of the variable switching point algorithm with variable switching on the grid side it is first compared to a state-of-the-art approach for high DC-link capacitance presented in [4]. For both simulations, the DC-link capacitance was set to the value of C =3100 µF allowing a qualitative comparison between the two methods. The results are summarized in Figs. 4, 5 and 6. From the figures, it can be seen that for higher DC-link capacitances both methods show roughly similar performance. The total harmonic distortion of the grid-side current and voltage switching pattern during steady-state can be seen in Fig. 7. For the conventional MPC, the total harmonic distortion is 1.58% while the variable switching point MPC has approximately the same value of 1.45%.

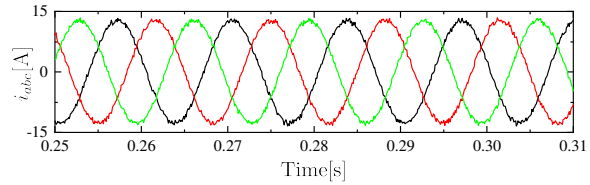
A. Experimental Results

To get an insight into the realtime capability of the proposed method and to include effects of sensor noises, a HIL experiment of the proposed method has been conducted. The HIL experiments do not account for current sensor noise issues, which might distort the results. An error in the recorded current influences the computation of the switching point which could potentially worsen the performance of variable switching point-based control methods. Common current sensors in grid-based applications are current transformer and Hall-effect based sensors which however have been found to have accuracy errors of less than 0.5% [21]. In addition to that, the error is dependent on the particular design of the sensor [22]. To provide an independent assessment, a HIL setup was therefore chosen which does not include the effects of the phase current sensors.

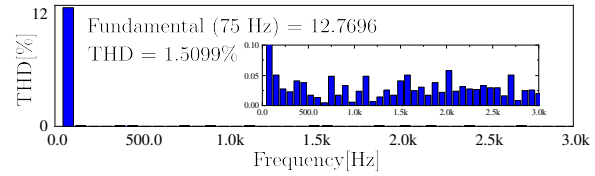
The HIL setup consists of a Plecs RT-box 1, which carries a plecs-blockset implementation of the physical back-to-back converter system running at a sampling time of 5μs. The measurements are converted to voltage signals and transferred via ethernet to an Imperix B-box which runs the controller. The B-box reads the signal transferred through the ethernet



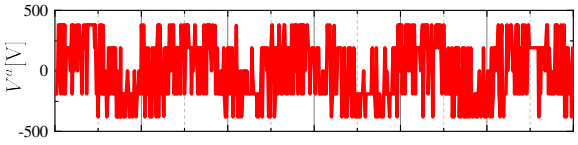
(a) Conventional MPC.



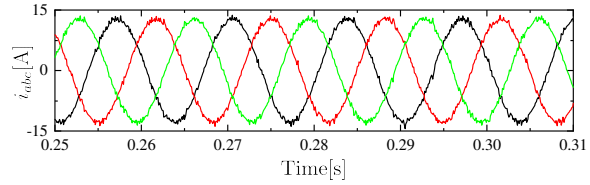
(b) Conventional MPC.



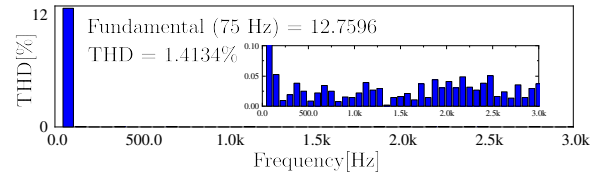
(c) Conventional MPC.



(d) VSP MPC.

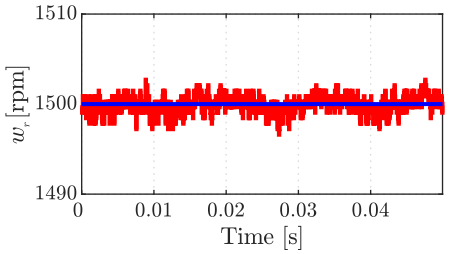


(e) VSP MPC.

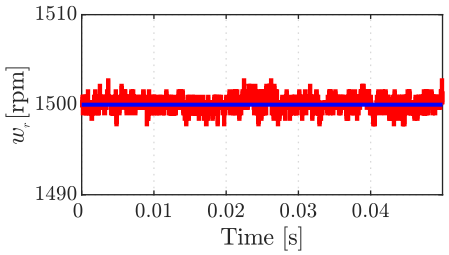


(f) VSP MPC.

Fig. 7. Steady state grid-side current dynamics and total harmonic distortion. The top plot shows the steady-state behaviour of the a-phase voltage during the simulation. The middle plot gives the corresponding current three-phase currents which are recorded during that time. A frequency analysis including the THD and fundamental frequencies of those currents is given in the lower plot.

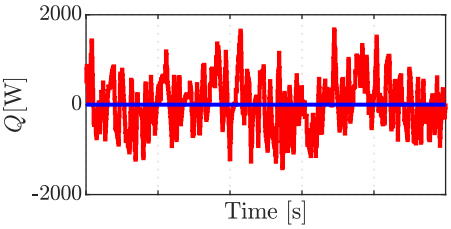


(a) Linear cost function.

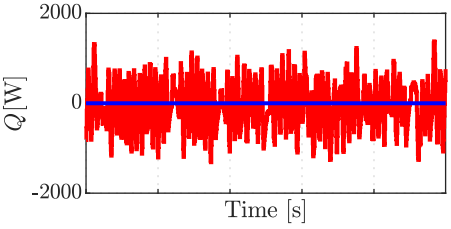


(b) Quadratic cost function.

Fig. 8. Hardware-in-the-loop simulation results for the machine side motor speed. The blue curve shows the reference and the red curve the measured quantity.



(a) Linear cost function.

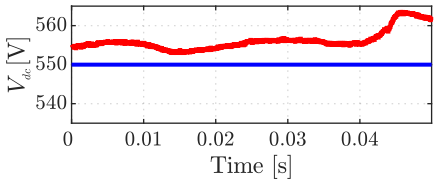


(b) Quadratic cost function.

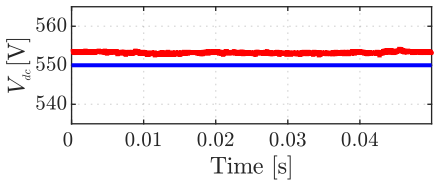
Fig. 9. Hardware-in-the-loop simulation results for the grid side reactive power. The blue curve shows the reference and the red curve the measured quantity.

connections using its internal sensors and computes the system behaviour at the next time instant. A sampling time of $T_{CTRL} = 50\mu$s is used for the controller on the B-box to compute the next switching state and the transition time. The switching state is then passed to the RT-box using optical connections.

To ease the computational burden, the HIL computes the machine side and grid side separately using two independent cost functions. The results for the machine side speed can be seen in Fig. 8 in which both the linear as well as the quadratic cost functions show good speed reference tracking. Both methods use the cost functions given in (38) and only differ in the computation of the switching point. The cost functions (38)



(a) Linear cost function.



(b) Quadratic cost function.

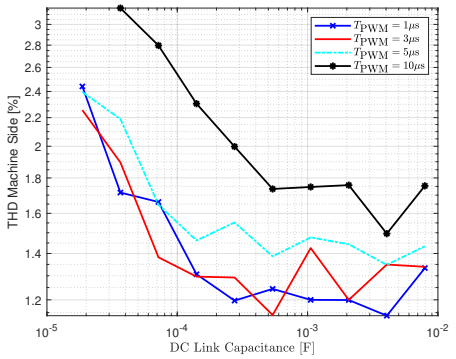
Fig. 10. Hardware-in-the-loop simulation results for the DC-link voltage. The blue curve shows the reference and the red curve the measured quantity.

optimize the reference tracking of the machine side quantities which is generating the speed trajectory. Since the cost function is similar for both methods, the speed trajectory is similar as well. A similar observation can be made for the grid side in Fig. 9 in which the linear cost function has slower changing ripples with spikes ranging up to almost 2 kW around the reference trajectory while the quadratic cost function has quicker changing ripples with slightly lower amplitude around 1 kW. Furthermore, it can be seen that in comparison to the numerical simulation results, the oscillations of the reactive power are larger which is due to additional time delays. As depicted in Fig. 10, the DC-link voltage it is visible that the quadratic cost function shows more accurate results, staying below 1% error while the linear cost function has larger deviations of up to almost 3%. Contrary to the grid-side and machine side quantities, the DC-link is not covered in the cost function given in (38). Instead, the DC-link is optimized by the switching point selection. The linear cost function assumes that the optimal value can be reached within one sampling interval. The quadratic cost function uses a quadratic minimization of the DC-link voltage error and thus yields more accurate results. Both methods, however, manage to control the DC-link voltage without reaching an error of more than 3%. A further improvement might be possible by changing the prediction model to a more accurate one such as a matrix-exponential based prediction model.

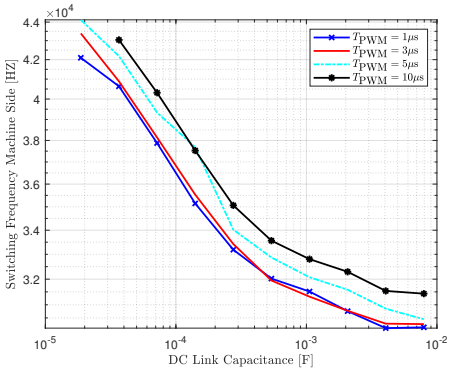
B. Robustness to Modulator Frequency

The proposed algorithm allows the converter to switch between two sampling instances of the controller. It therefore requires an additional implicit modulator to implement the variable switching point which runs at a higher sampling frequency. This modulator can have a sampling frequency that differs from the original sampling frequency of the system. To ensure a good performance of the system, the effect of the sampling frequency onto several error measures is discussed in the following.

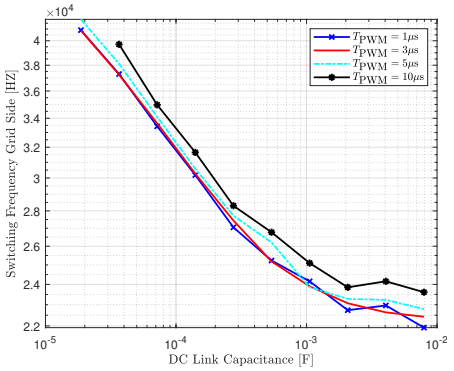
Figure 15 gives details of the quadratic VSP-MPC algorithm for different DC-link capacitance values. Additionally,



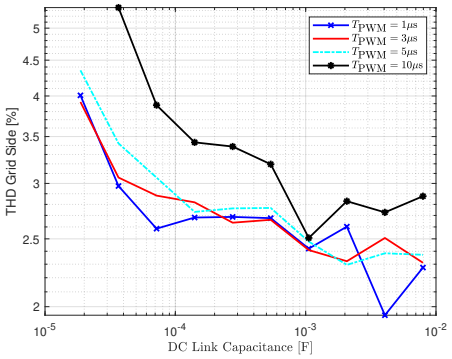
(a) Machine-side phase current total harmonic distortion.



(b) Machine-side switching frequency.

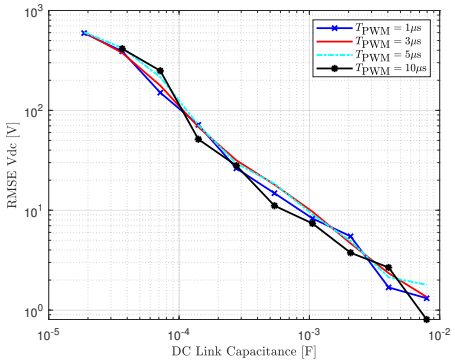


(c) Grid-side switching frequency.

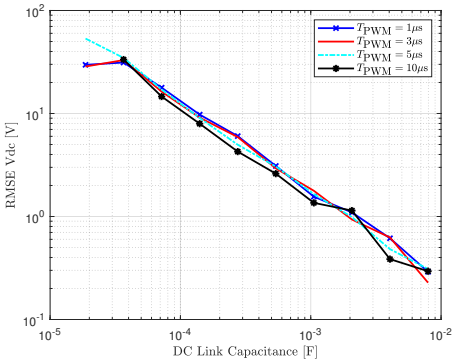


(d) Grid-side phase current total harmonic distortion.

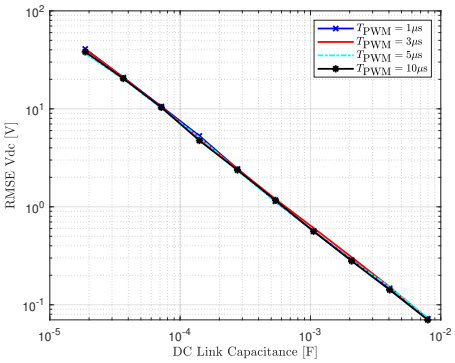
Fig. 11. Comparison of different error measures for the quadratic VSP-MPC algorithm presented in section IV-B. Each curve represents a certain modulator switching frequency. The two upper plots show the machine side current total harmonic distortion and switching frequency while the grid side data is shown in the lower two plots



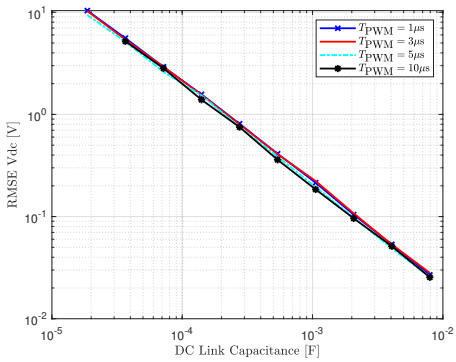
(a) Linear VSP-MPC applied on both sides.



(b) Linear VSP-MPC applied on Grid Side.



(c) Quadratic VSP-MPC applied on Grid Side.



(d) Quadratic VSP-MPC applied on both sides.

Fig. 12. Comparison of the root-mean-square error (RMSE) of the DC-link voltage for different DC-link capacitances. Each curve represents a certain modulator sampling frequency. The upper plots show the performance of linear VSP-MPC presented in section IV-A, while the lower two plots show the performance of the quadratic algorithm presented in section IV-B.

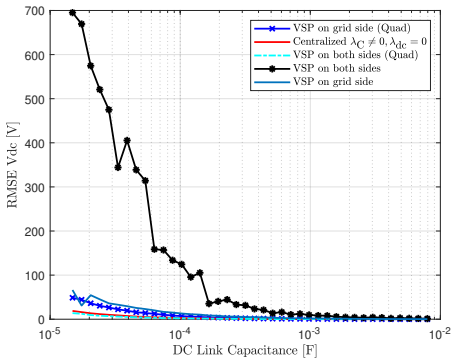
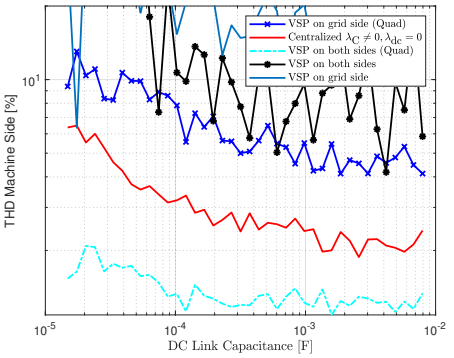
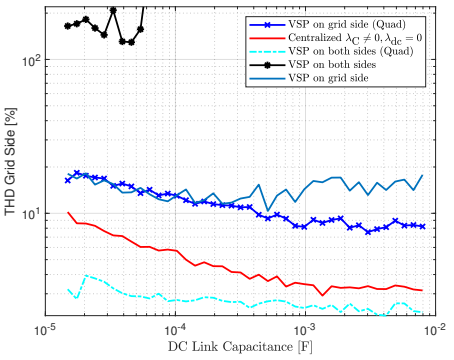


Fig. 13. Steady State RMSE of DC-link Voltage Performance Comparison. For all examined methods, the RMSE of the DC-link voltage is shown with respect to different values of DC-link capacitances in order to verify robustness to low DC-link capacitor values.



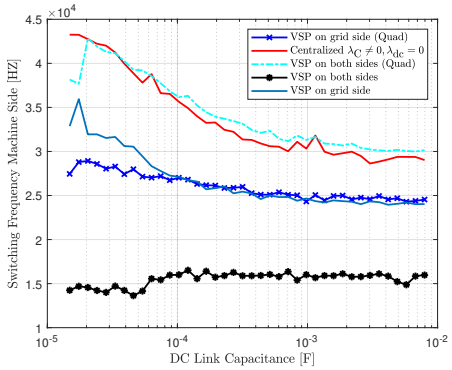
(a) Machine Side total harmonic distortion THD.



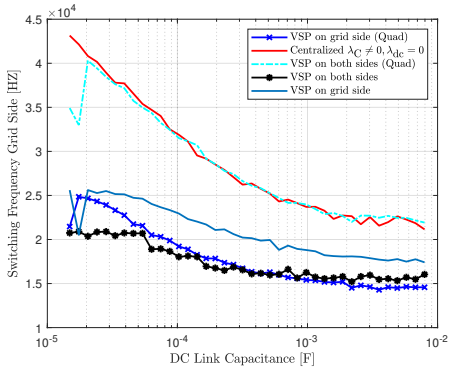
(b) Grid Side total harmonic distortion THD.

Fig. 14. Steady State Current Performance Comparison. The THD of the machine side currents is shown in the top plot. The lower plot show the grid side current THD for all examined methods for different DC-link capacitor values to compare the behaviour of different methods at lower DC-link capacitances.

the performance is shown for different sampling times of the modulator to show the effect of choosing a higher frequency for the implicit modulator. Fig. 11(a) shows that the total harmonic distortion of the machine side currents increase with increasing modulator period duration. An increase in total harmonic distortion (THD) is most pronounced at the step from $T_{\text{PWM}} = 5\ \mu\text{s}$ to $T_{\text{PWM}} = 10\ \mu\text{s}$. This can be explained by increasing off-grid error due to the more coarse sampling of the modulator. To reduce the switching losses of the converter, it is important to keep the switching frequency low. The switching frequency is measured by the number of times the converter



(a) Machine Side.



(b) Grid Side.

Fig. 15. Switching Frequency Comparison. The top plot shows the switching frequency of the inverter part of the back-to-back converter. The switching frequency was recorded for all examined methods and for several DC-link capacitance values. The lower plot shows a comparison of the switching frequency on the rectifier side of the back-to-back converter for all examined methods over different DC-link capacitance values.

has to switch from one state to another per second. The switching frequency of the converter is shown in Fig. 11(b) for the machine side and Fig. 11(c) for the grid side. It can be seen that the switching frequency slightly decreases with increasing modulator frequencies for all capacitances. A similar observation to the machine-side current THD in Fig. 11(a) can be made for the grid-side current THD as shown in Fig. 11(d). The root-mean-square error of the DC-link voltage is also independent of the modulator frequency as seen in Fig. 12(a) for the linearized approach. This shows that allowing only limited variation of the switching point already yields an improvement in the DC-link voltage performance. This effect can be observed if the framework is applied onto only one side of the converter as seen in Fig. 12(b) and Fig. 12(c) as well for the quadratic control approach as shown in Fig. 12(d). It can be seen that for the linear VSP approach, the root-mean-square error (RMSE) reaches a value of 1V at a DC-link capacitance of roughly 1 mF and 10 mF. In case of the quadratic scheme, the same value is reached for lower DC-link capacitances, namely 0.5 mF and 0.1 mF. For the given approaches approaches, the machine-side and grid-side trajectory optimization is performed by the switching state selection given in (36) which is similar in both cases. The DC-link voltage however is optimized by the VSP based frameworks. The VSP based frameworks are using

a linear optimization for the linear approach and a quadratic cost function minimization for the quadratic approach, which yields a higher robustness for low DC-link capacitances.

C. Comparative Analysis

A second simulation was conducted to examine the robustness of both methods to low DC-link capacitances. This paper focuses on the comparison of the proposed MPC scheme with other MPC-based methods. A comparison of MPC-based approaches with classic control techniques that are established in industry can be found in [1], chapter 4, for example. It was found that MPC requires less parameter tuning effort and achieves lower DC-link ripples at a similar switching frequency. In this scenario, the following methods were added to the comparison:

- VSPMPC with variable switching on both sides.
- Centralized MPC [5] with $\lambda_C = V_{\mathrm{dc},\infty}^{\mathrm{ref}}/36$, $\lambda_{\mathrm{dc}} = 0$.
- VSPMPC with a quadratic minimization scheme.

To compare the performance for low DC-link capacitance, 40 values for C varying from C =10 µF to C =6 mF with a logarithmically increasing step size were evaluated. For this simulation, the modulator period duration was selected as $T_{\mathrm{PWM}} = 5\ \mu\mathrm{s}$. For all four methods, the RMSE of the DC-link voltage (Figure 13) increases with lower DC-link capacitances. It can be seen that the linear approach has a higher DC-link error compared to all other methods, especially for low DC-link capacitance values while the quadratic VSP algorithm on both sides shows the best overall performance. The THD on the machine side as well as grid side is shown in Figure 14. The THD is low for the quadratic VSP algorithm applied to machine-side and grid side which is explained due to having the lowest DC-link distortion in the case of low DC-link capacitance. Both linear VSP schemes show bad performance for the THDs. Furthermore, the switching frequencies for both converter sides (Figure 15) were examined under steady-state conditions. In this case, the quadratic VSP algorithm requires the highest switching frequency, together with the centralized MPC approach. The lowest switching frequency is achieved by the linear VSP algorithm which, however, might be explained by the breakdown in performance shown in Fig. 14 and Fig. 13. Moreover it can be seen that using the variable switching point on both sides with the linear scheme leads to an unstable solution. The quadratic solution on both sides, as well as the linear solution on the grid side, show roughly equal performance but both methods are outperformed by the algorithm presented in [5].

VI. Conclusion

This paper presented a variable switching point predictive control method for back-to-back converters that is robust to low DC-link capacitances. To achieve this, it is best to compute the switching point using a quadratic minimization scheme. This however comes at the expense of higher computational complexity. To implement the variable switching point, an additional modulator is required. Simulation results show that the clock frequency of the modulator should be significantly higher than the clock frequency of the controller. Moreover, with decreasing DC-link voltage the variable switching point schemes have a slower break down in performance compared to an existing model predictive control method. Furthermore, the results showed that for low DC-link capacitances the proposed method has low total harmonic distortion of the current on both the machine side as well as the grid side.

References

[1] Z. Zhang, "On control of grid-tied back-to-back power converters and permanent magnet synchronous generator wind turbine systems," Dissertation, Technical University of Munich, Munich, 2016.

[2] Z. Zhang, F. Wang, T. Sun, J. Rodríguez, and R. Kennel, "Fpga-based experimental investigation of a quasi-centralized model predictive control for back-to-back converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, Jan 2016.

[3] A. Rodríguez-Cabero, F. H. Sánchez, and M. Prodanovic, "A unified control of back-to-back converter," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016.

[4] F. Grimm and Z. Zhang, "Centralized direct model predictive control of back-to-back converters," in *2018 IEEE International Power Electronics and Application Conference and Exposition (PEAC)*, Nov 2018.

[5] F. Grimm, Y. Li, X. Liu, and Z. Zhang, "Predictive control of back-to-back converters with dc-link capacitance minimization," in *2019 IEEE International Symposium on Predictive Control of Electrical Drives and Power Electronics (PRECEDE)*, May 2019.

[6] G. Patsakis, P. Karamanakos, P. Stolze, S. Manias, R. Kennel, and T. Mouton, "Variable switching point predictive torque control for the four-switch three-phase inverter," in *2013 IEEE International Symposium on Sensorless Control for Electrical Drives and Predictive Control of Electrical Drives and Power Electronics (SLED/PRECEDE)*, Oct 2013.

[7] P. Stolze, P. Karamanakos, M. Tomlinson, R. Kennel, T. Mouton, and S. Manias, "Heuristic variable switching point predictive current control for the three-level neutral point clamped inverter," in *2013 IEEE International Symposium on Sensorless Control for Electrical Drives and Predictive Control of Electrical Drives and Power Electronics (SLED/PRECEDE)*, Oct 2013.

[8] P. Karamanakos, A. Ayad, and R. Kennel, "A variable switching point predictive current control strategy for quasi-z-source inverters," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, March 2018.

[9] P. Karamanakos, P. Stolze, R. M. Kennel, S. Manias, and H. du Toit Mouton, "Variable switching point predictive torque control of induction machines," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 2, June 2014.

[10] S. Wendel, P. Karamanakos, A. Dietz, and R. Kennel, "Operating point dependent variable switching point predictive current control for pmsm drives," in *2019 IEEE International Symposium on Predictive Control of Electrical Drives and Power Electronics (PRECEDE)*, May 2019.

[11] M. M. Mardani, M. H. Khooban, A. Masoudian, and T. Dragičević, "Model predictive control of dc–dc converters to mitigate the effects of pulsed power loads in naval dc microgrids," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5676–5685, 2019.

[12] Q. Xiao, L. Chen, H. Jia, P. W. Wheeler, and T. Dragičević, "Model predictive control for dual active bridge in naval dc microgrids supplying pulsed power loads featuring fast transition and online transformer current minimization," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 5197–5203, 2020.

[13] L. Chen, F. Gao, K. Shen, Z. Wang, L. Tarisciotti, P. Wheeler, and T. Dragičević, "Predictive control based dc microgrid stabilization with the dual active bridge converter," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 10, pp. 8944–8956, 2020.

[14] L. Tarisciotti, L. Chen, S. Shuai, and T. Dragicevic, "Large signal stability analysis of dab converter using moving discretized control set– model predictive control," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 5922–5929.

[15] F. Grimm and M. Baghdadi, "Variable switching point model predictive control for dc-link capacitance minimization of back-to-back converters," in *2020 27th International Workshop on Electric Drives: MPEI Department of Electric Drives 90th Anniversary (IWED)*, 2020, pp. 1–6.

[16] J. Rodriguez, J. Pontt, C. A. Silva, P. Correa, P. Lezana, P. Cortés, and U. Ammann, "Predictive current control of a voltage source inverter," *IEEE transactions on industrial electronics*, vol. 54, no. 1, 2007.
[17] J. Rodriguez, J. Pontt, P. Correa, P. Lezana, and P. Cortes, "Predictive power control of an ac/dc/ac converter," in *Fourtieth IAS Annual Meeting. Conference Record of the 2005*, vol. 2. IEEE, 2005.
[18] P. Karamanakos, P. Stolze, R. Kennel, S. Manias, and T. Mouton, "Variable switching point predictive torque control," in *2013 IEEE International Conference on Industrial Technology (ICIT)*, Feb 2013.
[19] B. G. Gu and K. Nam, "A theoretical minimum dc-link capacitance in pwm converter-inverter systems," *IEE Proceedings - Electric Power Applications*, vol. 152, no. 1, Jan 2005.
[20] P. Stolze, P. Karamanakos, R. Kennel, S. Manias, and C. Endisch, "Effective variable switching point predictive current control for ac low-voltage drives," *International Journal of Control*, vol. 88, no. 7, 2015.
[21] V. Miron-Alexe, "Comparative study regarding measurements of different ac current sensors," in *2016 International Symposium on Fundamentals of Electrical Engineering (ISFEE)*, 2016, pp. 1–6.
[22] E. Lesniewska, "Influence of the selection of the core shape and winding arrangement on the accuracy of current transformers with through-going primary cable," *Energies*, vol. 14, no. 7, p. 1932, 2021.