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Abstract

An ultra-compact 1.4mm×1.4mm, 128×120 SPAD image sensor with a 5-wire interface is designed for time-resolved fluorescence microendoscopy. Dynamic range (DR) is extended by noiseless frame summation in SRAM attaining 126dB time resolved imaging at 15fps with 390ps gating resolution. The sensor SoC is implemented in STMicroelectronics 40nm/90nm 3D-stacked BSI CMOS process with 8µm pixels and 45% fill factor.

Introduction

Ultra small form factor cameras enable minimally invasive surgical procedures and diagnostics in lung, blood vessel and urinary tract inspection [1]. A trend towards disposable "chip on tip" endoscopes to obviate laborious and sometimes imperfect sterilization procedures is made possible by low cost, nanoscale CIS manufacturing [2]. There is an increasing requirement to enhance intensity-based image visualization with other diagnostic cues such as the use of fluorescence or spectral information [3,4]. Our device now adds fluorescence lifetime imaging (FLIM) as a powerful contrast mechanism for cancerous tissue or fluorescent smartprobe-guided pathogen identification [5]. A 3D-stacked BSI SPAD array is combined with an oversampled noiseless SRAM-based image integration scheme to provide low noise, high sensitivity, high dynamic range (HDR) time gated images. Although the image resolution is >10x lower than other chip on tip sensors [6,7] due to SPAD pixel size, the sensor extends HDR FLIM and 3D-imaging capabilities to pill and distal camera endoscopy.

Sensor Architecture

The SoC (Fig. 1) runs from 5-wires; two IO pads (a system clock and a bidirectional data line), SPAD and core supplies and ground. A power on reset (POR) block initializes the sensor and a custom digitally synthesized micro-controller unit (MCU) controls rolling and global shutter video timing, the on-chip HDR oversampling and data transfer to the host. The SoC interacts via the ARM single wire debug (SWD) protocol. A power management block (Fig. 2) comprising a bandgap and a 1.1V voltage supply regulator is designed to offer 4-wire operation using an external resistive divider of the SPAD supply (V_{HV}).

The 8µm all-digital pixel circuit (Fig. 3) integrates a 14-bit counter with overflow protection yielding a maximum count of 15360 events equating to a DR of 83.7dB. Shot-noise limited operation together with zero parasitic light sensitivity global shutter operation are unique features of such digital pixels. Furthermore, HDR imaging is provided by noiseless frame summation in two 262kb SRAM banks. Use of SRAM achieves 20 times higher bit density than the in-pixel counters. An image processing block, operating at the oversampled internal frame rate interfaces the pixel array to the SRAM. It consists of a memory read block, adder/transform block and memory write block. Two HDR frame summation modes are implemented. In the first, image frames are accumulated in 32-bit lossless format using both SRAMs in parallel (Fig. 4). This requires integration to be paused for off-chip readout at 8fps with 12.5MHz system clock. In the second, a floating point 16-bit mode splits the SRAM into two banks operating in ping-pong fashion allowing continuous streaming of compressed data at higher frame rate of 15fps.

Time resolved imaging is made possible by an on-chip time gate generation circuit (Fig. 5) based on an open-loop ring oscillator (RO) with 0.001mm² area and 390ps resolution. User-programmable start/stop registers define a temporal region of interest (ROI) by width and time offset of the time-gate outputs. The RO has a coarse all-digital background frequency-drift compensation loop managed by the MCU counting RO clock periods within a system clock period and updating the time-gate start/stop registers. Moreover, the RO employs a self-reset function every system clock cycle to minimize accumulated jitter. The time gating circuit can generate two time gates A and B which are broadcast globally to the array via clock trees. The times gates can also be interleaved to odd and even columns to minimize motion distortion. Time gate C drives an external pulsed light source.

Experimental Results

Dynamic range is characterized as a function of the number of oversampled frames in Fig. 6 corresponding closely to photon shot noise theory (inset). Fig. 7 shows the time gating linearity and uniformity. A race condition between pixel read and reset signals has caused a corner of the array to be insensitive to light. Subsequent images have been cropped to the functional image area. FLIM was performed on a sample of Convallaria Majalis, using a 20X widefield Olympus IX71 microscope, with a Picoquant LDH, 485nm laser, the results (Fig. 8) showing accurate lifetime estimates. Median dark count rate is 15Hz at 1V excess above breakdown of 16.5V. HDR imaging was performed in bright conditions which cause single frames to be saturated (Fig. 9). The 30dB extension of DR is seen to recover detail in the clipped areas of the image. The table of comparison indicates that this array has the highest DR of all endoscopic sensors and the highest resolution of SPAD-based sensors for microendoscopy. At maximum activity, power consumption is 10mW from V_{DD} and 100mW from V_{HV}.

Acknowledgements-The PROTEUS project funded this work (EP/K03197X/1) with silicon manufacturing through the ENIAC POLIS project. We are grateful to Paul Dalgarno, Heriot-Watt University for access to microscopy lab facilities.

References

[1] M. Sousa et al., IEEE Sensors, 2017. [2] T. Al Abbas et al., IEDM, 2016. [3] M. Al. Rawhani et al., Nat. Sci. Reports, 2015. [4] P. Demosthenous et al., IEEE Trans. Biomed. Circ. Sys. 2016. [5] B. Mills et al., JoVE, 2017.

[6] https://www.ovt.com/sensors/OV6946

[7] http://www.toshibacameras.com/products/pdf/IKCT2.pdf.

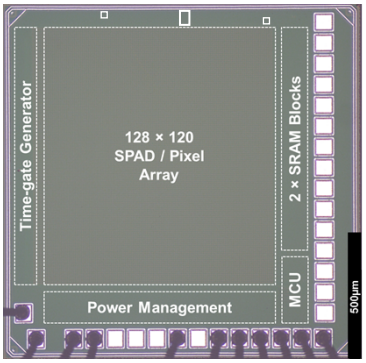


Fig. 1 Photomicrograph of the sensor top tier with bottom tier blocks overlaid. Additional 6 IO pads bonded for testability

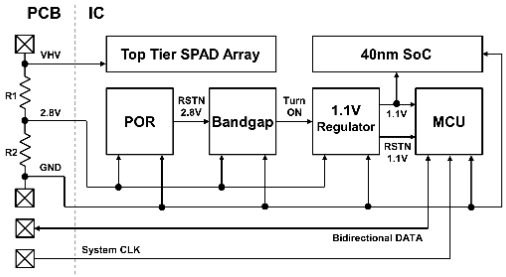


Fig. 2 Power management block showing 4-wire option

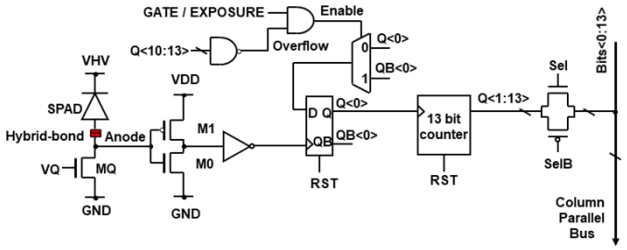


Fig 3 Pixel circuit

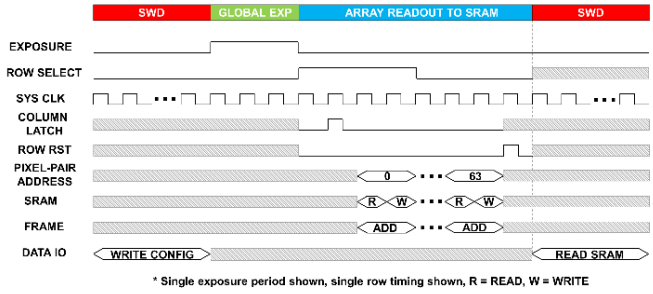


Fig. 4 System timing showing global shutter operation mode

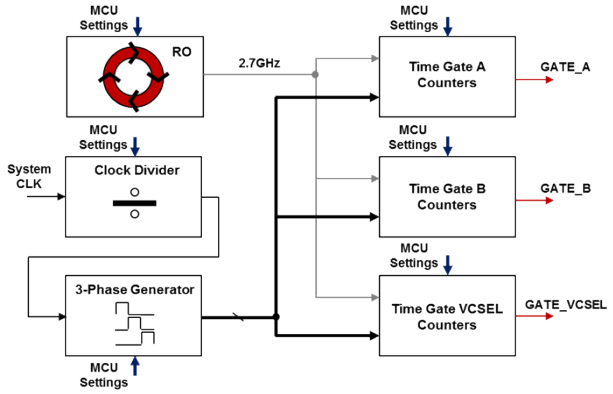


Fig. 5 Time gate generator

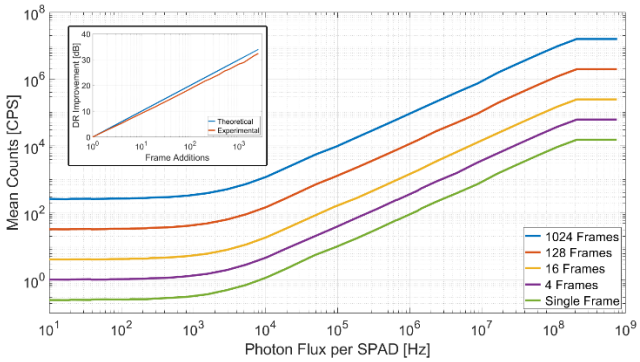


Fig. 6 Dynamic range extension by oversampling (V_{HV}=17.5V)

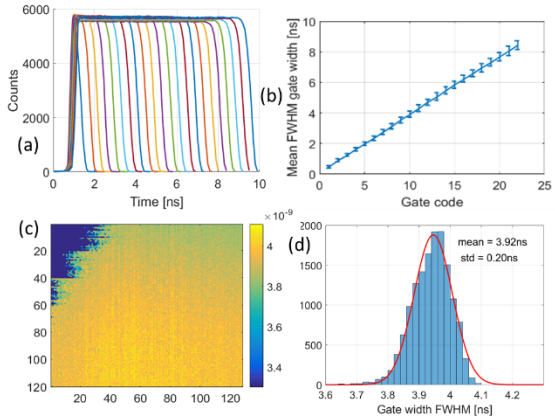
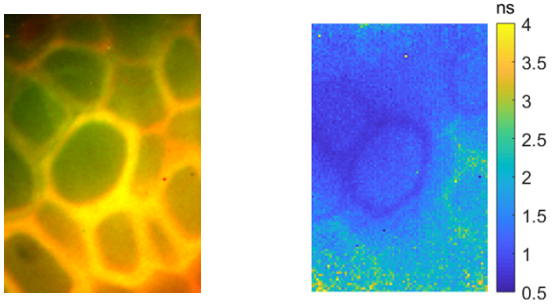


Fig. 7 Time gating characterization: (a) pixel (60,64), (b) Mean FWHM gate widths (c) across the pixel array (d) histogram of (c)



(a) 2 color intensity (b) fluorescence lifetime

Fig. 8 Fluorescence images from the sensor

(a) single frame (b) 8 summed (b) 128 summed

Fig. 9 Oversampled HDR images (total exposure 5ms)

	NanEye [1]	[3]	OV6946 [6]	IK-CT2 [7]	This work
Resolution	250 × 250	32x32	400 × 400	220 × 220	128 × 120
Type	CIS	SPAD	CIS	CIS	SPAD
Pixel Pitch	3µm	75µm	1.75µm	n/a	8µm
Technology	FSI	0.35µm HV	0.11µm BSI	BSI	3D-Stacked BSI
Frame Rate	42 to 55 fps	1 fps	30 fps	60 fps	15 fps
Full Well	15ke-	65k photons	n/a	n/a	15.36k photons
Dynamic Range	58 dB	96.2 DB	65.8 dB	n/a	126 dB
Shutter	Rolling	Rolling	Rolling	n/a	Rolling / Global
Connection Pins	4	68	4	n/a	5
Output Interface	LVDS	Digital	Analogue	n/a	Digital
Sensor Dimensions	1mm × 1mm	3.7mm × 3.7mm	0.95mm × 0.94mm	0.7mm × 0.7mm	1.4mm × 1.4mm
Intensity Imaging	Yes	Yes	Yes	Yes	Yes
Time-Resolved	No	No	No	No	**Yes**

Table I: Table of comparison