An Indirect Time-of-Flight SPAD Pixel with Dynamic Comparator re-use for a Single-Slope ADC

An Indirect Time-of-Flight SPAD Pixel with Dynamic Comparator re-use for a Single-Slope ADC

Kasper Buckbee[1,2], *Student Member, IEEE,* Neale A. W. Dutton[2], *Member, IEEE,* Robert K. Henderson[1], *Fellow, IEEE,*

[1]School of Engineering, Institute for Integrated Micro and Nano Systems, The University of Edinburgh, Kasper.Buckbee@ed.ac.uk

[2]STMicroelectronics Imaging Division, Edinburgh, UK

***Abstract*—This paper presents a 2-bin SPAD-based indirect time-of-flight (ITOF) pixel circuit with low power low-voltage differential clock distribution and a partially in-pixel single-slope ADC. An in-pixel dynamic comparator performs dual functions as a SPAD event-driven low-swing clock sampler and a comparator for self-referenced ADC conversion with digital delta reset sampling (DRS). The pixel achieves a full well capacity of 128 – 512 photons (6.83 – 8.82 ENOB), a low dynamic power consumption of 13.9-24.5 nW/MHz SPAD rate at a pitch of 7.2 µm in STMicroelectronics' 40nm CMOS and is 3D stacking ready.**

***Index Terms*—Analog counter, CMOS, single-photon avalanche diode (SPAD), analog to digital converter (ADC), dynamic comparator.**

I. Introduction

INNOVATION is required on the quest for ever higher resolution time-of-flight (TOF) imagers. Our previous work in [1] presented two analog counter based pixel designs with 2- and 4- in pixel time-bins (also called time gate or tap). This work builds on the 2-bin pixel design by adding the capability to perform a self-referenced single-slope analog to digital conversion (SS-ADC) – first reported in [2] – partially in-pixel. Fig. 1 shows the schematic of the proposed pixel design and its building blocks.

Recent advances in SPAD detector design have shrunk the SPAD pitch down to 6 µm [3] and the first 2D SPAD arrays at a similar pitch were reported in [2] and [3]. However, both pixel designs remain single-bin and leave the time-of-flight signal integration outside the pixel matrix. The smaller SPAD pitch results in lower detector power consumption but comes at the cost of reduced fill factor. To solve this issue [4] employs charge-focused SPADs to ensure a near 100% fill factor even at these small pitches. Therefore, to enable large resolution arrays of 1 MP and beyond the pixel circuitry must also be low power (< 1 µW/pix), have multiple bins (> 2), high count depth (> 9-bit) and match the small SPAD pitch.

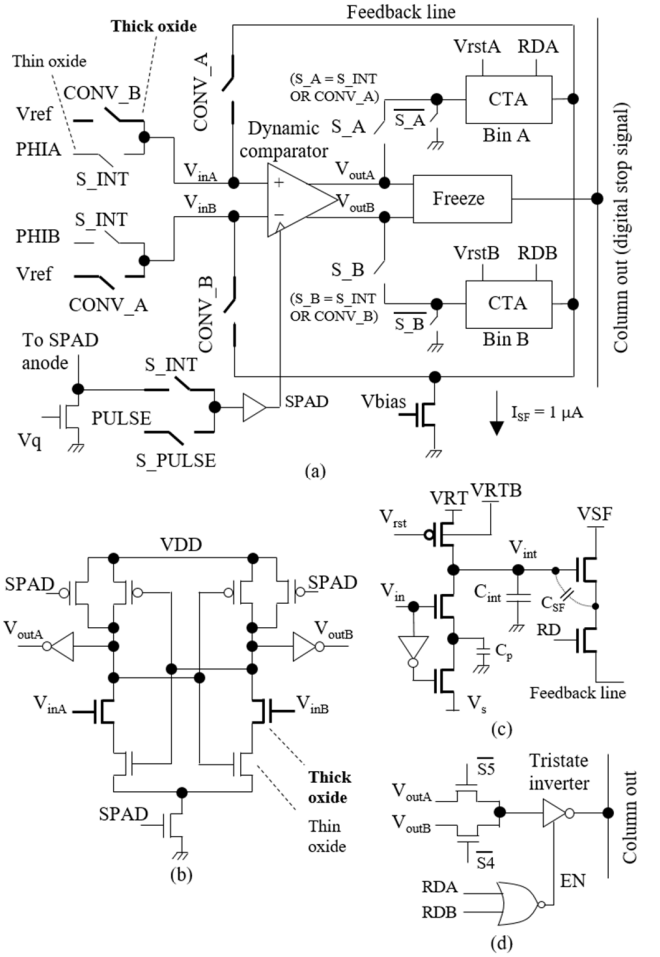

Figure 1. (a) Self-referenced pixel schematic which includes a SPAD front-end and is 3D-stacking ready, (b) schematic of the dynamic comparator with thick oxide input pair, (c) schematic of the CTA analog counter and (d) expanded schematic of the freeze logic block for generating a digital stop signal to the column line. For further detail on the dynamic comparator and CTA counters the interested reader is referred to our previous work in [1].

This paragraph of the first footnote will contain the date on which you submitted your paper for review, which is populated by IEEE. It is IEEE style to display support information, including sponsor and financial support acknowledgment, here and not in an acknowledgment section at the end of the article. For example, "This work was supported in part by the U.S. Department of Commerce under Grant BS123456." The name of the corresponding author appears after the financial information, e.g. *(Corresponding author: M. Smith).* Here you may also indicate if authors contributed equally or if there are co-first authors.

Kasper Buckbee is with the University of Edinburgh and ST Microelectronics Imaging Division, Edinburgh, Scotland (e-mail: Kasper.Buckbee@ed.ac.uk). Neale A. W. Dutton, is with ST Microelectronics Imaging Division, Edinburgh, Scotland (e-mail: Neale.Dutton@st.com). Robert K. Henderson is with University of Edinburgh, Edinburgh, Scotland (e-mail: Robert.Henderson@ed.ac.uk).

Our earlier work in [1] showed that smaller pitch pixels down to 4.8 µm, with multiple time bins and high count depths can be achieved in the analog domain. However, the drawback of analog domain pixels are the inherent noise issues present in their design, such as kT/C noise, leakage currents, counting non-linearity and pixel-to-pixel variations. Several analog domain pixels have been presented: [5] presented a time-gated 1-bin pixel with off-chip ADC conversion which was capable of 7-bit counting, but suffered from noise issues resulting from buffering the counter voltage off-chip. [2] presented a similar 1-bin time-gated pixel with self-referenced on-chip ADC conversion to allow for faster readout and first-order removal of pixel non-uniformities. This was achieved by buffering the analog counting voltage onto an on-chip column line, storing it on a sample and hold capacitor and comparing it to a ramp generated by the same pixel during conversion. However, a downside of this method is the increase of the capacitive load on the column line when the imager is scaled to higher resolutions, thus slowing down the ADC conversion and limiting frame rate. To solve these scalability issues our proposed pixel design includes the TOF signal integration and ADC partially in-pixel and contrary to [2] has a digital instead of analog column line. By re-using the in-pixel dynamic comparator for the ADC our analog line ("Feedback line" in Fig. 1) can be completely in-pixel. As a result there is no increase of the capacitive load when scaling the pixel to higher resolutions. Moreover, compared to [2] and [6], the use of low-swing clocks with a dynamic comparator significantly reduces the clock distribution power compared to full swing CMOS, as given similar driving circuitry the clock distribution losses are proportional to fCV^2 (where f is the clock frequency, C the capacitance of the metal line and V the clock voltage swing). Finally, through our proposed novel timing sequence the pixel benefits from a digital delta reset sampling (DRS) readout which omits the need for sample and hold capacitors in the column circuit.

II. Test Chip Overview

A test chip containing a 3x3 pixel test structure was manufactured in ST Microelectronics' 40 nm front-side illuminated (FSI) process. The pixel is 3D stacking ready and includes a SPAD front-end, but is tested on the bottom tier wafer only. Fig. 2 (a) shows a block diagram of the single-pixel test structure embedded in a 3x3 pixel matrix of dummy pixels to mimic the environment of a full imager and (b) the layout of the pixel. The pixel column line is connected to the column parallel circuit shown in (c) and consists of an up-down counter and logic to enable and choose its counting direction. It should be noted that only the first 9-bits of the counter are used in this work and the rest are redundant. Finally, Fig. 2 (d) shows a timing diagram of the column parallel circuit which performs digital DRS. This sequence is best understood by examining the pixels two modes of operation: first, as a time-resolved photon counter and second as a self-referenced SS-ADC. These two modes and the pixel circuit are discussed next.

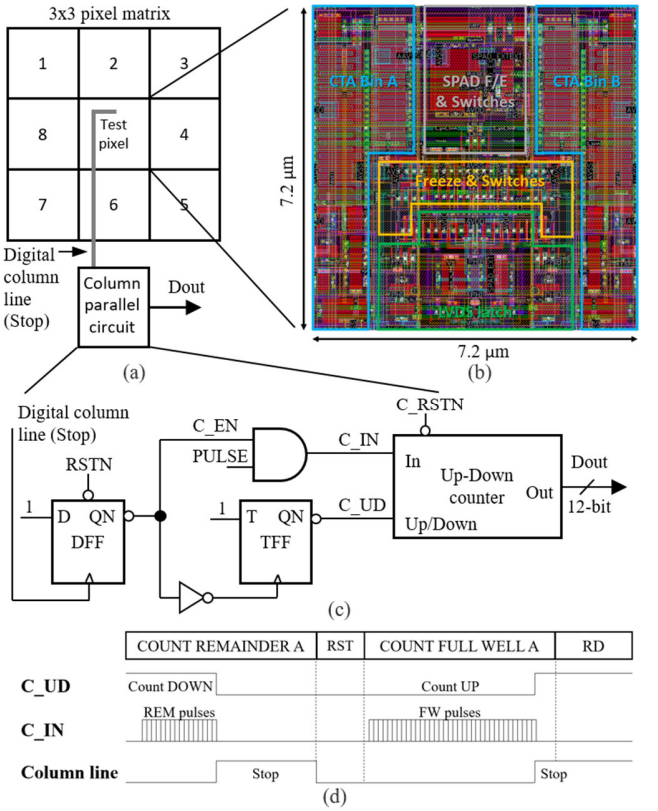

Figure 2. (a) Block diagram of the 3x3 pixel matrix and column parallel circuit, (b) pixel layout, (c) column parallel circuit with up-down counter for digital DRS readout and (d) timing diagram for the column parallel circuit.

A. The Pixel Circuit

The pixel shown in Fig. 1 (a) consists of three key blocks: Fig. 1 (b) shows the dynamic comparator with a thick oxide input pair (to handle an up to 2.5 V voltage swing at its input), (c) shows the charge transfer amplifier (CTA) analog counter (with C_{int} ~ 15 fF), and (d) the freeze logic block for producing a stop signal onto the column line. Additionally, the pixel has switches to change the functionality between photon-counting and ADC mode. Finally, it should be noted that the increased transistor count of this pixel and the need to use thick oxide devices for the dynamic comparator input pair and some of the switches increases the area compared to our previous 2-bin pixel at 4.8 µm (with no integrated ADC functionality).

B. TOF Pixel Operation

Referring to the timing diagram sequence in Fig. 3, the pixel operation starts as follows: first, both CTA's are reset after which the control signals are changed such that S_INT, S_A and S_B are high, CONV_A, CONV_B, S_PULSE, RDA and RDB are low and the pixel operates as a 2-bin time-resolved photon counter. In this mode the dynamic comparator operates as a SPAD-event driven front-end that resolves a pair of low-swing clocks PHIA and PHIB (200 – 600 mV_{p-p}) into one of two full-swing outputs V_{outA} and V_{outB} for each SPAD event. The time-resolved SPAD events are then counted by the analog counters as ΔV/event as shown on the V_{int} trace in Fig. 3.

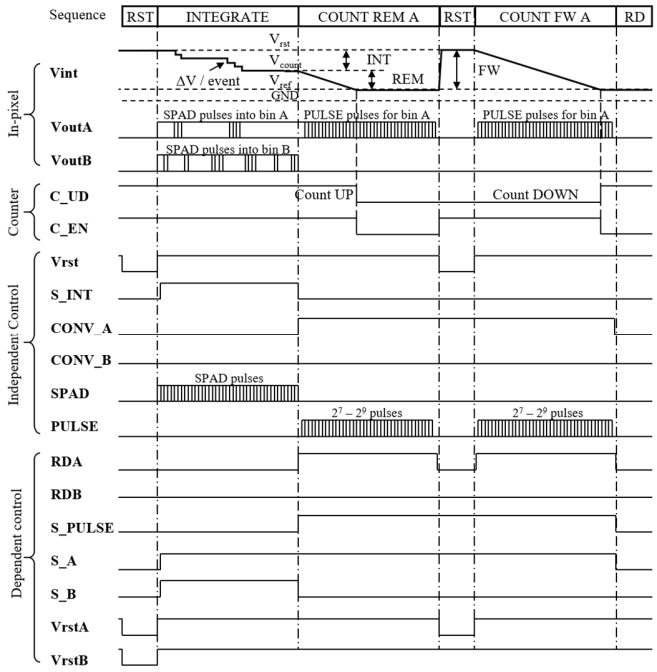

Figure 3. Timing diagram of the self-referenced pixel during integration and conversion of Bin A.

C. In-pixel Digital DRS Operation

Following integration, the DRS SS-ADC conversion starts with Bin A. The control signal states are changed such that CONV_A, S_A, RDA and S_PULSE are high and S_INT, CONV_B, S_B and RDB are low. The voltage in Bin B is held constant by grounding its input through a pull-down transistor. Now, instead of the low-swing clock signals, the dynamic comparator has been repurposed to monitor Bin A's counting voltage at its positive input and a reference voltage V_{ref} (0.5V – 0.6V) at its negative input. The trigger for the comparator has also been changed to an external PULSE source instead of the SPAD. The conversion is then performed in two steps as mentioned before: first the number of counts remaining in Bin A after integration (REM in Fig. 3) is determined with respect to the reference voltage V_{ref}. This occurs by comparing the voltage of Bin A against V_{ref} and if it is higher than V_{ref}, the comparator will trigger output V_{outA} for each PULSE trigger, thus decrementing the voltage in Bin A. At the same time every PULSE trigger decrements the up-down counter. Once the voltage of Bin A falls below V_{ref} the dynamic comparator will trigger V_{outB} instead, which is registered by the freeze logic block and results in a trigger on the digital column line. This causes the column parallel counter to be disabled and switch counting direction. Second, Bin A is reset and the full-well count (FW in Fig. 3) is determined against V_{ref} in the same manner. However, this time the up-down counter counts up instead of down. Therefore, the number of steps counted during integration (INT in Fig. 3) is derived by the counter according to:

$$INT = FW - REM. \quad (1)$$

An identical timing sequence is then used for the conversion of Bin B, with the comparator inputs swapped. This occurs by changing the control signals such that CONV_B, S_B, RDB and S_PULSE are high and S_INT, CONV_A, S_A and RDA are low. Therefore, it takes four ramp durations and two readouts to convert both bins. It should be noted that any variability between the SPAD and PULSE pulses can cause an error due to different pulse shapes driving the comparator and therefore the analog counters, thus modulating their step size. To resolve this issue a pulse shaper as used in [6] can be implemented with a slight area penalty as the tradeoff.

III. Measurement Results

The measurement setup used to test the pixels was automated with Python scripts and a XEM7310 FPGA was used to generate emulated SPAD and timing pulses to the pixel. All experiments were carried out at room temperature.

A. Counting Results

Fig. 4 shows a summary of the pixels counting performance in 7-bit and 9-bit counting mode, where:

a) Shows the combined histograms of the first 10 counts of the pixel in 7-bit counting mode. Each color represents the distribution of output codes for one fixed input photon count and a Gaussian overlay has been overlaid for clarity. The read noise of the 9th count (light blue) is 0.48 LSB and indicates the precision of the pixel.

b) Shows the combined histograms of the last 10 counts of the pixel in 7-bit counting mode. The read noise of the 128th count (light blue) is 0.47 LSB. This suggests that cumulative noise during integration is not the dominant noise contributor of the pixel in 7-bit mode.

c) Shows the full scale range of the pixel in 7-bit and 9-bit counting mode. The pixel full scale range can be adjusted by varying the CTA bias voltage V_s and is set to V_s = 0 mV in 7-bit mode and V_s = 400 mV in 9-bit mode. The bin-to-bin count error is < 5 % of each full-scale range.

d) Shows the measured and simulated accuracy of the pixel calculated as the difference between the output code and the input counts. It ranges from +2 to -75 and is caused by two main factors: first, step size modulation between the INT and FW counting sequences due to an effective change in C_{int} caused by different capacitive coupling of C_{SF} when the source follower is on versus off (see Fig. 1b). Second, kick-back from the dynamic comparator on the feedback line during FW conversion, causing incomplete settling and thus effectively modulating the step size. These errors also result in the ENOB being reduced (i.e. for 7-bit mode the ENOB becomes $\log_2(128\text{-}14)$ = 6.83 bits). However, this error can be compensated with a look-up table.

B. Timing and Power Results

Fig. 5 a) shows the pixel time bin characterization transitioning from Bin B to Bin A with 100 input counts and is plotted for two different clock swings of 200 mVpp and 400 mVpp. The increased clock swing improves the bin-to-bin transition time from ~100 ps to ~60 ps but will also increase the power consumption of the clock distribution network.

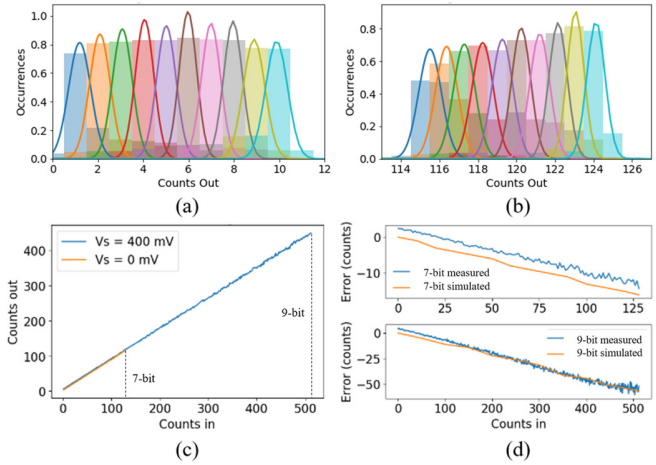

Figure 4. Counting performance: (a) shows histograms of the first 10 counts in 7-bit mode, (b) histograms of the last 10 counts in 7-bit mode, (c) full scale range in 7- and 9-bit mode and (d) error counts in 7- and 9-bit mode.

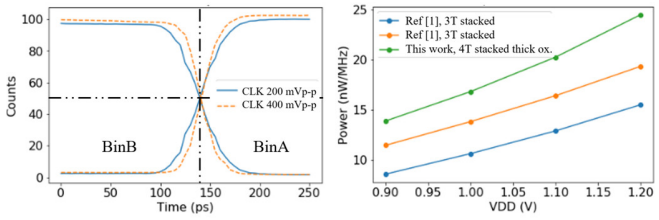

Figure 5. (a) Time bin characterization with a clock swing = 200 mV (blue) and 400 mV (orange), (b) dynamic comparator power consumption (green, thick oxide input pair) compared to our previous work in [1] (both thin oxide).

It can also be seen that the transition between the two bins occurs at half of the input counts and thus a near 100% demodulation contrast is achieved. It should be noted that an offset error between the two bins can be seen in the plot, but can be corrected by use of a look-up table. Fig. 5 b) shows the power consumption of the dynamic comparator which is slightly increased compared to our previous work in [1]. This is due to the thick oxide input pair causing an increased internal node capacitance therefore increasing the power. Fig. 6 shows a power breakdown of the pixel scaled up to a 1 MP array and shows that the overall power consumption is dominated by the comparators (4.6 – 8.1 mW/MHz SPAD frequency), followed by the in-pixel current sinks (60 mW) and lastly the analog counters (0.026 mW). Thus, assuming a frame rate of 30 fps at a 33% duty cycle the array would consume between 87 mW - 812 mW depending on incident light level.

IV. Conclusion

Compared to our previous work in [1] this pixel design has a comparable power consumption while extending the counting range of the pixel to 9-bits compared to [2]. It implements a novel timing sequence to allow for a digital DRS readout scheme and makes use of a dynamic comparator and low voltage clocking scheme to save on clock distribution power compared to [6]. Furthermore, compared to [2] the pixel has a completely in-pixel analog feedback line allowing easy scale-up to large resolution

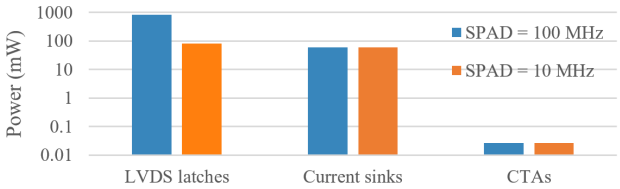

Figure 6. Power breakdown of the pixel when scaled to a 1 MP array.

TABLE I
COMPARISON TO STATE OF THE ART

	This work		[2] JSSC 2016	[1] IISW 2021	[1] IISW 2021	Park [3] JSSC 2021	Dutton [6] IISW 2013
Readout method	Self-referenced readout			Non-self-referenced readout			
Technology (nm)	**40**		350	40	40	110	130
Bins per pixel	**2**		1	2	4	2	1
Pixel pitch (µm)	**7.2**		15	4.8	7.1	32	9.8
Bit depth (bit)	**7**	**9**	8	7 – 10	7 – 10	9	6
Area per bit (µm²/bit)	**3.24**	**2.80**	22.2*	1.65 – 1.15	1.80 – 1.26	26.2*	15.5*
ENOB (bit)	**6.83**	**8.82**	5.40	7.10 – 10.0	7.00 – 10.0	-	6.6
Step size (mV)	**13****	**4****	16.5	13.7 – 1.86	13.6 – 1.94	1.5	13.1
Pixel noise (mV)	**6.11*****	**7.6*****	1.3	1.9	2.6	-	0.4
Input referred noise (Step = e- equiv.)	**0.47*****	**1.90*****	0.08	0.1 – 1.0	0.2 – 1.3	< 0.7	0.03
Per pixel dynamic power (nW/MHz)	**13.9 – 24.5**		-	8.60 – 19.3	17.1 – 38.6	-	-
Predicted 1 MP array power (mW/MHz)	**4.60 – 8.10**		-	2.80 – 6.40	5.60 – 12.8	-	-

*Pixel area estimated from reported pixel fill factor and chip micrographs. ** Simulation estimate. *** Includes ADC noise.

arrays without affecting its capacitive load and conversion speed. The column line is purely digital and functions as a trigger to a column parallel up-down counter that performs digital DRS and allows for a single readout per pixel bin. Furthermore, the pixel demonstrates the re-use of an in-pixel dynamic comparator for ADC functionality reducing the area required for additional column-parallel circuitry. Finally, Table 1 presents a comparison to the state of the art.

Acknowledgment

The authors would like to acknowledge the support of David Poyner, Clive Brown, Catherine Popon and Sara Pellegrini from ST Microelectronics.

References

[1] K. Buckbee, N. A. W. Dutton, and R. K. Henderson, "SPAD based Time of Flight Pixel Circuits for Large Scale Arrays," in *IISW 2021*, 2021, pp. 3–6, [Online]. Available: https://imagesensors.org/Past Workshops/2021 Workshop/2021 Papers/P19.pdf.

[2] M. Perenzoni *et al.*, "A 160 × 120 Pixel Analog-Counting Single-Photon Imager With Time-Gating and Self-Referenced Column-Parallel A / D Conversion for Fluorescence Lifetime Imaging," *IEEE J. Solid-State Circuits*, vol. 51, no. 1, pp. 155–167, 2016, doi: 10.1109/JSSC.2015.2482497.

[3] S. Shimada *et al.*, "A Back Illuminated 6 µm SPAD Pixel Array with High PDE and Timing Jitter Performance," in *IEDM 2021*, 2021, pp. 446–449.

[4] K. Morimoto *et al.*, "3 . 2 Megapixel 3D-Stacked Charge Focusing SPAD for Low-Light Imaging and Depth Sensing," in *IEDM 2021*, 2021, pp. 450–453.

[5] N. A. W. Dutton, L. A. Grant, and R. K. Henderson, "9.8um SPAD-based Analogue Single Photon Counting Pixel with Bias Controlled Sensitivity," *Int. Image Sens. Work.*, pp. 7–10, 2013, [Online]. Available: http://www.imagesensors.org/Past Workshops/2013 Workshop/2013 Papers/06-3_068-Dutton_Paper.pdf.

[6] B. Park *et al.*, "A 64 × 64 SPAD-Based Indirect Time-of-Flight Image Sensor with 2-Tap Analog Pulse Counters," *IEEE J. Solid-State Circuits*, vol. 56, no. 10, pp. 2956–2967, 2021, doi: 10.1109/JSSC.2021.3094524.