High Step-down Bridgeless Sepic/Cuk PFC Rectifiers with Improved Efficiency and Reduced Current Stress

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***Abstract*—Two high step-down bridgeless power factor correction (PFC) rectifiers based on the switched inductors network (SIN) are introduced in this paper. The proposed rectifiers employ the SIN to provide high step-down voltage gain with a higher duty cycle than the competitors. They also offer higher efficiency, lower current stress and total peak switching device powers. A thorough and straightforward design algorithm in the discontinuous conduction mode (DCM) is provided that ensures a unity power factor and a low total harmonic distortion (THD) with a simple control scheme. As a demonstration of the superior performance of the proposed rectifiers, a 300W high-gain sepic rectifier setup, with 48V_{dc} output voltage from a 230V_{rms}/50Hz source is built in the laboratory.**

***Index Terms*—Efficiency, high step-down, PFC rectifier, switched-inductor network.**

I. Introduction

A few examples of PFC rectifiers in use are telecom power supplies, electric vehicles (EVs), adapters/chargers, LED drivers, and uninterruptible power supplies (UPSs) [1]–[8]. The common configuration of the PFC rectifiers consists of a full bridge diode rectifier followed by a DC-DC chopper, dominantly the boost circuit [9], [10]. The main problem with this configuration is that the output is always higher than the rectified voltage, which necessitates the integration of a step-down DC-DC chopper in the final topology, as shown in Fig. 1. The added circuitry increases the power loss, cost, and volume of the converter [11], [12]. If the boost PFC is replaced by a step-down circuit, aiming to tackle the aforementioned problem, then the quality of the input current deteriorates drastically due to the dead angle problem, illustrated in Fig. 2. In fact, when the output voltage is higher than the input AC voltage, the step-down chopper cannot operate and periods of zero current appears around the zero-crossings of the AC waveforms. An auxiliary converter, such as the buck-boost or the flyback, can be connected in parallel or series to enhance the quality of the input current. [12], [13]. The price is again added cost, volume and loss of the final converter [13]. The converters with buck-boost ability, such as the buck-boost, the cuk, and the sepic can be used for the PFC stage. These converters offer the step-down capability as well as a high-quality input current and avoid the additional stage for decreasing the output voltage [14]–[22]. Since the internal capacitors in the sepic and cuk converters participate in energy transfer, these converters have already been proven as better solutions than the buck-boost one [20]. On the other hand, in those applications, such as battery chargers, and telecom power supplies, where a low output voltage is needed, the switch on-time becomes too short. This poses a practical limit on the maximum switching frequency that can be achieved with these circuits [20], [23]. Furthermore, as a result of the low duty cycle, current stresses are increased. As the PFC rectifiers presented in [14]–[19], [21], [22] suffer from a limited step-down gain, they cannot be considered as a viable solution in low output voltage applications. The rectifier proposed in [20] solves this problem at the expense of a greater number of semiconductors in the current path. Also, possible differences in output inductors result in voltage spikes across the output diodes. There are some high step-down PFC rectifiers based on the buck converter [24]–[28]. These converters provide high step-down gains with great number of components. As expected, the quality of the input current is low, which is mainly due to the dead angle problem of the input current. Also, the reported efficiencies are lower than the conventional solutions.

Regardless of the chosen circuit topology, PFC rectifiers can be controlled in either discontinuous conduction mode (DCM) or continuous conduction mode (CCM). The DCM operation offers better closed-loop control performance with a simple single-loop control, which makes it easier to be designed/analyzed and even implemented in practice [13], [21]. However, for a given voltage gain the duty-cycle of DCM operation is smaller than the CCM one. As a result, the problems mentioned above about the very short on-time of switches at high switching frequencies becomes even worse.

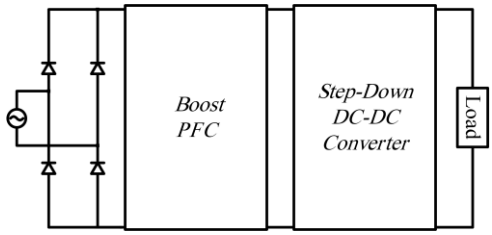

Fig. 1. Conventional boost PFC rectifier with step-down DC-DC converter.

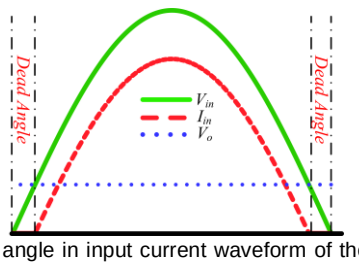

Fig. 2. Dead angle in input current waveform of the buck PFC rectifiers.

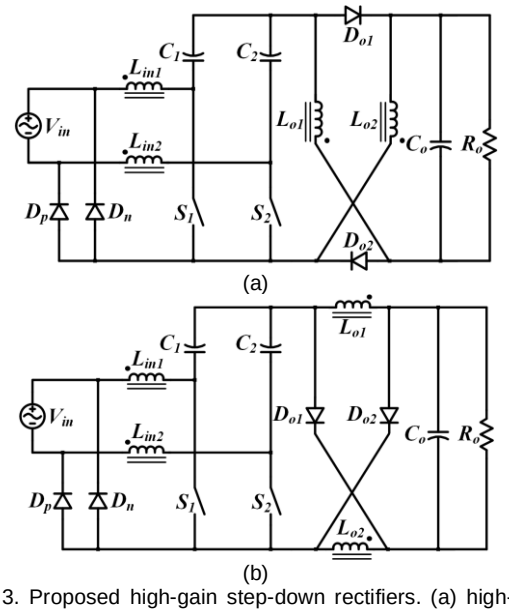

Fig. 3. Proposed high-gain step-down rectifiers. (a) high-gain sepic, and (b) high-gain cuk PFC rectifiers.

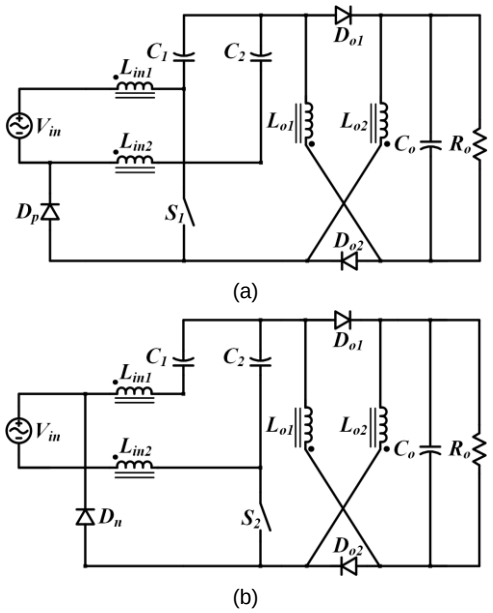

Fig. 4. Equivalent circuits for the proposed high-gain sepic PFC rectifier during: (a) positive half-cycle and (b) negative half-cycle of the input voltage.

The conventional buck-boost converter cannot provide a high step-down voltage gain. In order to overcome the problems mentioned above, this paper proposes two bridgeless sepic and cuk PFC rectifiers integrated with a switched inductor network (SIN). Thanks to the SIN, the proposed rectifiers provide a high step-down voltage gain, such that the problem of the low duty cycle is effectively avoided, even under DCM operation. So, the operation principles and components design procedure are developed for the DCM mode to take advantage of the small power losses of the switches at turn on, and the diodes at turn off transitions. The proposed rectifiers offer lower current stresses, conduction and switching losses, and total peak switching device powers (SDP_{peak}) [29] and [31] than the conventional PFC rectifiers. To support the theoretical analysis of the proposed rectifiers and show their superior performance, a 300W high-gain sepic rectifier setup, with $48V_{dc}$ output voltage from a $230V_{rms}$/50Hz source is built in the laboratory. In section II, the configuration of the proposed rectifier and operation modes are presented followed by a straightforward components design algorithm given in section III. Various comparative studies are presented in section IV. The experimental results are reported in section V. Section VI concludes the paper.

II. Proposed PFC Rectifiers

A. Circuit Configuration

The proposed PFC rectifiers are shown in Fig. 3. These circuits are mainly inspired by the converters proposed in [21] and [30]. The proposed topologies consist of switches S_1 and S_2, diodes D_{o1} and D_{o2}, and two low-frequency diodes D_p and D_n. Other components are two pairs of coupled inductors, L_{in1}-L_{in2}, and L_{o1}-L_{o2}, and two capacitors C_1 and C_2. The input and output inductors share a common core to reduce the size of the converter. It will be shown later that high step-down conversion is achieved for both proposed rectifiers with minimum losses and reduced current stresses. The sepic (cuk) derived circuit is formed by connecting two high-gain sepic (cuk) converters for each half-line cycle. The switches S_1 and S_2 can be easily driven by the same gating signal. Also, their emitters are at the same potential, so just one isolated gate diver is needed, which highly simplifies the modulation and drive circuit. The operation of both PFC rectifiers is similar and for the sake of saving space and better presentation, only the sepic circuit is analyzed in this section. However, the results are the same for both sepic and cuk rectifiers. The equivalent circuits of the sepic rectifier during the positive and negative half-line cycles are shown in Fig. 4(a) and Fig. 4(b), respectively.

B. Principle of Operation

In order to simplify the steady-state analysis of the proposed rectifier, it is assumed that the output capacitor C_o and input inductors L_{in1} and L_{in2} are large enough such that the output voltage and the input current can be assumed almost constant during a switching period. Because of the symmetry of the circuit, just the positive half-cycle operation is analyzed. The rectifier works in DCM mode to take benefit of many advantages such as the near-unity power factor with a single control loop, and zero turn-on and zero turn-off of the switches and the high-frequency output diodes, respectively. The operational modes and theoretical waveform of the proposed sepic PFC rectifier are shown in Fig. 5 and Fig. 6, respectively. The capacitors voltage equations can be written as:

$$V_{C_1} = \begin{cases} v_{in}(t) + V_o & 0 \le t \le \dfrac{T}{2} \\ V_o & \dfrac{T}{2} \le t \le T \end{cases} \quad (1)$$

$$V_{C_2} = \begin{cases} V_o & 0 \le t \le \dfrac{T}{2} \\ v_{in}(t) + V_o & \dfrac{T}{2} \le t \le T \end{cases} \quad (2)$$

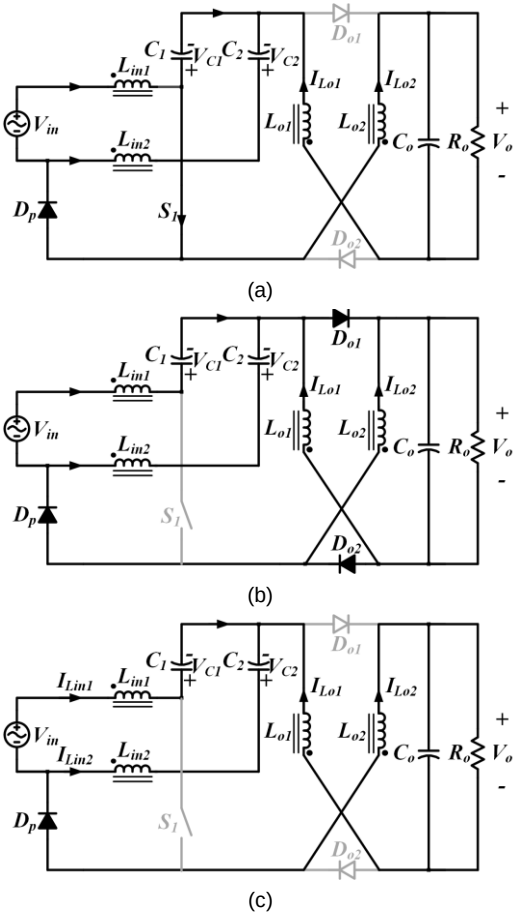

Fig. 5. Operation modes: (a) I (b) II (c) III of the proposed sepic PFC rectifier.

where T is the period of the input voltage and V_o is the output voltage. As can be seen in Figs. 5 and 6, the converter operation during a switching period can be divided to three modes, analyzed below.

a) Mode I: [t_0~t_1]

In this mode, S_1 is turned on, as shown in Fig. 5(a). The diode D_p is forward biased and conducts too and the output diodes are blocking. The currents through input and output inductors are increasing linearly, as shown in Fig. 6. The voltage equations of this mode can be written as

$$V_{L_{in1}} = V_{L_{in2}} = v_{in} \tag{3}$$

$$V_{L_{o1}} = V_{L_{o2}} = \frac{v_{in}}{2}. \tag{4}$$

The switch current is the sum of the input and the output inductors'. The peak of switch current can be then written as

$$I_{s_1}^{max} = \frac{V_m}{L_e} DT_s \tag{5}$$

where T_s is the switching period, V_m is the peak amplitude of the input voltage and L_e is defined as

$$\frac{1}{L_e} = \frac{2}{L_{in}} + \frac{1}{2L_{o1}}. \tag{6}$$

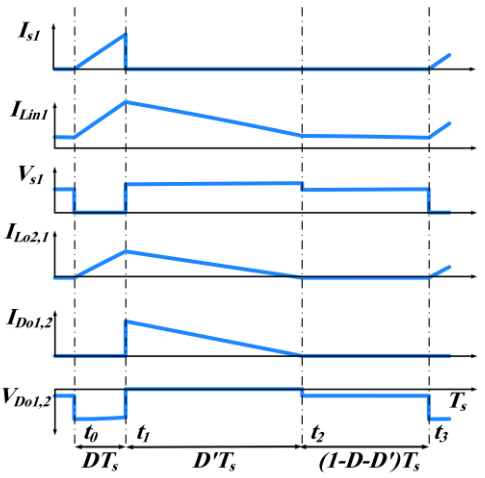

Fig. 6. Theoretical waveforms during one switching period in positive half-cycle for the sepic high-gain PFC rectifier with DCM operation.

b) Mode II: [t_1~t_2]

As in Fig. 5(b), at the beginning of this mode S_1 is turned off, and the output diodes D_{o1} and D_{o2} start conducting to provide a path for the inductors' currents. Diode D_p remains on. The currents through the input and output inductors are decreasing linearly, as shown in Fig. 6. The voltage equations can be written as

$$V_{L_{in1}} = V_{L_{in1}} = -2V_o \tag{7}$$

$$V_{Lo1} = V_{Lo2} = -V_o. \tag{8}$$

This mode ends when the currents through the output diodes reach zero and consequently, these diodes turn off at zero current. The normalized length of this interval is given by

$$D' = \frac{D}{2M}\sin(\omega t) \tag{9}$$

where ω is the source angular frequency, and M is the voltage gain and defined as

$$M = \frac{V_o}{V_m}. \tag{10}$$

c) Mode III: [t_2~t_3]

In this mode, the output diodes and the main switches are off. Diode D_p is still on. The currents of the inductors are constant, and the voltages across inductors are zero.

Thanks to the DCM operation of the proposed rectifiers, the problems arising from inequality of the output inductors, such as the voltage spikes across the semiconductors, are avoided. So, the additional energy of the output inductors caused by unequal inductances can be discharged safely in Mode III.

III. Analysis And Design

A. Voltage Gain

To make a better comparison with other rectifiers, the equations of the proposed rectifiers are rewritten in accordance with [16] and [21]. The voltage gain, already defined in (10), can be found by calculating the average current of the output diode. From Fig. 5, the average current of the output diode over one switching cycle can be written as

$$\bar{i}_{D_{o1}} = \frac{D^2 T_s v_{in}^2}{8 L_e V_o}. \quad (11)$$

On the other hand, the average current over one cycle of the voltage source is

$$I_{D_{o1}} = \frac{D^2 T_s V_m^2}{4 L_e V_o} = \frac{V_m^2}{2 R_e V_o} \quad (12)$$

where R_e is defined as

$$R_e = \frac{2L_e}{D^2 T_s}. \quad (13)$$

At steady-state, I_{Do1} equals the average current through the output resistor, R_o. So, the voltage gain yields as

$$M = \sqrt{\frac{R_o}{R_e}} = \sqrt{\frac{R_o D^2 T_s}{8 L_e}} = \frac{D}{\sqrt{2K_e}} \quad (14)$$

where K_e is defined as

$$K_e = \frac{4L_e}{R_o T_s}. \quad (15)$$

In DCM operation mode, one can readily conclude that

$$D' < 1 - D. \quad (16)$$

By using (14), (15) and (16) the following condition for DCM operation is then obtained

$$K_e < K_{e,crit} = \frac{1}{2(M + \frac{\sin(\omega t)}{2})^2} \quad (17)$$

and to ensure DCM operation during the whole line period, $K_e < K_{e,crit\_min}$ must be satisfied. $K_{e,crit\_min}$ is defined in (18).

$$K_{e,crit\_\min} = \frac{1}{2(M + 0.5)^2} \quad (18)$$

For the sake of a better representation, $K_{e,ratio}$ is defined as:

$$K_{e,\text{ratio}} = \frac{K_e}{K_{e,crit\_\min}} \quad (19)$$

therefore, $K_{e,\text{ratio}} < 1$ ensures DCM operation.

By writing the voltage-second balance, the voltage gain in the CCM mode can be calculated from (4) and (8) as

$$M_{CCM} = \frac{D}{2(1-D)}. \quad (20)$$

According to (20), the output voltage gain of the proposed rectifier is lower than those of the Sepic rectifiers presented in [19] and [21]. So, at the same output voltage, the duty cycle of the proposed rectifier is higher than the competitors'.

B. Component Design

1) Passive Components:

The values of the inductors L_{in1} and L_{in2} are designed based on their maximum current ripples ($\Delta I_{Lin1,2}$), as below

$$L_{in1,2} = \frac{1}{\Delta I_{Lin1,2}} \frac{V_m D T_s}{\sqrt{2} P_o}. \quad (21)$$

where P_o is the output power.

As mentioned above, if $K_{e,\text{ratio}} < 1$ the converter works in DCM mode. By using (18) and (19) one can calculate K_e. The inductors L_{o1} and L_{o2} are then designed by using equations (6), (15) and system parameters. The *LC* circuit across the input, as shown in Fig. 5, consists of the input capacitors and the inductors of the proposed rectifiers. Any possible resonance may deteriorate the quality of the input current. According to [16], the capacitors C_1 and C_2 of the proposed rectifies are designed from (22).

$$C_{1,2} = \frac{1}{(2\pi f_{res})^2 \times (L_{in1} + L_{o1})} \quad (22)$$

For a safe operation, the resonance frequency, f_{res}, must be much higher than the source frequency, f_{in}, and enough lower than the switching frequency, f_s, i.e.

$$f_{in} < f_{res} < f_s. \quad (23)$$

The peak voltage across capacitors can be written as

$$V_{C1,2}^{max} = V_m + V_o. \quad (24)$$

On the other hand, the output capacitor is designed according to tolerable ripple at the nominal power, as given in (25) where *%r* is the output voltage ripple ratio.

$$C_o = \frac{P_o}{2\pi f_{in} \%r \, V_o^2} \quad (25)$$

2)Active Components:

In the following, the semiconductors ratings of the proposed rectifier are calculated to select proper semiconductor elements.

The maximum voltage stresses across the semiconductors can be written as (26)

$$\begin{cases} V_{S1,S2}^{max} = V_m + 2V_o \\ V_{Do1,Do2}^{max} = \frac{V_m}{2} + V_o \\ V_{Dp,Dm}^{max} = V_m. \end{cases} \quad (26)$$

The current stresses are also calculated as

$$\begin{cases} I_{S1,S2}^{max} = \frac{2P_o}{V_m} + \frac{V_m D T_s}{2L_{o1}} \\ I_{Do1,Do2}^{max} = \frac{V_m D T_s}{2L_{o1}} \\ I_{Dp,Dm}^{max} = \frac{2P_o}{V_m}. \end{cases} \quad (27)$$

In this section, the design of passive and active components is investigated. The converter components for the experimental prototype can be determined by using equations (1)-(27).

COMPARATIVE ANALYSIS

This section presents a comparative study that is accompanied by experimental results. The proposed rectifiers are compared with the buck-boost rectifiers presented in [15]–[21]. The number of passive components, the number of semiconductors in the current path, the voltage gain, and the total voltage stresses are compared in Table I. The proposed rectifiers provide a high step-down voltage gain in comparison to others while the number of components is comparable with them. The total voltage stresses of the semiconductors of the competitors are normalized based on those of the proposed rectifiers. The results show that the proposed rectifiers offer acceptable total voltage stresses compared to the others. For the sake of a fair comparison, all converters are designed with the same $K_{e,ratio}$, input and output voltages and output power. The current stress,

TABLE I
COMPARISON AMONG VARIOUS PFC RECTIFIERS

Feature		Proposed Sepic and Cuk	Buck boost of [15]	Buck boost of [16] (Type I)	Buck boost of [16] (Type II)	Buck boost of [17]	Sepic of [19] and [18]	Cuk of [20]	Sepic and Cuk of [21]
No. of switches		2	2	2	2	2	2	1	2
No. of fast diodes		2	4	2	2	4	1	2	1
No. of slow diodes		2	-	-	-	-	2	4	2
No. of inductors		4	3	3	3	3	2	3	3
No. of magnetic cores		2	3	2	2	3	2	3	3
No. of capacitors		3	3	3	3	3	2	2	3
No. of semiconductors in current path	Mode I	2	2	2	2	2	3	3	2
	Mode II	3	1	2	2	1	3	4	2
	Mode III	1	0	1	1	0	2	2	1
Voltage gain in, CCM mode		$\frac{D}{2(1-D)}$	$\frac{2D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{1-D}$	$\frac{D}{2(1-D)}$	$\frac{D}{1-D}$
Calculated efficiency (%)		94.8	88.3	93	93.1	89.9	92.9	94.2	93.7
Ratio of current stress of main switch. $I_{s,peak}$ / $I_{s,peak,\ Proposed}$		1	3.2	1.7	1.8	1.71	1.8	1	1.7
Ratio of SDP,peak $\sum SDP,peak$/ $\sum SDP,peak$, *proposed*		1	3.5	2	2	2.8	1.3	0.7	1.5
Ratio of total voltage stress of semics. ∑Vs / ∑Vs_proposed		1	1.07	0.78	0.78	1.12	0.97	1.24	0.92

the total peak switching device powers (SDP_{peak}) and the total power losses are calculated by using the PLECS simulations. According to [31] the SDP of a switching device is expressed as the product of its voltage and current stresses. The SDP_{peak} is defined as the aggregate of SDPs of all the switching devices used in the circuit. SDP_{peak} is a measure of the total semiconductor device requirement, thus an important cost indicator of a converter. The results are shown in Table I. The proposed rectifiers almost have the lowest current stresses and SDP_{peak}. As a result, the implementation cost of the proposed rectifiers is lower than the competitors. By doing the power loss calculations reported in [23], [32] and assuming the same components with the same parasitic parameters and conditions, the total power losses of rectifiers are compared too, and the results are shown in Fig. 7. As seen from this figure, the proposed rectifiers offer the lowest power loss compared to all other rectifiers. Also, the comparison of loss distribution among various PFC rectifiers is shown in Fig. 7. The rectifiers presented in [24]–[28] provide a high step-down gain based on the buck converter. These rectifiers have too many components. Furthermore, the input current quality is low with high harmonic contents due to the dead zone of the input current with the buck PFC converters. Also the rectifiers proposed in [24]–[28] suffer from lower efficiency than the proposed rectifiers. So, it is safe to conclude that the proposed rectifiers provide a high step-down gain with reduced current stresses, total power losses, and a high-quality input current.

IV. EXPERIMENTAL VERIFICATION

A laboratory prototype is implemented to validate the performance and analytical results of the proposed rectifier. The prototype sepic rectifier is shown in Fig. 8. The parameters of the proposed rectifier and the test conditions are reported in

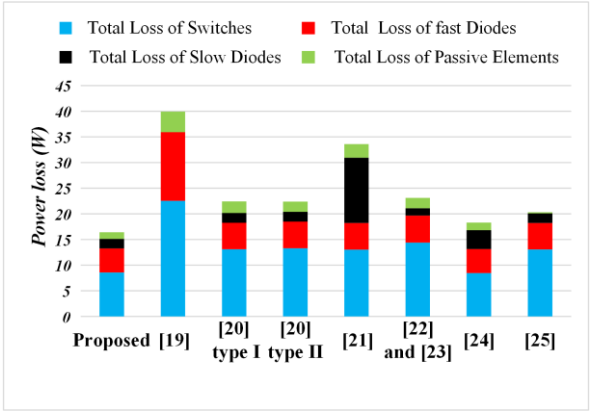

Fig. 7. Comparison of loss distribution among various PFC rectifiers.

TABLE II
EXPERIMENTAL CONDITIONS AND PARAMETERS

Parameters	Value
Output power, P_o	300 W
Output voltage, V_o	48 V_{dc}
Input voltage, v_{in} /f_{in}	230 V_{rms}/ 50Hz
Switching frequency, f_s	65 kHz
Input inductors, $L_{in1,}$ & L_{in2}	4 mH
Output inductors, L_{o1}, & L_{o2}	30.2 µH
Inner capacitors, C_1, & C_2	1 µF, 275 V_{ac}
Output capacitor, C_o	6800 µF, 50V
Switches, S_1, & S_2	FGW85N60RB
Output diodes, D_{o1}, & D_{o2}	FFSH5065A
Low frequency diodes, D_p & D_m	SF5L60U

Table II. The output voltage is assumed 48 V_{dc}. This output voltage is a standard value in industrial applications like a telecom power supply. To have a high-quality input

current, the output inductors are designed based on equations (6)-(20) to ensure DCM operations.

The input and output inductors are specified in Fig. 8. Furthermore, they are wound on a common magnetic core. As a result, the volume and cost of the converter are reduced. The output inductors wound on the left and right limbs of a EE42 ferrite core. The air gap is inserted on both the left and right sides. The values of input inductors are calculated from (21). The input and output capacitors are designed based on equations (22)-(25). The semiconductors are selected based on equations (26) and (27).

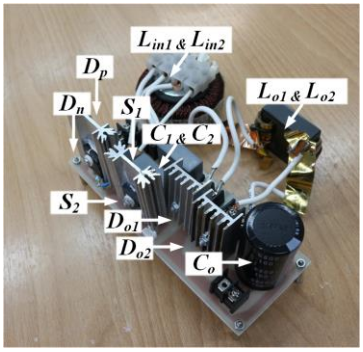

Fig. 8. The experimental prototype.

To provide experimental results, a STM32F407VG discovery board from STMicroelectronics and gate driver circuits are used to generate the PWM pulses in an open-loop control system. The steady-state waveforms of the input and the output voltage and current of the proposed sepic rectifier are shown in Fig. 9. The input 230 V_{rms} voltage is well converted to 48 V_{dc}, as shown in Fig. 9(a). The output voltage has an acceptable ripple of less than 6%. The input current (i_{in}) and the output current (I_o) are shown in Fig. 9(a). The input current is a highly sinusoidal waveform with the measured THD of 4.4% at 300W.

The voltage across the capacitor C_1 (v_{C1}), the voltage across the high-frequency switch S_1 (v_{S1}), and the current thorough the input inductor L_{in1} (i_{Lin1}) are all shown in Fig. 9(b). The experimental results confirm theoretical analysis in sections II and III. Also, the experimental voltages across the low-frequency diode (v_{Dp}), fast diodes (v_{Do1} and v_{Do2}), and the current thorough the output inductors (i_{Lo1} and i_{Lo2}) are shown

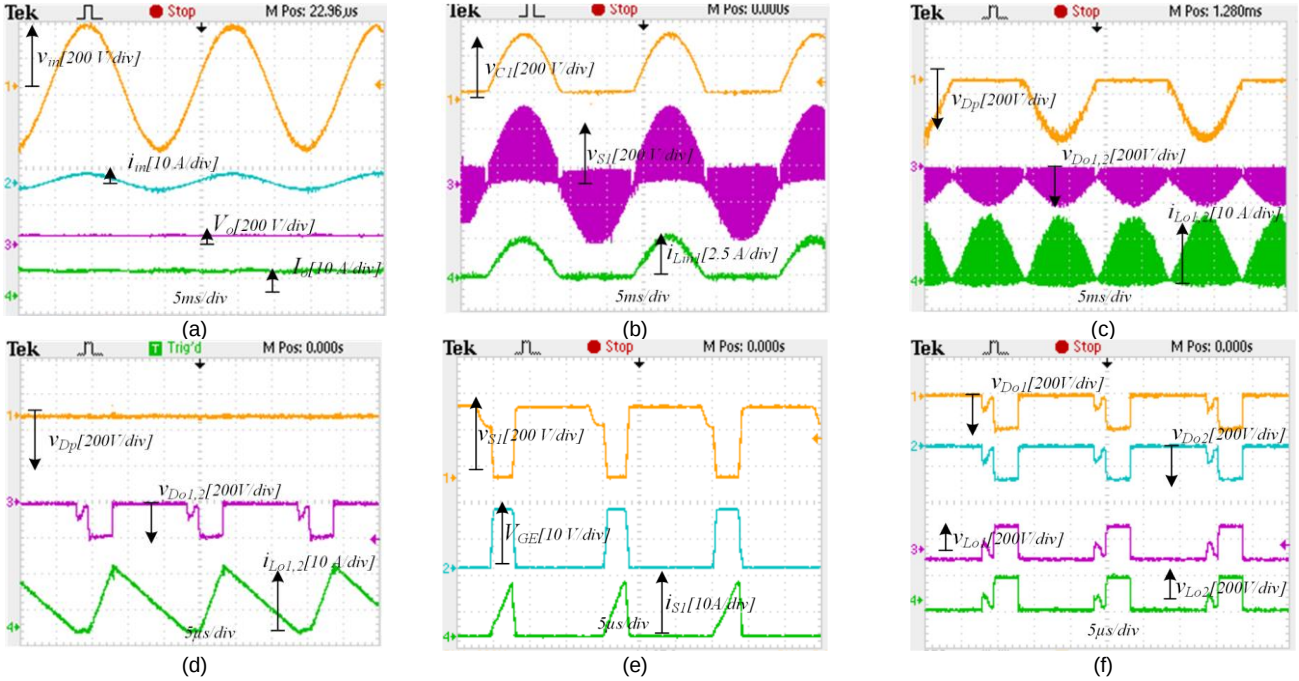

Fig. 9. Experimental results of (a) input and output waveforms, (b) voltages across S_1 and C_1 and current through L_{in1}, and (c) voltages across D_p and $D_{o1,2}$ and current through output inductor, (d) zoomed view of voltages across D_p and $D_{o1,2}$ and current through output inductor, (e) zoomed view of voltage across S_1, gate-emitter voltage and switch current, and (f) zoomed view of voltages across $D_{o1,2}$ and $L_{o1,2}$ for the proposed sepic PFC rectifier at rated power.

in Fig. 9(c). The zoomed views of voltages across the low-frequency diode (v_{Dp}), fast diodes (v_{Do1} and v_{Do2}), and the current thorough the output inductors (i_{Lo1} and i_{Lo2}) are also shown in Fig. 9(d). The zoomed view of voltage across the high-frequency switch S_1 (v_{S1}), the current thorough the high-frequency switch (i_{s1}), and the gate-emitter voltage of switch (V_{GE}) are all shown in Fig. 9(e). The zoomed view of voltage across the output diodes and output inductors are all shown in Fig. 9(f). The results confirm that no voltage spikes can be detected across the output diodes and high-frequency switches. Furthermore, the high-frequency switch turns on with a zero current. From these figures, the currents of the output inductors have three modes during a switching period and become constant when the high-frequency diode and the switch are off. The DCM operation helps shape the sinusoidal input current waveform. Moreover, the switches turn on and the output diodes turn off occur at zero current.

The harmonic contents and the power factor of the proposed sepic rectifier are measured by using a FLUKE-435 power analyzer. The harmonic amplitudes required by IEC 61000-3-2 standard and measured harmonic amplitudes for the proposed sepic PFC rectifier at 300W are compared in Table III. The results show the harmonic contents are significantly lower than the standard limits. The power factor at different output powers is shown in Fig. 10, which is almost always near unity.

Also, the calculated and measured efficiency versus various output loads is reported in Fig. 11. The measured efficiency at 300W is 93.58%. The proposed rectifier provides high efficiency under different loads.

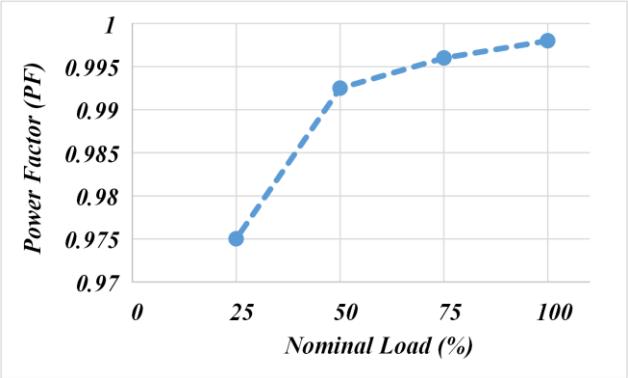

Fig. 10. Measured power factor versus the percent of nominal load.

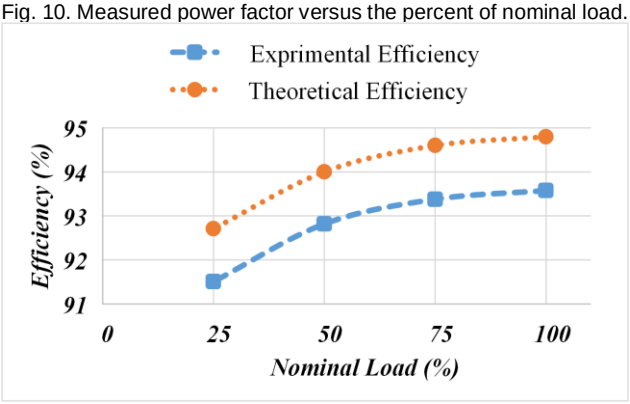

Fig. 11. Measured and calculated efficiency versus the percent of nominal load.

TABLE III
HARMONICS AMPLITUDES REQUIRED BY IEC 61000-3-2 AND MEASURED FOR THE PROPOSED SEPIC PFC RECTIFIER AT RATED POWER.

Input current harmonics	Harmonic order & amplitude in (mA)						
	3rd	5th	7th	9th	11th	13th	15th
Proposed rectifier	2.15	1.81	1.76	1.76	1.78	1.8	1.82
IEC 61000-3-2 standard limits, (class D)	1020	570	300	150	105	88.8	154

CONCLUSIONS

This paper proposed two improved high step-down PFC rectifiers based on the sepic and cuk converters. By employing a SIN, a high step-down gain is achieved. The proposed rectifiers offer a relatively high efficiency compared to the recently proposed competitors. In addition, the total ratings for all semiconductors defined by the SDP_{peak} parameter are lower than the reported rectifiers. Furthermore, the current stresses of high-frequency semiconductors are reduced. The theoretical achievements are all verified through extensive tests on a prototype with 300W power.

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