Gate Stress Polarity Dependence of AC Bias Temperature Instability in Silicon Carbide MOSFETs

Xiaohan Zhong, Huaping Jiang, Lei Tang, Xiaowei Qi, Peng Jiang, Li Ran, *Senior Member IEEE*

***Abstract*- As applications of silicon carbide (SiC) power metal oxide semiconductor filed electrical transistors (MOSFETs) grow steadily, more effort is being made to manage the risk of threshold voltage instability. It has been reported that the development of AC bias-temperature-instability (AC BTI) depends on the polarity of the gate voltage, but the underpinning mechanism is yet to become clear. Working for an explanation, the authors put forward an electric-field based polarity model which is also experimentally verified in this paper. This model shows that it is the bipolar electric field, rather than the gate voltage itself, that speeds up the threshold voltage drift. The model may be a stepping stone towards the eventual understanding and management of the dynamic threshold voltage drift.**

***Index Terms*-silicon carbide, MOSFET, threshold voltage, electric field, gate stress polarity**

I. Introduction

As wide bandgap material for the third generation power semiconductor devices, silicon carbide (SiC) has 10 times higher breakdown field and 3 times better thermal conductivity than silicon [1]. High voltage and high temperature SiC power switches are becoming a mainstream, especially those rated above 600 V. SiC MOSFETs are now a strong competitor to the Si-based IGBTs for their superior performance in terms of low switching loss and high junction temperature limit [2][3].

However, the difficulties of manufacturing and the defects in the compound semiconductor material can still lead to threshold voltage instability of SiC MOSFETs in operation [3]. According to the stress mode applied on the gate electrode, threshold voltage instability is usually classified as static or dynamic.

Static threshold voltage instability, also known as static bias-temperature-instability (BTI), refers to the threshold voltage drift under a static gate stress [4][5][9]. In order to better distinguish, this static bias-temperature-instability is referred as DC BTI. It was found that positive and negative gate voltages could cause drifts in the positive and negative directions respectively. The static drift of the threshold voltage can be treated as a low-risk issue in circuit operation which can be managed through interface passivation and/or by correctly selecting the gate voltage, etc [8][11].

Dynamic threshold voltage instability was once referred to as the threshold hysteresis [6][7][12], and regarded as harmless to circuit operation [16][17]. However, recent studies have shown that the threshold hysteresis itself is only a short-term effect of dynamic threshold instability [13]-[15]. There is also a long-term effect [16], which is referred to as AC BTI. It was found that the switching events might be the main driving force of AC BTI. It was further found that significant AC BTI occurred only with a bipolar gate voltage waveform [18]. It is implied that AC BTI should perhaps be attributed to a bipolar gate stress. However, the reason why AC BTI depends on the gate voltage polarity has not been explained and the mechanism of possible gate stress polarity dependence is still unclear.

The authors are searching for an explanation to AC BTI. In this paper, an electric-field based model is proposed and verified. It is hoped that studies on such a model could eventually lead to the understanding and management, in design or operation, of the dynamic threshold voltage drift.

TABLE I
SiC MOSFETs under Tests

Device	Gate Structure	Maximum V_{GSmax}	Gate Resistor	Initial V_{TH} @ RT
DUT.R	Trench	+22/-4 V	27 Ω	4.524 V
DUT.I	Trench	+23/-7 V	29 Ω	4.792 V
DUT.C	Planar	+25/-10 V	10 Ω	4.051 V
DUT.S	Planar	+25/-10 V	14 Ω	5.727 V

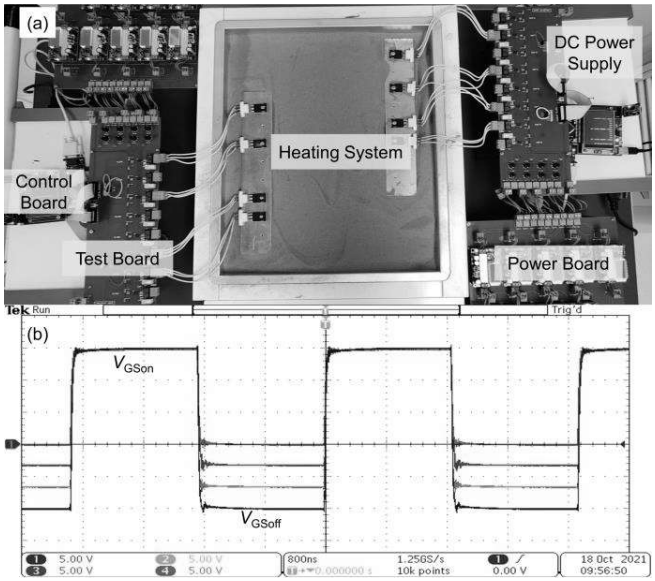

Fig. 1 (a) Experiment setup of threshold voltage drift test system, and (b) typical voltage waveform applied to gate of DUT.

Xiaohan Zhong, Huaping Jiang, Lei Tang, Xiaowei Qi, Peng Jiang, Li Ran are with the School of Electrical Engineering, Chongqing University, Chongqing, 400044, China. (Xiaohan Zhong and Huaping Jiang contributed equally to this work.) (e-mail: Stefan.Jiang@foxmail.com; L.Ran@warwick.ac.uk.)

Li Ran is also with University of Warwick, School of Engineering School of Engineering, University of Warwick, Coventry, CV4 7AL, U.K.

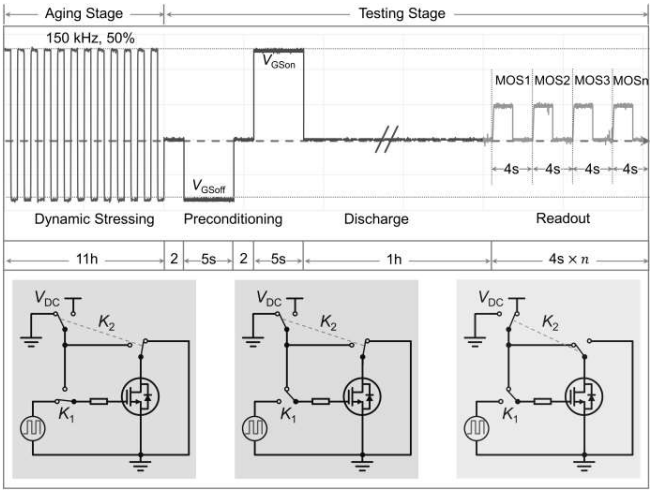

Fig. 2 Schematic illustration of dynamic threshold voltage drift test process. The threshold voltage aging and testing cycle last for 12 hours.

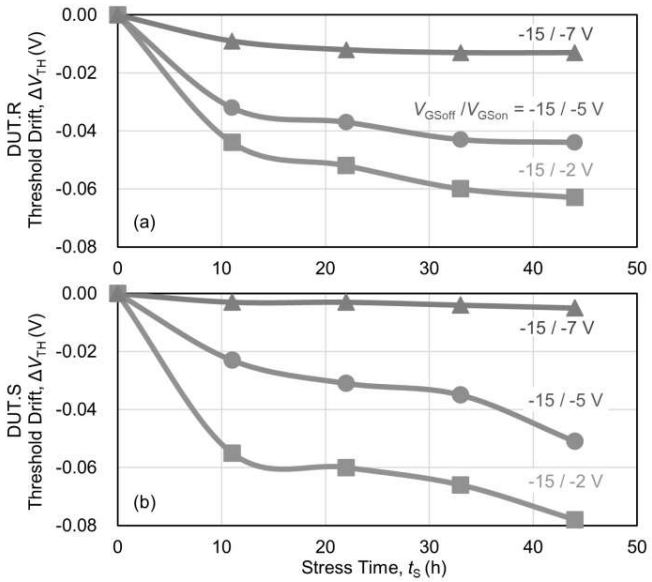

Fig. 3 Threshold voltage drifts of DUT.R and DUT.S with stressing time. The off-state gate voltage is -15 V. All the tests are carried out under room temperature with frequency of 150 kHz and duty ratio of 50%. The junction temperature is 25 °C.

II. Model Establishment and Experiment Validation

Showing the nature of AC BTI in concern, threshold voltage drift tests were conducted previously under different gate voltage profiles [18]. Four kinds of commercially available trench and planar gate SiC MOSFETs are selected as devices under test (DUTs). They are shown in Table I. To characterize the drift of threshold voltage, a test system is set up as shown in Fig. 1. The threshold voltage drift test cycle and the related topologies are shown in Fig. 2. In the aging stage, the drain was shorted to the source and a 150kHz square wave voltage of 50% duty ratio was applied between the gate and source. The testing stage includes three substages: preconditioning, discharge, and readout stage. For repeatability, preconditioning is used to align the final state of the gate voltage for all DUTs after aging. The circuit topology during two 5-s bias phases is the same as that in the aging stage. All electrodes are shorted to the ground during the 2-s zero bias phase. A 1-hour discharge stage is introduced after preconditioning to remove any residual threshold hysteresis effect by shorting all electrodes to the ground. During the threshold voltage readout, the gate and drain electrodes of the DUT are short to the power supply. The threshold voltage, V_{TH}, is defined as the gate voltage when the drain current I_D reaches 10 mA. And the threshold voltage drift, ΔV_{TH}, is the difference of each threshold voltage test value with the initial threshold voltage test value, i.e. $\Delta V_{TH}(t_S) = V_{TH}(t_S) - V_{TH}(0)$, where t_S is the accumulated aging time that the DUTs have been subject to. The bipolar gate waveform, which means that the on- and off-state gate voltages were of opposite polarities, could cause fairly fast threshold voltage drift and such drift was practically permanent. It was also shown that a unipolar (non-bipolar) gate signal had only small effect similar to that of static gate stress.

In order to explore the underpinning mechanism, it would be necessary to look into the effect on the electric field inside the device because the capturing-emission of carriers near the SiC and gate oxide interface would depend on the electric field distribution. It is hoped that further understanding of the interactions at the microscopic scale would help find an explanation.

Fig. 3 shows results of threshold voltage drift under unipolar gate voltages. The off-state gate voltage V_{GSoff} is fixed at -15 V,

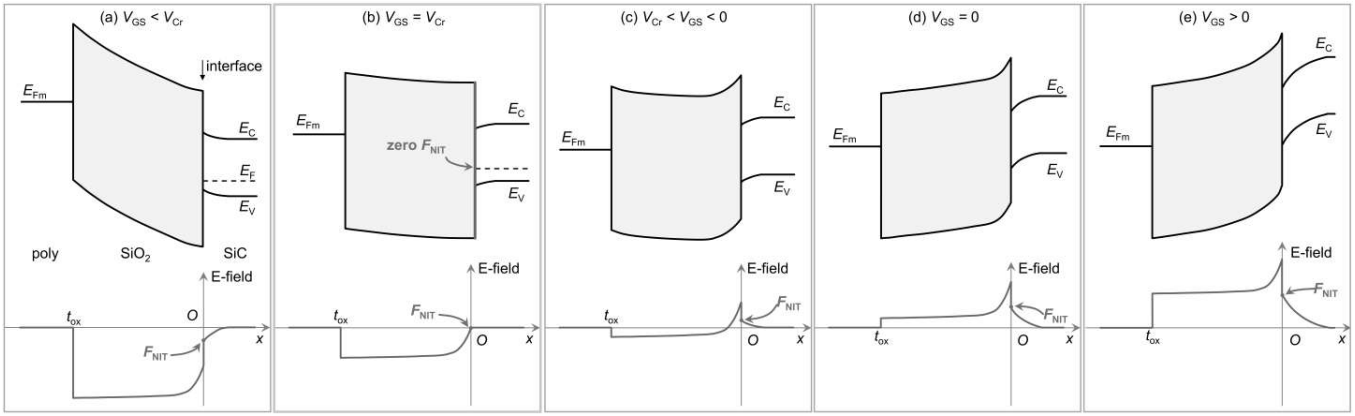

Fig. 4 Electric field across the gate interface. When the gate voltage V_{GS} is lower than the flat band voltage V_{Cr}, the electric field across the gate interface is negative. When the V_{GS} is higher than the V_{Cr}, the electric field is positive. The electric field is zero when the V_{GS} equals V_{Cr}.

but the on-state gate voltage V_{GSon} of the square wave gate voltage is set to -7 V, -5 V or -2 V. As the overall static bias of V_{GSoff}/V_{GSon} = -15/-2 V is less negative than that of -15/-7 V, threshold voltage drift of -15/-2 V should less negative than that of -15/-7 V. However, it is found that the threshold voltage drift effect is greater under gate voltage of -15/-2 V than -15/-7 V. This implies that, in addition to the DC BTI, some other mechanism takes place for -15/-2 V and it might be over-simplified to define the polarity of gate stress using the gate voltage. From the aspect of electric field, since the AC BTI is argued to attributed to near-interface oxide traps trapping and de-trapping charges, the polarity of the gate stress probably can be defined by the electric field on the SiC/SiO_2 interface.

Assuming that the electric field distribution is not uniform across the gate oxide, then the local electric field may become positive even the gate voltage is still negative, as shown in Fig. 4. In line with such a possibility, an electric-field based polarity model is proposed. The polarity of the electric field near the SiC/SiO_2 interface (F_{NIT}) is assumed to be directly related to the gate stress polarity dependence of the AC BTI because the electric-field dependence trapping and releasing (de-trapping) of carriers happen in the oxide within 3nm near the SiC/SiO_2 interface [19]. Therefore, bipolar gate stress refers to the gate stress when the resultant F_{NIT} reverses within one switching cycle (i.e. bipolar F_{NIT}), while unipolar gate stress refers to the gate stress when the resultant F_{NIT} does not reverse within one switching cycle (unipolar F_{NIT}). There is a specific gate voltage at which the electric field near the SiC/SiO_2 interface is zero (F_{NIT} = 0 V/m). This specific gate voltage is referred as the critical gate voltage (V_{Cr}), which is determined by the work-function difference and the interface or near interface charge. As long as the off-state gate voltage is lower than V_{Cr} and the on-state gate voltage is higher than V_{Cr} ($V_{GSoff} < V_{Cr} < V_{GSon}$), the electrical field F_{NIF} reverses within one switching cycle (bipolar F_{NIF}). Such gate stress is bipolar gate stress. Thus, AC BTI happens, resulting in significant threshold voltage drift. The critical gate voltage V_{Cr} can be expressed as

$$V_{Cr} = \phi_{ms} - \frac{Q_{ox}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} \quad (1)$$

where ϕ_{ms} is the work-function difference, Q_{ox} is the charges lie within the gate oxide, C_{ox} is the capacitance of gate oxide, Q_{it} is the interface trapped charges. Since the density and polarity of the interface trapped charge depend on the electric field cross the SiC/SiO_2 interface, this critical gate voltage may vary with the interface electric field. Furthermore, since V_{Cr} is not equal to zero, it can be predicted that there is a non-zero turning point of the threshold voltage drift curve with different gate voltages. This turning point is not only the dividing point between unipolar and bipolar gate stress, but also the dividing point

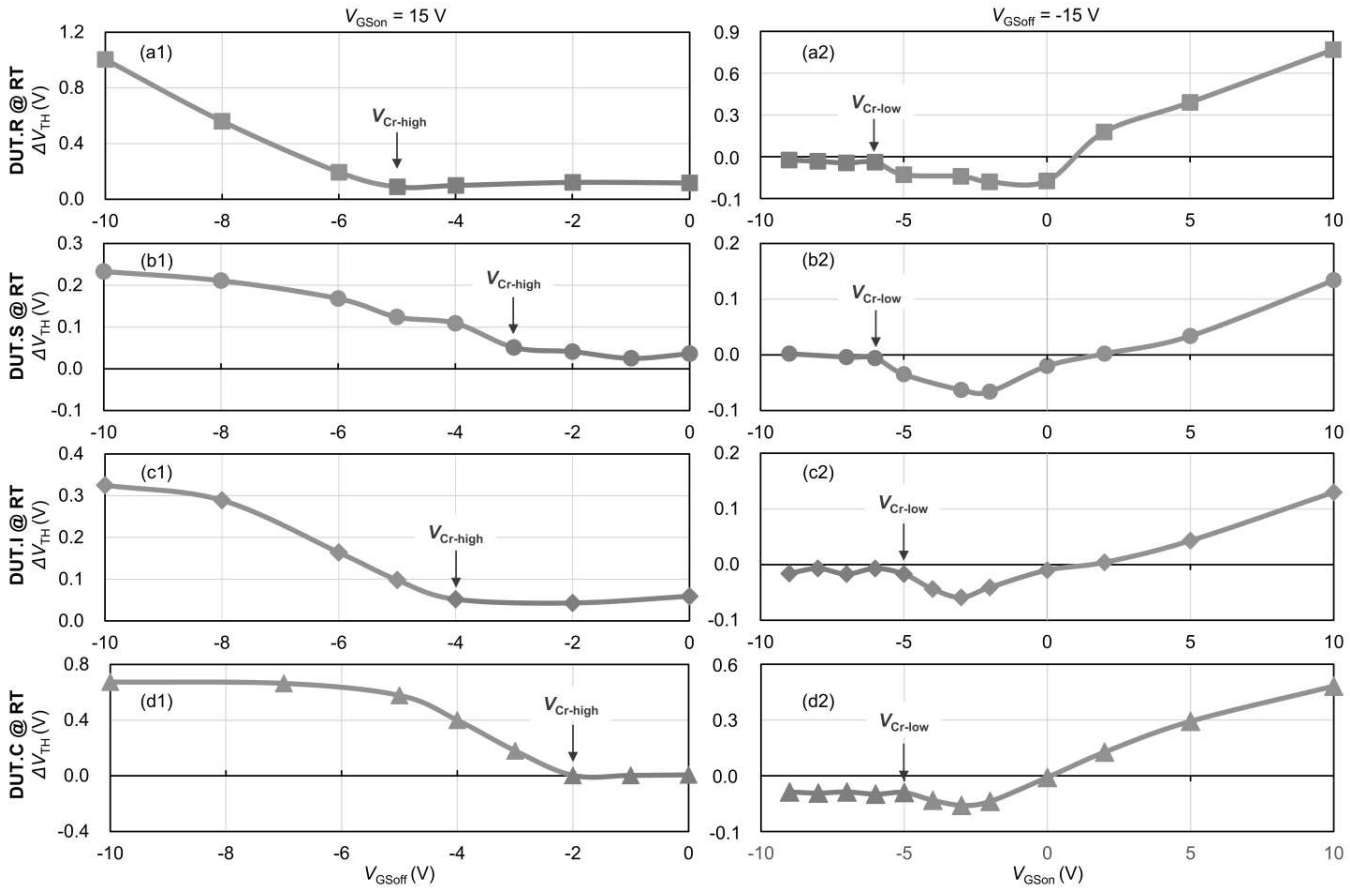

Fig. 5 Threshold voltage drifts under different on- and off-state gate voltages. (a1) (b1) (c1) (d1) Threshold voltage drifts versus V_{GSoff} with a fixed V_{GSon} of 15 V; (a2) (b2) (c2) (d2) threshold voltage drifts versus V_{GSon} with a fixed V_{GSoff} of -15 V. The frequency and duty cycle of the dynamic gate stress are 150 kHz and 50% respectively. The junction temperature is 25 °C. The stress time lasts for 66 hours. The gray color refers to the negative drifted DC BTI. The blue color refers to the negative drifted AC BTI while the pink color refers to the positive drifted AC BTI.

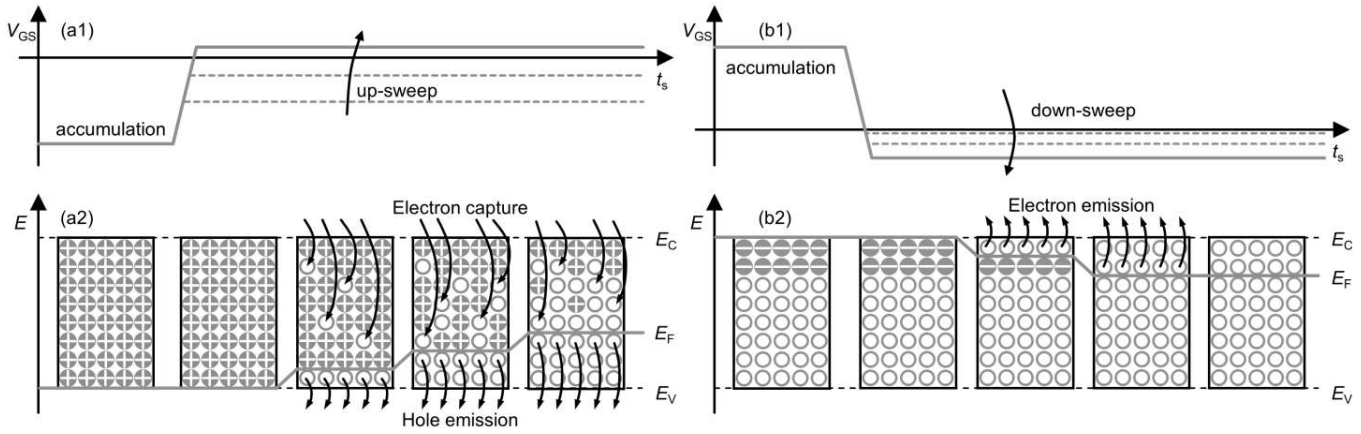

Fig. 6 Schematic illustration of restoration of thermal equilibrium after positive and negative gate bias. The turn-on and turn-off switching process are illustrated in (a1) and (b1), corresponding band diagram and gradual charging of interface states in (a2) and (b2). Neutral interface states are illustrated as open circles.

between DC BTI and AC BTI. The gate voltage corresponding to this turning point can be approximately regarded as equal to the V_{Cr}.

The curves of threshold voltage drift versus on- and off-state gate voltage are shown in Fig. 5. Indeed, as expected above, a turning point is observed in the threshold voltage drift curve. Whether it is changing V_{GSoff} with fixed V_{GSon} or changing V_{GSon} with fixed V_{GSoff}, once the gate voltage crosses a certain voltage, a significant threshold voltage drift can be observed. In other words, AC BTI happens when the gate voltage crosses this specific gate voltage. It can be inferred that the electric field F_{NIT} under this specific gate voltage is approximately zero. According to the electric model proposed above, this specific gate voltage corresponding to the turning point can be regarded as approximately equal to V_{Cr}. Therefore, the performance results of DUT.R and DUT.S shown in Fig. 3 can be explained. For a fixed V_{GSoff} of -15 V, the gate stress bipolarity increases with the increase of V_{GSon}. When V_{GSon} = -7 V which is lower than V_{Cr} of -6 V, the near interface oxide electric field F_{NIT} is unipolar and the threshold drift is dominated by DC BTI and thus relatively small. Once V_{GSon} goes higher than V_{Cr}, the polarity of F_{NIT} becomes bipolar and AC BTI effect starts to take place. The gate stress is bipolar under gate voltage of -15/-2 V. And consequently, it is no longer unusual for the threshold voltage of DUT.R or DUT.S under -15/-2 V gate stress to drift significantly and more than that under -15/-7V. Furthermore, it is also found that the V_{Cr} is different for different devices, which is caused by the difference in the manufacturing process and the crystal plane of the channel.

Furthermore, it is worth noting that the V_{Cr} in the V_{GSoff}-ΔV_{TH} curve and V_{GSon}-ΔV_{TH} curve are different. Take DUT.R and DUT.C as an example, increasing V_{GSon} from -9 V to 10 V with a fixed low V_{GSoff} of -15 V, the critical voltage is -6 V for DUT.R and -5 V for DUT.C, decreasing V_{GSoff} from 0 V to -10 V with a fixed high V_{GSon} of 15 V, the critical voltage is -5 V for DUT.R and -2 V for DUT.C. The critical gate voltage measured with a fixed low V_{GSoff} of -15 V is referred as $V_{Cr\text{-}low}$, and the critical gate voltage measured with a fixed low V_{GSon} of 15 V is referred as $V_{Cr\text{-}high}$. For the four devices, $V_{Cr\text{-}low}$ is lower than $V_{Cr\text{-}high}$, and the underpinning mechanism of this difference can be explained by interface trapped charge Q_{it}.

In formula (1), the critical gate voltage V_{Cr} is associated with interface trapped charge Q_{it}, the difference between $V_{Cr\text{-}low}$ and $V_{Cr\text{-}high}$ may result from different density of interface trapped charges. As shown in Fig. 6, during the negative bias, the negative electrical field urges holes to be trapped by the

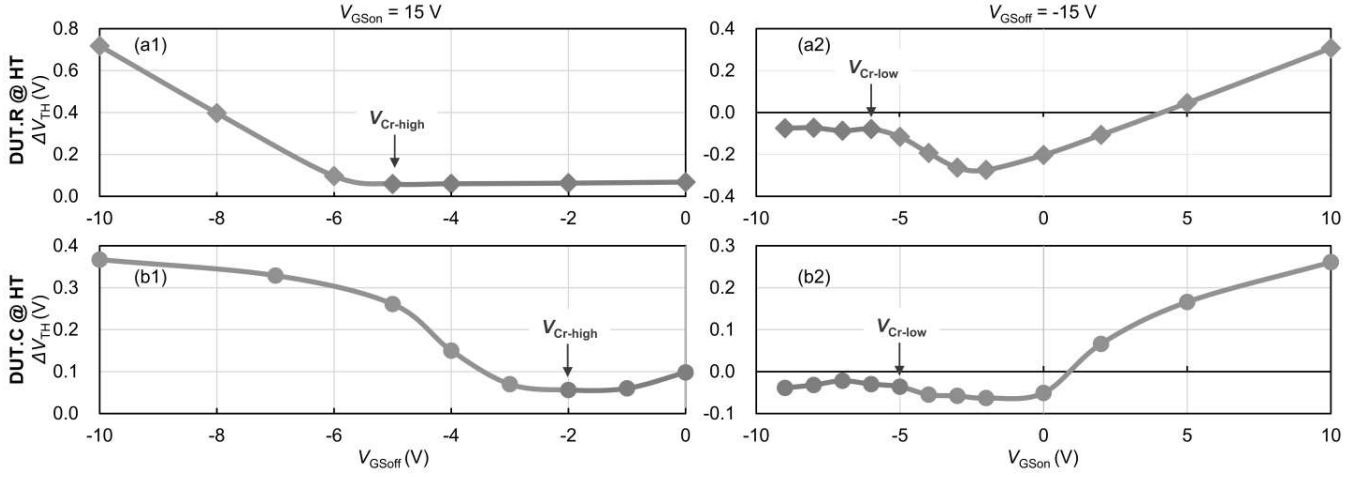

Fig. 7 Threshold voltage drifts under different on- and off-state gate voltages. (a1) (b1) Threshold voltage drifts of DUT.R and DUT.C versus V_{GSoff} with a fixed V_{GSon} of 15 V; (a2) (b2) threshold voltage drifts of DUT.R and DUT.C versus V_{GSon} with a fixed V_{GSoff} of -15 V. The frequency and duty cycle of the dynamic gate stress are 150 kHz and 50% respectively. The junction temperature is 175 °C.

interface trap, the Fermi level is pinned to the valance band. A large number of positive charges accumulate on the SiC/SiO_2 interface [6], which leads to a positive Q_{it} and a decrease in the critical gate voltage ($V_{Cr\text{-}low}$). Therefore, during increasing V_{GSon} with fixed V_{GSoff}, V_{GSon} only needs to be higher than this lower critical gate voltage, F_{NIF} reverses, and AC BTI starts to take place. During the positive bias, the positive electrical field urges the electrons to be trapped by the interface trap, the Fermi level is pinned to the conduction band edge. A small number of the negative charges are accumulated on the SiC/SiO_2 interface [6], which causes a negative Q_{it} and a higher critical gate voltage ($V_{Cr\text{-}high}$). Therefore, during decreasing V_{GSoff} with fixed V_{GSon}, V_{GSoff} only needs to be lower than this higher critical gate voltage, F_{IF} reverses, and AC BTI starts to take place. Therefore, $V_{Cr\text{-}low}$ is lower than $V_{Cr\text{-}high}$ ($V_{Cr\text{-}low} < V_{Cr\text{-}high}$).

Furthermore, experiments of dynamic threshold voltage drift under different gate voltages were carried out at high junction temperature. As shown in Fig. 7, $V_{Cr\text{-}low}$ and $V_{Cr\text{-}high}$ are approximately equal to those at room temperature, and $V_{Cr\text{-}low}$ is still lower than $V_{Cr\text{-}high}$.

Since the V_{Cr} is not equal to 0, it is then reasonable to expect that the threshold voltage drift depends on the modified, effective gate biases defined as

$$\begin{cases} V^*_{GSon} = V_{GSon} - V_{Cr} \\ V^*_{GSoff} = V_{GSoff} - V_{Cr} \end{cases}. \quad (3)$$

The threshold voltage drift direction is a result of the balance between the effective negative and positive biases and could be positive as well as negative. For DUT.R With V_{Cr} of -5 V, the threshold voltage drifts under effective positive and negative gate voltage V^*_{GSon} / V^*_{GSoff} of 10/-3 V and 3/-10 V are shown in Fig. 8. Fig.8 also presents the threshold voltage drifts of DUT.S stressed under effective positive and negative gate voltage V^*_{GSon} / V^*_{GSoff} of 12/-1 V and 1/-12 V. For DUT.R, the absolute drift value under effective gate stress of 10/-3 V is higher than that under effective gate stress of -3/-10 V. For DUT.S, the absolute drift value under effective gate stress of 12/-1 V is higher than that under effective gate stress of 1/-12 V. It is indicated that the positive drift is faster compared to the negative drift. In other words, positive drift is easier than negative drift. It might attribute to the different density and energy distribution of accepter-type and donor-type interface traps.

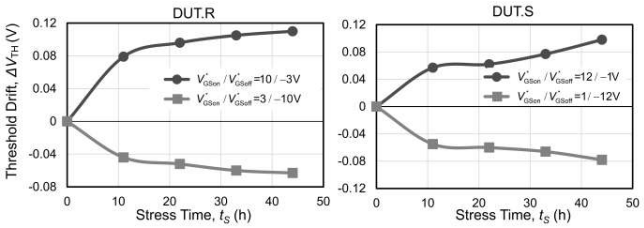

Fig. 8 (a) Threshold voltage drift of DUT.R under effective gate stress of 10/-3 V and 3/-10 V. (b) Threshold voltage drift of DUT.S under effective gate stress of 12/-1 V and 1/-12 V.

III. Conclusions

An electric-field based polarity model was proposed in this paper to explain the dependence of the AC BTI on the gate stress polarity, and the related threshold voltage drift experiments were carried out to verify the credibility of this model. It is found that the AC BTI is introduced by the bipolar electric field across the gate interface instead of the bipolar gate stress. Furthermore, the bipolar electric field is formed as long as the critical gate voltage within the gate voltage interval of (V_{GSoff}, V_{GSon}). Furthermore, the critical gate voltages corresponding to up-sweep V_{GSon} and down-sweep V_{GSoff} are not the same, which is related to the short-term effect of interface traps trapping or de-trapping charges. In general, the electric-field based polarity model and the features of AC BTI reported in this paper may help better understand the mechanism of the dynamic threshold voltage drift.

References

[1] T. Kimoto and J. A. Cooper, *Fundamentals of Silicon Carbide Technology: Growth, Characterization, Devices, and Applications*. Singapore: Wiley, Nov. 2014.

[2] Q. Zhang, G. Wang, H. Doan, S.-H. Ryu, B. Hull, J. Young, S. Allen and J. Palmour, "Latest results on 1200 V 4H-SiC CIMOSFETs with $R_{sp,on}$ of 3.9 mΩ·cm^2 at 150 ℃," in *Proc. 27th Int. Symp. on Power Semiconductor Devices ICs (ISPSD)*, Hong Kong, China, May. 2015, pp. 89-92, doi: 10.1109/ISPSD.2015.7123396.

[3] B. J. Baliga, *Silicon Carbide Power Devices*. Singapore: World Scientific, Jan. 2006.

[4] C. Schleich, J. Berens, G. Rzepa, G. Pobegen, G. Rescher, S. Tyaginov, T. Grasser, M. Waltl, "Physical Modeling of Bias Temperature Instabilities in SiC MOSFETs," in *2019 IEEE International Electron Devices Meeting (IEDM)*, 2019, pp. 20.5.1-20.5.4, doi: 10.1109/IEDM19573.2019.8993446.

[5] M. Waltl, "Defect Spectroscopy in SiC Devices," 2020 IEEE International Reliability Physics Symposium (IRPS), 2020, pp. 1-9, doi: 10.1109/IRPS45951.2020.9129539.

[6] T. Aichinger, G. Rescher and G. Pobegen, "Threshold voltage peculiarities and bias temperature instabilities of SiC MOSFETs," *Microelectronics Reliability*, vol. 80, pp. 68-78, Jan. 2018, doi: 10.1016/j.microrel.2017.11.020.

[7] B. Asllani, A. Castellazzi, O. A. Salvado, A. Fayyaz, H. Morel and D. Planson, "V_{TH}-hysteresis and interface states characterisation in SiC power MOSFETs with planar and trench gate," in *2019 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, Mar. 2019, pp, doi: 10.1109/IRPS.2019.8720612.

[8] W. Zhou, X. Zhong and K. Sheng, "High temperature stability and the performance degradation of SiC MOSFETs," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2329-2337, May. 2014, doi: 10.1109/TPEL.2013.2283509.

[9] D. B. Habersat, R. Green and A. J. Lelis, "Permanent and transient effects of high-temperature bias stress on room-temperature V_T drift measurements in SiC power MOSFETs," in *2019 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, Mar. 2019, pp. 1-4, doi: 10.1109/IRPS.2019.8720538.

[10] M. Domeij, J. Franchi, B. Buono, K. Lee, K-S. Park, C-S. Choi, S. Sunkari and H. Das, "Avalanche rugged 1200V 80mΩ SiC MOSFETs with state-of-the-art threshold voltage stability," in *2018 IEEE 6th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Atlanta, GA, USA, Oct. 2018, pp. 114-117, doi: 10.1109/WiPDA.2018.8569186.

[11] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin and H. Reisinger, "Review on SiC MOSFETs high-voltage device reliability focusing on threshold voltage instability," *IEEE Transactions on Electron Devices*, vol. 66, no. 11, pp. 4604-4616, Nov. 2019, doi: 10.1109/TED.2019.2938262.

[12] K. Puschkarsky, H. Reisinger, T. Aichinger, W. Gustin and T. Grasser, "Threshold voltage hysteresis in SiC MOSFETs and its impact on circuit operation," in *2017 IEEE International Integrated Reliability Workshop (IIRW)*, Fallen Leaf Lake, CA, USA, Oct. 2017, pp. 1-5, doi: 10.1109/IIRW.2017.8361232.

[13] K. A. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin, and H. Reisinger, "Understanding and Modeling Transient Threshold Voltage Instabilities in

SiC MOSFETs," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, pp. 1-10, 2018, doi: 10.1109/IRPS.2018.8353560

[14] A. J. Lelis, R. Green and D. B. Habersat, "SiC MOSFET threshold-stability issues," *Materials Science in Semiconductor Processing*, vol. 78, pp. 32-37, May. 2018, doi: 10.1016/j.mssp.2017.11.028.

[15] Infineon, "Guidelines for CoolSiC MOSFET gate drive voltage window", 2018.

[16] D. B. Habersat, R. Green and A. J. Lelis, "Evaluations of Threshold Voltage Stability on COTS SiC DMOSFETs Using Fast Measurements," in *2016 IEEE International Reliability Physics Symposium*, Pasadena, CA, USA, Apr. 2016, pp. CD-4, doi: 10.1109/IRPS.2016.7574588.

[17] K. Puschkarsky, T. Grasser, T. Aichinger, W. Gustin and H. Reisinger, "Understanding and modeling transient threshold voltage instabilities in SiC MOSFETs," in *2018 IEEE International Reliability Physics Symposium (IRPS)*, Burlingame, CA, USA, Mar. 2018, pp. 3B-5, doi: 10.1109/IRPS.2018.8353560.

[18] H. Jiang, X. Zhong, G. Qiu, L. Tang, X. Qi, and L. Ran, "Dynamic Gate Stress Induced Threshold Voltage Drift of Silicon Carbide MOSFET," *IEEE Electron Device Letters*, vol. 41, no. 9, pp. 1284-1287, Sept. 2020, doi: 10.1109/LED.2020.3007626.

[19] C. Yang, S. Wei and D. Wang, "Bias temperature instability in SiC metal oxide semiconductor devices" *Journal of Physics D: Applied Physics*, vol. 54, no. 12, 2021,