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Thermal characterization of direct wafer bonded Si-on-SiC

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ABSTRACT

Direct bonded Si-on-SiC is an interesting alternative to silicon-on-insulator (SOI) for improved thermal management in power conversion and radio frequency applications in space. We have used transient thermoreflectance and finite element simulations to characterize the thermal properties of direct bonded Si-on-4H–SiC samples, utilizing a hydrophobic and hydrophilic bonding process. In both instances, the interface has good thermal properties resulting in TBR_{eff} values of $6+4/-2\,m^2\,K\,GW^{-1}$ (hydrophobic) and $9+3/-2\,m^2\,K\,GW^{-1}$ (hydrophilic). Two-dimensional finite element simulations for an equivalent MOSFET showed the significant thermal benefit of using Si-on-SiC over SOI. In these simulations, a MOSFET with a 200 nm thick, 42 μm wide Si drift region was recreated on a SOI structure (2 μm buried oxide) and on the Si-on-SiC material characterized here. At $5\,W\,mm^{-1}$ power dissipation, the Si-on-SiC was shown to result in a >60% decrease in temperature rise compared to the SOI structure.

Si-on-SiC devices are being developed as an alternative to conventional silicon on insulator (SOI) devices for harsh environment applications, such as space. These devices aim to utilize SiC's high thermal conductivity to improve thermal management.[1–3] This material has been proposed for a number of applications, including radio frequency[3–5] and power conversion.[1,6] The semi-insulating SiC provides electrical isolation for the Si device layer with the benefits of removing the low thermal conductivity buried oxide (BOX) and integrating a SiC heat sink; this should provide significant benefits for passive cooling. The following is focused on power converter applications where Si-on-SiC could be useful in propulsion in deep space missions. In this application, increased passive cooling would aid the missions' science capabilities, reducing the number of active cooling components. Devices would need to support >600 V, and an example of a real SOI device architecture able to support such voltages and a proposed Si-on-SiC structure is shown in Fig. 1.[6,7] These schematics do not include all doping regions of the device, which were not considered during thermal simulations; a more complete structure is shown in Ref. 7. The field oxide and BOX were 2 μm, the Si drift region was 200 nm thick and 42 μm wide, and the Si regions under the contacts were 1 μm thick. For direct thermal comparison, the Si and SiC substrates were both assumed to be 300 μm thick.

In the past 15 years, direct wafer bonding of Si with SiC has been an area of steady interest.[2–5] Recently, there has been increased research into wafer bonding of semiconductors with heat sinks in general.[8,9] These bonds often utilize an amorphous or polycrystalline adhesion layer. Such materials have a low thermal conductivity compared to the bonded materials. If the interfacial layers are thick enough, they will introduce a significant thermal resistance, R, as $R = \frac{t}{\kappa}$, where κ is the thermal conductivity of the layer and t is its thickness. All thermal resistances are lumped into TBR_{eff}, which includes contributions from the interfacial layer thermal conductivity and intrinsic interfacial TBR arising from phonon mismatch or electron–phonon coupling. The TBR_{eff} parameter has been shown to be particularly important for the effective heterogeneous integration of high power density electronics on heat spreaders for thermal management, such as GaN HEMTs on SiC or diamond substrates.[10–12] However, this parameter has been neglected when characterizing and simulating Si-on-SiC.

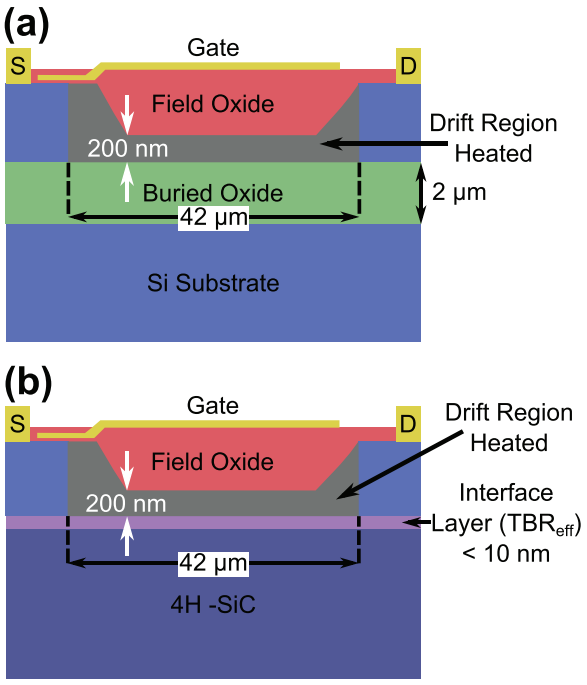

FIG. 1. (a) Device schematic of a SOI device, which can support >600 V with a 42 μm wide drift region and a 2 μm thick buried oxide layer; (b) the same device on a direct bonded 4H–SiC substrate. Heat was generated in the drift region during simulations.

In previous work, Shinohara *et al.* bonded a 6H–SiC wafer with a Si wafer in a wafer bonder at 1000 °C.[2] The bonding was partially successful, but little characterization was carried out. The thermal benefit of the SiC was investigated by measuring the electron mobility of devices on the unbonded Si and on the Si-on-SiC before and after an anneal at 300 °C in air. For material with poorer thermal management, higher surface temperatures would be experienced during the anneal resulting in degraded electronic properties. As expected, the bonded material exhibited significantly lower degradation. However, without further investigation of the interface, it would be difficult to quantify the exact benefit of the SiC.

Lotfi *et al.* bonded a poly-SiC wafer to a SOI wafer using an 800 nm, amorphous Si interlayer.[4] The amorphous Si was deposited on the SiC before both it and the SOI wafer underwent an IMEC clean.[15] Hydrophilicity of both wafers was enhanced using piranha solution before being bonded in a wafer bonder at >1000 °C for one hour. Transmission electron microscopy (TEM) showed that the amorphous Si had recrystallized into polycrystalline Si. After removal of the Si backside and BOX from the bonded SOI wafer, transistors were fabricated on the Si layer. Thermal performance was measured using the temperature rise of a calibrated resistor vs applied power density. The Si/SiC material showed a reduction in temperature of 26% compared to the SOI material, a promising result. However, it is likely that the thick layer of poly-Si introduced a significant thermal resistance. Its thermal conductivity is likely to be $< 20\ \mathrm{W\,m^{-1}\,K^{-1}}$ equating to a thermal resistance of $>40\ \mathrm{m^2\,K\,GW^{-1}}$, reducing the effectiveness of the SiC as a heatsink.[14] An examination of the types of

TABLE I. The expected thermal conductivity, thickness, and associated thermal resistance of a variety of interfacial materials used for SOI and Si-on-SiC.

Interfacial material	Expected thermal conductivity/ $\mathrm{W\,m^{-1}\,K^{-1}}$	Thickness/nm	Total thermal resistance/ $\mathrm{m^2\,K\,GW^{-1}}$
Polycrystalline SiO_2	<4[13]	2000[6]	>500
Polycrystalline Si	<20[14]	800[3]	>40
Amorphous SiO_2	~1[13]	2.5[1]	~2.5

interfacial materials frequently used with their thickness, and thermal resistance is shown in Table I. While this is a simplification, neglecting the thermal latency of layers thicker than a few 100 nm, it provides a useful comparison of the scale of thermal resistance introduced by different materials, which have been employed for Si-on-SiC and SOI.

In this work, transient thermoreflectance (TTR) has been used to characterize the TBR_{eff} between the Si and SiC substrate for a hydrophilic and a hydrophobic bonding process. Finite element analysis (FEA) has been used to quantify the effect of TBR_{eff} and substrate thermal conductivity on the thermal performance of devices on this material and to benchmark their performance against equivalent SOI devices.

Si-on-SiC wafers were produced by direct bonding of an SOI wafer to a 300 μm thick, 100 mm Ø, semi-insulating, on-axis, 4H–SiC wafer. These SiC wafers had undergone an optical polish on the C-face

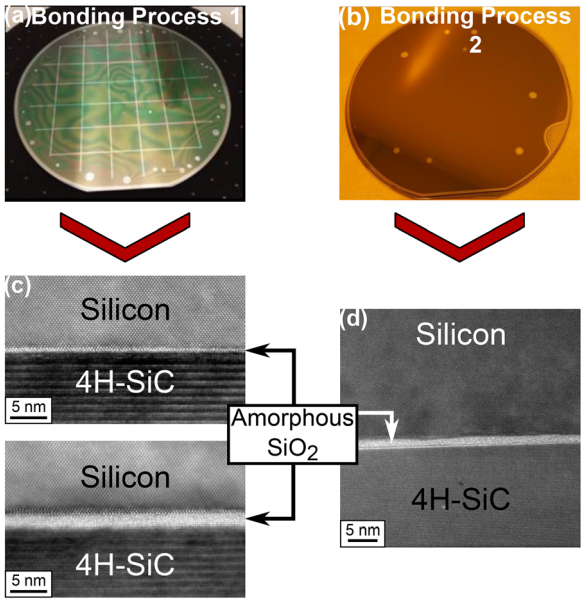

FIG. 2. (a) and (b) are optical images of the wafers following hydrophobic bonding and hydrophilic bonding, respectively. Reproduced with permission from Gammon *et al.*, Mater. Sci. Semicond. Process. **78**, 69 (2018). Copyright 2018 Authors, licensed under a Creative Commons Attribution (CC BY) license, Ref. 1 High resolution transmission electron micrographs of the interfaces of hydrophobic bonding (c) (reproduced with permission from Chan *et al.*, IEEE Trans. Electron Devices **64**, 3713 (2017). Copyright 2017 Authors, licensed under a Creative Commons Attribution (CC BY) license, Ref. 16) and hydrophilic bonding (d) are also presented.

TABLE II. Details of fixed parameters used for fitting of the thermoreflectance data. Parameters were assumed to be temperature independent due to <10 K temperature rise induced during the TTR measurement.

Material	Cross-plane thermal conductivity/W m^{-1} K^{-1}	In-plane thermal conductivity/W m^{-1} K^{-1}	Heat capacity/J kg^{-1} K^{-1}	Density/kg m^{-3}	Thickness/nm
Au	200[17,18]	Isotropic	128[19]	19320[19]	150
Si	140[20]	Isotropic	700[21]	2329[21]	1200
[a]4H–SiC	Fitted	$\sim\frac{6}{5}\kappa_{\perp}$[22]	690[21]	3211[21]	300 000

[a]On-axis semi-insulating.

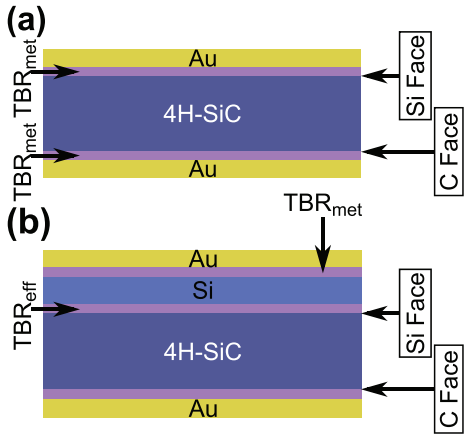

FIG. 3. Schematics of the material measured using TTR. (a) a debonded piece of ~300 μm thick 4H–SiC; (b) a ~1 μm thick Si layer bonded to the Si face of an ~300 μm thick piece of 4H–SiC. In both cases, the Si and C faces were coated with 150 nm Au.

and CMP on the Si-face. Bonding was performed using a hydrophobic bonding process and a hydrophilic bonding process.[1] For the hydrophobic process, a grid of 2 μm deep trenches was etched into the SiC to give a route for outgassing during the annealing process. The surface of the Si-face of the SiC and the device side of a SOI wafer were cleaned using a proprietary plasma process. They were then bonded using a hydrophobic bonding process with a 1200 °C 2-h anneal. This anneal formed a permanent bond and shrunk the interfacial oxide, which formed during the bonding process. The SOI wafer was then ground down to the BOX layer, which was removed using HF.

For the hydrophilic process, both wafers were cleaned by RCA cleaning and using an EVG wafer cleaner equipped with a de-ionized megasonic nozzle. They were then exposed to nitrogen free radicals in a wafer bonder, improving hydrophilicity, before contact was made. Bond strength was enhanced by annealing at 300 °C for 24 h under N_2 atmosphere. As in the hydrophobic process, the Si device layer was exposed by a combination of grinding and wet etching. The resulting wafers and TEM cross sections are shown in Fig. 2. The TEM images of the hydrophobic bond show a non-uniformly thick amorphous layer at the Si/SiC interface, which varied from < 0.2 to 2.5 nm thick across the wafer [Fig. 2(c)]. For the hydrophilic bond, a similar layer is seen with uniform thickness [~ 2.5 nm, Fig. 2(d)].

Thermal characterization was performed using transient thermoreflectance, and the full details of which are given in Ref. 23 A 150 nm Au transducer with a 10 nm Cr adhesion layer was deposited by thermal evaporation onto the surface of interest. A 532 nm continuous wave laser ($1/e^2$ spot size ~1 μm) monitored the surface reflectivity while a diode pumped passively Q-switched 355 nm pulsed laser (pulse length 1 ns, $1/e^2$ spot size $89+30/-28$ μm, error estimated as the 10th and 90th percentiles of the spot fitted on a standard Si sample) was used to periodically heat the surface. The resulting change in the reflectivity of the surface is linearly proportional to its temperature, and it is possible to extract unknown thermal properties of a stack using an adapted least squares fitting procedure.[24]

Error in the fitted parameters was estimated using a Monte Carlo (MC) error analysis as detailed in Ref. 25, repeating the fitting 2000 times with slight variation of the fixed material properties and laser parameters. Error in fixed parameters was assumed to be normally distributed. In general, a 2% standard deviation was used to generate these distributions. The exceptions were the Si thickness and Au thickness, where a 5% standard deviation was used, and the Si thermal conductivity where a skewed distribution was used to prevent unphysical values above 149 W m^{-1} K^{-1}. For experimental data points, the standard deviation was estimated from variation in multiple traces collected in each location and propagated when averaging traces measured in different locations. The full details of the fixed parameters are given in Table II. It is important to note that with this experimental

TABLE III. Extracted thermal properties from all samples studied using transient thermoreflectance. Error bars are the 10th and 90th percentile estimated from MC analysis. All parameters are assumed to be temperature independent as temperature rise is kept to less than 10 K.

Sample	TBR$_{met}$, C face/m^2 K GW^{-1}	$\kappa_{\perp,\text{C-face}}$/ W m^{-1} K^{-1}	TBR$_{met}$ Si face/ m^2 K GW^{-1}	$\kappa_{\perp,\text{Si-face}}$/ W m^{-1} K^{-1}	TBR$_{eff}$/ m^2 K GW^{-1}
Hydrophobic bond	11 ± 1	489 ± 65	N/A	323 ± 26	$6+4/-2$
Hydrophilic bond	7.1 ± 0.8	384 ± 50	N/A	259 ± 51	$9+3/-2$
Purposefully delaminated SiC	6.4 ± 0.6	$367+47/-46$	4.5 ± 0.6	$211+39/-36$	N/A

setup, there is most sensitivity for the cross-plane thermal conductivity and little sensitivity to the in-plane thermal conductivity. For this reason, the in-plane (a-direction) thermal conductivity of the SiC was assumed at 6/5 the cross-plane (c-direction) thermal conductivity, based on values reported for semi-insulating 4H–SiC produced by Wolfspeed ($\kappa_{\perp} \sim 390\ \mathrm{W\,m^{-1}\,K^{-1}}$, $\kappa_{||} \sim 490\ \mathrm{W\,m^{-1}\,K^{-1}}$).[22] Other materials were assumed to be isotropic.

Transient thermoreflectance measurements were performed on a SiC sample on both its Si face and C backside, demonstrated in the schematic in Fig. 3(a). This sample had been used for initial bonding trials where a weaker bond was formed making it possible to purposefully delaminate the Si for these measurements. For bonded samples, measurements were taken from the SiC backside (C face) and from the Si device layer [Fig. 3(b)]. A minimum of five measurements were

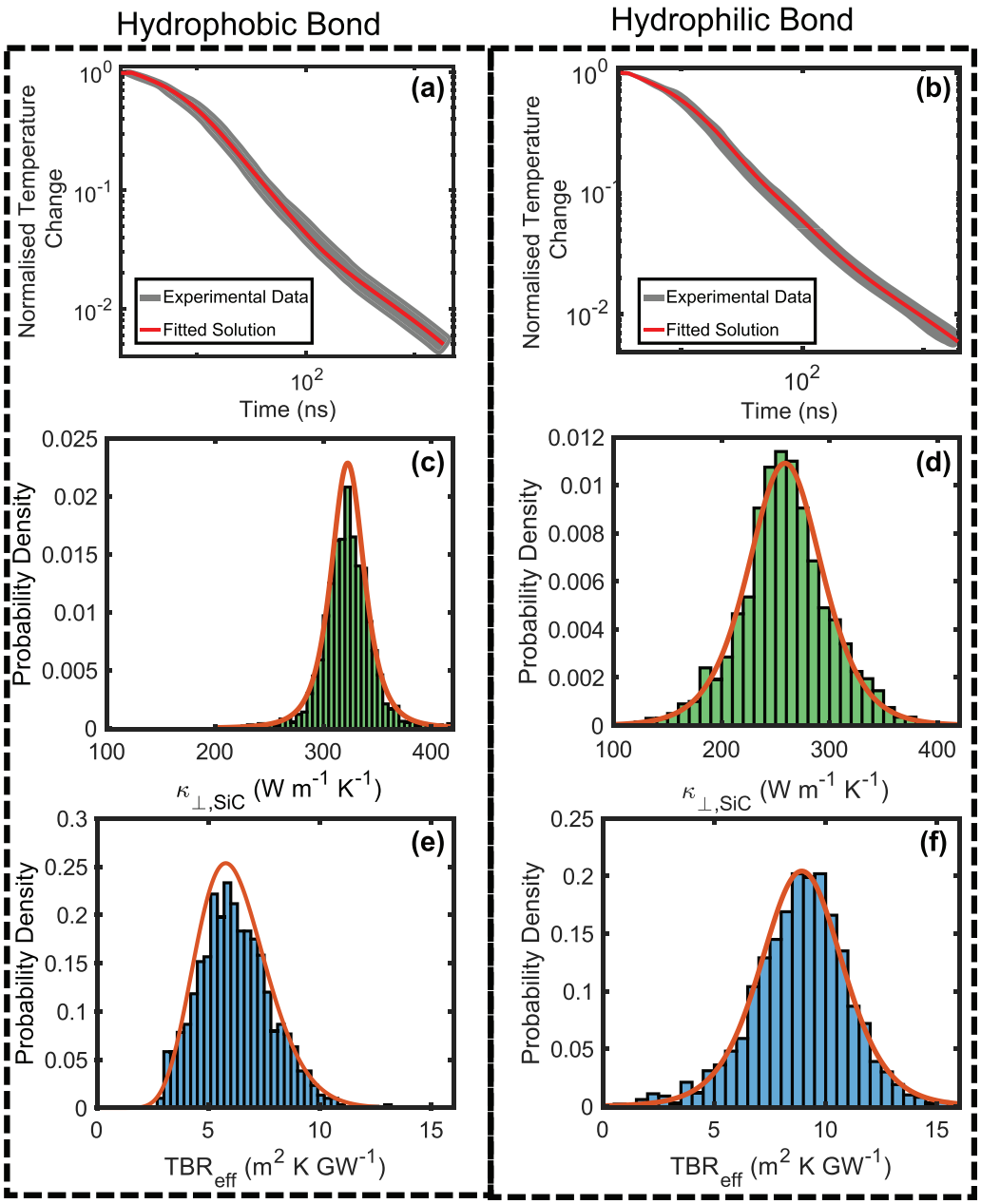

FIG. 4. (a) and (b) show examples of fitted thermoreflectance traces for hydrophobic and hydrophilic bonds taken from the Si device layer, gray band indicates experimental data ± one standard deviation; (c) and (d) show probability distributions of extracted SiC thermal conductivity for the same measurement ($\kappa_{\perp,SiC} = 323 \pm 26\ \mathrm{W\,m^{-1}\,K^{-1}}$ hydrophobic bond and $\kappa_{\perp,SiC} = 259 \pm 51\ \mathrm{W\,m^{-1}\,K^{-1}}$ hydrophilic); (e) and (f) show the same for extracted TBR$_{eff}$ (TBR$_{eff}$ = 6 + 4/−2 m^2 K GW^{-1} for hydrophobic bond and 9 + 3/−2 m^2 K GW^{-1} for hydrophilic).

taken at different locations on all samples, and the variation, which was observed, was included in the MC error analysis. In all cases, the thermal boundary resistance between the metal and the sample (TBR_{met}) and the SiC cross-plane thermal conductivity, $\kappa_{SiC,\perp}$, were fitted. For bonded samples, TBR_{eff} was fitted from the Si face. It was necessary to fit $\kappa_{SiC,\perp}$ for the bonded samples as there was a significant variation from sample to sample. This variation could arise from changes in growth and post-processing of the SiC as these wafers, although from the same vendor, were purchased several years apart.

A difference was also observed in the SiC thermal conductivity from the C to Si face with the Si face having a ~36% lower thermal conductivity than the C face on average. We expect the origin of this is the different polishing techniques used on either face. Studies have shown that polishing of SiC can result in subsurface damage, which extends to a depth of tens micrometers.[26] Similar trends have been observed in SiC wafers from other vendors although this was not ubiquitous, indicating that it is process dependent.[27] The results for all fitted parameters and samples are shown in Table III while example traces and histograms from MC analysis of bonded samples are shown in Fig. 4.

For both bonding processes, TBR_{eff} was found to be very low, $<10\ m^2\,K\,GW^{-1}$. In both cases, the interfaces appear to be well bonded while the low thermal conductivity, amorphous oxide at the interface is thin enough to avoid introducing a significant thermal resistance. The slightly higher value seen for the hydrophilic bond of $9+3/-2\ m^2\,K\,GW^{-1}$ compared to $6+4/-2\ m^2\,K\,GW^{-1}$ to the hydrophobic bond is unlikely to be a result of the different chemistry used. Instead, we believe that this is a result of the thicker interfacial layer. For the hydrophobic bond, this layer ranges from 0.25 to 2.5 nm thick, whereas, for the hydrophilic bond, this layer remained at 2.5 nm in all locations imaged (Fig. 1).

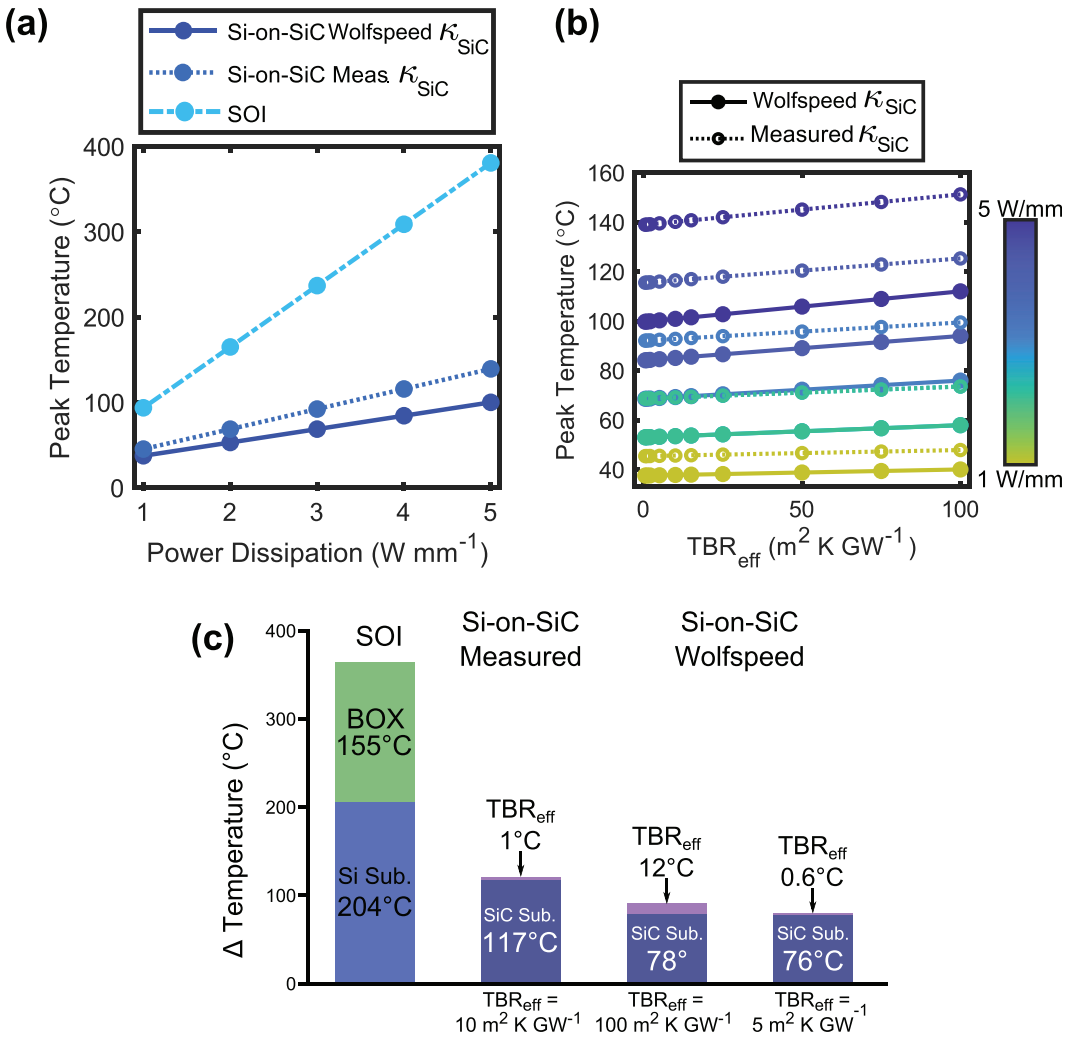

FIG. 5. (a) shows peak temperatures as a function of power dissipation for the example SOI and Si-on-SiC structure using $TBR_{eff} = 5\ m^2\,K\,GW^{-1}$ and $\kappa_{\perp,SiC} = 390\ W\,m^{-1}\,K^{-1}$ and $\kappa_{||,SiC} = 490\ W\,m^{-1}\,K^{-1}$ (Wolfspeed) or $\kappa_{\perp,SiC} = 259\ W\,m^{-1}\,K^{-1}$ and $\kappa_{||,SiC} = 325\ W\,m^{-1}\,K^{-1}$ (measured); (b) examines the effect of TBR_{eff} on the thermal management of Si-on-SiC devices at a range of power dissipations (1–5 W mm^{-1}); (c) examines temperature gradients across the layers at 5 W mm^{-1} power dissipation for SOI, the material measured here, and two hypothetical structures using 4H–SiC produced by Wolfspeed with $TBR_{eff} = 100\ m^2\,K\,GW^{-1}$ or $5\ m^2\,K\,GW^{-1}$.

Assuming a thermal conductivity of $\sim 1\,W\,m^{-1}\,K^{-1}$[26] for the amorphous interfacial layer, one would expect a minimum TBR_{eff} of $2.5\,m^2\,K\,GW^{-1}$ for the thickest layer seen in this work (2.5 nm, Fig. 2). However, this neglects the contribution of intrinsic TBR and any defects at the interfaces to TBR_{eff},[28] so naturally the actual TBR_{eff} will be higher than $2.5\,m^2\,K\,GW^{-1}$. Also, the effect of TBR_{eff} becomes vanishingly small below $10\,m^2\,K\,GW^{-1}$ and it is difficult to differentiate between 2.5 and $10\,m^2\,K\,GW^{-1}$ experimentally, reflected by the large error bars on the measured TBR_{eff} values.

The effect of TBR_{eff} and SiC thermal conductivity on device thermal resistance was examined using 2D FEA, steady-state thermal simulations, approximating a multi-finger device with a large gate width. The structures simulated are shown in Fig. 1 while results are shown in Fig. 5. For the Si-on-SiC device, a 10 nm thick layer was introduced at the Si/SiC interface, acting as an effective thermal boundary resistance (TBR_{eff}), varying its thermal conductivity to vary TBR_{eff} in the simulation. Considering the worst-case scenario from the samples examined in this work, $TBR_{eff} = 10\,m^2\,K\,GW^{-1}$ and $\kappa_{\perp,SiC,} = 259\,W\,m^{-1}\,K^{-1}$, we see a peak temperature of 140 °C at a power dissipation of $5\,W\,mm^{-1}$, simulated by internal heat generation inside the Si drift region. These simulations show a 67% decrease in temperature rise compared to an equivalent SOI device at the same power dissipation [Fig. 5(a)], despite the rather low SiC thermal conductivity. Using better quality SiC ($\kappa_{\perp,SiC} = 390\,W\,m^{-1}\,K^{-1}$[22]), this is improved to a 79% decrease assuming the same TBR_{eff}.

In Fig. 5(c), the origin of this benefit is examined in terms of the temperature gradient across the different layers in the structures. For SOI, the temperature is being dropped across both the BOX and Si substrate in similar quantities, whereas, for Si-on-SiC, most of the temperature is being dropped across the SiC. This implies a significant thermal improvement from removing the BOX. Additionally, we can see the effect of improving the substrate thermal conductivity as a much lower temperature gradient is observed across the SiC. The result of the improved thermal management for Si-on-SiC would be to increase device lifetime and reduce active cooling requirements.

In Fig. 5(b), the importance of TBR_{eff} for the thermal management of these devices is examined. In previous work, this parameter has been neglected.[2] However, these simulations demonstrate that, with good quality SiC, reducing TBR_{eff} from $100\,m^2\,K\,GW^{-1}$ to $<10\,m^2\,K\,GW^{-1}$ can result in a decrease in temperature rise by 11% at $5\,W\,mm^{-1}$. This is reinforced when examining the temperature gradients across the layers shown in Fig. 5(c). Such high TBR_{eff} values may be encountered when introducing thick, low thermal conductivity layers between the Si and SiC. This work demonstrates the importance of rigorous thermal characterization when preparing the Si-on-SiC material and fabricating devices. If TBR_{eff} were not considered and the variation in SiC thermal conductivity were to go unknown, it could have catastrophic results for these devices when deployed in space.

In summary, TBR_{eff} has been measured for two different direct-bonded Si-on-SiC wafers. Both hydrophobic and hydrophilic bonding results in interfaces with excellent thermal properties. Simulations have been used to show the thermal benefit of Si-on-SiC over conventional SOI. Even with low thermal conductivity SiC, Si-on-SiC results in a large decrease in peak temperatures at all power dissipations. These simulations also underlined the importance of considering, optimizing, and measuring the thermal properties of the Si/SiC interface when fabricating devices and simulating their thermal performance. This property can cause a large variation in peak temperatures particularly at higher power dissipation.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts of interest to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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