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Simulation of integrate-and-fire neuron circuits using HfO_2-based ferroelectric field effect transistors

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***Abstract*—Inspired by neurobiological systems, Spiking Neural Networks (SNNs) are gaining an increasing interest in the field of bio-inspired machine learning. Neurons, as central processing and short-term memory units of biological neural systems, are thus at the forefront of cutting-edge research approaches. The realization of CMOS circuits replicating neuronal features, namely the integration of action potentials and firing according to the all-or-nothing law, imposes various challenges like large area and power consumption. The non-volatile storage of polarization states and accumulative switching behavior of nanoscale HfO_2 - based Ferroelectric Field-Effect Transistors (FeFETs), promise to circumvent these issues. In this paper, we propose two FeFET-based neuronal circuits emulating the Integrate-and-Fire (I&F) behavior of biological neurons on the basis of SPICE simulations. Additionally, modulating the depolarization of the FeFETs enables the replication of a biology-based concept known as membrane leakage. The presented capacitor-free implementation is crucial for the development of neuromorphic systems that allow more complex features at a given area and power constraint.**

***Index Terms*—integrate-and-fire (I&F) neurons, leaky integration, neuromorphic circuits, ferroelectric FET (FeFET), hafnium oxide**

I. Introduction

In today's data-driven world, conventional computers fail to efficiently manage real-time data, due to the so called "von Neumann bottleneck" [1], [2]. In comparison, the brain is superior at processing data of changing environments and can make decision even in uncertain situations due to a superior processing rate [3]. It inspired the development of Artificial Neural Networks (ANNs) that excel at tasks involving real-time inputs and pattern recognition [4]. However, software implementations of ANNs on conventional computers are slow and power-hungry due to the parallel processing of complex computations [4], [5]. Biology minimizes the complexity of these computations by using spikes to represent information [6]. This led to the development of biological-inspired SNNs implemented on full-custom hardware. One of the main challenges is to balance biological plausibility with ease of implementation, to develop cost, area and power efficient circuits exhibiting performances similar to biology [7].

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As central processing and short-term memory elements in biological neural networks, neurons are at the forefront of interest for neuromorphic research. Here, the Leaky Integrate-and-Fire (LIF) model is a popular choice for VLSI systems due to its simplicity [8]–[10]. It is widely used in large, low power and massively parallel recurrent networks [11] to emulate the basic functionality of biological neurons, namely the integration of input signals to produce a spike-based output [7]. Conventional analog LIF neurons integrate input currents onto a membrane capacitor until the voltage across the capacitor exceeds a given threshold and triggers the generation of an output spike [12]. Not only do capacitors occupy significant chip area, their usage also results in large short circuit currents [6]. Recently, nanoscale HfO_2 - based FeFETs have demonstrated the ability to integrate action potentials symmetrically and fire according to the all-or-nothing law [13]. The full CMOS compatibility of small scaled FeFET devices makes them very promising candidates to replace the comparatively large capacitors in neuron circuits in state-of-the-art high-k metal gate technologies of the 28nm technology node [14]. This opens new possibilities for the development of hardware SNNs of high integration density [13].

In this work, we propose and simulate two different implementations of an I&F neuron circuit using HfO_2 - based FeFETs and demonstrate their ability to reproduce the integration and spiking behavior of biological neurons. The hysteretic behavior of the FeFETs was emulated by utilizing the Preisach hysteresis model [15] for a ferroelectric capacitor connected to the gate of an nFET. The complete FeFET model was adjusted to experimental data of single-device FeFETs. Further, the crucial feature of leaky integration of action potentials is implemented, resembling the LIF neuron model.

II. The Ferroelectric Field-Effect Transistor

Ferroelectric Field-Effect Transistors (FeFETs) are a specific type of nonvolatile storage elements [16]. Their gate stack comprises a ferroelectric layer, which has the function

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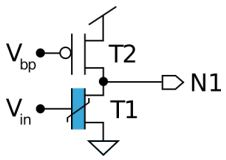

Fig. 1. Schematic of the 2-transistor (2T) circuit consisting of nFeFET T1 and pMOSFET T2. Input pulses (V_{in}) are applied at the T1 gate. The bias voltage V_{bp} controls the number of program pulses needed to shift the potential V_{N1} to generate an output spike. Transistor sizes are reported in Tab. I.

to modulate the transistor's channel conductivity through its stored spontaneous polarization P, described in the Preisach hysteresis model [15] as:

$$P = k \cdot P_{\mathrm{s}} \cdot \tanh\left(\frac{E_{\mathrm{eff}} \pm E_{\mathrm{c}}}{2\delta}\right) + P_{\mathrm{off}} \quad , \tag{1}$$

where

$$\delta = E_{\mathrm{c}} \cdot \left[\ln\left(\frac{1 + P_{\mathrm{r}}/P_{\mathrm{s}}}{1 - P_{\mathrm{r}}/P_{\mathrm{s}}}\right)\right]^{-1} \quad . \tag{2}$$

P_{s}, P_{r} and E_{c} are the saturation polarization, the remanent polarization and the coercive electric field, respectively. The scaling factor k and the offset P_{off} include information about the history of the ferroelectric layer. The effective electric field E_{eff} is time-dependent:

$$\frac{\mathrm{d}E_{\mathrm{eff}}(t)}{\mathrm{d}t} = \frac{E_{\mathrm{ext}}(t) - E_{\mathrm{eff}}(t)}{\tau_{\mathrm{eff}}} \quad , \tag{3}$$

where E_{ext} is the applied electric field. The time-dependency is reflected in delay parameter τ_{eff}. To write a polarization state into the ferroelectric layer, an electric field, sufficiently high to switch the ferroelectric domains, is applied. To set the FeFET into a high threshold voltage (HVT) state (erase operation), either a negative voltage is a applied at the gate while keeping all other terminals grounded, or a positive voltage is fed to the bulk, source, and drain terminals while grounding the gate. Conversely, applying a positive voltage at the gate, with all other terminals grounded, sets the FeFET into the low threshold voltage (LVT) state (program operation). To read the stored state, the readout voltage at the gate is chosen such that the resulting drain current is either high (LVT) or low (HVT). Alternatively, the FeFET can be fully programmed/erased by applying a sequence of pulses, each of which is, however, insufficient to induce an appreciable switching effect alone [17]. This accumulative switching, attributed to progressive polarization reversal within the ferroelectric material, will be exploited to simulate the I&F behavior.

III. Integrate-and-Fire neuron circuits

The difference in drain current corresponding to different FeFET polarization levels was utilized to implement the I&F circuits shown in Fig. 1 and 2. During the experiments, sequences of voltages were applied at V_{in}, consisting of a program pulse (2 V, 0.1 µs) followed by a read pulse (0.2 V, 9.7 µs) and an intermediate phase of 9.9 µs with $V_{in} = 0$ V. The nFeFET was initially in its HVT state and the read voltage was chosen below this high threshold voltage (V_{th}), turning

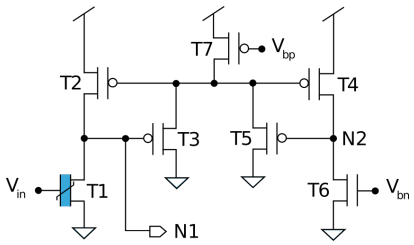

Fig. 2. Schematic of the 7-transistor (7T) circuit. T1 represents the nFeFET. V_{bp} and V_{bn} are biasing voltages. After a sufficient number of input pulses applied at V_{in}, the voltage V_{N1} shifts down during the read phase triggering the spike generator output. Transistor sizes are reported in Tab. I.

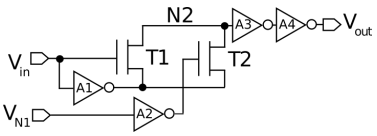

Fig. 3. The spike generator circuit generates a 1 V output spike at V_{out} only during the read phase (low V_{in}) if V_{N1} is below the switching threshold of the inverter A2. It receives V_{N1} from the neuron circuits shown in Fig. 1 and 2 and V_{in} is the input voltage shared with the neuron circuits. The negative reset pulse to the FeFET to end the spike is provided externally.

TABLE I: Transistor sizes used in the two neuron circuits

Transistor	2T WxL (nm)	7T WxL (nm)
T1, nFeFET	500x500	500x500
T2, pMOS	1000x100	240x30
T3-T5, pMOS		30x30
T6, nMOS		500x30
T7, pMOS		80x30

the transistor T1 off. After an output spike from the spike generator (Fig. 3) the FeFET was reset to its initial HVT state by externally applying a reset pulse (−4 V, 10 µs). After 1 ms, new voltage pulses were applied to the circuits.

A. 2-transistor (2T) implementation

The 2T implementation consists of a pMOSFET connected in series to the nFeFET (Fig. 1). It uses the fact that V_{N1} settles to a value to balance the currents flowing through both transistors. The bias V_{bp} applied to T2 ensures that as long as the nFeFET T1 remains in HVT state, V_{N1} also remains above the detection threshold of the spike generator (Fig. 3), resulting in no output spike. With each input pulse applied at V_{in}, T1 accumulatively switches towards the LVT state, reducing its V_{th}. After accumulating several input pulses, the lower V_{th} of T1 allows a noticeable current flow during the read phase. Thus, V_{N1} reduces, which is detected by the spike generator, emitting a high output spike at V_{out}.

B. 7-transistor (7T) implementation

The 7T circuit (Fig. 2) is based on the Lazzaro's hysteretic Winner-take-all circuit which implements a nonlinear inhibition. Only one of the two outputs of this circuit (N1 or N2) is at a high voltage level, suppressing the other node [18]. Which node is "winning" is decided based on the current flowing in the two outer branches set by T1 and T6. In the presented

implementation, one of the input transistors is replaced by the nFeFET T1. The sub-threshold bias V_{bp} at T7 limits the total current flow through T3 and T5. V_{bn} is set to ensure that the drain current through T6 is larger than the current through T1 in HVT state. T2 and T4 have a common gate voltage, so their drain voltages vary to accommodate the different currents in the two outer branches. While the FeFET is in the HVT state, the potential V_{N1} does not trigger the spike generator (Fig. 3). Once a sufficient number of input pulses accumulatively switch T1 to the LVT state, the increasing current through T1 causes V_{N1} to decrease, triggering the spike generator and resulting in a high output spike.

C. Spike generator circuit

Because the high amplitude program pulses surpass the threshold voltage of the FeFETs and result in undesired shifts of the voltage V_{N1}, we use the spike generator shown in Fig. 3 to generate the output spikes only during the read phase. The two transistors T1 and T2 realize a NOR logic gate and the two inverters A3 and A4 are used to obtain a 1 V output spike. When V_{N1} is low during the read phase ($V_{in} = 0.2\,\mathrm{V}$), the inverters A1 and A2 enable the right input branch and provide a high voltage to A3, resulting in a high V_{out}. Similarly, the left branch would provide a high voltage to inverter A3 when both V_{in} and V_{N1} are high, which will not happen in the presented neuron circuits. In all other cases, the output remains at 0 V.

D. Reset operation

The focus of this work is to investigate the adoption of accumulative switching behavior of FeFETs as input node of LIF neurons. One important aspect, however, is the reset of the FeFET devices after triggering an output spike. The reset might be realized by switching V_{in} to a negative voltage, e.g. by adding an additional transistor from the input node to a fixed negative bias point, its gate being triggered by the rising edge of output pulses. A more detailed analysis of the reset operation is the focus of ongoing research.

IV. Results

For simulations the 28SLP-based FeFET technology from GLOBALFOUNDRIES with a supply voltage of 1 V was used. Fig. 4 - Fig. 7 show the time course of V_{in} and V_{out} during the experiments. After a sufficient number of program pulses, the spike generator emitted a 1 V output spike (V_{out}) during the read phase.

A. 2 transistor circuit

Program pulses applied to the FeFET T1 shifted its polarization towards the LVT state, resulting in a decrease of V_{N1} during the read phase as shown in Fig. 4. For $V_{bp} = 0.85\,\mathrm{V}$, eight program pulses were required to set the threshold voltage of the FeFET and the potential V_{N1} low enough to trigger the spike generator during the read phase.

The value of V_{bp} determined the drain current of T2, which in-turn affected the drain voltage V_{N1}. Fig. 6a shows how varying V_{bp} alters the number of program pulses needed to produce an output spike.

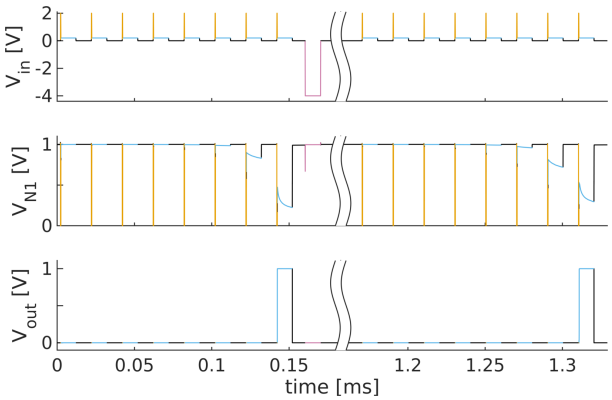

Fig. 4. Simulation results of the 2T circuit. V_{in} is the input voltage at the FeFET gate and V_{N1} depicts the voltage at node N1. V_{out} is the output of the spike generator. With a bias voltage of $V_{bp} = 0.85\,\mathrm{V}$, eight input pulses ($V_{in} = 2\,\mathrm{V}$) are required to program (orange) the nFeFET to produce an output spike during the read phase (blue) ($V_{in} = 0.2\,\mathrm{V}$). After the reset pulse (purple) of $-4\,\mathrm{V}$ there is a 1 ms break.

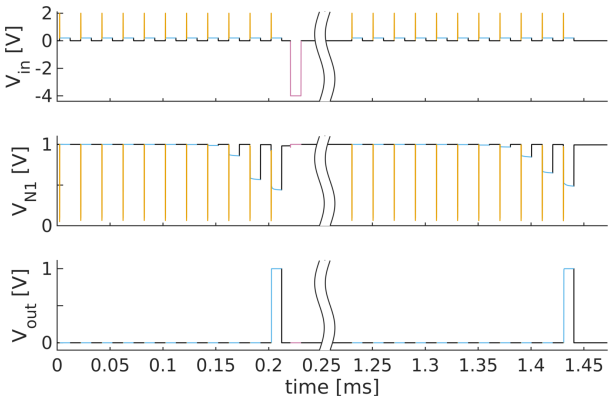

Fig. 5. Simulation results of the 7T circuit. V_{in}, V_{N1} and V_{out} represent the input voltage, the voltage at node N1 and the output voltage of the spike generator, respectively. With a bias voltage of $V_{bn} = 0.25\,\mathrm{V}$, 11 input pulses ($V_{in} = 2\,\mathrm{V}$, orange) are required to program the nFeFET to produce an output spike during the read phase ($V_{in} = 0.2\,\mathrm{V}$, blue). After the reset pulse (purple) of $-4\,\mathrm{V}$ there is a 1 ms break.

B. 7 transistor circuit

For $V_{bn} = 0.25\,\mathrm{V}$, V_{N1} gradually decreased during the read phase after nine input program pulses had been applied at V_{in} (Fig. 5). Here, 11 program pulses resulted in a sufficiently low V_{N1} to give rise to a high V_{out} of the spike generator during the read phase. Increasing the bias voltage V_{bn} increased the drain current flowing through T6, thus requiring a lower threshold voltage of the FeFET for an output spike to occur. This lower threshold voltage was reached by providing more program pulses to the FeFET (see Fig. 6b).

C. Leaky integration

In biological neurons action potentials are integrated in a leaky manner, i.e. the value of integrated input potentials begins to decrease slowly when there are no consecutive input pulses. The 7T circuit was analyzed to exploit the erase operation of the FeFET to mimic this behavior. Small

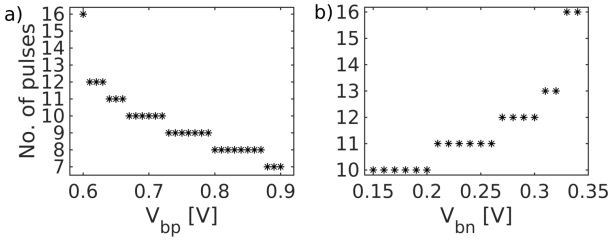

Fig. 6. Number of program pulses required for generating an output spike during the read phase as a function of the bias voltages for the **a)** 2T circuit and **b)** 7T circuit.

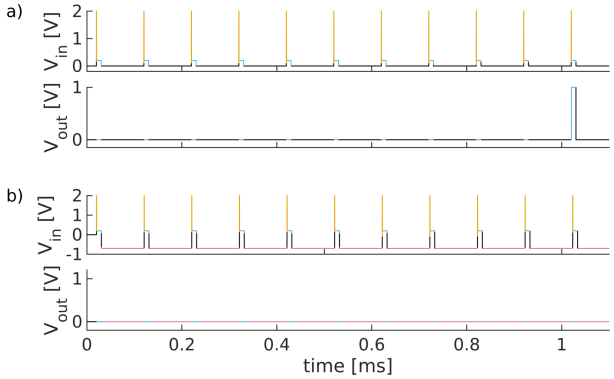

Fig. 7. Simulation of leaky integration in the 7T circuit. V_{in} is the input voltage applied to the gate of the FeFET and consists of a program (orange) (2 V, 0.1 µs), a read (blue) (0.2 V, 9.7 µs) and a leakage phase (V_{leak}, 90 µs). V_{out} is the output voltage of the spike generator. **a)** Without leakage (V_{leak} = 0 V, black), after the 11th program pulse an output spike is emitted. **b)** When leakage is enabled ($V_{leak} = -0.7$ V, purple), no output spike is emitted.

negative voltages applied at V_{in} accumulatively reversed the polarization of the FeFET, shifting its V_{th} towards the HVT state. We divided V_{in} into three phases: a program pulse (2 V, 0.1 µs) followed by a read phase (0.2 V, 9.7 µs) and a leakage phase (-0.7 V, 90 µs). Fig. 7 shows the input to the 7T circuit and the output of the spike generator after a set of program pulses. First, in Fig. 7a the leakage mechanism was disabled by applying 0 V during the leakage phase. The read phase after 11 program pulses resulted in an output spike. However, when V_{in} was set to -0.7 V during the leakage phase as shown in Fig. 7b, the leakage mechanism was enabled and no output spike occurred after 11 program pulses. As the observed behavior is a property of the FeFET, the same feature can be demonstrated in the 2T circuit. Additionally, the leakage strength can be controlled by varying the negative voltage applied between the program-read pairs, as has been experimentally demonstrated on FeFETs (see Fig. 5 in ref. [13]).

V. Conclusions

We simulated two I&F neuron circuits using HfO_2 - based FeFETs and show the possibility of a leaky integration. These circuits effectively eliminate the need for capacitors in analog VLSI SNNs. The undesired voltage shifts of V_{N1} during program pulses were suppressed by the spike generator. By ways of an additional bias transistor, the 7T circuit offers an additional tuning parameter of the circuit. The exact implementation of the reset operation after an output spike will be explored further. An intentionally unstable polarization in a properly designed gate stack, which spontaneously switches back from the LVT into the HVT state, could mimic the leaky behavior and replace the applied negative bias voltage [13]. Combining ferroelectric synapses [19] with the circuits shown in this work can pave the way to the development of an all ferroelectric neural network implementation.

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