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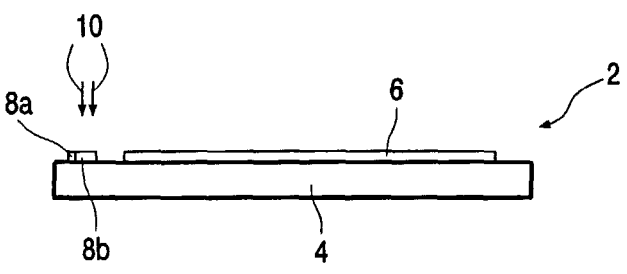
(54) Title: ACTIVE MATRIX DISPLAY DEVICES AND THE MANUFACTURE THEREOF



(57) Abstract: An active plate (2) for an active matrix display device (16), the active plate (2) comprising a substrate (4), a pixel area (6) and an adjacent drive circuit area (8). Both areas include polycrystalline silicon material formed by a process in which a metal is used to enhance the crystallisation process (MIC poly-Si), but only the MIC poly-Si in the drive circuit area (8) is subjected to an irradiation process using an energy beam (10). TFTs are fabricated with MIC poly-Si which have leakage currents in the off state sufficiently low for them to be acceptable for use as switching elements in the pixel area of matrix display devices. As only the drive circuit area (8) need be irradiated to provide poly-Si having the desired mobility, the time taken by the irradiation process can be significantly reduced.

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DESCRIPTION

ACTIVE MATRIX DISPLAY DEVICES AND THE MANUFACTURE THEREOF

The present invention relates to active matrix display devices comprising polycrystalline silicon thin film transistors and the manufacture thereof.

The high carrier mobility of polycrystalline silicon (poly-Si) relative to amorphous silicon (a-Si) makes it an attractive material for use in large area electronic devices such as active matrix liquid crystal displays (AMLCDs) and active matrix polymer LED displays (AMPLEDs). Conventionally, poly-Si films used for example in thin film transistors (TFTs) have been manufactured by solid phase crystallisation (SPC). This involves depositing an a-Si film on an insulating substrate and crystallising the a-Si film by exposing it to a high temperature for a prolonged period of time, that is typically a temperature in excess of 600°C for up to 24 hours.

As an alternative, US-A-5147826 discloses a lower temperature method of crystallising an a-Si film,comprising the steps of depositing a thin film of nickel for example on the a-Si film and annealing the film. The metal catalyses crystal growth at temperatures below 600°C and also provides more rapid crystal growth than would otherwise occur. For example, a typical anneal using the method of US-A-5147826 might be at around 550°C for 10 hours. This represents an improvement over prior methods for at least two reasons: first, it enables low cost non-alkali glass substrates such as borosilicate to be used which would normally suffer glass compaction and warp at temperatures of 600°C or more; and secondly, as the anneal duration is reduced, the manufacturing throughput rate is increased and therefore the associated manufacturing cost may be reduced. The contents of US-A-5147826 are incorporated herein by reference.

Polycrystalline silicon material formed by a process in which a metal element is used to enhance the crystallisation process, as described in US-A-

5147826 for example, is referred to hereinafter as metal induced crystallisation poly-Si or MIC poly-Si.

In known active matrix display devices, the displayed image is created by an array of pixels, distributed in rows and columns over the "pixel area" of a substrate of the device. One or more TFTs are provided in each pixel to control the respective pixel. Integrated drive circuits comprising TFTs are provided in a "drive circuit area" on the same substrate, around the pixel area. Signals defining the images to be displayed are fed to the drive circuits which in turn send signals to the pixels to generate the images. As described in US-A-5756364, it is desirable for the TFTs of the drive circuit area to have a high mobility, whilst in the pixel area, it is more important that the TFTs have a sufficiently small off-current and that the variation in off-current of the TFTs across the display is minimised. The contents of US-A-5756364 are incorporated herein by reference.

US-A-5756364 discloses that the crystallinity of MIC poly-Si may be improved by illuminating it with laser light. It states that TFTs formed in this way have a relatively high mobility of more than 100 cm^2/Vs, making them suitable for the drive circuitry of an active matrix display. Such TFTs are said however to have large off-currents that greatly vary from one transistor to another, making them unsuitable for use in the pixel area of a display. It proposes the formation of MIC poly-Si only in the drive circuit area, followed by illumination of the drive circuit and pixel areas with different respective laser illumination energy densities, which forms poly-Si in the pixel area. The TFTs in the drive circuit area have the suitable properties noted above, whilst the TFTs created in the pixel area have a relatively small mobility of less than 20 cm^2/Vs, but a small off-current variation. In order to restrict the formation of MIC poly-Si to drive circuit area, a silicon dioxide mask is formed over the pixel area prior to addition of a solution containing the metal element used to enhance the crystallisation process.

It is an object of the present invention to provide an improved active matrix display device comprising poly-Si with different electrical properties in

the drive circuit and pixel areas of the device, and a process for fabricating such a device.

The present invention provides an active plate for an active matrix display device, the active plate comprising a substrate, a pixel area and an adjacent drive circuit area, both areas including MIC poly-Si, with only MIC poly-Si in the drive circuit area having been subjected to an annealing process using an energy beam.

The invention further provides a method of fabricating an active plate for a matrix display device, the active plate having a pixel area and an adjacent drive circuit area, the method comprising the steps of:

(a) depositing an amorphous silicon film on a substrate;

(b) adding to the pixel and drive circuit areas a metal element for accelerating crystallisation of amorphous silicon;

(c) heating the substrate to crystallise amorphous silicon in the film to form MIC poly-Si; and

(d) irradiating MIC poly-Si in the drive circuit area with an energy beam.

TFTs manufactured using MIC techniques have been hampered by the problem of relatively high leakage currents in their "off" state, making them unsuitable for use in applications such as the pixel area of AMLCDs. The applicant has determined that TFTs may be fabricated with MIC poly-Si which have leakage currents in the off state sufficiently low for them to be acceptable for use as switching elements in the pixel area of matrix display devices.

The applicant has determined that certain combinations of process parameters yield devices with surprisingly good operating characteristics. It is believed that the combination of longer anneal times of 24 hours or more with average nickel concentrations in the polycrystalline silicon material of 10^{18} to $5x10^{19}$ atoms/cm^3 are particularly beneficial. Preferably, the anneal time is 36 hours or more. Furthermore, the average nickel concentration in the polycrystalline material is preferably in the range $2.5x10^{18}$ to $2.5x10^{19}$ atoms/cm^3.

Also, it is thought that the combination of an anneal time of 24 hours or more, with average nickel concentrations in the poly-Si material of 10^{18} to $5x10^{19}$ atoms/cm^3, and the use of ion implantation to dose the a-Si with nickel leads to substantially improved results. Longer anneal times of 36 hours or more and/or nickel concentrations in the polycrystalline material in the range $2.5x10^{18}$ to $2.5x10^{19}$ atoms/cm^3 may also be advantageously employed in this process.

Previously, it has been suggested that unacceptably high leakage currents in poly-Si TFTs formed by MIC processes are caused by the presence of the catalyst ion, for example, nickel. However, the applicant has found that a significant cause of leakage is regions of uncrystallised a-Si remaining after the MIC process. If longer anneal times are employed, crystallisation occurs in two ways so as to reduce the size of or even remove these a-Si regions. During the initial phase of crystallisation, MIC is dominant. The a-Si film is crystallised into needle-like grains by the migration of a $NiSi_2$ silicide phase. However, the $NiSi_2$ precipitates are stopped when they meet other grain boundaries, other Si needles, or the top and bottom of the a-Si surfaces. Thus, this stage ends, leaving small amounts of a-Si between the needle-like grain structures. If annealing is continued, the thickness of the needle-like grains is increased by SPC, thereby reducing the remaining volume of a-Si.

As described above, it has been found that the combination of longer annealing times with other predetermined parameters provides poly-Si material with improved characteristics. The use of longer anneal times is compensated for by the trend in AMLCD manufacture towards the production of smaller display substrates with higher levels of specialised integration of circuitry in poly-Si on the substrate (in personal digital assistants, and mobile telephones for example), as the desire for high throughput of such devices will not be so great. Also batches of smaller displays can be started through the annealing process at intervals to provide the requisite supply of substrates without the use of an impractically large and expensive furnace.

The applicant has also found that the use of metal atoms in the concentration range $1.3x10^{18}$ to $7.5x10^{18}$ atoms/cm^3 enables polycrystalline

semiconductor TFTs to be formed with leakage properties acceptable for use in the pixel area of an active matrix display device with an annealing process of duration significantly less than previously thought necessary. Such TFTs and methods for their manufacture are described in copending United Kingdom Patent Application No. 0215566.1 (our ref. PHGB 020109), the contents of which are incorporated herein by reference. Whilst an annealing time of 20 hours at a temperature of around 550°C achieves the desired properties, it has also been realised that the metal concentrations disclosed above enable this time to be reduced to 10 hours or even 8 hours or less at a temperature of 600°C or less. This leads to substantial productivity and efficiency increases in the manufacturing process.

Preferably, the average concentration of metal atoms in the polycrystalline semiconductor material is in the range $1.9x10^{18}$ atoms/cm^3 to $5x10^{18}$ atoms/cm^3. More preferably, the average concentration of metal atoms is around $2.5x10^{18}$ atoms/cm^3.

Furthermore, it has been found that the application of an electric field to a substrate during the MIC annealing process (often referred to a field enhanced MIC or FEMIC) may accelerate the process, reducing its duration. An example of FEMIC is described in "Electric-field-enhanced crystallization of amorphous silicon" by Jin Jang et al, Nature, Vol. 395, p481-483, the contents of which are incorporated herein by reference.

It will be appreciated that other metals may be used instead of or together with nickel in MIC processes. For example, one or more elements selected from the group consisting of Ni, Cr, Co, Pd, Pt, Cu, Ag, Au, In, Sn, Pb, As, and Sb may be employed. More preferably, one or more elements from the group Ni, Co and Pd are used.

Ion implantation is preferably used to dose a-Si with metal in a MIC procedure as it affords precise control over dosage, uniformity and ion depth. Nevertheless, other methods may be employed for this purpose. For example, the metal atoms may be applied the a-Si in a solution, typically by a spin-coating process. Other processes include sputtering or sol-gel coating a layer of nickel, and the use of a nickel precursor during the a-Si CVD process.

As MIC poly-Si is formed in both the pixel and drive circuit area in the present invention, this obviates the need for the deposition and patterning of a silicon dioxide mask to restrict the introduction of the metal element used in the MIC process, as is the case in the methods of US-A-5756364. The fabrication process is thereby simplified and made more cost effective.

Furthermore, as only MIC poly-Si in the drive circuit area is subjected to an annealing process using an energy beam, the time taken by this step can be significantly reduced.

Typically, the energy beam will be generated by a laser, but it will be appreciated that other types of radiation may be used, such as infra-red radiation for example.

As noted in US-A-5756364, a pulsed oscillation laser may be used in the laser annealing process. The use of pulses of short duration helps to minimise heating of the display substrate during the crystallisation procedure. The present inventors have realised that, when a pulsed oscillation laser is used, there may be sufficient variation in the intensity of the energy pulses generated by the laser to lead to significant non-uniformity in the quality of the MIC poly-Si. As noted above, it is particularly important to minimise variations in the properties of the TFTs in the pixel area of a display device to avoid degradation of displayed images. The present invention provides the further advantage that MIC poly-Si can be formed without a laser annealing treatment in areas of the device susceptible to variations resulting from the use of a pulsed laser, such as the pixel area. This is beneficial in the case of an AMPLED, wherein the TFTs in the pixels have an analogue role in controlling the amount of current fed to each PLED.

The drive circuit area of the device may comprise both digital and analogue circuitry. For example, both digital processing circuitry and analogue to digital converters may be provided. Preferably, only the polycrystalline silicon material within the digital circuitry of the drive circuit area has been subjected to a laser annealing process. This is because the analogue circuitry is likely to be more susceptible to variations in the properties of constituent TFTs caused by pulse-to-pulse variations during the laser annealing process.

Embodiments of the invention will now be described by way of example and with reference to the accompanying schematic drawings, wherein:

Figure 1 shows a plan view of the active plate of an active matrix display device according to a first embodiment of the invention;

Figure 2 shows a cross-sectional side view along line A-A of Figure 1;

Figure 3 shows a plan view of the active plate of an active matrix display device according to a second embodiment of the invention; and

Figure 4 shows a side view of an active matrix device including an active plate embodying the invention.

It should be noted that the Figures are diagrammatic and not drawn to scale.

The active plate 2 of Figure 1 comprises a substrate 4 for use in an active matrix display, typically formed of glass. On the upper surface thereof are defined a rectangular pixel area 6 and an adjacent peripheral drive circuit area 8 formed of circuitry for driving pixels making up the pixel area. Leads connecting to the substrate and interconnecting the drive and pixel areas are omitted for clarity in the Figure. The width, w, of the elongate peripheral drive circuit area extending along two sides of the pixel area may typically be of the order of 5mm. The length, d, of a diagonal across the pixel area may vary from around 60mm for smaller displays used in handheld devices, up to around 430mm or more for desktop or LC-TV displays. It can therefore be seen that the drive circuit area 8 is a small fraction of the combined area of the pixel and drive circuit areas. As only the drive circuit area or a proportion of it need be subjected to a laser annealing process in accordance with the invention, the time taken for this step can be substantially reduced.

The drive circuit area 8 shown in Figure 1 comprises regions 8a and 8b where analogue circuitry and digital circuitry, respectively, are provided in the finished display device. In a preferred embodiment, only material in digital circuitry regions 8b is subjected to a laser annealing process, as described above.

A method of forming poly-Si material on a substrate in the configuration shown in Figure 1 will now be described. Firstly, a layer of silicon dioxide is deposited over the substrate to a depth of around 200nm, using plasma enhanced chemical vapour deposition (PECVD) for example. A film of amorphous silicon is then deposited by PECVD, which is around 40nm thick.

An areal density of nickel of around $1x10^{13}$ atoms/cm^2 is then implanted into the a-Si layer at an implantation energy typically of 20keV. Energies of up to 30keV have been successfully used with layers of this thickness to create TFTs with the desired leakage characteristics. It can be seen that the average concentration of nickel atoms in the 40nm thick a-Si layer resulting from this dose is therefore around $2.5x10^{18}$ atoms/cm^3.

The semiconductor material is crystallised by annealing, preferably in N_2 atmosphere, for around 8 hours at 550°C.

The MIC poly-Si film in the drive circuit area 8 is then irradiated using a KrF excimer laser which emits a rectangular beam, for example.

Figure 2 shows a cross-sectional side now along line A-A of Figure 1. It illustrates the irradiation of digital circuitry region 8b using a laser beam 10, whereas the pixel area 6 and analogue circuitry region 8a are not irradiated with the beam.

The length of the laser beam 10 at the substrate surface is preferably at least as great as the length of the longer of the limbs of the L-shaped drive circuit area. As only the drive circuit area is to be annealed using the laser, irradiation may be carried out by scanning the beam over one of the limbs of the L-shaped drive circuit area, and then rotating the substrate or laser beam through 90 degrees, before scanning the beam over the remainder of the area. Alternatively, after irradiating one limb of the drive circuit area, the beam width may be reduced so that a more intense, narrower beam may be swept more quickly over the remainder of the area, continuing in the same direction.

It will be appreciated that the time taken for the laser annealing process may be further reduced by locating the drive circuitry in a more compact area. Only a single scanning operation in one direction of constant width may then be required. For example, as shown in Figure 3, the drive circuit area 8 may

be provided along one side only of the pixel area 6. Both sets of row and column electrodes may be driven from one side of the display in this way by provision of an additional set of electrodes running from the drive area 8, across the pixel area 6 parallel to the column electrodes, with each of the additional electrodes connecting to a respective row electrode.

The resulting MIC poly-Si material is patterned to define the semiconductor bodies of the TFTs in the drive circuit and pixel areas 8, 6. Photolithography, implantation, deposition and etching process steps may then be carried out in a known manner to form the individual poly-Si TFT structures.

It is preferable to carry out a plasma hydrogenation process after fabrication of the TFTs to improve their performance. It is believed by the inventors that this is especially beneficial for material fabricated by the methods described herein which create poly-Si material films with little or no amorphous material present. Typically, this is carried out at around 350°C for about 1 hour.

An AMLCD 16, as shown in side view in Figure 4, may be formed in a known manner by sandwiching a layer of liquid crystal material 14 between a completed active plate 2 and a passive plate 12.

Whilst embodiments of the invention are described herein with reference to silicon material, it will be apparent that compound semiconductor films (for example silicon films containing germanium) may be used in accordance with the invention.

In the example described above, the invention is embodied in an AMLCD. It will be appreciated that the invention may also be advantageously employed in other active matrix display devices such as AMPLEDs, which include switching matrices and integrated circuitry on the same substrate.

From reading the present disclosure, other variations and modifications will be apparent to persons skilled in the art. Such variations and modifications may involve equivalent and other features which are already known in the art, and which may be used instead of or in addition to features already described herein.

Although Claims have been formulated in this Application to particular combinations of features, it should be understood that the scope of the disclosure of the present invention also includes any novel feature or any novel combination of features disclosed herein either explicitly or implicitly or any generalisation thereof, whether or not it relates to the same invention as presently claimed in any Claim and whether or not it mitigates any or all of the same technical problems as does the present invention.

The applicant hereby give notice that new Claims may be formulated to such features and/or combinations of such features during the prosecution of the present Application or of any further Application derived therefrom.

CLAIMS

1. An active plate (2) for an active matrix display device (16), the active plate (2) comprising a substrate (4), a pixel area (6) and an adjacent drive circuit area (8), both areas including MIC poly-Si, with only MIC poly-Si in the drive circuit area (8) having been subjected to an annealing process using an energy beam (10).

2. An active plate (2) of Claim 1 wherein the drive circuit area (8) comprises a digital circuitry region (8b) and an analogue circuitry region (8a), each including MIC poly-Si, with only MIC poly-Si in the digital circuitry region having been subjected to an annealing process using an energy beam (10).

3. An active plate (2) of Claim 1 or Claim 2 wherein substantially all the MIC poly-Si of the drive circuit area (8) is located to one side of the pixel area (6).

4. An active plate (2) of any preceding Claim wherein the MIC poly-Si includes nickel at a concentration in the range of 1.3×10^{18} to 7.5×10^{18} atoms/cm^3.

5. An active plate (2) of Claim 4 wherein the MIC poly-Si includes nickel at a concentration around 2.5×10^{18} atoms/cm^3.

6. An active matrix display device (16) including an active plate (2) of any preceding claim.

7. A method of fabricating an active plate (2) for a matrix display device (16), the active plate having a pixel area (6) and an adjacent drive circuit area (8), the method comprising the steps of:

(a) depositing an amorphous silicon film on a substrate (4);

(b) adding to the pixel and drive circuit areas (6, 8) a metal element for accelerating crystallisation of amorphous silicon;

(c) heating the substrate (4) to crystallise amorphous silicon in the film to form MIC poly-Si; and

(d) irradiating MIC poly-Si in the drive circuit area (8) with an energy beam (10).

8. A method of Claim 7 wherein the drive circuit area comprises a digital circuitry region and an analogue circuitry region, each including MIC poly-Si, and in step (d) only MIC poly-Si to be used in the digital circuitry region (8b) of the finished plate (2) is irradiated with the energy beam (10).

9. A method of Claim 7 or Claim 8 wherein in step (b) the metal element is nickel and it is added to the amorphous silicon film at a concentration in the range 1.3×10^{18} to 7.5×10^{18} atoms/cm^3.

10. A method of Claim 9 wherein in step (b) the metal element is nickel and it is added to the amorphous silicon film at a concentration around 2.5×10^{18} atoms/cm^3.

11. An active plate for an active matrix display device substantially as described herein with reference to the accompanying Drawings.

12. An active matrix display device substantially as described herein with reference to the accompanying Drawings.

13. A method of fabricating an active plate for an active matrix display device substantially as described herein with reference to the accompanying Drawings.

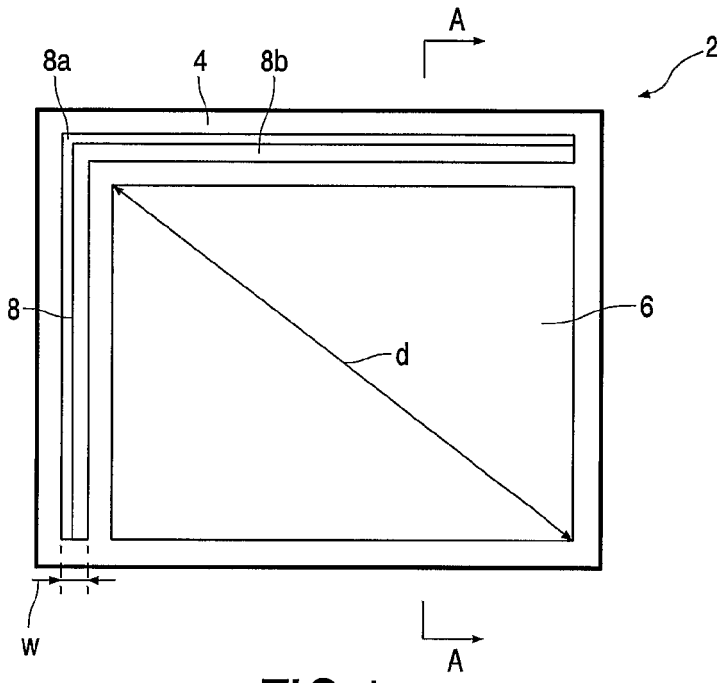

FIG.1

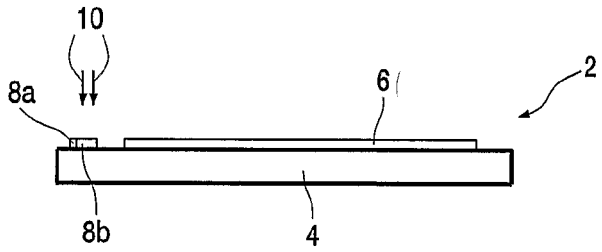

FIG.2

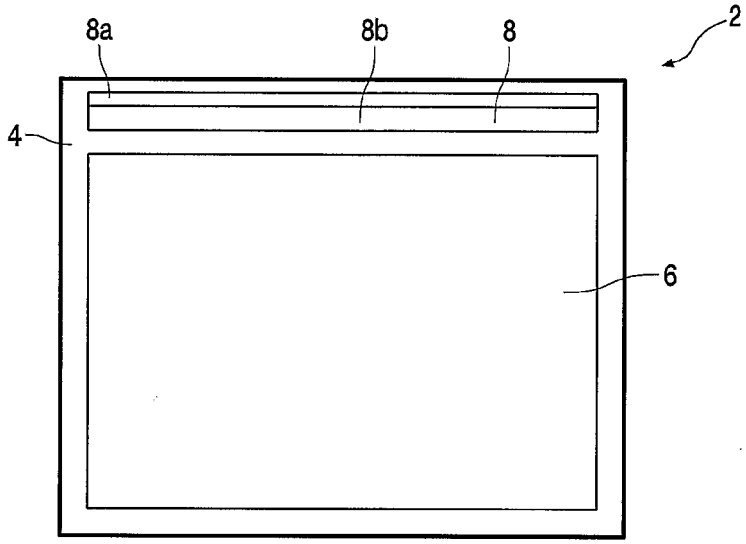

FIG.3

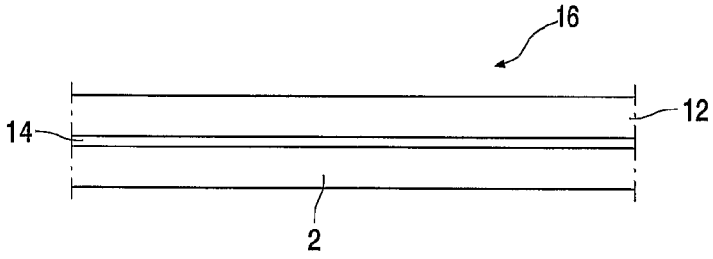

FIG.4

INTERNATIONAL SEARCH REPORT

Intel ~ al Application No
PCT/IB 03/02063

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20 H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GANG LIU ET AL: "SELECTIVE AREA CRYSTALLIZATION OF AMORPHOUS SILICON FILMS BY LOW-TEMPERATURE RAPID THERMAL ANNEALING" APPLIED PHYSICS LETTERS, AMERICAN INSTITUTE OF PHYSICS. NEW YORK, US, vol. 55, no. 7, 14 August 1989 (1989-08-14), pages 660-662, XP000080893 ISSN: 0003-6951 the whole document	1-10

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
4 September 2003	12/09/2003

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Agne, M

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	KHAKIFIROOZ A ET AL: "UV-assisted nickel-induced crystallization of amorphous silicon" PREPARATION AND CHARACTERIZATION, ELSEVIER SEQUOIA, NL, vol. 383, no. 1-2, 15 February 2001 (2001-02-15), pages 241-243, XP004317347 ISSN: 0040-6090 the whole document ---	1-10
A	US 6 084 247 A (TAKEMURA YASUHIKO ET AL) 4 July 2000 (2000-07-04) column 3, line 1 - line 20 column 4, line 7 - line 14 column 8, line 50 -column 11, line 27 column 25, line 10 -column 26, line 63 ---	1-10
A	PARK K-C ET AL: "Poly-Si thin film transistors fabricated by combining excimer laser annealing and metal induced lateral crystallization" JOURNAL OF NON-CRYSTALLINE SOLIDS, NORTH-HOLLAND PHYSICS PUBLISHING. AMSTERDAM, NL, vol. 299-302, April 2002 (2002-04), pages 1330-1334, XP004353226 ISSN: 0022-3093 the whole document -----	1-10

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

Continuation of Box I.2

Claims Nos.: 11-13

Claims 11-13 generally refer to the description and drawings, but they do not contain any technical features of the claimed subject-matter. Their scope is entirely unclear.

The applicant's attention is drawn to the fact that claims, or parts of claims, relating to inventions in respect of which no international search report has been established need not be the subject of an international preliminary examination (Rule 66.1(e) PCT). The applicant is advised that the EPO policy when acting as an International Preliminary Examining Authority is normally not to carry out a preliminary examination on matter which has not been searched. This is the case irrespective of whether or not the claims are amended following receipt of the search report or during any Chapter II procedure.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 03/02063

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☒ Claims Nos.: 11-13
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:
see FURTHER INFORMATION sheet PCT/ISA/210

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

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