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DEVELOPING NON-INVASIVE PROCESSING METHODOLOGIES AND UNDERSTANDING THE MATERIALS PROPERTIES OF SOLUTION-PROCESSABLE ORGANIC SEMICONDUCTORS FOR ORGANIC ELECTRONICS

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by

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Dedication

To my family.

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Essential to the success of organic electronics, and in particular organic thin-film transistors, is the realization of stable, high-mobility, electrically-active organic materials that can enable low-cost solution-based processing methods. The development of viable solution-processable organic semiconductors helps make this possible. Consequently, understanding the materials properties of solution-processable organic semiconductors and how the processing conditions associated with device fabrication affect device performance are key to realizing low-cost organic electronics. In this work, we focused on understanding the processing-structure-property relationships of a solution-processable organic semiconductor, triethylsilylethylnyl anthradithiophene (TES ADT). Specifically, we demonstrated how a solvent-vapor annealing process can induce the crystallization of TES ADT post device processing. Bottom-contact thin-film transistors

with annealed TES ADT routinely exhibit an average charge-carrier mobility of 0.1 cm^2/V-s, which is sufficient to drive backplane circuitry in flexible display applications.

Additionally, we demonstrated that the manner in which source and drain electrodes are defined significantly affects the performance of the resulting TES ADT thin-film transistors. Specifically, the yield of functioning top-contact TES ADT thin-film transistors with electrodes defined by evaporation through a shadow mask directly on the organic semiconductor is low, and of the functioning devices, the charge-carrier mobility varies significantly (0.01 – 0.1 cm^2/V-s). In comparison, top-contact TES ADT thin-film transistors with electrodes defined separately and then laminated against the organic semiconductors have high yield and high charge-carrier mobility (0.2 ± 0.06 cm^2/V-s). This result emphasizes the importance of adapting existing or developing new thin-film transistor fabrication techniques to overcome the materials limitations of organic semiconductors. Along the same vein, we also demonstrated an elastomeric stamp-based, solventless printing process, nanotransfer printing (nTP), for the additive patterning of copper electrodes and interconnects of feature sizes 1 – 500 μm. These printed copper patterns differ from similarly printed gold patterns in that they are not electrically conductive. Leaching the elastomeric stamps in hot toluene prior to printing, however, allowed us to routinely print conductive copper features with an average resistivity of 31 μΩ-cm.

Another aspect of thin-film transistor fabrication that is crucial for optimal device performance (i.e., low off currents and low leakage currents) is the patterning and isolation of the organic semiconductor between neighboring devices. We demonstrated

two novel techniques for patterning TES ADT. The first technique utilizes UV light in the presence of dichloroethane vapors to *simultaneously* pattern and crystallize TES ADT. TES ADT thin-film transistors patterned with this technique exhibit high charge-carrier mobility (0.1 cm^2/V-s) and low off currents (10^{-11} A). The second patterning technique uses a PDMS stamp to selectively remove TES ADT from the non-channel regions of the thin-film transistor. This technique can be used to pattern both as-spun and crystalline TES ADT thin films. Crystalline TES ADT thin-film transistors patterned with this technique exhibit an average charge-carrier mobility of 0.2 cm^2/V-s and low off currents on the order of 10^{-11} A, while amorphous TES ADT thin films that are first patterned and then crystallized exhibit an average charge-carrier mobility of 0.1 cm^2/V-s and off currents on the order of 10^{-10} A.

Table of Contents

List of Tables

List of Figures

List of Illustrations

Chapter 1: Introduction and Background

Over the last several decades, a new trend in electronics research, namely, organic electronics, has emerged. Organic electronics refers to devices made with electrically-active materials that are carbon based, such as conducting and semiconducting polymers and smaller conducting and semiconducting organic molecules.[1] The interest in organic electronics stems from the promise of low-cost, large-area flexible electronics.[2] Organic electronics are not expected to compete with the more conventional semiconductor technology because the switching speeds of devices made with organic electrically-active materials is several orders of magnitude less than devices based on silicon, germanium or gallium arsenide.[3] Rather, organic electrically-active materials are promising for specialty applications, such as flexible displays,[4-6] organic light-emitting diodes,[7] organic photovoltaic cells,[8-11] wearable electronics,[12] sensors,[13] and radio-frequency identification tags.[14] As indicated by the list of potential organic electronic device applications, the development of electrically-active organic materials spans several classes of organic materials, from photoluminescent materials to electrically-conducting and electrically-semiconducting materials. This dissertation will solely focus on understanding the processing-structure-property relationships of solution-processable organic semiconductors for thin-film transistor applications.

For organic semiconductors to be commercially relevant in thin-film transistors applications, such as backplane circuitry to drive flexible displays[5] and electronic papers,[15] the devices containing the organic materials of interest must exhibit electrical properties comparable to those of amorphous silicon devices,[16, 17] i.e., a charge-carrier mobility of 0.1 – 1 $cm^2/V\text{-}s$, an on/off current ratio $\geq 10^4$, a threshold voltage close to zero that does not shift under normal operating conditions.[18] Further, the organic

semiconductor should be stable at ambient conditions.[18] Devices with several organic semiconductors, such as pentacene[19-26]and rubrene[27] exhibit charge-carrier mobilities within, or even exceeding, this range have been realized. The environmental stability and processability of organic semiconductors, however, are still of concern. In organic semiconductors, the molecules are held together by van der Waals forces, which are much weaker than the covalent bonds that typically exist in single-crystal, inorganic semiconductors.[2] As a consequence, organic semiconductors tend to be prone to oxidation and degradation at ambient conditions. While encapsulation[28] has been shown to greatly suppress this chemical fragility, the development of organic semiconductors that are environmentally stable remains an active area of research. Specifically, this dissertation will show that the stability of small-molecule organic semiconductors can be improved through the incorporation of substituent groups that also impart solution processability.

Low-cost processing and processibility of organic materials are additional concerns associated with organic semiconductors. If organic thin-film transistors are to be commercially realized, it is essential to develop low-cost fabrication methods to compensate for the high production costs of organic semiconductors stemming from complex, multi-step syntheses and purification processes.[29] Ideally, these low-cost processing methods should yield highly-ordered organic semiconductor thin films as device performance (i.e., high charge-carrier mobility and high on/off current ratio) is greatly influenced by the molecular structure and morphology of the organic semiconductor thin film.[30] To achieve high charge-carrier mobility in devices, the organic semiconductor should adopt an orientation which maximizes the π-π stacking between adjacent molecules. Further, the π-π stacking direction between molecules should be arranged in the same direction as the current flow.[30] Additionally, larger grain

sizes tend to give better mobilities.[31] The deposition conditions should therefore be optimized to yield organic semiconductor thin films with a high degree of molecular ordering and large grains. Generally speaking, there are two methods for depositing organic semiconductors: vapor deposition and solution deposition. Vapor deposition involves heating the organic semiconductor with a resistive heating source in a high vacuum environment (typically 10^{-6} – 10^{-8} Torr). Several organic semiconductors, such as pentacene,[32-36] tetracene,[37, 38] metallophthalocyanines[31, 39] and oligothiophene derivatives,[40-42] can be deposited by vapor deposition. Currently, the highest reported charge-carrier mobility for organic thin-film transistors (5 cm^2/V-s) uses a vapor deposited pentacene thin film.[43] The advantage of vapor deposition is that vapor deposition generally forms uniform, highly-ordered, organic semiconductor thin films with good reproducibility from run-to-run.[30] The degree of crystallinity and the morphology of the vapor deposited thin films – which ultimately dictates thin-film transistor device performance – can be tweaked by controlling the deposition rate and substrate temperature during vapor deposition.[30] The biggest limitations of vapor deposition are high materials consumption and long pump down cycles. The substrate size is also limited by the size of the vacuum chamber, so only a small footprint can be processed at a time (typically $\leq$ 6 in x 6 in). Further, the vacuum deposition system requires a high initial capital investment.[30]

The alternative to vapor deposition is solution deposition. Low-cost solution deposition methods, such as spin casting,[44-47] drop casting,[48, 49] and a variety of printing techniques, such as screen printing,[42, 50] ink-jet printing[51-54] and direct printing from a stamp,[28, 55-59]are well-suited for large-area deposition. The attributes of solution processing thus drive the active research on solution-processable organic semiconductors. Yet, there remain several key challenges associated with realizing solution-processable

organic semiconductors. For example, many small-molecule organic semiconductors, like pentacene, are not soluble in organic solvents. To get around this challenge, three approaches have been used to obtain soluble organic semiconductors: the development of soluble polymer organic semiconductors,[39, 60, 61] the development of soluble small-molecule organic semiconductor precursors that can be subsequently converted to its electrically-active counterpart post device processing,[62-65] and the development of soluble small-molecule organic semiconductors that are electrically active as deposited.[66-69]

Polymers typically have good film forming properties, which make them attractive candidates for solution processing. Polymer semiconductor thin films can be amorphous or semicrystalline. Polymers that are completely amorphous[70-73] provide a uniform path for charge transport that results in very stable device performance (i.e., low threshold voltage shifts under operating conditions and unvarying charge-carrier mobility across the chip).[74] The amorphous nature of the polymer semiconductor thin film, however, limits the maximum charge-carrier mobility in the resulting thin-film transistors to 10^{-3} to 10^{-2} cm^2/V-s.[72, 73, 75] To achieve polymer thin-film transistors with high charge-carrier mobility ($\geq$ 0.1 cm^2/V-s) requires polymer semiconductors that are semicrystalline[76] or liquid-crystalline.[61] The quintessential semicrystalline polymer semiconductor is regioregular poly (3-hexylthiophene) (P3HT)[48, 77] which, with proper processing conditions, exhibits a charge-carrier mobility of 0.1 – 0.3 cm^2/V-s. The charge-carrier mobility of P3HT depends strongly on the degree of crystallinity,[78] regioregularity,[39, 77] and molecular weight[79] of the P3HT polymer. P3HT adopts a 2-D anisotropic semicrystalline lamellar microstructure with strong π-π interchain interactions separated by a layer of insulating side chains. This lamellar microstructure thus leads to fast in-plane charge transport.[76] Studies of high molecular weight P3HT thin films indicate that higher degrees of crystallinity generally result in P3HT thin-film transistors

with higher charge-carrier mobility.[78] The charge-carrier mobility of P3HT has also been shown to increase with increasing degrees of regioregularity[76] and increasing molecular weight.[79, 80] Higher molecular weight samples of P3HT tend to have larger grains and hence fewer grain boundaries that limit charge transport in the resulting thin-film transistors. The charge-carrier mobility of polymer semiconductors can be further improved by modifying the gate dielectric surface with hydrophobic self-assembled monolayers (SAMs). It is believed that the SAM plays one of two roles. The SAM lowers the surface energy of the dielectric surface by removing residual surface moisture and other polar groups thus promoting phase segregation of the polymer at the dielectric-semiconductor interface.[77] The SAM can also induce microstructural changes in the polymer thin film through specific interactions between the SAM headgroup and the functional groups of the polymers, i.e., the orientation of P3HT molecules with respect to the dielectric surface can be parallel or perpendicular depending on whether the dielectric is treated with a $–CH_3$ terminated SAM or a $–NH_2$ terminated SAM, respectively.[81]

Although P3HT thin-film transistors shows high charge-carrier mobility, these transistors are susceptible to large threshold voltage shifts when operated in air because P3HT forms a reversible charge-transfer complex with oxygen.[82, 83] In the presence of both UV light and oxygen, P3HT is susceptible to photooxidation, which results in a loss of conjugation length along the polymer chain. Consequently, the charge-carrier mobility degrades in the resulting thin-film transistors.[84] The environmental and operational stability of P3HT can be improved by incorporating partially conjugated co-monomers into the polymer backbone.[85] Incorporating the comonomers can disrupt the delocalization of the π electron system by preventing the neighboring coupled monomer units from forming an extended conjugated pathway and hence reducing the susceptibility of P3HT to photooxidation. The planar backbone conformation of

individual polymer molecules is, however, conserved thus preserving the close π-π intermolecular distance that enables high charge-carrier mobility along the polymer chain.[85] The derivative P3HT polymer will still self-assemble into semicrystalline lamellar microstructures, and charge-carrier mobilities up to 0.15 cm^2/V-s are achieved in air in the resulting short channel (3 – 5 μm) thin-film transistors.[85] Another approach for reducing the oxidative potential of P3HT is to strategically substitute long alkyl side-chains on the polymer backbone to disrupt some of the extended π-conjugation. The large alkyl side chains also cause the polymer chains to self-assemble into lamellar structures with 3-D π-stacking.[46] Since these derivative P3HT polymers maintain their semicrystalline lamellar micorostructures, the charge-carrier mobility is not affected by the chemical modification (0.1 – 0.3 cm^2/V-s), even when the transistors are operated at ambient conditions.[46]

While polymer semiconductors, such as P3HT[39, 77, 82] and polythiophene derivatives,[46, 60, 86-88] show promise for organic electronics, the charge-carrier mobility of polymer semiconductors will always be limited by the morphology of the polymer semiconductor thin films. Due to polymer chain entanglements, it is impossible to achieve completely crystalline polymer semiconductor thin films. These entanglements kinetically hinder crystallization; the resulting thin films will thus always contain amorphous regions, as well as crystalline regions with grain boundaries and defects that act as charge traps. Consequently, polymer semiconductors will always exhibit a lower charge-carrier mobility compared to solution-processable, small-molecule organic semiconductors. For example, the highest charge-carrier mobility achieved with polymer thin-film transistors is 0.2 – 0.6 cm^2/V-s from polythiophene derivatives[87-89] while the highest charge-carrier mobility achieved with solution-processable small-molecule organic thin-film transistors is 1.8 cm^2/V-s from triisopropylsilyl pentacene.[49] Solution-

processable small-molecule organic semiconductors can exhibit superior charge-carrier mobility because they tend to form highly-crystalline thin films under appropriate processing conditions.[90]

The realization of solution-processable, small-molecule organic semiconductors can be achieved with soluble organic semiconductor prescursors or with soluble organic semiconductors. Many of the soluble small-molecule organic semiconductor precursors that have been developed are pentacene precursors[62, 63, 65] because pentacene devices have been routinely shown to exhibit charge-carrier mobility > 1cm^2/V-s[20, 21] in vapor-deposited thin-film transistors. Pentacene, however, is insoluble in organic solvents. Chemically modifying pentacene through the addition of side groups, such as dienophiles, yields an adduct that is soluble in organic solvents.[63] Pentacene precursors, however, require subsequent thermal[62, 63, 91] or chemical[65] conversion post deposition to convert the precursor molecules to electrically-active pentacene. The most promising results have been obtained from pentacene precursors that utilize Diels-Alder adduct chemistry with N-sulfinyl[63] or tetrachlorobenzene[62] leaving groups substituted on the center phenyl ring of pentacene. Both of these precursor compounds can be converted to electrically-active pentacene with a thermal annealing step at temperatures ranging from 130 – 200˚C. Higher annealing temperatures (200˚C) yield pentacene thin-film transistors with charge-carrier mobilities as high as 0.9 cm^2/V-s.[63] This charge-carrier mobility is slightly lower compared to thin-film transistors with vapor deposited pentacene films because defects or imperfect ordering introduced during spin coating of the small-molecule organic semiconductor precursor are not completely eliminated during the thermal annealing step.[62] In addition to lower charge-carrier mobility, there are other drawbacks associated with soluble small-molecule organic semiconductor precursors. The conversion temperature required for achieving high charge-carrier

mobility thin-film transistors may not be compatible with low-cost plastic substrates, and the additional conversion step can be time consuming.[30] Solution-processable small-molecule organic semiconductors that are electrically-active immediately after deposition are thus desired.

To date, the most promising route for realizing solution-processable small-molecule organic semiconductors that do not require thermal or chemical conversion post deposition to render electrical activity involves the incorporation of bulky substituents, such as alkynes, on the aromatic backbone of acenes[66, 69, 92, 93] and acenedithiophenes.[68, 69] These susbstituents not only impart solubility to the small-molecule organic semiconductor, but they also increase the stability of the molecules at ambient conditions, and affect how the molecule orders/crystallizes in the resulting thin film. Varying the size and position of the substituent thus provides a method of controlling the crystallization and subsequent packing of the molecules. It has been shown that the crystal packing of organic semiconductors has a dramatic effect on the electrical properties of organic semiconductors.[90] Generally, as the degree of π-stacking increases in the organic semiconductor thin film, the charge-carrier mobility of the resulting thin-film transistor also increases.[94] For example, substituting triisopropyl silyl groups on the center phenyl ring of pentacene yields a solution-processable pentacene derivative, TIPS pentacene, that forms highly-crystalline thin films when drop cast from solution.[49, 66] Thin-film transistors utilizing drop-cast TIPS pentacene exhibit a charge-carrier mobility of 1.8 cm^2/V-s.[49] Similarly, placing triethyl silyl groups on the center phenyl ring of anthradithiophene yields a solution-processable anthradithiophene derivative, triethylsilylethylnyl anthradithiophene (TES ADT), that also adopts a highly-crystalline thin film morphology when cast from solution.[68, 69] Thin-film transistors with blade cast TES ADT exhibit a charge-carrier mobility of 1 cm^2/V-s.[69] Both TIPS pentacene and

TES ADT adopt a 2-D crystal packing with 2-D face-to-face π-stacking interactions.[94] In contrast, solution-processable organic semiconductors that adopt 1-D π-stacking, such as triethylsilylethynyl pentacene[94] and n-propylsilylethynyl pentacene[94] exhibit charge-carrier mobility on the order of 10^{-3} cm^2/V-s or less.[94] To date, only solution-processable small-molecule organic semiconductors that adopt a 2-D crystal packing with 2-D π-stacking interactions exhibit high charge-carrier mobilities (≥ 0.1 cm^2/V-s).[94]

Once solution-processable organic semiconductors that adopt 2-D crystal packing are identified, such as TIPS pentacene and TES ADT, it is important to develop solution processing methods for reproducibly generating well-ordered, crystalline thin films of these organic semiconductors. Unlike vapor deposition techniques, which easily form well-ordered semiconductor thin films,[34, 90] solution deposition often generates semicrystalline or even completely amorphous semiconductor thin films because the quality of these films is highly dependent on the solvent evaporation rate. Slower solvent evaporation rates allow the molecules more time to organize, generally yielding more ordered and more crystalline organic semiconductor thin films. Consequently, spin casting, a technique in which the solvent evaporates within the first few seconds of deposition, often generates amorphous organic semiconductor thin films as-cast. In order for spin casting to be utilized in fabricating organic devices, straightforward methods for inducing order in as-spun organic semiconductor thin films need to be developed. Thermal annealing, for example, can be used post-deposition to induce structural reorganization in as-spun organic semiconductor thin films.[30, 95] For example, the mobility of as-spun poly[5,5'-bis(3-alkyl-2-thienyl)-2,2'-bithiophene] can be improved from 0.004 to 0.09 cm^2/V-s with thermal annealing at 140˚C.[95] In Chapter 3, we demonstrate a simple solvent-vapor annealing process for crystallizing as-spun TES ADT thin films.[45] The results detailed in Chapter 3 suggest that we can manipulate the

structure and thereby the electrical properties of solution-processable organic semiconductors, through the advantageous selection of appropriate post-processing conditions.

Other solution deposition techniques, such as drop casting (analogous to ink-jet printing[51-54, 74, 96] where the solvent is allowed to evaporate slowly at ambient conditions), can be used to directly obtain crystalline organic semiconductor thin films because the solvent evaporation rate is greatly retarded (minutes to hours depending on the volatility of the solvent), thereby allowing crystallization to occur simultaneously. Organic thin-film transistors with drop-cast organic semiconductor thin films thus generally exhibit higher charge-carrier mobility compared to thin-film transistors with as-spun organic semiconductor films.[49] Drop casting, however, is not a suitable technique for generating continuous large-area organic semiconductor films as it is difficult to control the solvent evaporation rate over large areas. If the solvent evaporation rate is not well controlled, the morphology of the resulting organic semiconductor thin film will be structurally heterogeneous, which will in turn result in great variations in the performance of such devices.

Since the quality of the organic semiconductor film depends so heavily on the solvent evaporation rate, we observe a lot of variation in both the quality of the organic semiconductor thin film and the corresponding electrical properties of the resulting organic thin-film transistors with solution deposition techniques. To establish the relevance of the device characteristics reported throughout this dissertation, all values will be reported as representative averages over all batches of devices tested, along with the accompanying standard deviation.

In addition to the organic semiconductor deposition conditions, other factors related to device fabrication can also affect the performance of organic thin-film

transistors. Of particular importance is the manner in which electrical contact is established with organic semiconductors and the geometry of the thin-film transistors. Traditionally, electrical contacts and interconnects are patterned through a combination of photolithography,[97] lift-off,[98] and chemical mechanical polishing (CMP).[99-102] Often though, the solvents and processing conditions associated with these techniques are not compatible with organic semiconductors. For example, it is well documented that the solvents associated with photolithography can cause organic semiconductor thin films to degrade[103] or delaminate from the dielectric surface.[104] Consequently, conventional device fabrication technologies need to be adapted, or new fabrication technologies need to be developed, to overcome the inherent physical and chemical limitations of organic electrically-active materials.

The typical device architecture of thin-film transistors can be classified as either top- or bottom-contact depending on how the electrodes contact the organic semiconductor.[3, 105] Both transistor configurations are shown in Figure 1.1. Bottom-contact thin-film transistors (Figure 1.1a) – where the electrodes are pre-patterned prior to the deposition of organic semiconductor layer – are generally known to have poorer device characteristics compared to analogous devices fabricated in the top-contact geometry (Figure 1.1b) where the electrodes are directly deposited on top of the organic semiconductor.[3, 105] Such disparity in transistor performance is speculated to result from uniformity differences in the organic semiconductor thin films between the two transistor geometries.[3, 106] In the case of bottom-contact thin-film transistors, the organic semiconductor is simultaneously deposited on two different surfaces: the dielectric surface and on top of the electrodes (Figure 1.1a). Due to surface energy differences, the growth behavior of the organic semiconductor can change dramatically across the electrode-dielectric interface resulting in structural discontinuities in the organic

semiconductor thin film at this interface. The structural disorder at electrode-dielectric interface can hamper charge transfer, which can in turn limit device performance.[3, 106] In contrast, a uniform organic semiconductor thin film is first deposited on the gate dielectric in top-contact thin-film transistors. Electrodes are then defined directly on top of the uniform organic semiconductor layer. As a result, the grains are continuous across the charge injection and extraction interfaces. Top-contact thin-film transistors therefore are often preferred to maximize device performance.[107-109] Top-contact thin-film transistors are fabricated by layer-by-layer patterning techniques. The organic semiconductor and metal electrodes are sequentially deposited through shadow masks to define the active channel regions. While this technique allows high-performance organic thin-film transistors to be fabricated, these transistors are typically large, with channel lengths, L, limited by the resolution of the shadow mask (25-30μm).[30]

Smaller features are easily patterned using photolithography.[97] According to the 2005 International Technology Roadmap for Semiconductors (ITRS 2005), features as small as 70nm can be routinely patterned using photolithography.[110] Combining photolithography with lift-off[98, 111] provides an effective method for fabricating the source and drain electrodes for organic thin-film transistors. Photolithography, however, is rarely used to define the organic semiconductor layer or the electrodes in top-contact thin-film transistors due to the chemical incompatibility between organic semiconductors and photoresist and the accompanying solvents, as discussed previously.[103, 104] As a consequence, photolithography is typically limited to patterning electrodes in bottom-contact thin-film transistors prior to organic semiconductor deposition. To achieve top-contact thin-film transistors with channel lengths smaller than 25 – 30 μm, non-traditional patterning techniques are required. An example of such a technique is soft-contact lamination (ScL).[28, 57] ScL effectively separates the deposition of the organic

semiconductor from the patterning steps required to define the source and drain electrodes of the transistor. Specifically, the organic semiconductor is deposited independently on one substrate (which already contains the pre-patterned gate and gate dielectric), while the source and drain electrodes are patterned on a separate, conformable substrate. The two substrates that contain the electrically-active components are then brought together and laminated to establish electrical contact. Since the source and drain electrodes are fabricated on an independent substrate, photolithography can be used to define the channel dimensions of the thin-film transistor, allowing small-channel, top-contact transistors ($L < 30$ μm) to be realized. Typically the conformable substrate on which the source and drain electrodes are defined is crosslinked poly(dimethylsiloxane) (PDMS). PDMS is chosen because of its mechanical properties, which allow molecular contact to be established between the PDMS and the substrate containing the organic semiconductor thin film when they are laminated.[28] The laminated electrodes can be peeled from the organic semiconductor thin film without damage to the organic semiconductor film. Consequently, several source and drain electrode pairs with varying channel dimensions can be laminated against the same organic semiconductor film to determine the thin-film transistor performance as a function of channel length.[112] Additionally, contacts formed by lamination can exhibit lower contact resistance between the electrode and the organic semiconductor layer than contacts formed by directly evaporating gold on top of the semiconducting layer.[113] In combination, these effects demonstrate that ScL is an extremely effective method for non-destructively fabricating high-performance, small-channel, top-contact organic thin-film transistors. We will further illustrate the versatility of ScL for fabricating top-contact, TES ADT thin-film transistors in Chapter 4.

As just discussed, non-traditional patterning techniques, such as ScL, are extremely useful for defining metal contacts and interconnects in organic devices because these techniques have been developed to accommodate the unique materials properties of organic semiconductors. Another non-traditional patterning technique that warrants discussion is nanotransfer printing, nTP.[56, 114-118] Nanotransfer printing is a solventless, additive, contact printing technique that exploits interfacial chemistry to transfer metal features from a stamp (either a PDMS stamp, or a hard stamp, such as GaAs) to both conformal and rigid substrates.[56] Features as small as 1 – 5 μm can be patterned by nTP with elastomeric stamps while, features as small as 75 nm can be patterned by nTP with rigid stamps.[117] The effectiveness of nTP for patterning gold electrodes and interconnects has been demonstrated with pentacene thin-film transistors and pentacene and hexadecafluorophthalocyanine complimentary inverter circuits.[56] The electrical performance of both the pentacene thin-film transistors (charge-carrier mobility of 0.1 cm^2/V-s) and the complementary inverter circuits was comparable to larger-scale devices in which the gold electrodes and interconnects had been deposited through a shadow mask.[56] Copper, however, is the more relevant metal for current-day electronic applications because of its low resistivity and low tendency for electromigration.[119-121] In Chapter 5 we demonstrate nTP for additively patterning copper electrodes and interconnects.

Beyond patterning the electrical contacts, patterning and isolating the organic semiconductor thin film between adjacent devices is critical for obtaining high-performance organic thin-film transistors. Solution deposition techniques, such as spin casting and drop casing, indiscriminately deposit organic semiconductor across the substrate. Since the charge carriers are not confined to the channel region of the thin-film transistors, these transistors often exhibit high off currents (or low on/off current ratios,

~10^3), parasitic leakage currents (non-zero source-drain currents at zero applied bias), and they also suffer from electrical cross talk between transistors within the same array.[5, 122] Patterning the organic semiconductor is thus necessary to confine the charge carriers to the channel region. Currently, there are three techniques for patterning organic semiconductors: a derivative of photolithography where the organic semiconductor is protected by a barrier layer in the regions of interest,[97] shadow masking,[123] and printing.[52, 53, 57, 58, 124-127]

The chemicals and solvents involved in photolithography can often damage the organic semiconductor resulting in chemical degradation or delamination.[103, 104] As such, the organic semiconductor in the region of interest needs to be protected by a barrier layer if photolithography is to be successfully used to pattern organic semiconductors. In this derivative photolithography process, a water based poly(vinyl alcohol) polymer containing a chromium catalyst serves as the photoresist for patterning pentacene.[128] The photoexposed poly(vinyl alcohol) becomes water insoluble, allowing the unexposed poly(vinyl alchol) regions to be washed away with water. Water does not, however, cause the protected pentacene film to delaminate. The exposed pentacene film can then be removed with oxygen plasma.[30] Pentacene thin-film transistors patterned with this technique exhibited a charge-carrier mobility of 0.6 cm^2/V-s and an on/off current ratio of 10^5.[128] A second and more general photolithography technique for patterning the organic semiconductor is to create reentrant photoresist patterns on the substrate prior to depositing the organic semiconductor.[129] When the organic semiconductor is subsequently deposited, the semiconductor film breaks along the edge of the photoresist profile, resulting in regions of isolated organic semiconductor. Applying this patterning technique to pentacene thin-film transistors yielded pentacene inverters with large voltage

gains and submicron rise and fall time constants, and pentacene ring oscillators with sub-75-μs propogation delays.[129]

The use of shadow masks to pattern organic semiconductors is much more straightforward and eliminates exposing the organic semiconductor to harmful chemicals altogether. The organic semiconductor is deposited through a metal shadow mask to form the active channel region of the thin-film transistors.[123] There are, however, two significant limitations associated with shadow masks: as mentioned earlier in our discussion on patterning electrodes, the minimum feature size of metal shadow masks is limited to 25 – 30 μm.[30] Further, shadow masks cannot be used with solution-processable organic semiconductors because the shadow mask does not form a liquid-tight seal with the substrate. One recent exception to the minimum feature size limitation was demonstrated by Muyres and coworkers at 3M.[130] They fabricated a polymer shadow mask by laser ablation with 10 μm features. Using this polymer shadow mask they built radio-frequency identification circuitry.[19] These polymer shadow masks, however, are not commonly used because the precise multilayer alignment required to define the active components of organic devices is difficult to achieve with shadow masks.[30]

Perhaps the organic semiconductor patterning technique that stands to make the most impact on organic thin-film transistor fabrication is printing. Significant progress has been made recently in developing printing methods for all organic thin-film transistors.[53, 131, 132] Printing can be further broken down by specific techniques: screen printing,[42, 50, 133] ink-jet printing,[52-54, 96] microcontact printing,[126, 134, 135] and hot lift-off.[127] Several of the more traditional printing techniques, such as screen printing[42, 50, 133] and ink-jet printing,[52-54, 96] are already widely used on a commercial basis for printing silicon-based circuit boards,[136] text, and pictures with high resolution.[30, 137] Since the infrastructure already exists, there is financial motivation for modifying these printing

techniques for organic thin-film transistor fabrication.[30] Screen printing has been successfully adapted for plastic organic thin-film transistors in which all the components are printed.[50] The organic semiconductor, poly(3-alkylthiophene), was specially formulated so that it could be pushed through a screen mask to form the desired pattern on the substrate. The performance of the screen printed transistors with printed polyimide gate dielectric and source and drain electrodes printed from a conductive ink (479SS from Acheson Co.) was comparable to the performance of bottom-contact transistors built on a silicon/silicon dioxide platform with gold electrodes patterned by photolithography.[50] The biggest limitation of screen printing, however, is its resolution – the smallest feature that can be printed reproducibly is 75 μm due to ink spreading.[30]

Ink-jet printing[52-54, 96] is another printing technique that is readily adaptable for polymer organic thin-film transistor fabrication by replacing the traditional ink with specially-formulated polymer solutions.[30] Several all-polymer thin-film transistors have been fabricated with ink-jet printing.[52, 53] Thin-film transistors with ink-jet printed regioregular poly(thiophene) exhibited a charge-carrier mobility of 0.1 cm^2/V-s (which is identical to the charge-carrier mobility of thin-film transistors with spin-coated poly(thiophene)) and a high on/off current ratio of 10^6.[54] Typically, the resolution of ink-jet printing is around 25 μm unless surface patterning is utilized to limit ink spreading.[30] If a hydrophobic dewetting pattern is used to prevent ink spreading, the feature resolution can be reduced to 200 nm.[51] Arrays of poly(9,9'-dioctyl-fluorene-*co*-bithiophene) (F8T2) thin-film transistors (channel length = 500 nm, channel width = 80 μm) that use an underlying hydrophobic 1H, 1H, 2H, 2H-perfluorodecyltrichlorosilane dewetting pattern and printed poly(3,4-ethylenedioxythiophene)/poly(4-styrene sulphonate) (PEDOT/PSS) electrodes exhibited a charge-carrier mobility of 0.003 cm^2/V-s, and an on/off current ratio of 10^4.[51] The charge-carrier mobility is slighltly lower than F8T2 thin-film

transistors (channel length = 2 μm) with gold electrodes patterned by photolithography. The authors attribute this lower mobility to the low conductivity of the PEDTOT/PSS electrodes and short channel effects.[51]

While both screen printing and ink-jet printing are well-developed techniques that have been adapted for organic thin-film transistor fabrication, neither technique can provide the resolution (10 μm) needed for useful organic thin-film transistor circuits unless a high-resolution surface dewetting pattern is used.[30] Soft-lithography techniques, such as microcontact printing[126, 138] are able to provide the needed feature resolution down to a few microns or even tens of namometers.[134] For example, microcontact printing was recently used to directly pattern a solution-processable organic-inorganic semiconductor, $(C_6H_5C_2H_4NH_3)_2SnI_4$.[135] In this demonstration, microcontact printing was used to create a high-resolution hydrophilic-hydrophobic surface pattern (channel lengths of 6 – 100 μm). When the semiconductor is subsequently deposited by spin coating, the semiconductor only deposits on the hydrophilic regions. The charge-carrier mobility of the microcontact-printed transistors was 0.5 cm^2/V-s with an on/off current ratio of 10^5.[127]

Another printing technique that exists for patterning organic semiconductors is hot lift-off.[127] Unlike the previously discussed printing techniques, hot lift-off is a subtractive technique. A partially-cured, patterned epoxy stamp is pressed onto the organic semiconductor thin film and heated to promote adhesion between the epoxy stamp and the organic semiconductor in the regions of contact. Peeling the epoxy stamp removes the organic semiconductor from the substrate in the regions previously in contact with the epoxy stamp. A patterned semiconductor film is left behind. Vapor-deposited small-molecule organic semiconductor films of copper phthalocyanine, and metal-free phthalocyanine were patterned with this hot lift-off technique. Copper

phthalocyanine thin-film transistors patterned with the hot lift-off technique exhibited a charge-carrier mobility of 0.02 $cm^2/V\text{-}s$, which is typical of copper phthalocyanine thin-film transistors,[48] and an on/off current ratio of $10^4 - 10^5$.[127]

The preceding paragraphs illustrate that the techniques currently available for patterning organic semiconductor thin films are limited in their application. This is particularly true for solution-processable organic semiconductors in which the patterning must be completed in two steps. Often the materials properties of the organic semiconductors dictate that unique patterning techniques must be developed for a particular organic semiconductor. We will demonstrate two such techniques for patterning TES ADT in Chapter 6. One technique uses UV light in the presence of solvent vapors to simultaneous pattern and crystallize TES ADT. The second technique uses PDMS stamps to selectively remove TES ADT from the non-channel regions of the thin-film transistors.

In summary, there are many aspects of organic semiconductor materials design and thin-film transistor fabrication that must be controlled to yield high-performance organic devices. The materials properties of organic semiconductors can be tailored during the chemical synthesis to yield stable, solution-processable materials that form well-ordered thin films that exhibit high charge-carrier mobility when utilized in thin-film transistor applications. Additionally, the manner in which electrical contact is established to organic semiconductors can have a dramatic effect on the electrical properties of the resulting devices. It is therefore important to choose an appropriate technique for defining electrodes that is compatible with the organic semiconductor of interest, and one that meets the feature size requirements of the particular device application. Finally, it is also important to pattern the organic semiconductor. Patterning the organic semiconductor reduces parasistic leakage currents and electrical cross talk

between neighboring transistors. Elimination of leakage currents and optimization of on/off current ratios correspond to higher contrast between the on and off states of the transistor resulting in more efficient device operation.

FIGURES:

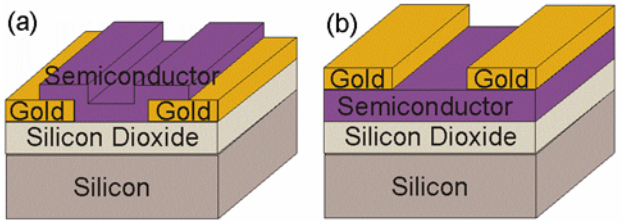

Figure 1.1. Schematic of organic thin-film transistors in (a) bottom-contact geometry and (b) top-contact geometry.

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Chapter 2: Experimental Techniques

ORGANIC THIN-FILM TRANSISTOR OPERATION AND FABRICATION:

Organic thin-film transistors can be fabricated in two device geometries, top-contact or bottom-contact. These device geometries are illustrated in Figure 1.1. Both top- and bottom-contact transistors are fabricated on a substrate with a gate electrode which is insulated from the other device components by a gate dielectric. In our experiments a highly-conductive, n-doped silicon wafer serves as the gate electrode. A thermally-grown silicon dioxide layer (100 or 300 nm) serves as the gate dielectric. In the top-contact geometry, the organic semiconductor is deposited directly on the dielectric surface, and electrodes are subsequently deposited on top of the organic semiconductor. In the bottom-contact geometry, the electrodes are patterned directly on the dielectric surface and the organic semiconductor is subsequently deposited on top of both the electrodes and on the exposed dielectric surface in the channel.

Organic thin-film transistors are three terminal devices that operate like switches; they are either "on" or "off" depending on whether a bias is applied to the gate. When a bias is not applied to the gate, the transistors are "off, and current does not flow from the source to the drain. Consequently, the organic semiconductor acts as an insulator. When a bias is applied to the gate, the organic semiconductor acts like a conductor and the dielectric acts like a capacitor causing charges to accumulate at the gate-dielectric and organic semiconductor-dielectric interfaces. For a p-type organic semiconductor (n-type), a negative (positive) bias is applied to the gate, resulting in negative (positive) charges at the gate-dielectric interface. Correspondingly, positive (negative) charges accumulate at the organic semiconductor-dielectric interface. These positive (negative) charges that accumulate at the organic semiconductor-dielectric interface form a charge

transport channel (which typically only extends 50 angstroms into the organic semiconductor[1]) in the organic semiconductor. Now when a bias is applied to the source, current flows from the source electrode to the drain electrode through the charge transport channel. Increasing the magnitude of the bias applied to gate increases the amount of charges that accumulate at the gate-dielectric and organic semiconductor-dielectric interfaces, resulting in higher current flow from the source to the drain.

The relevant parameters extracted from the current-voltage characteristics of thin-film transistors are the charge-carrier mobility (μ), the threshold voltage (V_T) and the on/off current ratio. The charge-carrier mobility is the most cited parameter. It is the drift velocity (cm/s) of the charge carrier (either holes (p-type) or electrons (n-type)) per unit applied field (V/cm). The charge-carrier mobility has units of cm^2/V-s. To effectively drive backplanes in flexible display applications, a charge-carrier mobility of 0.1 – 1 cm^2/V-s is desired.[2] The charge-carrier mobility can be extracted from equation 2.1, which is borrowed from established inorganic transistor theory:[3]

$$I_{SD} = \frac{W\mu C_i}{L}[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^{\ 2}}{2}] \qquad \text{Equation 2.1}$$

where I_{SD} is the source-drain current, W is the channel width, L is the channel length, μ is the charge-carrier mobility, C_i is the capacitance per unit area of the gate insulator, V_{GS} is the gate-source voltage, V_T is the threshold voltage and V_{DS} is the source-drain voltage. In the linear regime, $V_{DS} << (V_{GS} - V_T)$[3], and this equation can be simplified to:

$$I_{SD} = \frac{W\mu_{lin} C_i}{L}(V_{GS} - V_T)V_{DS} \qquad \text{Equation 2.2}$$

where μ_{lin} represents the charge-carrier mobility extracted from the linear regime of the current-voltage characteristics. When, $V_{DS} > (V_{GS} - V_T)$, equation 2.1 can be simplified to:

$$I_{SD} = \frac{W\mu_{sat} C_i}{2L}(V_{GS} - V_T)^2 \qquad \text{Equation 2.3}$$

where μ_{sat} represents the charge-carrier mobility extracted from the saturation regime of the current-voltage characteristics. Because I_{SD} is now independent of the source-drain voltage, this regime is also known as the saturation regime.[3] In this dissertation we report charge-carrier mobilities from the saturation regime. Typically, the charge-carrier mobility measured in the linear regime is slightly less than the charge-carrier mobility measured in the saturation regime because contact resistance at the source and drain electrodes can dominate at low source-drain voltages, limiting the number of charge-carriers injected into the transistor channel.[4] At higher source-drain voltages the channel resistance dominates so the saturation regime characteristics should better reflect the organic semiconductor properties. By collecting source-drain current-voltage measurements as a function of gate voltage (Figure 2.1a), and plotting $\sqrt{I_D}$ in the saturation regime versus V_{GS}, (Figure 2.1b) we can determine the slope of the fitted line and calculate the saturation charge-carrier mobility by solving for μ_{sat} in equation 2.3:

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_D}}{\partial V_{GS}}\right)^2$$

Equation 2.4

Typically, the measured current-voltage characteristics resemble those shown in Figure 2.1a. When the organic semiconductor thin film is amorphous, however, a significant amount of current-voltage hysteresis (the magnitude of the source-drain current varies depending on whether the source-drain voltage is swept from positive to negative values or from negative to positive values) can appear in the current-voltage measurements as shown in Figure 2.2.

The threshold voltage is the voltage at which the transistor turns from the "off" state to the "on" state, and it is a strong indicator of the quality of the interface between the organic semiconductor and the gate dielectric.[5] According to equation 2.3, the threshold voltage can be graphically determined from the x-intercept of the fitted line used to extract the charge-carrier mobility in the saturation regime. For backplane

circuitry applications the threshold voltage should be as close to zero as possible.[2] For a p-type (n-type) semiconductor, a negative (positive) threshold voltage will increase the power consumption of the device, because higher source-drain and gate biases are required to operate the device in the saturation regime. A positive (negative) threshold voltage indicates that the device is always on, even if a bias is not applied to the device. To turn the device off, a positive (negative) gate bias greater than the threshold voltage must be applied, which is also known as reverse biasing the device.[3] A non-zero threshold voltage is a reflection of the dielectric-organic semiconductor interface and can be affected by surface ions, moisture and dielectric surface treatments.[6, 7] The threshold voltage can also be increased by unintentional doping from impurities in the organic semiconductor.[8]

The on/off current ratio is the ratio of the source-drain current in the "on" state to the source-drain current "off" state. The purity of the organic semiconductor often affects the magnitude of the off currents.[5] Only high-purity materials yield transistors with low ($\leq 10^{-11}$ A) off currents. For backplane circuitry applications the on/off current ratio should be at least 10^4.[2] We calculate the on/off current ratio from a plot of the source-drain current as a function of gate voltage, which is also known as the transfer characteristics. A representative plot of the transfer characteristics is shown in Figure 2.3. The on/off current is calculated by dividing the source-drain current at V_G = -20 V (on current) by the source-drain current at V_G = 30 V (off current) at a constant source-drain voltage of -20 V.

We built organic thin-film transistors with solution-processable organic semiconductors obtained from Professor John Anthony's research group in the Department of Chemistry at the University of Kentucky. Top and bottom-contact thin-film transistors were fabricated on prime-grade, heavily-doped silicon wafers with 100 or

300 nm of thermally-grown oxide (Silicon Quest International or NOVA Electronics), which served as the gate and gate dielectric, respectively. In the bottom-contact geometry, the source and drain electrodes, consisting of a 2 – 5 nm titanium strike layer and 40 nm of gold, were patterned directly on the silicon dioxide surface via e-beam evaporation through a shadow mask. The channel lengths varied from 100 to 300 μm and channel widths varied from 1000 μm to 2000 μm. Following deposition of the source and drain electrodes, the patterned silicon substrate was either used as-is (Chapter 3) or sonicated in deionized water for three minutes and then placed in the UV/Ozone chamber for 5 – 20 minutes (Chapters 4 and 6). The surface treatment varied depending on the silicon wafer manufacturer. Wafers from Silicon Quest International were used as-is, while silicon wafers from NOVA Electronics required the water and UV/Ozone treatment to achieve high-quality thin-film transistors. The organic semiconductor, triethylsilylethylnyl anthradithiophene (TES ADT), was dissolved in toluene (Fisher Scientific) to form a 2 wt% solution, and deposited directly onto the patterned silicon platform by spin casting. The spin casting was executed at 1000 rpm for 60 sec. For experiments in Chapter 3 involving TES ADT derivatives, the derivative organic semiconductors were dissolved in solvent (toluene, chloroform and benzene (Fisher Scientific)) to form 0.5 – 1 wt% solutions. Solutions of TES ADT derivatives were deposited onto patterned silicon platforms by spin casting and drop casting. For drop casting, a few drops of the organic semiconductor solution were dropped onto the pre-patterned silicon platform. The solution-covered chip was then covered with a Petri dish lid to control the solvent evaporation rate so the organic semiconductor could crystallize. All of the fabricated thin-film transistors were then heated on a 90°C hot plate at ambient conditions to remove residual solvent, and tested to obtain the "as-cast" electrical characteristics. Prior to electrical characterization, individual organic thin-film

transistors were isolated from neighboring devices by scratching the organic semiconductor film in the non-channel regions with a razor blade.

After testing, spin-coated TES ADT devices were annealed in a solvent vapor environment for 2 to 10 minutes. All solvent-vapor annealing and electrical measurements were conducted in the dark at ambient conditions since TES ADT can be photosensitive.[5] The solvent vapor environment was created by pouring approximately 15 ml of dichloroethane (Aldrich) into the bottom of a glass Petri dish. The fabricated transistors were attached to the Petri dish lid and placed over the pool of solvent for a specified amount of time (typically 2 – 10 minutes). Solvents were used as-purchased. After solvent-vapor annealing, the TES ADT thin-film transistors were retested to obtain the "annealed" electrical characteristics.

In the top-contact transistor geometry, TES ADT was deposited directly on the silicon dioxide surface. Prior to TES ADT deposition, the silicon substrate was sonicated in deionized water for 3 minutes and placed in a UV/Ozone chamber for 10 minutes. The TES ADT solution (2 wt% in toluene) was spin coated on the UV/Ozone-cleaned silicon at 1000 rpm for 60 sec and then baked on a 90ºC hot plate to remove residual solvent. The TES ADT film was then annealed over 15 ml of 1,2-dichloroethane in a Petri dish until the TES ADT film crystallized (typically 2 – 15 minutes). Gold source and drain electrodes were then deposited on top of TES ADT through a shadow mask by e-beam evaporation. The evaporation rate of gold was either 1 angstrom/sec or 10 angstrom/sec. Prior to electrical characterization, individual TES ADT thin-film transistors were isolated from neighboring devices by scratching through the TES ADT film in the non-channel regions of the transistors with a razor blade.

SILICON MASTER FABRICATION FOR PDMS STAMP FABRICATION:

Silicon masters were used to create PDMS stamps for top-contact thin-film transistors by lamination (Chapter 4) and for nanotransfer printing (Chapter 5). We created the silicon masters from silicon test wafers (Wafer World, p-type, 1 – 20 Ω-cm resistivity). Prior to patterning, the silicon wafer was thoroughly cleaned in a piranha solution (70% H_2SO_4, 30% H_2O_2 at 70 – 80˚C) for 10 minutes followed by 3 minutes of sonication in acetone and isopropanol. The cleaned silicon substrate was dried under a stream of nitrogen and then dehydrated on a 160˚C hot plate for 10 minutes. After allowing the silicon wafer to cool to room temperature, Omni coat adhesion promoter & release agent (MicroChem Corporation) was spin coated on the silicon wafer and baked at 200˚for 5 minutes. SU8-2025 photoresist (MicroChem Corporation) was then spin coated on top of the Omni coat layer and baked at 90˚C for 10 minutes. The photoresist was then exposed for 40 seconds (10 mW/cm^2) with a 365 nm flood source (ABM Inc., 2105C2 Illuminator Controller) through a metal mask. Following pattern development in propylene glycol methyl ether acetate (PGMEA; Alfa Aesar), the exposed regions of the silicon wafer were etched with SF_6 at 100 mTorr and 300 W for 30 minutes in a March Plasma CS1701F Reactive Ion Etcher to create 15 μm recessed regions in the silicon wafer. The SU8-2025 photoresist was then removed by soaking the silicon substrate in N-methylpyrrolidone (NMP; Aldrich) for 10 minutes followed by a fresh piranha solution for 20 minutes. During these cleaning procedures, the Omni Coat adhesion promoter and release agent dissolves causing the SU8-2025 photoresist to lift-off the silicon substrate. The patterned silicon master was then descummed for 5 minutes in a UV/Ozone chamber and treated with (tridecafluoro-1,1,2,2-tetrahydroctyl) trichlorosilane (F-SAM; Gelest, Inc.)[9] to make the silicon surface non-stick. The resulting silicon master contained raised

source and drain electrode features with 15 μm deep trenches between the source and drain electrode pairs, as shown in Figure 2.4.

PDMS STAMP AND PDMS MASTER FABRICATION:

PDMS stamps for fabricating top-contact TES ADT thin-film transistors by lamination (Chapter 4) and for nanotransfer printing (Chapter 5) are fabricated from Dow Corning's Sylgard 184 poly(dimethylsiloxane) (PDMS) formulation.[10] Sylgard 184 is a two component system that consists of a PDMS prepolymer and a crosslinker. The prepolymer and crosslinker are mixed in a 10:1 (w:w) ratio and degassed. PDMS stamps are fabricated by casting the PDMS prepolymer mixture against the F-SAM-treated silicon master (Figure 2.4). After curing the prepolymer mixture overnight at room temperature or at 60°C for 2 hrs, the PDMS is peeled from the master. The PDMS stamp has the negative image of the master. A stamp with the positive image can also be fabricated by using the previously generated PDMS stamp (with the negative image) as a master. To ensure that the second-generation PDMS stamp releases effectively, the PDMS master was also treated with FSAM before casting.

SOFT-CONTACT LAMINATION FOR TOP-CONTACT THIN-FILM TRANSISTORS:

In soft-contact lamination,[11, 12] the source and drain electrodes are patterned on a PDMS stamp independent of the transistor platform. The PDMS stamp containing source and drain electrode features is placed in a UV/Ozone chamber for 8 minutes to activate the surface of the PDMS stamp with –OH groups. Subsequently, 2 nm of titanium and 15 nm of gold were deposited on the raised and recessed regions of the PDMS stamp. The titanium promotes the adhesion of gold to the activated PDMS stamp. Separately, TES ADT was deposited and annealed on a silicon/silicon dioxide substrate as described

previously. Gold contact pads (40 nm) were subsequently deposited around the exterior of the annealed TES ADT film by e-beam evaporation. A 5nm titanium layer was used to adhere the gold contact pads to the silicon substrate. The annealed TES ADT film was protected during the titanium and gold evaporations to prevent damage. Laminating the PDMS stamp with freshly-evaporated gold against the silicon/silicon dioxide substrate with annealed TES ADT completes the circuit, as illustrated in Figure 2.5. The recessed regions of the PDMS stamp serve as the channels of the resulting thin-film transistors. While laminating the PDMS-supported gold electrodes against the TES ADT film, it was important to ensure that the source and drain electrodes contacted both the TES ADT film and the gold contact pads surrounding the TES ADT film. During I-V characterization, the test probes were contacted against the gold contact pads rather than the source and drain electrodes on the PDMS stamp for ease of measurement.

I-V CHARACTERIZATION:

An Agilent 4156C Precision Semiconductor Parameter Analyzer was used to make all electrical measurements. For organic thin-film transistor characterization, 3-probes were contacted to the gate, source, and drain electrodes, respectively. A constant bias was applied to the gate electrode (0 to -20 V in -4V steps), while the bias applied to the source electrode was swept from +4 V to -30V and back to +4 V in 2 V increments. The resulting source-drain current was measured as a function of increasing gate voltage. These current-voltage measurements (Figures 2.1a and 2.2) were used to quantify the charge-carrier mobility and threshold voltage for each thin-film transistor (Chapters 3, 5, 6), as described above. The transfer characteristics used to calculate on/off current ratio were collected by applying a constant bias to the source electrode (-20 V) while the gate bias was swept from 20 V to -30 V and back to 20 V in 2 V increments. Again, the resulting source-drain current was measured (Figure 2.3).

To determine the resistivity of printed copper wires, we used 2 probes to measure the resistance of the copper lines as a function of wire length (Chapter 5). The voltage was swept from +5 V to -5V in 0.25 V increments, and the resulting current was measured. Using ohm's law, we can calculate the resistance, R, along the wire.

$$R = \frac{I}{V}$$ Equation 2.5

By plotting the resistance as a function of wire length, we can calculate the slope and determine the resisivity, ρ, of the printed copper from equation 2.6:

$$\rho = \frac{R}{LA}$$ Equation 2.6

where L is the length of the copper line and A is the cross-sectional area of the copper line.

ATOMIC FORCE MICROSCOPY (AFM):

A Digital Instruments Dimension 3100 Multimode AFM was used to perform several surface characterization experiments. Surface morphology and root-mean-squared (rms) roughness of TES ADT thin films and printed copper features were collected in tapping mode. Standard tapping tips (Nano Devices Metrology Probes) with a resonant frequency of 150 kHz and a spring constant of 5 N/m were used to collect topography images.

Conductive-Probe AFM (C-AFM):

A second AFM experiment, conductive-probe AFM (C-AFM), was used to characterize the through-plane conductivity of printed copper patterns (Chapter 5). As shown in Figure 2.6, the copper feature was printed onto a conductive substrate, such as gold. An electrical contact was made from the gold substrate to the conductive metal

base plate of the AFM using conductive silver paint (SPI Supplies). A bias (0 to -50 mV) was applied to the base plate and the resulting current (0 to 200 pA) was measured through the printed copper feature at the AFM tip. A conductive, platinum-coated AFM tip was used for these measurements (Mikro Masch CSC11/Ti-Pt/15). During the C-AFM measurements, the AFM was operated in contact mode. Height and conductivity images were collected simultaneously.

Scanning Surface Potential Microscopy (SSPM):

Additionally, a third AFM experiment, scanning surface potential microscopy (SSPM),[13] was used to measure the surface potential across the length of the channel in TES ADT thin-film transistors during operation. With this technique, the conductive AFM tip (MikroMasch NSC15/Ti-Pt) scanned the surface twice. On the first pass, the microscope was operated in tapping mode to acquire the surface topography. On retracing the topography, the tip was raised off the surface (10 nm) and an AC electric field was applied at the resonance frequency of the tip. A feed back loop was used to measure and null the phase shift between the tip and the surface by adding a DC bias.[14] In the surface potential mode, we collected the contact potential difference between the tip and the surface. All scans were conducted in a nitrogen environment. The topography images were collected with the source, drain and gate electrodes grounded, while the surface potential images were collected while operating the transistor in the linear regime. An external power source supplied the source-drain and gate voltages to power the device. A bias of -2 V was applied to the drain while the gate bias was stepped from 0 V to -20 V in -4 V increments. We collected surface potential data in the linear regime because this is the regime where the contact resistance can dominate.[13] These SSPM experiments were performed in collaboration with Timothy J. Smith and Professor

Keith Stevenson in the Department of Chemistry and Biochemistry at the University of Texas at Austin.

DIFFERENTIAL SCANNING CALORIMETRY (DSC):

A Perkin Elmer DSC 7 was used to characterize the TES ADT family of solution-processable organic semiconductors. We were interested in identifying crystallization temperatures and phase transitions for each of the organic semiconductors examined, if they existed. Typically, the organic semiconductors (2 – 10 mg) were heated from 50 – 200˚C at 10˚C/min. For quantitative analysis, the specimen was heated again; only data from the second heat scan was reported. Before scanning the actual molecules, a baseline with a similar empty pan was collected using the same heating rate. If an organic semiconductor exhibited a thermal transition, controlled cooling experiments were also conducted to determine the crystallization temperature. Cooling rates varied from 1 – 5˚C/min.

X-RAY PHOTOELECTRON SPECTROSCOPY (XPS):

X-ray photoelectron spectroscopy (XPS) analysis was performed in Dr. M. White's laboratories in the Department of Chemistry with a Physical Electronics ESCA 5700 spectrophotometer equipped with a monochromatic Al Kα X-ray source, a hemispherical electron analyzer and a low energy electron flood gun for charge compensation of insulating samples. Samples were introduced through a preparation chamber before being transferred into the analysis chamber at $2x10^{-10}$ Torr. The samples were typically analyzed at a takeoff angle of 45°C defined as the angle between the sample and the detector. All spectra were collected at a pass energy of 11eV. The survey scan spectra were acquired from 0 to 1200eV to qualitatively identify peaks. High-

resolution scans were then collected to quantitatively identify specific binding environments. For depth profiling analysis, an argon ion beam was used to etch the sample. The etch rate (7.2 nm/min) is linear and controlled by the sample current. Etching proceeds until the intensity of the peak of was reduced to 25% of its maximum value. Data analysis consisted of fitting and subtracting a linear baseline from each high-resolution elemental spectrum, and then numerically integrating each baseline-subtracted peak. The integrated area was then corrected by the appropriate sensitivity factor for each element. To compare samples, the integrated peak intensities were normalized by the integrated peak intensity of a common reference peak such as C 1s or Cu 2p.

SCANNING ELECTRON MICROSCOPY (SEM):

A LEO 1530 SEM with low operating voltage capabilities and an in-lens annular detector was used to characterize the feature size and edge resolution of printed copper patterns. SEM images of printed copper features were collected at a working voltage of 10 kV and working distance of 6 mm. The low operating voltage capabilities of the LEO system permitted us to image poly(dimethylsiloxane) (PDMS) polymers non-destructively. PDMS stamps were coated with approximately 10 nm of chrome/gold to make the surface conductive before loading the sample into the SEM chamber. SEM images of PDMS stamps were collected at a working voltage of 1 kV and a working distance of 4 mm. TES ADT was not imaged by SEM because even low working voltages (1 kV) caused TES ADT to dewet from the silicon substrate.

OPTICAL MICROSCOPY:

An Eclipse ME 600L Nikon Metallurgical Microscope equipped with episcopic differential interference contrast (DIC) and a Nomarski prism was used to characterize the morphology and grain size of TES ADT thin films. All optical microscope images were collected at ambient conditions with a digital camera (Nikon DXM 1200).

FIGURES:

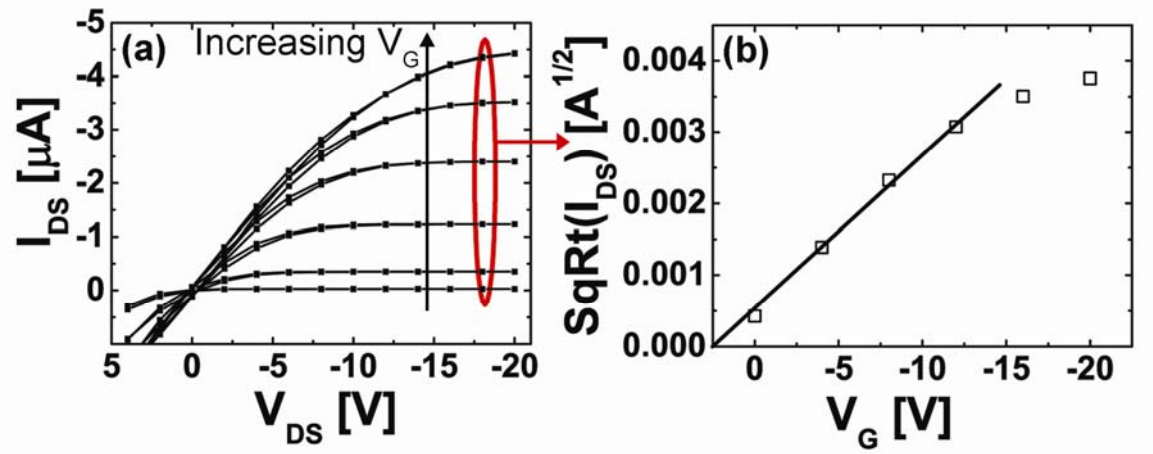

Figure 2.1. (a) Representative current-voltage output curves for a p-type organic semiconductor as a function of increasing gate voltage. In (b) the square root of the source-drain current in the saturation regime has been plotted as a function of gate voltage. The saturation charge-carrier mobility and threshold voltage of the thin-film transistor can be extracted from the slope and x-intercept of the fitted line, respectively.

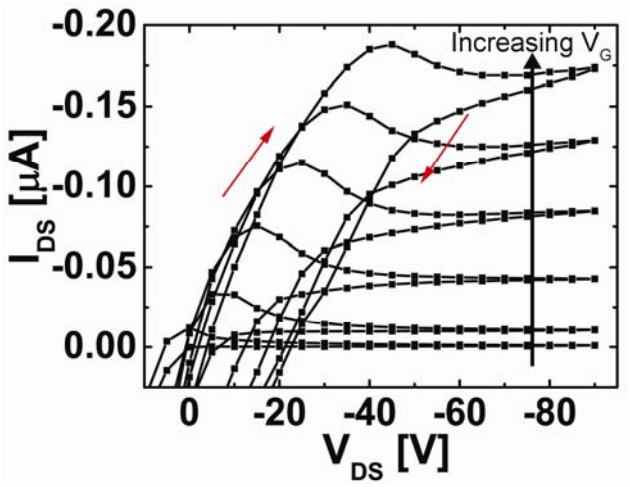

Figure 2.2. Current-voltage output curves for an as-spun (amorphous) TES ADT thin-film transistor. There is significant current-voltage hysteresis between the forward and reverse sweep directions.

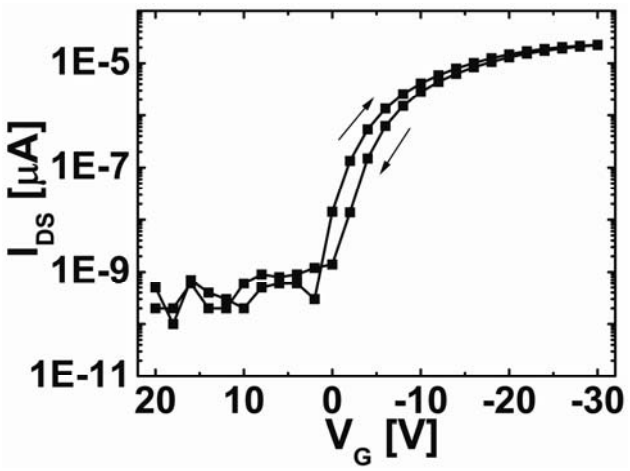

Figure 2.3. Representative transfer characteristics for a p-type organic thin-film transistor collected at a source-drain voltage of -20 V. The on/off current ratio is determined from this plot by dividing the maximum on current by the off current.

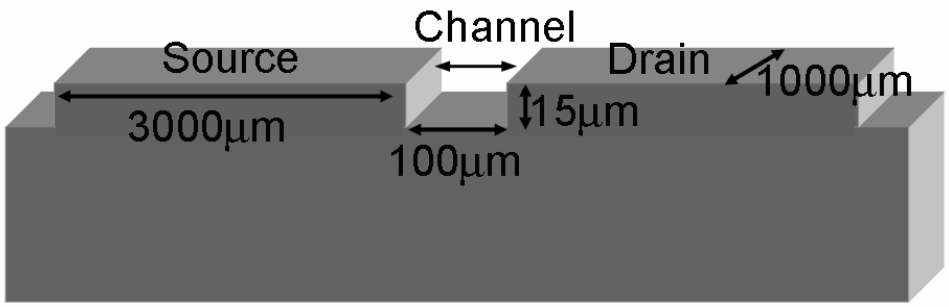

Figure 2.4. Schematic of silicon master with source and drain features after photolithography and reactive-ion etching.

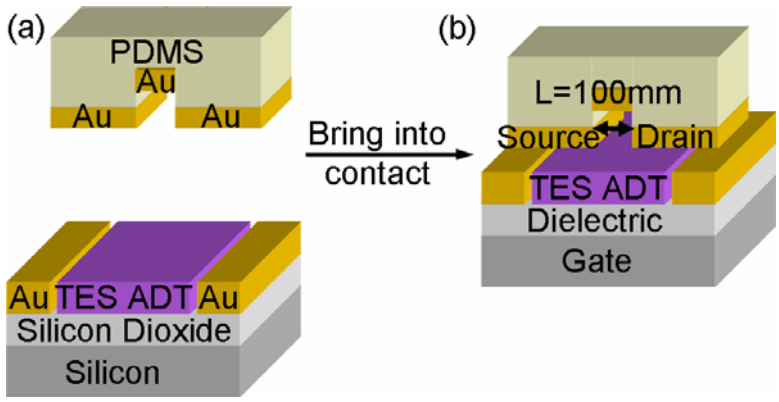

Figure 2.5. Soft-contact lamination scheme. (a) Titanium (2 nm) and gold (20 nm) are deposited onto a PDMS stamp with source and drain electrode features. (b) TES ADT is spin coated and annealed on a silicon substrate (with 100 nm of thermally-grown silicon dioxide). Gold contact pads (40 nm) are subsequently evaporated around the exterior of the TES ADT film. (c) The top-contact transistor is completed by contacting the PDMS stamp containing the source and drain electrodes against TES ADT. The recessed region of the PDMS stamp defines the channel dimensions (L = 100 μm, W = 1000 μm) of the thin-film transistor.

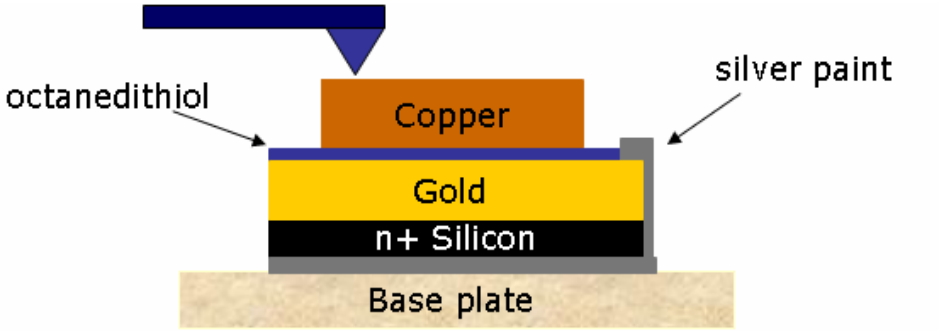

Figure 2.6. Schematic of the conductive probe AFM (C-AFM) set-up for measuring through-plane conductivity of printed copper patterns.

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Chapter 3: Understanding the Processing-Structure-Property Relationships of Solution-Processable Anthradithiophene Derivative Organic Semiconductors

TRIETHYLSILYLETHYNYL ANTHRADITHIOPHENE

As the electronics industry moves towards the realization of organic electronic devices, such as flexible displays,[1] organic light-emitting diodes,[2] photovoltaic cells,[3] sensors,[4] and radio-frequency identification tags,[5] solution-processable, electrically-active organic materials are desired because solution processability enables a host of fast, large-area, low-cost deposition techniques, such as drop casting, spin casting and printing.[6-11] Electrically-active organic materials, however, are often poorly soluble in organic solvents or they exhibit poor stability in solution.[12, 13] Recent research in the development of solution-processable, electrically-active, organic materials has focused on developing air-, moisture-, and light-stable, solution-processable organic semiconductors[14-16] with charge-carrier mobility comparable to that of amorphous silicon (0.1 – 1 cm^2/V-s).[17, 18] These new, solution-processable organic semiconductors are typically semi-crystalline polymers, such as polythiophenes (charge-carrier mobility of 0.1 - 0.3 cm^2/V-s),[19-22] or small-molecule organic precursors that require subsequent chemical and/or thermal conversion after deposition to become electrically active (0.01 to 0.7 cm^2/V-s).[23-26]

In recent years, some promising solution-processable, small-molecule organic semiconductors that do not require any post-deposition conversion have been developed Professor John Anthony's research group in the Department of Chemistry at the University of Kentucky.[27-31] Unlike previous generations of solution-processable organic semiconductors, the organic semiconductors synthesized by the Anthony research group are electrically active immediately after deposition without any subsequent conversion

steps. These solution-processable organic semiconductors are derived from pentacene[32, 33] and anthradithiophene,[34-36] both well-studied small-molecule organic semiconductors. Through the addition of bulky side chains and backbone substitutions, the Anthony group imparts solution processability, 2-D ordering, and stability to pentacene and anthradithiopehene derivatives.[27, 37, 38] We obtained the most viable solution-processable anthradithiophene derivative, triethylsilylethynyl anthradithiophene (TES ADT; see Illustration 3.1),[28, 29] for our studies. TES ADT is a promising p-type organic semiconductor because it is highly soluble in a variety of organic solvents, forms highly-ordered crystalline films, exhibits good stability both in solution and in the solid state, and can be processed and characterized at ambient conditions.

While solution-processable organic semiconductors are attractive from a low-cost processing perspective, devices with solution-processed organic semiconductor thin films often exhibit reduced electrical properties compared to devices with their thermally-evaporated counterparts due to a lack of molecular ordering in the solution-processed films.[23, 26, 39-42] For example, during spin casting, the solvent evaporates before the organic semiconductor can fully order. Consequently, spin-cast films are often amorphous, and the charge carrier mobility of the resulting device is poor (10^{-3} – 10^{-4} cm^2/V-s).[20, 43] In contrast, thermally-evaporated pentacene films are highly crystalline, and the charge-carrier mobility of the resulting device is often greater than 1 cm^2/V-s.[44, 45] This disparity in charge-carrier mobility between crystalline and amorphous small-molecule organic semiconductor thin films creates a need for post-deposition steps to increase crystallinity and enhance grain growth in as-deposited, solution-processable organic semiconductors.

Recently, we demonstrated how a straightforward, one-step, solvent-vapor annealing process can induce crystallization, and thereby can dramatically improve the

electrical properties of TES ADT.[46] To evaluate the electrical properties of the solvent-vapor annealed TES ADT film, we built and tested bottom-contact thin-film transistors on silicon (see Figure 1.1a), on which TES ADT is directly spin coated. After spin casting, the TES ADT thin film is amorphous. The subsequent solvent-vapor annealing is a physical process that enhances grain growth and thin-film crystallinity of the spin-coated TES ADT; additional reactions – either by thermal or chemical means – to convert the as-deposited material into an electrically-active organic semiconductor are not neccessary. While thin-film transistors built with this material can exhibit high charge-carrier mobility, there is great device-to-device variability (0.001 to 1 cm^2/V-s). This variability appears to correlate with morphological inhomogeneities in the as-deposited TES ADT films. With solvent-vapor annealing, we can repeatedly and reproducibly fabricate TES ADT thin-film transistors that exhibit an average charge-carrier mobility of 0.13 ± 0.07 cm^2/V-s in air over large areas. The charge-carrier mobility of these solvent-vapor annealed transistors is on par with backplane requirements to drive displays (mobility $\geq$ 0.1 cm^2/V-s).[6, 12]

Our bottom-contact TES ADT thin-film transistors were built on a silicon-silicon dioxide platform. The highly-doped silicon served as a common gate electrode for all the transistors on the same chip, and the thermally-grown silicon dioxide (300 nm) served as the gate dielectric. Gold source and drain electrodes were defined on the dielectric surface by electron-beam evaporation through a shadow mask. TES ADT solution (2 wt% in toluene) was then directly spin coated on the freshly-evaporated electrodes; neither the electrodes nor the dielectric surface were treated prior to TES ADT deposition. Although there are several reports in literature that demonstrate that modifying the dielectric surface with hydrophobic, self-assembled monolayers improves the charge-carrier mobility of pentacene[47, 48] and polythiophene[22] thin-film transistors, we

found that dielectric modification did not improve TES ADT thin-film transistor performance. This will be discussed in more detail later in this chapter. Additional details on the fabrication of these thin-film transistors are provided in the thin-film transistor fabrication section in Chapter 2. Figure 3.1a contains an optical microscope image of as-spun TES ADT taken in the channel region of a representative thin-film transistor. The optical microscope image is featureless over large areas, suggesting that the as-spun TES ADT is amorphous. Unlike TES ADT powder that reveals high levels of crystallinity[29] (Figure 3.2), x-ray diffraction experiments carried out on the as-spun film reveal no Bragg reflections, confirming that the film is completely amorphous. That TES ADT is unable to crystallize in the as-spun film stems from the fact that solvent (toluene) evaporation occurs much faster than the time required for TES ADT to crystallize. The output characteristics of this particular device (channel length, L = 208 μm; channel width, W = 1984 μm) are shown in Figure 3.1b. We tested 15 such devices of varying channel dimensions. These devices uniformly exhibited a low charge-carrier mobility (0.002 ± 0.002 cm^2/V-s), low on currents, and severe current hysteresis. The device characteristics are not impressive, yet they are not uncommon amongst thin-film transistors with solution-deposited organic semiconductors.[49-52]

Exposing the thin-film transistors to dichloroethane vapor changed the morphology of TES ADT rapidly and dramatically. Figure 3.1c contains an optical microscope image of TES ADT in the channel region of the same thin-film transistor after it was exposed to dichloroethane vapor for two minutes. Dichloroethane solvent-vapor annealing is performed in a Petri dish. Approximately 10 – 15 mL of dichlorethane are placed in the bottom of a glass Petri dish, and our as-spun TES ADT transistors are secured to the lid of the Petri dish with double-sided tape. Closing the Petri dish creates a dichloroethane-rich vapor environment. Exposing the as-spun TES ADT transistors to

dichloroethane vapors for 2 – 10 minutes is sufficient to completely crystallize the TES ADT film. We observe large grains (spanning several hundred microns to several millimeters) as evinced by the birefringence contrast in the optical microscope images in Figure 3.1c. At the microscopic level, x-ray diffraction experiments indicated that the annealed film is highly crystalline (Figure 3.2), and adopts the triclinic crystal structure (a = 6.73 Å; b = 7.25 Å; c = 16.7 Å; $\alpha = 98.14^{o}$; $\beta = 94.53^{o}$; $\gamma = 103.9^{o}$) of TES ADT in the bulk.[29] Accordingly, the device characteristics improved drastically. The output characteristics of the same device, after exposure to dichloroethane vapor for two minutes, are shown in Figure 3.1d. Of 23 such devices tested, the average charge-carrier mobility was 0.11 ± 0.09 cm^2/V-s. The on currents increased by at least a factor of 100, and the hysteresis observed in the current-voltage characteristics of the as-spun thin-film transistors was largely eliminated. While the on current increased drastically with solvent-vapor annealing, we generally observed an increase in the off current with annealing as well. But since the increase in the off current was generally small, we observed a moderate overall increase in the on/off current ratios (about two orders of magnitude).

To examine this solvent-vapor annealing process more closely, we also looked at the effects of annealing TES ADT thin-film transistors with solvent vapors of varying polarity – acetone (most polar of the solvents explored, Hilderbrand solubility parameter,[53] δ, of 9.77 $cal^{1/2}/cm^{3/2}$), tetrahydrofuran, toluene, and hexanes (non-polar; δ = 7.24 $cal^{1/2}/cm^{3/2}$) – to determine how polarity (among other solvent physical properties; listed in Table 3.1) affects the structural rearrangement of TES ADT, and accordingly, the resulting device performance of TES ADT thin-film transistors. A summary of the device statistics after two minutes of solvent-vapor annealing with each of the solvents is presented in Figure 3.3. Of the solvents studied, dichloroethane vapor annealing yielded

transistors with the highest charge-carrier mobility (0.11 ± 0.09 cm^2/V-s) and on/off current ratio, while hexanes vapor annealing (0.002 ± 0.001 cm^2/V-s, 5 transistors tested) resulted in very little improvement over the as-spun transistors. Toluene vapor annealing yielded transistors with a charge-carrier mobility (0.05 ± 0.04 cm^2/V-s, 18 transistors tested) that is an order of magnitude higher than the as-spun transistors. Acetone (0.01 ± 0.001 cm^2/V-s, 15 transistors tested) and tetrahydrofuran (0.02 ± 0.02 cm^2/V-s, 5 transistors tested) vapor annealing yielded transistors with moderately improved charge-carrier mobility. Although marked differences in the device performance were noted, we did not observe a one-to-one correlation between the polarity of the solvent with improvements in the charge-carrier mobility or the on/off current ratios of the annealed devices. Comparing thin-film transistors annealed in acetone and dichloroethane vapor, two solvents with similar boiling temperatures and vapor pressures, we discerned that dichloroethane vapor annealing (0.11 ± 0.09 cm^2/V-s) is much more effective than acetone annealing (0.01 ± 0.001 cm^2/V-s). Yet, when we compared dichloroethane and toluene (0.05 ± 0.04 cm^2/V-s) vapor annealing, we observed that both solvents have a comparable effect on TES ADT despite drastic differences in the boiling temperatures and vapor pressures. So improvements in the charge-carrier mobility and the on/off current ratios do not appear to correlate with the boiling temperatures or the vapor pressures of the solvents either.

We are, however, able to correlate the improved charge-carrier mobility with the solubility of TES ADT in these solvents. TES ADT has low solubility in acetone and hexanes (< 100 mg/ml). Correspondingly, solvent-vapor annealing with these solvents yielded transistors with the lowest charge-carrier mobility. TES ADT is highly soluble in toluene and tetrahydrofuran (> 100 mg/ml), and transistors annealed in toluene and tetrahydrofuran solvent vapors exhibited an order of magnitude improvement in charge-

carrier mobility compared to as-spun transistors. In contrast, TES ADT is moderately soluble in dichlorethane (~ 100 mg/ml), and annealing with dichloroethane vapors yielded transistors with the highest charge-carrier mobility. These results suggest that there is an optimal TES ADT solubility that results in transistors with high charge-carrier mobility. Further, based on these results, we speculate that the solvent-vapor annealing process causes a structural rearrangement in the as-spun TES ADT film. To confirm this, we examined the annealed films under the optical microscope as a function of solvent-vapor annealing time and solvent type.

Table 3.1. Physical properties of solvents for solvent-vapor annealing and device characteristics after solvent-vapor annealing.

Solvent	Boiling Point	Vapor Pressure[54]	Solubility Parameter, δ ($cal^{1/2}/cm^{3/2}$) [53]	Charge-Carrier Mobility (cm^2/V-s)	V_T (V)	On/Off Current Ratio
Acetone	56.5°C	200 torr at 22.7°C	9.77	0.01 ± 0.001	36.1 ± 65.1	10^2
1,2-Dichloroethane	57.2°C	230 torr at 25°C	9.76	0.11 ± 0.09	24.0 ± 18.9	10^3
Hexanes	62-69°C	150 torr at 25°C	7.24	0.002 ± 0.0004	-1.4 ± 3.2	10^2
Tetrahydrofuran	66°C	143-145 torr at 20°C	9.52	0.02 ± 0.02	6.0 ± 5.2	10^2
Toluene	110.6°C	22 torr at 20°C	8.91	0.05 ± 0.04	11.1 ± 24.6	10^2

To further examine the effects of solubility on TES ADT film morphology and device performance, we characterized solvent-vapor annealed transistors as a function of time exposed to the solvent vapor. For simplicity and clarity, we will limit this discussion to the three solvents that yielded transistors with dramatically different device characteristics: dichloroethane, with which vapor annealing yielded devices with the highest charge-carrier mobility (0.11 ± 0.09 cm^2/V-s); toluene, with which vapor annealing yielded devices with moderate charge-carrier mobility (0.05 ± 0.04 cm^2/V-s); and acetone, with which vapor annealing did not markedly improve device performance.

Figure 3.4 contains optical microscope images of TES ADT taken at various stages of vapor annealing with dichloroethane (top three microscope images) and toluene (bottom three). In dichloroethane, grain growth occurs very quickly. We observe large grains after having exposed TES ADT to dichloroethane vapor for merely a minute. With additional annealing, the remaining amorphous region (note changes in the bottom left corner of the microscope images during the progression of Figures 3.4a-c) within the film crystallizes. To first order, toluene vapor annealing induces rapid grain growth as well. We observe that the amorphous region at the bottom of Figure 3.4d (after a one minute exposure to toluene vapor) becomes progressively crystalline on annealing. Grain growth with toluene vapor annealing, however, is accompanied by the formation of finger-like patterns on extended annealing that results from TES ADT dewetting the silicon substrate (Figures 3.4d-f). This dewetting phenomenon starts off as individual "holes" in the crystalline region of the films (Figure 3.4d). These holes subsequently develop into continuous finger-like patterns across the entire TES ADT film on extended annealing (Figures 3.4e and f). That dewetting only occurs with toluene vapor annealing, and not dichloroethane vapor annealing, stems from the fact that toluene partitions more significantly in TES ADT compared to dichloroethane. So TES ADT is more mobile when plasticized with toluene vapor compared to when it is plasticized with dichloroethane vapor for a given exposure. We also carried out similar microscopy experiments with the acetone vapor annealed specimen (not shown). Exposing TES ADT to acetone did not induce significant grain growth, even after extended periods. The resulting optical microscope images therefore look very similar to that of the as-spun TES ADT shown in Figure 3.1a. X-ray diffraction experiments carried out on these annealed films are consistent with the observed morphological transformation. The spectra are shown in Figure 3.2. In particular, dichloroethane and toluene vapor annealed

films are highly crystalline; these films adopt the crystal structure of bulk TES ADT on annealing.[29] On the contrary, acetone vapor annealed films are amorphous.

The variation in device characteristics with solvent-vapor annealing time is consistent with the morphological transformation that takes place with solvent-vapor annealing. Figure 3.5 summarizes the device characteristics of TES ADT bottom-contact thin-film transistors with time for dichloroethane-, toluene-, and acetone-vapor annealing. Generally, we observe a steady increase in the charge-carrier mobility and the on/off current ratio with increasing annealing time. The increase in charge-carrier mobility was most pronounced during the first two minutes of annealing where the most significant grain growth occurs. Subsequent annealing only improved the charge-carrier mobility modestly. With toluene-vapor annealing, however, we observe a slight drop off in the charge-carrier mobility beyond two minutes of annealing. We attribute this to the discontinuities that result as a consequence of TES ADT dewetting the silicon substrate (see Figures 3.4e and f). In contrast, dichloroethane-vapor annealing produced grains that are similar in size but continuous; the thin-film transistors that were exposed to dichloroethane vapor exhibited charge-carrier mobility that increases monotonically with annealing.

Similar to toluene-vapor annealing, vapor annealing with tetrahydrofuran, another solvent that partitions significantly in TES ADT, yielded TES ADT thin films that were highly crystalline and devices with moderate charge-carrier mobility (0.02 ± 0.02 cm^2/V-s). Solvent-vapor annealing with hexanes, which at room temperature only weakly partitions in TES ADT, yielded results similar to acetone-vapor annealing – the TES ADT thin films were largely amorphous and little improvement in device characteristics was observed as a consequence.

With the exception of hexanes, all solvent-vapor annealing processes increased the threshold voltage of the transistors (Figure 3.3). Recall that the threshold voltage is the voltage required to switch the transistor from the "off" state to the "on" state. For practical applications, the threshold voltage of organic thin-film transistors should be zero. A threshold voltage of zero is uncommon; therefore it is desirable for organic thin-film transistors with p-type organic semiconductors to have a small, negative threshold voltage to avoid having to apply a positive bias to turn off the transistors. Since the threshold voltage is also an indication of the quality of the organic charge transport interface,[14, 55] the fact that solvent-vapor annealing increased the threshold voltage of the transistors is a good indication that the solvent vapor is able to penetrate the thickness of the organic semiconductor thin film (≈ 100 nm) to either alter the interfacial dipole,[56, 57] or to induce structural rearrangement at the buried organic semiconductor-dielectric interface. Indeed, several recent studies have reported how the modification of the organic semiconductor-dielectric interface with self-assembled monolayers (SAMs) with varying headgropus can shift the threshold voltage towards positive or negative values depending on polarity of the headgroups.[56, 58-60] For example, treating the dielectric surface with a SAM containing fluorine headgroups (electron withdrawing; so holes accumulate at the organic semiconductor-dielectric interface at zero bias) prior to organic semiconductor deposition can induce a positive threshold voltage in pentacene (p-type) thin-film transistors. On the other hand, treating the dielectric surface with a SAM containing NH_2- headgroups (electron donating; electrons accumulate at the organic semiconductor-dielectric interface) prior to organic semiconductor deposition can induce a negative threshold voltage in pentacene thin-film transistors.[60] Placing a SAM with a permanent electric dipole along the molecular axis between the organic semiconductor and the dielectric surface is thus equivalent to applying a negative bias to the gate; it

creates a charge accumulation layer at the dielectric-semiconductor interface.[56] In our experiments, we noted a strong correlation between the polarity of the solvent and the magnitude of the threshold voltage. That is, annealing the TES ADT thin-film transistors in the most polar solvent vapor, acetone, resulted in the highest threshold voltage, whereas annealing the thin-film transistors in non-polar solvent vapor, like hexanes, resulted in a near-zero threshold voltage. The polarity of the other solvents in question fall in between that of acetone and hexanes, and the threshold voltages of the thin-film transistors annealed in these solvent vapors are bracketed by those of acetone and hexanes vapor annealed devices accordingly. Since TES ADT is a p-type organic semiconductor, a positive threshold voltage indicates hole accumulation at the organic semiconductor-dielectric interface, even without the application of a gate bias.[61] By this rationale, it is not surprising that the magnitude of the threshold voltage changes with the polarity of the solvent. For example, having acetone vapor – the most polar and thus the most electronegative of the solvents – at the organic semiconductor-dielectric interface induces the highest concentration of holes to accumulate at the interface in question. As such, the threshold voltage is large and positive (36.1 ± 65.1 V). At the other polarity extreme, the presence of hexanes (non-polar) at the interface does not induce any hole accumulation so the threshold voltage remains close to zero (-1.4 ± 3.2 V). We note that a positive and highly variable threshold voltage was recorded for as-spun TES ADT devices that were not annealed (5.4 ± 14.6 V). Since the dielectric surface was not treated, variations are not uncommon given that any contaminants or imperfections, such as the presence of moisture, oxygen, hydroxyl groups, and mobile ions, at the organic semiconductor-dielectric interface can influence the threshold voltage.[56, 62-64] Solvent-vapor annealing with hexanes thus appears to displace such contaminants at the interface in question.

We previously established that the threshold voltage generally increases at short solvent-vapor exposure times; the magnitude of the threshold voltage depends on the polarity of the solvent in use. With extended annealing, however, the threshold voltage recovers. With both toluene and acetone solvent-vapor annealing, the threshold voltage actually falls below zero after ten minutes of annealing. That the threshold voltage recovers with extended annealing implies that the alteration of the surface potential at the organic semiconductor-dielectric interface does not solely govern the threshold voltage. While it has been established that the morphology of the organic semiconductor thin film does not have an adverse effect on the threshold voltage,[56] structural changes at the molecular length scale at the organic semiconductor-dielectric interface may be responsible for the subsequent reduction in threshold voltage with extended annealing. Although we do not observe macroscopic changes in the morphology of the TES ADT film, there may be microscopic structural rearrangement occurring at the organic semiconductor-dielectric interface that causes the threshold voltage to shift.

Building on the relationship between polarity and threshold voltage (i.e., annealing with low polarity solvents, such as hexanes vapors, yielded transistors with low threshold voltage, while annealing with high polarity solvents, such as acetone vapors, yielded transistors with a high threshold voltage), we explored ways of manipulating the solvent quality to achieve TES ADT thin-film transistors that simultaneously possess both high charge-carrier mobility and low threshold voltage. Since solvent-vapor annealing with hexanes does not yield highly crystalline TES ADT films, hexanes alone cannot be used to realize devices with high charge-carrier mobility and low threshold voltage. In an effort to combine the desirable effects of both hexanes and dichloroethane solvent-vapor annealing, we attempted to implement a two-step annealing process. We built bottom-contact thin-film transistors on a silicon/silicon dioxide (300nm) platform.

Gold source and drain electrodes were deposited through a shadow mask by e-beam evaporation. Prior to depositing the TES ADT solution (2wt% in toluene), the patterned silicon substrate was placed in the UV/Ozone chamber for 20 minutes. After depositing the TES ADT film, we collected device characteristics on the as-spun transistors (charge-carrier mobility = 0.002 ± 0.004 cm^2/V-s, V_T = 10.1 ± 5.4 V). We then exposed the as-spun TES ADT thin-film transistors to dichloroethane vapors, yielding a crystalline TES ADT film with high charge-carrier mobility (0.2 cm^2/V-s) and high threshold voltage (35.3 ± 9.9 V). Subsequently, we exposed the crystalline TES ADT thin-film transistors to hexanes vapors in an attempt to lower the threshold voltage of the annealed transistors. The results are summarized in Table 3.2. As expected, the dichloroethane solvent-vapor annealing step crystallizes the TES ADT film, resulting in a two order of magnitude improvement in the charge-carrier mobility compared to the charge-carrier mobility of the as-spun transistors. The subsequent hexanes solvent-vapor annealing step, however, did not lower the threshold voltage of the thin-film transistors unless extended annealing (> 7 hours) was implemented. Over a period of seven hours of exposure to hexanes vapors, there was minimal change in the threshold voltage (Figure 3.6). Upon annealing beyond seven hours, the threshold voltage began to decrease slightly. Simultaneously, we observe the charge-carrier mobility also began to decrease sharply. Upon examination of the TES ADT film in the channel after extended hexanes annealing, we observed severe dewetting of the TES ADT film from the silicon dioxide surface which resulted in a discontinuous TES ADT film across the transistor channel. This dewetting, shown in Figures 3.7b and c, is responsible for the decrease in the charge-carrier mobility. We speculate that the hexanes solvent-vapor annealing failed to reduce the threshold voltage significantly is related to the previous dichloroethane solvent-vapor annealing step. Once the TES ADT film is crystallized by dichloroethane vapors, it is

difficult for the hexanes vapors to penetrate through the crystalline TES ADT film to reach the organic semiconductor/dielectric interface. As such, short annealing times in the presence of hexanes vapors are not sufficient to lower the threshold voltage. With extended annealing, on the order of 7 – 12 hours, the hexanes vapors are able to reach the semiconductor/dielectric interface resulting in a reduction of the threshold voltage by a factor of 2. But this threshold voltage reduction is accompanied by a siumultaneous decrease in the charge-carrier mobility by an order of magnitude due to TES ADT dewetting.

Table 3.2. Variation of TES ADT charge-carrier mobility and threshold voltage with annealing solvent and time.

Annealing Conditions	**Charge-Carrier Mobility (cm^2/V-s)**	**Threshold Voltage (V)**
As-spun transistors	0.002 ± 0.004	10.1 ± 5.4
2 minutes 1,2-Dichloroethane (DCE)	0.2 ± 0.04	35.3 ± 10.0
2 minutes DCE + 3 minutes Hexanes	0.3 ± 0.06	31.9 ± 8.3
2 minutes DCE + 10 minutes Hexanes	0.3 ± 0.1	33.0 ± 6.2
2 minutes DCE + 40 minutes Hexanes	0.2 ± 0.04	32.8 ± 10.4
2 minutes DCE + 7 hours Hexanes	0.1 ± 0.04	29.2 ± 10.7
2 minutes DCE + 11 hours Hexanes	0.03 ± 0.01	14.5 ± 3.1

To prevent dewetting of TES ADT from the silicon dioxide surface, it is necessary to reduce the hexanes vapor annealing time to minutes, rather than hours. We have already shown, however, that short hexanes annealing times are not effective at reducing the threshold voltage of crystalline TES ADT films. To overcome this challenge, we switched to a mixed solvent-vapor annealing process. By mixing together hexanes and dichloroethane solvent vapors, we hoped to simultaneously crystallize the as-spun TES ADT film in the channel of the thin-film transistor, and lower the threshold

voltage. In the mixed solvent-vapor annealing experiments, we varied the ratio of hexanes to dichloroethane from 1:1 (v/v) through 15:1 (v/v) in the annealing solvents. In our experimental setup, we did not have control over the solvent composition in the vapor space. Since dichloroethane has a lower boiling point and a higher vapor pressure compared to hexanes, we expect that the ratio of dichloroethane to hexanes will be higher in the vapor space than in the liquid phase. We built bottom-contact TES ADT thin-film transistors by the same procedures described previously with one exception. Following electrode deposition, the silicon substrate was placed in a UV/Ozone chamber for 20 minutes. TES ADT was subsequently deposited and annealed as described previously. The charge-carrier mobility and threshold voltage for each set of transistors (we tested approximately 5 transistors for each solvent mixture) are plotted as function of solvent composition in the liquid phase in Figure 3.8. All solvent mixtures yielded thin-film transistors with high charge-carrier mobility (~0.1 cm^2/V-s) and typical on/off current ratios ($10^3 – 10^4$, data not shown). From Figure 3.8, there appears to be an optimal ratio of hexanes to dichloroethane of 3:1 v:v in the liquid phase that yields transistors with high charge-carrier mobility and reduced threshold voltage. Annealing with this solvent vapor mixture also yielded devices with maximum on/off current ratios. That the threshold voltage after mixed solvent-vapor annealing is non-zero is not unexpected since both hexanes and dichloroethane vapors are present at the semiconductor/dielectric interface during the annealing process. It is worth noting, however, that the threshold voltage achieved with the mixed solvent-vapor annealing is lower than annealing with dichloroethane solvent vapors alone. This is an important result because it illustrates that we are able to manipulate the materials properties of TES ADT through advantageous selection of processing conditions. Given the lower boiling point and higher vapor pressure of dichloroethane compared to hexanes, we would expect a higher composition

of dichlorethane in the vapor space than what we added to the liquid phase, which may explain why the threshold voltage is significantly higher than zero. Currently, we are not able to explain why the higher ratios of hexanes to dichloroethane actually increase the threshold voltage especially given that the TES ADT films annealed with the mixed solvent vapors all look comparable under the optical microscope (Figure 3.9). We speculate that the variations in threshold voltage are related to the condition of the dielectric surface prior to TES ADT deposition.

In fact, we have observed several examples in which the condition of the silicon dioxide surface not only affects the transistor performance, but it also affects the adhesion of TES ADT to the silicon dioxide surface. For example, lowering the surface energy of the silicon dioxide surface by treating it with hydrophobic molecules, such as octadecyltrichlorosilane (OTS) and hexamethyldisilazane (HMDS), prevents TES ADT from adhering to the treated silicon dioxide surface. This result contradicts previous literature reports which show that modifying the silicon dioxide surface with OTS and HMDS improves the charge-carrier mobility of pentacene (from 10^{-1} cm^2/V-s to greater than 1.5 cm^2/V-s),[47, 48, 65-67] polythiophene (from 0.05 cm^2/V-s to 0.1 cm^2/V-s)[22] and polyfluorene (from $7x10^{-4}$ to 0.02 cm^2/V-s)[68] thin-film transistors. We have since determined the optimal conditions for TES ADT deposition: the silicon dioxide surface needs to be "dirty." In other words, if the silicon dioxide surface is cleaned too thoroughly with piranha solution and/or solvents, TES ADT will dewet from the silicon dioxide surface when plasticized with solvent during solvent-annealing. Our experience indicates that TES ADT thin-film transistors perform best when the silicon dioxide surface is sonicated in deionized water for less than 5 minutes to remove particulates and treated in a UV/Ozone chamber for 5 – 20 minutes prior to TES ADT deposition. We speculate that the UV/Ozone cleaning generates a hydrophilic surface that interacts

favorably with TES ADT molecules to yield a continuous TES ADT thin film, yet not sufficiently polar to induce dewetting. Additional surface cleaning is unnecessary, and can actually lead to discontinuous TES ADT thin films.

In summary, we discovered that a simple solvent-vapor annealing process can induce drastic morphological and structural rearrangement within amorphous thin films of TES ADT, a solution processable p-type organic semiconductor. As a result, thin-film transistors fabricated with annealed TES ADT showed dramatically improved device characteristics over thin-film transistors fabricated with as-spun TES ADT. Further, the device characteristics of annealed TES ADT thin-film transistors are on par with applications requirements.[6, 12] This solvent-vapor annealing process is physical – the solvent vapor partitions into the thin films enabling structural rearrangement to take place over the entire silicon substrate – and does not involve a subsequent chemical reaction. The extent of morphological transformation and improvement in electrical characteristics depends on the partitioning ability of the solvent vapor into the organic semiconductor. Toluene vapor partitions strongly in TES ADT; we observe large grains that are highly crystalline on annealing. This grain growth, however, is accompanied by simultaneous dewetting of the material from the silicon substrate, which in turn leads to moderately improved device characteristics. Acetone and hexanes vapors, on the other hand, partition weakly in TES ADT. As a consequence, little annealing takes place, so we do not observe any marked difference in morphology or in device characteristics between as-spun and annealed devices. The ability of dichloroethane vapor to partition into TES ADT appears to be "just right" – we observe large, continuous, highly crystalline grains spanning several hundred microns to several millimeters. Accordingly, we observe the most pronounced improvements in the device characteristics of dichloroethane vapor annealed TES ADT devices.

More subtly, we observe an interesting correlation between the threshold voltage of the annealed devices and the type of annealing solvent. To first order, the magnitude of the threshold voltage is governed by the polarity of the solvent. Our experiments suggest that the solvent vapor is able to penetrate the as-spun organic semiconductor thin film. The adsorbed solvent vapor is capable of modifying the surface potential at the organic semiconductor-dielectric interface. Attempts to lower the threshold voltage of dichloroehane-annealed transistors with a subsequent hexanes solvent-vapor annealing step were unsuccessful because the hexanes vapors were unable to penetrate crystalline TES ADT thin films to reach the organic semiconductor-dielectric interface. Annealing as-spun TES ADT thin-film transistors in a mixture of hexanes and dichloroethane solvent vapors did yield thin-film transistors with crystalline TES ADT thin films in the channel regions and a lower threshold voltage than if the as-spun TES ADT thin-film transistors had been annealed solely in dichloroethane solvent vapors.

TES ADT DERIVATIVES

Charge-carrier mobility in organic semiconductors generally depends on π-π stacking between adjacent molecules.[69] Pentacene, an organic semiconductor that holds the record for having the highest charge-carrier mobility among organic semiconductors (as high as 5 cm^2/V-s),[32, 33, 70-72] forms a herringbone crystal structure with 2-D π-π stacking with edge-to-face π-interactions (Figure 3.10a).[73-75] Further increasing the 2-D π-π stacking to realize face-to-face π-interactions (Figure 3.10b) should thus result in organic semiconductors with even higher charge-carrier mobilities.[29-31, 69, 76] Our effort in this area involves the examination of a series of TES ADT derivatives in which backbone substitutions have been made to yield either 1-D or cofacial 2-D π-π stacking. To date, only devices made with molecules that exhibit 2-D π-π orbital overlap exhibit

acceptable thin-film transistor performance.[29, 77] The series of TES ADT derivatives we studied is shown in Illustration 3.2. Halogens, methoxy groups, and methyl groups were substituted on the terminal carbon of the thiophene rings on the anthradithiophene backbone. In general, as the size of the substituent increases, the crystal packing typically shifts from 1-D "slip-stack"[29] packing to 2-D cofacial "bricklayer" π-stacking[29] and then back to the 1-D "slip-stack" packing and finally to a herringbone packing to accommodate the steric hindrance caused by the substituents.[77] These crystal packings are illustrated in Figure 3.10 for clarity. The switch from "slip-stack" packing to "bricklayer" packing occurs when the substituent diameter is close to one half the diameter of the anthradithiophene backbone.[78] The triethylsilyl substituents on TES ADT are approximately one half the diameter of the anthradithiophene backbone, so TES ADT adopts a 2-D cofacial "bricklayer" packing (Figure 3.10b), which is consistent with our findings that devices containing crystalline TES ADT generally exhibit high charge-carrier mobility. If the diameter of the substituent is less than one half the diameter of the anthradithiophene backbone the crystal packing remains unchanged by the addition of the substituent.[77]

To evaluate the TES ADT derivatives, we built and tested bottom-contact thin-film transistors on silicon with 100 nm of silicon dioxide by the procedures described previously. Our transistors had a channel length of 100 μm and a channel width of 1000 μm. We dissolved TES ADT-Cl, TES ADT-I, and TES ADT-Br in toluene (0.5wt%) and spin coated them directly on the patterned silicon substrate. Devices made with all three of these molecules exhibited unremarkable device performance, the thin-film transistor characteristics are summarized in Table 3.3. Specifically, TES ADT-Cl did not show any field effect, while the as-spun charge-carrier mobilities of TES ADT-I devices (0.002 ± 0.0005 cm^2/V-s, 9 transistors tested) and TES ADT-Br devices (0.008 ± 0.003 cm^2/V-s,

10 transistors tested) were comparable to that of devices made with as-spun TES ADT (0.002 ± 0.002 $cm^2/V\text{-}s$). Optical microscope images of as-spun TES ADT-I and TES ADT-Br films are shown in Figures 3.11a and c, respectively. Neither of the as-spun thin film showed signs of crystallinity. Solvent-vapor annealing with toluene, 1,2-dichloroethane, 1,2-dichlorobenzene and chloroform did not improve the charge-carrier mobility of the as-spun transistors, although chloroform did induce crystallization in TES ADT-I, as shown in Figure 3.11b. Since solvent-vapor annealing did not crystallize the organic semiconductor films, we performed differential scanning calorimetry (DSC) on TES ADT-Cl and TES ADT-I to determine if thermal annealing was a viable option. Unlike TES ADT, which shows a high degree of crystallinity by DSC, we did not observe any significant thermal transitions in TES ADT-Cl or TES ADT-I, as shown in Figure 3.12. These results suggest that the molecules are not good candidates for thermal annealing. Additionally, we tried to improve the performance of the halogenated TES ADT derivatives by varying the deposition conditions. We chose solvents that the TES ADT derivatives were more soluble in, such as chlorobenzene, 1,2-chlorobenzene and chloroform. Spin casting TES ADT-Cl and TES ADT-I from chlorobenzene and 1,2-dichlorobenzene generated discontinuous organic semiconductor thin films. Drop casting TES ADT-I and TES ADT-Br from toluene also yielded discontinuous thin films (Figures 3.13a and b). Drop casting TES ADT-Cl from chloroform yielded a continuous thin film (Figure 3.13c). Devices made with drop cast TES ADT-Cl, however, did not show field effect. From these results, we concluded that TES ADT-I, TES ADT-Cl and TES ADT-Br are not promising organic semiconductor candidates. These results are consistent with the crystal packing adopted by the TES ADT-I, -Cl, and -Br molecules. The size of the halogen substituents is large enough to cause crystal packing to shift from the 2-D cofacial "bricklayer" π-stacking adopted by TES ADT (Figure 3.10b) back to the

1-D "slipstack" packing illustrated in Figure 3.10c. In the 1-D "slipstack" packing, there is virtually no π-orbital overlap in the organic semiconductor thin films, thereby limiting charge transport.

Table 3.3. Summary of the electrical characteristics of thin-film transistors with TES ADT derivatives.

Molecule	Deposition Method (Solvent)	# of TFTs	Charge-Carrier Mobility (cm^2/V-s)	Threshold Voltage (V)
TES ADT-I	Spin cast (toluene)	9	0.002 ± 0.0005	-2.2 ± 1.7
TES ADT-Cl	Spin cast (toluene) drop cast (chloroform)	6	–	–
TES ADT-Br	Spin cast (toluene)	10	0.008 ± 0.003	18.6 ± 5.1
TES ADT-F	Spin cast (toluene)	5	0.001 ± 0.0005	37.7
	Drop cast (toluene)	11	0.05 ± 0.03	2.6 ± 1.6
TES ADT-F with PFBT	Drop cast (toluene)	25	0.2 ± 0.07	0.6 ± 3.0
MeOTES ADT	Spin cast (toluene)	20	0.002 ± 0.002	7.9 ± 7.8
	Drop cast (toluene)	10	0.002 ± 0.003	-2.7 ± 5.5
	Blade cast (toluene)	10	0.003 ± 0.003	-1.7 ± 0.5
Methyl TES ADT	Spin cast (toluene)	15	0.001 ± 0.001	-2.5 ± 1.1
	Drop cast (toluene)	7	0.002 ± 0.002	24.9 ± 13.3
	Blade cast (toluene)	12	0.005 ± 0.006	9.9 ± 6.9

Of all the halogenated TES ADT derivatives, TES ADT-F is the most promising organic semiconductor candidate as the fluorine substituent is small enough to be sterically neutral.[78] As a consequence, the 2-D cofacial "bricklayer" π-stacking adopted by TES ADT should be conserved in the TES ADT-F (Figure 3.10d). Although the charge-carrier mobility of as-spun TES ADT-F thin-film transistors is unremarkable (0.001 ± 0.0005 cm^2/V-s, 5 transistors tested), drop-cast TES ADT-F thin-film transistors exhibit charge-carrier mobility that is an order of magnitude higher (0.05 ± 0.03 cm^2/V-s). Optical microscope images of as-spun and drop-cast TES ADT thin-film transistors

are shown in Figures 3.14a and b, respectively. As expected of an as-spun film, as-spun TES ADT-F is amorphous; there is no evidence of crystallinity in the optical microscope image shown in Figure 3.14a. Similar to the TES ADT transistors, we suspect the amorphous film is responsible for the low charge-carrier mobility observed in as-spun TES ADT-F thin-film transistors. Corresponding with these structural observations, the current-voltage curves of as-spun TES ADT-F thin-film transistors exhibit low on currents, severe current-voltage hysteresis, and significant leakage currents, as shown in Figure 3.15a. In contrast, TES ADT-F drop cast from toluene or benzene forms highly-crystalline thin films comprising 2-D, long, flat rods. These rods tend to span the length of the transistor channel, as shown in Figure 3.14b. The current-voltage curves of drop-cast TES ADT-F thin-film transistors exhibit high on currents, and virtually no current-voltage hysteresis or leakage currents as shown in Figure 3.15b. These results are consistent with the 2-D structure of the long, flat rods present in the drop-cast TES ADT-F film. Attempts to improve the structure and charge-carrier mobility of as-spun TES ADT-F thin-film transistors with solvent-vapor annealing proved unsuccessful.

The charge-carrier mobility of drop-cast TES ADT-F thin-film transistors could be further improved (0.2 ± 0.07 $cm^2/V\text{-}s$) by treating the gold electrodes with pentafluorobenzenethiol (PFBT) prior to TES ADT-F deposition. Electrode modification is achieved by immersing the transistor platform with predefined gold source and drain electrodes in a 2mM solution of PFBT in ethanol for 2 minutes prior to TES ADT-F deposition. During immersion, the –SH head group of the PFBT molecule covalently bonds to the gold electrodes, but will not react with the silicon dioxide. The PFBT-treated transistor platform is subsequently rinsed with ethanol and dried under a stream of nitrogen. Treating the electrodes with a molecule with a strong electron withdrawing head group, such as PFBT, is a simple method for increasing the charge carrier

concentration at the semiconductor/electrode interface.[79] The increased charge carrier concentration should improve charge injection from the source electrode into the organic semiconductor thin film resulting in improved charge-carrier mobility.[79-81] The electrode treatment can be equated with doping of inorganic semiconductors to create more charge carriers in the transistor channel. Physically doping organic semiconductors to increase charge carriers at device contacts, however, is not effective because dopants are not stable in organic semiconductors, and tend to diffuse into the organic semiconductor channel over time, or under the influence of an applied electric field.[79] Covalently bonding PFBT to the gold electrode through the thiol head group provides a stable and effective way to increase the charge carrier density at the organic semiconductor-electrode interface.[82] The morphology of TES ADT-F drop cast on PFBT-treated gold electrodes is identical to the TES ADT-F film drop cast on untreated gold electrodes, as shown in Figures 3.14b and c. Typical current-voltage characteristics for TES ADT-F thin-film transistors in which the gold electrodes have been treated with PFBT are shown in Figure 3.15c. The current-voltage curves exhibit virtually no leakage currents, minimal current-voltage hysteresis, and the on-currents are improved by 3-fold compared to analogous TES ADT thin-film transistors without electrode treatment.

PFBT should not react with silicon dioxide, but it is possible for the molecules to physisorb on the dielectric surface. To verify that the PFBT treatment only modifies the electrode surface, and the silicon dioxide surface, we immersed a silicon substrate (with 100 nm of silicon dioxide) in a 2mM solution of PFBT before evaporating gold through a shadow mask to define the source and drain electrodes. A solution of TES ADT-F was then drop cast on the transistor platform to complete the devices. The charge-carrier mobility of this set of transistors was 0.04 ± 0.01 $cm^2/V\text{-}s$, which is comparable to the charge-carrier mobility of drop cast TES ADT-F thin-film transistors fabricated on an

untreated transistor platform (Table 3.3), suggesting minimal PFBT physisorbtion on the silicon dioxide. The fact that the morphology of TES ADT-F drop cast on PFBT-treated silicon dioxide is identical to morphology of the TES ADT-F films drop cast on untreated silicon dioxide (optical microscope image not shown) provides further evidence that PFBT treatment only modifies the charge injection interface, and not the charge transport interface. We can potentially further increase the charge-carrier mobility of these devices with the appropriate dielectric surface treatment. This was first demonstrated with pentacene thin-film transistors where the dielectric surface was treated with hexamethyldisilazane (HMDS) or octadecyltrichlorosilane (OTS) prior to pentacene deposition.[47, 48] The details of surface treatments are currently being explored by another graduate student.

The remaining TES ADT derivatives we studied were TES ADT-MeO and TES ADT-methyl (see Illustration 3.2 for their chemical structures). Similar to the halogenated TES ADT derivatives, we dissolved both molecules in toluene for solution processing. Bottom-contact, thin-film transistors were fabricated by drop casting, spin casting and blade casting from 1-2wt% solutions of these molecules. Optical microscope images of these solution-processed films are shown in Figure 3.16. All of the fabricated TES ADT-MeO and methyl TES ADT thin-film transistors showed field-effect. The average charge-carrier mobilities of both TES ADT-MeO and TES ADT-methyl, however, were only on the order of 10^{-3} $cm^2/V\text{-}s$ regardless of deposition technique (Table 3.3). Representative current-voltage curves, shown in Figure 3.17, exhibit low on currents and significant current-voltage hysteresis. While drop cast TES ADT-MeO films (Figure 3.16a) shows signs of crystallinity, the crystal domains are small, on the order of 5 – 20 μm, much smaller than the 100 μm channel length. Both spin coated and blade coated TES ADT-MeO films are amorphous (Figures 3.16b and c). Attempts to

improve the charge-carrier mobility of TES ADT-MeO thin-film transistors by solvent vapor annealing with 1,2-dichloroethane, toluene and methylene chloride were unsuccessful. We also tried to improve the performance of TES ADT-MeO by modifying the silicon dioxide surface with HMDS before depositing the TES ADT-MeO solution. Unfortunately, the surface treatment prevented TES ADT-MeO from forming a continuous film on the HMDS-treated channel. Since solution deposition did not yield TES ADT-MeO thin-film transistors with high charge-carrier mobility, we also tried depositing the TES ADT-MeO by thermal evaporation. Bottom-contact thin-film transistors were fabricated on HMDS-treated silicon, OTS-treated silicon, UV/Ozone-cleaned silicon and untreated silicon. In all cases, the thermally evaporated TES ADT-MeO thin-film transistors did not show significant field effect. The low charge-carrier mobility exhibited by TES ADT-MeO thin-film transistors can be explained by the crystal packing of TES ADT-MeO. Although the MeO substituent is not large enough to cause a shift from the 2-D "bricklayer" crystal packing to the 1-D "slipstack" packing, it is large enough to dirupt the π-stacking between adjacent TES ADT-MeO molecules as shown in Figure 3.10e. Given the poor π-stacking present in TES ADT-MeO thin films it is not surprising that TES ADT-MeO thin-film transistors perform so poorly.

The drop cast TES ADT-methyl film crystallized in a needle-like morphology (Figure 3.16d) that exhibited poor field effect despite the high degree of crystallinity and continuous nature of the material in the transistor channel. The morphologies of the as-spun and blade cast TES ADT-methyl films are unlike any of the other TES ADT derivatives (Figures 3.16e-f). The films are not completely amorphous as we observe many small grains throughout the TES ADT-methyl films. Additionally, the as-spun and blade cast films are not uniform across the transistor channel. Solvent vapor annealing with 1,2-dichlorethane, toluene and methylene chloride caused the TES ADT-methyl film

to dewet from the silicon dioxide surface. Chloroform and carbon disulfide solvent-vapor annealing did cause the TES ADT-MeO film to crystallize, as shown in Figure 3.18. The charge-carrier mobility, however, was actually reduced in these crystalline films. Similar to TES ADT-MeO, we speculate that the poor charge-carrier mobility in TES ADT-methyl transistors is caused by poor π-stacking in TES ADT-methyl films. While the methyl substituent is not large enough to cause the crystal packing to shift from 2-D cofacial "bricklayer" to 1-D "slipstack" packing, the methyl substituent is large enough to disrupt the π-stacking between adjacent TES ADT-methyl molecules (Figure 3.10e). As a consequence, TES ADT-methyl thin-film transistors exhibit poor charge-carrier mobility.

Overall, both TES ADT-MeO and TES ADT-methyl are not viable organic semiconductors. These results were initially surprising given the 2-D cofacial "bricklayer" crystal packing adopted by TES ADT-methyl and TES ADT-MeO molecules. Upon, closer examination, however, these results are consistent with the small degree of π-stacking present in TES ADT-MeO and TES ADT-methyl thin-films. The MeO- and methyl- substituents disrupt the π-stacking between adjacent molecules (Figure 3.10e). Consequently, the intermolecular π-orbital overlap in TES ADT-MeO and TES ADT-methyl is significantly reduced compared to TES ADT (Figure 3.10b) and TES ADT-F (Figure 3.10d) yielding thin-film transistors that exhibit low charge-carrier mobility.

In summary, we can correlate the thin-film transistor performance of TES ADT and TES ADT derivatives with the degree of π-stacking present in the organic semiconductor thin film. Organic semiconductor thin films of TES ADT-I, TES ADT-Cl, and TES ADT -Br, in which the large size of the halogen substituent causes the crystal packing to shift from a 2-D cofacial "bricklayer" crystal packing to a 1-D

"slipstack" crystal packing with minimal π-orbital overlap all yield thin-film transistors with unremarkable charge-carrier mobility ($\leq 10^{-3}$ $cm^2/V\text{-}s$). TES ADT-MeO and –methyl thin-film transistors also exhibit low charge-carrier mobility because the size of the methoxy and methyl substituents disrupt the π-orbital overlap between neighboring molcecules despite the fact that these molecules retain the 2-D cofacial "bricklayer" crystal packing. In contrast, TES ADT and TES ADT-F, which both adopt 2-D cofacial "bricklayer" crystal packings with 2-D π-orbital overlap, yield thin-film transistors with high charge-carrier mobility (≥ 0.1 $cm^2/V\text{-}s$). The charge-carrier mobility of TES ADT-F thin-film transistors can be further improved with electrode treatment (0.2 ± 0.07 $cm^2/V\text{-}s$). Consequently, TES ADT-F warrants further study as a solution-processable organic semiconductor. Specifically, we intend to examine how dielectric and electrode surface treatments can be used to improve TES ADT-F thin-film transistor performance.

FIGURES:

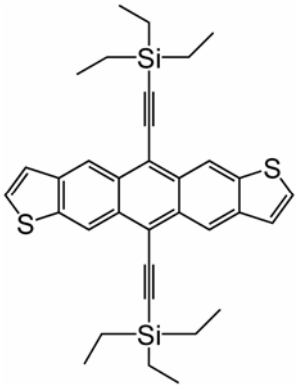

Illustration 3.1 Chemical structure of triethylsilylethynyl anthradithiophene (TES ADT).

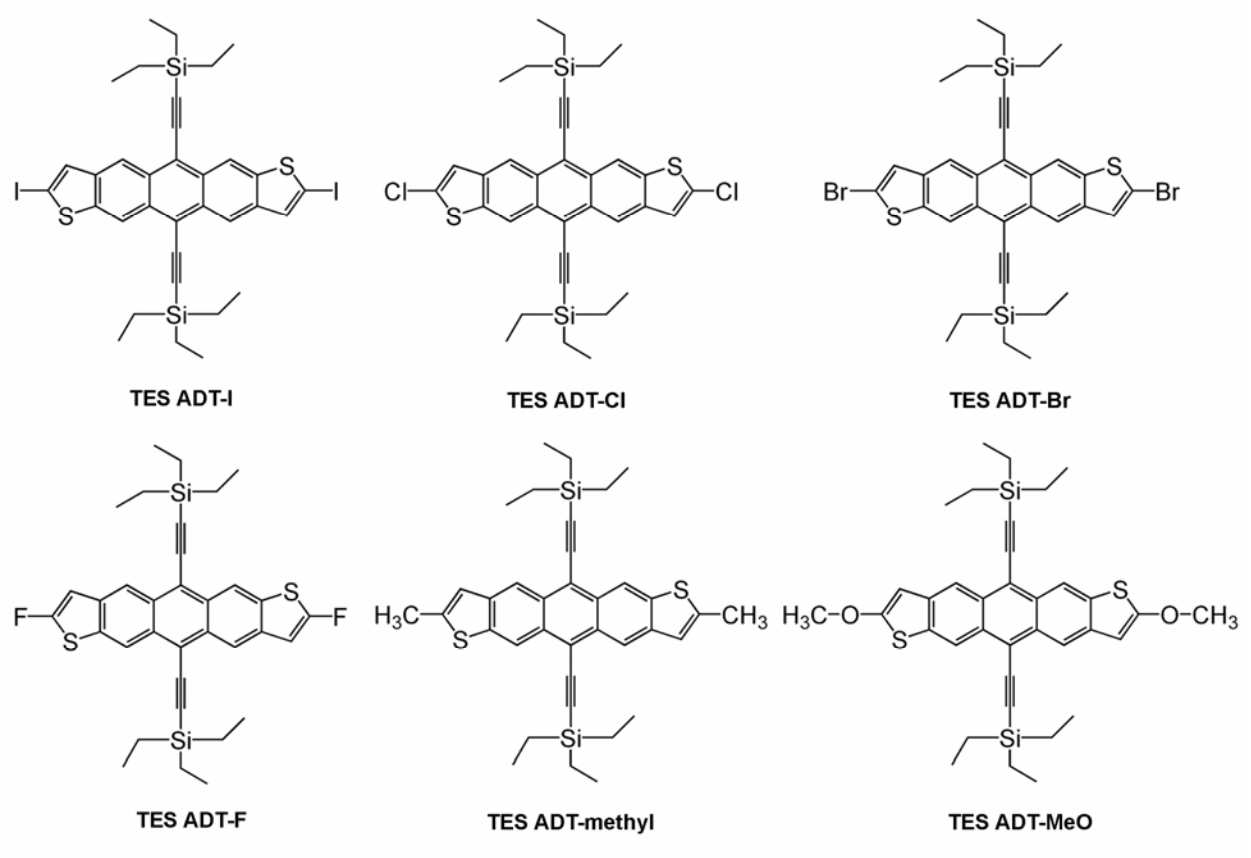

Illustration 3.2 Chemical structures of TES ADT derivatives.

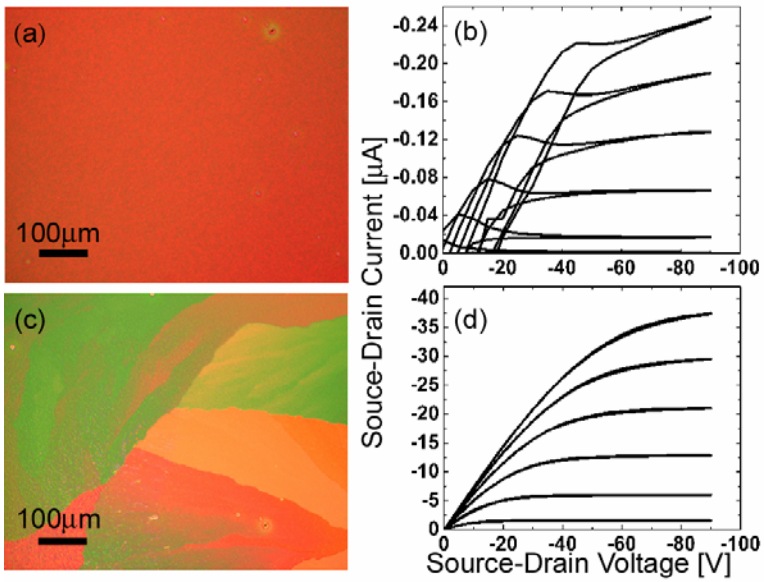

Figure 3.1 (a) Optical microscope image taken in the channel region and (b) the corresponding output characteristics of an as-spun TES ADT thin-film transistor (W/L = 9.5, charge-carrier mobility = 0.002 cm^2/V-s). (c) Optical microscope image of the channel region and (d) the corresponding output characteristics (charge-carrier mobility = 0.2 cm^2/V-s) of the same thin-film transistor after 2 minutes of dichloroethane solvent-vapor annealing. The gate voltage was increased from 0 to -50 V in increments of -10 V during electrical characterization.

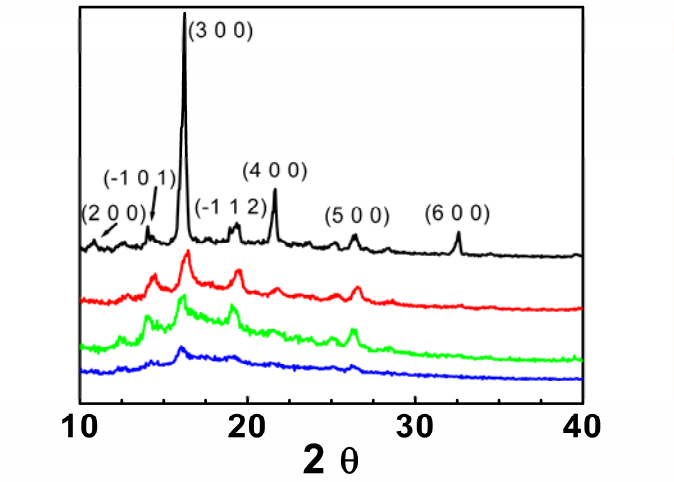

Figure3.2 X-ray diffraction spectra of TES ADT powder (black line) and TES ADT thin-films annealed with dichloroethane vapors (red line), toluene vapors (green line), and acetone vapors (blue line).

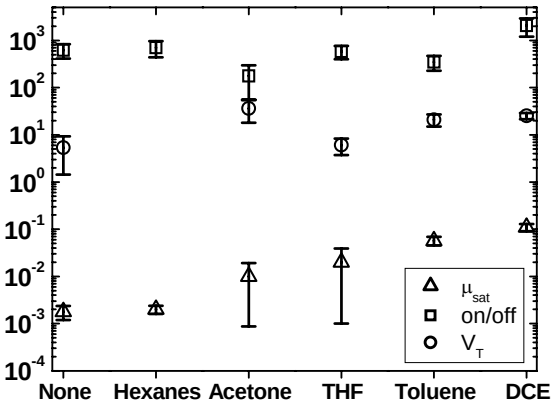

Figure 3.3 Thin-film transistor characteristics after 2 minutes of solvent-vapor annealing. Note: the threshold voltage of thin-film transistors annealed in hexanes vapors is -1.4 ± 3.2V.

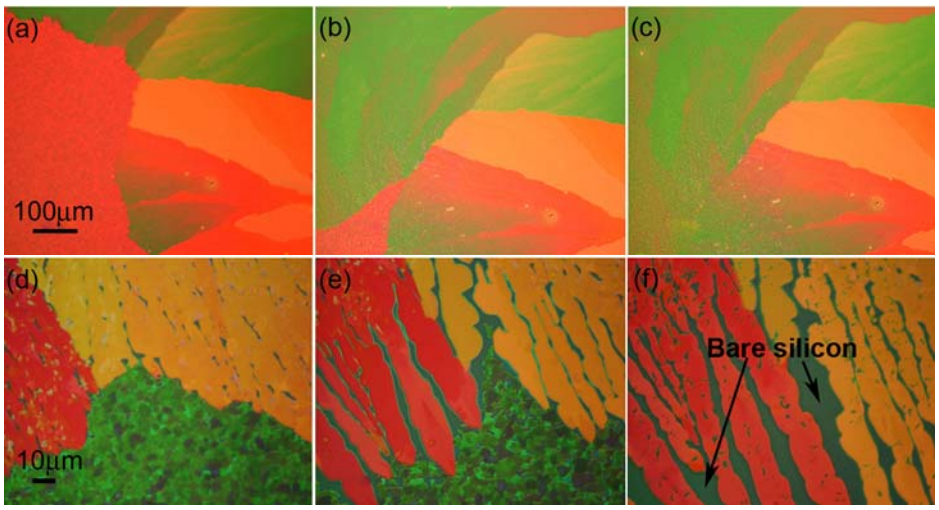

Figure 3.4 Optical microscope images of TES ADT at different time points of solvent-vapor annealing. TES ADT films (a) after 1min, (b) 2 min, and (c) 10min exposure to dichloroethane vapors. (d) After 1min, (e) 2 min, and (f) 10 min exposure to toluene vapors. Large and continuous crystalline domains develop quickly in films annealed with dichloroethane vapors. Toluene-vapor annealing also induces rapid grain growth, but this is accompanied by dewetting.

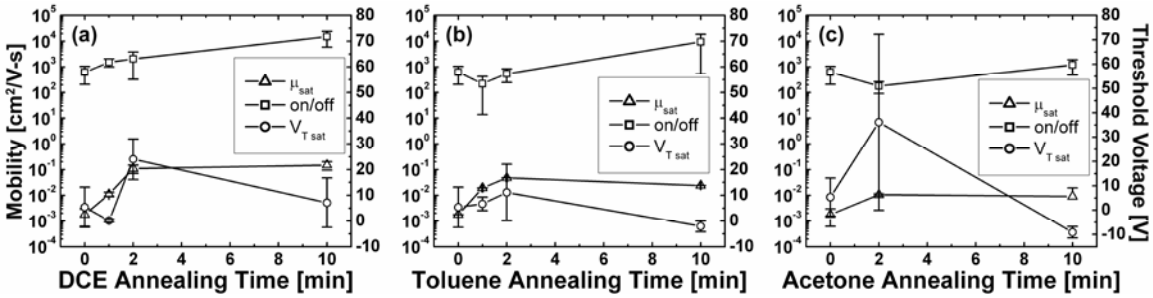

Figure 3.5 Device characteristics as a function of annealing time in (a) dichloroethane vapors, (b) toluene vapors, and (c) acetone vapors.

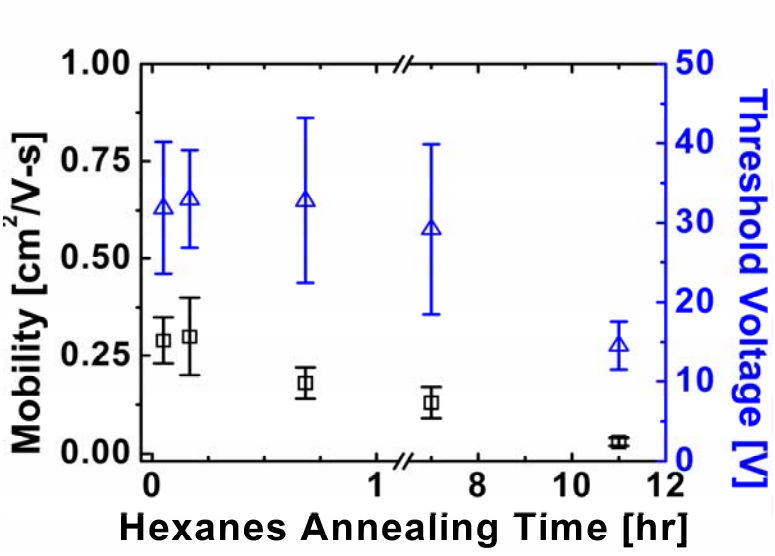

Figure 3.6 Variation of the output characteristics of a dichloroethane vapor-annealed TES ADT thin-film transistor that is subsequently subjected to a hexanes solvent-vapor annealing step.

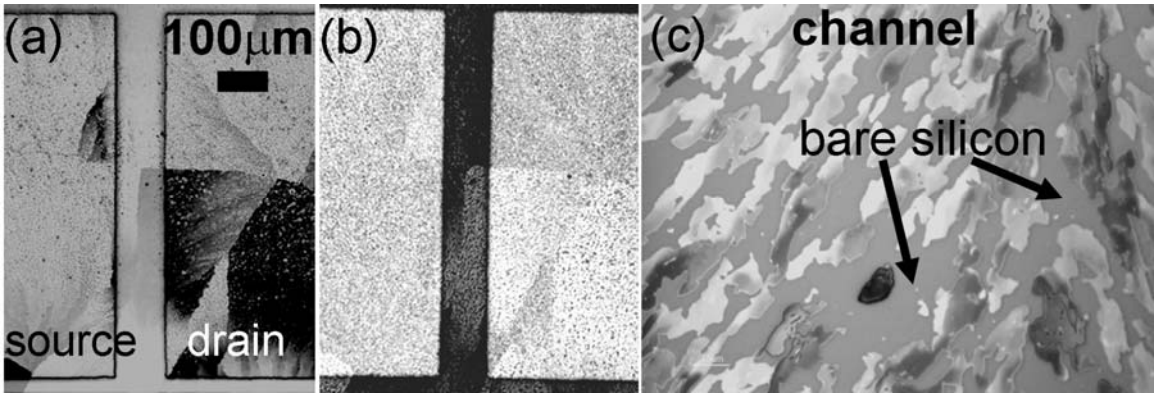

Figure 3.7 Optical microscope images of dichloroethane vapor-annealed TES ADT thin-film transistor (a) before and (b) after 7 hours of hexanes vapor annealing. (c) Magnified view of the channel after hexanes vapor annealing illustrates the severity of the TES ADT dewetting as large regions of bare silicon are visible.

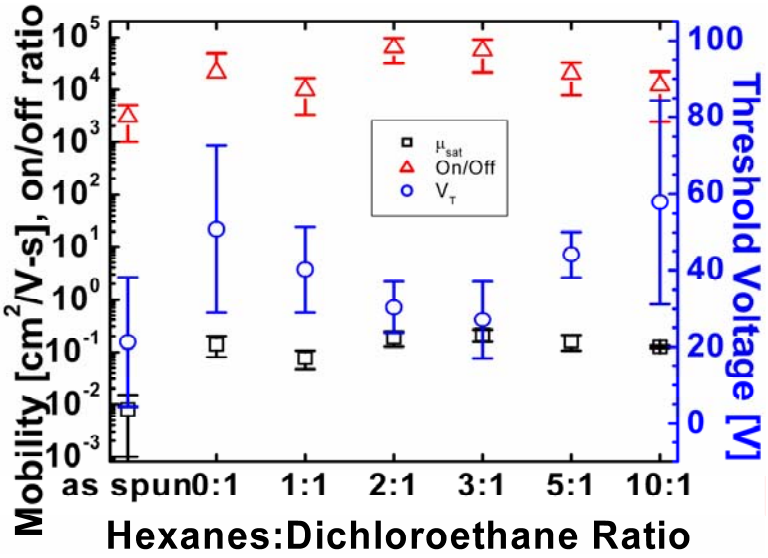

Figure 3.8 Variation of TES ADT thin-film transistor output characteristics with annealing solvent composition in the liquid phase.

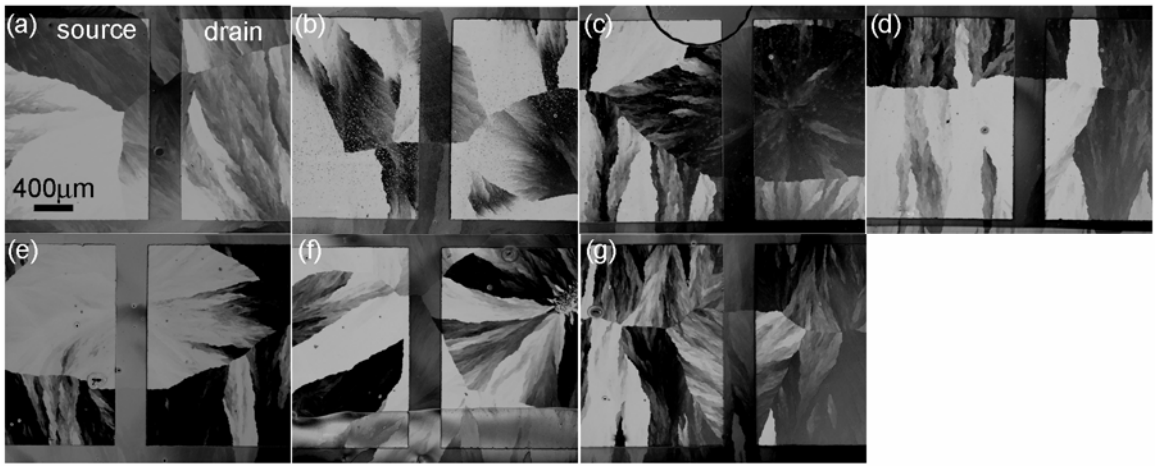

Figure 3.9 Optical microscope images of TES ADT thin-film transistors annealed in solvent vapors of mixed composition: (a) pure 1,2-dichloroethane (DCE), (b) 1:1 (v:v) mixture of hexanes and DCE, (c) 2:1 (v:v) mixture of hexanes and DCE, (d) 3:1 (v:v) mixture of hexanes and DCE, (e) 5:1 (v:v) mixture of hexanes and DCE, (f) 10:1 (v:v) mixture of hexanes and DCE, and (g) 15:1 (v:v) mixture of hexanes and DCE. All the volume ratios refer to liquid phase solvent mixtures.

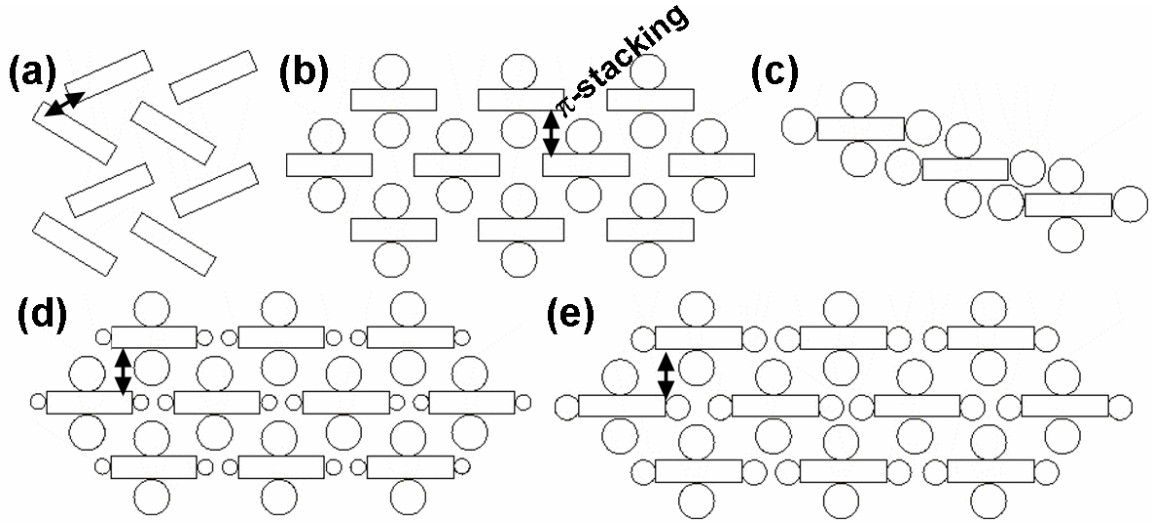

Figure 3.10 Representation of crystal packings typically adopted by organic semiconductors. (a) Herringbone crystal packing (b) 2-D cofacial bricklayer packing with strong π-orbital overlap adopted by TES ADT, (c) 1-D slip-stack crystal packing with no π-orbital overlap adopted by TES ADT-I, TES ADT-Cl and TES ADT-Br, (d) 2-D cofacial bricklayer packing with strong π-orbital overlap adopted by TES ADT-F, and (e) 2-D cofacial bricklayer packing adopted by TES ADT-MeO and TES ADT-methyl with minimal π-orbital overlap. In the cartoons, the rectangle represents the anthradithiophene backbone and the circles represent the TES, halogen, methoxy and methyl substituents.

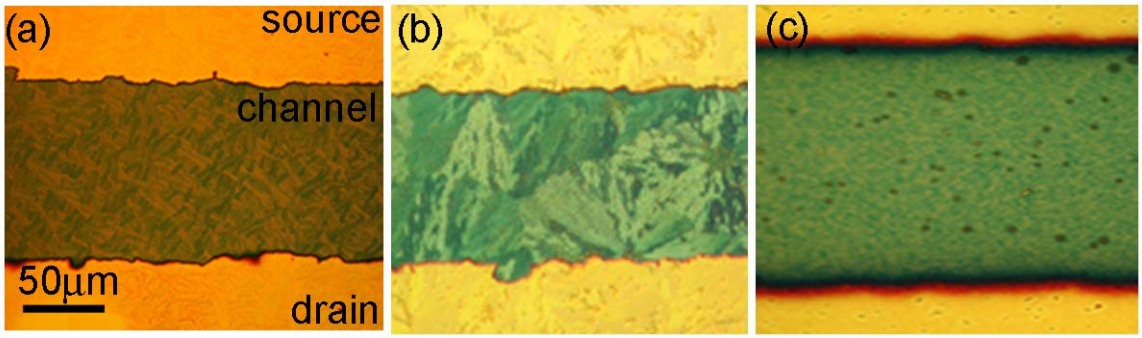

Figure 3.11 Optical microscope images of the channel region of an (a) as-spun TES ADT-I thin-film transistor, (b) of the same TES ADT-I thin-film transistor annealed over chloroform vapors, and (c) of an as-spun TES ADT-Br thin-film transistor.

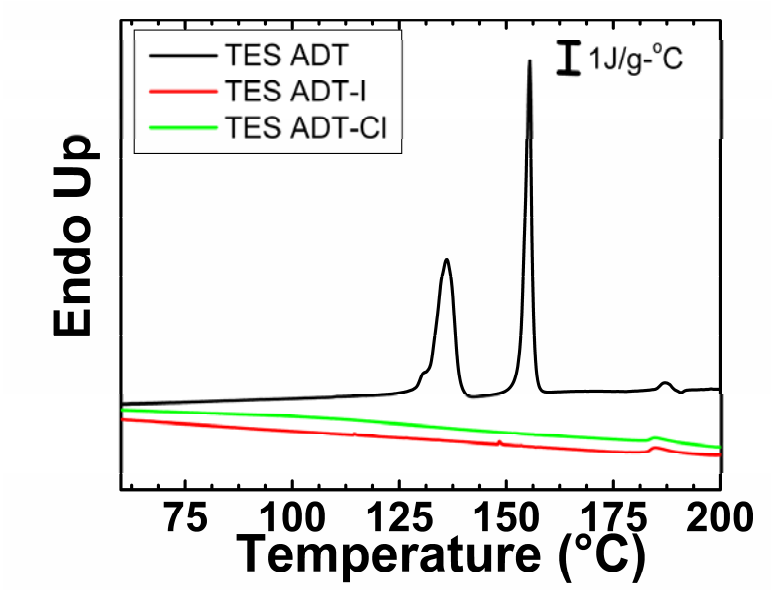

Figure 3.12 Differential scanning calorimetry of TES ADT (black line), TES ADT-I (red line) and TES ADT-Cl (green line). In sharp contrast to TES ADT, neither TES ADT-I or TES ADT-Cl showed significant crystallinity.

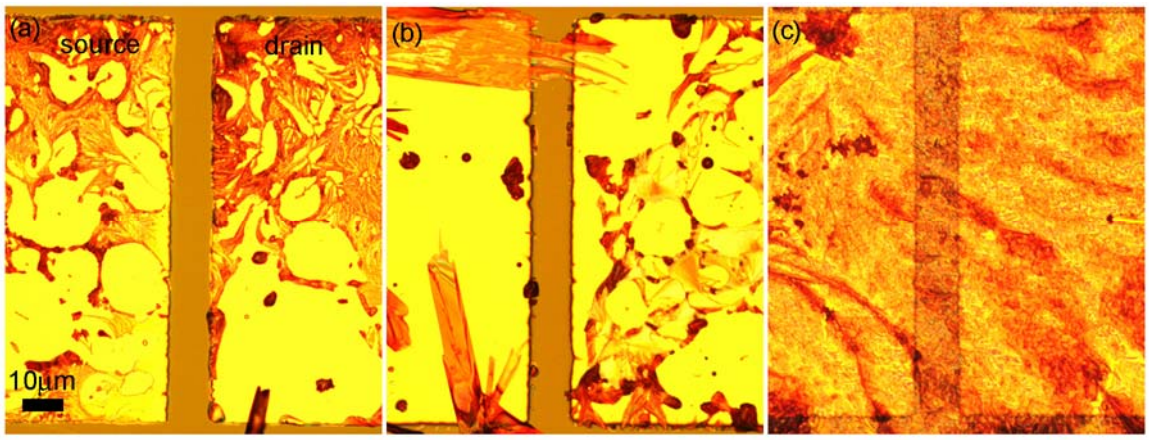

Figure 3.13 Optical microscope images of the channel regions of thin-film transistors with (a) drop cast TES ADT-I, (b) drop cast TES ADT-Br, and (c) drop cast TES ADT-Cl.

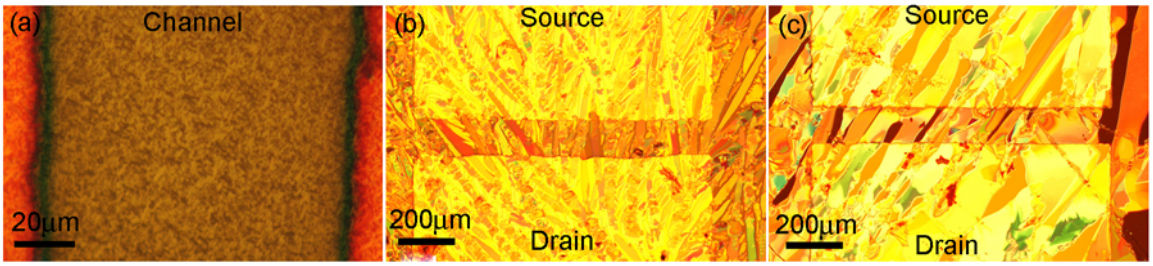

Figure 3.14 Optical microscope images of the channel region of thin-film transistors with (a) as-spun TES ADT-F, (b) drop cast TES ADT-F, and (c) drop cast TES ADT-F on PFBT treated gold electrodes.

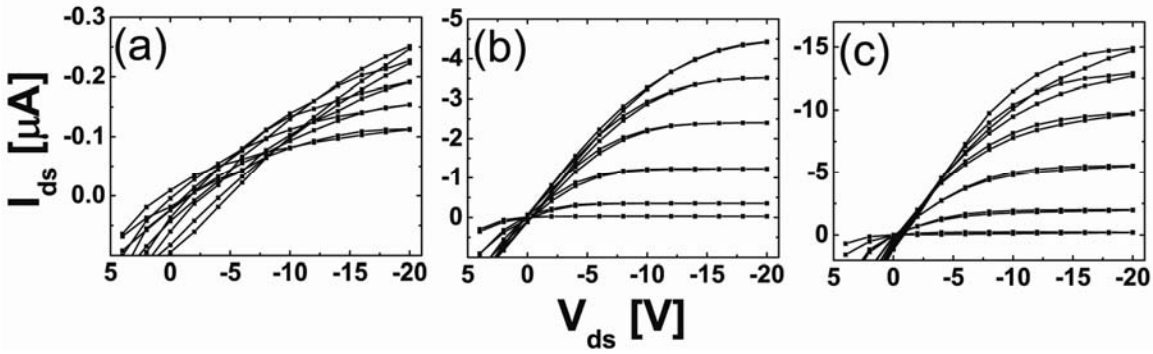

Figure 3.15 Typical current-voltage characteristics of TES ADT-F thin-film transistors with (a) as-spun TES ADT-F, (b) drop cast TES ADT-F, and (c) TES ADT-F drop cast on PFT treated gold electrodes. For all transistors L = 100 μm, W = 1000 μm.

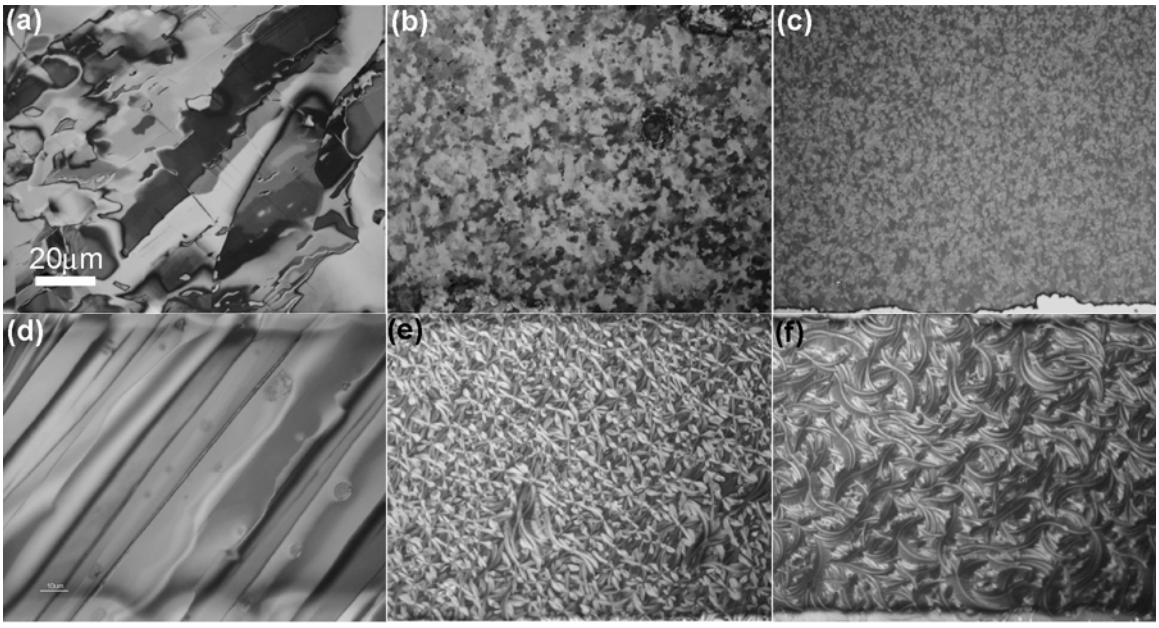

Figure 3.16 Optical microscope images of the channel region of (a) drop cast TES ADT-MeO, (b) spun cast TES ADT-MeO, (c) blade cast TES ADT-MeO, (d) drop cast TES ADT-methyl, (e) spun cast TES ADT-methyl and (f) blade cast TES ADT-methyl thin-film transistors.

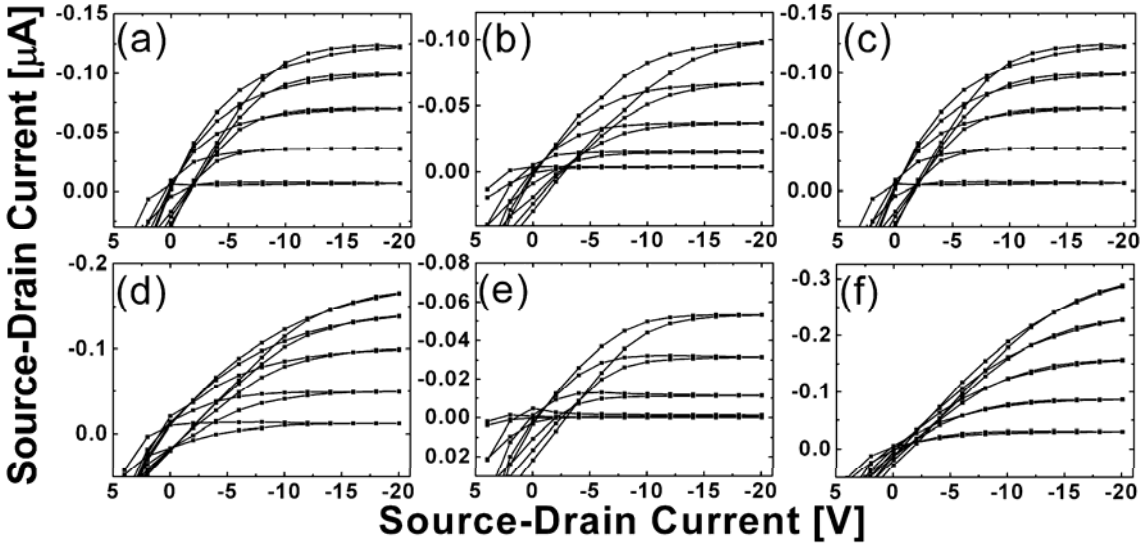

Figure 3.17 Typical current-voltage characteristics of (a) drop cast TES ADT-MeO, (b) spun cast TES ADT-MeO, (c) blade cast TES ADT-MeO, (d) drop cast TES ADT-methyl, (e) spun cast TES ADT-methyl and (f) blade cast TES ADT-methyl thin-film transistors. For all transistors L = 100 μm, W = 1000 μm.

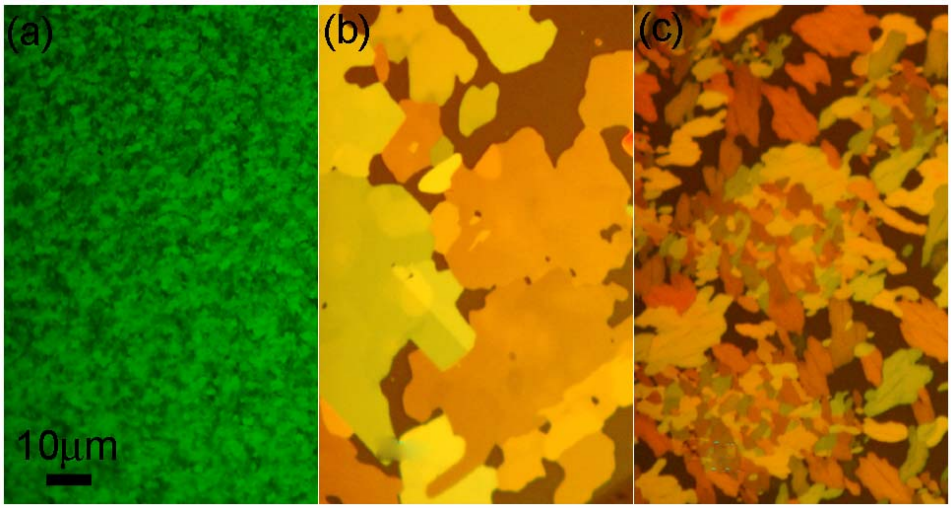

Figure 3.18. Optical microscope images of TES ADT-MeO thin films: (a) as-spun, (b) after annealing in carbon disulfide vapors, and (c) after annealing in chloroform vapors.

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Chapter 4: Making Electrical Contact to Solution-Processable Triethylsilylethynyl Anthradithiophene

In addition to the materials properties of organic semiconductors themselves, thin-film transistor geometry and the manner in which electrical contact is established to organic semiconductors play critical roles in thin-film transistor performance. Thin-film transistors can be classified as top-contact or bottom-contact devices depending on where the electrodes make contact with the organic semiconductor film. Both geometries are depicted in Figure 1.1. In the bottom-contact geometry, the source and drain electrodes are deposited directly on the dielectric layer. The organic semiconductor is then subsequently deposited on top of both the electrodes and the exposed dielectric layer. In the top-contact geometry, the organic semiconductor is deposited directly on the dielectric layer. This results in a more uniform organic semiconductor thin film compared to the organic semiconductor thin film in the bottom-contact geometry. The top-contact transistor is completed by subsequently depositing the source and drain electrodes on top of the organic semiconductor layer. Consequently, top-contact transistors typically have fewer defects at the electrode/semiconductor interface and exhibit enhanced electrical properties compared to bottom-contact transistors.[1-4]

Often, the transistor geometry dictates how the source and drain electrodes are patterned in thin-film transistors. In bottom-contact transistors, the source and drain electrodes can be patterned by either direct evaporation/sputtering through a shadow mask or photolithography and lift-off. In top-contact transistors, the source and drain electrodes are typically patterned by direct evaporation/sputtering through a shadow mask since photolithography is generally not compatible with organic semiconductors.[5] Direct evaporation through a shadow mask is the most straightforward way of making electrical contact to both top- and bottom-contact organic thin-film transistors. This technique

requires a stencil or shadow mask, typically cut from a thin sheet of metal, to be contacted against the substrate. A blanket coating of metal is then deposited on the substrate by evaporation or sputtering. The metal only reaches the substrate surface in the regions not protected by the shadow mask. The biggest limitation of direct evaporation through a shadow mask is the feature resolution - the smallest feature that can be reliably drilled into the shadow mask is limited to 25 – 30 μm. To achieve smaller feature sizes, photolithography and lift-off are typically used. With photolithography and lift-off, the substrate surface is patterned with photoresist by standard photolithography procedures.[6] A blanket coating of metal is then deposited on the entire substrate by evaporation or sputtering. Following metal deposition, the substrate is soaked in an appropriate solvent to remove the remainder of the photoresist. As the photoresist dissolves, the overlaying metal layer 'lifts off' the substrate; metal only remains in the areas that was not originally covered with photoresist. While photolithography and lift-off is capable of generating very small features (≥ 1 μm), its application is generally limited to bottom-contact transistor geometry due to an inherent incompatibility between organic semiconductors and the photolithography processing conditions.

Since the goal of our study was to compare how TES ADT performs in top- and bottom-contact transistors geometries, we used direct evaporation through a shadow mask to fabricate gold source and drain electrodes of the same geometry and dimensions for top- and bottom-contact thin-film transistors. Since the processing of the gold source and drain electrodes was the same for top- and bottom-contact transistors, any differences in thin-film transistor performance must stem from the organic semiconductor. We built our thin-film transistors on a silicon/silicon dioxide platform. The highly-doped silicon served as a common gate electrode for all of the transistors on the same chip and the 100 nm thermally-grown silicon dioxide layer served as a gate dielectric. For bottom-contact

transistors, gold source and drain electrodes were defined on the silicon dioxide surface using e-beam evaporation through a shadow mask. The silicon substrate with freshly-evaporated electrodes was then placed in the UV/Ozone chamber for 10 minutes. TES ADT solution (2 wt% in toluene) was directly spin-coated on the UV/Ozone cleaned substrate. Following a short (2 minutes) bake at 90˚C to remove any residual toluene, the TES ADT thin-film transistors were annealed in a 1,2-dichloroethane solvent-vapor environment until the TES ADT film completely crystallized (2 – 10 minutes). See chapter 3 for additional details on the solvent-vapor annealing process. For top-contact transistors, the highly-doped silicon substrate was placed in the UV/Ozone chamber for 10 minutes. Following UV/Ozone cleaning, TES ADT solution (2 wt% in toluene) was directly spin-coated and annealed in a dichloroethane solvent-vapor environment as described for the bottom-contact devices. Gold source and drain electrodes were then deposited directly on top of the crystallized TES ADT film by e-beam evaporation through the same shadow mask used to define the electrodes for the bottom-contact devices at a rate of 1 angstrom/sec or 10 angstrom/sec. Before characterizing the top- and bottom-contact TES ADT thin-film transistors electrically, individual transistors were isolated by scratching through the TES ADT film with a razor blade to minimize leakage currents.

Figures 4.1a-c show output characteristics for a bottom-contact transistor, a top-contact-transistor with gold electrodes evaporated at 10 angstroms/sec, and a top-contact transistor with gold electrodes evaporated at 1 angstrom/sec, respectively. For all transistor geometries, the thickness of the gold electrodes was 40 nm. The bottom-contact transistor performs as expected, exhibiting a charge-carrier mobility of 0.2 cm^2/V-s and virtually no current-voltage hysteresis (Figure 4.1a). We were surprised, however, by the output characteristics of the top-contact transistors. Contrary to

expectations, the top-contact transistor actually underperforms the bottom-contact transistor. Further, the performance of the top-contact transistor appears to be correlated with the gold evaporation rate. At a gold evaporation rate of 10 angstroms/sec, we observe non-linear behavior in the linear regime of the current-voltage characteristics (Figure 4.1b), and an order of magnitude decrease in the on-currents and charge-carrier mobility (0.08 cm^2/V-s) compared to the bottom-contact transistor (Figure 4.1a). The performance of the top-contact transistor further degrades when the gold electrodes are evaporated at a slower rate of 1 angstrom/sec. In fact, this top-contact transistor does not show any significant field-effect behavior (Figure 4.1c). Further, the yield of functioning devices with electrodes that were evaporated at 1 angstrom/sec is extremely low; only a few transistors showed field dependence characteristics for a given chip containing approximately 100 transistors. Of the devices that do exhibit field effect, the current-voltage characteristics are not different from those shown in Figure 4.1c. The statistics for all of the transistors we tested are summarized in Table 4.1. Overall, the top-contact transistor charge-carrier mobility is not higher than the bottom-contact transistor charge-carrier mobility regardless of the gold evaporation rate. Optical microscope images of a bottom-contact transistor and a top-contact transistor with gold evaporated at 10 angstrom/sec are shown Figures 4.2a and b, respectively. From these images we cannot explain why the top-contact transistor performs so poorly. The annealed TES ADT film appears to be crystalline in both channel regions with large grains spanning the length of the transistor channels.

Table 4.1. Summary of device characteristics of TES ADT thin-film transistors comparing top- and bottom-contact transistor geometry. In all transistors L = 100 μm, W = 1000μm.

Transistor Geometry	# TFTs	Gold Evap. Rate	Charge-Carrier Mobility (cm^2/V-s)	Threshold Voltage (V)	On/Off Current Ratio
Bottom-contact, direct evaporation	121	–	0.11 ± 0.05	4.3 ± 6.0	10^4
Bottom-contact, photolithography & lift-off	13	–	0.04 ± 0.01	2.1 ± 1.1	10^3
Top-contact, direct evaporation	29	10 Å/s	0.07 ± 0.03	-1.6 ± 3.4	10^4
Top-contact, direct evaporation	16	1 Å/s	0.03 ± 0.02	-2.4 ± 3.5	10^3
Top-contact, lamination	39	–	0.19 ± 0.06	0.3 ± 1.9	10^3

To determine if the gold evaporation was damaging the TES ADT film, we characterized the TES ADT film before and after gold evaporation by x-ray diffraction (XRD). The TES ADT film was spin coated and annealed on a silicon/silicon dioxide substrate to simulate the channel region in transistors. After collecting the diffraction spectra of the annealed TES ADT film, 40 nm of gold were deposited on top of the annealed TES ADT film by e-beam evaporation at 1 angstrom/sec. The diffraction spectra were recollected on the annealed TES ADT film without removing the overlying gold. These results are shown in Figure 4.3. The annealed TES ADT thin film before gold evaporation (black line) is crystalline; we observe diffraction peaks associated with the (100), (200), (300), etc., planes of the lattice. We also observe a peak at $2\theta \sim 33^\circ$ that corresponds to the (200) plane of the underlying single-crystal silicon substrate.[7] After evaporating 40 nm of gold onto the same annealed TES ADT film, we observe the same Bragg diffraction peaks and we do not detect a discernable shift in the diffraction peak positions or a broadening of the diffraction peaks (red line). A new peak at $2\theta \sim 38.3^\circ$ is

observed; it corresponds to the (111) plane of the overlying gold.[8] These results indicate that the crystal structure of the TES ADT thin film remains unchanged after gold evaporation.

Since both optical microscopy and x-ray diffraction reveal that the morphology and structure of TES ADT is not affected by the gold evaporation, we looked for evidence of chemical degradation or oxidation of TES ADT by x-ray photoelectron spectroscopy (XPS). We conducted XPS experiments on the TES ADT film before and after gold evaporation. In order to detect the TES ADT signal through the evaporated gold, only 2 nm of gold were deposited on the annealed TES ADT film. High-resolution elemental scans were collected for carbon, sulfur, silicon and oxygen. If oxidation or any other chemical degradation occurred during gold evaporation, we should observe peak broadening, peak shifts, or the emergence of new peaks that were not present in the original annealed TES ADT spectra. The XPS spectra for carbon, sulfur, and silicon before and after gold evaporation are shown in Figure 4.4. We did not observe any peaks in the oxygen spectra before or after gold evaporation, so the oxygen spectra are not shown. Based on the chemical structure of TES ADT, oxygen should not be present in the annealed TES ADT film. The fact that oxygen is not present in the TES ADT film after gold evaporation indicates the gold evaporation is not causing oxidation in the TES ADT film. We can also rule out degradation or chemical modification of TES ADT with gold evaporation as the shapes and positions of the carbon, sulfur, and silicon peaks are unchanged before and after gold evaporation. The most significant difference between the two sets of data is the attenuation of the peak intensities due to an increase in the photoelectron path length because of the presence of 2nm of overlying gold. Combining the results from XRD and XPS, we conclude that gold evaporation is not affecting the crystal structure or chemical integrity of the bulk of the TES ADT film. Instead, the gold

evaporation must have a localized effect on the TES ADT directly underneath the evaporated gold. This is in fact what we observe when we characterize the TES ADT film by atomic force microscopy (AFM). Figure 4.5 contains images of the TES ADT film before gold evaporation, the TES ADT film directly underneath the evaporated gold (the gold was peeled away with scotch tape before imaging), and the TES ADT film protected by a shadow mask during the gold evaporation. Comparing the annealed TES ADT film before (Figures 4.5a and d) and after (Figures 4.5b and e) gold evaporation, we observe that the TES ADT film directly underneath the evaporated gold has been damaged during the evaporation. Specifically the TES ADT morphology underneath the gold appears pitted. This observed pitting does not, however, increase the roughness of the TES ADT thin film. At the slower evaporation rate of 1 angstrom/sec, the TES ADT directly underneath the gold is actually about 1 nm less rough than the annealed TES ADT. Further, this pitting is observed with gold evaporation rates of 1 angstrom/sec and 10 angstroms/sec (Figures 4.5b and e). The TES ADT film protected by the shadow mask during the gold evaporation (Figures 4.5c and f), however, appears the same as the film before gold evaporation (Figures 4.5a and d). These images suggest that the gold evaporation can damage the TES ADT film locally in the regions that are directly exposed.

Our results are not the first evidence of gold evaporation causing damage to organic thin films.[9-11] A recent report by Cho and coworkers[9] has shown that the rate at which gold is directly evaporated on a crystalline pentacene film can affect thin-film transistor performance. The authors compared two sets of top-contact pentacene thin-film transistors. In one set of devices, gold electrodes were deposited at 0.2 angstroms/sec, and in the other set of devices, gold electrodes were deposited at 7 angstroms/sec. Similar to the trends we observed with TES ADT, the slower gold

evaporation rate yielded pentacene transistors with reduced charge-carrier mobility and increased contact resistance. It is important to note that although Cho and coworkers detect a reduction in charge-carrier mobility with a slow gold evaporation rate, the charge-carrier mobility of their top-contact pentacene transistors is still higher than the average charge-carrier mobility of bottom-contact pentacene transistors. In our TES ADT thin-film transistors, the charge-carrier mobility of our bottom-contact TES ADT thin-film transistors is in all cases equivalent or better than the charge-carrier mobility of our top-contact TES ADT thin-film transistors.

We suspect the differences mentioned above stem from the way in which the evaporated gold interacts with the organic semiconductor thin film on contact. In our system gold evaporation likely causes localized melting of TES ADT (T_m = 155.3˚C) when highly energetic gold atoms make contact. This localized melting disrupts charge injection/extraction at the organic semiconductor/electrode interfaces in the resulting devices thereby reducing device performance. We have performed differential scanning calorimetry (DSC) experiments, shown in Figure 4.6, that indicate that TES ADT is thermally unstable; once it melts, it is difficult to recrystallize. In these experiments, TES ADT was heated from 50˚C to 200˚C at 10˚C/min. We observed two transitions on the first heat: a broad peak at 136.2˚C and a narrow, sharp peak at 155.3˚C. After quickly cooling to 50˚C, the TES ADT was heated from 50˚C to 200˚C again. On the second heat, no transitions were observed. Attempts to recrystallize TES ADT by thermally annealing at 152˚C (overnight) and 105˚C (for 90 minutes) were unsuccessful. Additionally, we tried to recrystallize the TES ADT with controlled cooling. Cooling rates of 5˚C/min and 2˚C/min were unsuccessful, however, a rate of 1˚C/min allowed successful recrstallization of TES ADT (crystallization occurred at 100˚C). That TES ADT only recrystallizes under well-controlled conditions indicates that if the gold

evaporation is causing localized melting, it is unlikely that the TES ADT will recrystallize during the gold evaporation process. The fact that we do not detect a significant reduction in crystallinity with XRD indicates that the melted regions are a minor component of the TES ADT film.

To further characterize how this localized melting affects the performance of TES ADT thin-film transistors, we conducted scanning surface potential measurements (SSPM) on the bottom- and top-contract transistors in collaboration with Timothy J. Smith in Professor Keith Stevenson's group in the Department of Chemistry and Biochemistry at the University of Texas at Austin. SSPM allows us to collect complimentary topography and surface potential data across the electrodes, electrode/channel interfaces, and the channel of the thin-film transistor while the transistor is operating. We collected surface potential data in the linear regime (Vds = -2V) as a function of gate voltage (varied from 0V to -20V, -4V increments). In the linear regime the potential drop across the channel should be linear with distance.[12] Further, if the contact resistance is significant in the organic thin-film transistor, it can dominate the channel resistance in the linear regime, hindering charge injection and charge extraction at the source and drain electrodes, respectively. Consequently, high contact resistance limits the measured charge-carrier mobility of the thin-film transistor.[13]

Our SSPM results for top- and bottom-contact TES ADT thin-film transistors are shown in Figure 4.7. We only observe surface potential drops at the source and drain electrodes, indicating that contact resistance does exist in our devices. Further, the potential drop at the source and drain electrodes is significantly smaller in the bottom-contact transistor (Figure 4.7a, bottom) than in the top-contact transistor (Figure 4.7b, bottom), indicating that charge injection and charge extraction are less efficient in the top-contact transistor. Using ohm's law (Equation 4.1) we can extract the channel

resistance and the contact resistance at the organic semiconductor/source and organic semiconductor/drain interfaces from the measured potential drop across the respective interfaces.

$$R_{source/drain} = \frac{\Delta V_{source/drain}}{I} \qquad \text{(Equation 4.1)}$$

Where $R_{source/drain}$ is the contact resistance at the source or drain electrode, $\Delta V_{source/drain}$ is the potential drop at the organic semiconductor/source or organic semiconductor/drain interface and I is the source-drain current measured simultaneously. The channel and contact resistances we calculated for the bottom- and top-contact transistors are summarized in Table 4.2. Since gold evaporation does not affect the TES ADT film in the channel, we expect the channel resistance to be comparable in both transistors. Quantification of the channel resistances in both devices indicate that this is in fact the case (~1 x 10^6 Ω). We do expect, however, a significant difference in the contact resistances at the organic semiconductor/electrode interfaces based on the differences in device performance between the top- and bottom-contact transistors. In fact, the contact resistance at both the source and drain electrodes is an order of magnitude higher in the top-contact transistor than in the bottom-contact transistor (Table 4.2). This result contradicts previous literature reports which show that bottom-contact transistors exhibit higher contact resistance than top-contact transistors.[14, 15] That we measure a higher contact resistance in the top-contact TES ADT thin-film transistor is consistent with our AFM data which suggests that gold evaporation causes localized damage to the TES ADT film immediately beneath the gold layer. Since the gold evaporation causes defects in the TES ADT film right at the organic semiconductor/electrode interfaces, charge extraction and injection are more hindered in the top-contact transistor, as evidenced by the increased contact resistance at the source and drain electrodes.

Table 4.2. Channel and contact resistances in bottom- and top-contact TES ADT thin-film transistors.

Transistor Geometry	$R_{channel}$	R_{source}	R_{drain}
Bottom-contact	9.6×10^5 Ω	3.5×10^5 Ω	2.4×10^5 Ω
Top-contact	1.1×10^6 Ω	6.6×10^6 Ω	3.6×10^6 Ω

To show that the decreased transistor performance is directly attributed to the gold evaporation rather than differences in the organic semiconductor film quality due to differences in transistor geometry, we built top-contact transistors by soft-contact lamination.[16-19] With this technique, shown in Figure 2.4, the TES ADT semiconductor is spun and annealed on silicon dioxide in the exact manner as discussed previously for top-contact transistors by direct evaporation. Gold contact pads are deposited by e-beam evaporation along the exterior of the annealed TES ADT film. Source and drain electrodes of analogous geometry and dimensions are fabricated independently on a patterned PDMS stamp. Titanium (2nm) and gold (15-18 nm) are deposited onto a PDMS stamp by e-beam evaporation. The titanium and gold fluxes are perpendicular to the PDMS stamp to ensure that the metal deposition is on the raised and recessed regions of the stamp, and not on the sidewalls, resulting in electrically isolated gold electrodes. Prior to depositing metal on the patterned PDMS stamp, the PDMS is subjected to an 8 minute UV/Ozone treatment. The UV/Ozone treatment activates the PDMS surface so that the evaporated titanium and gold layers permanently adhere to the PDMS stamp.[16] Contacting the gold-coated PDMS stamp non-destructively against the annealed TES ADT film completes the transistor (Figure 4.2c). The PDMS-supported gold source and drain electrodes also contact the gold contact pads along the exterior of the annealed TES ADT film. The contact pads allow us to measure the current-voltage characteristics of the laminated top-contact transistors without directly probing the electrodes on the PDMS

stamp (the flexible nature of PDMS makes it extremely difficult to directly make electrical contact with metal films supported by PDMS without puncturing through the metal film). The mechanical properties of the PDMS allow conformal contact to be established between the gold electrodes and the TES ADT thin film with minimal external pressure when brought together. This process is reversible; the gold-coated stamps can be removed from the substrate without damaging the organic semiconductor thin film. Multiple gold-coated stamps can be contacted against the same substrate in this manner. Typical current-voltage characteristics of a laminated, top-contact transistor are shown in Figure 4.1d. This transistor exhibits higher on currents and charge-carrier mobility (0.24 cm^2/V-s) compared to top-contact thin-film transistors with gold electrodes defined by direct evaporation and bottom-contact transistors with equivalent channel dimensions. The average device characteristics for each transistor geometry and fabrication technique, i.e., bottom-contact geometry, top-contact geometry by direct evaporation and top-contact geometry by lamination, are summarized in Table 4.1 for comparison. That top-contact transistors with directly evaporated electrodes underperform their bottom-contact counterparts while top-contact transistors with laminated electrodes outperform their bottom-contact counterparts clearly emphasizes that it is the manner in which the electrodes are fabricated and patterned that is critical to achieving optimal transistor performance. Further, these results indicate that standard methods for making electrical contacts to inorganic semiconductors are not always suitable for making contact to organic semiconductors.

Another example that demonstrates this last point involves the fabrication of bottom-contact TES ADT thin-film transistors with gold electrodes patterned by photolithography and lift-off. To define gold electrodes in bottom-contact transistors by photolithography requires that the silicon dioxide surface be treated with an adhesion

promoter, such as hexamethyldisilazane (HMDS), to prevent the undeveloped photoresist from releasing from the silicon dioxide surface during pattern development. HMDS-treated silicon dioxide surfaces, however, are not compatible with TES ADT solution processing. When TES ADT is deposited on HMDS-treated silicon dioxide surfaces, it balls up and does not form a continuous thin film. TES ADT forms the highest quality thin films on high surface energy surfaces like UV/Ozone cleaned silicon dioxide. Removal of the HMDS layer is not straightforward, as piranha (mixture of 70 v/v% sulfuric acid and 30 v/v% hydrogen peroxide) and UV/Ozone cleaning do not completely remove HMDS from the silicon dioxide surface. To demonstrate the consequences of incomplete HMDS removal, we built two sets of bottom-contact thin film transistors. In the first set of transistors, the electrodes were patterned by direct evaporation through a shadow mask. In the second set of transistors, the electrodes were patterned by photolithography and lift-off. The electrode dimensions were identical in both sets of transistors. After patterning the electrodes, both sets of transistors were subjected to piranha cleaning followed by 10 minutes of UV/Ozone cleaning. Following the UV/Ozone treatment, TES ADT solution (2 wt% in toluene) was spin coated on both sets of electrodes and annealed in dichloroethane vapors until TES ADT crystallized. Optical microscope images of the resulting TES ADT films are shown in Figure 4.8. From these images it is clear that the grain size of the annealed TES ADT film in the bottom-contact transistor with electrodes evaporated through a shadow mask (on the order of 1 mm; Figure 4.8a) is much larger than the grain size of the annealed TES ADT film in the bottom-contact transistor with electrodes defined by photolithography and lift off (on the order of 100 – 300 μm; Figure 4.8b). The differences in grain size manifest themselves in the device characteristics which are summarized in Table 1 – the charge-carrier mobility of the bottom-contact transistors with electrodes evaporated through a shadow

mask is twice as high as the charge-carrier mobility of the bottom-contact transistors with electrodes patterned by photolithography and lift-off. We attribute the difference in grain size and charge-carrier mobility to the presence of residual HMDS from the photolithography patterning process. Although the piranha and UV/Ozone cleaning remove enough of the HMDS layer to allow TES ADT to form a continuous film, the silicon dioxide surface after photolithography and lift-off is not equivalent to the silicon dioxide surface that was not treated with HMDS. These results clearly indicate that processing history is not completely erased through standard cleaning procedures and that this processing history can have a dramatic effect on thin-film transistor performance.

To summarize our results on making electrical contact to organic semiconductors, we have shown that the manner in which the electrodes are patterned is extremely important to achieving optimal device performance. Traditional patterning techniques for making top-contact transistors by direct evaporation through a shadow mask, and bottom-contact transistors by photolithography and lift-off do not yield the best performing TES ADT transistors. Contrary to expectations, top-contact TES ADT thin-film transistors with electrodes defined by direct evaporation through a shadow mask actually underperform bottom-contact TES ADT thin-film transistors with electrodes defined by direct evaporation through a shadow mask. We observe this surprising result because the direct evaporation of gold on crystalline TES ADT thin films induces local melting that increases the contact resistance at the organic semiconductor/electrode interface. The increased contact resistance hinders charge extraction and injection at the organic semiconductor/electrode interfaces resulting in reduced charge-carrier mobility in top-contact thin-film transistors with gold electrodes defined by direct evaporation. In actuality, top-contact thin-film transistors perform as expected if non-traditional patterning methods, such as soft-contact lamination, are used to non-destructively make

contact to TES ADT. Our results indicate that to fully realize organic electronics, patterning methodologies for making electrical contact will have to evolve to satisfy the materials limitations of organic semiconductors.

FIGURES:

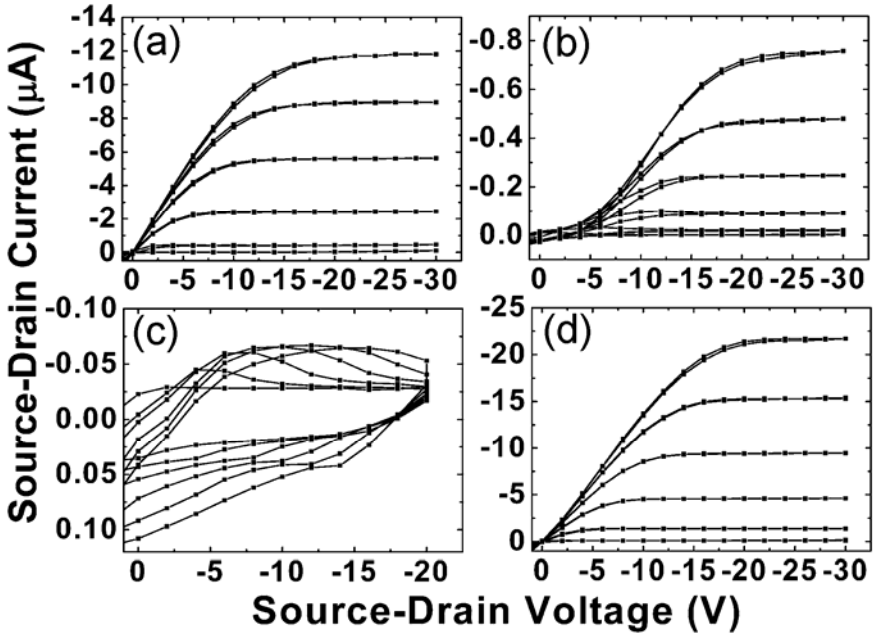

Figure 4.1 Current-voltage characteristics of TES ADT (a) bottom-contact thin-film transistors, (b) top-contact thin-film transistors with source and drain electrodes defined by direct evaporation of gold at 10 angstroms/sec, (c) top-contact thin-film transistors with source and drain electrodes defined by direct evaporation of gold at 1 angstrom/sec, and (d) top-contact thin-film transistor with laminated source and drain electrodes.

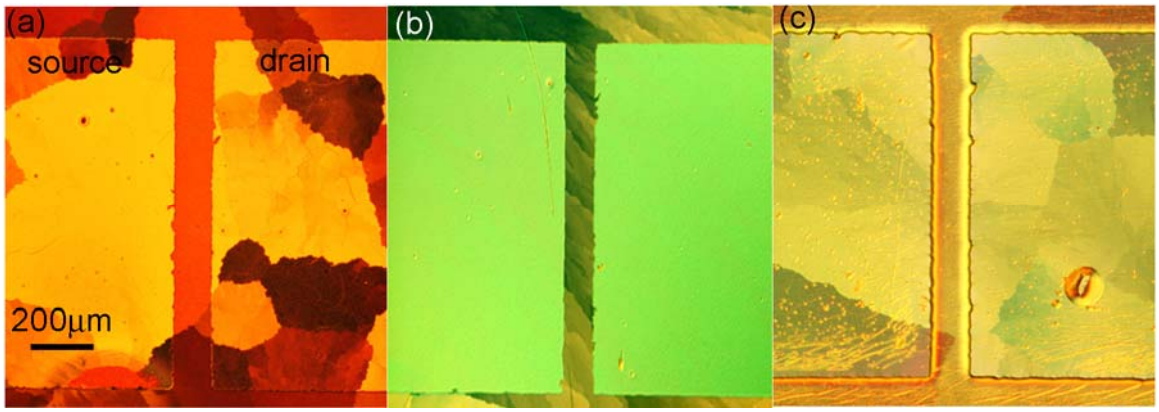

Figure 4.2 Optical microscope images of (a) a bottom-contact TES ADT thin-film transistor, (b) a top-contact TES ADT thin-film transistor with electrodes defined by direct evaporation of gold at 10 angstroms/sec, and (c) a top-contact TES ADT thin-film transistor with laminated electrodes.

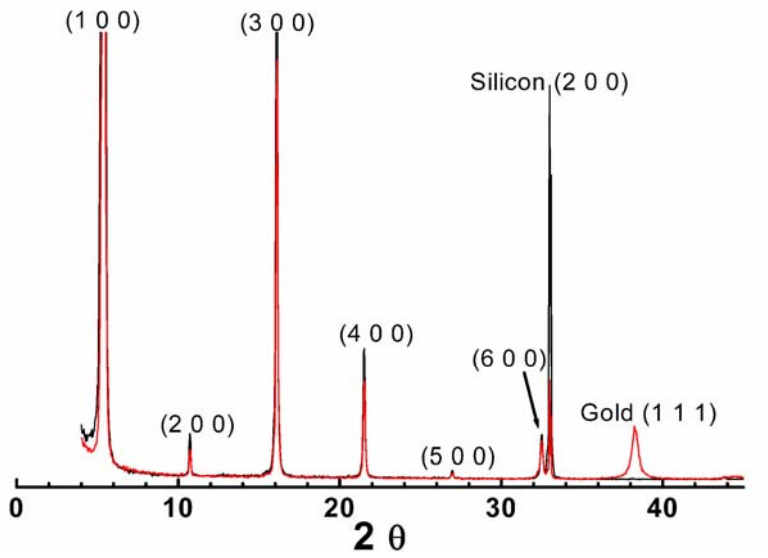

Figure 4.3 X-ray diffraction spectra of a crystalline TES ADT thin film before (black line) and after (red line) gold evaporation at 1 angstrom/sec.

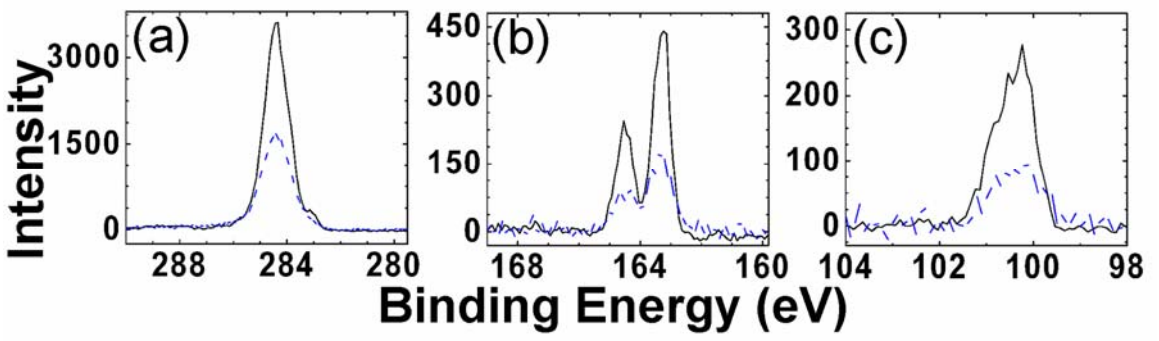

Figure 4.4 XPS high-resolution elemental scans of (a) Carbon 1s, (b) Sulfur 2p, and (c) Silicon 2p in a crystalline TES ADT thin film before (black lines) and after (blue lines) gold evaporation.

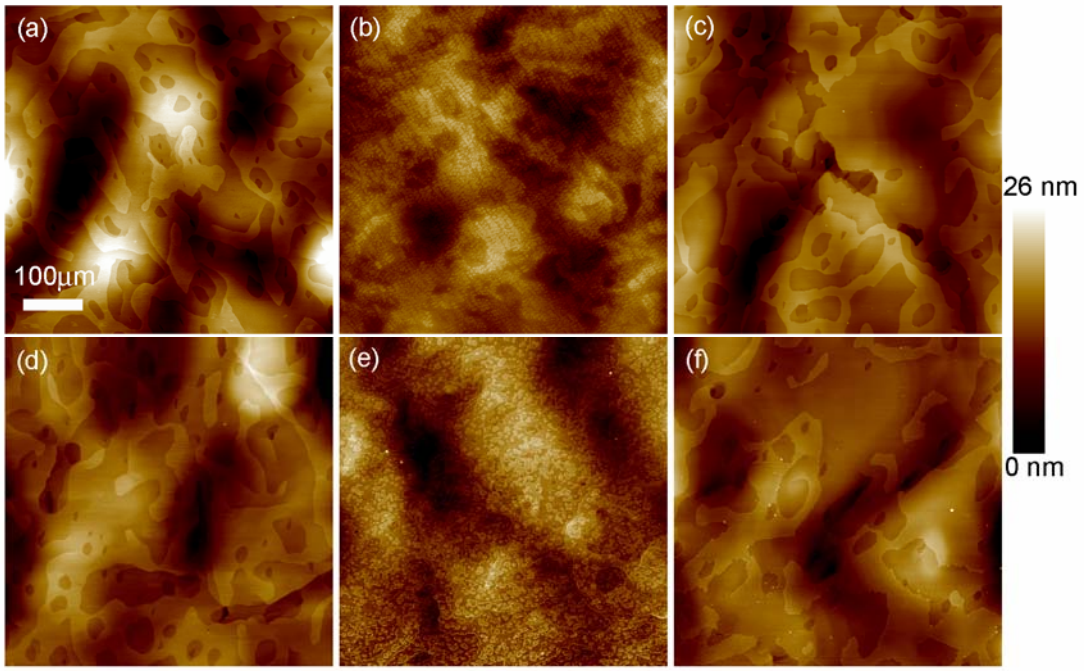

Figure 4.5 Atomic force microscopy images of crystalline TES ADT films (a) before gold evaporation at 1 angstrom/sec, (b) after removing evaporated gold layer (1 angstrom/sec), (c) protected by shadow mask during evaporation at 1 angstrom/sec, (d) before gold evaporation at 10 angstroms/sec, (e) after removing evaporated gold layer (10 angstroms/sec), and (f) protected by shadow mask during gold evaporation at 10 angstroms/sec.

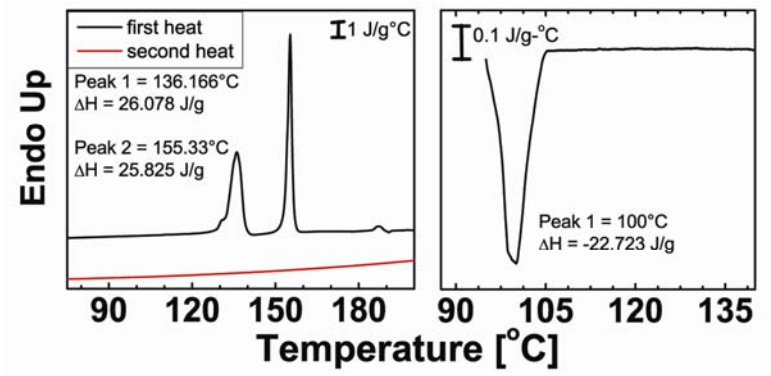

Figure 4.6 Differential scanning calorimetry of TES ADT. Thermal transitions with (a) heating at 10˚C/min and (b) cooling at 1˚C/min.

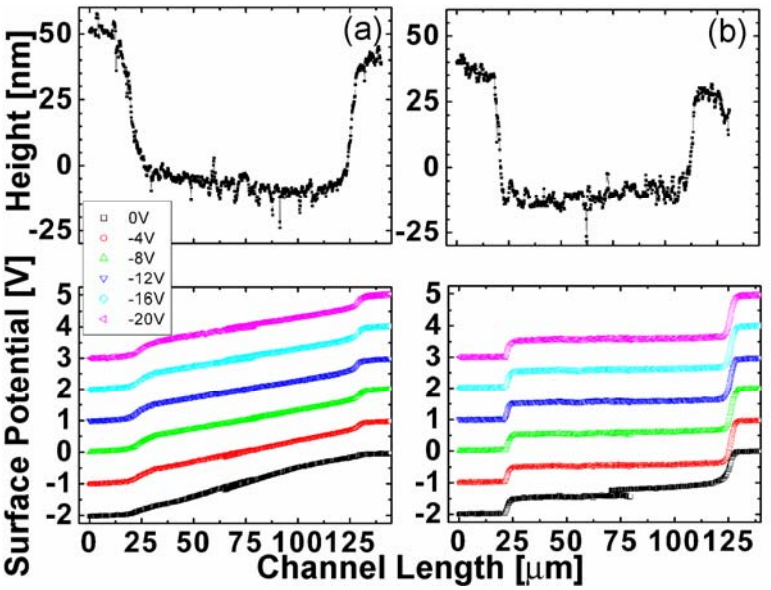

Figure 4.7 Topography and surface potential profiles of (a) a top-contact TES ADT thin-film transistor and (b) a bottom-contact TES ADT thin-film transistor.

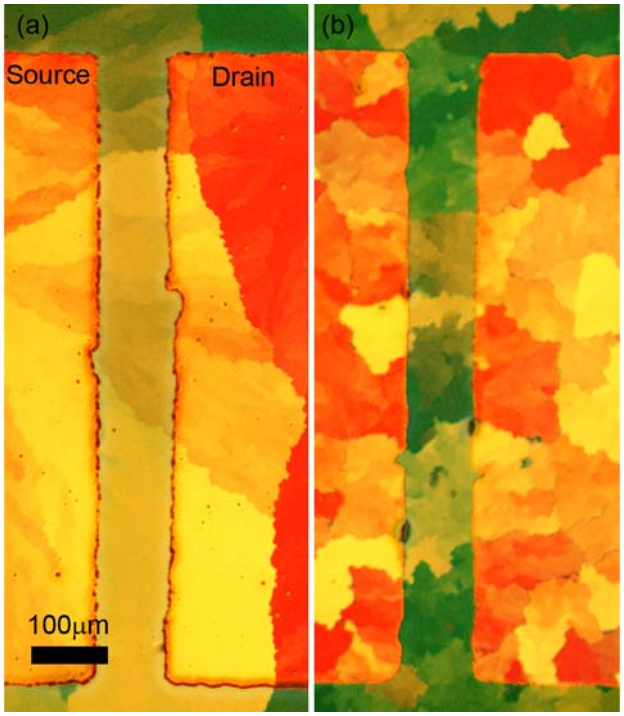

Figure 4.8 Optical microscope images of bottom-contact TES ADT thin-film transistors with gold electrodes defined by (a) direct evaporation through a shadow mask and (b) photolithography and lift off.

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Chapter 5: Alternative Patterning Methods

As discussed in the previous chapter, the manner in which electrical contacts and interconnects are patterned can critically affect device performance. Traditional subtractive methods for making electrical contacts and interconnects, such as photolithography[1] and chemical mechanical polishing (CMP),[2-5] are often incompatible with organic electronics. For example, the solvents used for photolithography can cause organic semiconductors to degrade or to delaminate from the dielectric surface.[6] To overcome this inherent incompatibility between standard patterning techniques and the fragile nature oforganic semiconductors, alternative patterning methodologies for defining metal electrodes and interconnects need to be developed. Ideally, these patterning techniques should be additive, fast, low-cost, cover large areas, and should occur at ambient conditions. Ink-jet printing[7-9] and several soft lithography techniques, such as cold welding,[10] soft contact lamination[11-14] (discussed in chapter 3), and nanotransfer printing (nTP),[12, 15-18] satisfy these requirements. Although ink-jet printing is a promising direct technique for patterning electrodes, the process requires precursor deposition from organic solvents and thermal annealing and sintering at high temperatures to generate continuous, conductive metal features. Instead, we chose to focus on nTP because of the versatility of nTP for patterning metals,[17, 18] multilayers,[18-20] insulators and polymer films,[21, 22] and for making contact to molecular layers[23] without using organic solvents or high processing temperatures. In particular, there are several examples in the literature in which gold has been successfully patterned by nTP for organic device applications.[18, 23] Copper, however, is the more relevant metal for microelectronic applications because of its high conductivity and low tendency for

electromigration.[24, 25] Consequently, it would be beneficial to develop a nTP protocol for additively patterning copper features.

Since gold and copper are both coinage metals,[26-28] we expected copper to behave similarly to gold in nTP. We thus initially attempted to pattern copper on GaAs using thiol interfacial chemistry,[15] as previously demonstrated for patterning gold features.[17, 18] Figure 5.1 illustrates the process for patterning copper on GaAs. Poly(dimethylsiloxane), PDMS, stamps are created by casting and curing Sylgard 184 prepolymer (Dow Corning) against a silicon master previously patterned by conventional photolithography.[17, 18] Immediately prior to depositing thiol molecules, GaAs substrates were etched with hydrochloric acid for 2 min to remove the native oxide layer. We chose hydrochloric acid as the etchant over ammonium hydroxide because AFM analysis indicated that hydrochloric acid etching resulted in a smoother surface (rms = 0.4 nm). 1,8-Octanedithiol is deposited onto freshly-etched GaAs substrates from a 10mM ethanol solution for times varying between 18 – 24 hours, resulting in covalent bonds between one of the thiol endgroups and the substrate. We can verify that the bond between sulfur and gallium and sulfur and arsenic exists by x-ray photoelectron spectroscopy (XPS). The GaAs substrates are then rinsed with copious amounts of fresh ethanol to remove unbound molecules from the surface, and are dried under a stream of nitrogen. PDMS stamps, with freshly deposited copper on the raised and recessed regions, are immediately contacted against the treated substrates. When brought together, the stamps form molecular contact with the GaAs substrates without external pressure.[12] In the regions of contact between the stamp and the thiol-treated GaAs substrate, the remaining unreacted thiol endgroup from the 1,8-octanedithiol molecule will form a covalent bond with copper. This process results in the permanent attachment of the copper patterns to the substrates as copper-sulfur bonds form spontaneously in the regions of contact. In effect,

the 1,8-octanedithiol acts like a molecular 'glue' between the GaAs substrate and the printed copper features. The printed copper patterns therefore always pass Scotch tape adhesion tests. The entire printing process occurs at room temperature with contact times less than 30 seconds.

We can print copper patterns that are uniform over large areas (Figure 5.1b) A Scanning Electron Microscopy (SEM) image of a printed copper feature reveals an edge roughness of approximately 200 nm as shown in Figure 5.2a. This edge roughness is clearly visible on the PDMS stamp, shown in Figure 5.2b, indicating that the silicon master was poorly fabricated. While the present edge roughness is limited by the stamp quality, our previous work with gold patterning indicates that the edge resolution of the printed features can be as small as the metal grain size provided a defect-free stamp is used.[17]

While patterning copper is procedurally similar to patterning gold with nTP, we did observe one marked difference in the resulting metal patterns: printed gold patterns are always conductive,[17, 18] whereas printed copper patterns, regardless of thickness, are never electrically conductive. To better understand the discrepancy between printed gold and copper, we carried out x-ray photoelectron spectroscopy (XPS) depth profiling experiments on these patterns. An argon ion beam was used to sputter through the printed copper pattern until the copper 2p peak intensity (932.7 eV[29-33]) was reduced to 25% of its maximum value and a gallium 2p peak (1116.7 eV[33]) was observed concomitantly, which indicated that we had approached the copper/GaAs interface. High-resolution individual scans of copper 2p (925 – 970 eV) and copper Auger LMM lines (600-640eV), oxygen 1s (525 – 545 eV), and gallium 2p (1110 – 1160 eV) were collected throughout the sputtering process. Since PDMS is generally known to leave behind a surface residue of oligomers[34-37] – this phenomenon has influenced the structure

and purity of alkanethiol self-assembled monolayers patterned by microcontact printing,[35, 36] – and the surface in question was previously in contact with the PDMS stamp, we also tracked the silicon 2p peak (102.1 eV[38]) associated with the Si-O bonds in PDMS. For analysis of the gold pattern, the gold 4f peak (84.0 eV[33]) was also scanned as a function of printed gold pattern depth.

Figure 5.3a contains three Cu LMM spectra. The middle spectrum was obtained after a printed copper pattern had been sputtered briefly (2nm beneath original surface). Its signal more closely resembles that of metallic copper (top spectrum) than that of copper(II) oxide (bottom spectrum). In fact, sputtering experiments indicate that the bulk of the printed, non-conductive pattern is composed of metallic copper, and not oxidized copper. This observation strongly suggests that chemical changes, i.e., oxidation, cannot be responsible for the insulating nature of the printed copper patterns.

Figures 5.3b and c contain XPS scans of the O1s region at various depths of the printed gold and copper patterns, respectively. Both patterns exhibit strong O1s peaks at 532.2 eV[38] associated with the presence of PDMS in the surface scans. O1s peaks associated with moisture[39] are detected in the surface scans of both printed patterns as well. Aside from an additional O1s peak at 530.5 eV[29-33] that corresponds to copper oxide in the copper pattern, the surface scans of both patterns appear remarkably similar. That some PDMS and moisture contamination are detected on printed copper and gold surfaces is expected as these surfaces were previously in contact with PDMS stamps. Further comparison of the XPS depth profiling scans, however, revealed surprising differences between the printed gold and copper patterns. In the case of the gold pattern (Figure 5.3b), a brief sputtering removes all contaminants from the surface; there is no evidence of PDMS or any moisture contamination 5 nm beneath the printed surface. In sharp contrast, the PDMS O 1s peak persists along the entire thickness of the copper

pattern (Figure 5.3c; both the moisture and the copper oxide peaks disappear after sputtering) suggesting that PDMS oligomers are actually present well beneath the printed surface (75 nm). In fact, the XPS scan obtained near the copper/GaAs interface (bottom spectrum of Figure 5.3c) still shows evidence of PDMS. A summary of the depth profiling experiments is presented in Figure 5.4 where the integrated intensities of the O 1s peak are normalized against the integrated intensities of the metal peaks along the depth of the patterns. Tracking the normalized integrated intensity of the Si 2p peak as a function of pattern depth also reveals similar trends; this is exactly what one expects if PDMS were present throughout the depth of the pattern. While the origin of this apparent difference between printed gold and copper patterns remains unclear, we speculate that it is a strong function of metal morphology. Specifically, we believe the oligomers can permeate between copper grains thereby eliminating the percolative pathway for conduction.

To corroborate our XPS data, we conducted conductive-probe atomic force microscopy (C-AFM) on gold and copper patterns printed by nTP. See Chapter 2 for further details on the C-AFM technique. In the C-AFM experiments, we measured the conductivity of the printed metal through the thickness of the printed feature, as shown in Figure 2.6. Since this technique requires that we measure current through the substrate, we printed copper and gold features on a conductive gold substrate rather than GaAs. Similar to printing copper and gold on GaAs substrates by nTP, the conductive gold substrate was treated with 1,8-octanedithiol to create a reactive surface. One end of the 1,8-octanedithiol molecules form covalent S-Au bonds anchoring the 1,8-octanedithiol molecules to the gold substrate. The second –SH functionality is free for subsequent reaction with the metal feature to be transferred. Upon contacting a PDMS stamp with copper or gold features against the thiol-terminated gold substrate, we form S-Cu or S-Au

bonds in the regions of contact between the PDMS stamp and the gold substrate. After removing the PDMS stamp, copper and gold features are permanently bound to the conductive gold substrate through the 1,8-octanedithiol molecules. To make the C-AFM measurements, we established electrical contact between the gold substrate and the base plate of the AFM sample stage with conductive silver paint. A bias ranging from 0 to -50 mV was applied to the base plate and the resulting current was measured through the conductive, platinum-coated tip. C-AFM images were collected in contact mode. With this technique, conductivity and topography images were collected simultaneously, and are shown in Figure 5.5. As observed in the topography images (Figures 5.5a and b), the morphologies of the printed gold and copper features are similar. There is, however, a dramatic difference in the conductivity of the two metal features as shown in Figures 5.5d and e. The printed gold feature is highly conductive; we measured a through-plane current of 200 pA at an applied bias of -50 mV, which is at the maximum compliance of the C-AFM system. The printed copper feature, however, exhibited a through-plane current of less than 5 pA at an applied bias of -50 mV. It is important to note that despite the reduced through-plane current levels measured, we did observe individual conductive grains in the printed copper feature shown in Figure 5.5e. This result provides further evidence that a physical barrier – namely, PDMS oligomers – disrupts the conduction pathway between conductive copper grains in the printed copper features.

We discovered that a simple modification to the existing nTP procedure can reproducibly yield conductive copper patterns. Specifically, leaching the PDMS stamps in toluene at constant reflux (110˚C) for 48 – 72 hours prior to printing sufficiently removes residual PDMS oligomers. Patterned PDMS stamps are placed in a soxhlet extractor for the leaching. After 48 – 72 hours of leaching with hot toluene, the PDMS stamps are removed from the soxhlet extractor and placed in a room temperature vacuum

oven for 12 – 18 hours to drive off residual toluene. The mechanical properties of the PDMS stamp are changed slightly by the leaching process; after leaching the stamps are more rigid and require slight external pressure to achieve conformal contact between the stamp and the substrate. As a consequence of the changed mechanical properties, the maximum thickness of copper that can be printed with toluene-leached PDMS stamps is 25 nm (versus 80 nm that could be printed with as-cast PDMS stamps). The inset of Figure 5.6 contains an optical micrograph of a continuous copper line pattern printed with a leached PDMS stamp. This pattern, along with several others, exhibits an average resistivity of 31 μohms-cm (Figure 5.6). This value is higher than the reported value of 2.67 μohms-cm for a 40 nm thick copper film.[40] We attribute the higher resistivity in the printed copper features to a small amount of residual PDMS oligomers that reside in the printed copper features even after PDMS stamps are leached. With analogous XPS depth profiling experiments, we detect a small amount of PDMS oligomers both on the surface and inside the copper patterns printed with leached stamps (Figure 5.3d <20% of what was present in the patterns printed with as-cast stamps). While the PDMS still permeates into printed copper (Figure 5.4), the copper features printed with leached PDMS stamps are still highly conductive. Further, C-AFM experiments on copper features printed with the leached PDMS stamps yield conductivity images with current levels on par with printed gold features (Figure 5.5 f). Additionally, the topography images indicate that the leaching process has no effect on the morphology of the printed copper (Figure 5.5 c).

In summary, we have extended nTP for patterning conductive copper. Interestingly, printing with as-cast PDMS stamps − which are commonly used for self-assembled monolayer formation,[41] deposition of catalysts and precursors for electroless plating,[42] and patterning of nanoparticle arrays[43] − generates non-conductive copper patterns. Contrary to previous studies that have shown that PDMS oligomers only reside

on the contacted surfaces, our XPS analysis indicates that the PDMS oligomers are actually present in the bulk of the printed copper patterns. C-AFM studies which show that individual copper grains are conductive within an overall nonconductive copper feature further support the XPS analysis. PDMS oligomers, however, are not present in printed gold patterns and we speculate that this may be the fact that gold is not prone to oxidation, while copper is prone to oxidation. Silver, another metal that is prone to oxidation, behaves similarly to copper in the nTP patterning process. These results seem to indicate that metals prone to oxidation are susceptible to PDMS oligomer penetration. With minor adjustments to the procedure, however, nTP can be a valuable tool for patterning conductive copper in a purely additive manner.

FIGURES:

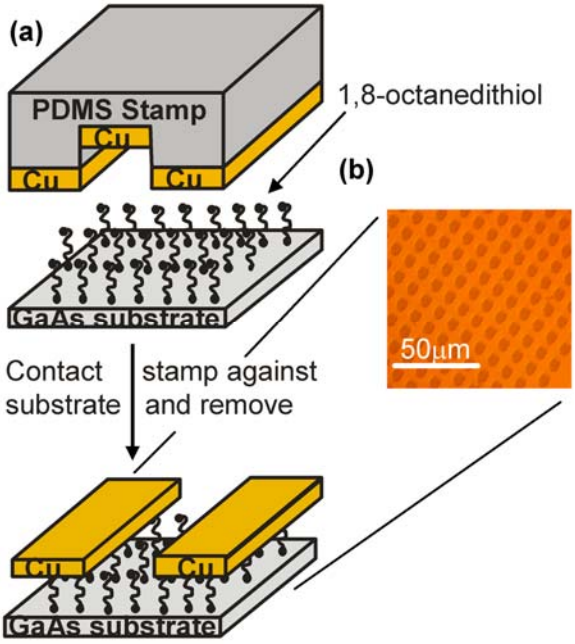

Figure 5.1 (a) Schematic of copper pattern transfer by nTP. Copper is deposited onto the raised and recessed regions of a PDMS stamp by e-beam evaporation. The PDMS stamp is then contacted for < 30 seconds at room temperature against a GaAs substrate that was pretreated with 1,8-octanedithiol. After removing the stamp, the copper patterns are bound to the GaAs substrate in the areas of contact. (b) Optical microscope image of a printed copper pattern revealing the large-area printing capability of nTP. Light regions correspond to copper, dark regions correspond to GaAs.

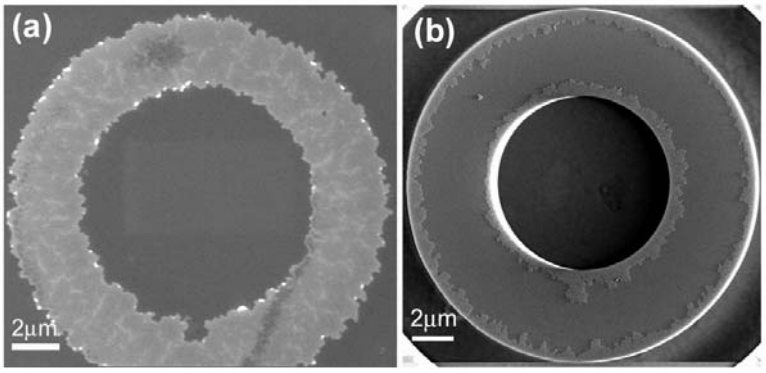

Figure 5.2 Scanning electron microscopy (SEM) images of (a) a copper feature printed by nTP and (b) the PDMS stamp after printing the copper feature. The roughness at the PDMS stamp edge is faithfully transferred to the printed copper feature.

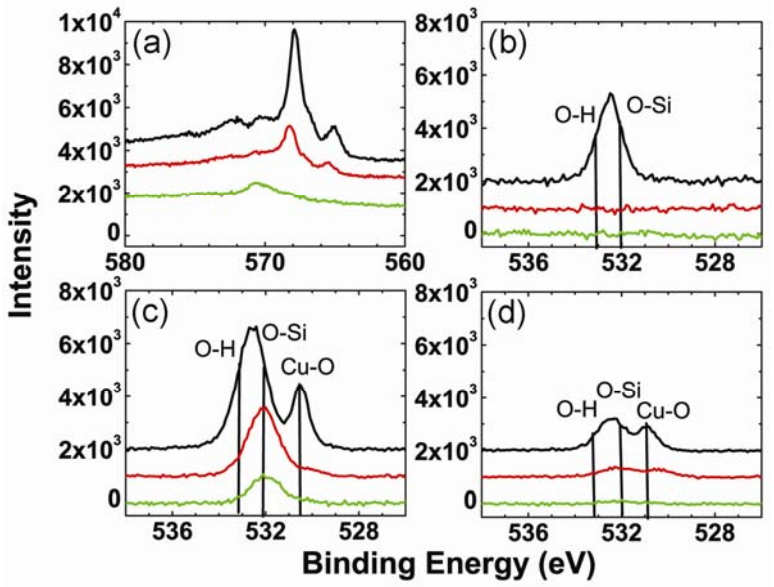

Figure 5.3 (a) Copper *LMM* spectra of metallic copper (II) oxide (red ling), a printed nonconductive copper pattern 2 nm beneath the surface (green line), and metallic copper (black line). O *1s* spectra of (b) gold and (c) copper printed with as-cast PDMS stamps, and (d) copper printed with a toluene-leached stamp. All spectra are offset for clarity. In graphs b through d, the top spectra (black line) were obtained on the printed surfaces, while the middle (red line) and bottom spectra (green line) were obtained 5 nm below the surface and at the metal/GaAs interface, respectively.

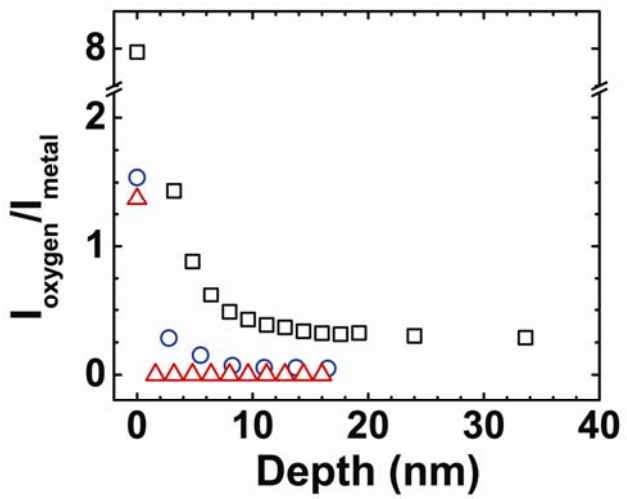

Figure 5.4 Normalized integrated peak intensities of oxygen 1s along the depth of printed gold (Δ),non-conductive copper (□), and conductive copper (○) patterns. All peaks were also normalized by the appropriate atomic sensitivity factor. (See Ref. 33). The PDMS oligomers reside only on the surface of gold, but permeate through the copper patterns.

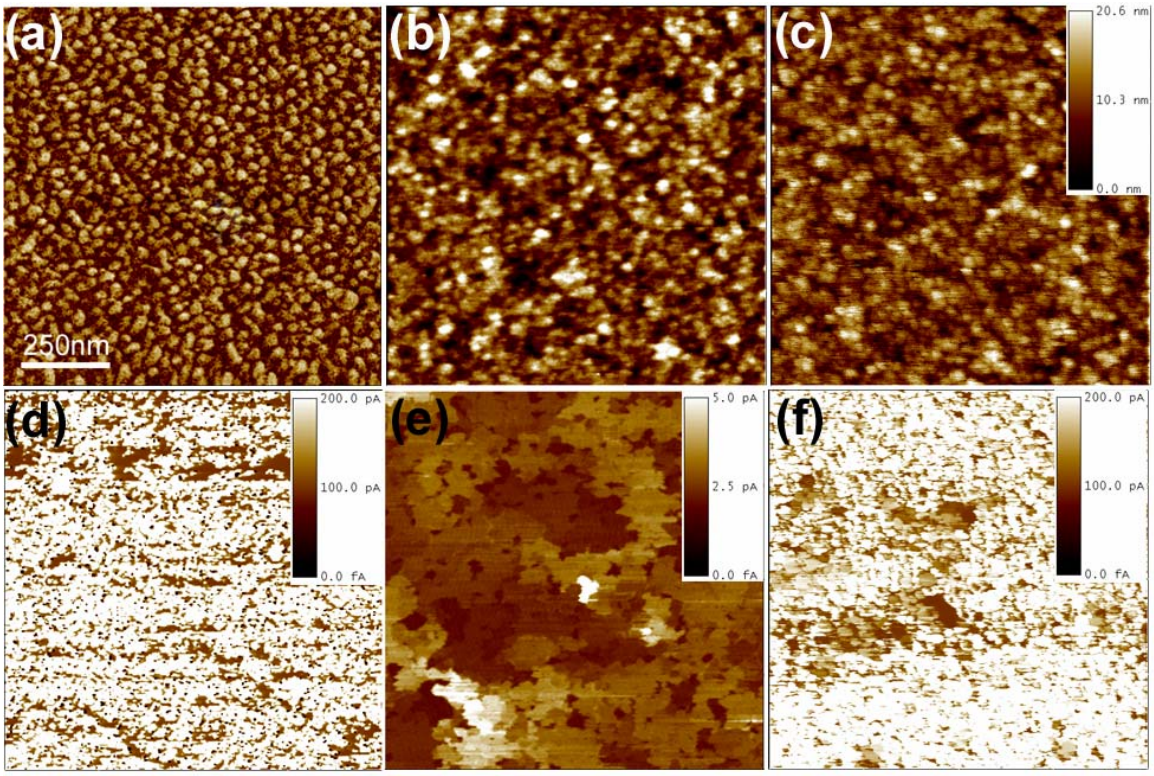

Figure 5.5 AFM topography images of (a) gold and (b) copper printed with as-cast PDMS stamps and (c) copper printed with a toluene-leached PDMS stamp. The scale bar shown in (c) applies for images (a) through (c). Corresponding conductivity images of (d) gold and (e) copper printed with as-cast PDMS stamps and (f) copper printed with a toluene-leached PDMS stamp. In graphs d through f the individual metal grains are conductive.

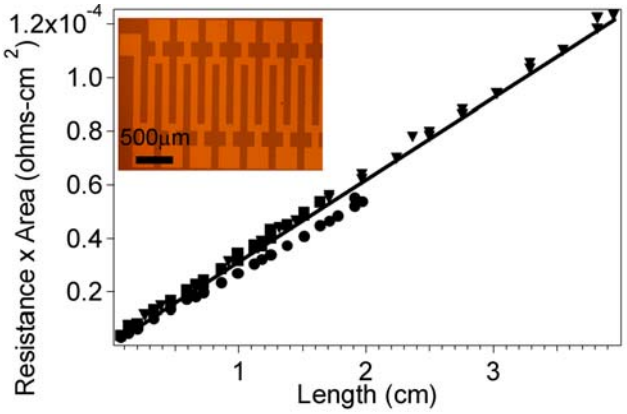

Figure 5.6 Resistance measured along the length of printed continuous copper lines. The slope yields an average resistivity of 31μΩ-cm. Top inset: Optical microscope image of one of the printed copper lines. Light regions correspond to copper.

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Chapter 6: Novel Methods for Patterning Solution-Processable Triethylsilylethynyl Anthradithiophene

Unpatterned organic semiconductor films often exhibit leakage currents (non-zero source-to-drain currents at zero applied source-to-drain bias) and high off currents (source-to-drain currents of 10^{-6} – 10^{-9} A despite a zero gate voltage) because the charge carriers are not confined to the channel region of the thin-film transistor. Confining the organic semiconductor to the channel region of the thin-film transistor through patterning eliminates the leakage currents and electrical cross talk between adjacent transistors and lowers the off currents.[1] There are three main methods of patterning organic semiconductors: a derivative of photolithography that uses a barrier layer to protect the organic semiconductor in the regions of interest,[2-6] deposition through a shadow mask[7, 8] and printing.[9-13] Although photolithography is the traditional method for patterning inorganic semiconductors,[2] photolithography (i.e., solvents, developers, and pre- & post-bake processing temperatures) is generally not compatible with organic semiconductors. Specifically, photolithography tends to cause chemical and physical degradation of the organic semiconductor thin film due to delamination and/or changes in the film morphology.[14] Therefore if photolithography is used to pattern organic semiconductors it is used in conjunction with a blocking layer to protect the organic semiconductor during subsequent processing,[4, 6] or is used to define reentrant resist profiles that are not removed after the semiconductor is deposited.[3, 5] (When the organic semiconductor is subsequently deposited it breaks over the reentrant resist profile resulting in isolated semiconductor regions.) Patterning with shadow masks is much more straightforward. Shadow masks are not, however well-suited for patterning solution-processable organic semiconductors with high fidelity since the shadow masks do not form a liquid-tight seal when contacted against the substrate. As a consequence, shadow masks are limited to

patterning vapor-deposited organic semiconductors, such as pentacene[3, 5] and copper hexadecafluorophthalocyanine.[5] Printing methods, such as ink-jet printing[9, 10, 15] and screen printing,[12, 13, 16] are much more viable options for patterning solution-processable organic semiconductors because both the deposition and patterning are completed simultaneously. To date, organic thin-film transistors fabricated with printing techniques have been limited to solution-processable polymer organic semiconductors since polymers tend to have better film forming properties.[9, 11] There are few techniques available for patterning solution-processable, small-molecule organic semiconductors deposited by simple solution deposition techniques, such as spin casting or drop casting. In these techniques, the organic semiconductor is indiscriminately deposited across the substrate.

We have developed two techniques for patterning solution-processable organic semiconductor triethylsilylethylnyl anthradithiophene (TES ADT) after is has been deposited by spin coating. The first technique utilizes UV light in the presence of solvent vapors to selectively cause the TES ADT to dewet in the irradiated regions. Simultaneously, the solvent vapors induce TES ADT to crystallize in the non-irradiated regions. Patterning TES ADT channel regions with this technique yielded devices with highly crystalline TES ADT thin films exhibiting an average charge-carrier mobility of 0.1 cm^2/V-s, no leakage currents and low off currents (10^{-11} A). The second patterning technique utilizes PDMS stamps to selectively remove crystalline TES ADT from the non-channel regions of the transistor post-processing and post-annealing. Similar to the light patterning technique, the PDMS patterning technique yields TES ADT thin-film transistors with high charge-carrier mobility, no leakage currents and low off currents. Both patterning techniques are suitable for patterning arrays of transistors.

In all of our patterning experiments we used a bottom-contact TES ADT thin-film transistor platform. Gold source and drain electrodes (40 nm thick) were deposited by e-beam evaporation through a shadow mask onto a heavily doped silicon substrate with 100 nm of thermally-grown silicon oxide. The silicon served as a common gate while the silicon dioxide served as the gate dielectric. The transistor channel length was 100 μm and the channel width was 1000 μm. Prior to depositing the TES ADT solution on the transistor platform, the silicon substrates with gold electrodes were sonicated in deionized water for approximately 3 minutes and then placed in a UV/Ozone chamber for 10 minutes. Following substrate cleaning, a 2 wt% solution of TES ADT in toluene was spin coated to complete the transistor.

For light patterning, we used an Omnicure UV curing system from EXFO. This unit uses a 200 W mercury lamp with a main peak at 365 nm. At a system iris setting of 98% our samples are irradiated with 540 mW/cm^2. The UV light is projected onto the sample surface in a specified pattern with a Discovery 1100 micro-mechanical mirror array from Texas Instruments. The array consists of 1024 x 768 aluminum micro-mechanical mirrors. Each mirror can be individually addressed to deflect light through or away from a fixed focal point lens. The template used to dictate the micro-mirror positions is created using any computer drawing program. With the Discovery 1100 system, the projected light pattern cannot exceed a 2 mm x 2 mm footprint. During irradiation the TES ADT film is simultaneously exposed to dichloroethane solvent vapors for plasticization. In the irradiated regions, plasticized TES ADT will dewet from the silicon dioxide surface. If an extremely high energy source is used, it is possible for the TES ADT to dewet from the silicon dioxide surface without the presence of solvent vapors. For example, we observed this type of dewetting with scanning electron microscopy (SEM) with a 1 kV working voltage (approximately 1 W/cm^2 irradiation

assuming a 52 pA beam current and a 50 μm x 100 μm spot size). The maximum setting on the UV light source, however, does not cause the TES ADT to dewet unless dichloroethane solvent vapors are present. To concurrently hold the TES ADT thin-film transistor and dichloroethane solvent while satisfying the space constraints associated with the UV light source set-up, we built a cylindrical, glass sample holder with a diameter of 2.5 cm and a height of 1 cm. The as-spun TES ADT transistor is seated on top of an 8 mm spacer inside of the sample holder and a few drops of dichloroethane are added to the bottom of the sample holder. Since the TES ADT transistor sits on top of a spacer in the holder, the dichloroethane liquid does not come into direct contact with the TES ADT film. The transistor is then manually aligned (by eye) under the light source to ensure that the transistor channel is not illuminated during the patterning process. Once alignment is complete, the sample holder is partially covered with a glass cover-slip to create a dichloroethane-rich vapor space. (If the sample holder is completely covered by the glass cover slip, the vapor space becomes so concentrated with dichloroethane vapors that the TES ADT film forms large, 3-D crystals within seconds. This type of crystallization generates a discontinuous TES ADT film across the silicon dioxide surface. It is thus important to maintain some air in the vapor space to slow the crystallization process so we maintain a laterally continuous TES ADT film.) Immediately after the cover slip is put in place, the light source is turned on for 60-120 seconds. In the regions in which the TES ADT thin film is illuminated, TES ADT dewets from the silicon dioxide surface. The progress of the dewetting can be monitored through a color change in the areas of illumination (when looking through protective eyewear, the color changes from red to white to indicate that the dewetting is complete). UV/VIS analysis of TES ADT (in solution and in a thin film) before and after UV exposure at 540 mW/cm^2 for 2 minutes yields identical spectra, indicating that the UV exposure is not

degrading the TES ADT molecules. We speculate that the dewetting is driven by surface energy differences between the substrate and the TES ADT. The surface energy of the substrate is high after UV/Ozone treatment (contact angle of ~0º), while TES ADT has a relatively low surface energy (contact angle of 80º). As TES ADT molecules are plasticized by the combination of dichloroethane vapors and UV light energy converted to thermal energy (TES ADT is slightly absorbing at 365 nm) in the irradiated regions, the TES ADT molecules are mobile enough to migrate from the higher energy silicon dioxide and gold surfaces to the lower energy TES ADT surface. Consequently we observe a ridge (200 – 400 nm in height) at the edge of the patterned TES ADT thin film indicating that TES ADT has accumulated at this edge. While TES ADT is dewetting in the illuminated regions, TES ADT simultaneously crystallizes in the dark regions. Consequently, we can anneal and pattern TES ADT in a single step, minimizing any post-deposition processing required to yield high performance thin-film transistors. Optical microscope images of an unpatterned but separately crystallized transistor and a transistor patterned with UV light are shown in Figures 6.1a and b, respectively. The corresponding current-voltage characteristics for each of the transistors are shown in Figures 6.1c and d, respectively. While the charge-carrier mobility of the patterned and unpatterned transistors is comparable, the leakage currents that are evident in the unpatterned transistor are virtually eliminated in the patterned transistor. Additionally, the light patterning is effective in reducing the off current by an order of magnitude in the patterned transistor (10^{-11} A). With the projection system limitations (2 mm x 2 mm maximum illumination area) and electrode dimensions we used in our experiments, we were only able to pattern a maximum of three transistors with a single light exposure, as shown in Figure 6.2. The current-voltage characteristics of the patterned array of transistors were comparable to those of annealed TES ADT thin-film transistors (Chapter

3) with an average charge-carrier mobility of 0.1 $cm^2/V\text{-}s$. The off-current, however, is an order of magnitude lower in the light-patterned thin-film transistors (10^{-10} A) as compared to previous thin-film transistors in which we only scratched through the TES ADT film to isolate individual transistors (10^{-9} A). It is important to note that the UV light patterning technique only works on amorphous TES ADT thin films. Once the TES ADT film crystallizes, it is extremely difficult to remove from the silicon dioxide surface. Since were are patterning and crystallizing the TES ADT film simultaneously, the TES ADT thin-film transistors must be patterned with a single light exposure. Alternatively, on can use a larger UV light projection system to increase the patterning footprint. Further, using a moving solvent vapor reservoir, this process is amenable to being continuous.

The second technique we developed for patterning TES ADT thin-film transistors is a contact patterning technique that uses a PDMS stamp to selectively remove TES ADT from the silicon dioxide surface. This technique is versatile; it can be used to pattern both amorphous and crystalline TES ADT films. In this process a patterned PDMS stamp is contacted against a TES ADT film. In the regions of direct contact between PDMS and TES ADT, TES ADT diffuses into the PDMS stamp. The regions of the TES ADT film not in direct contact with the PDMS stamp (corresponding to the recessed regions of the PDMS stamp) are unchanged during the patterning process. That TES ADT diffuses into PDMS is a surprising result given that the diffusing species is a crystalline solid. Yet we see that TES ADT does in fact diffuse into the PDMS stamp as evidenced by the loss of crystallinity in the TES ADT film shown in Figure 6.3 Diffusion of TES ADT into PDMS can be prevented if the surface of the PDMS stamp is coated with a barrier layer such as gold prior to contact with TES ADT. This is why the top-contact thin-film transistors with laminated gold electrodes perform so well in

Chapter 4. Figure 6.3a shows the crystalline TES ADT film immediately after contacting it with a patterned PDMS stamp. The images are taken through the PDMS while the same PDMS stamp is in contact with the TES ADT film throughout this process. The rectangular regions of the image correspond to the recessed regions of the PDMS stamp in which there is an air pocket between the PDMS stamp and the TES ADT film. In the remaining areas, the PDMS stamp is in direct contact with the TES ADT film. As time progresses (Figures 6.3b-f), TES ADT diffuses into the PDMS stamp and we observe a loss of crystallinity in the film directly in contact with the PDMS stamp. The TES ADT film not directly in contact with PDMS, however, maintains its crystallinity. Partial diffusion of TES ADT into the PDMS stamp is evident after only 30 minutes of contact time (Figure 6.3b). After approximately 6 hours of contact time (Figure 6.3e), the TES ADT film has completely diffused from the silicon dioxide surface into the PDMS stamp. The contact time required to achieve complete removal of TES ADT from the silicon dioxide surface can be reduced if we pattern as-spun TES ADT, rather than annealed TES ADT. When PDMS is contacted against an amorphous TES ADT film, 45-60 minutes of contact time is sufficient to completely remove the organic semiconductor from the non-channel regions of the transistor. Subsequent annealing of the patterned TES ADT thin-film transistors yields transistors with an average charge-carrier mobility of 0.09 ± 0.02 $cm^2/V\text{-}s$ and an off-current of 10^{-10} A. This charge-carrier mobility is lower than if we were to crystallize the TES ADT film prior to patterning with PDMS. We believe that this result is a function of the TES ADT grain size. Typically, the TES ADT grain size is larger if we anneal the TES ADT film prior to patterning. During the annealing process, the edges of the TES ADT film serve as nucleation sites for grain growth which proceeds inward towards the channel. Since the perimeter-to-area ratio of the patterned TES ADT film is larger than a typical unpatterned TES ADT film, the nucleation density is greater

in the first case. As such, we consistently observe smaller grains (several hundred microns) in the patterned TES ADT film compared to the unpatterned TES ADT film (several millimeters) on annealing. Consequently, the measured charge-carrier mobility is slightly lower in TES ADT thin-film transistors in which the as-spun TES ADT film is patterned prior to annealing.

Although patterning crystalline TES ADT films requires longer contact times with PDMS to completely remove TES ADT from the non-channel regions of the transistor, the resulting transistors retain their high charge-carrier mobility, exhibit virtually no leakage currents, and have low off currents. Optical microscope images of the actual thin-film transistors patterned with PDMS after varying contact times are shown in Figure 6.4. After one hour of contact time (Figure 6.4b), we observe partial diffusion of TES ADT into the PDMS stamp and we are able to detect the beginning of a well-defined channel region. Correspondingly, we observe a dramatic reduction in the leakage currents in the current-voltage characteristics shown in Figure 6.5. After 3 hours of contact time (Figure 6.4c), the channel region can clearly be differentiated from the non-channel region of the transistor. Complete removal of the TES ADT film from the non-channel regions, however, has not yet been achieved. With 6 hours of contact time, the TES ADT film has completely diffused into the PDMS stamp in the regions of contact (Figure 6.4d). By optical microscopy, there is no detectable difference in the amount of TES ADT removed after 12 hours of PDMS contact time as compared to 6 hours of PDMS contact time. There is, however, a difference in the off currents. As the amount of TES ADT removed from the non-channel regions of the thin-film transistors increases, the off-currents of the thin-film transistor decrease correspondingly. The off-current is plotted as function of PDMS contact time in Figure 6.6. After one hour of contact time there is minimal change in the off current as would be expected from the extent of TES

ADT removal depicted in Figure 6.3b; the TES ADT film is still essentially continuous outside the channel region. Reduction in the off current becomes more pronounced with longer PDMS contact times. We observe an order of magnitude decrease in the off current with 3 hours of contact time (we have only partially removed the TES ADT film from the non-channel regions of the thin-film transistor), and two orders of magnitude decrease with 6-12 hours of contact time (by optical microscopy all of the TES ADT film has been removed from non-channel regions of the thin-film transistors). After 12 hours of PDMS contact, the measured off current is on the order of 100 pA in the patterned transistors, which is significantly less than the 20 nA measured in the unpatterned transistors. Additionally, the average charge-carrier mobility (right y-axis in Figure 6.6) and threshold voltage (not shown) are not affected by the long PDMS contact times implying that the integrity of the TES ADT film in the transistor channel is not compromised by the patterning process. All of the PDMS patterned device characteristics are summarized in Table 6.1. Further, large-area arrays of transistors can easily be patterned with our PDMS patterning technique. Similar to the light patterning technique, this technique is scalable so we can pattern TES ADT over large areas. In our experiments, we were limited by the size of the shadow masks we use to pattern the electrodes on the silicon substrate (the shadow mask only contains electrode pairs for 8 thin-film transistors). One can easily extend the size of the shadow mask to make PDMS stamps of a larger footprint. An array of eight patterned transistors is shown in Figure 6.7a after 12 hours of PDMS contact time. Each transistor in the array is clearly isolated, eliminating any electrical cross talk between individual transistors. Representative current-voltage curves from a transistor in this array are shown in Figure 6.7b. We do not observe any significant leakage currents, while the on currents are high (15 μA) and the off current is low (100 pA).

Table 6.1. Summary of current-voltage characteristics of TES ADT thin-film transistors patterned by PDMS contact method.

Before Patterning			After Patterning			
Charge-Carrier Mobility (cm^2/V-s)	**Threshold Voltage (V)**	**On/Off Ratio**	**PDMS contact time**	**Charge-Carrier Mobility (cm^2/V-s)**	**Threshold Voltage (V)**	**On/Off Ratio**
0.16 ± 0.05	2.0 ± 1.9	2.3×10^3	1 hr	0.15 ± 0.03	2.1 ± 1.6	1.7×10^4
0.18 ± 0.04	0.8 ± 0.7	1.3×10^3	3 hr	0.14 ± 0.04	1.8 ± 1.2	1.1×10^4
0.21 ± 0.06	2.9 ± 1.1	9.2×10^2	6 hr	0.19 ± 0.06	2.8 ± 0.8	3.1×10^4
0.25 ± 0.05	0.8 ± 0.7	2.0×10^3	12 hr	0.22 ± 0.05	0.2 ± 0.5	1.0×10^5

In summary, we have demonstrated two techniques for patterning the solution-processable TES ADT organic semiconductor post deposition. The first technique utilizes UV light in the presence of 1,2-dichloroethane vapors to *simultaneously* pattern and crystallize the as-spun TES ADT film. The TES ADT exposed to the UV light dewets from the silicon dioxide surface, while the TES ADT not exposed to light crystallizes. The second technique exploits the unique materials properties of TES ADT. We selectively remove TES ADT from the non-channel regions of the transistor using a PDMS stamp. In the regions of contact between TES ADT and PDMS, the TES ADT diffuses into PDMS leaving behind a bare silicon dioxide surface with sufficient contact time. This technique can be used to pattern both as-spun and crystalline TES ADT films. Both technique successfully eliminate leakage currents and lower off currents in the patterned thin-film transistors.

FIGURES:

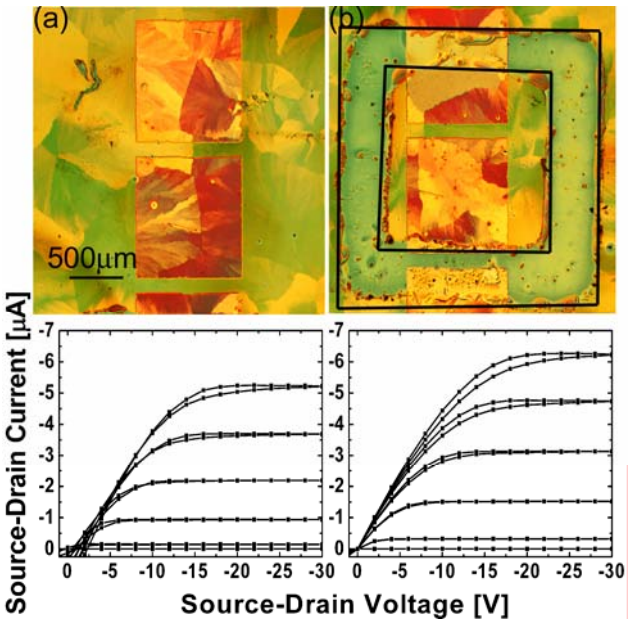

Figure 6.1 Optical microscope images and current-voltage characteristics for (a) an unpatterned but separately crystallized TES ADT thin-film transistor with a charge-carrier mobility of 0.10 cm^2/V-s and an off current of 3.4 x 10^{-10} A and (b) a TES ADT thin-film transistor patterned and simultaneously crystallized with UV light with a charge-carrier mobility of 0.12 cm^2/V-s and an off current of 8.4 x 10^{-11} A. In both transistors L=100 μm and W=1000 μm. Leakage currents are eliminated and off-currents are reduced in the patterned transistor. The highlighted region in (b) was irradiated during patterning.

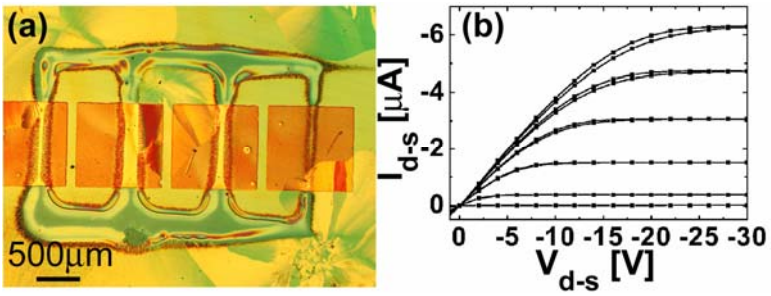

Figure 6.2 (a) Array of transistors (L=100 μm, W=1000 μm) patterned using UV light. (b) Current-voltage characteristics of a representative transistor in the patterned array. The transistor exhibits a charge-carrier mobility of 0.12 cm^2/V-s and an off current of 1.6 x 10^{-10} A.

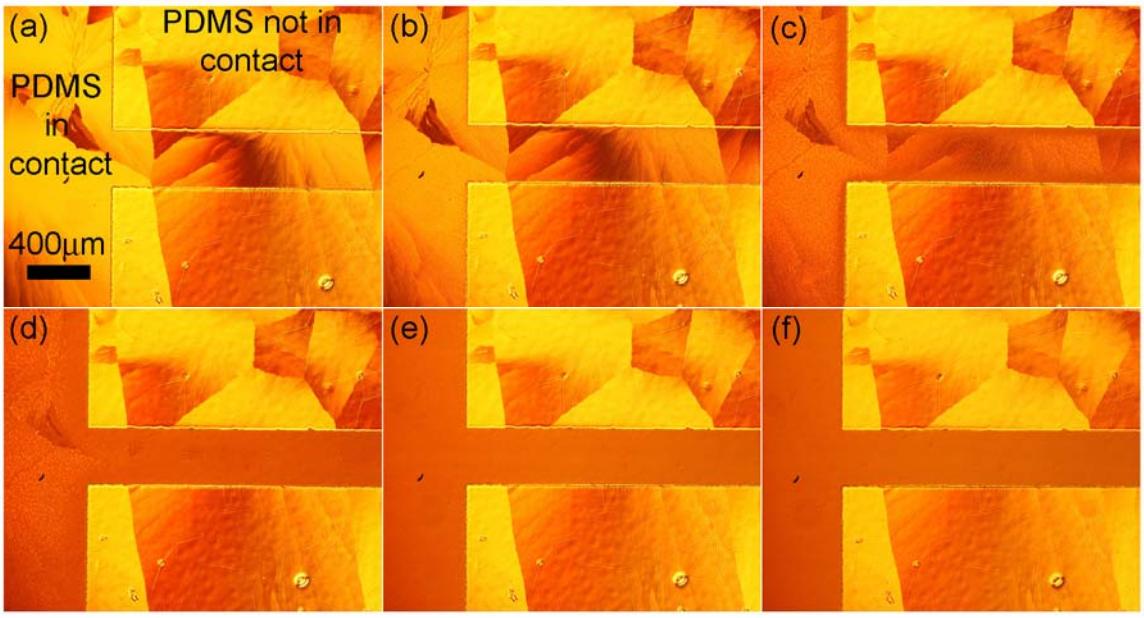

Figure 6.3. Optical microscope images taken through the same PDMS stamp tracking the diffusion of crystalline TES ADT into the stamp. TES ADT film (a) immediately after contact with a PDMS stamp, (b) after 30 minutes of contact, (c) after 1 hour of contact, (d) after 3 hours of contact, (e) after 6 hours of contact, and (f) 8 hours of contact .

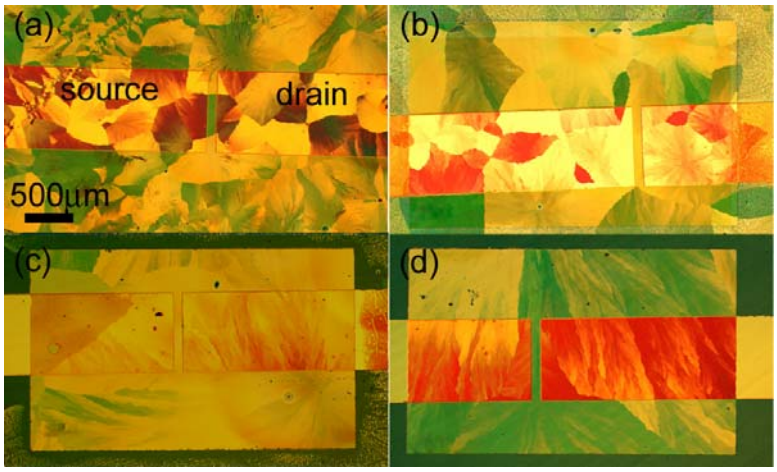

Figure 6.4 Optical microscope images of TES ADT thin-film transistors: (a) unpatterned, (b) after 1 hour of contact time with PDMS, (b) after 3 hours of contact time with PDMS, and (d) after 6 hours of contact time with PDMS. The TES ADT diffuses into the PDMS stamp in the regions of contact leaving behind a well-defined channel region after 6 hours of contact time. All of the images were taken after removing the PDMS stamp after the specified amount of time.

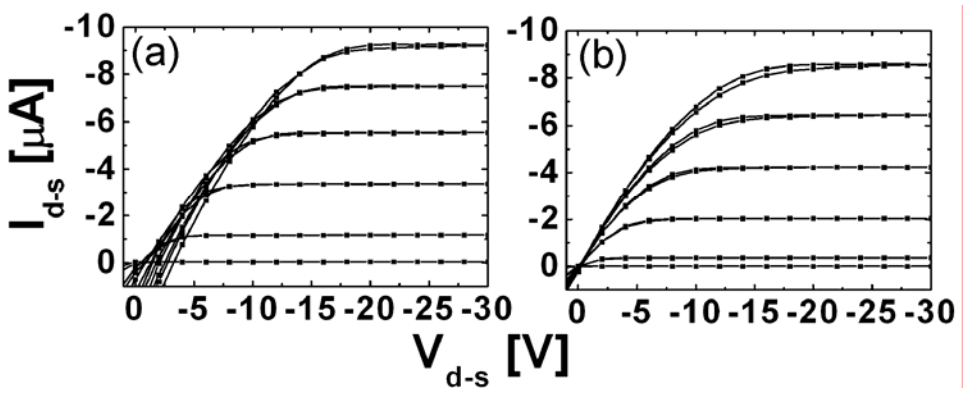

Figure 6.5 Current-voltage characteristics of (a) an annealed but unpatterned TES ADT thin-film transistor and (b) the same TES ADT thin-film transistor after patterning with a PDMS stamp for 1 hr. The transistor dimensions are L=100 μm and W=1000 μm. The leakage currents are eliminated in the patterned transistor while the magnitude of the on currents is virtually unchanged.

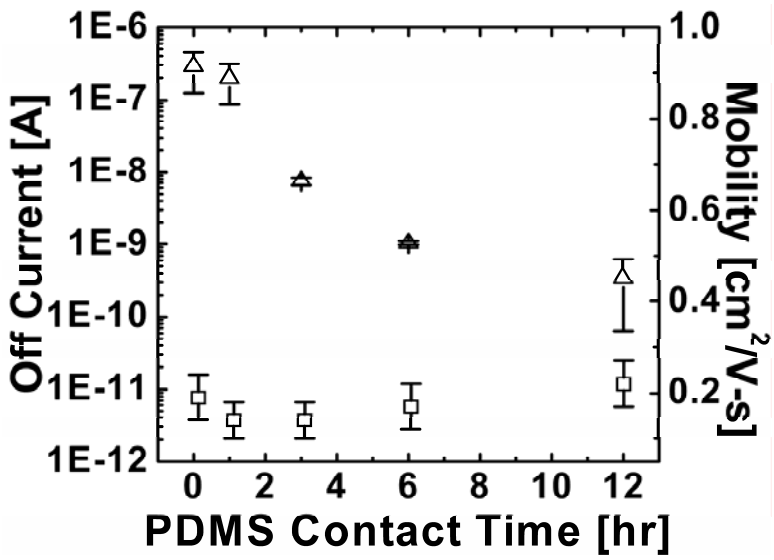

Figure 6.6 Reduction in off current (Δ) observed with increased contact time between PDMS and annealed TES ADT thin-film transistor while the charge-carrier mobility (□) remains virtually unchanged.

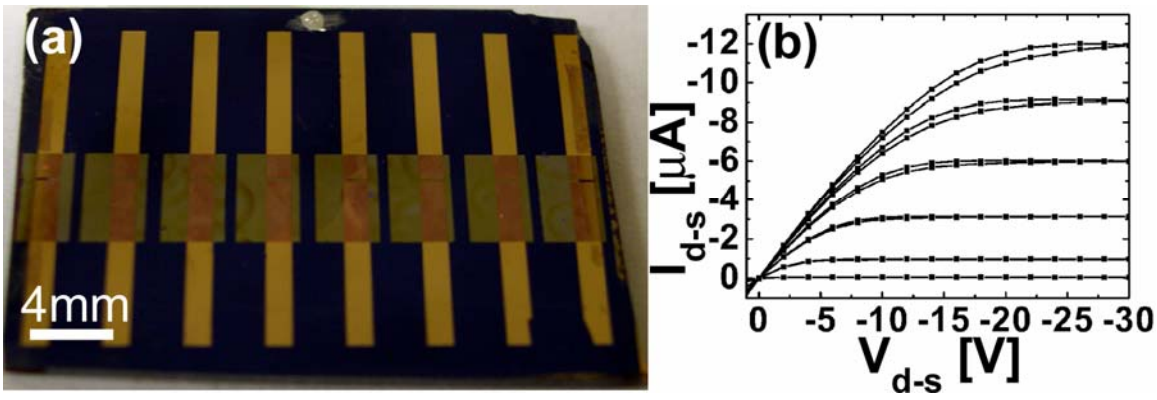

Figure 6.7 (a) Array of transistors (L=100 μm, W=1000 μm) patterned with a PDMS stamp for 6 hours. (b) Typical current-voltage characteristics of a transistor in the patterned array. The transistor array exhibits a charge-carrier mobility of 0.22 ± 0.05 cm^2/V-s and an off current of 2 x 10^{-10} A.

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Chapter 7: Conclusions and Future Work

CONCLUSIONS:

This thesis focuses on understanding the processing-structure-property relationships of a solution-processable organic semiconductor, triethylsilylethylnyl anthradithiophene (TES ADT) for functional thin-film transistors. TES ADT is an anthradithiophene derivative that has been functionalized with bulky triethyl silyl groups that impart solubility and can induce the molecules to pack in a 2-D cofacial manner. With TES ADT, we can thus form highly-ordered thin films from solution. When TES ADT is incorporated in a thin-film transistor platform, our devices exhibit electrical characteristics that are on par with backplane requirements for driving large-area flexible displays[1] and electronic papers.[2]

We demonstrated a simple solvent-vapor annealing process that can induce order in amorphous, as-spun TES ADT thin films. The thin-film transistors with annealed TES ADT routinely exhibit a charge-carrier mobility of 0.13 ± 0.07 $cm^2/V\text{-}s$, which is sufficient to drive backplane circuitry in flexible display applications.[3] This result is significant because low-cost deposition techniques, like spin casting, that generally yield amorphous organic semiconductor thin films (which exhibit low charge-carrier mobility in device applications) can now be used in conjunction with a straightforward solvent-vapor annealing step to fabricate thin-film transistors with high charge-carrier mobility. Beyond inducing structural reorganization in amorphous organic semiconductor thin films, we can also tune the threshold voltage of annealed TES ADT thin-film transistors through solvent-vapor annealing with the appropriate solvent. Annealing with a mixture of hexanes and dichloroethane solvent vapors yields TES ADT thin-film transistors whose threshold voltage is lower than the threshold voltage of thin-film transistors

annealed only with dichloroethane. This result demonstrates that the material properties of the solution-processable organic semiconductor can be tuned post deposition providing us an additional degree of freedom towards functioning low-cost thin-film transistors. This flexibility in processing does not exist with vapor-deposited organic semiconductors, like pentacene.

Additionally, we demonstrated that the manner in which the electrodes are defined can significantly affect the charge-carrier mobility of TES ADT thin-film transistors. For example, when top-contact electrodes are defined by evaporating gold through a shadow mask directly on the organic semiconductor, the yield of functioning top-contact thin-film transistors is extremely low (< 25%), and of the functioning transistors, the charge-carrier mobility varies significantly (0.01 – 0.1 cm^2/V-s). In comparison, top-contact TES ADT thin-film transistors with electrodes defined separately and then laminated against the organic semiconductors have high yields (> 90%) and the devices exhibit high charge-carrier mobility (0.19 ± 0.06 cm^2/V-s). A second example demonstrates that the charge-carrier mobility of TES ADT thin-film transistors can also be affected by the method used to define bottom-contact electrodes. In this example, bottom-contact TES ADT thin-film transistors in which the gold electrodes are defined by direct evaporation through a shadow mask exhibit a charge-carrier mobility (0.11 ± 0.05 cm^2/V-s) that is approximately twice the charge-carrier mobility of bottom-contact TES ADT thin-film transistors in which the gold electrodes are defined by photolithography and lift off (0.04 ± 0.01 cm^2/V-s). In addition to affecting the charge-carrier mobility, the method used to define the electrodes can also have a significant effect on the contact resistance in the resulting thin-film transistors. Specifically, the contact resistance in top-contact thin-film transistors with directly evaporated top-contact gold electrodes (6.6 x 10^6 Ω) is an order of magnitude higher than

the contact resistance in bottom-contact thin-film transistors in which the bottom-contact electrodes were also defined by evaporation of gold through a shadow mask (3.5×10^5 Ω). This result contradicts previous literature reports which show that the contact resistance is higher in bottom-contact pentacene thin-film transistors.[4-6] All of these results emphasize the importance of adapting existing thin-film transistor fabrication techniques, or developing new thin-film transistors techniques to overcome the materials limitations of organic semiconductors in order to achieve high-performance organic devices. This point becomes especially relevant as device structures become more complicated and require additional patterning to define interconnect wiring and contacts for circuits. In particular, photolithography[7] and chemical mechanical polishing[8] are two traditional methods used for patterning interconnect wiring. These two techniques require solvents and chemical environments that are often not compatible with organic materials.[9, 10] We demonstrated a solventless printing process, nanotransfer printing (nTP), for additively patterning copper electrodes and interconnects. The nTP technique is a stamp-based technique that transfers copper features from a poly(dimethylsiloxane) (PDMS) stamp to a substrate (e.g. GaAs, silicon/silicon dioxide). Copper feature ranging in size from 1 – 500 μm are readily patterned by nTP. Unlike gold patterns printed in this manner, oligomers from the as-cast PDMS stamps permeate through the entire thickness of printed copper features resulting in non-conductive copper patterns. Leaching the PDMS stamps in hot toluene, however, successfully removes the oligomers from the PDMS stamp prior to printing. Consequently, conductive copper features with an average resistivity of 31 μΩ-cm can be patterned with leached PDMS stamps. That the PDMS oligomers present in as-cast PDMS stamps can have such a detrimental effect on the conductivity of printed metal patterns was unexpected given the large number of soft lithography techniques that utilize as-cast PDMS stamps without any significant

performance degradation. As soft lithography techniques become more prevalent for device fabrication, more metals that are prone to oxidation could potentially be transferred from PDMS stamps. It is significant therefore that residual PDMS oligomers can be removed from as-cast PDMS stamps in a straightforward manner enabling conductive metal features to be patterned.

Another aspect of thin-film transistor fabrication that is crucial for optimal organic device performance is the patterning and isolation of the organic semiconductor between adjacent devices. It is important to pattern the organic semiconductor to constrain the charge carriers to the transistor channel to minimize parasitic leakage currents and off currents, as well as to reduce electrical cross talk between adjacent thin-film transistors. We demonstrated two novel techniques for patterning TES ADT post deposition. The first technique utilizes UV light in the presence of dichloroethane solvent vapors to simultaneously pattern and crystallize TES ADT. Thin-film transistors patterned with this technique exhibit high charge-carrier mobility (0.1 cm^2/V-s) and low off currents (10^{-11} A). The second patterning technique uses a PDMS stamp to selectively remove TES ADT from the non-channel regions of the thin-film transistor. In the regions of contact between the TES ADT film and the PDMS stamp, the TES ADT diffuses into the PDMS stamp. This technique can be used to pattern both as-spun and crystalline TES ADT films. Longer PDMS contact times are required to completely remove crystalline TES ADT. Crystalline TES ADT thin-film transistors patterned with this technique exhibit an average charge-carrier mobility of 0.2 cm^2/V-s and low off currents on the order of 10^{-11} A, while amorphous TES ADT films that are patterned and then crystallized exhibit an average mobility of 0.1 cm^2/V-s and off currents on the order of 10^{-10} A. Both patterning techniques successfully eliminate leakage currents and lower off currents by 2 – 3 orders of magnitude compared to the off currents in equivalent

transistors with unpatterned TES ADT. Given the limited number of techniques available for patterning organic semiconductor thin films post deposition, these results are significant in that they provide two viable options for effectively patterning organic semiconductors deposited from solution. Further, our patterning techniques allow low-cost deposition techniques that indiscriminately deposit organic semiconductor across the substrate, such as spin casting, to be utilized in the fabrication of high-performance organic thin-film transistors in conjunction with a straightforward patterning step to define the organic semiconductor region.

Overall, we have shown that there are several aspects of organic semiconductor materials design and thin-film transistor fabrication that can be controlled to yield high-performance organic thin-film transistors. The synthesis of organic materials can be specially tailored to yield solution-processable organic semiconductors that form highly-ordered thin films with 2-D π-stacking when deposited from solution. These highly-ordered organic semiconductor thin films can yield thin-film transistors with high charge-carrier mobility. We can further improve the charge-carrier mobility of devices containing these solution-processed organic thin films by choosing techniques for establishing efficient electrical contact to the organic semiconductor. Additional device improvements, such as low leakage currents and off currents, can be achieved in solution-processed organic thin-film transistors by patterning the organic semiconductor film with a technique that accounts for the inherent materials limitations of organic semiconductors.

FUTURE WORK:

As we have shown throughout this dissertation, processing can have a significant effect on organic thin-film transistor performance. In particular, processing that affects the condition of the dielectric surface critically affects the continuity and molecular ordering of solution-deposited organic semiconductor thin films and the threshold voltage of organic thin-film transistors.[11-14] Future work is warranted to determine how the dielectric surface energy can be controlled through cleaning and/or chemical modification to routinely yield continuous, well-ordered TES ADT films, and consequently TES ADT thin-film transistors with high charge-carrier mobility ***and*** low threshold voltage. For example, treating the dielectric surface with hydrophobic molecules, such as hexamethyldisilazane (HMDS) or octadecyltrichlorosilane (OTS), molecules shown to increase order in pentacene thin films,[14-18] yield discontinuous TES ADT films from solution processing. Since lowering the dielectric surface energy does not yield continuous TES ADT thin films, exploring alternate surface treatments that increase the surface energy of the dielectric surface are warranted to determine if highly-ordered TES ADT films can be obtained from solution deposition techniques. Additionally, it is worth examining if surface treatments can be used to lower the threshold voltage of TES ADT thin-film transistors. There already exist several examples in the literature that describe how self-assembled monolayers with headgroups of varying dipoles can be used to modify the threshold voltage of pentacene thin-film transistors.[11, 12] For example, treating the dielectrice surface with a $–NH_2$ terminated monolayer prior to organic semiconductor deposition yields pentacene thin-film transistors with negative threshold voltages while treatment with a $–CH_3$ terminated monolayer yields pentacene thin-film transistors with a positive threshold voltage.[12] Efforts should be made to determine if a similar approach will work with TES ADT thin-film transistors. Combining dielectric

surface treatments and solvent-vapor annealing has the potential to yield highly-ordered TES ADT films that can in turn yield tunable, high-performance organic thin-film transistors. These experiments need not be limited to TES ADT and could be conducted with other promising solution-processable organic semicondutors as they are identified.

Another approach worth pursuing is varying the dielectric material to determine how particular gate dielectric materials affect solution-processed organic thin-film transistor performance. For example, when hydroxyl-free polymers, such as divinyltetramethylsiloxane-bis(benzocyclobutene), are used as gate dielectrics in polymer thin-film transistors, several semiconducting polymers (e.g. poly(fluorine)-based and poly(p-phenylenevinylene)-based polymers) show ambipolar charge transport.[19] Efforts to determine if ambipolar transport exists in solution-processable small-molecule organic semiconductors is warranted.

Related to the discussion above is understanding how modification of the interfacial chemistry between the organic semiconductor and electrode surfaces can be utilized to reduce contact resistance (charge-carrier injection/extraction barrier) at the organic semiconductor-electrode interfaces. Methods for improving the charge injection and extraction at the gold source and drain electrodes with interfacial chemistry are worth exploring. This can be accomplished, for example, by treating the electrodes with self-assembled monolayers that are strongly electron withdrawing such as pentfluorobenzenethiol (PFBT) and nitrobenzenethiol.[20-22]

Also, the solution-processable organic semiconductor TES ADT-F warrants further consideration. We have already demonstrated that modification of the gold electrodes with pentafluorobenzethiol improves the charge-carrier mobility of drop cast TES ADT-F thin-film transistors by an order of magnitude. Future research efforts should explore whether dielectric surface treatments, similar to the ones discussed above,

can be used to further improve TES ADT-F thin film transistor performance (i.e., increase charge-carrier mobility and on/off current ratio, and lower the threshold voltage).

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Vita

Kimberly Christine Dickey was born to Richard and Linda Felmet on December 10th, 1977 in Buffalo, New York. She graduated from Warren Area High School in 1995. After graduating from high school, Kimberly attended Cornell University where she obtained her bachelor's degree in Chemical Engineering in 1999. While attending Cornell University, Kimberly participated in the engineering co-op program, completing two co-op terms with Schering-Plough, a pharmaceutical company located in Union, New Jersey. At Schering-Plough, Kimberly assisted with the start-up of a brand new pilot plant. After graduating from Cornell University, Kimberly accepted a full-time position with Merck and Co., Inc., a pharmaceutical company located in Rahway, New Jersey. Kimberly worked at Merck for three years performing process scale-ups, producing pharmaceutical compounds to support clinical and safety trials, and transferring production processes to the manufacturing division. While at Merck, Kimberly met her future husband, Michael Dickey. In 2001, Kimberly decided to pursue a doctorate degree at The University of Texas at Austin, where she spent the next four and a half years researching solution-processable materials for organic electronics.

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