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Planar *p–n* Junction Based on a TMDs/Boron Nitride Heterostructure

Abdurrahman Ali El Yumin, Jie Yang, Qihong Chen, Oleksandr Zheliuk, and Jianting Ye*

Transition metal dichalcogenides (TMDs) are attracting growing interest for their prospective application in electronic and optical devices. As a leading material in researches of two-dimensional (2D) electronics, although band structure is layer-dependent, the TMDs show ambipolar properties. While optically excited light emission has been widely investigated, study on electrically generated emission is still limited. Taking the advantage of its ambipolarity and presence of direct band-gap in monolayer, we developed an electrically driven light emitting device based on stacked 2D flakes to obtain sharp planar *p–n* junction in monolayer. Specifically, we have fabricated atomic-layer TMDs/boron nitride (BN) artificial heterostructures using stacked h-BN thin flake as a mask to partially cover the TMDs transistor channel allowing high-density hole accumulation (*p*-region) via localized exposure to gate-controlled accumulation of anions. Transport through the junction shows typical diode-like rectification current with accompanying strong and sharp light emission from the crystal edge of BN mask for the monolayer case.

1. Introduction

Transition metal dicalcogenides (TMDs) such as WS_2, MoS_2, $MoSe_2$, and WSe_2 shows unique layer dependent properties such as indirect-direct band gap transition. Strong photoluminescence (PL), and the large exciton binding energy observed in semiconducting TMD monolayers is due to the absence of interlayer coupling and the lack of inversion symmetry,[1–4] which has made monolayer TMDs promising for various functionalities in ultrathin, flexible, and transparent devices, such as transistor,[5,6] photo detector,[7] and light-emitting diodes.[8–11]

Studies of electronic and optical properties of monolayer TMDs have been widely performed. The exciton and its derivative such as trions and biexcitons has been conducted mostly by optical pumping.[12–16] The measurements include PL dependence of carrier density controlled by electrical field, optical fluence, and circularly polarized incident light.[3,13,17–20] Recently, features of electrically induced light emission has been studied although the magnetic induced valley polarization[21] and chiral light-emitting transistor.[10,22] Specifically, the experiments of electroluminescence (EL) have been performed on lateral or vertical *p–n* junction by irradiative recombination of electrically generates electrons and holes. The out-of-plane *p–n* junction was usually fabricated as 2D heterostuctures by stacking two or more monolayer with different intrinsic doping such as *p*- and *n*-type semiconductors.[23–25] Meanwhile, light emitting diodes (LEDs) based on exfoliated $MoSe_2$, WSe_2, and WS_2 have been realized also by electrostatically induced *p–n* homojunctions using two independent gate in the in-plane adjacent regions.[8–11] Alternatively this lateral *p–n* junction can also be made by doping a partially covered few-layer MoS_2 chemically.[26]

For application in valley optoelectronics, lateral *p–n* junction configuration is more favorable as electronic transport can be confined to the in-plane direction of the monolayer devices. Recent studies reported that the circular polarized transition is sensitive to the relative angle between the crystal orientation and the field direction[10,27] thus fabricating sharp *p–n* interface with highly controllable orientation is high demanded in the future device applications.

In this paper, we report the fabrication of lateral *p–n* junction based on stacking TMDs/boron nitride (BN) heterostructures. The TMD flakes were prepared by mechanical exfoliation for few layer samples and CVD growth for monolayer. For making *p–n* junctions, the TMD flakes are partially covered by few-layer BN as insulating mask, which prevents charge accumulation under the BN mask. Whereas, in exposed region, carriers are induced electrostatically using ionic gating,[28] which is much efficient than conventional solid state gating[6,29,30] for accessing ambipolar transport of TMDs. To stabilize ion movement, the so-called freezing-while-gating technique was performed by freeze the ionic liquid below its glass transition temperature.[29] The as prepared devices, shows gate tunable diode rectification and sharp EL emission profile. For monolayer case, strong EL in visible range ($\sim$620 nm) indicates well-defined lateral *p–n* junction interface. Furthermore, our EL spectra measurement

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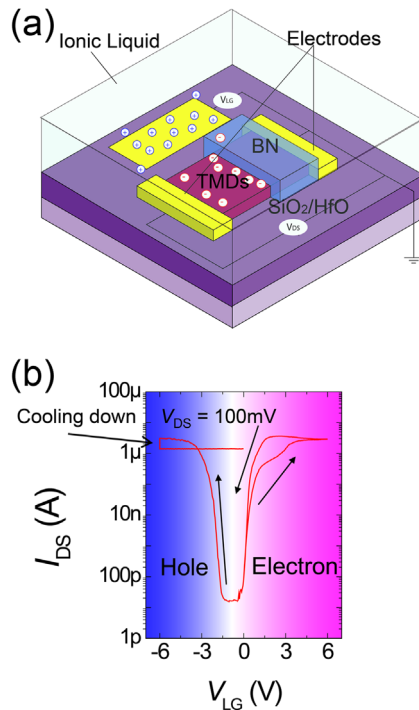
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Figure 1. (a) Schematic cartoon of atomic layer TMDs planar p–n junction device. (b) Transfer characteristic of few-layer MoS_2 using ionic liquid gate at $T = 220$ K. Note that the insulating region is slightly shifted to the negative side indicating intrinsic electron doping in the sample. To accumulate hole carrier in exposed area, we gated our device to $V_{LG} = -6$ V and immediately cooled down to fix ion movement.

indicates signature of charged exciton emission by comparison with PL spectra, which occurs in the high carrier density regime.

2. Device Fabrication

Figure 1(a) shows the schematic structure of planar p–n junction made on MoS_2 flakes. The TMD flake is partially covered by BN masking the vertical electric field from ionic gating. For multilayer devices, few atomic layers MoS_2 and BN are prepared from mechanical exfoliating $2H$-MoS_2 and h-BN on SiO$_2$/Si substrate (SiO: 285 nm). For monolayer case, we use monolayer WS_2 grown by chemical vapor deposition on SiO$_2$/Si substrate.[31] The as grown monolayers are subsequently transferred onto HfO/Si substrate (HfO: 50 nm). We patterned contact electrodes (Ti/Au: 0.5/40 nm) into hall bar configuration by e-beam lithography and e-beam evaporation (TFC-2000). The few-layers BN ($d = 20$–30 nm) were laminated onto the channel after lifting off the device to reach partial coverage using the dry transfer method.[32]

The transistor operates by gating (N,N-diethyl-N-methyl-(2-methoxyethyl) ammonium bis (triluoromethy-lsulfonyl) imide) (DEME-TSFI), a typical ionic liquid widely used in ionic gating. Compared to conventional solid gate, high gate efficiency in ionic gating can more effectively induce large hole concentration. The high efficiency of this gating method has been proven for inducing $n_{2D} = 10^{14}$ cm^{-2}, which allows routinely access to

the ambipolar characteristics of n-type semiconductor (e.g., MoS_2) and also superconductivity.[6,33] The electrical transport and optical spectroscopy were performed under high vacuum (10^{-6} mbar). Figure 1(b) shows electrical transfer curve for few-layer MoS_2 EDLTs of the area exposed to ionic liquid. The device clearly shows ambipolar behavior with the insulating region slightly shifted to the negative side indicating low electron doping and intrinsic semiconducting behavior. To accumulate holes, we applied V_{LG} up to -6 V until the source drain current I_{DS} started to saturate. Then, we immediately cooled down the system below the glass transition temperature ($T = 170$ K) to fix this partial doping configuration.

3. Results and Discussion

Figure 2 shows the source drain current–voltage (I–V) characteristics of few-layers MoS_2 p–n junction devices. Here, we investigate two devices of 4 and 13 nm, which are estimated by optical color contrast. One can see that both of devices show diode rectification behavior as a function of source and drain bias. The increase of back gate voltage clearly enhances forward-bias current. However, as shown in Figure 2(a), the reverse bias current increases significantly after $V_{BG} = 30$ V for 13 nm sample. On the other hand, as shown in Figure 2(b), the thinner 4 nm device shows that rectification of the p–n junction is preserved even at high back gate voltage $V_{BG} = 100$ V. This two different rectification behaviors are due to formation of different p–n junctions in flakes of different thicknesses. As schematically drawn in Figure 2(c), the effect of liquid gate only occurs in the proximity of surface layer, while the bottom layers remain in intrinsic state. Hence, for thicker device, the increase of reverse-bias current is attributed to unintended formation of conduction channel due to backgate-induced carrier accumulation at the bottom surface of the flake. Whereas, this conduction channel cannot form as the additional layer in thinner device because of influence of electrical field from the top ionic gating.

To understand the different rectification in different thicknesses, we performed numerical calculation to obtain potential distribution under both liquid gate and back gate in both vertical and horizontal direction. To calculate the potential distribution, we numerically solve the two-dimensional (2D) poisson equation

$$-\nabla^2 V(x, z) = \frac{\rho}{\varepsilon_r \varepsilon_0}, \tag{1}$$

where $V(x, z)$, ρ, ε_r, and ε_0 correspond to potential at (x, z), charge density, dielectric constant, and permittivity in vacuum, respectively. The calculation uses 2D finite different methods by setting the charge density as 10^{14} cm^{-2} for exposed channel surface (by ionic gating) and 5×10^{12} cm^{-2} for the bottom surface (by back gating). Figure 2(d) shows the numerical solution of Eq. (1). Potential distribution in vertical region can be divided into three region; top channel (A), insulating channel (B), and bottom channel (C). Channel A represents the channel where the actual rectification of p–n junction occurs as the ionic liquid induce hole accumulation only close to the top surface. When the applied back gate increases, the carrier also can be accumulate in bottom layer creating additional conducting channel (C).
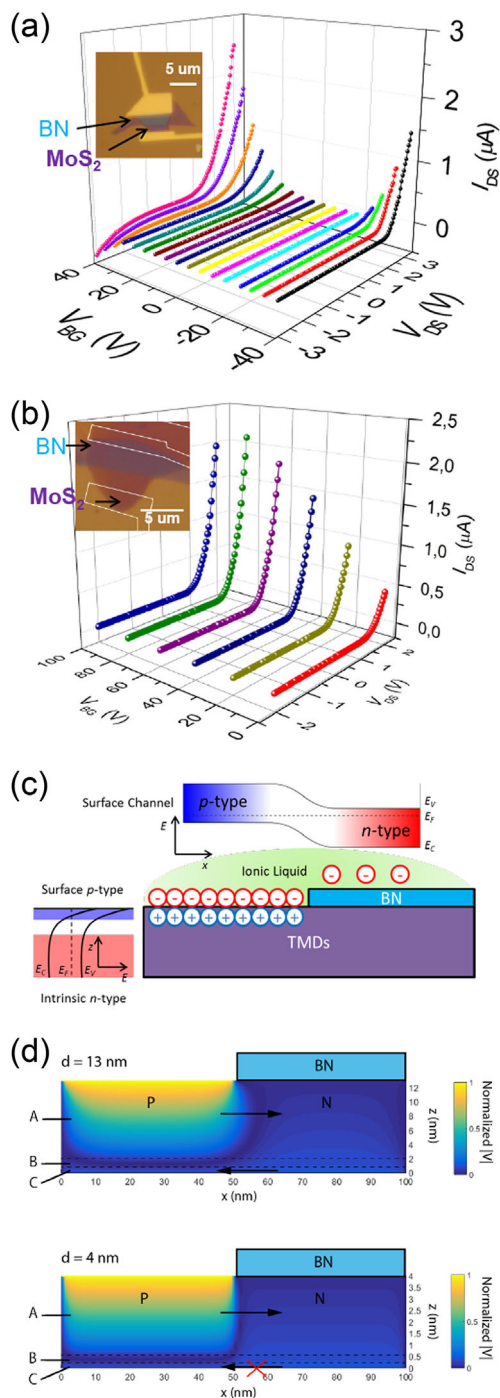
Figure 2. (a) I–V characteristic of 13 nm thickness MoS$_2$ planar p–n junction device in fixed liquid gate $V_{LG} = -6$ V under various back gate voltage. Note that the reversed-bias current starts to increase after $V_{BG} = 30$ V at $T = 170$ K. (b) I–V curve of 4 nm MoS$_2$ p–n device under similar gating condition with (a). Here, one can see no reversed-bias current observed even in high back gate $V_{BG} = 100$ V. (c) Schematic band structure in vertical direction (side panel) and surface channel (upper panel). (d) Normalized potential distribution of device under both liquid- and back gate in vertical direction. Position A, B, and C are top channel, insulating channel, and bottom channel, respectively, as described in text.

In thick layer device, the thickness of this bottom conduction channel can be estimated as ∼1 nm, which is bigger than thickness of monolayer MoS$_2$ ($d = 0.6$ nm). Therefore, this layer can be enhanced as the applied back gate increases yielding conducting state on the bottom part (channel C). Moreover, this bottom layer behaves a transistor channel when the reverse bias is applied. In contrast, this is unlikely happened in thinner layer case as the bottom layer thickness is estimated less than 0.5 nm, smaller than the thickness of monolayer, implying the applied back gate cannot provide additional access from bottom. In addition, when the negative back gate is applied as shown in Figure 2(a), channel C becomes insulating and electrical transport only occurred in channel A.

To investigate optoelectronic properties, we chose CVD grown monolayer WS$_2$ as our channel material because of the much higher quantum efficiency in monolayers. Our monolayer device was fabricated on HfO high-k dielectric substrate to enhance back gate efficiency. The formation p–n junction was performed by the previous method used in few layers. As shown in **Figure 3** (a), the I–V rectification of monolayer device is. As one can see, transport through p–n junction shows typical diode-like rectification current with accompanying strong and sharp light emission from the crystal edge of BN mask (see inset) at 170 K under $V_{BG} = 4.5$ V. In addition, no indication of reverse bias current observed until $V_{DS} = -3$ V indicating strong p–n junction formation in the p–n interface.

The back gate dependence of rectification at $T = 80$ K is displayed in Figure 3(b). Just like in the case of few layer devices, similar forward-bias enhancement also occurs as increase of the back gate. From logarithmic scale plot, the rectification start to occur at $V_{BG} = 1.8$ V implying the transition between insulating state and p–n junction formation in n-type region. Furthermore, the ideality factor n of p–n junction can be determined by theoretical fitting using extended Shockley diode equation[11,34]:

$$I_{DS} = \frac{nV_T}{R_S} W\left[\frac{I_0 R_S}{nV_T} \exp\left(\frac{V_{DS} + I_0 R_S}{nV_T}\right)\right] - I_0, \qquad (2)$$

where W is Lambert-function, I_0 is reverse-bias current, R_s is series resistance. The $V_T = k_B T/q$ is thermal voltage at temperature T. Here, k_B is the Boltzmann constant, and q is electron charge. The obtained n values is bigger than 2 exceeding the limit of the ideal diode and Shockley–Read–Hall (SRH) recombination theory.[35] This large n value is typically observed in GaN based p–n junction due to presence of tunneling mechanism in carrier transport process.[36–38] From the calculation, we observed that the ideality factor remain constant from 3 to 5 V with average $n_a = 6.8$ indicating the p–n junction operation and the recombination process is independent on the change of carrier density in this regime. It indicates that the carrier density at optimum operation regime only affects the series resistance of p–n junction device after establishing the p–n junction.

As shown in Figure 3(c), the electroluminescence (EL) spectra of monolayer device is compared with its photoluminescence (PL) spectra. The EL measurement was performed under $V_{BG} = 4.5$ V and injection current $I_{DS} = 13.9 \, \mu$A, While the PL measurement was taken in as-grown CVD monolayer. The comparison shows that the EL spectra (red line) are red-shifted compared to the PL spectra.
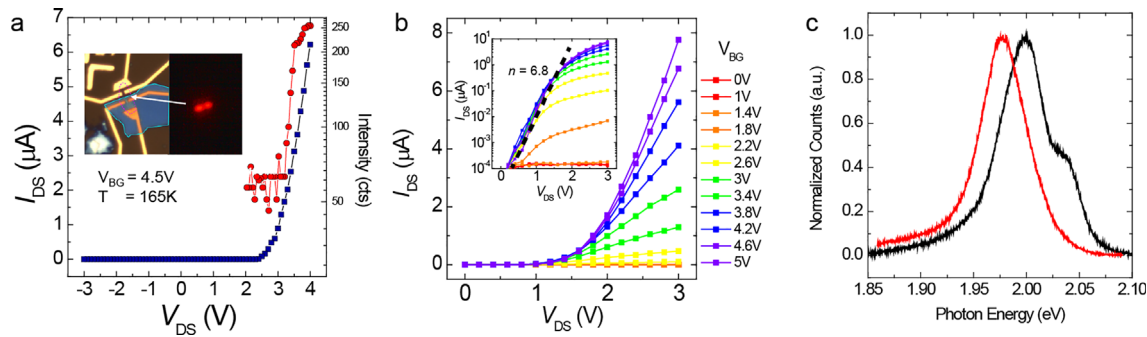
Figure 3. (a) Device operation of planar monolayer p–n junction under 4.5 V backgate voltage and −5 V liquid gate at temperature 165 K. Blue square and red round symbols represent, respectively, source–drain current and intensity detected by CCD camera as function of voltage bias. Inset: Microscopy images of p–n junction device (left panel) and light emission taken at 100 ms exposure time (right panel). (b) Electrical performance under forward bias at different backgate conditions at 80 K. Inset: logarithmic scale of I–V curve with dashed line corresponding to ideality factor. (c) EL (red) and PL (black) spectra at 80 K. The PL spectrum was taken under 650 μW m^{-2} fluence power.

We attribute the peak shift to the different carrier density induced in the sample. In EL case, the carrier was accumulated by both liquid- and back gate so that overall carrier density is estimated as in the order of 10^{13} cm^{-2}. Under the influence of doped carrier, the recombination process can involve charged exciton which has lower photon energy than that from intrinsic exciton PL.[12,39] Therefore, we suggest that the light emission of our monolayer device is dominated by charged exciton. Furthermore, recent studies also shows that crystal defect due to impurities or transfer process can trigger this charged exciton emission.[16,40] In our case, the p–n junction device is fabricated by transferred CVD grown monolayer flakes. Hence formation of defect is highly possible. The influence of crystal defect can be observed in PL spectra where peak shoulder exists at higher photon energy.

4. Conclusions

In conclusion, we demonstrated diode rectification behavior in our lateral p–n junction based on atomic layer TMDs/BN heterostructures. In few layer samples, the rectification behavior is thickness dependent where additional conduction layer is formed in bottom surface, which clearly affects device performance under high back gate bias. For monolayer case, light emission from the crystal edge of BN mask has been observed indicating sharp and well-defined p–n junction. Furthermore, our EL spectra measurement indicates signature of charged exciton emission by comparison with PL spectra due to the high carrier density induced in our sample.

Conflict of Interest

The authors declare no conflict of interest.

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