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# Field-Effect Transistors Based on Formamidinium Tin Triiodide Perovskite

*Shuyan Shao, Wytse Talsma, Matteo Pitaro, Jingjin Dong, Simon Kahmann, Alexander Joseph Rommens, Giuseppe Portale, and Maria Antonietta Loi**

**To date, there are no reports of 3D tin perovskite being used as a semiconducting channel in field-effect transistors (FETs). This is probably due to the large amount of trap states and high p-doping typical of this material. Here, the first top-gate bottom-contact FET using formamidinium tin triiodide perovskite films is reported as a semiconducting channel. These FET devices show a hole mobility of up to 0.21 cm$^2$ V$^{-1}$ s$^{-1}$, an $I_{ON/OFF}$ ratio of $10^4$, and a relatively small threshold voltage ($V_{TH}$) of 2.8 V. Besides the device geometry, the key factor explaining this performance is the reduced doping level of the active layer. In fact, by adding a small amount of the 2D material in the 3D tin perovskite, the crystallinity of $FASnI_3$ is enhanced, and the trap density and hole carrier density are reduced by one order of magnitude. Importantly, these transistors show enhanced parameters after 20 months of storage in a $N_2$ atmosphere.**

## 1. Introduction

The charge-transport properties of semiconductors are one of the most critical physical properties for the functioning of optoelectronic devices such as solar cells, light-emitting diodes, and field-effect transistors (FETs). Investigations of charge transport in the field-effect transistor configuration are very useful as they can give indication of the material properties with a relatively simple experiment, which is very appropriate for comparative studies.[1–8]

In the past several years, organic metal halide perovskites have been emerging as a class of promising semiconducting materials for optoelectronic devices.[7,9–21] However, for quite a long time it had been very difficult to investigate the charge-transport properties in FETs; reasons for this difficulty have been accounted to ion migration, structural polarization, and phonon scattering, which have negative effect as they can screen the gate electrical field. Early research works failed to obtain well-behaving metal halide perovskite FETs at room temperature. Only recently, researchers have partially overcome the great difficulties in fabricating lead halide perovskite-based FETs, and not only 3D lead halide perovskites but also the lead-based 2D Ruddlesden–Popper (R–P) homologous ($A'_2A_{n-1}Pb_nX_{3n+1}$, $n = 1$), in the form of thin film and single crystals, have been investigated as FET-active materials.[7,10,21,22]

Among the tin-based halide perovskites, only 2D R–P ($n = 1$ phase) such as $PEA_2SnI_4$ (PEA is phenylethammonium) has been investigated in FETs. Due to the quantum and dielectric confinements in R–P perovskite, the charge tunneling perpendicular to the inorganic layers is strongly inhibited, and the charge transport is mostly confined in the 2D corner sharing inorganic octahedral layer. Therefore, structural defects with the alignment of the inorganic layers not parallel to the substrate are very detrimental to the performance of FETs. In the past, strategies to eliminate the grain boundaries such as enlarging the grain size and growing single crystals were developed to improve FET's performances. In 1999, Kagan et al. reported a hole mobility of 0.6 cm$^2$ V$^{-1}$ s$^{-1}$ in a transistor with bottom-gate and bottom-contact geometry, which used as a semiconducting channel a spin-coated R–P tin halide of formula, $PEA_2SnI_4$.[20] Mitzi et al. improved the hole mobility to 2.6 cm$^2$ V$^{-1}$ s$^{-1}$ with a superior $PEA_2SnI_4$ film morphology, which was obtained with a low-temperature melt-processing technique.[23]

Traps on the surface of the dielectric layer can capture free charges in the semiconducting channel impeding in this way charge transport. Matsushima et al. succeeded in enhancing the hole mobility of the transistor by passivating the trap states at the silicon dioxide surface with a self-assembled monolayer containing $NH_3I$ terminal groups.[24]

FETs being interface-based devices, the device geometry and the position of the dielectric layer with respect to the active layer are very critical for the FET functioning. The energy barrier at active material/source (drain) interface is also extremely important as a large Schottky barrier can strongly inhibits the injection in the semiconductor channel and limits the device

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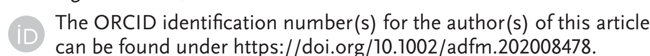
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performance. Matsushima et al. improved the hole mobility of $PEA_2SnI_4$ up to 15 $cm^2 V^{-1} s^{-1}$ by using a polymer with high dielectric constant as the dielectric layer and minimizing the hole injection barrier with $MoO_3$ interfacial layer in FET with top-gate and top-contact geometry[24–26] To summarize, the charge-transport properties of the R–P tin perovskite materials were found to highly depend on the film morphology, device geometry, surface trap passivation, and energy barrier at the source/drain contact.

Unlike the 2D R–P, because of the absence of quantum- and dielectric-confinement effects, the 3D tin perovskite materials potentially enable much faster charge transport.[27,28] Moreover, 3D tin perovskite should enable charge transport in three dimensions. However, it is unclear how the crystallographic properties and microstructures of these 3D tin perovskite films influence their transport properties.

However, the investigation of the charge-transport properties of the 3D tin-based perovskites is impeded by the big difficulties in fabricating a working FET. This is most probably associated with the notorious high p-doping level of the 3D tin perovskite due to the large amount of trap states, in particular, tin vacancies.[29–31] As a consequence, the quantity of holes in tin perovskites overwhelms the injected ones, compromising the possibility of controlling the conduction with the gate field. As a small gate voltage is not enough to deplete these holes in the semiconducting channel, this poses challenges to switch off the transistor. Therefore, in order to get good performance for these devices, effective strategies to eliminate the tin vacancies should be developed.

In one of our recent works, we successfully reduced the p-doping level (hole density) in 3D formamidinium tin triiodide ($FASnI_3$) perovskite of more than one order of magnitude by incorporating a small amount of the 2D R–P tin perovskite.[30] The addition of the R–P phase enhances enormously the crystallinity and the orientation of the 3D phase. The highly ordered 3D phase is potentially very interesting for its application as an active layer in FETs. This gives us the motivation to investigate its charge-transport properties. We fabricated reference FETs, which use pure 3D tin perovskite film as the semiconducting channel, in bottom-gate bottom-electrode configuration, with $SiO_2$ as the dielectric material. These devices, as expected, failed to show field-modulated charge transport due to high density of holes ($5.8 \times 10^{17}$ $cm^{-3}$) in the channel. Conversely, the FETs using the 2D/3D perovskite semiconducting channel show field-induced p-type conduction in the same device geometry due to the reduced hole carrier density ($10^{16}$ $cm^{-3}$). The FET using a 48 nm thick 2D/3D layer shows a hole mobility extracted from the linear region of 0.12 $cm^2 V^{-1} s^{-1}$ and a threshold voltage ($V_{TH}$) of 28 V. Compared to the FET based on 2D/3D, the FET based on pure 2D R–P layer shows an inferior hole mobility in the order of $10^{-3}$ $cm^2 V^{-1} s^{-1}$ due to the combined quantum- and dielectric-confinement effects and larger injection barrier at the perovskite/bottom-electrode interface. An improved device structure, using $Al_2O_3$ as the top-gate dielectric, allows us to reduce significantly the $V_{TH}$ to 2.8 V as a direct consequence of the oxide high capacitance. Moreover, in this optimized device geometry, the hole mobility is increased up to 0.21 $cm^2 V^{-1} s^{-1}$ with an $I_{ON/OFF}$ ratio of $10^4$. Interestingly, these devices show mostly improved performances after 20 months of storage in $N_2$ atmosphere.

## 2. Results and Discussion

We prepared the 3D and 2D/3D films with a thickness of around 306 nm following the previously reported procedure for the fabrication of solar cells.[30] Figure S1 (Supporting Information) shows the X-ray diffraction (XRD) patterns of these two films. The 3D film is composed of randomly oriented grains, exhibiting the diffraction peaks of (100), (120), (122), and (200) planes. In contrast, the 2D/3D film is composed of highly oriented grains, showing dominant diffraction peaks of (100) and (200) planes. It is noteworthy that the 2D/3D film shows significantly higher crystallinity as compared to 3D film, which is evidenced by the intense and narrower diffraction peaks. Though we refer to this sample as 2D/3D in order to differentiate it from pure 3D sample, the diffraction peak from the 2D phase at lower $2\theta$ angle is negligible due to its small amount. Therefore, the 2D/3D sample can be treated as highly crystalline and oriented 3D phase. This is further confirmed by the fact that both films show practically the same absorption spectra (Figure S2, Supporting Information). In order to gain deeper insight into the orientation and the phase distribution, **Figure 1**a,b displays the grazing incidence wide-angle X-ray scattering (GIWAXS) images of the 3D tin perovskite films detected at X-ray incident angles of 0.25° and 2.0°, respectively. The diffraction rings verify that the entire 3D film is composed of randomly oriented 3D grains (Figure 1c). Figure 1d,e displays the GIWAXS images of the 2D/3D films recorded under the same experimental conditions, where it is evident that the top part of the film consists of pure 3D grains, whereas the bottom part consists of 3D grains and of a very small amount of $PEA_2FASn_2I_7$ ($n = 2$ phase) (Figure 1f). The 3D grains of the 2D/3D film are oriented with *h00* planes packing dominantly in the out-of-plane direction over the in-plane direction, and the $n = 2$ phase is oriented with the inorganic layers parallel to the substrate. The high crystallinity and orientational order observed in 2D/3D film are associated with the changes in the crystallization process, in which 2D tin perovskite promotes the surface crystallization of the 3D tin perovskite.[32] Figure S3 (Supporting Information) shows the atomic force microscopy (AFM) images of the two films. The pure 3D film exhibits large grains with sharp grain boundaries, while the 2D/3D film shows fused grain boundaries.

**Figure 2**a shows the time-resolved photoluminescence (PL) spectra of the 3D and 2D/3D films. The 2D/3D film exhibits much slower (8.15 ns) decay dynamics of the charge carriers than the pure 3D film (1.54 ns), indicating that the highly crystalline 2D/3D film has a much lower trap density than the 3D counterpart. Seebeck coefficients of the 3D and 2D/3D films demonstrated that holes dominate the electrical conductivity.[30] Also the electrical conductivity of the 2D/3D film is considerably lower than the one of the 3D films (Figure 2b). Mott–Schottky analysis (Figure 2c) shows that the carrier density of the 2D/3D sample is about 50 times lower than that of the 3D one. These results are in agreement with the decrease of the trap states in the 2D/3D film, particularly the tin vacancies, which are one of the main factors causing the high p-doping of the tin perovskite.[30] As we discussed in the previous paragraphs, the enhanced crystallinity and orientational order are the underlying factors to reduce the trap density and p-doping level of the 2D/3D film.


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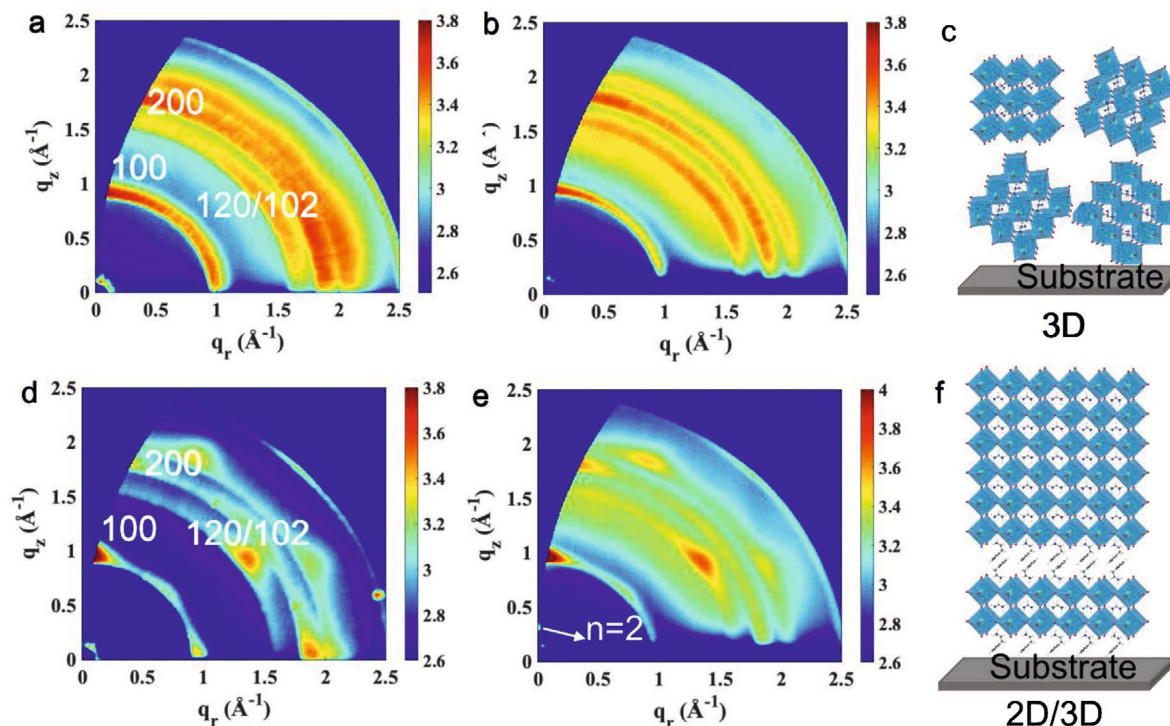


**Figure 1.** a) GIWAXS images of the a,b) 3D, d,e) 2D/3D films detected with an incident X-ray angle of 0.25° and 2.0°, respectively. Schematic illustration of the phase distribution and orientation of the c) 3D and f) 2D/3D films.

In order to compare the transport properties of these two types of films, we start the investigation with a simple bottom-gate and bottom-contact geometry as shown in **Figure 3**a. A 230 nm thick $SiO_2$ layer on commercial highly n-doped silicon substrate was used as the dielectric material, which has a capacitance of 15 nF cm$^{-2}$. Gold was used to define both source and drain electrodes. The channel length ($L$) and width ($W$) are 20 µm and 10 mm, respectively. It is noted that we only did a short UV–ozone treatment to the $SiO_2$ surface before spin-coating the perovskite layer.

Figure 3b shows the energy levels of $FASnI_3$ and Au, which are taken from a previous report.[33,34] Apparently, there is an energy barrier for hole injection at Au/perovskite interface. In one of our recent works, we found that a small quantity of lead-based R–P, $n = 2$ phase does not form a continuous thin layer, but segregates into small domains embedded in the dominant 3D lead-based perovskite matrix at the bottom of the perovskite film.[35] Since the quantity of the 2D tin perovskite in 2D/3D film in this work is very small, it is most probable that the 2D phase also forms very small segregated domains. Therefore, 3D tin perovskite dominates the energy level alignment at the perovskite/Au interface.

FETs made with the 3D film show very weak p-type field-modulated conduction. In Figure 3c, the output characteristics, reporting the source–drain current ($I_{DS}$), swept over source–drain voltage ($V_{DS}$) at specific gate voltages ($V_G$), shows a very narrow linear region (0 V ≥ $V_{DS}$ ≥ −5 V) and a broad saturated region, when a negative $V_{DS}$ is applied to the device (p-channel). It is noted that the $I_{DS}$ does not increase significantly with the gate voltage. Upon a positive $V_{DS}$ (n-channel), the device does show the sign of saturation and formation of n-type channel only at 60 V; at lower voltages only holes appear to be present. The transfer curves are almost flat over the swept gate voltage range in both the p- and n-channel, and do not show either any subthreshold regime or off state (Figure 3d). The channel has a conductivity of about 1.9 × 10$^{-2}$ S cm$^{-1}$; calculated from the linear region of the output curves in the absence of the gate voltage, this value is in good agreement with the one obtained in a lateral two-terminal device (Figure 2a). Such a high electrical conductivity is due to severe self-doping by the tin vacancies. Therefore, a very large positive gate voltage is needed to deplete the holes in the channel and turn off the transistor.

Compared to the pure 3D-based device, the FETs using 2D/3D film as the semiconducting channel show more pronounced gate-modulated conductance (Figure 3e), the $I_{DS}$ current increases significantly with the increased $V_G$. Though the transfer curves do not show a clear off state in the p-channel (Figure 3f), they show a subthreshold region. The threshold voltage is estimated to be 60 V by extrapolation of the linear region to the $x$-axis and correcting for the used $V_{DS}$. This is confirmed by transfer curves measured for the n-channel. Such an improvement in the gate-modulated conduction behavior is associated with the reduction of the trap states in the 2D/3D film, which by itself is a consequence of the high crystallinity of the thin film. The channel has a conductivity of about 1.2 × 10$^{-4}$ S cm$^{-1}$. The hole carrier density in this 2D/3D film is reduced more than one order of magnitude (1.2 × 10$^{16}$ cm$^{-3}$). The devices fabricated using 300 nm thick 2D/3D films show a low hole mobility of 9 × 10$^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ calculated from the linear region of the transfer curve in forward direction at $V_{DS}$ = −5 V (Table S1, Supporting Information). In this case, even if the transistor is still not well performing, the gate


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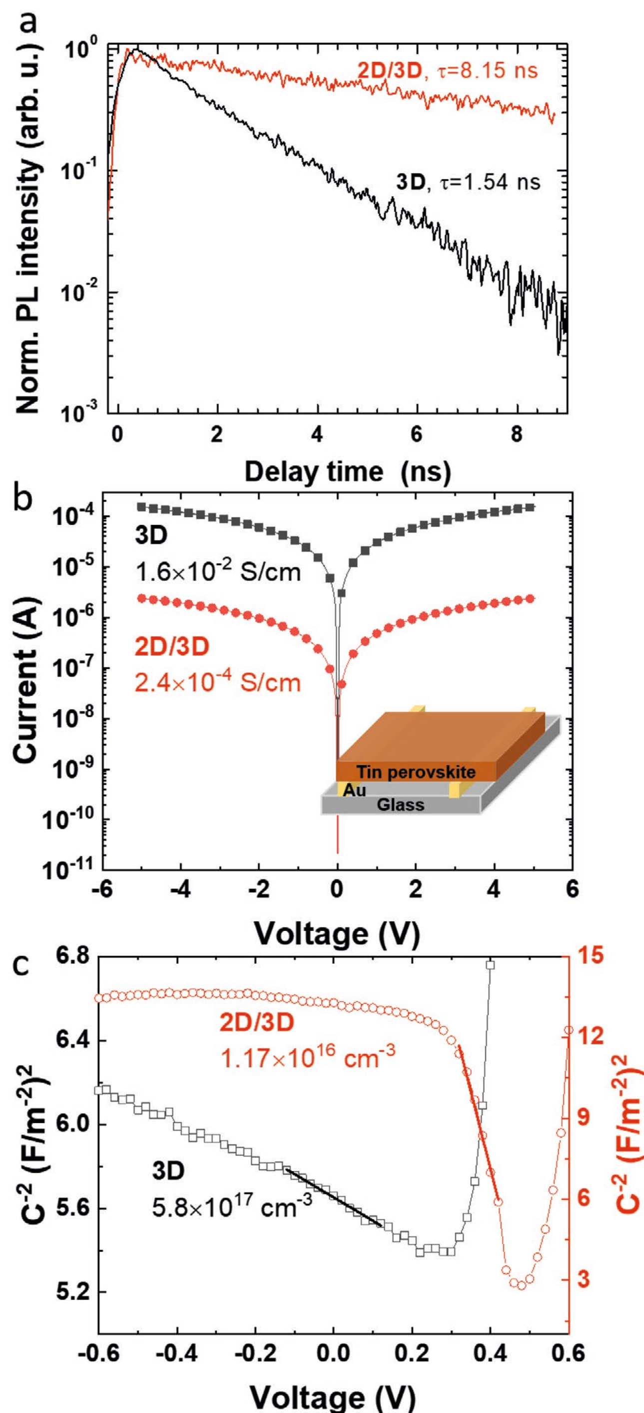


**Figure 2.** a) Time-resolved PL spectra, b) electrical conductivity, c) $C^{-2}$ as a function of bias voltage in the dark condition of the 3D and 2D/3D samples.

electrode is able to perform some modulation on the current crossing the channel.

Since the 2D/3D tin perovskite film offers superior performance compared to the 3D tin perovskite also when used as active layer of FETs, hereafter we focus on improving their performance. **Figure 4** show the output and transfer curves of the FETs with different thin-film thicknesses (110, 48, and 28 nm) to compare with the one obtained with 306 nm film. Importantly, the thinner films maintain the same crystallographic preferential orientation of the inorganic octahedron as the thick film (Figure S4, Supporting Information). The devices fabricated using 110, 48, and 28 nm thick 2D/3D films show hole mobilities of 0.07, 0.09, and 0.03 $cm^2$ $V^{-1}$ $s^{-1}$ calculated from the linear region of the transfer curve in forward direction at $V_{DS} = -5$ V (Table S1, Supporting Information). The threshold voltages estimated by extrapolating the linear region of the transfer curve in forward direction are 55.6, 45.8, and 43.1 V, respectively. These FETs exhibit higher hole mobility and smaller threshold voltage compared to the one using 306 nm thick films. In case of thick films, a large part of the thickness is unaffected by the gate electric field, causing a leakage paths and high off current due to carrier diffusion. Instead, thinner films are within the range of the gate electric field, leading to lower off current in the transistor characteristics. Figure S5 (Supporting Information) shows AFM images of the films with various thicknesses. When the film thickness decreases, more pinholes and open grain boundaries appear in the film. This is caused by the lower quantity of the ionic species in the diluted precursor solution. On the contrary of what has been previously reported for R–P based FET, it seems that the grain boundaries and pin holes are, to a great extent, less detrimental for the FETs based on 2D/3D films in the bottom-gate geometry. This is probably due to the fact that in the absence of quantum and dielectric confinement the charge transport takes place in the multiple inorganic octahedral layers of the 3D grains near the substrate. Therefore, these pinholes are not detrimental till the electrical coupling between the grains is enough to allow charge carrier percolation. For layers thinner than 28 nm, devices failed to give proper performance because the perovskite grains become isolated.

The next important question is how the quantity of the 2D perovskite influences the performance of the transistors. Three tin perovskite films (of thickness around 110 nm) with nominal compositions of $PEA_2FA_7Sn_8I_{25}$ ($n = 8$), $PEA_2FA_3Sn_4I_{13}$ ($n = 4$), and $PEA_2SnI_4$ ($n = 1$, pure 2D) were prepared (see the "Experimental Section"). The polycrystalline $PEA_2SnI_4$ film is composed of pure 2D perovskite grains, of which the $h$00 planes stack in the out-of-plane direction (Figure S6a–c, Supporting Information). The Bragg spots indicate that inorganic octahedral layers of the $n = 1$ phase are highly oriented but not perfectly parallel to the substrate. Some inorganic layers of the $n = 1$ phase are slightly tilted. Instead, the $PEA_2FA_7Sn_8I_{25}$ and $PEA_2FA_3Sn_4I_{13}$ films are composed of mixed phases including $n = 1$, 2 and $n \geq 3$ phases (Figure S6d–i, Supporting Information). Likewise, the inorganic layers of the $n = 1$ and $n = 2$ grains in those films are oriented preferentially parallel to the substrate, while the $n \geq 3$ phases are oriented with inorganic layers perpendicular to the substrates. Moreover, the $n = 1$ and $n = 2$ phases are located throughout the entire $PEA_2FA_7Sn_8I_{25}$ and $PEA_2FA_3Sn_4I_{13}$ films. Obviously, the quantities of the $n = 1$ and $n = 2$ phases in these films are much higher compared to that in 2D/3D film. In this case, the hole injection mainly occurs at the low-dimensional perovskites/Au interface, which is similar to what is happening in pure 2D perovskite/Au interface. All these devices with higher 2D content exhibit p-type gate-modulated conduction, but the $I_{DS}$s of these FETs in output and transfer curves are more than one order of magnitude lower


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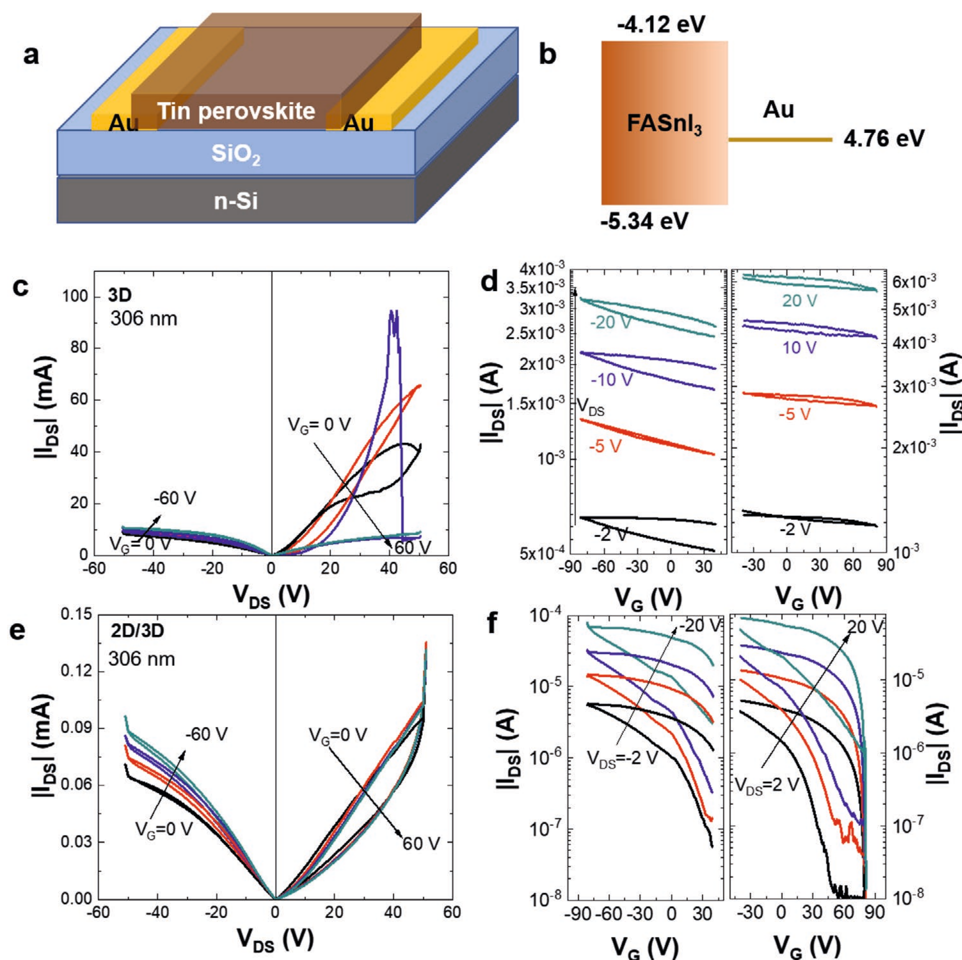


**Figure 3.** a) Bottom-gate and bottom-contact FET structure. b) The energy level of $FASnI_3$ and Au. c) Output and d) transfer curves of the FET using 3D Sn perovskite as a semiconducting channel. e) Output and f) transfer curves of a typical FET using 2D/3D Sn perovskites as the semiconducting channel. Note: the thickness of the active layer is around 306 nm.

than that of the 2D/3D film (Figure S7, Supporting Information). The hole mobility values of these FETs are in the range of $10^{-3}$ cm$^2$ V$^{-1}$ s$^{-1}$ (Table S2, Supporting Information), which is one order of magnitude lower than the FET based on 2D/3D film. This confirms that the charge injection mostly occurs at the low-dimensional tin perovskite/Au interface and subsequent transport of these charges in the $PEA_2FA_7Sn_8I_{25}$, $PEA_2FA_3Sn_4I_{13}$, and $PEA_2SnI_4$ phases is disrupted. The combined quantum- and dielectric-confinement effects cause lower charge carrier mobility of the 2D R–P than 2D/3D perovskite.[27,28] Due to the confined charge transport of these R–P films, the structural defects, such as the pin holes and grain boundaries (Figure S8, Supporting Information), and imperfect alignment of the inorganic layers with respect to the substrate (Figure S7, Supporting Information) are very detrimental to the charge transport. In other words, the R–P-based FETs require for optimal performances a more perfect microstructure, i.e., smaller quantity of pinholes and grain boundaries, and perfect parallel orientation of the inorganic layers. Furthermore, the larger inject barrier at low-dimensional perovskite/Au interface due to the deeper valence band (–5.58 eV) of these R–P phases is another factor leading to inferior hole mobility than the 2D/3D film.

Due to the advantages of the 2D/3D-based FET, we continue to improve their performance with a different device structure. In order to turn off the 2D/3D-based FET at small gate bias (low $V_{TH}$), $Al_2O_3$ gate dielectric is used in a bottom-contact and top-gate geometry (**Figure 5**a). Before the deposition of $Al_2O_3$ layer (60 nm) by atomic layer deposition (ALD), a very thin layer (≈10 nm) of polymethyl methacrylate (PMMA) is spin-coated on top of the perovskite layer to passivate its surface traps and protect it from any decomposition during the ALD process. The PMMA/$Al_2O_3$ double dielectric layers have a capacitance of 78 nF cm$^{-2}$ (see experimental details for capacitance measurements). Without the PMMA layer, the device loses its current and does not show any FET behavior (Figure S9, Supporting Information). Figure 5b,c shows the output and transfer curves of the fresh FET with a PMMA layer. Compared to those fabricated with the bottom-gate geometry, the top-gate FETs exhibit several important features: i) the output and transfer curves show much smaller hysteresis; ii) the output characteristics show a clear saturation; the on and off current ratio ($I_{ON/OFF}$) is about $10^4$; and iii) the $V_{TH}$ is of only 2.8 V. The hole mobility calculated from the linear region of the transfer curve in the forward direction is 0.21 cm$^2$ V$^{-1}$ s$^{-1}$ (at


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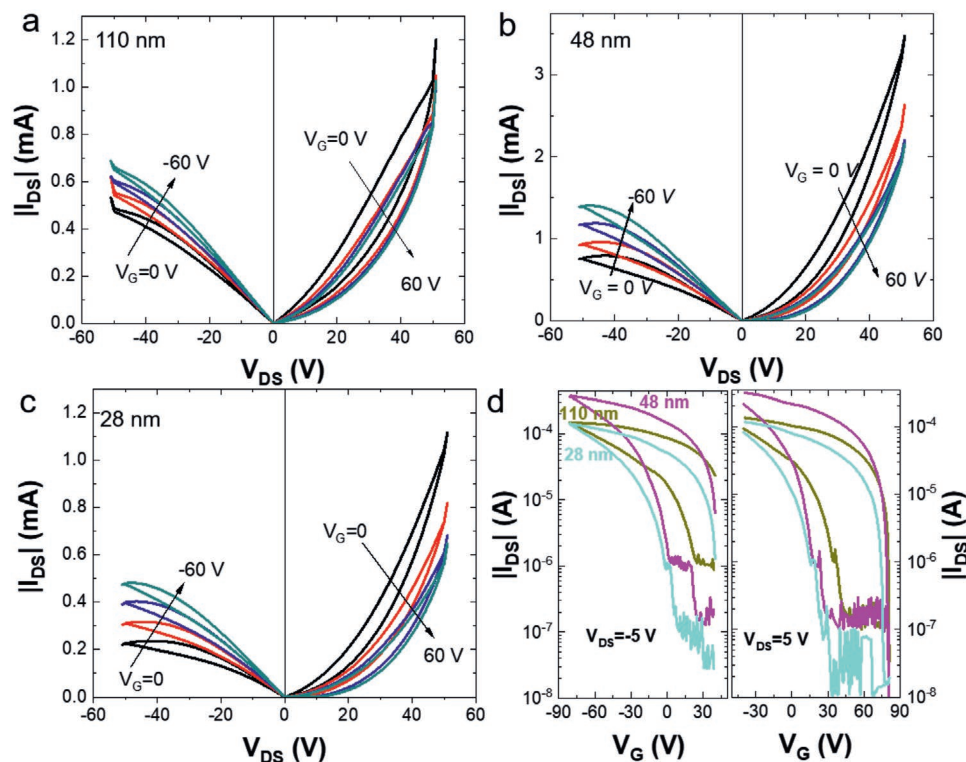


**Figure 4.** a–c) Output curves and d) transfer curves (at $V_{DS} = -5$ V) of the FET using 2D/3D Sn perovskite as a semiconducting channel with thicknesses of 110, 48, and 28 nm, respectively.

$V_{DS} = -2$ V) for a 48 nm thick semiconducting layer. Interestingly, these devices are stable when stored in a nitrogen-filled glove box. The output and transfer curves of devices stored in glove box for more than 20 months exhibit much smaller hysteresis compared to the fresh devices (Figure 5d,e); the mobility is increased (0.32 cm$^2$ V$^{-1}$ s$^{-1}$); and the $V_{TH}$ is superior to that of fresh devices. It is possible that slight change in the microstructure of the 2D/3D film or of the interface between 2D/3D film and PMMA/$Al_2O_3$ layers is responsible for the reduction of charge trapping. The only parameter that shows a degradation is the $I_{ON/OFF}$ ratio, which decreases slightly with respect to that of the fresh devices.

This is, to the best of our knowledge, the first report on well-behaving FETs using 3D tin perovskite film as a semiconducting channel. These results were achieved thanks to our recipe for enhancing the crystallization of the 3D perovskite by adding a small amount of 2D R–P phase, giving rise to a decrease of the Sn vacancies and of the hole doping. Research on pure R–P phases shows that the hole mobility of the FET was significantly improved by optimizing the fabrication process and the device structure.[21,24,25] Therefore, we believe that there is great potential, starting from these results, to further improve the figure of merit of FETs fabricated with $FASnI_3$.

## 3. Conclusion

In conclusion, we report the first top-gate, bottom-contact FET transistor using 3D tin perovskite film as the semiconducting channel. This device shows a hole mobility of 0.21 cm$^2$ V$^{-1}$ s$^{-1}$, an $I_{ON/OFF}$ ratio of 10$^4$, and a $V_{TH}$ of 2.8 V. A key factor to achieve this performance is to reduce the p-doping level of the 3D tin perovskite by adding a tiny amount of tin 2D R–P phase, which significantly improves the crystallinity and orientation of the $FASnI_3$. These devices show outstanding stability in $N_2$ atmosphere with most improved performances after 20 months of storage. Moreover, we demonstrated that the 2D/3D based FET shows higher hole mobility compared to those based on low-dimensional R–P perovskites due to their lower sensitivity to the microstructure (orientation of the inorganic planes) and lower hole injection barrier at perovskite/source interface.

## 4. Experimental Section

*Materials*: PEAI (>98%) and formamidinium iodide (FAI) (>98%) were purchased from TCI EUROPE N.V. $SnI_2$ (99.999%), $SnF_2$ (>99%), *N*,*N*-dimethylformamide (DMF) (99.8%), and dimethyl sulfoxide (DMSO) (99.8%) were purchased from Sigma–Aldrich. All the materials were used as received without further purification.

*XRD*: XRD patterns of the perovskite films were recorded on a Bruker D8 Advance X-ray diffractometer with a Cu K$\alpha$ source ($\lambda$ = 1.54 Å) and a Lynxeye detector.

*AFM*: Surface morphologies of the perovskite films were imaged by an AFM running in ScanAsyst mode, using a Bruker Dimension Icon. The AFM images were analyzed using the software Gwyddion.

*C–V, Electrical Conductivity, and GIWAXS Measurements*: *C–V*, electrical conductivity, and GIWAXS measurements were performed following the previously reported procedure.[30]

*Capacitance Measurement*: The capacitance of the PMMA/$Al_2O_3$ dielectric was measured in a sandwich device structure indium tin oxide (ITO)/PMMA/$Al_2O_3$/Al. The capacitance–frequency measurements were conducted under dark condition in a frequency range of 1–10$^6$ Hz


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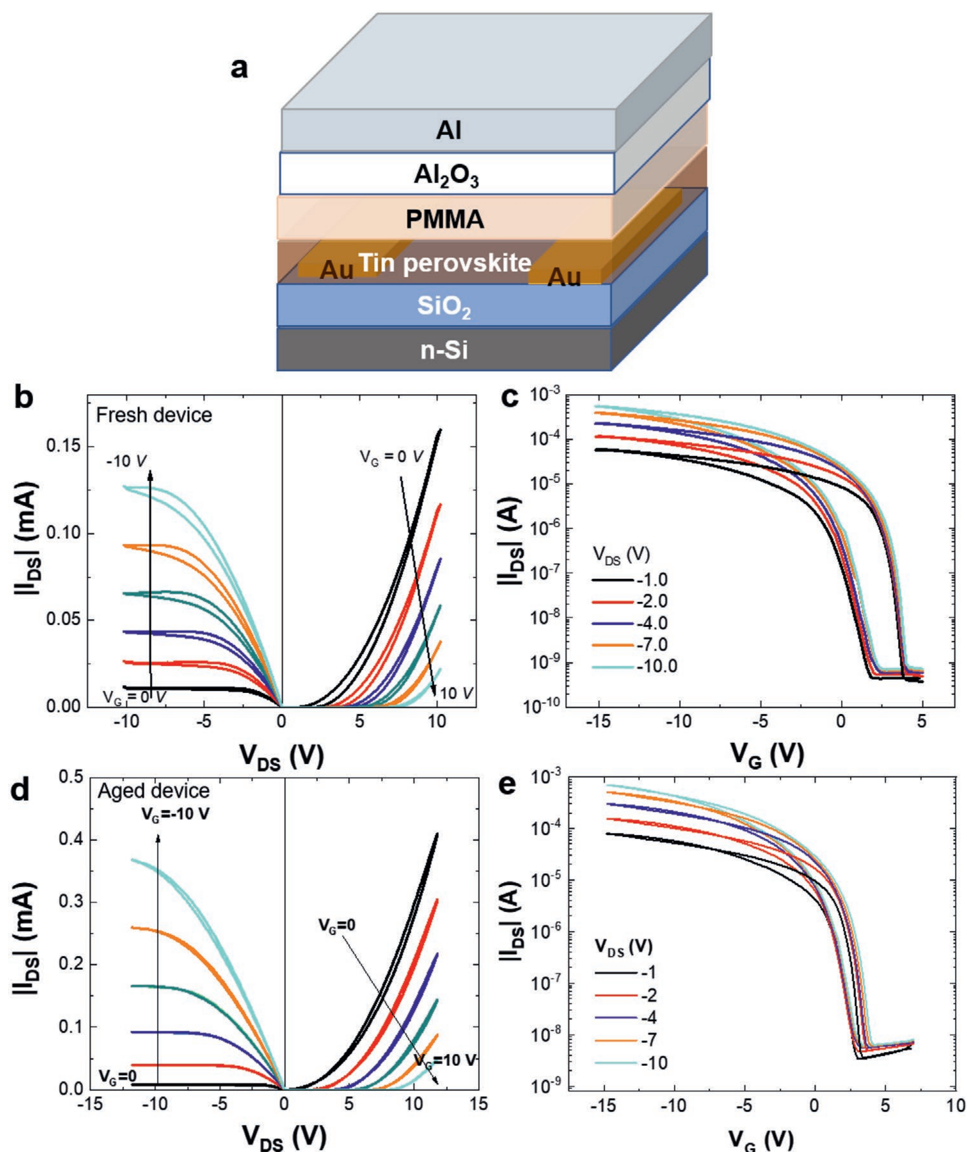


**Figure 5.** a) Top-gate and bottom-contact FET structure. b) Output and c) transfer curves of the fresh FETs using 2D/3D Sn perovskite as a semiconducting channel (thickness 48 nm). d) Output curves and e) transfer curves of the FET using 2D/3D as the semiconducting channel (thickness 48 nm) aged in the nitrogen-filled glove box for 21 months.

with an AC driving voltage of 20 mV on a Solarton 1260 impedance gain-phase analyzer.

*Device Fabrication and Electrical Characterization*: Commercially available silicon substrates (Fraunhofer Institute), consisting of on top a thermally grown $SiO_2$ dielectric layer (230 nm thickness) and lithographically defined source- and drain-bottom electrodes (10 nm ITO/30 nm Au), were cleaned using an ultrasonication bath in acetone and isopropyl alcohol. The substrates were subjected to UV–ozone treatment for 20 min, and they were then transferred to a nitrogen-filled glove box. For the bottom-gate geometry, the reference $FASnI_3$ film was spin-coated on the substrates from a precursor solution comprising 1 M FAI, 1 M $SnI_2$, and 0.1 M $SnF_2$ in mixed solvents of DMSO and DMF (1:4 volume ratio) at 4000 rpm for 60 s. Diethyl ether was used as the antisolvent during the spin-coating process. The $FASnI_3$ film was then annealed at 65 °C for 20 min. The 2D/3D tin perovskite films were obtained under the same conditions from solutions containing PEAI, FAI, $SnI_2$, and $SnF_2$ with a molar ratio of 0.08:0.92:1:0.1 ($SnI_2$ concentration: 1 M for 306 nm, 0.5 M for 110 nm, 0.25 M for 48 nm, 0.125 M for 28 nm). $PEA_2FA_7Sn_8I_{25}$ film was obtained from precursor solution containing PEAI, FAI, $SnI_2$, and $SnF_2$ with a molar ratio of 0.25:0.875:1:0.1 ($SnI_2$ concentration 0.5 M). $PEA_2FA_3Sn4I_{13}$ film was obtained from precursor solution containing PEAI, FAI, $SnI_2$, and $SnF_2$ with a molar ratio of 0.5:0.75:1:0.1. ($SnI_2$ concentration 0.5 M). $PEA_2SnI_4$ film was obtained from precursor solution containing PEAI, $SnI_2$, and $SnI_2$ with a molar ratio of 2:1:0.1 ($SnI_2$ concentration 0.5 M). For the top-gate geometry, a thin layer of PMMA (10 nm) was spin-coated on top of the perovskite films and then transferred under nitrogen atmosphere to the atomic layer deposition reactor. There, $Al_2O_3$ (≈48 nm) was deposited by ALD at 100 °C, using $H_2O$, and trimethylaluminium. Electrical measurements were performed using a probe station placed in a nitrogen-filled glove box at room temperature under dark conditions. The probe station was connected to an Agilent E5270B semiconductor parameter analyzer. The reported charge carrier mobilities were extracted from the $I_{DS}$–$V_G$ transfer characteristics in the linear regime.


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## Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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## Conflict of Interest

The authors declare no conflict of interest.

## Keywords

3D tin perovskite, dedoping, field-effect transistor, formamidinium tin triiodide, hole mobility

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