The Dissertation Committee for Junghyo Nah Certifies that this is the approved version of the following dissertation:

High Performance Germanium Nanowire Field-Effect Transistors and Tunneling Field-Effect Transistors

Committee:

Emanuel Tutuc, Supervisor

Sanjay K. Banerjee

Jack C. Lee

Ananth Dodabalapur

Leonard F. Register

Li Shi

High Performance Germanium Nanowire Field-Effect Transistors and Tunneling Field-Effect Transistors

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Junghyo Nah, B. E.; M. S. E.

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Dedication

To my wife and parents for their love and support

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High Performance Germanium Nanowire Field-effect Transistors and Tunneling Field-effect Transistors

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The scaling of metal-oxide-semiconductor (MOS) field-effect transistors (FETs) has continued for over four decades, providing device performance gains and considerable economic benefits. However, continuing this scaling trend is being impeded by the increase in dissipated power. Considering the exponential increase of the number of transistors per unit area in high speed processors, the power dissipation has now become the major challenge for device scaling, and has led to tremendous research activity to mitigate this issue, and thereby extend device scaling limits. In such efforts, non-planar device structures, high mobility channel materials, and devices operating under different physics have been extensively investigated. Non-planar device geometries reduce short-channel effects by enhancing the electrostatic control over the channel. The devices using high mobility channel materials such as germanium (Ge), SiGe, and III-V can outperform Si MOSFETs in terms of switching speed. Tunneling field-effect transistors use interband tunneling of carriers rather than thermal emission, and can potentially realize low power devices by achieving subthreshold swings below the thermal limit of 60 mV/dec at room temperature.

In this work, we examine two device options which can potentially provide high switching speed combined with reduced power, namely germanium nanowire (NW) field-effect transistors (FETs) and tunneling field-effect transistors (TFETs). The devices use germanium (Ge) – silicon-germanium (Si_xGe_{1-x}) core-shell nanowires (NWs) as channel material for the realization of the devices, synthesized using a 'bottom-up' growth process. The device design and material choice are motivated by enhanced electrostatic control in the cylindrical geometry, high hole mobility, and lower bandgap by comparison to Si. We employ low energy ion implantation of boron and phosphorous to realize highly doped contact regions, which in turn provide efficient carrier injection. Our Ge-Si_xGe_{1-x} core-shell NW FETs and NW TFETs were fabricated using a conventional CMOS process and their electrical properties were systematically characterized. In addition, TCAD (Technology computer-aided design) simulation is also employed for the analysis of the devices.

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CHAPTER 1

Research Background

1.1 MOTIVATION

The metal oxide semiconductor field-effect transistors (MOSFETs) have been the most important building blocks of CMOS (Complementary metal-oxide-semiconductor) circuits since their first introduction in 1960 [1, 2]. For the past 40 years, transistor scaling has been continued as predicted by “Moore’s law” [3]. It prospects the scaling of the gate length by a factor of 0.7 per every 2~3 years, doubling the number of transistors on integrated circuits [Figure 1-1, 1-2].

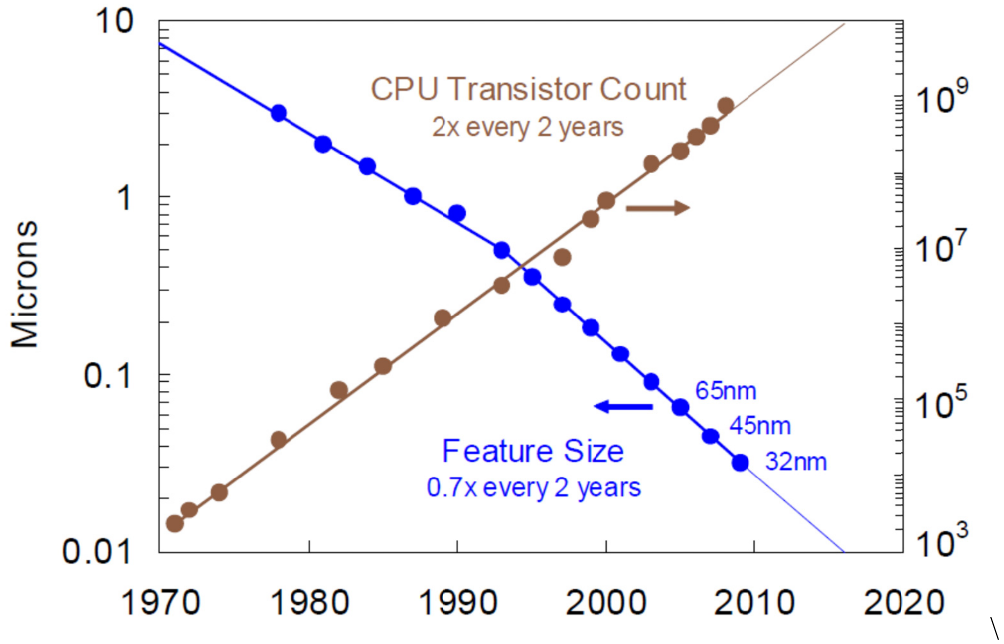


Figure 1-1: Historical scaling trend of CMOS following Moore’s law [4].

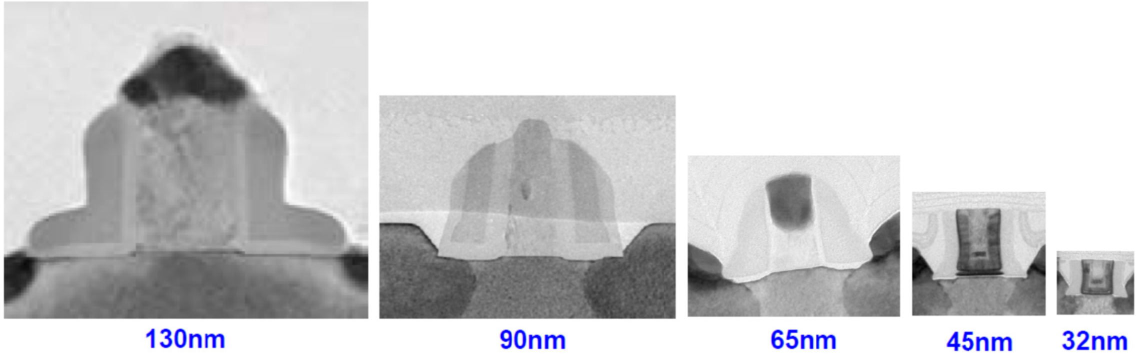


Figure 1-2: Scaling of MOSFETs below sub 100 nm regime [source: Intel].

The device scaling provides advantages, such as higher packing density, the higher circuit speed, and the lower power consumption. With these reasons, pursuing Moore's law has been a driving force for semiconductor industry to invest enormous efforts into scaling process technologies. Currently, the 32-nm process technology has already been employed in production [Figure 1-2]. However, continuing this scaling trend down to sub 10 nm regime appears to slow down and is challenged by technical and physical limitations [4-7]. To further extend device scaling limits, non-planar device structures [8-19], different channel materials other than Si [20-25], and devices working under different physics have been explored [26-29]. Recently, bottom-up grown semiconductor nanowires have been widely employed to examine such device options, motivated by the conveniences that they provide for the control of dimensions and compositions of NWs [30-38]. In particular, germanium (Ge)- Silicon Germanium (Si_xGe_{1-x}) core-shell NWs have gained increasing attentions as a channel materials to realize high performance transistors with low power consumption thanks to their unique physical properties [36-38].

In the remaining sections, the challenges with device scaling are first clarified and the possible future transistor options to overcome such challenges will be explored.

Finally, the potential advantages of Ge-Si_xGe_{1-x} core-shell NWs for the realization of high performance nanowire field-effect transistors (FETs) and tunneling field-effect transistors (TFETs) are discussed.

1.2 CHALLENGES IN DEVICE SCALING

The device scaling generates both economical benefits and device performance gains. However, as the transistors shrink aggressively, the device performances can be degraded by the so-called short-channel effects. The scaling theory, described by Dennard, provides scaling guidelines such that MOSFETs can be scaled without reliability and performance degradation [39]. For example, when the channel length (L_g) of a MOSFET scales by a factor α, it is necessary to scale down a gate oxide thickness (t_{ox}) and a depletion width (x_d) to keep the overall electric field unchanged in the device [Figure 1-3]. This scaling rule has worked well to scale the device down to near 100 nm regime. However, as the device dimensions approach sub-100nm regime, the device scaling faces several challenges, neccetiating new materials and process technologies [4-7].

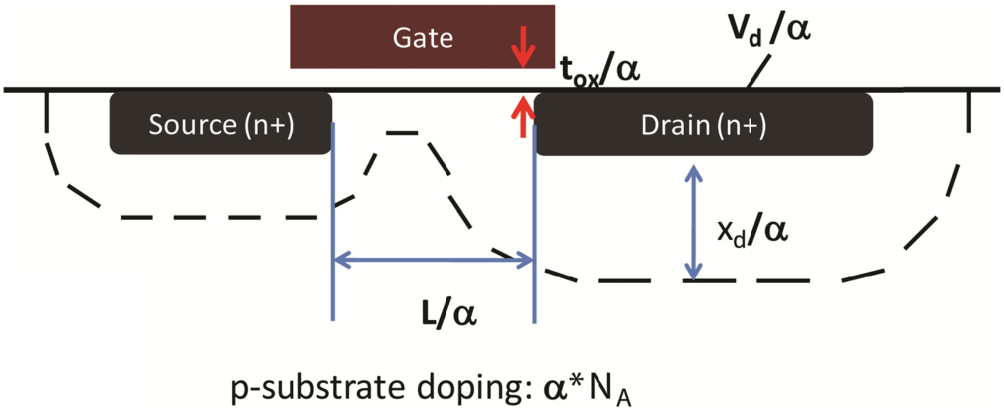


Figure 1-3: Schematic of MOSFET indicating device scaling parameters.

The most detrimental effect in device scaling is the increase of leakage current. The leakage current (I_{leak}) in transistors is composed of four major leakage components as illustrated in Figure 1-4:

$$I_{leak} = I_{sub} + I_{ox} + I_{GIDL} + I_{diode} \quad 1.1$$

,where I_{sub} is the subthreshold current, I_{ox} is the gate oxide tunneling currents, I_{GIDL} is the gate induced drain leakage current, and I_{diode} is the reverse bias diode leakage from the drain to the substrate. With the device scaling, the I_{sub} has exponentially increased due to the threshold voltage shift induced by drain induced barrier lowering (DIBL). The higher channel doping concentration (N_A), which is necessary to suppress short-channel effects causes the higher junction capacitance and diode leakage current (I_{diode}). As the gate oxide (SiO_2) thickness reaches few atomic layers, I_{ox} greatly increases to affect device performance. In addition, the increased electric field between the gate and the drain terminal affects the gate induced drain leakage current (I_{GIDL}). As a result, total leakage current (I_{leak}) continuously increase with the device scaling, leading to higher I_{OFF} current as shown in Figure 1-5(b).

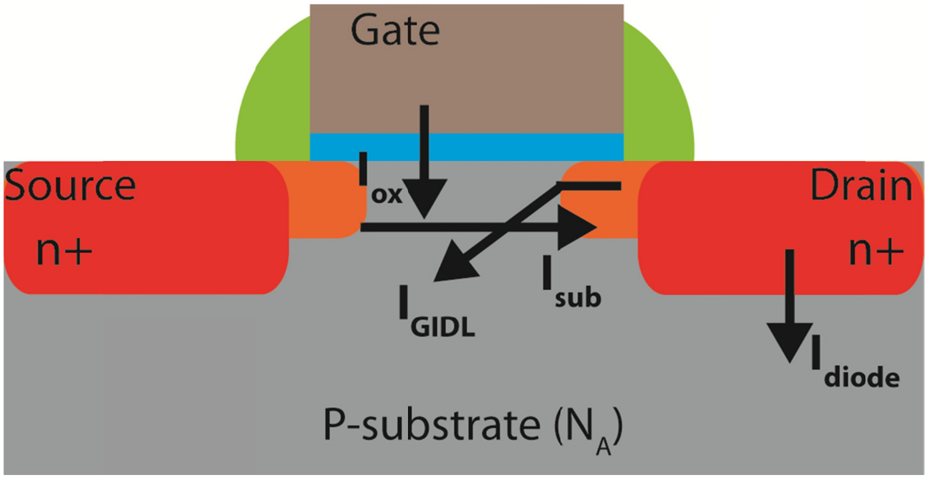


Figure 1-4: Schematic of MOSFET indicating leakage current sources.

Different from the ideal switch that turns ON and OFF instantly as shown in Figure 1-5(a), the switching in MOSFETs is fundamentally limited by the subthreshold swing (*SS*). The subthreshold swing is defined as the gate voltage needed to change the drain current by one order of magnitude, $SS = -[d(logI_d)/dV_g]^{-1}$; I_d is the drain current, and V_g is the gate voltage. Thus, to realize high-speed and low-power devices, a small *SS* value is desirable. Figure 1-5(c) shows the energy band profile of a conventional *n*-type MOSFET, illustrating carrier injection mechanisms affecting the *SS* values. In MOSFETs, the conduction occurs by injection of electrons from source into the channel. The carrier distribution in the source, given by the product $g(E)\cdot f_e(E)$, where g(E) is the density of state and $f_e(E)$ is the Fermi distribution of electrons in the source, allows high energy electrons to be injected into the channel when a potential barrier is present (OFF state), as shown in Figure 1-5(c). Indeed, the thermal broadening of the Fermi distribution limits the *SS* values to $kT/q\cdot\ln(10)$ = 60 mV/dec at room temperature [Figure 1-5(b)]. Due to this limit, the switching action close to the ideal switch can never be achieved in MOSFETs. With the scaling of device, the *SS* and I_{OFF} can be further increased due to short-channel effects [Figure 1-5(b) orange line].

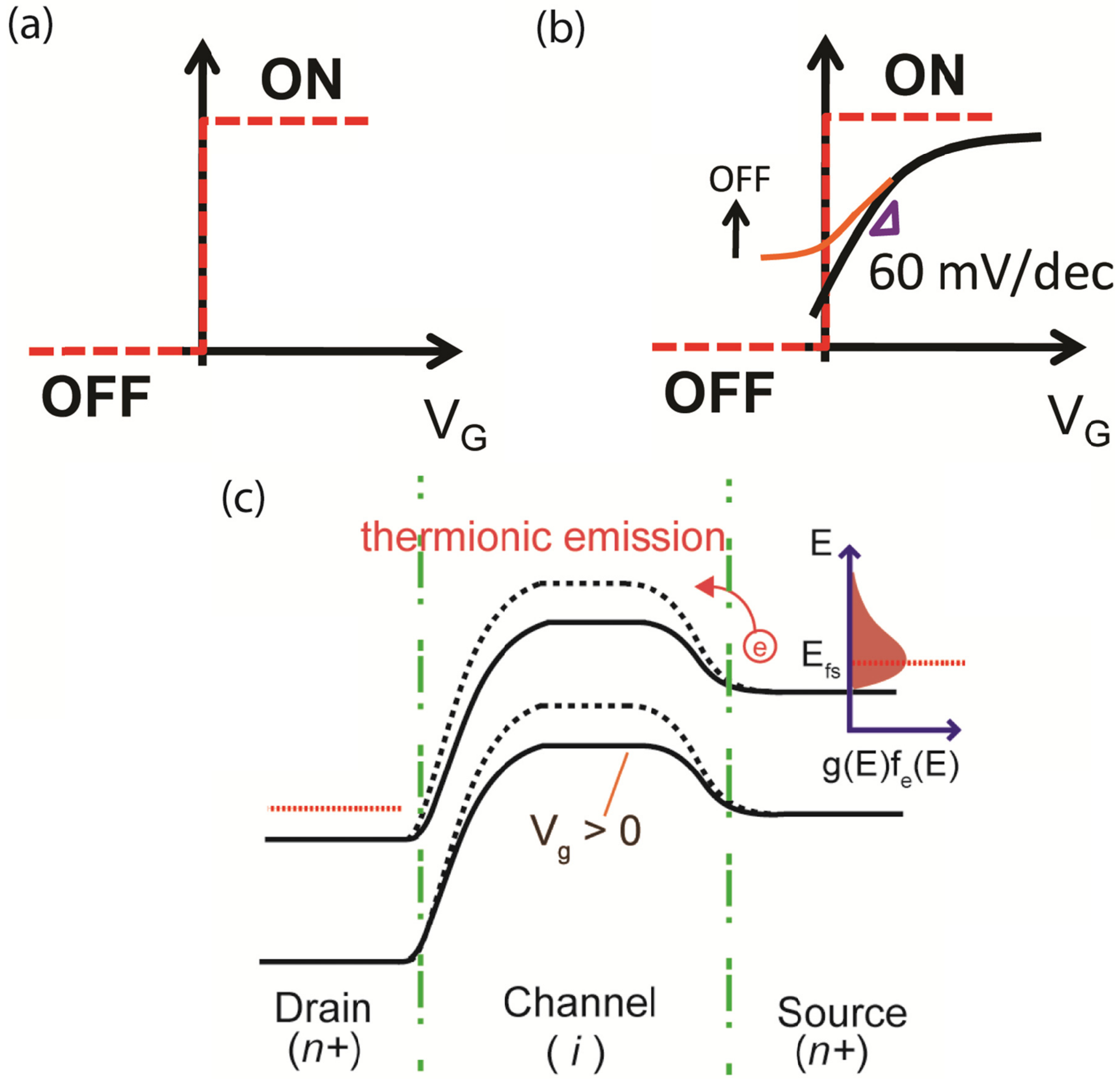


Figure 1-5: (a) The ideal switch instantly turns ON/OFF (b) The I_d-V_g characteristics of a MOSFET showing a subthreshold swing of 60 mV/dec at room temperature (black line). The I_{OFF} and *SS* can be further increased due to short-channel effects (orange line) (c) Energy band profile of a conventional n-type FET. The carrier injection depends on the thermionic emission of electrons over the potential barrier in the channel.

Therefore, considering the growing number of transistors on a chip and I_{OFF} increase due to short-channel effects, the power consumption management has now become the biggest challenge for continuing the device scaling. Figure 1-6 shows the active and passive power density calculated from the highest density logic regions for the reported CMOS devices [40]. Indeed, the data show that the leakage power is expected to surpass switching power at the channel length ~40 nm.

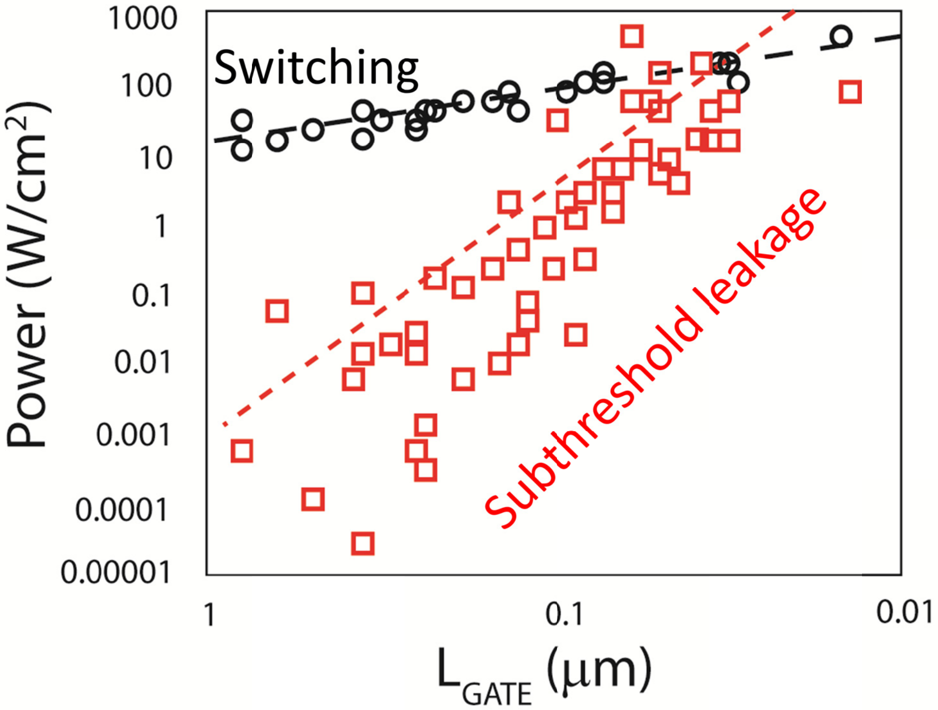


Figure 1-6: Power density vs. gate length. The data demonstrate that the subthreshold power consumption approaches to the active power consumption at short channel lengths. [40]

1.3 FUTURE TRANSISTOR OPTIONS

Previous section discussed the challenges for the continuing MOSFET scaling. In attempts to overcome such challenges, several new approaches have been explored recently.

1.3.1 Gate-all-around device structure

Non-planar device structures have been proposed to provide better electrostatic control over the channel. As the device dimensions shrink, the planar MOSFETs are suffering from increased short-channel effects. Thus, non-planar device structures, such as FinFETs (fin field-effect transistors), tri-gated FETs, Ω-gated FETs and GAA FETs (gate-all-around field-effect transistors) have attracted much attentions to provide enhanced gate controls over the channel and thereby reduce the short-channel effects [Figure 1-7] [8-19]. Among device geometries, theoretical studies suggest that the GAA structure implemented with the reduced channel thickness can provide the most efficient gate control.[41, 42] Experimental results have also demonstrated greatly improved short-channel device characteristics in GAA FETs, showing immunity to short-channel effects down to gate lengths of 30 nm [Figure 1-8] [17]. Thus, by employing GAA device geometry in MOSFETs, the device scaling can be extended without suffering from stand-by power dissipation due to short-channel effects while maintaining the performance of the devices.

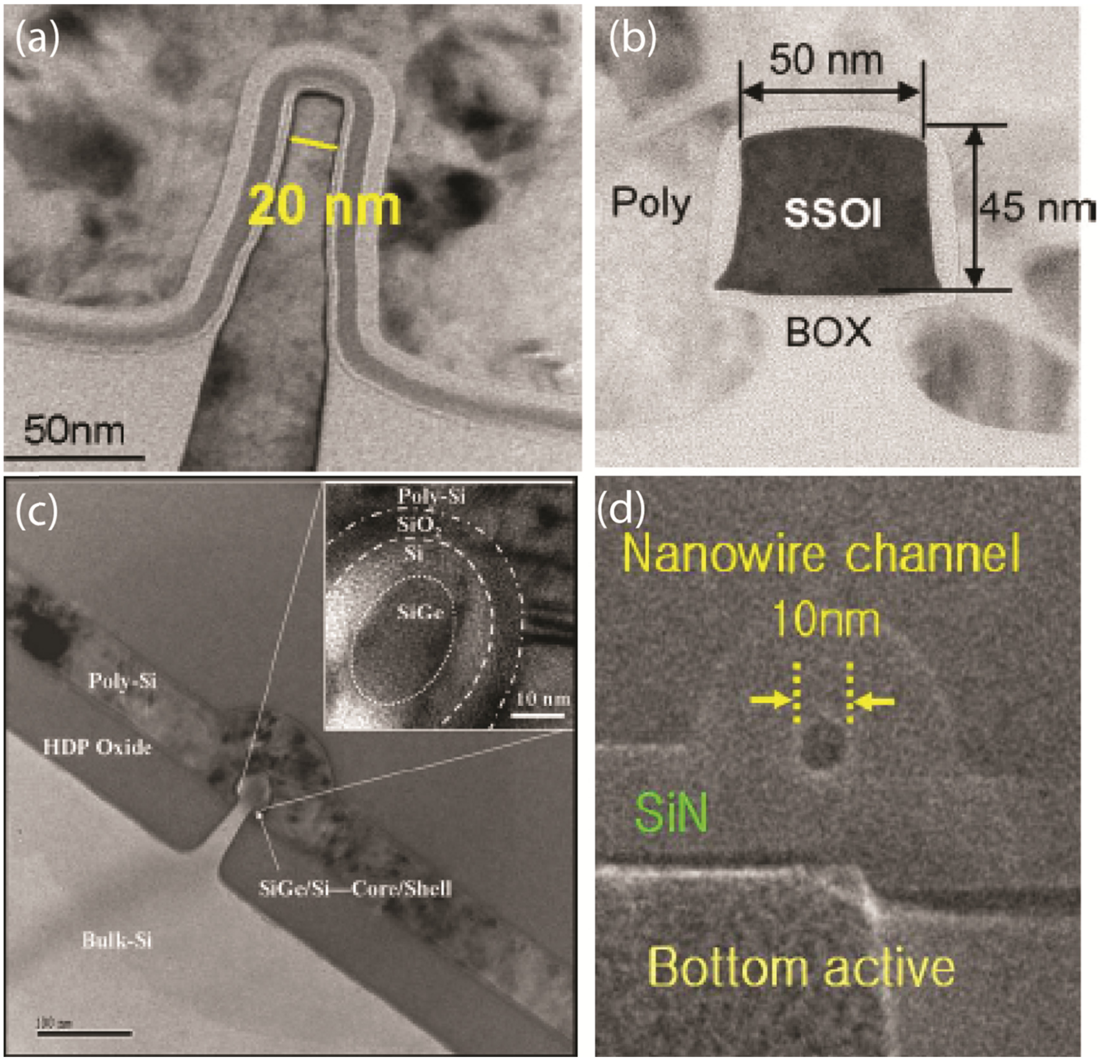


Figure 1-7: Device structures providing enhanced gate control over the channel (a) FinFET [9] (b) Tri-gate FET [16] (c) Ω-gated FET [11] (d) Gate-all-around (GAA) FET [17]

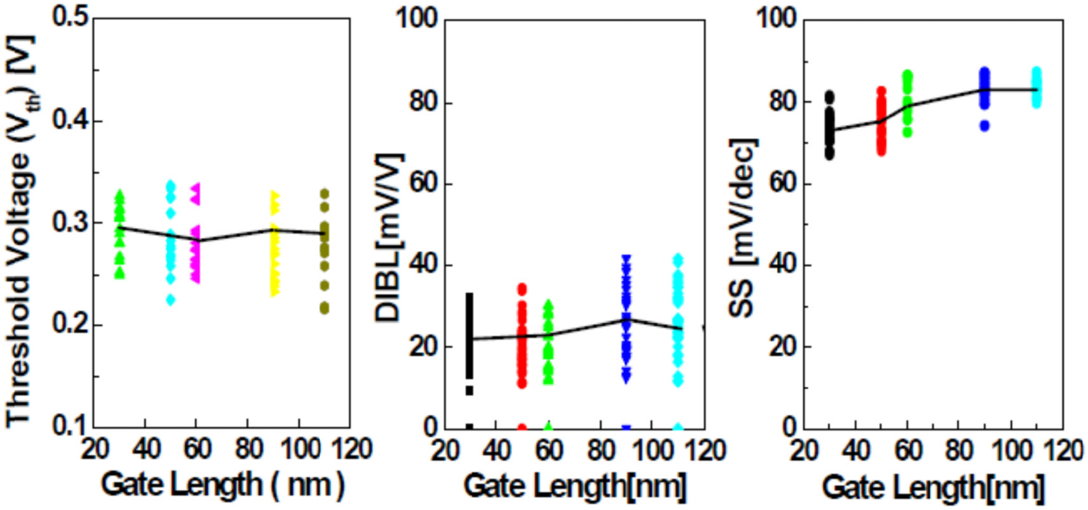


Figure 1-8. V_t roll-off, *SS*, and DIBL are not affected by the gate length scaling, demonstrating immunity to short-channel effect due to GAA device geometry realized along a NW [17].

1.3.2 High mobility channel material

On-current saturation in conventional Si MOSFETs with the device scaling necessitates high mobility channel materials to boost drive currents (I_{Dsat}) [43-47]. This saturation phenomenon in very short channel Si MOSFETs is believed to be limited by carrier injection from the source to the channel, where the injection velocity from the source (v_s) in short channel devices is set by thermal injection velocity (v_{inj}), experimentally demonstrated as ~40% of v_s [43-45]. In addition, the experimental results show that measured carrier velocity has a proportional relation with the low field effective mobility (μ) [46]. Thus, higher v_{inj} values can be achieved by employing high mobility channel materials.

The performance metrics, such as drive current and logic gate delay can be express in terms of v_{inj}, explaining the advantage of high mobility channel materials.

$$I_{Dsat} \approx Q_{inv} \times v_{inj} \quad 1.1$$

$$\tau = \frac{C_L V_{CC}}{I_{Dsat}} = \frac{L_g \times V_{CC}}{(V_{CC} - V_t) \times v_{inj}} \quad 1.2$$

where τ is the logic gate delay, Q_{inv} is the inversion charge density, C_L is the load capacitance, V_{CC} is the supply voltage, L_g is a MOSFET gate length, and V_t is the threshold voltage. By coupling equation 1.1 and 1.2, the advantages incorporating high mobility channel material for MOSFETs can be identified as the increase in the drive current and the reduction in the gate delay. Therefore, the high mobility channel materials, such as III-V compound semiconductors and germanium (Ge), have brought the attractions as channel materials for the deeply scaled MOSFETs, which can extend the device scaling trend without sacrificing the performance of the devices [20-23,47].

1.3.3 Tunneling field-effect transistors

As discussed in Chapter 1.2, the scaling of MOSFETs has been stymied by the increase in dissipated passive power, which stems from short-channel effects with shrinking device dimensions. Therefore, the need for novel devices, which can potentially provide a reduced dissipation power at switching speeds comparable to Si MOSFETs looms increasingly large. Tunneling field-effect transistors (TFETs) have gained significant attention as promising candidates to replace MOSFETs [48-56]. TFETs consist of gated *p-i-n* structures, e.g. a *p*-doped drain (source), an intrinsic channel, and an *n*-doped source (drain) [Figure 1-9(a)]. The carrier injection from the highly doped source into the channel relies on band-to-band tunneling (BTBT) at the reversed biased source-channel junction. TFETs have been theoretically shown to exhibit a steep turn-off, below the thermal limit of 60 mV/dec, and a sufficiently high ON-current comparable to that of Si MOSFETs, depending on the host semiconductor [48-50]. In particular, the semiconductors with low bandgap and tunneling effective mass are desirable to employ as a channel material for TFETs [51].

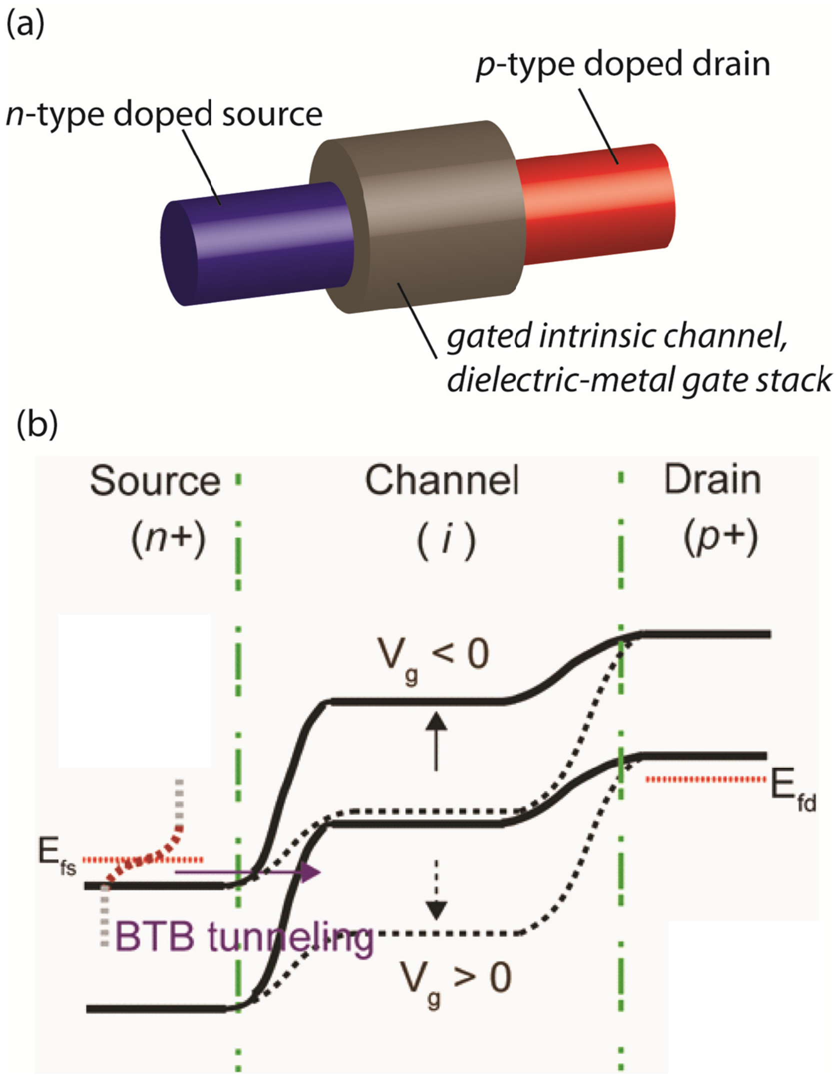


Figure 1-9. (a) Schematic representation of a TFET structure, having a n-doped source, a p-doped drain, and a gated *intrinsic* channel. (b) Energy band profile along a TFET. The carrier injection into the channel relies on BTBT, which enables the *SS* smaller than 60 mV/dec.

The carrier injection mechanism in a TFET differs from that of a FET. Figure 1-9(b) shows the energy band diagram along a TFET, consisting of a *p*-doped drain, an intrinsic channel, and an *n*-doped source, with the intrinsic segment being controlled by the gate bias. The switching of this device depends on the modulation of the energy band in the intrinsic segment. When the valence band in the channel is pulled above the conduction band at the source by applying a negative gate bias, the electric field at the source-channel junction becomes sufficiently high and holes are injected into the channel via BTBT. Similarly, when the valence band in the channel is pulled down with a positive gate voltage, the tunneling barrier width at source-channel junction becomes wide and tunneling is prevented, although tunneling at the drain-channel junction may be enabled. A key aspect of carrier injection in TFETs is that the high energy carriers in the source are prevented from tunneling at the source-channel junction [Figure 1-9(b)], effectively leading to a lower effective temperature of the carriers in the channel, and consequently an *SS* value below 60 mV/dec.

1.4 GE-SI_XGE_{1-X} CORE-SHELL NANOWIRES FOR FIELD-EFFECT AND TUNNELING FIELD-EFFECT TRANSISTORS

In the previous chapter, possible device options to mitigate performance degradation and power dissipation problems entailed with the device scaling were introduced. To examine such options, Ge-Si_xGe_{1-x} core-shell NWs are employed in this study, where Ge-Si_xGe_{1-x} core-shell NWs consist of a Ge core and a Si_xGe_{1-x} shell grown epitaxially on the Ge surface, described in more detail in Chapter 2.1.

The Ge-Si_xGe_{1-x} core-shell NWs provide a number of advantages to realize high performance NW FETs and TFETs. First of all, thanks to NW's cylindrical geometry, GAA device geometry can be easily implemented on a NW. The efficient energy band modulation of the channel using a gate bias is important for both NW FETs and TFETs. In FETs, it helps to minimize short-channel effects and OFF-state leakage currents, and thereby it enables further device scaling. In TFETs, since the switching of the device relies on the modulation of energy band profile in an *intrinsic* channel, a strong gate coupling to the channel realizes higher ON-state current as well as better *SS* characteristics. Secondly, Ge has the highest hole drift mobility due to its low hole effective mass, which is especially advantageous property for deeply scaled high performance *p*-type MOSFETs. [Figure 1-10] Thirdly, thanks to smaller bandgap of Ge (0.67 eV), higher BTBT currents by comparison to Si TFETs can be achieved in Ge-based TFETs. Lastly, by optimizing Si_xGe_{1-x} shell thicknesses and compositions of the NWs and thereby enhancing hole confinement effects and strain effects, the channel mobility can be further increased.

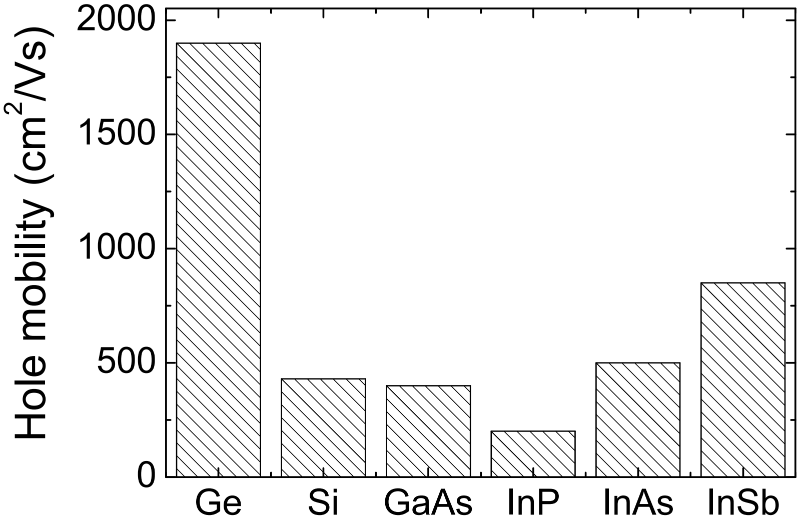


Figure 1-10: Hole mobility of the group IV semiconductors and group III-V compound semiconductors.

In addition to above mentioned physical advantages over Si, there are also several advantages in device fabrication aspects. Most of all, Ge is a CMOS compatible material. Thus, the fabrication technologies developed for Si can also be applied for Ge. Moreover, since Ge can be easily integrated on Si substrates [57, 58], a cylindrical channel similar to a NW can even be fabricated by "top-down" process [19]. Lastly, low thermal budget process can be easily employed for the dopant activation [59, 60], relieving thermal requirements for contemporary high-κ metal gate process [61].

Therefore, Ge-Si_xGe_{1-x} core-shell NWs are the promising channel material to realize both high performance NW FETs and NW TFETs.

1.5 CHAPTER ORGANIZATION

This chapter briefly presented the historical trend of the CMOS device scaling and entailing problems, such as performance degradation and stand-by power dissipation. To alleviate these problems and continue the scaling trend, the device structure providing an enhanced electrostatic control over the channel, high mobility channel materials, and TFETs were proposed as possible options to examine. In this research, Ge-Si_xGe_{1-x} core-shell NWs are employed for the realization of high performance NW FETs and TFETs thanks to their structural and physical advantages. Chapter 2 will present the growth of Ge-Si_xGe_{1-x} core-shell NWs and the electrical characteristics of the doped NWs realized by low energy ion implantation. In Chapter 3, the fabrication of high performance of Ge-Si_xGe_{1-x} core-shell NW FETs with highly doped source and drain will be presented, where the NW FETs are fabricated using a conventional CMOS process. The scaling properties of the devices will be presented and further investigated with TCAD simulation. Chapter 4 will present the fabrication and electrical characteristics of Ge-Si_xGe_{1-x} core-shell NW TFETs, consisting of a gated *p-i-n* structure. In addition, enhanced performance of NW TFETs by employing flash-assisted rapid thermal process will be presented. Chapter 5 will summarize the findings of this research and provide suggestions for future work.

CHAPTER 2

Growth and doping of germanium nanowires

The discussion in the Chapter 1 demonstrated the scaling trend of MOSFETs and explained the needs for new materials, device structures, and physics to continue the device scaling. As one of the candidates, Ge-Si_xGe_{1-x} core-shell NWs have gained interests because the gate-all-around (GAA) device geometry can be easily realized in NWs, where better electrostatic control over the channel than any other device geometry can be achieved. In addition, Ge's high hole mobility makes them a favorable platform to realize high performance field-effect transistors (FETs). Furthermore, Ge's lower bandgap by comparison to Si is an attractive property for the realization of tunneling field-effect transistors (TFETs). With these reasons as noted in the Chapter 1, Ge-Si_xGe_{1-x} core-shell NWs is considered as a promising material for the study of both FETs and TFETs. However, the biggest challenge to employ the NWs for both FETs and TFETs is an ability to reliably dope the NWs. For instance, high doping concentration up to 10^{20} cm^{-3} is necessary for the efficient carrier injection from the metal contact to a NW, which is a basic requirement for the high performance NW FETs. Also, doping a NW with different polarities of dopants is required to realize gated *p-i-n* TFETs. Therefore, two prerequisites for this study are to establish the growth process of high quality Ge-Si_xGe_{1-x} core-shell NWs and reliable NWs doping techniques

In this chapter, the growth process of Ge-Si_xGe_{1-x} core-shell NWs will be first introduced, followed by NW-doping using low energy ion implantation is then described. Specifically, the NW-doping with low energy boron- and phosphorus-implantation is investigated for different activation temperatures and ion doses.

2.1 GROWTH OF GE-SI_XGE_{1-X} CORE-SHELL NANOWIRES

Ge-Si_xGe_{1-x} core-shell NWs were grown on Si (111) substrate in a chemical vapor deposition (CVD) chamber via the vapor-liquid-soild (VLS) growth mechanism. The growth process of Ge-Si_xGe_{1-x} core-shell nanowires is outlined in Figure 2-1. Si (111) substrate is first cleaned with diluted hydrofludic (HF) acid (1:50 = HF:H_2O) to remove the native oxide layer on a wafer, followed by 1 nm of Au deposition using e-beam evaporator. Then, the substrate is transferred to load in CVD chamber. The wafer is annealed in the growth chamber at a substrate temperature of 350 ˚C in H_2 ambient, which forms droplet from the pre-deposited Au film. Then, the Ge core is first grown at a total pressure of 5 Torr and at the wafer temperature of 285 ˚C using 60 SCCM (cubic centimeter per minute at STP) GeH_4 (10 % diluted in He). The Si_xGe_{1-x} shell is grown in the same chamber in ultrahigh vacuum. This is done by rerouting the gas flow through a turbo pump, then coflowing 7 SCCM of SiH_4 with 60 SCCM of GeH_4 at a growth chamber temperature of 400 ˚C, which results in the epitaxial growth of Si_xGe_{1-x} shell on the Ge-core. The Si and Ge content can be tuned by changing the SiH_4 and GeH_4 partial pressure during the shell growth process, realizing the band engineered core-shell NW heterostructure. Figure 2-2(a) shows as-grown Ge-Si_xGe_{1-x} core-shell NWs on a Si (111) substrate. To verify the shell thickness and the content of Si_xGe_{1-x} shell, transmission electron microscopy and energy dispersive X-ray spectroscopy were used [Figure 2-2 (b), (c)]. The Si_xGe_{1-x} shell has a thickness of ~ 4 nm and an approximate Si content of x = 0.3. The role of the Si_xGe_{1-x} shell is two-fold. First, it acts as a passivation layer for the Ge surface, which is known to have a high density of interface traps in contact with a dielectric. Secondly, thanks to a positive band offset between Si_xGe_{1-x} and Ge valence band, it serves as a barrier and confines the holes in the Ge core. In particular, we chose a reduced Si content, x = 0.3, in order to minimize the strain in the Ge-Si_xGe_{1-x} core-shell heterostructure, while still maintaining the interface passivation.

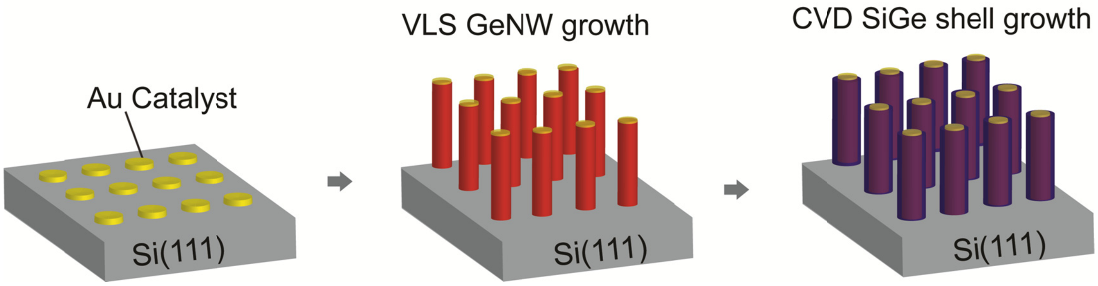


Figure 2-1: Schematics of the Ge-Si_xGe_{1-x} core-shell NW growth process. The Au droplets form during the H_2 anneal and serve as a catalyst for VLS Ge NW growth. After Ge NW growth, the Ge surface is passivated with Si_xGe_{1-x} shell.

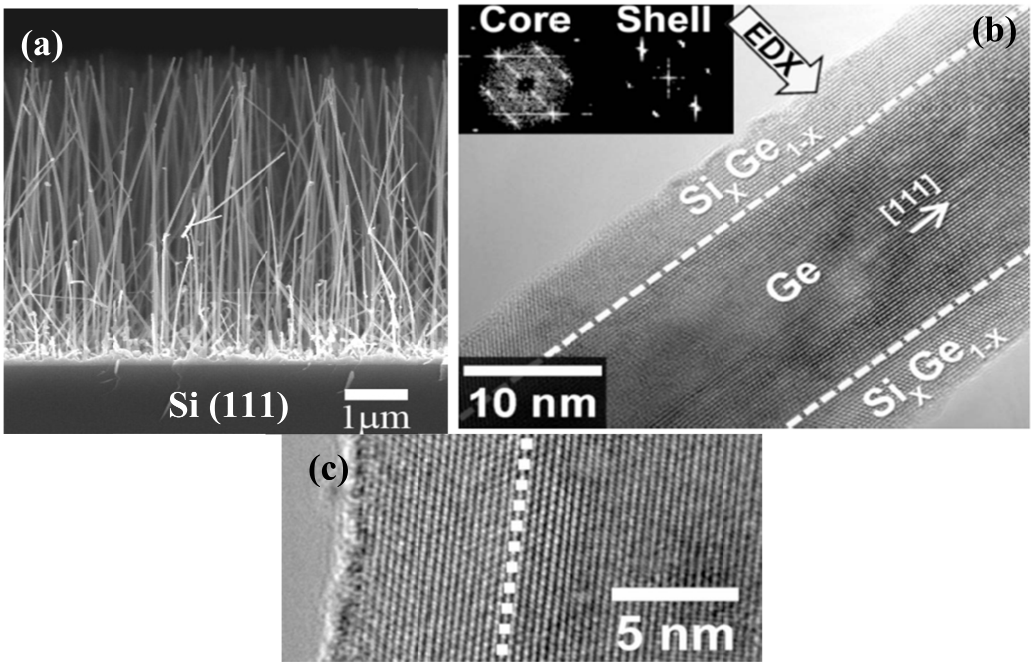


Figure 2-2: SEM and TEM of Ge-Si_xGe_{1-x} core-shell NWs (a) Cross sectional SEM showing an epitaxial NW growth on Si(111) substrate (b) TEM micrograph of a NW and Fourier transform of core and shell region (c) High resolution TEM of the same NW. The dashed lines in (b), (c) indicate the interface between the core and shell of a NW [62].

2.2 DOPING OF SEMICONDUCTOR NANOWIRES

2.2.1 Metal-Semiconductor contacts

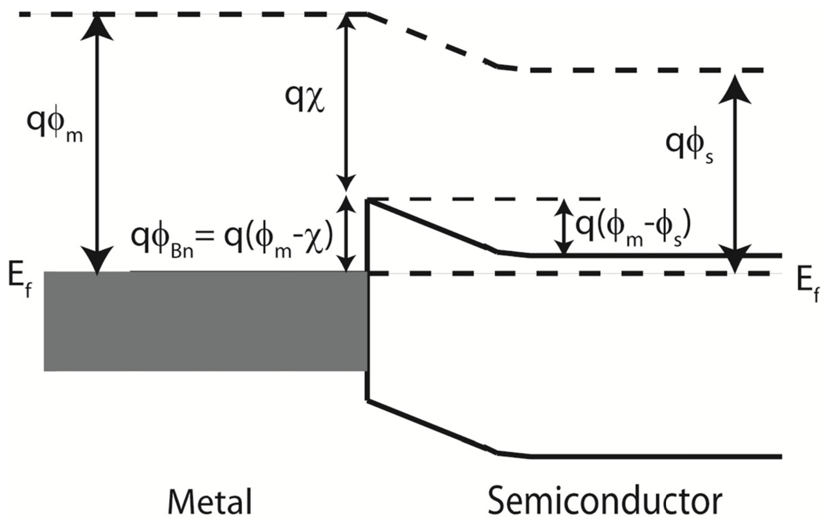


Figure 2-3: Energy band diagram of a metal-semiconductor contact in thermal equilibrium.

When the metal makes a contact with the semiconductor (*n*-type), the Fermi level (E_f) in the two materials must be the same and the vacuum level must be continuous. Thus, the energy band diagram for the ideal metal-semiconductor contact can be drawn as shown in the Figure 2-3. There exists the finite barrier height $q\phi_{Bn}$ from the metal to semiconductor conduction band, described by

$$q\phi_{Bn} = q\phi_m - q\chi \qquad 2.1$$

,where ϕ_m is the metal work function and χ is the semiconductor electron affinity. On the semiconductor side, the built-in potential (V_{bi}) exists from a semiconductor to a metal contact, simply determined by the work function difference between two materials.

$$V_{bi} = q(\phi_m - \phi_s) \qquad 2.2$$

Thus, to achieve ohmic contact between a metal and a semiconductor, it is ideal to choose the metal having a similar or smaller work function compared with that of semiconductor. However, the experimentally observed barrier heights for most semiconductors, such as Si, Ge, and III-V materials are relatively independent of metal work functions, which is attributed to Fermi level pinning, where the Fermi levels in semiconductors are pinned at a certain energy level in the bandgap and cause a depletion-type contacts [63-65]. Therefore, the barrier height engineering to obtain ohmic contacts becomes an impractical approach. Another approach to implement ohmic contacts is to make the barrier width sufficiently thin, so that electrons can easily tunnel through the barrier from the metal to semiconductor and vice versa. Figure 2-4 shows the schematics of the conduction mechanisms between a metal and semiconductor for different semiconductor doping concentrations.

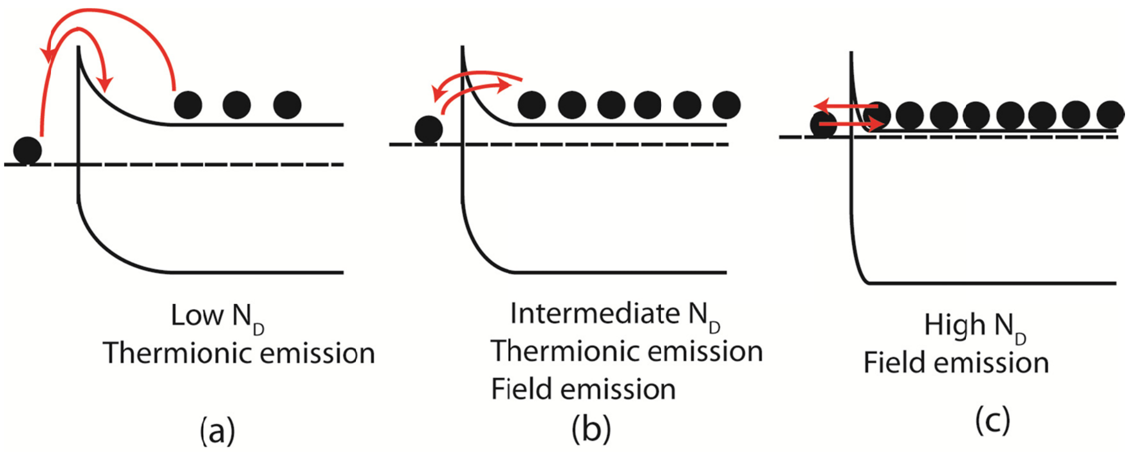


Figure 2-4: The conduction mechanism for a metal contact to *n*-type substrate. (a) Metal contact on a lightly doped substrate. Electron flows as a result of thermionic emission over the potential barrier (b) Metal contact on a substrate with an intermediate doping level. Thermionic-field emission dominates (c) Metal contact on a highly doped substrate. Electron tunneling dominated conduction [66].

For lightly doped semiconductor in Fig. 2-4(a), the current flows by thermionic emission of carriers, where the electrons thermally excited over the barrier. As a result, the potential barrier prevents efficient carrier transports between the two materials, which cause significant degradation in device performance. For a substrate with a medium level doping concentration, electrons are thermally excited to an energy level where the tunnel barrier is sufficiently thin for the tunneling. [Fig. 2-4(b)] For a highly doped substrate shown in Fig. 2-4(c), the electron tunneling between the metal and semiconductor can easily occur thanks to narrow tunnel barrier and thereby realizes low contact resistance. Therefore, the ability dope the semiconductor nanowires up to very high level (10^{20} cm^{-3}) in controllable manners is the most crucial challenge to employ the NWs for device applications.

2.2.2 Nanowire dopoing techniques

As discussed in the previous section, the doping of semiconductor is the essential requirement to enable efficient carrier injection from the metal to semiconductor. The NW-doping in this research is important in two aspects. First, doping the NWs up to very high level realizes the low contact resistance between the metal and a semiconductor nanowire as well as eliminate ambipolar behavior, and thereby high performance NW FETs can be realized. Secondly, for the realization of high performance NW TFETs, consisting of a gated *p-i-n* structure, the highly doped NW in the source region is also important to form a thinner tunnel junction between the source (*n*+ or *p*+) and the *intrinsic* channel junction, which increases BTBT currents. In addition, the ambipolar behavior can be controlled by the precise modulation of the drain doping concentration.

However, NW-doping is not trivial as bulk substrate doping due to NW's reduced dimensions.

To dope NWs, several doping methods have been investigated. In *situ* doping of Ge NWs, grown using the vapor-liquid-solid (VLS) mechanism, can be achieved by co-flowing dopant gases, e.g. B_2H_6 or PH_3, along with the growth precursors. While high doping levels can be realized using this approach, the dopant atoms are primarily incorporated either via conformal NW growth (B_2H_6) or through the NW surface (PH_3) rather than Au catalyst [67, 68]. This results in the entire NW being doped, with a doping concentration proportional to the exposure to the doping agent. Moreover, due to the nature of the *in situ* doping mechanism, axial doping modulation, or uniform doping concentrations are difficult to achieve.

Semiconductor doping using ion implantation, on the other hand, is a widely employed technique in semiconductor device manufacturing, as it allows for precise control of the doping level and depth, and uniform doping concentration. However, semiconductor NW doping using ion implantation is much more difficult with respect to planar, bulk devices, due to ion beam-induced damage and the resulting NW amorphization. While in the case of bulk substrates, high energy ion bombardment may cause an amorphization of the semiconductor crystal structure, the amorphized region can be recrystallized by a subsequent process with the bulk crystal structure underneath the amorphous layer serving as a template for crystal regrowth. The recrystallization of semiconductor NW after ion implantation may not always be possible however, if the entire NW body is amorphized during the ion implantation. For instance, Fig. 2-5(a) is the transmission electron micrograph (TEM) of a Ge-Si_xGe_{1-x} core-shell NW, phosphorus-implanted (ion energy: 6 keV, dose: 10^{15} cm^{-2}) at a normal incidence with respect to the NW surface.

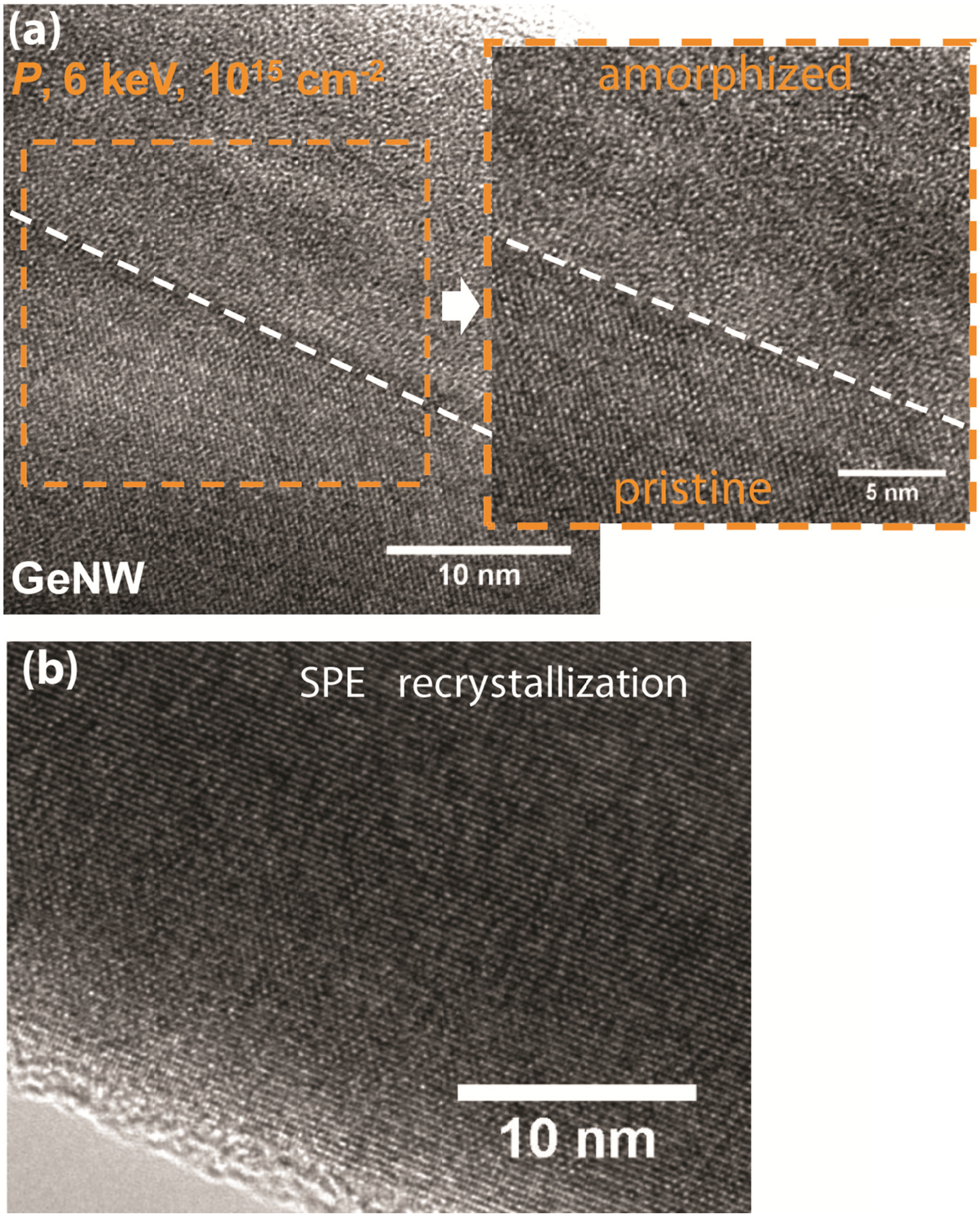


Figure 2-5: (a) Phosphorus-implantation damaged Ge-Si_xGe_{1-x} core-shell nanowire (energy: 6 keV, dose: 10^{15} cm^{-2}). The white-dashed line shows the boundary between the amorphized NW and the pristine NW (b) Solid-phase-epitaxy (SPE) recrystalized NW using thermal anneal.

It clearly shows that the boundary (white colored dashed line) between the amorphized region and the pristine region of the NW. In this case, the NW is not fully-amorphized and the amorphized section of the NW was recrystallized by thermal annealing at 600 ˚C for 3 min, using the pristine NW region as a template for NW recrystallization. [Figure 2-5(b)]

2.3 DOPING OF GE-SI$_X$GE$_{1-X}$ CORE-SHELL NWS USING LOW ENERGY ION IMPLANTATION

Among the available NW-doping techniques, ion implantation is the appropriate approach to achieve precise axial doping modulation along the NWs, which is an essential requirement to implement high performance NW-based FETs and TFETs. Although the ion implantation conditions for planar Ge substrates have been well established, using the ion implantation for Ge NW doping has never been investigated. In addition, it is not trivial due to NW's reduced dimensions as noted previously, necessitating more careful determination of NW doping conditions. Thus, it is important to carefully decide the parameters such as ion energy, ion dose, and activation conditions for the doping of Ge-Si$_x$Ge$_{1-x}$ core-shell NWs. In this chapter, the doping of Ge-Si$_x$Ge$_{1-x}$ core-shell NWs using either boron- or phosphorus-implantation is described in detail.

2.3.1 TRIM simulation

The two important parameters which characterize the ion range are the ion implantation energy and dose. The ion implantation energy determines the projection and straggle of implanted atoms, while the ion implantation dose determines the implanted dopant level in a target substrate. As discussed in the Chapter 2.2.2, due to the small diameters of NWs, these parameters should be more carefully decided by comparison to bulk substrates since the excessive implantation energy and dose can cause amorphization of the entire NW body.

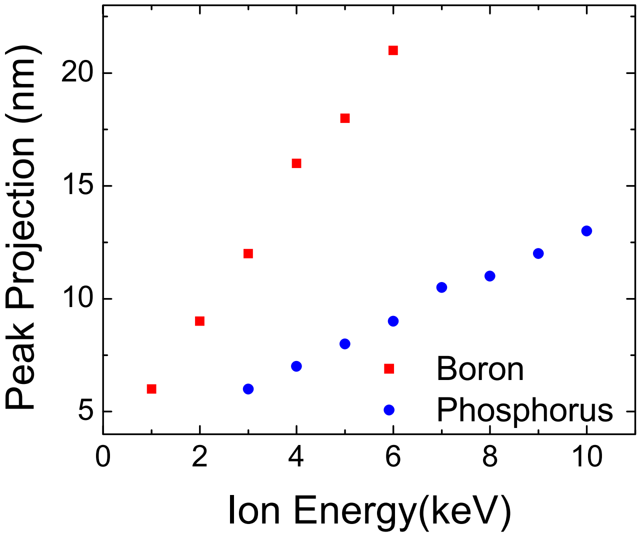
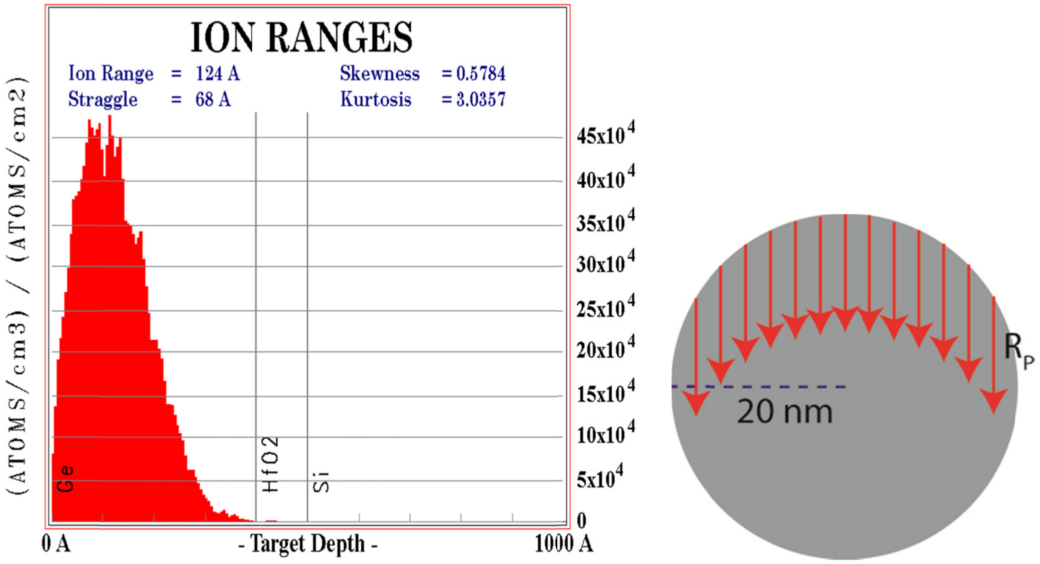


Figure 2-6: Peak projection range of boron and phosphorus in a Ge substrate as a function of ion energy (TRIM simulation).

To determine the implantation energy of the ions, the TRIM (the Transport of Ions in Matter) simulation was employed, which calculates the distribution of implanted ions in a solid and is known to provide very accurate as-implanted dopant profile in a 2D substrate [69]. In the simulations, ions were implanted at a normal incidence with respect to the Ge/HfO_2/Si substrate, where the Ge layer and the HfO_2/Si represents a Ge NW and a substrate served as a back-gate, respectively. The Ge layer thickness was chosen as 40 nm, which is the average diameter of NWs used in the study. By varying the implant energy for each dopant in TRIM simulation, the projection range (R_P) was extracted. Figure 2-6 shows the peak projection range of both boron (B) and phosphorus (P) atoms for different ion energies. The desired peak-projection range of dopants was around 10 ~ 15 nm in order to prevent the amorphization of the entire NW body and also preserve the pristine seed crystalline layer for solid-phase-epitaxial recrystallization using thermal annealing. Thus, in this study, ion energies for boron and phosphorus were determined as 3 keV and 6 keV, respectively.

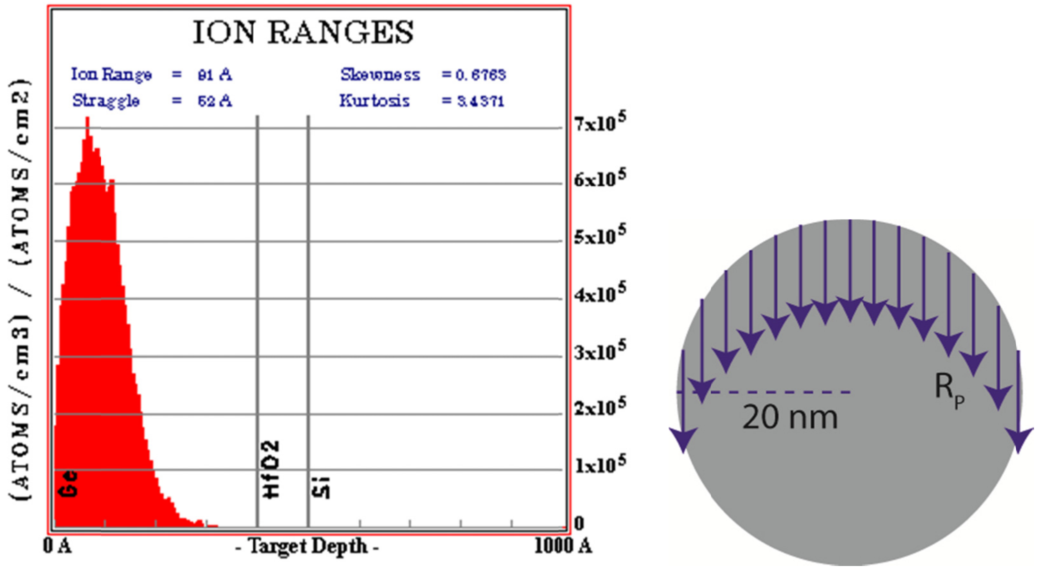


(a) (b)

Figure 2-7: (a) Boron distribution in a Ge layer. The boron atoms are implanted at the energy of 3 keV. Ge layer represents Ge NW on a HfO_2/Si substrate. The peak concentration of implanted B is located at ~12 nm. (b) Schematic representation of B peak distribution in a NW using the R_P in TRIM simulation.

Figure 2-7(a) shows the B distribution in a Ge layer (40 nm) and it shows that the peak B concentration at ~12 nm from the surface, where B is implanted at the energy of 3 keV at a normal incidence with respect to a Ge surface. Figure 2-7(b) shows the schematics of R_P distribution in the NW using the R_P extracted from Fig. 2-7(a). Similarly, the distribution of implanted phosphorus in Ge and the schematics of R_P

distribution in the NW are also shown in Figure 2-8. The projection range of phosphorus in Ge (40 nm) was targeted at ~10 nm, slightly shallower than the one used for B in Ge. This value was chosen in order to minimize the implant induced defects in NWs, which is expected since P is a heavier and bigger atom than B, and can cause more damages and defects in Ge.



(a) (b)

Figure 2-8: (a) Phosphorus distribution in a Ge layer. Phosphorus atoms are implanted at the energy of 6 keV. Ge layer represents Ge NW on a HfO_2/Si substrate. The peak concentration of implanted P is located at 9 nm. (b) Schematic representation of P peak distribution in a NW using the R_P in TRIM simulation.

Here, it should be noted that even if the projection range of dopants can be estimated using TRIM simulations, expected total number of dopants in a NW cannot easily be approximated since the simulation assumes a 2D substrate rather than one dimensional

NW, where the relatively large dopants loss is expected in a NW by comparison to a planar substrate.

2.3.2 Fabrication of back-gated Ge-Si_xGe_{1-x} core-shell NW FETs

To electrically probe the doping concentrations in Ge-Si_xGe_{1-x} core-shell NWs, back-gated NW FETs were fabricated. The fabrication process of a back-gated NW FET is described in Figure 2-9. Table 2-1 describes the details of fabrication processes. First, the Si (111) substrate having as-grown Ge NWs was cleaved into small pieces, and one piece was suspended in an ethanol solution and sonicated at low power for 10 s to prevent mechanical damage on NWs. Afterwards, the NW solution is spin onto a dielectric substrate, consisting of a 10nm-thick HfO_2 layer grown onto an *n*-type Si wafer, where it has predefined alignment markers to locate the NWs. [Figure 2-9 (b)] The samples were subsequently implanted with either boron or phosphorus. For B-doped NWs, the B-implant doses were varied from 10^{14} to 10^{15} cm^{-2}, at fixed ion implant energy, 3 keV. B-implanted NWs on a HfO_2/Si substrate were then activated using a conventional rapid thermal process (RTP) at 400 to 650 ˚C for 5 min in N_2 ambient. On the other hand, for P-doped NWs, P-implant doses were varied from 5×10^{14} to 2×10^{15} cm^{-2} at the energy of 6 keV, followed by RTP at 400 to 600 ˚C for 5 min in N_2 ambient. Next, the positions of NWs having a length longer than 4 μm, required for multi-terminal patterning, were determined using scanning electron microscopy (SEM). Then, multi-terminal contacts along the NW were defined by e-beam lithography (EBL). The channel length (*L*), the space between adjacent metal contacts was set at 500 nm for all the devices. Finally, the EBL patterned samples were dipped in diluted HF (1:50 = HF:H_2O) for 15s to remove native oxide on the NWs, a 100 nm of Ni was deposited using e-beam evaporator, and then lift-off was done in acetone which is boiled in water bath at 55 ˚C. The contact anneal at 150 ˚C for 1 min using RTP finalizes the device fabrication. Figure 2-9 (c) show the fabricated back-gated NW FETs with multi-terminal contacts along the NW.

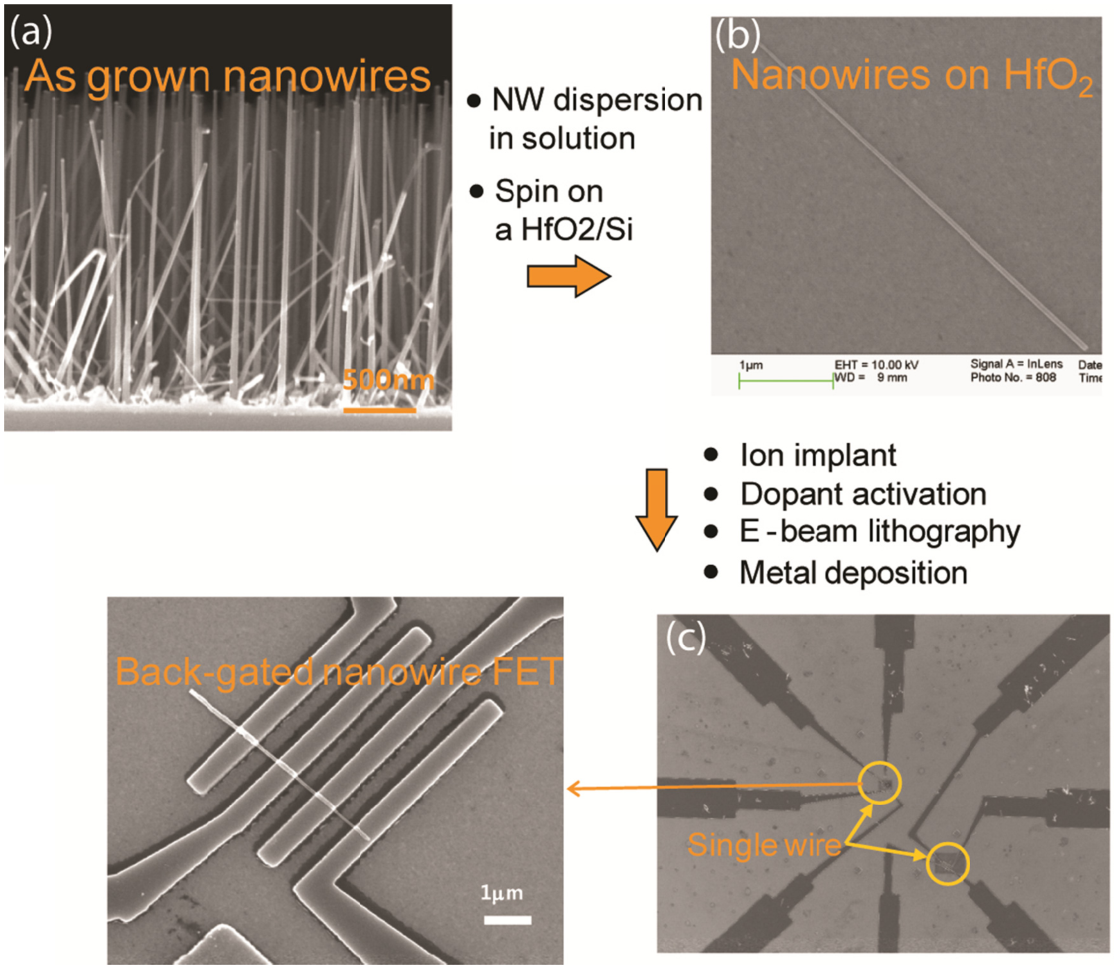


Figure 2-9: Fabrication process of back-gated NW FETs with multi-terminal contacts. (a) As-grown Ge-Si$_x$Ge$_{1-x}$ core-shell NW on a Si (111) substrate (b) Dispersion of NWs on a HfO$_2$/Si substrate (c) Back-gated NW FETs with multi terminal contacts.

Table 2-1: Device fabrication process flow of back-gated NWFETs

1. Immersion of a cleaved NW wafer piece in an ethanol solution
2. Low power sonication for 10 s to detach as-grown NWs from the Si substrate
3. Spin on a HfO_2(10nm)/ Si (n) substrate with pre-defined alignment markers at rpm, 1000~1500.
4. Boron implant (Energy: 3 keV, Doses: 10^{14}, 5×10^{14}, and 10^{15} cm^{-2}) Phosphorus implant (Energy: 6 keV, Dose: 5×10^{14},10^{15}, and 2×10^{15} cm^{-2})
5. Boron dopant activation (400 ~650 ˚C for 5 min in N_2 ambient) Phosphorus dopant activation (400 ~600 ˚C for 5 min in N_2 ambient)
6. E-beam lithography to define multi-terminal contacts along a NW
7. Diluted HF dip (1:50=HF:H_2O) for 15s, followed by Ni (100 nm) evaporation and lift-off.

2.3.3 Calculation of capacitance

The gate-to-channel capacitance values are necessary for the calculation of mobility and doping concentration in a NW. However, due to the reduced dimensions of the NWs, direct measurements of capacitances are difficult. Thus, we used the Sentaurus Technology computer-aided design (TCAD) simulation (Synopsis®) for the calculation of gate-to-channel capacitance. Figure 2-10 shows the device structure used for the capacitance calculation, consisting of a Ge core, a 4 nm thick $Si_{0.3}Ge_{0.7}$ shell, and a HfO_2 (10 nm)/ Si (n+) substrate. Here, Si substrate was served as a back-gate electrode. By applying a negative voltage, holes are first equally induced both in the Ge core and Si_xGe_{1-x} shell. As the applied back-gate voltage is further decreased, holes populating in

Si_xGe_{1-x} shell increase. Since it is biased using back-gate voltages, hole density is mainly distributed near the interface between a NW and a substrate as shown in Figure 2-10.

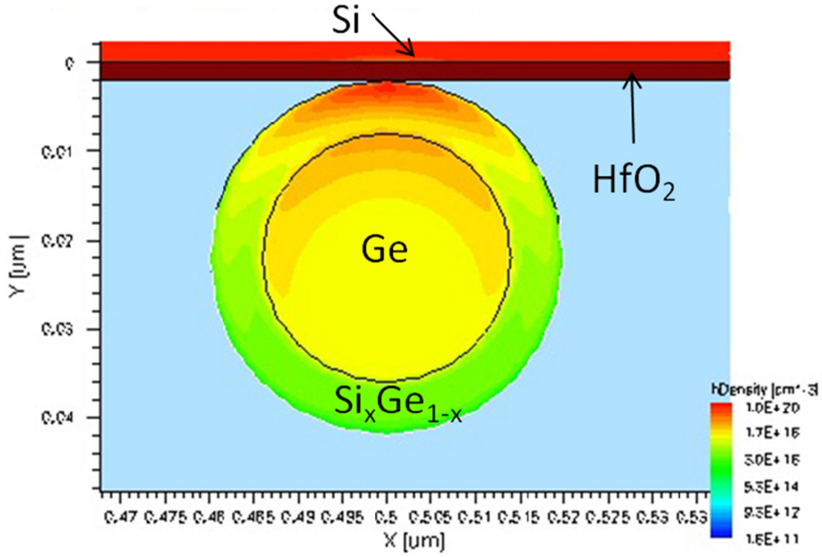


Figure 2-10: Schematic representation of a back-gated Ge-Si_xGe_{1-x} core-shell NW FET used in the simulation. Holes are mainly populated at the interface between a NW and substrate.

Figure 2-11 data show an example of hole densities in the core and shell calculated for a NW with a diameter of 40 nm. The band offset between Ge and Si_xGe_{1-x} layer was assumed as 0.2 eV. [ ] The total hole density per unit length (p) in a Ge-Si_xGe_{1-x} NW for a given gate voltage is calculated by summing the carrier density both in the shell and the core of a NW [Figure 2-11]. The carrier concentration in a NW is then obtained by $Q = e \cdot p = C_L \cdot |V_g - V_t|$, where e is the electron charge, C_L is a capacitance per unit length and V_t is a threshold voltage. Thus, total capacitance is extracted by the equation, $C_L = e \cdot (dp/dV_g)$. Figure 2-12 shows the C_L values for different diameters of NWs. The capacitances of NWs were calculated for different NW doping conditions, such as intrinsic NWs, highly doped NWs, and metallic NWs. Here, the capacitance values between a metallic NW and Si substrate were calculated using a finite element method

(Ansoft Q3D Extractor®) to crosscheck capacitance values of doped NWs extracted using Sentaurus TCAD simulation.

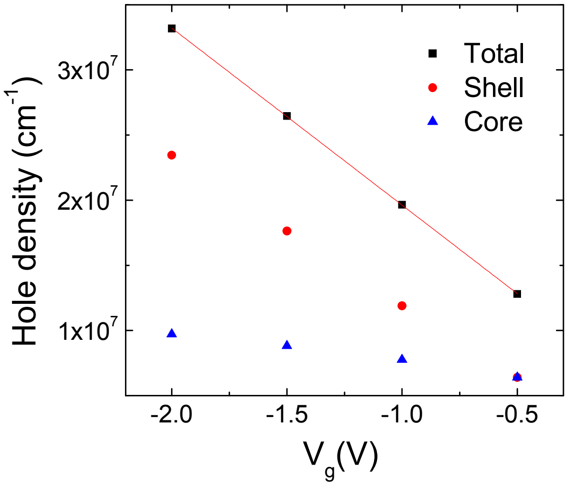


Figure 2-11: Total hole density *vs.* gate voltage. The total hole density is the sum of the hole density in the NW core and shell.

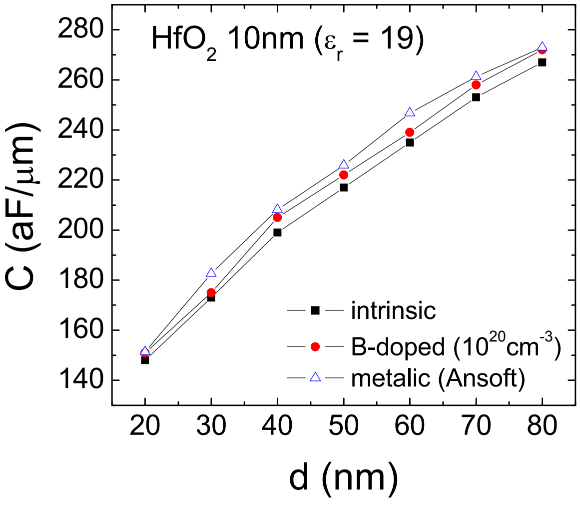


Figure 2-12: Capacitance *vs.* NW diameter (*d*) for each nanowire doping condition (intrinsic, highly doped and metallic NW condition). The capacitances were calculated using $C_L = e\cdot(dp/dVg)$. Blue triangles represent the capacitance values calculated using finite element method (Ansoft Q3D Extractor®) by assuming a metallic NW.

2.3.4 Electrical characterization of boron doped Ge-Si_xGe_{1-x} core-shell nanowires

Using Ge-Si_xGe_{1-x} core-shell NWs which is B-implanted at the energy of 3 keV with different doses (10^{14}, 5×10^{14}, and 10^{15} cm^{-2}) and activated at different temperatures from 400 to 650 ˚C, back-gated NW FETs were fabricated as shown in Chapter 2.3.2. Characteristics of NWs were then investigated by performing four-point (4-point), gate dependent resistivity measurements, with the substrate serving as back-gate. Specifically, we use four adjacent metal terminals, with the outer terminals used as current leads to inject and extract the current (I_d) in/out of the NW, while the inner terminals used to measure the voltage drop (ΔV_{4p}) along the NW (Figure 2-13). This method allows the measurement of the intrinsic NW resistivity without any contact resistance contribution. The channel length (L) is set by the 500nm metal contact spacing between the inner terminals, and the typical NW diameter (d) ranges from 30 nm to 60 nm with the average diameter of ~40 nm.

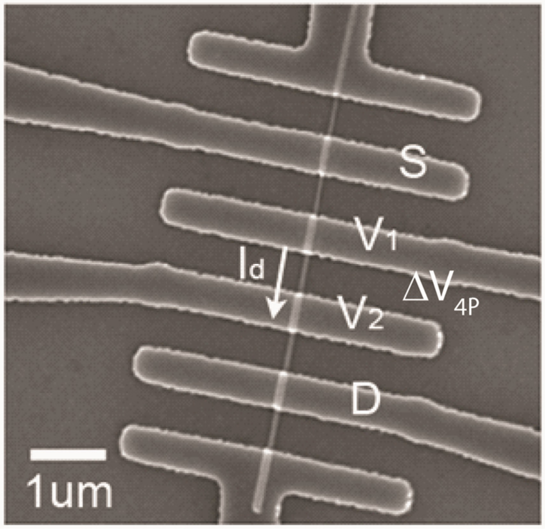


Figure 2-13: SEM of a NW device used for electrical characterization. The drain current (I_d) flows from source (S) to drain (D), and V_1 and V_2 are used to probe the voltage drop (ΔV_{4p}) along the NW.

Figure 2-14(a) data shows one example of 4-point current-voltage characteristic measured on B-implanted NWs, for three different implant doses, and at a back gate bias V_{bg}=0 V. All devices underwent a 5 min 600 °C RTP post-implantation to activate the B dopants. These data show a linear current voltage relation, corresponding to a high NW conductance, roughly proportional to the implant dose. The data indicate the NWs are doped, and that the ion beam-induced damage does not amorphize the NWs for the implant doses used here. In Figure 2-14(b), we show the I_d vs ΔV_{4p} at different V_{bg} values, varied from -1.0 to 1.0 V with a step size of 0.5 V. The conductance dependence on V_{bg} is used to extract the carrier mobility and doping concentration in the devices.

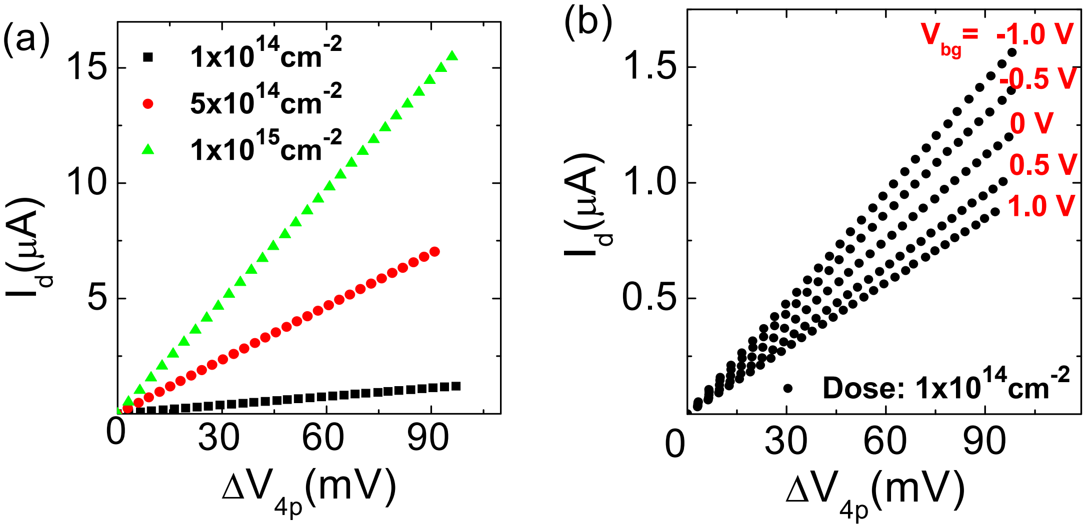


Figure 2-14: (a) I_d vs ΔV_{4p} data measured for NWs implanted with different B doses. The data show a conductance increase with the implant dose. (b) I_d vs ΔV_{4p} measured at different V_{bg} values for a B-implanted NW with a dose of 10^{14} cm^{-2}[70] [Sample:Ge52AB001~B003]

One key parameter in this study is the doping concentration, and its dependence on the implant dose. In order to extract the doping concentrations of our B-implanted Ge-Si_xGe_{1-x} core-shell NWs, the following model was employed. The NW conductance G is related to the doping concentration per unit length (p_L), and carrier mobility (μ) by the relation $G = p_L \cdot e \cdot \mu \cdot L^{-1}$; e is the electron charge. The carrier concentration per unit length depends, in turn, on the gate bias V_{bg}, via $p_L = p_{L,0} + (V_{bg} \cdot C_L \cdot e^{-1})$, where C_L is the back-gate to NW capacitance per unit length, $p_{L,0}$ is the carrier concentration at V_{bg}=0. Therefore, the device transconductance (dG/dV_{bg}) is related to the carrier mobility via $dG/dV_{bg} = \mu \cdot C_L \cdot L^{-1}$. From the measured gate-dependent 4-point conductance value, as shown in Figure 2-14(b), the transconductance is first calculated and then extract the carrier mobility using $\mu = L \cdot C_L^{-1} \cdot (dG/dV_{bg})$. The gate-to-channel capacitance values (C_L) calculated in the previous section has been applied to calculate the carrier mobility. The measured mobility typically ranges from 40 to 100 $cm^2/V{\cdot}s$ in these devices.

Once the carrier mobility is calculated for each device, the active *p*-dopant concentration (p) per unit volume of our Ge-Si_xGe_{1-x} core-shell NWs is determined using $\sigma = p \cdot e \cdot \mu$, where the conductivity σ is related to the measured conductance via $\sigma = G \cdot L \cdot S^{-1}$; S is the cross-sectional area of NW measured from scanning electron microscope (SEM) data. To investigate the p dependence on activation temperature (T), the B-implanted NWs were annealed at T=400, 500, 600, and 650 °C for 5min, in an N_2 ambient. The p vs T data extracted from over eighty devices implanted at different doses is summarized in Figure 2-15(a). These data do not indicate a discernable trend of the average doping concentration with increasing T, although the maximum doping concentration does increase slightly with T.

In order to estimate the fraction of implanted B atoms that become active, in Figure 2-15(b) the active dopant concentration per unit area p_{2D} for each device is plotted as a function of the areal implant dose. Assuming the NW is cylindrical, the areal and volume dopant concentrations are related by $p_{2D} = p \cdot (\pi d / 4)$. Figure 2-15(b) data show that the fraction of active implanted B atoms is typically around 15-25%, with a maximum of 80% for some devices. Due to their small footprint, NW to NW variations of implanted B atoms can be expected in our Ge- Si_xGe_{1-x} NWs, which in turn can cause the relatively wide distribution of p_{2D} shown in Figure 2-15(b).

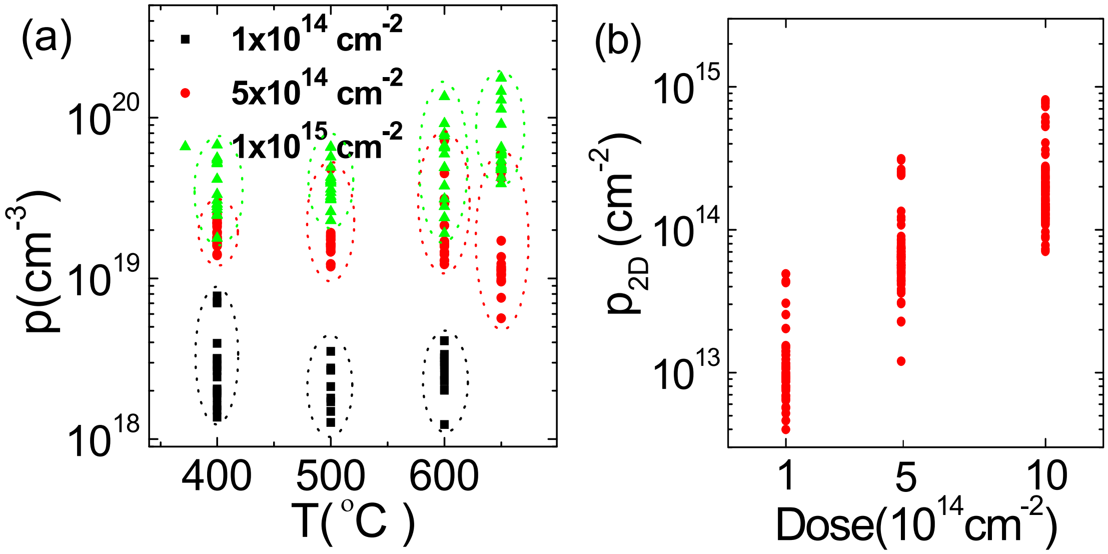


Figure 2-15: (a) Activated dopant concentration (p) vs the activation temperature (T) for different implant doses. (b) Activated dopant dose per unit area (p_{2D}) vs the implant dose. These data show that roughly 15%-25% of the implanted ions are active dopants in the NWs [70]. [Sample: Ge52A_B001~B011]

A few conclusions are apparent from the Figure 2-15 data. First, the doping concentration is rather insensitive to the annealing temperature. This observation is consistent with previous reports for B-implanted Ge substrates and can be explained by a relatively fast defect removal or regrowth velocity above 400 °C in bulk Ge [59, 60]. Second, the doping concentration of Figure 2-15 are comparable or larger that the reported solid solubility, ~5 × 10^{18} cm^{-3}, of B in bulk Ge [71].

In Figure 2-16, the doping concentration is plotted as a function of mobility for the different implant doses and activation temperatures. Although implant doses above 5 × 10^{14} cm^{-2} follows general doping density *vs* mobility relation, the distribution from implant dose at 10^{14} cm^{-2} are discontinued from the two higher implant doses. They are distributed at lower mobility region than expected. The reason for this deviation is still unclear, but we speculate that the reduced mobility values at a dose of 10^{14} cm^{-2} may be related to existing interface traps, and a certain level of implant dose might be required to suppress the impact of pre-existing interface traps.

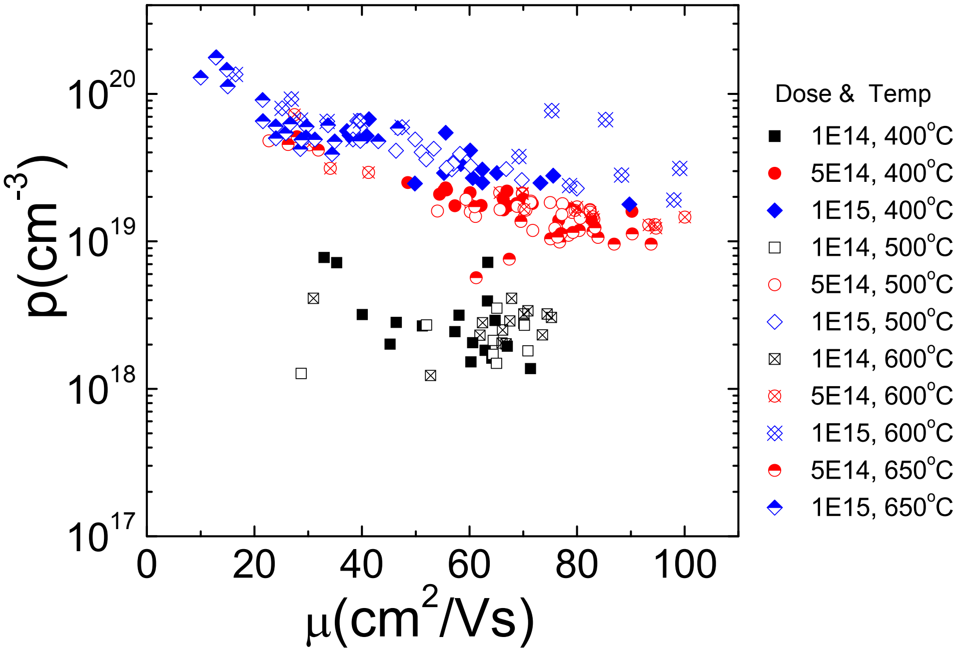


Figure 2-16: Doping concentration (*p*) vs mobility (*μ*) for different implant doses and activation temperatures. These data show that implant doses above 5 × 10^{14} cm^{-2} follow the general relation between doping density *vs* mobility.

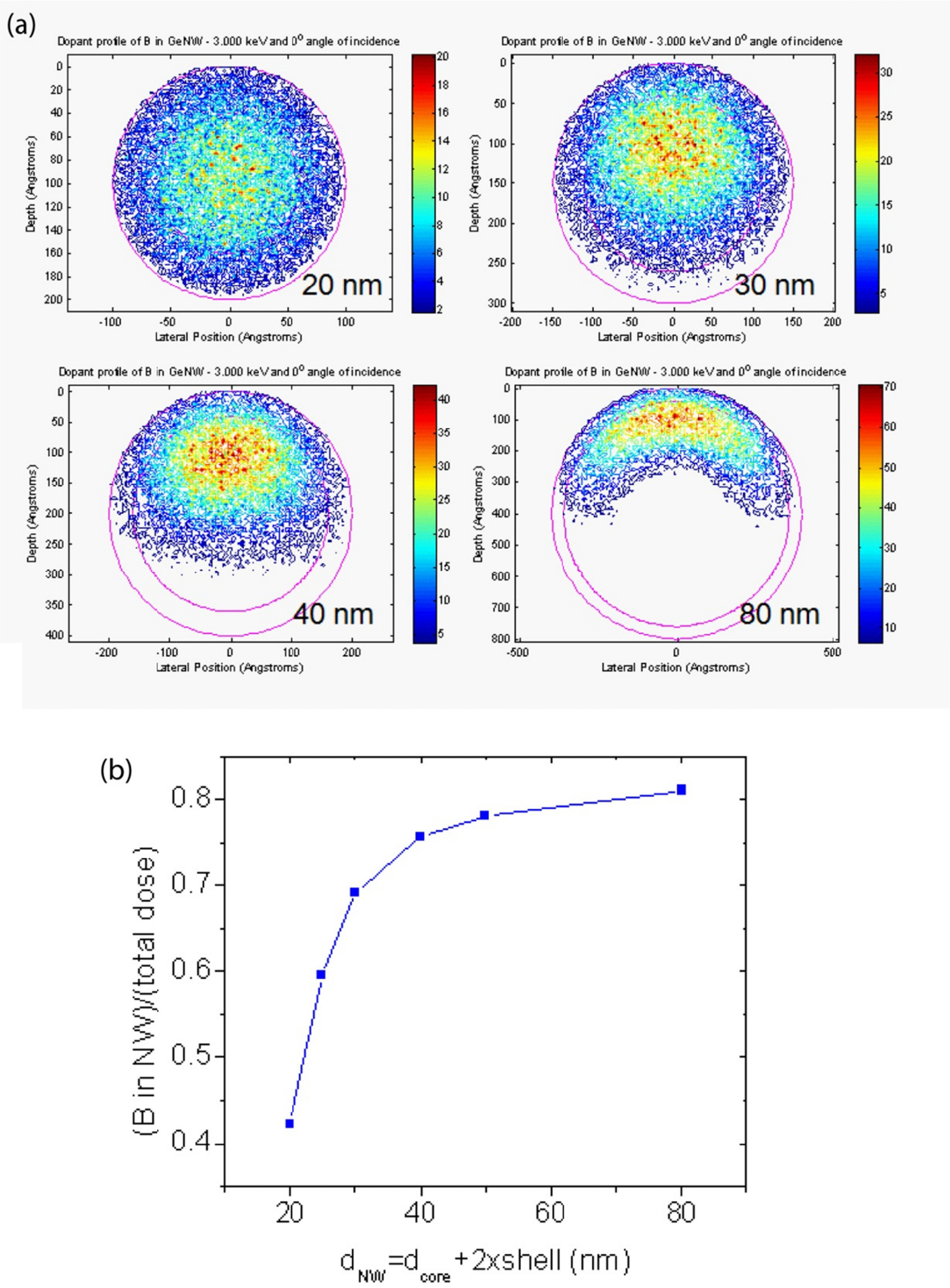


Figure 2-17: (a) Implanted boron distributions in Ge-Si_xGe_{1-x} core-shell NWs with different diameters (ion energy: 3keV) (b) Dopant loss as a function of the NW's diameter. Dopant loss is higher for NWs with smaller diameter.

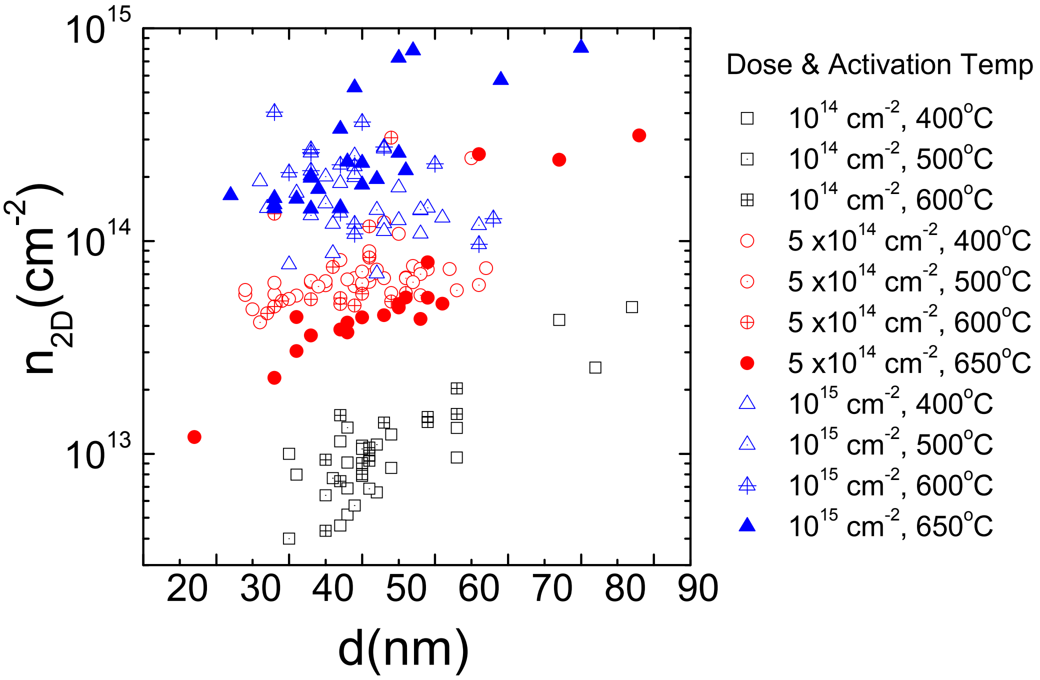


Figure 2-18: Activated dopant dose per unit area *vs* nanowire diameter (*d*) for each ion implant dose, demonstrating higher dopant loss due to lateral straggle for the NWs with smaller diameters.

The data in Figure 2-15 clearly show the wide *p*-distribution, which can be in part related to diameter dependent dopant loss due to lateral dopant straggle in NWs. To corroborate this possibility, 2D SRIM simulation was employed [72]. In the simulation, the NW, having the same $Si_{0.3}Ge_{0.7}$ *shell* thickness (4 nm) with different Ge core diameters, were B-implanted at the same energy of 3 keV. Figure 2-17(a) shows the *implanted*-B distributions in NWs, demonstrating the relative dopant levels in NWs and peak projection ranges for each diameter. The results in Figure 2-17(b) clearly show higher dopant loss in the smaller NW diameters. The dopant loss due to lateral dopant straggle becomes more severe for NWs with smaller diameter since dopants can be more easily escaped from the NW surface during the implantation process. Figure 2-18 shows the experimentally observed the activated dopant dose per unit area as a function of NW's diameter for each activation temperature and implant dose. Clearly, higher dopant loss is observed in NWs with small diameters, which is consistent with the general trend shown in Figure 2-17.

2.3.5 Electrical characterization of phosphorus doped Ge-Si_xGe_{1-x} core-shell nanowires

Electrical characteristics of phosphorus-doped NWs were measured using the same method explained in Chapter 2.3.4. After dispersing Ge-Si_xGe_{1-x} core-shell NWs on a SiO_2 (30 nm)/Si (*n*+) substrate, the NWs were implanted with phosphorus at the energy of 6 keV with a dose of 5×10^{14}, 10^{15}, and 2×10^{15} cm^{-2}, respectively. NWs were then RTP-annealed at different temperatures, 400 ~600 ˚C for 5 min. It was observed that

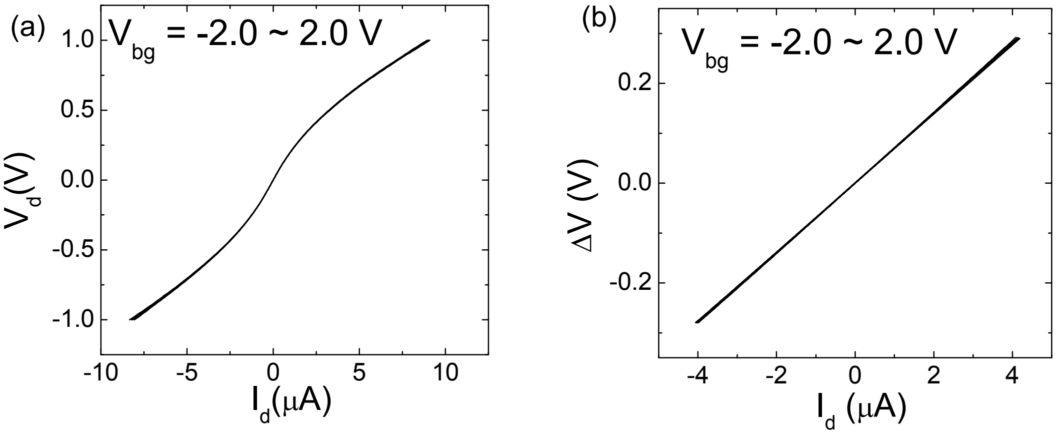


Figure 2-19: Representative current vs voltage characteristics of phosphorus doped NWs (P dose: 10^{15} cm^{-2}, RTP: 400 ˚C for 5 min) (a) I_d-V_d characteristics of a back-gated NW FET measured using a 2-point configuration for different gate voltages, V_{bg} = -2.0 ~ 2.0 V. Non-linear characteristics were observed at low drain bias condition. (b) I_d-V_d characteristics of a back-gated NW FET measured in a 4-point configuration for different gate voltages, V_{bg} = -2.0 ~ 2.0 V. Gate dependence was very weak for all devices, consistent with high doping level.

the dielectric (SiO_2) thickness should be thicker than 20 nm to prevent severe oxide leakage current due to ion implant damage.

Figure 2-19 shows the two-point and four-point current *vs* voltage characteristics of P-doped NWs (Implantation dose:10^{15} cm^{-2}, Activation: 400 ˚C for 5 min in N_2 ambient), where V_{bg} is biased from -2.0 to 2.0 V with a step of 1.0 V. Two observations are clear from the data in Figure 2-19. First, the two-point current-voltage characteristics shows a non-linear region at low drain bias, which indicates the presence of a barrier for electron injection [Figure 2-19(a)] Secondly, the conductance does not change with the gate bias, which may indicate that the NWs are highly doped. Thus, in this study we can only extract the NW-resistivities and the metal-to-NW contact resistances, using 2-point and 4-point current-voltage characteristics, but cannot investigate of the NW-doping concentration.

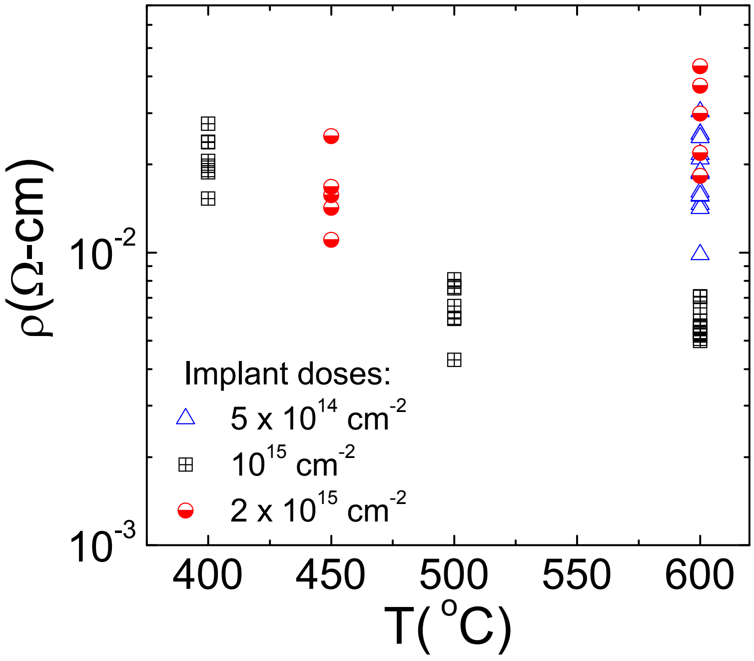


Figure 2-20: Resistivities (ρ) vs the activation temperature (T) for different P-implant doses. [Index: Ge48P002,P004,P009,P010,P011]

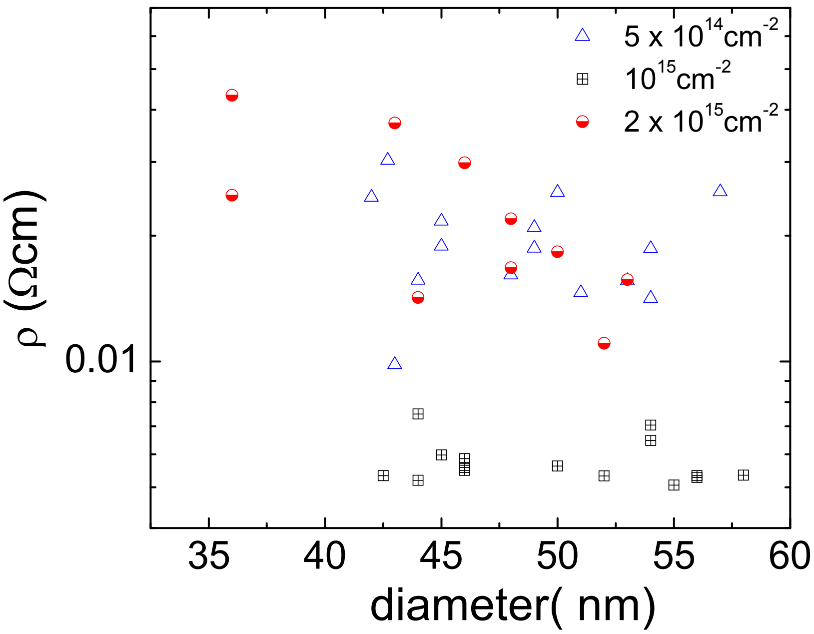


Figure 2-21: Resistivities (*ρ*) vs NW's diameters for different P-implant doses, activated at 600˚C.

Figure 2-20 summarizes the resistivities of P-doped NWs for different dopant activation temperatures and implant doses. Unlike the B-implanted NWs shown in Figure 2-15, the data in Figure 2-20 clearly show the high activation temperature results in lower resistivities. The resistivity values at a P-dose of 10^{15} cm^{-2} decrease as the activation temperature increases, and the lowest ρ value is observed at 600 ˚C. However, for an implant dose of 2×10^{15} cm^{-2}, the resistivities are increased slightly as the activation temperature increases from 450 to 600 ˚C. We suspect that the high P-dose, 2×10^{15} cm^{-2}, may have caused more defects and segregation of non-active dopants in NWs, which in turn increase the resisitivities of NWs. Thus, while the total number of implanted dopants in a NW may be increased at higher doses, the electrically active dopants level may not be increased accordingly. Interestingly, at an activation temperature of 600 ˚C activation lower nanowire resistivities were obtained from NWs implanted at a dose of 5×10^{14} cm^{-2} *vs.* 2×10^{15} cm^{-2}, suggesting that the optimum P-implant dose level is located between the two doses. Lastly, the resitivities of P-doped NW activated at 600˚C were plotted as a function of NW's diameters for different P-implant doses [Figure 2-21]. In general, the resistivities values do not show the diameter dependence.

2.3.6 Ni-nanowire contact resistances in doped Ge-Si_xGe_{1-x} core-shell NWs

Two important parameters evaluating the interface contacts between a semiconductor and a metal are contact resistance (R_c) and specific contact resistance (ρ_c). The contact resistance is given by ρ_c/A, where A is the area of active contact. Since the current does not always uniformly flow in a contact area, a transmission line model (TLM) is typically employed to model the current flow and to determine active contact area (A). Using the TLM, the relation between contact resistance and specific contact resistance in a NW can be derived [73].

Figure 2-22 (a) shows the TLM describing electron transport at the metal-semiconductor NW interface; W is the metal contact width, r is the radius of the NW, ρ_c is the specific contact resistance at the metal/NW interface, $I(x)$ is the current through a NW, v_0 is the voltage drop between a metal contact and semiconductor NW ($x = W$), and $V(x)$ is the voltage drop between x and $x = W$ in a NW. The differential resistance at a NW/Ni interface along a length dx is given by $\rho_c/(\pi r dx)$, assuming that Ni contact covers only the upper section of a NW since the bottom half section is screened from the metal deposition. [Figure 2-22 (b)]

The voltage and current along the NW can be described by the following relations

$$\frac{dV}{dx} = -\frac{\rho_s I}{\pi r^2}$$, where ρ_s is the NW channel resistivity 2.3

$$\frac{dI}{dx} = -\frac{\pi r}{\rho_c}(v_0 - V) \qquad 2.4$$

Combining 2.3 and 2.4, we get

$$\frac{d^2 I}{d^2 x} - \frac{\rho_s I}{r \rho_c} = 0 \qquad 2.5$$

Using the boundary conditions $I(0) = 0$, $I(W) = i_0$,

We obtain the following solution:

$$I(x) = i_0 \frac{\sinh(\frac{x}{L_T})}{\sinh(\frac{W}{L_T})} = 0 \qquad 2.6$$

, where $L_T = \sqrt{r\rho_c/\rho_s}$ is the transmission length of the Fig. 2 − 21(a) network. 2.7

Using the equation 2.4 and 2.6,

$$V(x) = v_0 - \frac{\rho_c i_0 \cosh(\frac{x}{L_T})}{\pi r L_T \sinh(\frac{W}{L_T})} \qquad 2.8$$

Since $V(W) = 0$,

$$v_0 = \frac{\rho_c i_0 \coth(\frac{W}{L_T})}{\pi r L_T} \qquad 2.9$$

Using 2.9, the relation between R_c and ρ_c can be obtained as following:

$$R_c = \frac{v_0}{i_0} = \frac{\rho_c \coth(\frac{W}{L_T})}{\pi r L_T} = \frac{\rho_s L_T \coth(\frac{W}{L_T})}{\pi r^2} \qquad 2.10$$

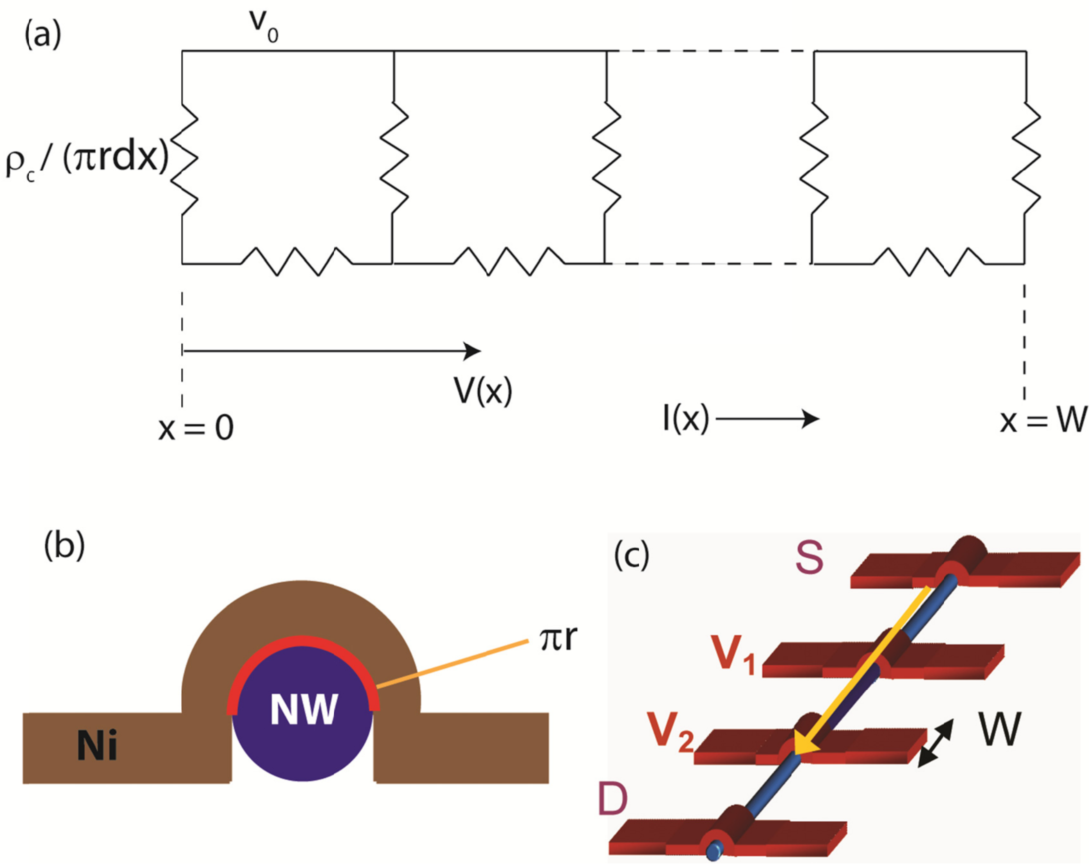


Figure 2-22: (a) Transmission line model for a metal/semiconductor nanowire contact. (b) Schematic representation of metal (Ni) deposited on a NW. The line denotes the circumference of the NW in contact with the deposited Ni. (c) Schematic representation of a multi-terminal device used for device characterization.

Based on equation 2.10, specific contact resistance of boron (B)- and phosphorus (P)-doped NWs were extracted. The contact resistances can be readily measured by subtracting the intrinsic channel resistance determined from the 2-point NW resistance. The channel resistance can be determined with 4-point current-voltage characteristics. Using the exacted R_c and ρ_s values into equation 2.10, we determine ρ_c.

Using equation 2.10, the metal (Ni) to NW specific contact resistances for both boron- and phosphorus-doped NWs were extracted. Table 2-2 summarizes the NW resistivities (ρ_s), contact resistances (R_c), and specific contact resistances (ρ_c) of B- and P-implanted NWs at different doses and dopant activation temperatures. Boron-doped NWs show lower contact resistances and specific contact resistances by comparison to P-doped NWs implanted at the same dose. In addition, the ρ_c values did not change much with the activation temperature. For B-implant doses above 5×10^{14} cm^{-2}, very low R_c and ρ_c values were achieved, where the R_c values between the Ni and a Ge-Si_xGe_{1-x} core-shell NW are 300 ± 200 Ω, corresponding to ρ_c values of $1.1 \times 10^{-9} \pm 2.2 \times 10^{-10}$ $\Omega \cdot cm^2$. On the other hand, in P-doped NWs, the R_c and ρ_c values were generally higher than those of B-doped NWs. Besides, higher thermal budget and implant dose, compared with the B-doping, are necessary to obtain the ρ_s below 10^{-2} $\Omega \cdot cm$, and the extracted ρ_c values were fluctuated more with the activation temperature for a given implant dose. Here, the lowest average ρ_c value, $9.7 \pm 9.5 \times 10^{-9}$ $\Omega \cdot cm^{-2}$, was observed at 500 °C at a dose of 10^{15} cm^{-2} while the lowest average ρ_s value was found at 600 °C at the same dose. Unlike the B-implant dose, the P-implant dose of 5×10^{14} cm^{-2} was not sufficient to obtain the low ρ_c and ρ_s. Whereas, at a P-implant dose of 2×10^{15} cm^{-2}, ρ_c and ρ_s values were sharply increased compared with those from an implant dose of 10^{15} cm^{-2}, which may be due to the implant-induced defect generation and segregation of the excessive dopants at the high implant dose as noted previously.

Table 2-2: Ion-implanted NW resistivities and NW-to-Ni contact resistances

Activation Temperature (˚C)	Dopant, Dose (cm^{-2})	Resistivity (Ω·cm)	Contact resistance (Ω)	Specific contact resistance (Ω·cm^{-2})
400	B, 10^{15}	$2.9 \pm 0.6 \times 10^{-3}$	330±41	$12 \pm 1.8 \times 10^{-10}$
	B, 5×10^{14}	$4.9 \pm 0.5 \times 10^{-3}$	480±90	$16 \pm 5.2 \times 10^{-10}$
	B, 10^{14}	$30 \pm 12 \times 10^{-3}$	1900±1480	$4.9 \pm 3.8 \times 10^{-8}$
	P, 10^{15}	$20 \pm 4 \times 10^{-3}$	6300±2100	$5.4 \pm 3.7 \times 10^{-8}$
450	P, 2×10^{15}	$17 \pm 5 \times 10^{-3}$	9800±4900	$1.7 \pm 0.6 \times 10^{-7}$
500	B, 10^{15}	$3.0 \pm 0.4 \times 10^{-3}$	168±14	$4.0 \pm 1.3 \times 10^{-10}$
	B, 5×10^{14}	$5.4 \pm 0.8 \times 10^{-3}$	243±73	$5.2 \pm 2.4 \times 10^{-10}$
	B, 10^{14}	$35 \pm 6.5 \times 10^{-3}$	3400±2900	$2.3 \pm 2.0 \times 10^{-8}$
	P, 10^{15}	$6.3 \pm 2.2 \times 10^{-3}$	1050±760	$9.7 \pm 9.5 \times 10^{-9}$
600	B, 10^{15}	$2.7 \pm 0.5 \times 10^{-3}$	220±130	$7.6 \pm 6.8 \times 10^{-10}$
	B, 5×10^{14}	$4.6 \pm 0.5 \times 10^{-3}$	270±110	$3.9 \pm 1.2 \times 10^{-10}$
	B, 10^{14}	$38 \pm 6.2 \times 10^{-3}$	3600±2800	$2.0 \pm 1.8 \times 10^{-8}$
	P, 2×10^{15}	$30 \pm 10 \times 10^{-3}$	12000±5300	$1.4 \pm 0.8 \times 10^{-7}$
	P, 10^{15}	$5.6 \pm 0.7 \times 10^{-3}$	2200±1400	$2.4 \pm 1.3 \times 10^{-8}$
	P, 5×10^{14}	$25 \pm 8 \times 10^{-3}$	14000±2900	$2.2 \pm 1.8 \times 10^{-7}$
650	B, 10^{15}	$3.7 \pm 0.9 \times 10^{-3}$	280±120	$1.3 \pm 1.1 \times 10^{-9}$
	B, 5×10^{14}	$7.2 \pm 2.0 \times 10^{-3}$	260±280	$8.1 \pm 7.8 \times 10^{-10}$

2.4 SUMMARY

In Chapter 2, we described the growth of Ge-Si_xGe_{1-x} core-shell NWs using a combination of VLS Ge NW growth and UHV CVD SiGe growth, The boron- and phosphorus-doping of the NWs using low energy ion implantation were systematically investigated. The data show the successful doping of Ge-Si_xGe_{1-x} core-shell NWs using ion implantation, both for boron and phosphorus. A B-doping concentration as high as 2 10^{20} cm^{-3} was achieved using ion implantation, with specific contact resistances as low as 4×10^{-10} $\Omega\cdot cm^2$. Similarly low channel resistances and contact resistances were also observed in P-doped NWs. Based on these results, high performance NW FETs and NW TFETs can be fabricated by employing conventional CMOS processes, as we describe in the following chapter.

CHAPTER 3

High Performance Germanium Nanowire Field-effect Transistors

Ge-Si_xGe_{1-x} core-shell NWs are the promising channel material for aggressively scaled FETs as discussed in Chapter 1. Most of all, gate-all-around device (GAA) geometry can be easily implemented along a NW due to its cylindrical structure, providing enhanced electrostatic control over the channel. In addition, thanks to Ge's higher hole mobility compared with other major group IV semiconductors and group III-V compound semiconductors, high performance *p*-type MOSFETs can be realized using the NWs. Despite the potential advantages that the Ge-Si_xGe_{1-x} core-shell NWs provide, the performance of the device will still be limited by the Schottky barrier at the metal-semiconductor interface when the metal is directly deposited on the source/drain regions of the NW. Moreover, ambipolar device characteristics are often observed in such devices [31]. Thus, a key to obtain the high performance NW FETs is the ability to highly dope the source and drain regions of the NW FETs. In the previous chapter, the NW-doping was successfully demonstrated using low energy ion implantation, where the B-doping concentration up to 10^{20} cm^{-2} was obtained in the NWs. Based on this finding, high performance Ge-Si_xGe_{1-x} core-shell NW FETs can be realized by utilizing CMOS fabrication process.

This chapter begins with describing the fabrication processes of Ω-shaped gate Ge-Si_xGe_{1-x} core-shell NW FETs with highly doped S/D, followed by investigations of the improved electrical characteristics by comparison to *undoped* S/D NW FETs. Using the high performance Ge-Si_xGe_{1-x} core-shell NW FETs with different gate lengths, the scaling properties of the devices are scrutinized. In addition, TCAD simulation (Synopsis®) was employed to better understand the observed experimental results.

Lastly, the device characteristics were also demonstrated for the NW FETs with different Si_xGe_{1-x} shell compositions.

3.1 FABRICATION PROCESS OF Ω-SHAPED GATE $GE\text{-}SI_XGE_{1-X}$ CORE-SHELL NW FETS

The fabrication process flow of Ω-shaped Ge-Si_xGe_{1-x} core-shell NW FETs is outlined in the Figure 3-1 and Table 3-1. After nanowire growth, the wafer was cleaved into small pieces using a diamond scriber. A wafer piece (~ 1cm ×1cm) with the NWs on it was suspended in an ethanol solution and then sonicated for 10 s and then dispersed on a substrate consisting of a 10 nm thick HfO_2 (10 nm) layer grown on a Si (100 *n*-type) substrate, which can serve as back-gate [Figure 3-1(a)]. The NWs on the substrate was clean with a 2% HF solution for 20 s and DI water for 20 s for 2 cycles. Right after cleaning steps, the gate oxide, a 9 nm-thick HfO_2, is deposited by atomic layer deposition (ALD) at 250 ˚C [Figure 3-1(b)]. The equivalent oxide thickness (EOT) was ~3.9 nm, verified by capacitance-voltage measurement on planar capacitors processed in parallel with the device. The gate electrode was patterned by EBL, followed by 120 nm of tantalum nitride (TaN) deposition. After lift-off, the device was clean with O_2 plasma for 10 s (50 W) to remove PMMA residues. The HfO_2 layer on S/D regions was etched by diluted HF (3 %). Next, using the self-aligned process, B-implanted at the energy of 3 keV and with a dose of 10^{15} cm^{-2}, and rotating 360 ˚ with 32 ˚ tilt during the ion implantation, which results in highly doped NW on S/D region *outside* the TaN metal gate. [Figure 3-1(c)] The devices were then annealed at 600 ˚C for 5 min in an N_2 ambient to activate dopants as well as remove implant-induced crystal damage in NWs. Subsequently the S/D contacts were defined by EBL again, followed by 100 nm of Ni deposition and lift-off. To improve contact on S/D, one minute contact anneal at 300 ˚C was performed and it finalizes device fabrication. [Figure 3-1(d)] Figure 3-1(e) shows a SEM of the fabricated device and Ω-shaped gate structure.

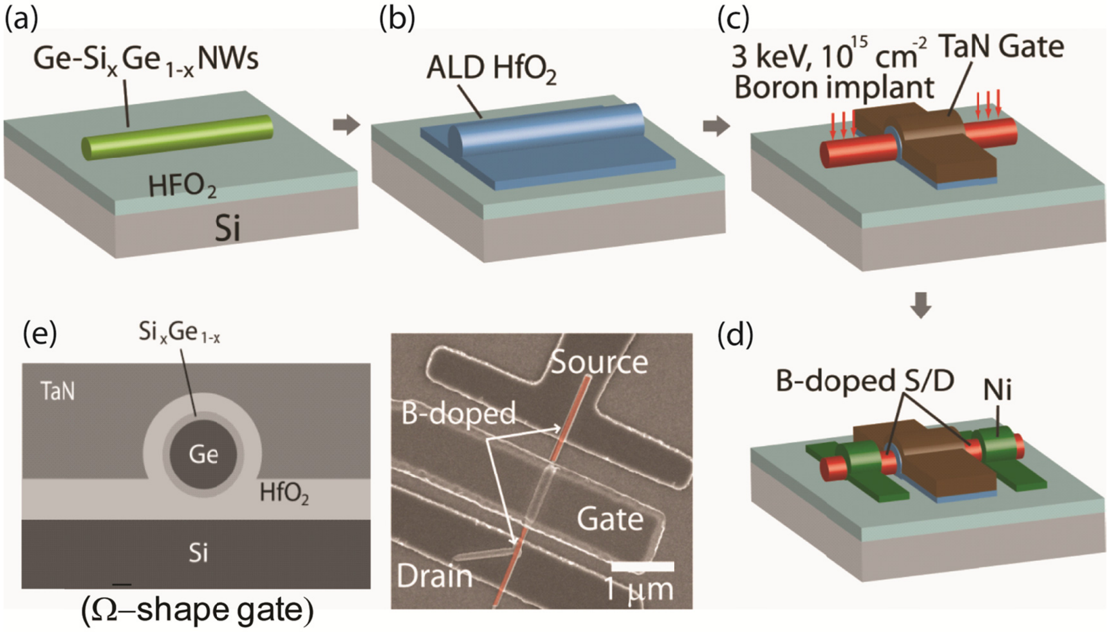


Figure 3-1: Schematic representation of a Ω-shaped gate Ge-Si$_x$Ge$_{1-x}$ core shell NW FET fabrication process flow and scanning electron micrograph

Table 3-1: Device fabrication process flow of Ge-Si$_x$Ge$_{1-x}$ core-shell NW FETs

- NW dispersion on a HfO$_2$(10 nm) / Si (n) substrate
- Native oxide removal on a NW using HF (2%) clean
- ALD HfO$_2$ deposition (9 nm) on a Ge-Si$_x$Ge$_{1-x}$ core-shell NW
- E-beam lithography to define a gate electrode
- TaN gate metal deposition (120 nm) using sputter and lift-off
- O$_2$ plasma clean at PWR 50W for 10s
- HFO$_2$ layer removal on the S/D regions using HF (3%)
- Boron implantation (dose:10^{15} cm^{-2}, energy: 3 keV, angle: 32°)
- Dopant activation (RTP, 600 °C, 5min)
- EBL to define S/D metal contacts and 100 nm Ni deposition

3.2 GE-SI$_X$GE$_{1-X}$ CORE-SHELL NW FETS WITH HIGHLY DOPED SOURCE AND DRAIN

To illustrate the role of doped source and drain on device characteristics, two NW FETs were prepared, where one device has a *highly doped* S/D while the other has an *undoped* S/D. Both NW FETs were fabricated using the process explained in Chapter 3.1, except that the *undoped* S/D NW FET was fabricated without a boron implantation step [Figure 3-1(c)]. Figure 3-2 shows a scanning electron micrograph (SEM) of a fabricated NW FET, where the S/D regions are either highly doped or undoped. Here L_g denotes the gate channel length and L_s denotes source/drain extensions, the section not covered by the top-gate electrode.

Figure 3-3 shows the electrical characteristics of NW FETs *without* B-doping in the S/D regions. Figure 3-3(a) shows the output characteristics (I_d-V_d) of the NW FET for two different back-gate biases, V_{bg} = 0 V and V_{bg} = -1.5 V. The NW FET has a diameter of 60 nm, L_g of 720 nm, and L_s of 830 nm.

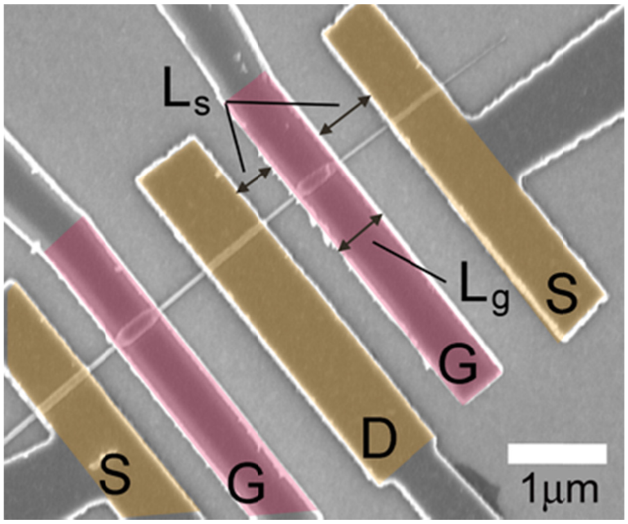


Figure 3-2: SEM of a dual-gated NW FET. The red regions (G) represent the gates, and the yellow regions represent the S/D. L_g denotes a gated channel length and L_s denotes a ungated channel length.[92]

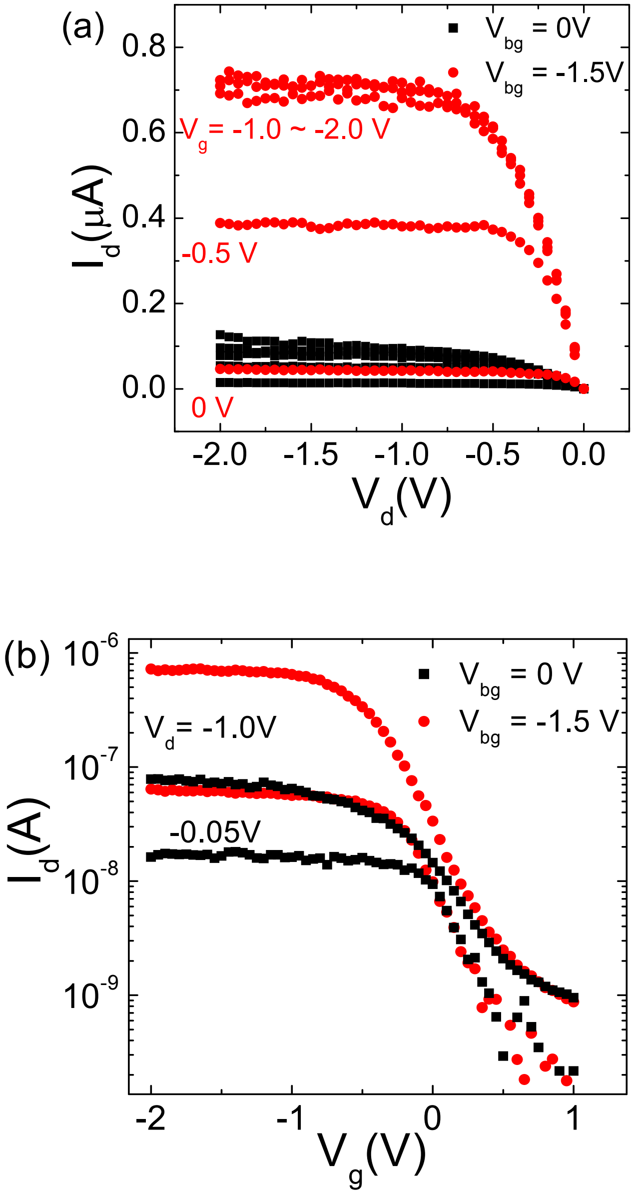


Figure 3-3: Electrical characteristics of a Ge-Si_xGe_{1-x} core-shell NW FET with undoped S/D, and with a channel length L_g = 720 nm. (a) I_d *vs* V_d data measured at different V_g values. (b) I_d *vs* V_g data measured at different V_d values. The data in both panels were measured at two back-gate biases: V_{bg} =0 V (square, black symbols) and V_{bg} = -1.5 V (round, red symbols). [Ge52AF002,F008] [92]

Figure 3-3(b) data show the transfer characteristics (I_d-V_g) for two values of V_{bg}. Here, ON-state (I_{ON}) and OFF-state (I_{OFF}) are defined as the drain current measured at $V_d = V_{cc} = -1.0$ V, and at top-gate biases $V_g = V_T + 0.7V_{cc}$ (ON-state) and $V_{off} = V_T - 0.3V_{cc}$ (OFF-state) respectively; V_T represents the threshold voltage of the device, defined by linearly extrapolating I_d vs V_g, measured at $V_d = -0.05$ V, to zero I_d.

Two observations are apparent from the data of Figure 3-3. First, the ON current is very low at $V_{bg} = 0$ V. The device shows a maximum current of 120 nA at $V_d = V_g = -2.0$ V, and an ON current $I_{ON} = 40$ nA, corresponding *ON/OFF* current ratio equal to 20 at $V_{bg} = 0$ V. The low I_{ON} is largely due to the resistance of the NW sections not covered by the top-gate, which acts as a series resistance (R_{ext}), combined with the metal to NW contact resistance (R_c) at the *S/D*. The measured channel resistance (R_m) is the sum of R_c, R_{ext}, and the top-gated channel resistance (R_{ch}). In order to roughly estimate the fraction of R_c and R_{ext} in R_m, R_{ch} is calculated by assuming a typical mobility (μ) value of ~ 80 cm^2/V·s, determined by a 4-point gate dependent measurement on the same intrinsic Ge-Si_xGe_{1-x} core-shell NWs. The expected value of R_{ch} at $V_g = -1.0$ V, using $R_{ch} = L_g[C_{ox}(V_g - V_t)\mu]^{-1}$ is ~46 kΩ; C_{ox} represents the NW capacitance per unit length. For this estimate, the capacitance value, $C_{ox} = 1.56$ nF/m, was calculated using a finite element method. On the other hand, the extracted R_m value at $V_g = -1.0$ V is 6.2 MΩ. Obviously, the intrinsic channel resistance is very small by comparison to the contact and series resistance. Thus, the performance of this NW FET is primarily degraded by the contact and series resistances.

Second, the device performance can be significantly changed by applying a back-gate bias. A negative V_{bg} value increases the hole concentration in the NW sections not covered by the top-gate, thereby reducing R_c and R_{ext}. The data of Figure 3-3 show a ten-fold increase in ON current for $V_{bg} = -1.5$ V compared to $V_{bg} = 0$ V, and a corresponding increase in *ON/OFF* current ratio to 130. The subthreshold slope (*SS*), defined as $SS = -[d(\log_{10} I_d)/dV_g]^{-1}$ at V_d = -0.05 V, decreases from 420 mV/dec for V_{bg} = 0 V, to 360 mV/dec for V_{bg} = -1.5 V. The overall performance enhancement is primarily due to reduced R_{ext} and R_c with applied V_{bg}, resulting in an increase in I_d. This confirms that the performance of NW FETs with undoped *S/D* is significantly limited by the contact and series resistances.

Figure 3-4(a) shows the output (main panel) and transfer (inset) characteristics for a NW FET, where S/D regions were B-doped using low (3 keV) energy ion implantation, at a dose of 1×10^{15} cm^{-2}. The NW diameter is 36 nm, and the device dimensions are L_g = 720 nm and L_s = 850 nm. Based on these data, the estimated value of external resistance, $R_{ext} + R_c$, for the NW FET with B-doped *S/D* of Figure 3-4(a) is 21.7 ± 1.8 kΩ. The NW FET with *doped S/D* of Figure 3-4(a) shows a maximum current I_{max} = 11 μA measured at V_g = -2.0 V, and a subthreshold slope, *SS* = 270 mV/dec. The *SS* value is relatively high compared to the thermal limit of 60mV/dec, and could stem from a high interface trap density. The ON-current has a value I_{ON} = 2 μA at V_d = -1.0 V, corresponding to an *ON/OFF* ratio of ~200. For comparison, in Figure 3-4(b), the output (main panel) and subthreshold (inset) characteristics for the NW FET with *undoped S/D* at $V_{bg} = 0$ *V* is shown, examined in Figure 3-3. Note that the two devices of Figure 3-4 have similar L_g and L_s dimensions. Compared with the undoped *S/D* NW FET of Figure 3-4(b), the I_{max} of the top-gated device with B-doped *S/D* is two orders of magnitude larger, and the *ON/OFF* ratio shows a ten-fold increase. Clearly, the device performance is enhanced after *S/D* B-doping. The device resistance R_m, measured at $V_g = -1.0$ *V* in the linear (small V_d) regime is 130 kΩ.

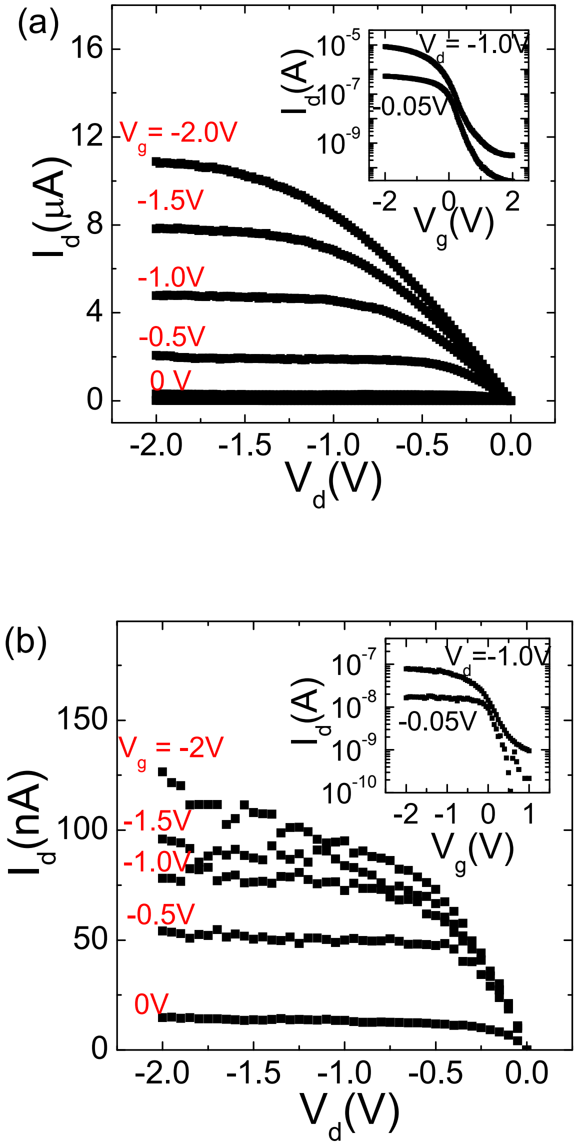


Figure 3-4: Electrical characteristics of a Ge-Si_xGe_{1-x} core-shell NW FET with undoped S/D, and with a channel length L_g = 720 nm. (a) I_d *vs* V_d data measured at different V_g values. (b) I_d *vs* V_g data measured at different V_d values. The data in both panels were measured at two back-gate biases: V_{bg} =0 V (square, black symbols) and V_{bg} = -1.5 V (round, red symbols). [92]

Using $R_m = R_c + R_{ext} + R_{ch}$ along with estimates for R_c and R_{ext}, R_{ch} is estimated to be ~108 kΩ. Thus, R_c and R_{ext} are small relative to R_{ch}, and the operation of Ge-Si_xGe_{1-x}NW-FET is now primarily limited by R_{ch} rather than R_c and R_{ext}. The corresponding effective mobility, extracted using the calculated gate capacitance per unit length of $C_{ox} = 0.95$ nF/m, is $\mu_{eff} = 60$ cm^2/V·s.

In summary, dual-gated Ge-Si_xGe_{1-x} core-shell NW FETs with highly doped source and drain show enhanced performance with respect to NW FETs with undoped *S/D*, thanks to reduced series and contact resistances, combined with efficient carrier injection from the doped *S/D*.

3.3 SCALING PROPERTIES OF GE-SI_XGE_{1-X} CORE-SHELL NW FETS

To further investigate the electronic properties, as well as prospect the potential device applications of Ge-Si_xGe_{1-x} core-shell NWs, the device performance as a function of gate channel length needs to be systematically investigated.

To probe the scaling properties of Ge-Si_xGe_{1-x} core-shell NW FETs, NW FETs with different channel lengths from 300 nm to 1 μm were fabricated. Based on the results in Chapter 2.2.4, in the B-doped S/D regions, we expect the a doping concentration of $10^{19} \sim 10^{20}$ cm^{-3}, a NW resistivity of $2.6 \times 10^{-3} \pm 1.9 \times 10^{-4}$ Ω·cm, and a Ni-NW specific contact resistivity of $1.1 \times 10^{-9} \pm 2.2 \times 10^{-10}$ Ω·cm^2, corresponding to contact resistances of 300 ± 200 Ω. Thus, the performance of NW FETs is not limited by external resistance components.

3.3.1 Electrical characteristics

To characterize the devices, the output characteristics (I_d-V_d) and transfer characteristics (I_d-V_g) of NW FETs were measured. Figure 3-5 shows output and transfer characteristics of Ge-Si_xGe_{1-x} core-shell NW FETs with different channel lengths (L_g), from 300 nm to 1 μm. The diameters of NWs in these NW FETs are in the similar range, i.e., d = 52 ± 4 nm. On the right axis of output characteristics, the drain current normalized to the NW's diameter are shown to facilitate the comparison of device characteristics between the devices. One apparent from the data in Figure 3-5 is that the maximum attainable I_d and transconductance values proportionally increase with the decreasing L_g. As L_g scales from 1 μm to 300 nm, the maximum I_d measured at $V_d = V_g = -2.0$ V increases to 12, 22, and 45 μm, corresponding to the normalized currents of 240, 420, and 800 μA· μm^{-1}. The transfer characteristics measured at $V_d = -1.0$ V shows peak transconductance of 6.1, 11.5, and 19.6 μS for each channel length L_g = 1 μm, 500nm, and 300 nm. Gate leakage currents in all measurement were below 10 pA.

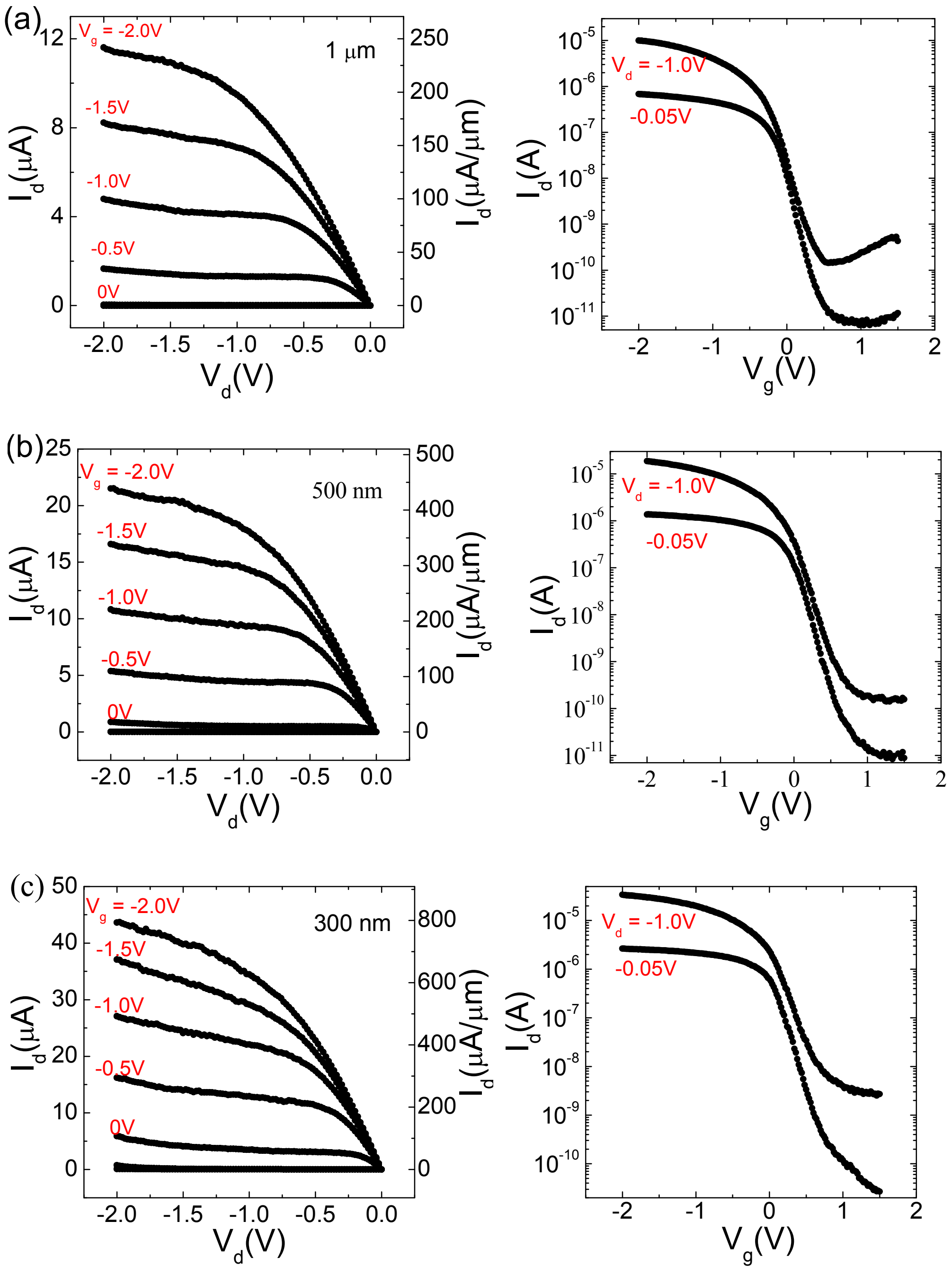


Figure 3-5: Electrical characteristics of a Ge-Si$_x$Ge$_{1-x}$ core-shell NW FET at different gate lengths (a) L_g = 1 µm d = 48 nm (b) L_g = 500 nm d = 49 nm (c) L_g = 300 nm d = 55 nm. In each panel, the left-side (right-side) graphs show I_d – V_d (I_d-V_g) characteristics. The axis on the right side of output characteristics show I_d normalized to the NW diameter (d). [Ge52AF010] [93]

3.3.2 Effective mobility

Effective mobility of Ge-Si_xGe_{1-x} core-shell NW FETs can be calculated using the relation,

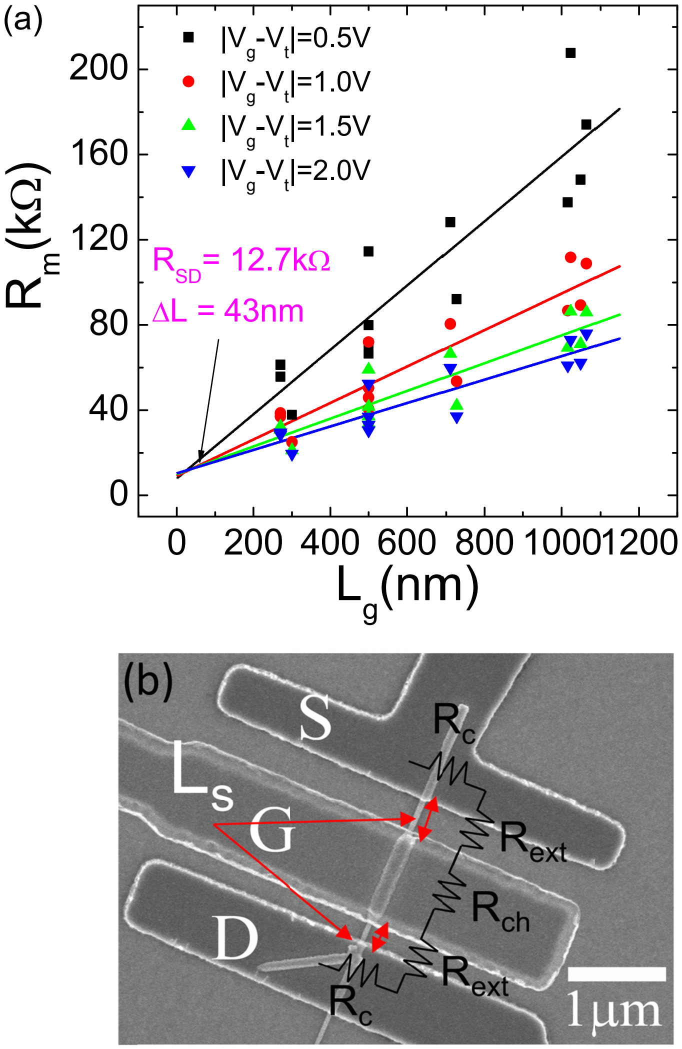
$$\mu_{eff} = \frac{L_{eff}\left(= L_g - \Delta L\right)}{R_{ch}C_{ox}\left|V_g - V_t\right|} \qquad 3.1$$

,where μ_{eff} is an effective mobility, L_{eff} is an effective channel length, the difference between the gate length (L_g) and the channel length reduction (ΔL), R_{ch} is an intrinsic channel resistance, and C_{ox} is the top-gate capacitance per unit length. Thus, the L_{eff}, R_{ch}, and C_{ox} values needs to be determined to calculate the effective mobility.

First, to obtain R_{ch} and L_{eff} values, the resistances between the source and the drain (R_m) are measured for different gate overdrive voltages $|V_g - V_t|$, from 0.5 V to 2.0 V, as a function of the gate channel lengths as shown in Figure 3-6(a). The measured resistance (R_m) is the sum of R_{ch} and the external series resistance (R_{SD}), and it can be expressed by the following relation,

$$R_m = \frac{V_d}{I_d} = R_{ch} + R_{SD} = \frac{L_{eff}(= L_g - \Delta L)}{\mu_{eff}C_{ox}|V_g - V_t|} + R_{SD} \qquad 3.2$$

For these measurements the low V_d = -0.05 V was applied, ensuring device operation in the *linear* region. The R_m values at different gate channel lengths for the each gate overdrive voltage are fitted with linear lines and these lines are intersecting at one point, where $R_m = R_{SD}$ = 12.7 kΩ for $L_g = \Delta L$= 43 nm can be obtained as shown in Figure 3-6(a). Thus, by subtracting R_{SD} from R_m and ΔL from L_g, R_{ch} and L_{eff} can be determined. Here, R_{SD} is the sum of the metal-NW contact resistance (R_c) and the extension resistance (R_{ext}) of L_s which is a highly-doped but not gated section of the NW [Figure 3-6(b)]. We note that high R_{SD} value stems mainly from R_{ext}, estimated as ~ 11 kΩ using Table 2.2. Thus, the performance of the NW FETs can be further improved by reducing L_s.



$$R_{SD} = 2R_{ext} + 2\,R_c$$

Figure 3-6: (a) Measured device resistance R_m at $V_d = -0.05$ V for different gate lengths. The common intercept determine both the external resistance and the effective channel length reduction. (b) Scanning electron micrograph of a fabricated NWFET, showing resistance components of the device.

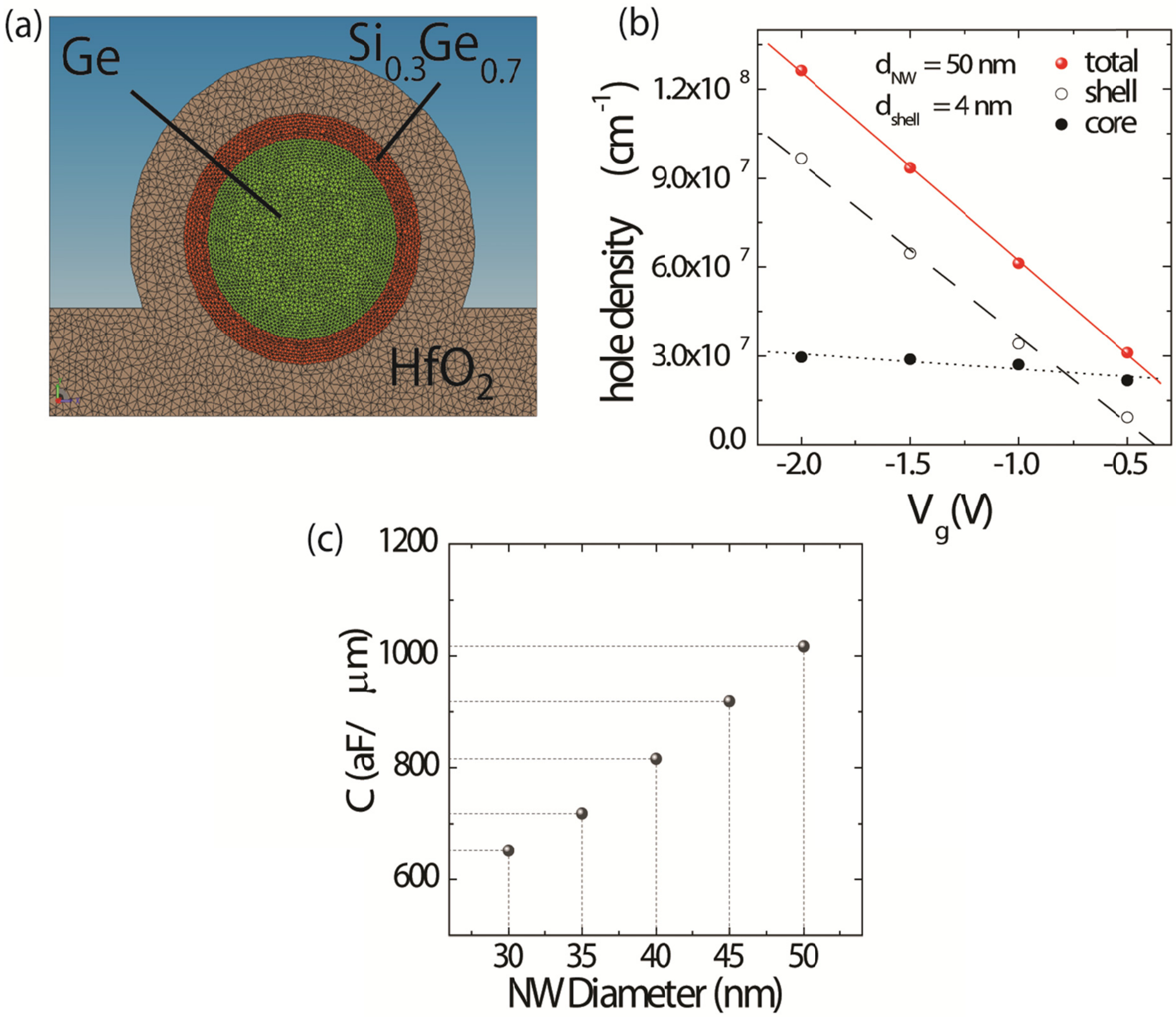


Figure 3-7: (a) Schematic representation of a Ge-Si_xGe_{1-x} core-shell NW FET used in the simulation. (b) Total hole density *versus* gate voltage. The total hole density is the sum of the hole densities in the NW core and shell. (c) Capacitance *versus* NW diameter. The capacitance values were calculated using the relation $C_{ox} = e \cdot (dp/dVg)$.[93]

In addition to R_{ch} and L_{eff} values, C_{ox} value should also be known to calculate the effective mobility. In this study, C_{ox} values were determined by using Sentaurus TCAD simulation (Synopsis®). The device structure used in simulations is shown in Figure 3-7 (a). It consists of a Ge core of varying size, a 4 nm-thick $Si_{0.3}Ge_{0.7}$ shell, and with a HfO_2

dielectric / TaN metal stack corresponding to the actual device. The valence band offset between $Si_{0.3}Ge_{0.7}$ and Ge interface was 0.05 eV in the simulation. Applying a negative gate bias initially induces holes in the Ge core, and at sufficiently large gate bias holes start to populate in the $Si_{0.3}Ge_{0.7}$ shell. Figure 3-7(b) data show an example of hole densities in the core and shell calculated for a Ge-$Si_{0.3}Ge_{0.7}$ core-shell with a 50 nm diameter and a 4 nm–thick shell. The total hole density per unit length (p) in a Ge-Si_xGe_{1-x} NW for a given gate voltage is calculated by summing the carrier density both in the shell and the core of a NW [Figure 3-7(b)]. The carrier concentration in NW is then obtained using $Q = e \cdot p = C_{ox} \cdot |V_g - V_t|$, where e is the electron charge and V_t is a threshold voltage. Total capacitance per unit length is extracted using $C_{ox} = e \cdot (dp/dV_g)$. Figure 3-7(c) summarizes the results of the Ω-shaped gate capacitances (C_{ox}) for different NW diameters.

Finally, by inserting the R_{ch}, L_{eff}, and C_{ox} values into the equation 3.1, the intrinsic carrier mobility in Ge-Si_xGe_{1-x} core-shell NW FETs can be extracted. Figure 3-8 shows the μ_{eff} values as a function of $|V_g - V_t|$. The results in the Figure 3-8 show that the peak mobility values ranges from 100 to 180 $cm^2 \cdot (V \cdot s)^{-1}$, which are threefold higher than those of the reported Si p-MOSFETs with HfO_2 gate dielectric [74].

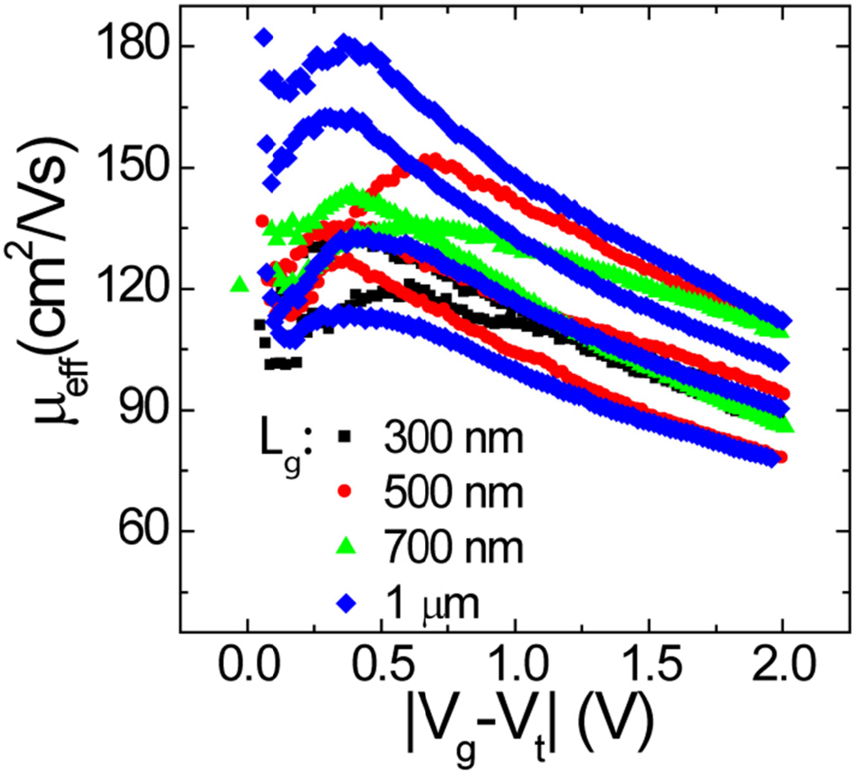


Figure 3-8: Effective mobility of the Ge-Si_xGe_{1-x} core-shell NW FETs for four different channel lengths as a function of gate overdrive.

3.3.3 Ge-Si_xGe_{1-x} core-shell NW FETs benchmarking

Two main figure of merit for logic devices are the ON- and OFF-state currents. The ON-state current I_{ON} determines the FET switching speed, whereas I_{OFF} determines the passive power consumed by a logic gate (e.g., an inverter). A high-speed low-power device should possess high I_{ON} and I_{ON}/I_{OFF} ratio. To gauge these performance metrics for our Ge-Si_xGe_{1-x} core-shell NW FETs, the ON-state current I_{ON} is defined as the measured I_d at a gate bias $V_{ON} = V_t + (2/3)\ V_{cc}$, where the V_{cc} value is -1.0 V, as well as the OFF-state current I_{OFF} as the measured I_d at $V_g = V_{OFF} = V_t - (1/3)V_{cc}$. The data in Figure 3-9 show the ON-OFF characteristics of Ge-Si_xGe_{1-x} core-shell NW FETs along with the data from recently reported planar Ge *p*MOSFETs, realized on Ge-on-Si substrate or Ge-on-insulator (GeOI) substrate [75-80]. The gate lengths of Ge *p*MOSFETs are demonstrated down to 60 nm, whereas those of Ge-Si_xGe_{1-x} core-shell NW FETs are shown from 1 μm to 300 nm. In addition, the equivalent oxide thickness (EOT) of the reported devices ranges from 1.4 ~1.9, while that of the NW FETs is ~3.9. We also note that the supply voltages of some devices are V_{cc} = -1.2 V [76, 78, 79].

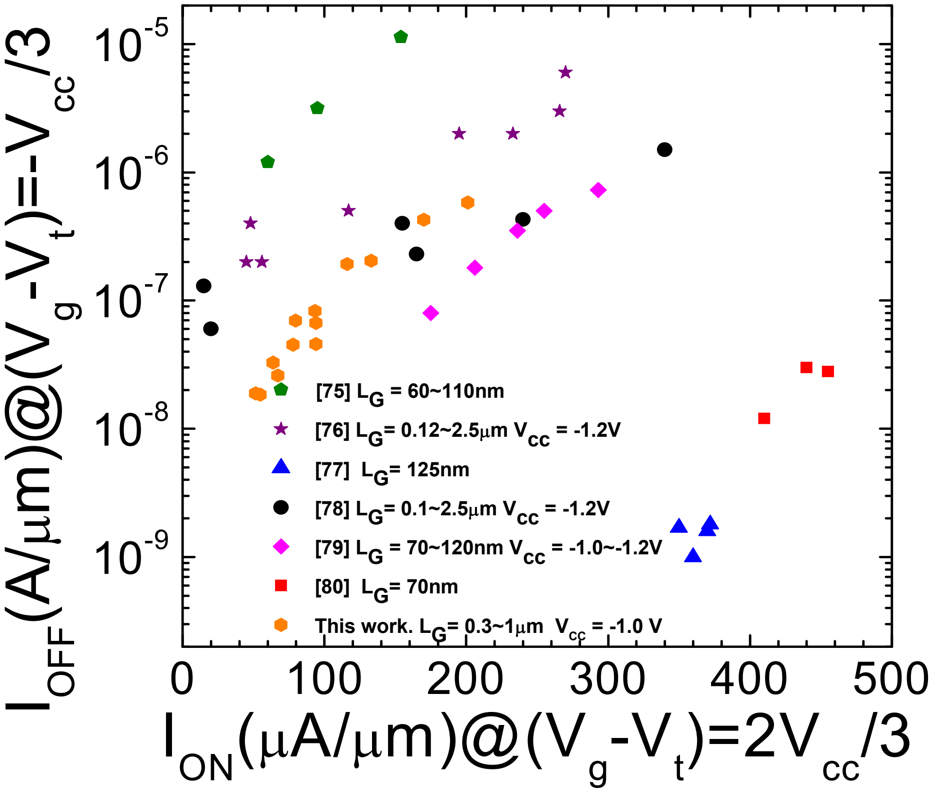


Figure 3-9: ON-OFF characteristics of the Ge-Si_xGe_{1-x} core-shell NW FETs along with planar Ge *p*MOSFETs. The ON-OFF characteristics of the NWFETs are comparable or better than those of most recent Ge *p*MOSFETs [75-80]. ON-currents in the NW FETs can be further increased by the device scaling. The ON-OFF characteristics of the NW FETs was determined using the V_{CC} = -1.0 V.

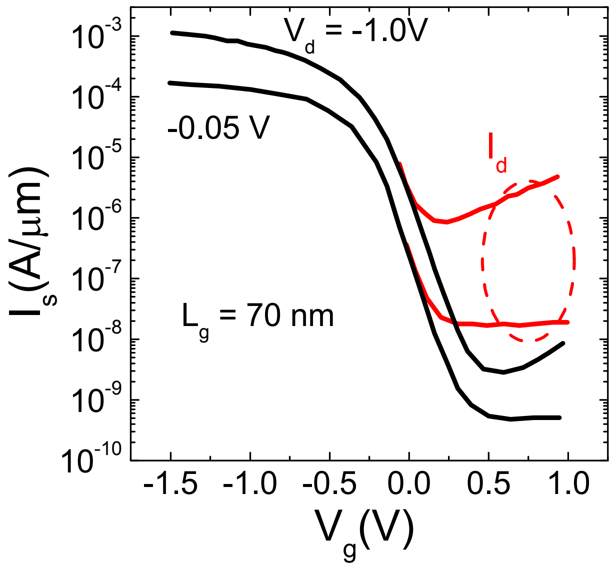


Figure 3-10: Transfer characteristics of the Ge *p*MOSFET measured at the source (black) and the drain (red). A large difference between I_d and I_s is originated the reverse-based diode leakage current between the drain (*p*+) and the substrate (*n*) [79].

As a result, higher ON-state currents were demonstrated in Ge *p*MOSFETs by comparison to the NW FETs [Figure 3-9]. However, ON-currents in our devices will be further increased by reducing the device dimensions. For similar gate lengths, the ON-OFF characteristics of NW FETs are comparable or better than those of Ge *p*MOSFETs. Lastly, we note that the OFF-currents of the Ge *p*MOSFETs fabricated on Ge-on-Si substrates were measured at the source due to high leakage current at the drain-substrate junction, which results in underestimation of OFF-currents [Figure 3-10] [75, 77, 78, 80]. The main source of the leakage current is reverse biased diode leakage currents at the drain (*p*+)/substrate (*n*) junction, where the drain is negatively biased and substrate is grounded. By comparison, ON-OFF characteristics of Ge-Si_xGe_{1-x} core-shell NW FETs and Ge *p*MOSFETs fabricated on GeOI, where the body is isolated by the oxide layer underneath, were all measured from the drain currents (I_d).

Next, to estimate the switching speed in our devices, we employ the intrinsic gate delay τ, which is defined as $\tau = CV/I$, where C is the gate capacitance, $V = V_{cc} = -1.0$ V, and $I = I_{ON}$. Figure 3-11 shows the relation between τ and the I_{ON}/I_{OFF} ratio of Ge-Si_xGe_{1-x} core-shell NW FETs along with previously reported data from Ge-Si core-shell NW FETs and Ge *p*MOSFETs [36, 77, 80]. Here we define a window of $V_{ON} - V_{OFF} = V_{cc} = -1$ V along the V_g axis to determine I_{ON} and I_{OFF}.

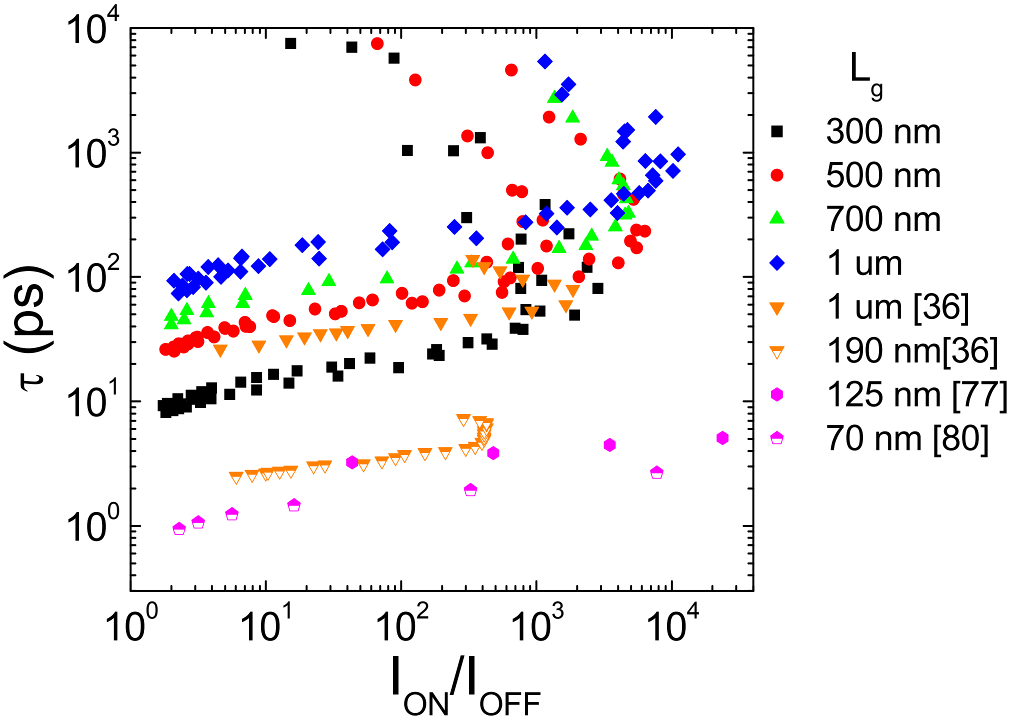


Figure 3-11: Intrinsic gate delay (τ) versus I_{ON}/I_{OFF} ratio for different L_g values along with Ge-Si core-shell NW FETs [36] and Ge *p*MOSFETs [77, 80] data from the literatures. The gate delay of our Ge-Si_xGe_{1-x} core-shell NW FETs is expected to further minimized with the gate length scaling.

The data in Figure 3-11 illustrates the tradeoff between I_{ON}/I_{OFF} and τ, meaning that CV/I improves with the reducing I_{ON}/I_{OFF} by increasing ON-state current at higher gate overdrive, while sacrificing the significant increase in I_{OFF} current. The I_{ON}/I_{OFF} ratio of the NW FETs reaches a maximum of up to 10^4, which is a ten-fold higher value than previous results in Ge-Si core-shell NW FETs [36] and is similar to the values in Ge MOSFETs whose I_{ON}/I_{OFF} was measured at the source [77, 80]. The intrinsic delay of our devices reduces with the gate length scaling and the devices with the same channel length have almost identical τ versus I_{ON}/I_{OFF} data. The intrinsic delay of the Ge-Si_xGe_{1-x} core-shell NW FETs will be further reduced with the device scaling.

3.3.4 Short-channel effects

The subthreshold slopes (*SS*), defined as $SS = -[d(\log I_d)/dV_g]^{-1}$, for different channel lengths are shown in Figure 3-12. These data show *SS* values ranging from 150 to 190 $mV \cdot dec^{-1}$. The measured *SS* values are higher than the thermal limit of 60 $mV \cdot dec^{-1}$ at room temperature, a finding that can be attributed to a finite trap density at the dielectric-semiconductor interface. To roughly estimate the density of interface traps (D_{it}) in Ge-Si_xGe_{1-x} NW FETs, *SS* data measured for a 1 μm channel length device is fitted with the equation, $SS = (2.3k_BT/e) \cdot [1 + C_{it}/C_{ox})]$, where C_{it} is a trap capacitance per unit length and *e* is the electron charge. Here, since the NW channel is nominally *undoped*, the depletion capacitance can be neglected. Thus, by inserting the C_{ox} value for a NW with a diameter of 45 nm, the trap capacitance can be obtained as C_{it} = 1500 aF/μm. Using the relation, $C_{it} = e \cdot D_{it}$, the estimated D_{it} was 6.6×10^{12} $cm^{-2}V^{-1}$, which can explain the relatively high *SS* in these devices.

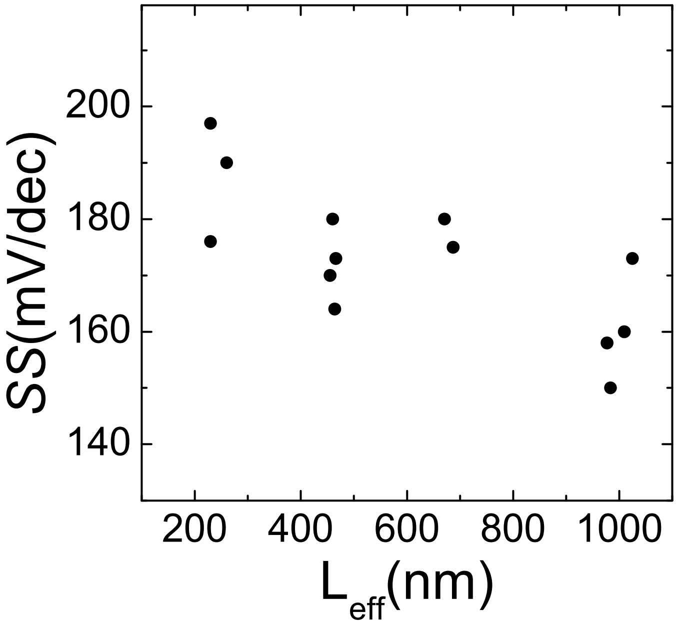


Figure 3-12: Subthreshold swing (*SS*) versus effective gate length. The *SS* values are generally high and slightly increase with the device scaling.

In addition, the drain induced barrier lowering (DIBL) and threshold voltages were also measured for devices with different channel lengths.[Fig. 3-13 and 3-14] In general, DIBL increases with the device scaling, demonstrating that short channel effect starts to emerge at the gate length below 300 nm. The threshold voltages are also slightly rolled off as the gate length shrinks as shown in Figure 3-14. Therefore, the fabrication process should be further optimized to improve the device performance, by reducing the non-gated the source and drain region (L_s), optimizing doping conditions, as well as by improving the dielectric quality.

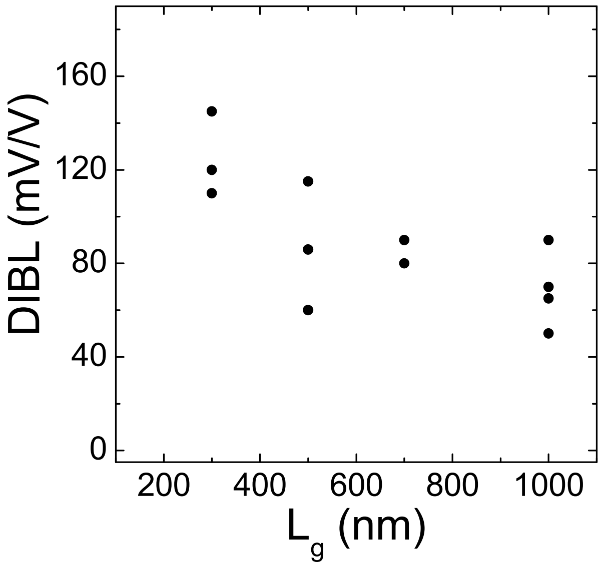


Figure 3-13: DIBL of Ge-Si_xGe_{1-x} core-shell NWFETs as a function of the channel length

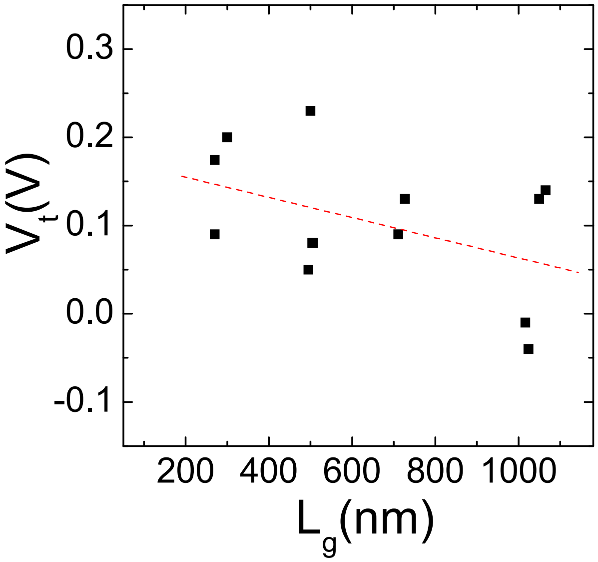


Figure 3-14: Threshold voltage vs. the gate lengths. Slight V_t shift with the device scaling

3.3.5 TCAD simulation results

The electrical characteristics and analyses of Ge-Si_xGe_{1-x} core-shell NW FETs in Chapter 3.3 show DIBL and high substhreshold swing (*SS*), which further increase with the gate length scaling, causing poor short-channel device characteristics. One minor reason for degraded device characteristics at the short channel length may be due to high dielectric constant of Ge (ε_{Ge} =16.0). For example, the electric flux (D_f) at the interface between the gate oxide and the semiconductor channel in a MOSFET is given by $D_f = \varepsilon_{ox}E_{ox} = \varepsilon_{Ge}E_{Ge}$ in Ge MOSFETs, while by $D_f = \varepsilon_{ox}E_{ox} = \varepsilon_{Si}E_{Si}$ in Si MOSFETs ($\varepsilon_{\mathrm{Si}}$=11.9). Thus, for the same D_f, the electric field strength in Ge (E_{Ge}) would be smaller than that in Si (E_{Si}) for the same. This implies that the gate electrostatic control in Ge devices would be less effective compared with Si devices and more prone to shor-channel effects. Next, the electrical characteristics of the devices in Chapter 3.3 show clear indications of gate-induced-barrier-lowering (GIDL) and high D_{it}, and they may have affected on the device performance. Thus, the roles of these factors on the device performance need to be better understood. In order to gain insight on the role of GIDL and D_{it}, the electrical characteristics of Ge-Si_xGe_{1-x} core-shell NW FETs were investigated using Sentaurus TCAD simulation (Synopsis®). Figure 3-15(a) shows the device structure used for the simulations and Fig. 3-15(b) shows the cross section of the device. The device structure used in the simulation is a gate-all-around (GAA) device geometry, where the Ge core has a diameter of 44 nm, the $Si_{0.4}Ge_{0.6}$ shell has a thickness of 5 nm, and SiO_2 gate dielectric has a 5 nm. Similar to the NW used for the experiment, the channel is *undoped* and the S/D, shaded regions in Fig 3-15(b), has the same B-doping concentration of 10^{20} cm^{-3}.

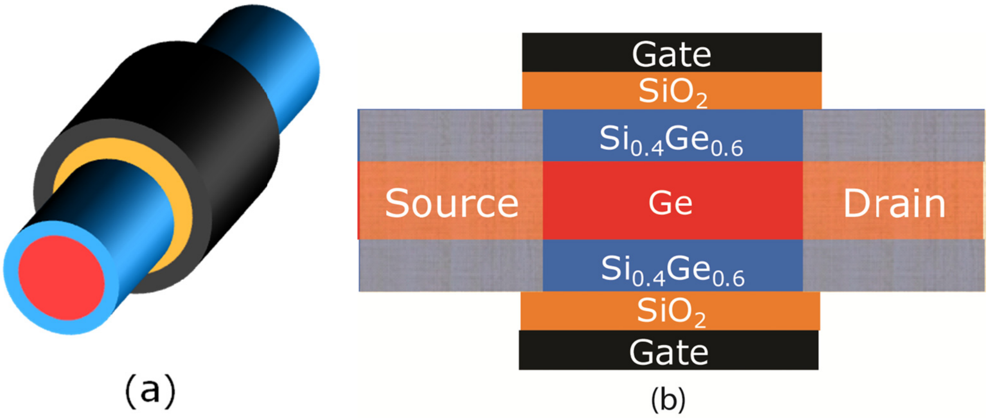


Figure 3-15: (a) Schematics of a Ge-Si_xGe_{1-x} core-shell NWFET with gate-all-around (GAA) device geometry. (b) The cross section of the NW FET. The shaded regions represent B-doped S/D regions (B: 10^{20} cm^{-3}).

The impact of GIDL on the device performance was first investigated. To evaluate the GIDL effect on the device performance, a simple band-to-band tunneling (BTBT) model was included in the device physics model and no trap distribution was assumed in the simulation. The plots in Figure 3-16 show the transfer characteristics from the simulation results. When the BTBT model is not included in the simulation, OFF-state currents at both high and low drain biases remain at the same value. On the other hand, when the BTBT model is included in the simulation, the OFF-state currents at V_d = -1.0 V was increased approximately four order of magnitude compared with the OFF-state currents at V_d = -0.05 V. The GIDL effect strongly emerges as the gate voltage is positively biased at a high drain voltage, V_d = -1.0V. With a large drain-to-gate bias, enough energy band bending occurs for valence band electrons to tunnel into the conduction band, which is the origin of GIDL. In the simulation, the tunneling current is only generated by direct BTBT of carriers and the trap-assisted tunneling current can be ignored since no trap distribution is assumed. High OFF-current level in the simulation is consistent with the experimental results. The direct BTBT of carriers facilitated by Ge's low bandgap is a main reason for high OFF-state leakage currents as demonstrated in the simulation. In conclusion, the GIDL effects clearly increase I_{OFF} but it does not degrade the *SS* and the DIBL of the device.

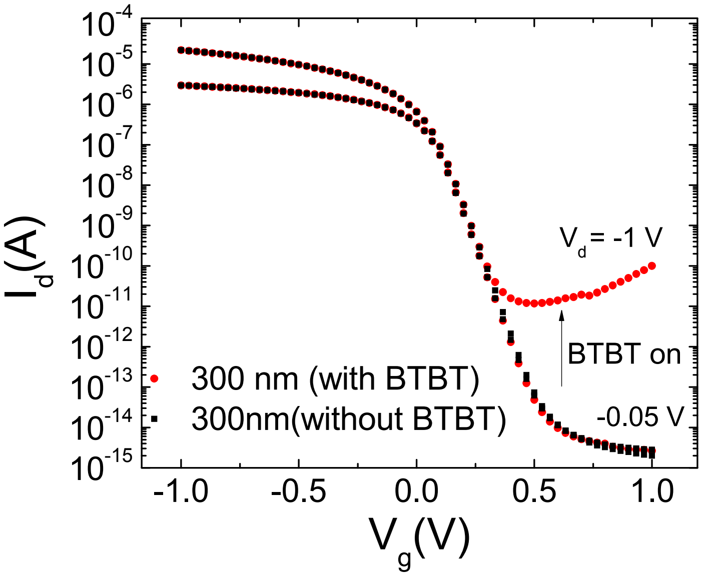


Figure 3-16: The I_d-V_g characteristics of Ge-Si_xGe_{1-x} core-shell NWFET with L_g = 300 nm. Black (■): transfer characteristics without band-to-band tunneling (BTBT) model, Red (●): transfer characteristics including BTBT model in the simulation).

Next, the transfer characteristics of the device were investigated at different gate lengths (L_g). To examine the gate length scaling effects, device structures and device physics in the simulation were kept in the same conditions and the gate length is only varied. In addition, the traps were ignored in the simulation. For gate lengths above 300 nm, DIBL and *SS* values are not changed even if the ON-current proportionally deceases with the gate length increase. Thus, we focus here on devices with L_g below 300 nm. Figure 3-17 show the transfer characteristics (I_d-V_g) of the Ge-SiGe core-shell NW FETs, calculated at different V_d = -0.05 V and -1.0 V for L_g = 300, 250, and 200 nm. As the gate length scales down, the DIBL is clearly observed at 200 nm, where it is increased from 6 mV/V to 76 mV/V. Below the gate length 200 nm, the channel potential modulation is obviously affected by the drain biases, where the drain current is controlled not only by the gate voltage, but also by the drain voltage. Thus, a potential barrier between the source and the channel is further decreased at high $V_d = -1.0$, leading to an increased drain current. Simulation results show the similar trend compared to the experimental results where DIBL starts to increase from the channel length below 300 nm. The increasing DIBL in the device causes the increase of *SS* from 62 mV/dec to 76 mV/dec as well. In conclusion, as the gate length scales down, it causes DIBL, which in turn degrades the *SS* of the device.

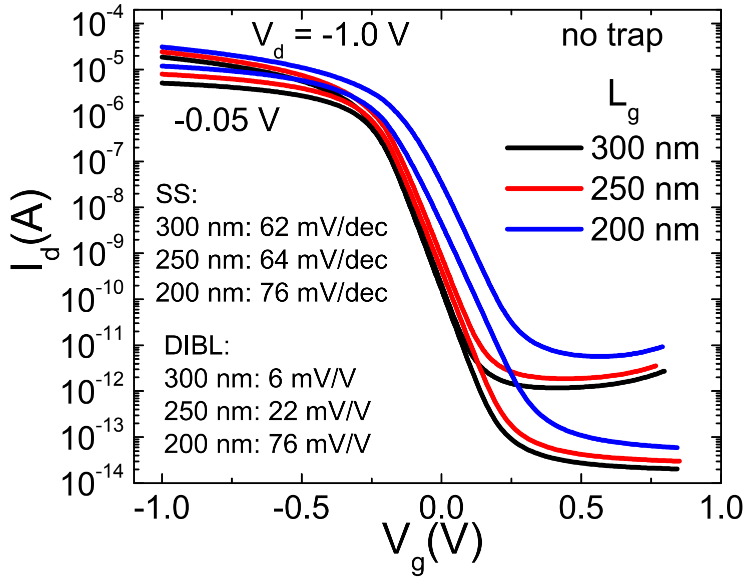


Figure 3-17: The I_d-V_g characteristics of Ge-Si_xGe_{1-x} core-shell NWFETs for different gate lengths from 300 nm to 200 nm.

Lastly, the impact of interface traps on the device performance was investigated. To examine the impact of interface traps on the device performance, the same device structure as shown in Fig. 3-15 and device physics which include BTBT model were employed in the simulations, while the interface trap density (D_{it}) and the gate lengths were varied. In the simulation, the uniform D_{it} was assumed over the bandgap and four different D_{it} values, 0, 10^{12}, 5×10^{12}, and 10^{13} $cm^{-2}V^{-1}$, were used to demonstrate their impact on the device performance. Figure 3-18 shows the transfer characteristics of the NW FET with L_g = 300 nm for different interface trap densities. The obvious observation from Fig.3-18 is that the *SS* and DIBL of the NW FETs are clearly affected by the increase of D_{it}. For example, the *SS* value is close to 60 mV/dec and DIBL is negligible at D_{it} = 0, whereas *SS* and DIBL are greatly increased as D_{it} approaches to 10^{13} $cm^{-2}V^{-1}$. The data in Figure 3-19 summarize the simulated (a) DIBL and (b) *SS* as a function of the gate lengths for different D_{it} values, plotted along with the experimental data of Ge-Si_xGe_{1-x} core-shell NW FETs shown in Fig 3-12 and Fig. 3-13. It shows that both *SS* and DIBL are moved to the higher level with the increase of D_{it} value, which are further degraded with the gate length scaling. The results clearly demonstrate that high D_{it} value is the main cause for relatively high *SS* values and DIBL observed in Chapter 3.3.4. The interface trap in MOSFETs works as a series capacitance with a gate capacitance, it prevents an efficient electrostatic control over the channel, and thereby short-channel effects can be more easily observed with the gate length scaling. Therefore, interface density of states should be minimized as possible in order to improve the performance of the devices and extend the device scaling.

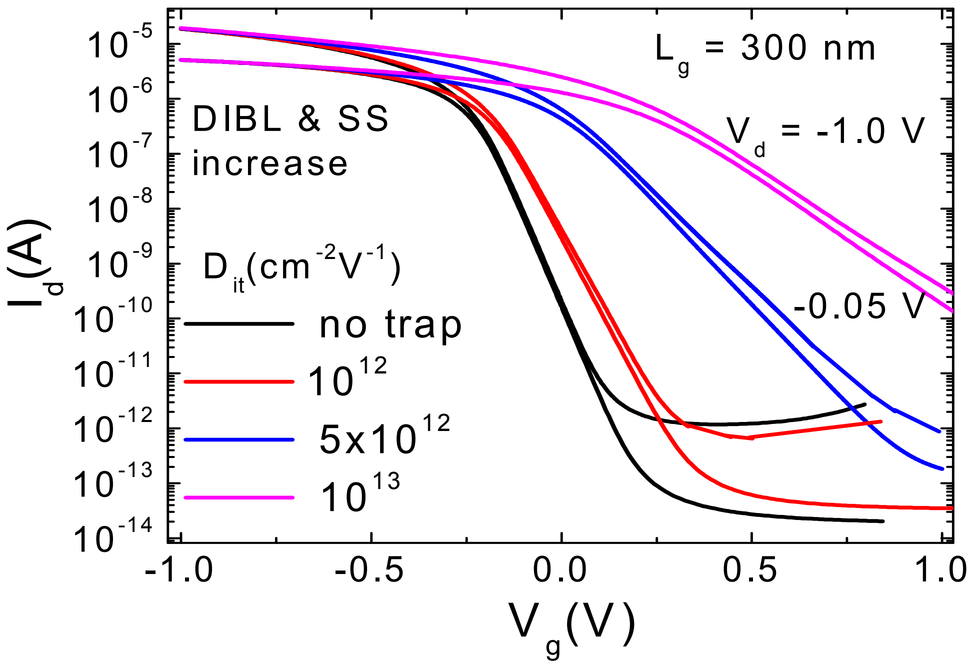


Figure 3-18: Impact of density of interface trap (D_{it}) on the performance of Ge-Si_xGe_{1-x} core-shell NWFETs with the gate length of 300 nm.

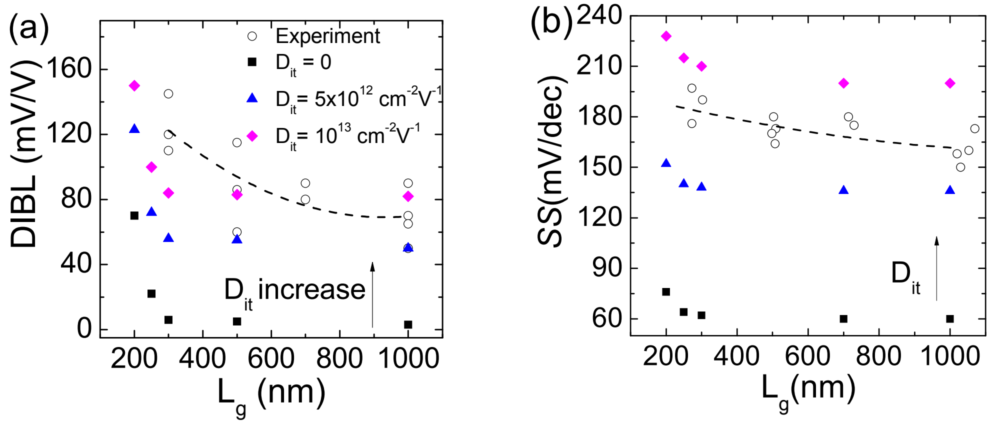


Figure 3-19: (a) DIBL *vs*. gate length for different interface trap level (D_{it}) (b) Subthreshold swing (*SS*) *vs*. gate length for different D_{it}.

3.4 PERFORMANCE DEPENDENCE ON SIGE SHELL CONTENTS

One of the main roles of Si_xGe_{1-x} shell in our NWs is to enhance the channel mobility in the NW FETs by confining the holes in the Ge core. Due to the valence band offset existing between the Ge core and the Si_xGe_{1-x} shell in the NWs, determined by the relative content of Si and Ge in the shell, hole confinement is expected in the Ge core. Thereby, the channel mobility can be improved by reduced the scattering from the impurities and surface roughness on a NW surface. In order to demonstrate the device performance dependence on the Si_xGe_{1-x} shell compositions, the NW FETs were fabricated using the Ge-Si_xGe_{1-x} core-shell NWs with different shell compositions, x = 0.5 and 0.7, having the same Si_xGe_{1-x} shell thickness, 3 nm. The valence band offset between the Ge core and Si_xGe_{1-x} shell is 0.15 eV for x =0.5 and 0.29 eV for x =0.7, determined by Sentaurus TCAD simulation. The valence band offset of the Ge-$Si_{0.7}Ge_{0.3}$ core-shell NW is a twofold higher than that of the Ge-$Si_{0.5}Ge_{0.5}$ core-shell NW and thereby higher hole confinement is expected in the Ge core. Using these NWs, two NW FETs were fabricated by employing the same process described in Chapter 3.1. To minimize the fabrication process dependent device performance variation, two devices were fabricated in parallel.

To investigate the devices characteristics, the output characteristics (I_d-V_d) and transfer characteristics (I_d-V_g) were measured at different temperatures from 300 K to 77 K. Figure 3-20 (a) and (b) show the electrical characteristics of a Ge-$Si_{0.5}Ge_{0.5}$ core-shell NW FET with L_g = 1550 nm and d = 45 nm, whereas Figure 3-20 (c) and (d) show those of a Ge-$Si_{0.7}Ge_{0.3}$ core-shell NW FET with L_g = 1550 nm and d = 37 nm. Figure 3-20 (a) and (c) present the temperature dependent I_d-V_d characteristics of each device and the drain current data normalized to the NW diameter (d) are shown on the right axis of the I_d-V_d graphs to facilitate a comparison of the device characteristics. Figure 3-20 (b) and

(d) show the temperature dependent I_d-V_g characteristics measured at V_d = -0.05 and -1.0 V. Using these electrical characteristics, the device performances at different temperatures are analyzed in details.

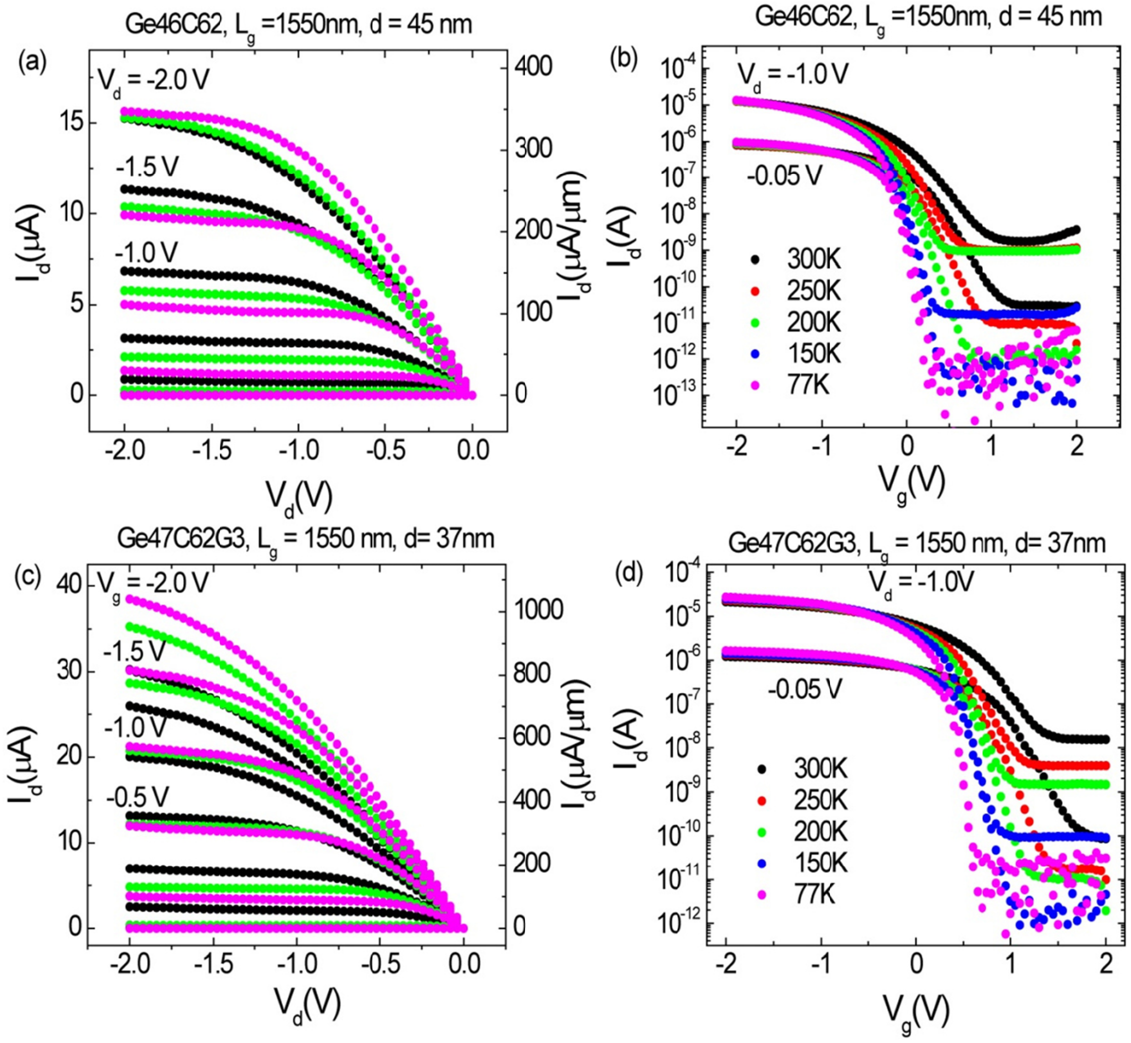


Figure 3-20: Electrical characteristics of Ge-Si$_x$Ge$_{1-x}$ core-shell NW FETs with different shell compositions measured for different temperature from 300K to 77K. (a),(b) I_d-V_d and I_d-V_g characteristics L_g = 1550 nm, d = 45 nm, and Si$_{0.5}$Ge$_{0.5}$ shell (c),(d) I_d-V_d and I_d-V_g characteristics L_g = 1550 nm, d = 37 nm, and Si$_{0.7}$Ge$_{0.3}$ shell. The right y-axis on I_d-V_d graph show I_d normalized to the NW diameter.

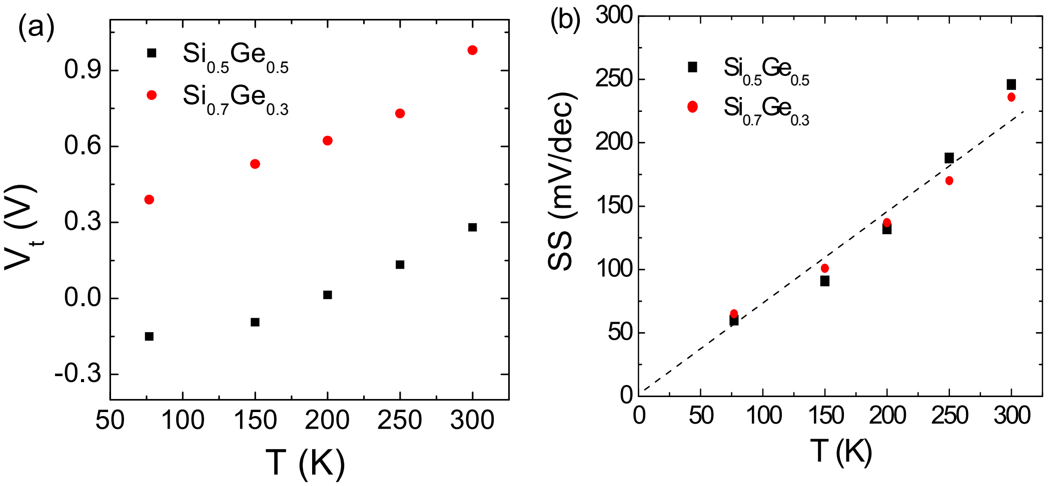


Figure 3-21: (a) Threshold voltage *vs.* temperature (*T*) (●) (b) Subthreshold swing (*SS*) *vs*. *T*. [Ge-Si$_{0.5}$Ge$_{0.5}$ core-shell NW FET (■), Ge-Si$_{0.7}$Ge$_{0.3}$ NW FET]

Figure 3-21 shows the threshold voltage (V_t) and subthreshold swing (*SS*) as a function of temperature for both NW FETs with Si$_{0.5}$Ge$_{0.5}$ shell and Si$_{0.7}$Ge$_{0.3}$ shell. The V_t of the NW FET at each temperature was defined by linearly extrapolating I_d versus V_g, measured at V_d = -0.05, to zero I_d. The V_t of Si$_{0.7}$Ge$_{0.3}$ shell device is 0.98 V at 300 K, which is higher than that of Si$_{0.5}$Ge$_{0.5}$ shell device, V_t = 0.29 V. As *T* is lowered from 300 K to 77 K, the V_t of the device is shifted to 0.4 V (Si$_{0.7}$Ge$_{0.3}$ shell) and -0.32 V (Si$_{0.5}$Ge$_{0.5}$ shell) [Fig. 3-21(a)]. The *SS* values of the NW FETs at 300 K are 246 mV/dec (Si$_{0.5}$Ge$_{0.5}$ shell) and 236 mV/dec (Si$_{0.7}$Ge$_{0.3}$ shell), and they decrease linearly with *T*. Similar *SS* values were observed in both devices over the temperature range that the devices were characterized. The relatively high *SS* values in both devices by comparison to the data shown in Fig. 3-12 can be attributed to the inferior the gate oxide quality along with high interface trap density on the NW surface. Using $SS = 2.3\cdot(kT/\mathrm{q})\cdot(1+eD_{it}/C_{ox})$, where C_{ox} is calculated with Sentaurus simulation, D_{it} values of each device were estimated. The estimated D_{it} value of the Ge-$Si_{0.5}Ge_{0.5}$ core-shell NW FET is ~1.3×10^{13} $V^{-1}cm^{-2}$ and that of Ge-$Si_{0.7}Ge_{0.3}$ core-shell NW FET is ~1.2×10^{13} $V^{-1}cm^{-2}$. Similar D_{it} values of both devices indicate that both NWs have a similar interface quality for the gate oxide deposition. Thus, the impact of D_{it} on device performance, as demonstrated in Chapter 3.3.5, may also be similar in both NW FETs.

In Figure 3-22, the I_{ON} and I_{OFF} current of the NW FETs are plotted for different temperatures. The I_d on y-axis is normalized to the NW's diameters. Using I_d-V_g graph shown in Figure 3-20, we define the I_{ON} as the measured I_d at a gate bias $V_{ON} = V_t + (2/3)V_{cc}$ and the I_{OFF} as the measured I_d at $V_{OFF} = V_t - (1/3)V_{cc}$ for V_{cc} = -2.0 V; the drain bias in both cases is V_d = -1.0 V. The ON-current of the Ge-$Si_{0.7}Ge_{0.3}$ core-shell NW FET is 270 μA/μm at 300K which is approximately two times higher than that of Ge-$Si_{0.5}Ge_{0.5}$ core-shell NW FET, 154 μA/μm. As temperature is decreased from 300 K to 77K, I_{ON} increases by 80 % (482 μA/μm) and 34 % (207 μA/μm), respectively for the NW FET with $Si_{0.7}Ge_{0.3}$ shell and $Si_{0.5}Ge_{0.5}$ shell. On the other hand, OFF-currents of both devices show more obvious temperature dependence, demonstrating about three orders of magnitude lower I_{OFF} at 77 K by comparison to I_{OFF} at 300 K. The I_{OFF} values of the NW FETs with $Si_{0.7}Ge_{0.3}$ shell are higher than those with $Si_{0.5}Ge_{0.5}$ shell over all the temperatures. Figure 3-23 shows ON-OFF current ratio of both devices from 300K to 77K. The results show that the ON-OFF current ratio increases as temperature is lowered from 300 K to 77 K, mainly due to I_{OFF} reduction at low temperature. The higher ON-OFF current ratio of the NW FET with $Si_{0.5}Ge_{0.5}$ shell by comparison to that with $Si_{0.7}Ge_{0.3}$ shell is resulted from its lower I_{OFF} value.

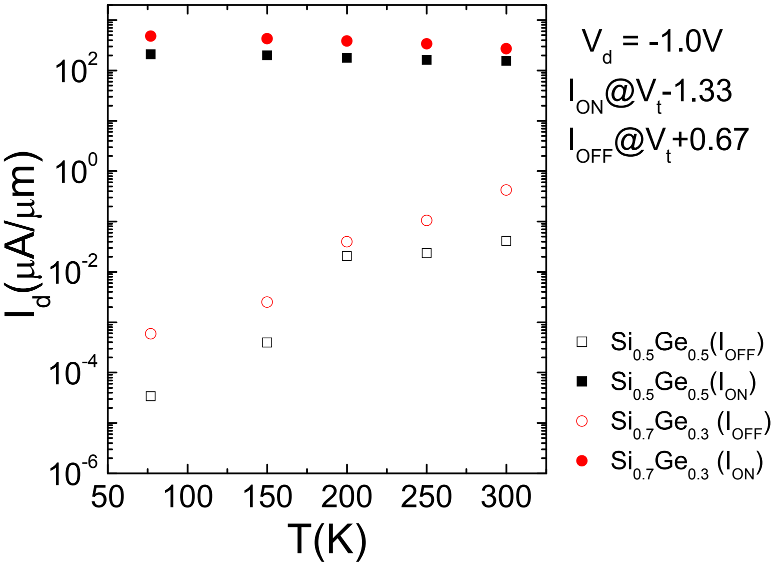


Figure 3-22: I_{ON} & I_{OFF} *vs*. Temperature (T). The I_d is normalized to the diameter (*d*) of the NWs. The I_{ON} values of the NW FET with $Si_{0.7}Ge_{0.3}$ shell are approximately two times higher than that of the NW FET with $Si_{0.5}Ge_{0.5}$ shell. The I_{OFF} values are also higher for the NW FET with $Si_{0.7}Ge_{0.3}$ shell.

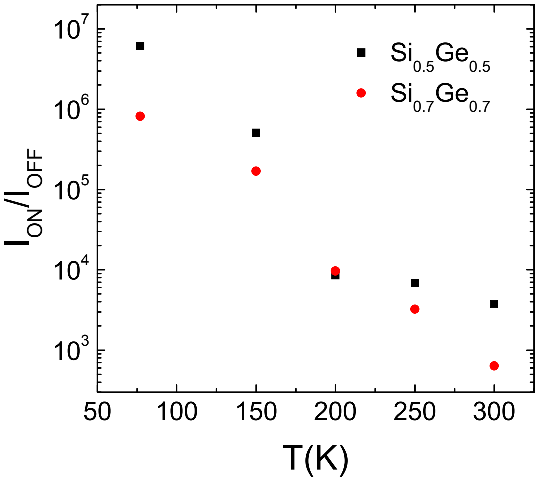


Figure 3-23: ON-OFF current ratio *vs.* temperature (T). The NW FET with $Si_{0.5}Ge_{0.5}$ shell shows higher ON-OFF current ratio.

To better understand OFF-current generation mechanism, Arrhenius plots of I_{OFF} are presented in Fig. 3-24 for (a) the linear region (V_d = -50 mV) and the (b) saturation (V_d = -1.0V). In the linear region (V_d = -50mV) shown in Fig. 3-24(a), the activation energies (E_A) of the devices are ~0.17 eV for $Si_{0.5}Ge_{0.5}$ shell and ~0.1 eV for $Si_{0.7}Ge_{0.3}$ shell. Again, the activation energy at higher drain bias (V_d = -1.0 V) is ~0.12 eV for the NW FET with $Si_{0.5}Ge_{0.5}$ shell and ~0.11 eV for the device with $Si_{0.7}Ge_{0.3}$ shell. Such activation energies, which are lower than a half of the Ge's bandgap, indicate that the OFF currents in both NW FETs are attributed to trap-assisted tunneling (TAT) or band-to-band tunneling (BTBT) [84]. In the Ge-$Si_{0.5}Ge_{0.5}$ core-shell NW FET, the E_A is reduced from 0.17 at V_d = -50 mV to 0.12 at V_d = -1.0 V as BTBT is being more dominant at high V_d. Interestingly, in the Ge-$Si_{0.7}Ge_{0.3}$ core-shell NW FET, the E_A values at both V_d do not show much difference.

A main finding is summarized in Figure 3-25, where the peak effective mobilities (μ_{eff}) of both devices are plotted as a function of temperature (T). Using Table 2.2, the external resistance (R_{SD}) is first subtracted from the total resistance (R_m) to obtain the channel resistance (R_{ch}) by the relation, $R_{ch} = R_m - R_{SD}$. The R_{SD} of the Ge-$Si_{0.5}Ge_{0.5}$ core-shell NW FET is ~11 kΩ, having an *ungated* channel length (L_s) of 560 nm, while that of Ge-$Si_{0.7}Ge_{0.3}$ core-shell NW FET is ~16 kΩ with L_s = 640 nm. Then, using the equation 3.1, the effective mobilities of the devices are calculated at each temperature. The μ_{eff} of the Ge-$Si_{0.7}Ge_{0.3}$ core-shell NW FET is ~280 $cm^2/V \cdot s$ at 300 K, which is a twofold higher current than that of the Ge-$Si_{0.5}Ge_{0.5}$ core-shell NW FET, 140 $cm^2/V \cdot s$. With reducing temperature to 77 K, the mobility goes up to 217 and 610 $cm^2/V \cdot s$, respectively for the NW FET with $Si_{0.5}Ge_{0.5}$ shell and $Si_{0.7}Ge_{0.3}$ shell. In the Ge-$Si_{0.5}Ge_{0.5}$ core-shell NW FET, the mobility is saturated at T below 150 K, indicating the impurity scattering limited μ_{eff} at low temperature in the device.

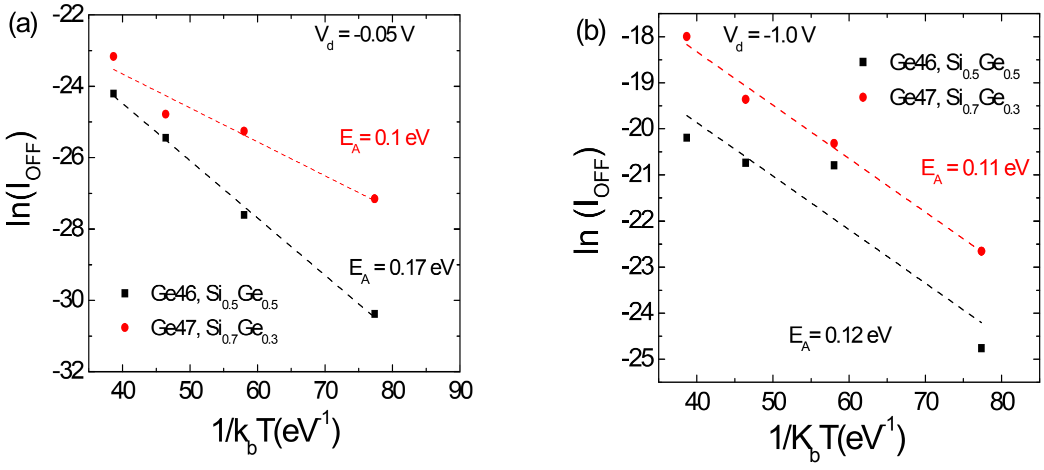


Figure 3-24: Arrhenius plot of I_{OFF} measured from 300K to150K at (a) V_d = -0.05 V and (b) V_d = -1.0 V. Low activation energies of both devices indicate that the I_{OFF} current are attributed to BTBT or TAT of carriers.

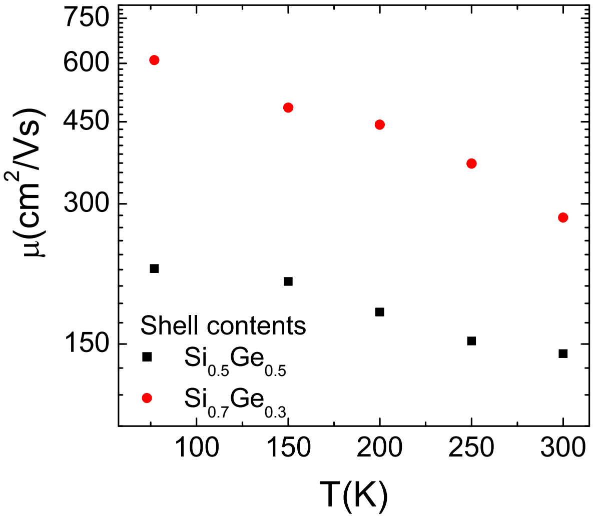


Figure 3-25: Peak mobility versus temperature plot of the NW FETs with $Si_{0.5}Ge_{0.5}$ (■) and $Si_{0.7}Ge_{0.3}$ (●) shell. At 77 K, the NW FET with $Si_{0.7}Ge_{0.3}$ shell demonstrates about three times higher mobility by comparison to the NW FET with $Si_{0.5}Ge_{0.5}$ shell.

On the other hand, the mobility of Ge-$Si_{0.7}Ge_{0.3}$ core-shell NW FET is continuously increased down to T = 77 K. In conclusion, higher mobility was demonstrated in the Ge-$Si_{0.7}Ge_{0.3}$ core-shell NW FET compared with the Ge-$Si_{0.5}Ge_{0.5}$ core-shell NW FET, which is resulted from enhanced hole confinement in the Ge-core thanks to higher band offset (0.29 eV) between the Ge core and the $Si_{0.7}Ge_{0.3}$ shell, leading to reduced scattering from the oxide-SiGe shell interface.

3.5 SUMMARY

In this chapter, the fabrication process of Ge-Si_xGe_{1-x} core-shell NW FETs with highly doped source and drain was demonstrated by employing a conventional CMOS process, where the highly doped S/D were realized by low energy boron ion implantation. The performances of these devices, namely ON-current and ON/OFF ratio, were improved by comparison to *undoped* S/D NW FETs, showing two orders of magnitude higher drive currents and a ten-fold increase in ON/OFF ratio. To substantiate the characteristics of high performance Ge-Si_xGe_{1-x} core-shell NW FETs, scaling properties of the devices were systematically investigated using the NW FETs with different channel lengths, which allowed to extract key device parameters, such as intrinsic channel resistance, carrier mobility, effective channel lengths, and external contact resistance, as well as to benchmark the device switching speed and ON/OFF current ratio. The results show that the mobilities of these devices are a three-fold higher than Si MOSFETs with high-κ dielectrics, and ON/OFF characteristics are comparable to or excelling the most recent planar Ge MOSFETs. TCAD simulation was also employed to better understand the performance degradation factors in the devices, indicating that high interface trap density in the devices is responsible for the performance degradation.

Lastly, the enhanced mobility due to hole confinement was demonstrated by engineering Si_xGe_{1-x} *shell* composition.

CHAPTER 4

Germanium Nanowire Tunneling Field-effect Transistors

In Chapter 3, the high performance Ge-Si_xGe_{1-x} core-shell NW FETs with highly doped source/drain were fabricated and their scaling properties were systematically investigated, which demonstrated higher hole mobility by comparison to a planar Si MOSFETs with a HfO_2 gate dielectric. By employing high mobility channel materials for MOSFETs, the scaling of devices may be further extended, but eventually it be stymied by the increase in dissipated passive power with reducing the device dimensions, which stems from short-channel effects. Therefore, the need for novel devices, which can potentially provide a reduced dissipated power at switching speeds comparable to Si MOS devices looms increasingly large. As discussed in the Chapter 1, TFETs consists of gated *p-i-n* structure and the carrier injection from the source to the channel relies on band-to-band tunneling (BTBT) at the reversed-biased source-channel junction. Since it relies on BTBT rather than the thermal broadening of Fermi distribution, subthreshold swing below 60 mV/dec can be potentially realized at room temperature [48-50]. To date, subthreshold swing below 60 mV/dec have been observed in TFETs using Si as the host semiconductor. However, the ON-currents in these devices are still very low to be applied for digital logic applications, which is mainly due to relatively high bandgap of Si. In this aspect, Ge-Si_xGe_{1-x} core-shell NWs can provide two potential advantages. First, the lower band-gap of Ge (0.67 eV) compared with Si (1.12 eV) allows for higher tunneling currents, by comparison to Si-based TFETs. Secondly, the Ω-shape gate geometry used here provides an enhanced electrostatic control of the channel by comparison to a planar device geometry, which in turn increases the BTBT current.

This chapter begins with a brief description of the fabrication process of NW TFETs. The electrical characteristics of NW TFETs are systematically investigated, including temperature dependent measurement. The role of dopant diffusion and activation is described, and their impact on the device performance is also studied. Finally, the improved device performance using flash-assisted rapid thermal process is reported.

4.1 FABRICATION PROCESS OF GE-SI_XGE_{1-X} CORE-SHELL NW TFETS

The fabrication process of NW TFETs is illustrated in the Figure 4-1(a). The device fabrication process is similar to that of the NW FETs except that the source and drain are implanted with different polarity of dopants. After growth, the NWs are harvested in an ethanol solution, and dispersed on a HfO_2 (10 nm)/Si (*n*-type) substrate. A 5.5 nm – thick HfAlOx top dielectric is deposited by atomic layer deposition (ALD) on the dispersed NW. The equivalent oxide thickness of deposited gate oxide was ~2.4 nm, evinced by capacitance-voltage measurement on planar capacitors processed in parallel with the device. The gate pattern is defined by e-beam lithography (EBL), TaN (tantalum nitride) deposition, and lift-off. The HfAlOx dielectric on *S/D* region is then etched in diluted HF (~ 2%). [Fig. 4-1(c)] In order to realize the source and drain contacts with different polarities, phosphorous and boron were ion implanted at low energy, respectively. In particular, polymethyl-methacrylate (PMMA) positive resist was used as an ion implant mask. [Fig. 4-1(d)] The source of NW TFETs is implanted at normal incidence with phosphorus, at an energy of 6 keV, with a dose of 10^{15} cm^{-2}, while the drain contact is masked with PMMA.

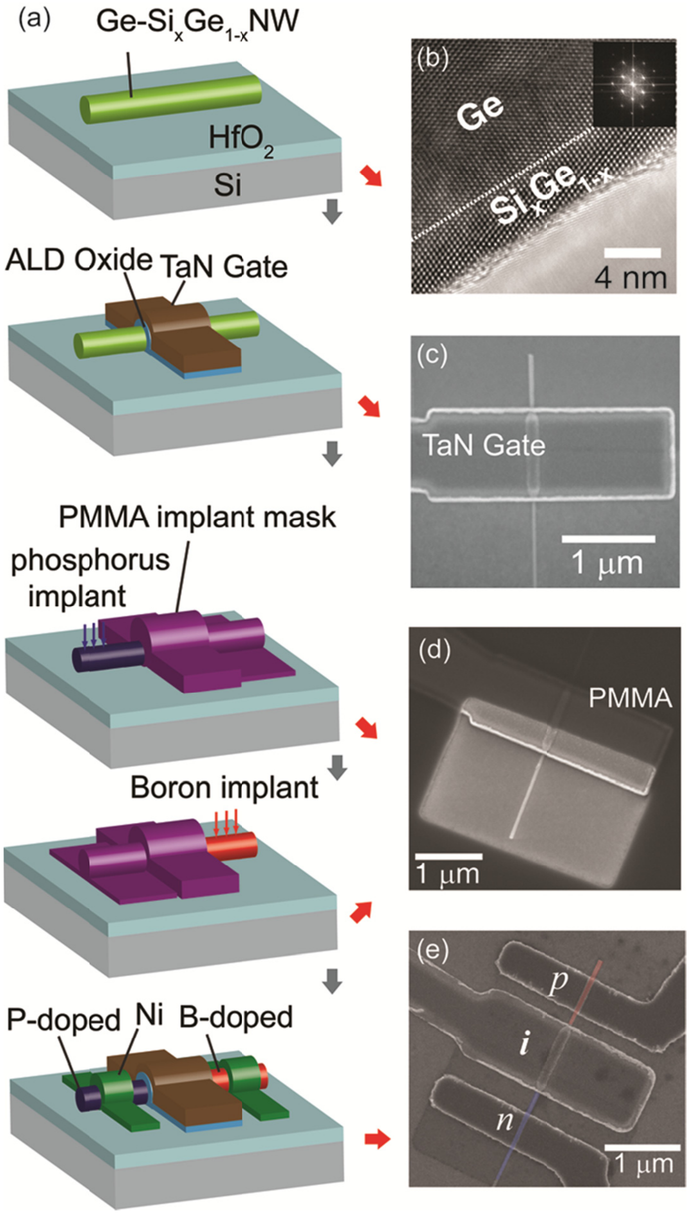


Figure 4-1: Ge-Si$_x$Ge$_{1-x}$ core-shell NW TFET **a.** Schematic representation of the NW TFET fabrication process flow **b.** Transmission electron micrograph of a Ge-Si$_x$Ge$_{1-x}$ core-shell NW, evincing a single crystal shell grown epitaxially on the Ge core **c.** Scanning electron micrograph (SEM) of the gate electrode **d.** SEM of ion-implant window. **e.** SEM showing a NW TFET device. The red (blue) colored region represents the *B*-doped (*P*-doped) NW section. [94]

Next, the NW TFET drain contact is boron-implanted at the energy of 3 keV, at a normal incidence with respect to the substrate, with different doses, 1×10^{14}, 5×10^{14}, and 1×10^{15} cm^{-2}. The dopants were then activated using a 450 °C anneal for 5 min in N_2 ambient, using rapid thermal process (RTP). The ion implant induced NW crystal damage is removed by activation anneal thanks to Ge's fast regrowth and defect removal. Lastly, the *S/D* metal contacts are patterned by EBL, Ni deposition (100 nm), and lift-off. A low temperature (200 °C), 1 min contact anneal finalizes the device fabrication process [Fig. 4-1(e)]. Table I summarizes the NW resistivities and the metal (Ni) to NW contact resistances, determined using four-terminals, back-gate dependent resistivity measurement on NWs uniformly implanted with the same doses, and following a similar activation anneal as the NW TFET devices.

Table 4-1: Ion implanted NW Resistivities and NW-to-Ni contact resistances

Dopant, Dose (cm^{-2})	Resistivity ($\Omega\cdot$cm)	Contact resistance (Ω)	Specific contact resistance ($\Omega\cdot$cm^{-2})
B, 10^{15}	$3.0 \pm 0.4 \times 10^{-3}$	168±14	$4.0 \pm 1.3 \times 10^{-10}$
B, 5×10^{14}	$5.4 \pm 0.8 \times 10^{-3}$	243±73	$5.2 \pm 2.4 \times 10^{-10}$
B, 10^{14}	$35 \pm 6.5 \times 10^{-3}$	3400±2900	$2.3 \pm 2.0 \times 10^{-8}$
P, 10^{15}	$6.3 \pm 2.2 \times 10^{-3}$	1050±760	$9.7 \pm 9.5 \times 10^{-9}$

4.2 ELECTRICAL CHARACTERISTICS OFGE-$\mathrm{SI_XGE_{1-X}}$ CORE-SHELL NW TFETS

4.2.1 Principle of NW TFET operation

The fabricated Ge-Si_xGe_{1-x} core-shell NW TFETs consist of gated p-i-n structures, e.g., a P-doped source, an *intrinsic* channel, and a B-doped drain. To demonstrate the operation principle of the NW TFETs, the energy band profiles along a nanowire axis for both OFF- and ON-state of the device was generated using TCAD simulation. The channel is made of Ge, having L_g of 150 nm with a diameter of 40 nm. The gate oxide (SiO_2) thickness was 3 nm. In the simulation, the source is doped with a P-doping concentration of 10^{20} cm^{-3}, the channel is an *intrinsic* region, the drain is doped with B-doping concentration of 10^{18}, 10^{19}, and 10^{20} cm^{-3}. In OFF-state (equilibrium condition), the valence band in the channel is below the conduction band of the source, the carriers cannot tunnel from source to the channel, where the *intrinsic* channel region acts as a tunneling barrier [Figure 4-2(top)]. On the other hand, when a gate voltage is negatively biased to V_g = -0.5 V, such that the valence band in the channel is pulled above the conduction band in the source, holes can be injected into the channel via band-to-band tunneling (BTBT) and a tunneling current will start to flow for a given negative drain voltage, V_d = -0.01 V [Figure 4-2(bottom)]. In Figure 4-3 (bottom), low drain V_d = -0.01 V is chosen to highlight the energy band modulation using the gate bias. Here only carriers within ΔΦ window contribute to the tunneling currents. The ON-currents can be increased by thinning the source-channel junction with more negative gate voltages.

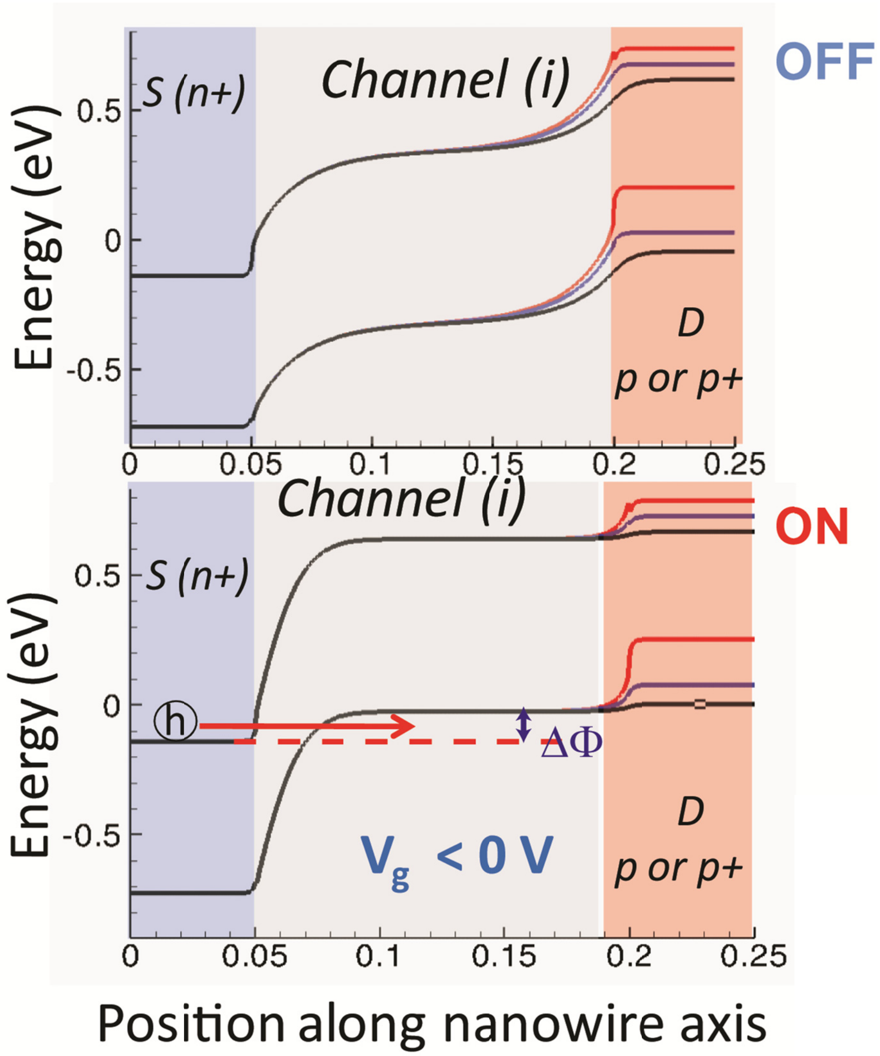


Figure 4-2: Energy band profiles of NW TFET with p-i-n device structure along a NW for OFF-state (top) and ON-state (bottom). The device turns on by BTBT of holes from the source to the channel when the valence band in the channel is pulled above the conduction band of the source with a negative gate bias. Red, blue, and black lines in the drain regions represent B-doping concentration 10^{20}, 10^{19}, and 10^{18} cm^{-3}, respectively.

4.2.2 Diode characteristics

Figure 4-3 shows the gated *p-i-n* diode characteristics of a representative NW TFET, having a diameter d = 36 nm and channel length L_g = 600 nm. The source (n+) and drain (p+) region of this NW TFET were ion-implanted with phosphorus and boron at a dose 10^{15} cm^{-2}, respectively. Figure 4-3 shows I_d vs. V_d data measured from -2.0 V to 2.0 V at constant V_g values, from 0 to -3.0 V. In forward bias (V_d > 0V), where the drain (p+) is positively biased at different V_g from 0 V to -3.0 V, our device works as a typical gated *p-i-n* diode. The maximum current in forward bias region is ~20 μA, corresponding ~550 μA/μm (normalized to the NW's diameter), and show little dependence on V_g. This high drive current confirms that dopants in *S/D* regions of NW FETs are well activated, and low *S/D* contact resistances are achieved.

Using the data of Table I, the estimated external source and drain resistance is ~20 kΩ in this device. The data in the forward bias region can be fitted with a diode equation, $I = I_o[\exp(\frac{qV_d}{nkT}) - 1]$, where I_o is the reverse bias saturation current, q is the electron charge, n is the ideality factor, k is Boltzmann constant, and T is temperature. The ideality factor of this diode is approximately ~ 1.8, indicating that recombination in the channel dominates the diode forward current. In the reverse bias region (V_d < 0) the current is controlled by carrier BTBT at the source-channel junction. The increase of I_d with V_g in reverse bias region is consistent with BTBT through a tunneling barrier that is thinned at an increased V_g. The device characteristics in the tunneling regime were further investigated using the NW TFET of Figure 4-3.

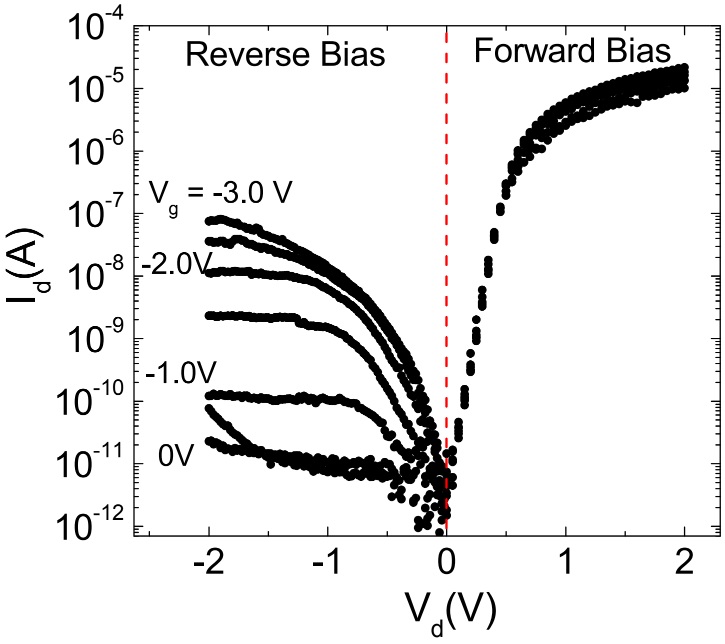


Figure 4-3: Diode characteristics of a Ge-Si_xGe_{1-x} core-shell NW TFET: The I_d -V_d characteristics of a NW TFET, with L_g = 600 nm, and d = 36 nm, on a log-lin scale. The phosphorous and boron implant doses are (P : 10^{15}cm^{-2}, B : 10^{15} cm^{-2}). Recombination dominates the current in forward bias, while BTBT dominates the current in reverse bias. [94]

4.2.3 Output and transfer characteristics

The NW TFET used for the diode characterization in Chapter 4.2.2 is further investigated as a field-effect transistor. Figure 4-4(a) shows I_d vs. V_g at different V_d values, and Fig. 4-4(b) shows I_d vs. V_d at different V_g values. In Figure 4-4(a), V_g was swept from -3.5 V to 1.0 V at constant V_d = -1.0, -1.5, and -2.0 V. Figure 4-4(a) data show a maximum attainable I_d of ~ 5 μA/μm (normalized to the NW diameter), a value comparable or higher to that of Si-based TFETs [52-54]. Figure 4-4(a) data also reveals ambipolar behavior, a finding explained by the high doping level of the *S* and *D* which are implanted with a 10^{15} cm^{-2} dose. The drain current at negative (positive) V_g stems from BTBT at the source (drain) - channel junction. The subthreshold slope of this device is 370 mV/dec for all V_d values. The relatively high *SS* value is attributed to interface traps, as well as a graded doping profile at the source-channel tunneling junction, induced by lateral straggle of dopants during ion implantation and diffusion during the dopant activation anneal. Figure 4-4(b) shows the output characteristics of this device. The I_d vs. V_d data shows saturation, similar to MOSFETs, with a V_g dependent saturation current. The saturation voltage has a linear dependence on V_g for a gate overdrive larger than 1.0V. However, I_d shows an exponential increase at small V_d until it reaches the saturation [Fig. 4-4(b)], a behavior attributed to the gate induced barrier thinning at the non-abrupt source-channel junction. While the data of Fig. 4-4(b) probes the NW TFET as a *p*-FET, the output characteristics of the same NW TFET used as an *n*-FET, namely with the boron-doped contact as source, are similar to the data of Fig. 4-4(b).

The electrical characterization of a NW TFET in Fig. 4-4 demonstrates that our device is successfully working as a TFET and it drives comparable or higher current than Si TFETs. However, considering Ge's low bandgap by comparison to Si, the current level is still not very high as theoretically expected one [81]. Low drain current can be induced by either non-abrupt junction profile or non-sufficient dopant activation in the source. Abrupt junction profile enables a sharper energy band profile and high active dopant level in the source make a thinner source-channel profile, which will result in higher BTBT current. The thermal process that we employed for the dopant activation, in particular for P in the source, may not be sufficient for high activation of implanted P dopants and have caused non negligible dopant diffusion, forming a non-abrupt source-channel energy profile [82, 83].

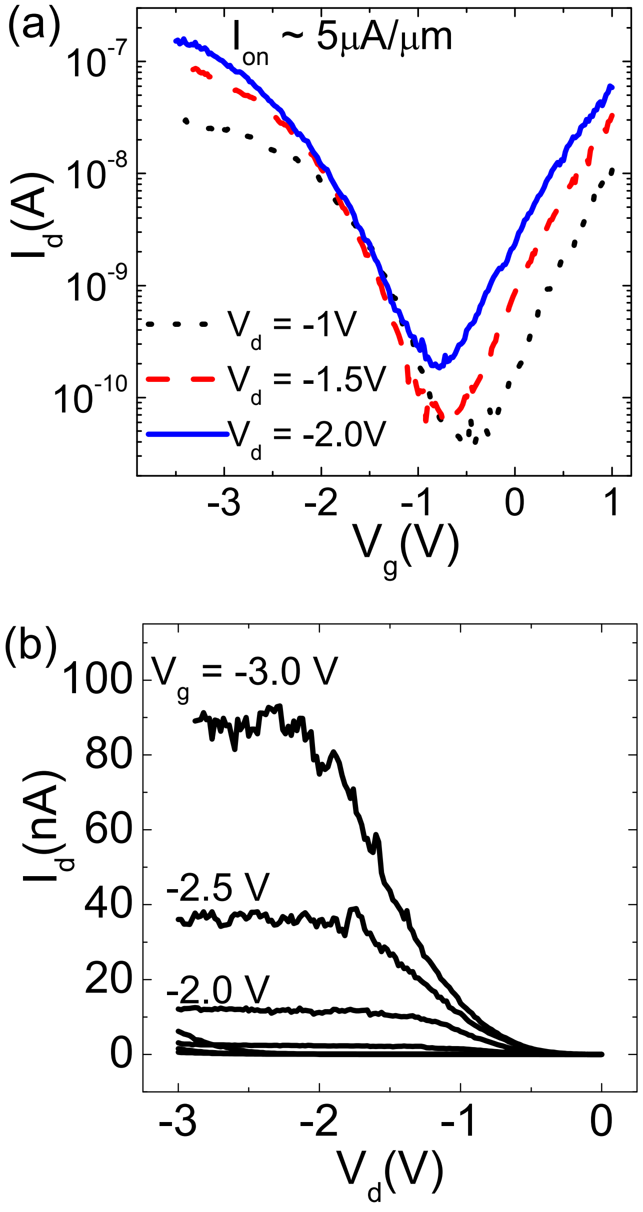


Figure 4-4: Electrical characteristics of a Ge-Si_xGe_{1-x} core-shell NW TFET: (a) Transfer characteristics (I_d - V_g) of a NW TFET with L_g = 600 nm, and d = 36 nm, and (P : 10^{15}cm^{-2}, B : 10^{15} cm^{-2}) implant doses. (b) The output characteristics (I_d - V_d) measured for the same device. [94]

Therefore, the NW TFET performance can be improved, namely higher ON-current and lower *SS* values, by realizing abrupt tunneling junction along with a better gate control.

4.2.4 Suppression of ambipolar behavior

The ambipolar behavior of Figure 4-4(a) data is undesirable for logic gates implementation. To mitigate this issue, NW TFETs with asymmetric source-drain doping concentrations were fabricated and investigated. The NW TFET drain-regions were implanted with boron at an implant energy of 3 keV, with different doses 1×10^{14}, 5×10^{14}, and 1×10^{15} cm^{-2}. The average boron doping concentrations corresponding to these implant doses are 2.2×10^{18}, 1.7×10^{19}, and 5.1×10^{19} cm^{-3}, respectively. The NW TFET source-regions were implanted with phosphorus at an implant energy of 6 keV, with a constant dose of 1×10^{15} cm^{-2}. The devices used in this measurement have similar dimensions, with L_g = 600 nm and d = 39 ± 5 nm. Figure 4-5 (a) shows I_d-V_g characteristics of these NW TFETs measured for different drain voltages, V_d = -1.0 and -2.0 V. The main finding of Figure 4-5(a) data is that the ambipolar behavior can be suppressed by reducing the drain doping concentration. Indeed, the devices with a drain B-implant dose of 10^{14} cm^{-2} show unipolar behavior. At higher B-implant doses, namely 5×10^{14} and 1×10^{15}cm^{-2}, the drain-channel junction becomes sufficiently thin to allow for BTBT, resulting in ambipolar device behavior. We note that NW TFETs with reduced drain doping concentration show subthreshold slopes larger than those with high drain doping. For example, at a drain implant dose of 10^{15} cm^{-2}, the *SS* values range between 350-450 mV/dec, while for a drain implant dose of 10^{14} cm^{-2}, the *SS* values range between 500 – 700 mV/dec. A possible explanation for this observation is the increased source and drain external resistance.

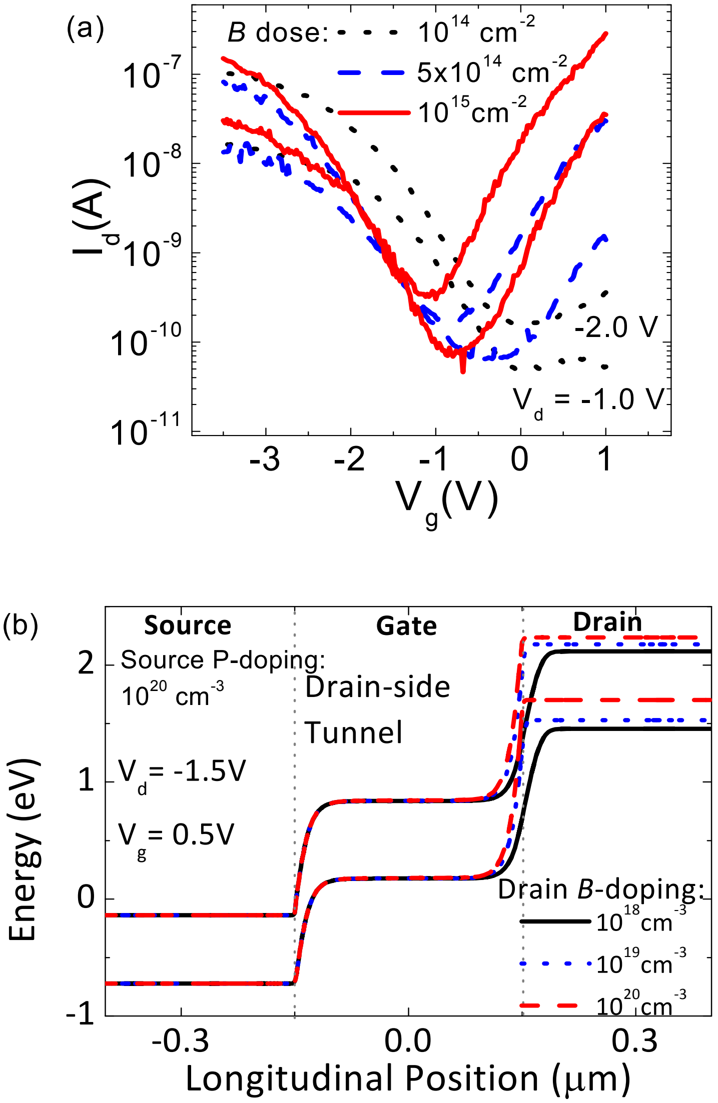


Figure 4-5: (a) $I_d - V_g$ characteristics of Ge-Si_xGe_{1-x} core-shell NW TFETs at different drain implant doses. As the drain *B*-implant dose decreases from 10^{15} to 10^{14} cm^{-2}, the ambipolar behavior is suppressed. The source of these devices is implanted with a phosphorus dose of 10^{15} cm^{-2}. (b) Energy band profiles for different drain concentrations, showing that the drain-channel junction becomes wider as the doping concentration decreases, which in turn prevents BTBT of electrons from the drain. (L_g = 300 nm, d = 40 nm, t_{ox} = 3 nm)

To explain the suppression of electron tunneling on a drain-channel junction in Fig. 4-5(a), TCAD simulation was used to generate the energy band profile for different drain B-doping concentrations [Figure 4-5(b)]. The channel material is Ge with L_g = 300 nm, d = 40 nm, and t_{ox} = 3 nm. The source P-doping concentration is 10^{20} cm^{-3} and the drain B-doping concentration is varied from 10^{18} to 10^{20} cm^{-3}, based on the experimental results. To illustrate the tunneling barrier width on a drain-channel junction, the gate is positively biased at V_g = 0.5 V for V_d = -1.5 V. Figure 4-5(b) shows that decreasing the drain B-doping concentration results in a wider tunneling barrier at the drain-channel junction, which prevents electron tunneling into the channel as experimentally demonstrated in Fig. 4-5(a).

4.2.5 Temperature dependent device characteristics

To substantiate that BTBT is the main carrier injection mechanism in Ge-Si_xGe_{1-x} core-shell NW TFETs, the device characteristics were investigated as a function of temperature [Figure 4-6], and also channel length. Figure 4-6(a) shows the transfer characteristics of a NWTFET with (P: 10^{15} cm^{-2}, B: 10^{15} cm^{-2}) source and drain doping, measured at different temperatures (*T*) from 300 K down to 77 K. These data show that the device characteristics do not change significantly with temperature. Figure 4-6(b) shows the *SS* values measured as a function of *T* for the NW TFET of Fig. 4-6(a) and a *conventional* Ge-Si_xGe_{1-x} NW FET, with highly B-doped *S/D* and similar dimensions (L_g = 600 nm, d = 38 nm). For NW TFETs, the measured *SS* values change little with *T* down to 77 K. As BTBT does not depend on temperature, the insensitivity to temperature of the *SS* values measured in NW TFETs is consistent with the BTBT as the dominant carrier injection mechanism. On the other hand the *SS* value of the NW FET decreases linearly with *T*, a trend that contrasts that of the NW TFETs, but expected for a conventional FET dominated by carrier injection over a potential barrier.

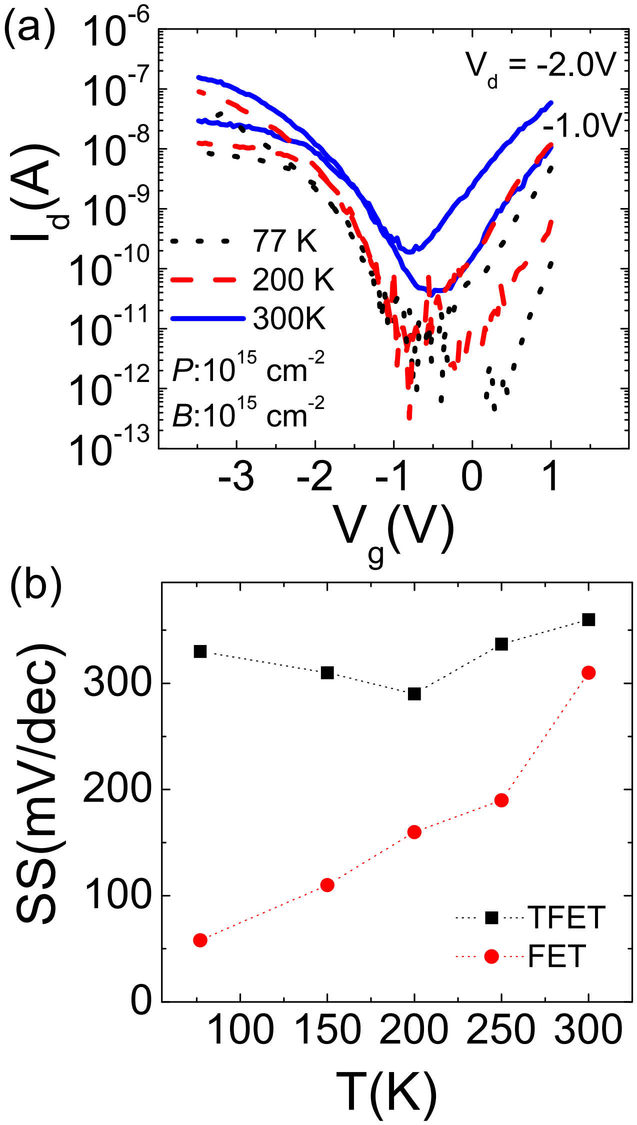


Figure 4-6: Device characteristics measured at different temperatures. a. NW TFET I_d - V_g characteristics measured at different temperatures. b. *SS* vs. *T* for a NW TFET (squares), compared to that of a conventional NW FET (circles).[94]

In addition, it is also noted here that the device characteristics are insensitive to channel length, for L_g values between 580 nm and 1100 nm, a finding which indicates that the carrier injection, not drift, determines the device performance, and is also consistent with BTBT-dominated injection. The linear temperature dependence provides a method to estimate the density of interface traps (D_{it}) in the NW FET devices. Using $SS = 2.3\cdot(kT/q)\cdot(1+eD_{it}/C_{ox})$, where C_{ox} is the gate dielectric capacitance, calculated self-consistently using Sentaurus simulations [Chapter 3.3.2], an interface trap density was extracted as $D_{it} = 1.2\times10^{13}$ cm^{-2}V^{-1}. Since both NW FETs and NW TFETs examined here have similar gate stacks, a similarly large D_{it} is expected in the NW TFET devices. The interface traps have a two-fold impact on the TFET device performance: on one hand they reduce the gate control of the channel as in a conventional FET, and because the band profile in the channel is intimately connected with the BTBT at the source, the large D_{it} also impacts the carrier injection efficiency.

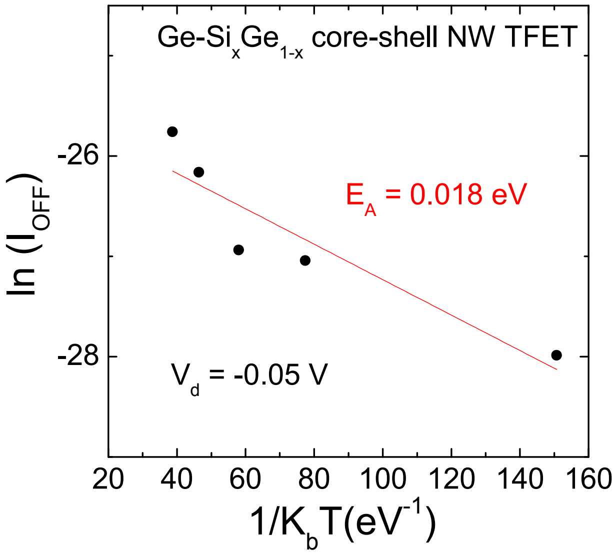


Figure 4-7: Activation energy extracted from the leakage floor of a NW TFET (B:10^{15} cm^{-2} P:10^{15} cm^{-2}) using Arrhenius plot.

Lastly, the activation energy of the NW TFET was extracted, using Arrhenius plot as shown in Figure 4-7. The leakage floors were measured at V_d = -0.05 V for different temperatures. The extracted activation energy is 0.018 eV, which demonstrates that leakage currents in this device are mainly determined by the onset of electron tunneling rather than a trap-assisted tunneling or *p-i-n* diode leakage [84, 85].

4.3 DIFFUSION OF BORON AND PHOSPHORUS IN GERMANIUM

In the Chapter 4.2, the performance of Ge-Si_xGe_{1-x} core-shell NW TFETs was demonstrated. Even if these devices show higher BTBT currents by comparison to Si-based TFETs, however, the ON-currents still remain relatively low by comparison to conventional FETs, consistent with reports in other semiconductors. The performance degradation in Ge-Si_xGe_{1-x} core-shell NW TFETs can possibly be caused by a graded dopant profile at the source-channel junction due to lateral straggle and diffusion of dopants. It prevents to maximize the lateral abruptness of the junction profile and result in low BTBT currents. Thus, the diffusion of boron and phosphorus atoms in Ge should be better understood.

Previously, the as-implanted and post activation profiles of boron and phosphorus atoms in a planar Ge substrate have been reported [82-83, 86-87]. Figure 4-8(a) shows that boron profiles in Ge for different annealing temperatures [86]. It clearly shows that dopant profiles do not change with annealing temperatures, which is consistent with the results shown in Chapter 2.3.4. The direct cause for the slow diffusion of boron atoms in Ge is still unclear, but it has been suggested that ion implantation-induced defects are paired with implanted boron atoms, which have high binding energies and leave the B atoms immobile [86-87]. The report shows that the diffusion of B is negligible up to 850

˚C. On the other hand, implanted-phosphorus profiles in Ge rapidly change with the temperatures as shown in Figure 4-8(b). This fast diffusion of P in Ge is usually explained by the dopant-vacancy-pair model [88, 89]. The reaction of ionized P^+ on substitutional sites with a vacancy with a doubly charge V^{2-} generates negative dopant-vacancy pair $(PV)^-$: $(PV)^- = P^+ + V^{2-}$, where direct diffusion of P^+ is negligible and the dominant diffusion is mediated by $(PV)^-$, enabling the indirect diffusion of P^+. In addition, a diffusion coefficient of P in Ge follows the equation, $D_{eff}(n) = D(n_i)\cdot(n/n_i)^2$. The equation is known as the concentration dependent diffusion equation, where $D_{eff}(n)$ is an effective diffusion coefficient, $D(n_i)$ is a diffusion coefficient at intrinsic carrier concentration, and n is the electrical concentration. Thus, as the impurity concentration increases, the effective diffusion coefficient increases with a quadratic dependence, resulting in fast diffusion of dopants in Ge.

As a result, for a given thermal budget applied for the dopant activation in NW TFETs, the diffusion of B in the drain is negligible, however, that of P in the source could be sufficiently large, resulting in a graded source-channel junction profile which in turn degrades the efficient BTBT from the source to the channel. Therefore, a thermal process providing enough active carriers with a minimal diffusion of P in Ge should be considered.

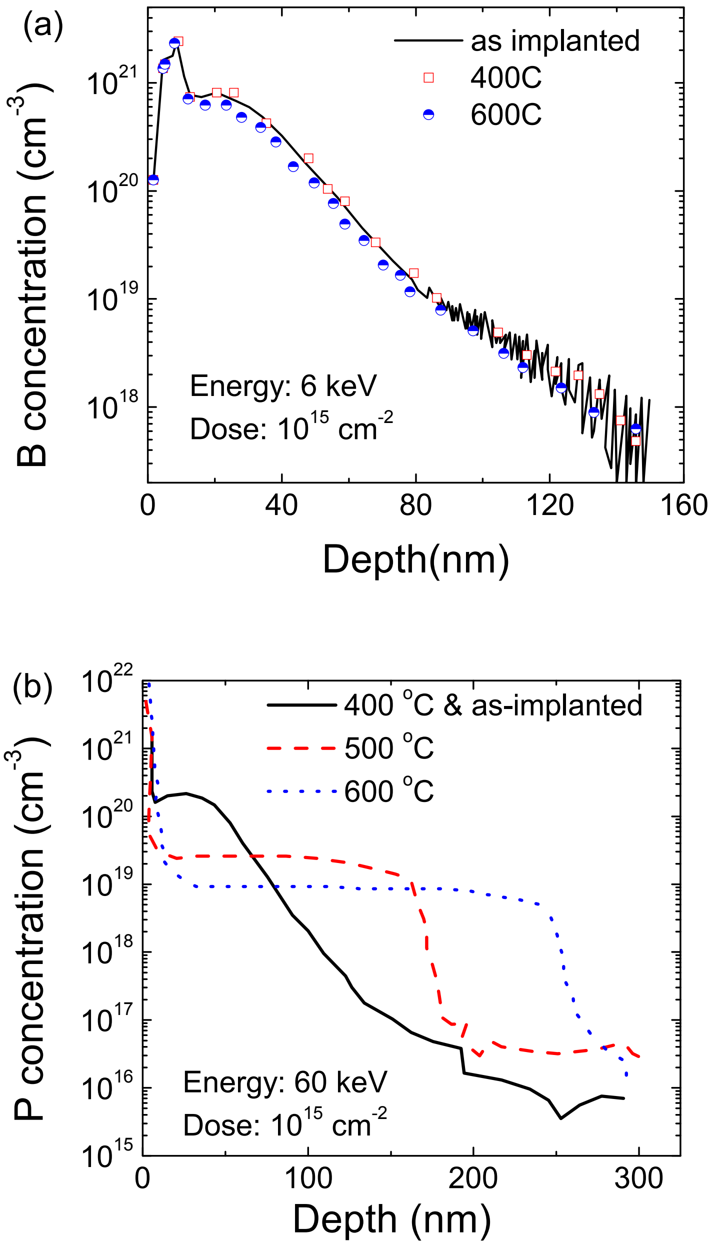


Figure 4-8: Profile of implanted dopants in Ge substrate (a) Profiles of boron implanted at the energy of 6 keV with a dose of 10^{15} cm^{-2}, and annealed at 400˚C and 600˚C for 1 min [86] (b) Profiles of phosphorus implanted at the energy of 60 keV with a dose of 10^{15} cm^{-2}, and annealed at 400, 500, and 600˚C for 30 min [82]. It is noted that as-implanted dopant profile is the same as the one of 400 ˚C

4.4 FLASH-ASSISTED RAPID THERMAL PROCESS

The data in Figure 4-8(b) showed the fast diffusion of P atoms in Ge, demonstrating close temperature dependence. Thus, to minimize diffusions of P during the thermal process, it is important to determine the minimum thermal budget required for the dopant activation and defect removal. By lowering the applied thermal budget, the diffusion of P atoms in Ge can be reduced, but the electrically active dopant level will also be lowered. Therefore, it is desirable to use a thermal process which minimizes the diffusion of implanted dopants while generating high doping concentrations of electrically active donors.

As the scaling of CMOS devices continues, there has been a rise in interest in advanced annealing techniques forming ultra-shallow junctions and realizing very high concentration of electrically active dopants to overcome short-channel effects as well as mobility reductions due to parasitic resistance. Flash-assisted rapid thermal process (fRTP) has been proposed as an alternate technique to realize both diffusionless junctions and high active doping concentration [90, 91] Figure 4-9 is a schematic drawing of the typical flash lamp setup and Figure 4-10 describes the general time-temperature profile of a fRTP. It first heats up to an intermediate temperature (T_i), where the diffusion can be ignored, by using a continuous arc lamp under the wafer to heat the bulk wafer similarly to a conventional RTP. Once it reaches T_i, then an additional power is delivered to the device side of the wafer using a high-energy flash lamp for only few milliseconds. During the flash anneal step, only a thin section of the top-side wafer is heated so that rapid heating or cooling of the devices on a wafer can be achieved by radiation and thermal conduction to the bulk. Therefore, it enables to form diffusionless junction as well as higher dopant activation.

The advantages provided by fRTP can also be useful to improve ON-currents of Ge-Si_xGe_{1-x} core-shell NW TFETs. The fRTP role in NW TFETs is two-fold. First, it maximizes the lateral abruptness of the doping profile by reducing dopant diffusion, which results in a sharper energy band profile between *S/D* and the channel. Second, it helps to increase the electrically active dopant level, resulting in a thinner tunnel barrier at the source-channel-junction.

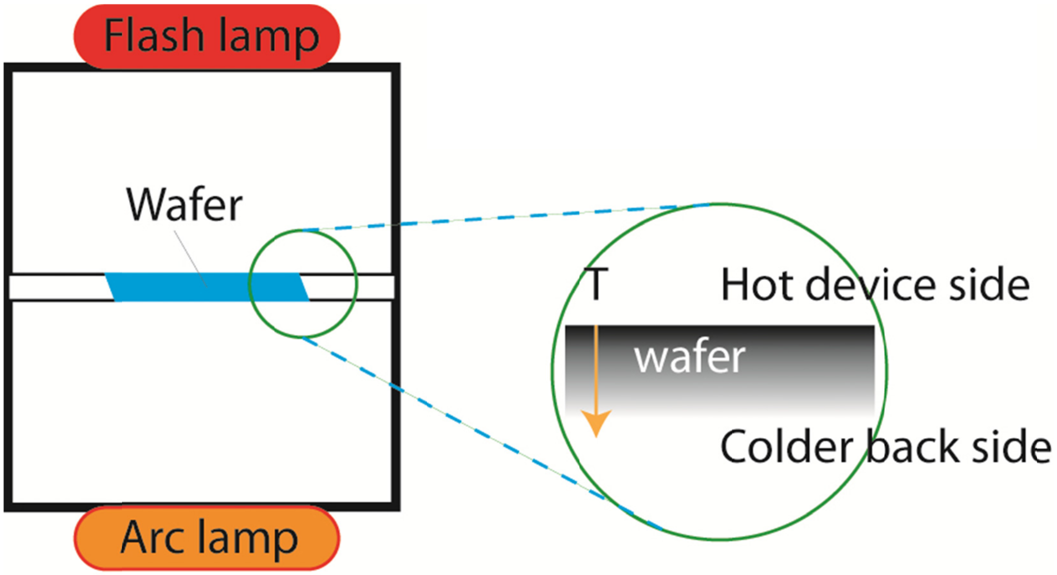


Figure 4-9: Schematic representation of the flash lamp tool. The Arc lamp under the wafer is used for the bulk heating of the wafer and high energy flash lamp is used for the dopant activation [91].

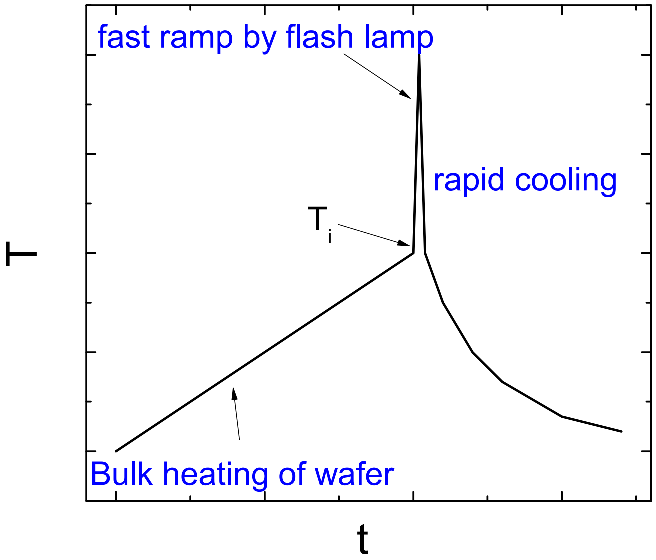


Figure 4-10: Time *vs* temperature profile of an fRTP process, consisting of bulk heating, flash heating, and rapid cooling steps.

4.5 DOPANT ACTIVATION OF P-IMPLANTED NANOWIRES USING FLASH-ASSISTED RAPID THERMAL PROCESS

In Chapter 4.4, the general fRTP process flow and potential advantages using it for the dopant activation in NW TFETs were introduced. To determine the optimum fRTP temperature for dopant activation in Ge-Si_xGe_{1-x} core-shell NW TFETs, the resistivity (ρ) values in phosphorus-implanted NWs were investigated at different activation anneal temperatures, as shown in Figure 4-11. Here, the focus was on the phosphorous (P) activation because of its higher diffusivity, and higher (>500 °C) temperatures required for activation. By comparison, boron activation is insensitive to temperature above 400 °C and its diffusion in Ge is negligible as discussed in Chapter 4.3. The device fabrication process is described in Chapter 2.3.2.

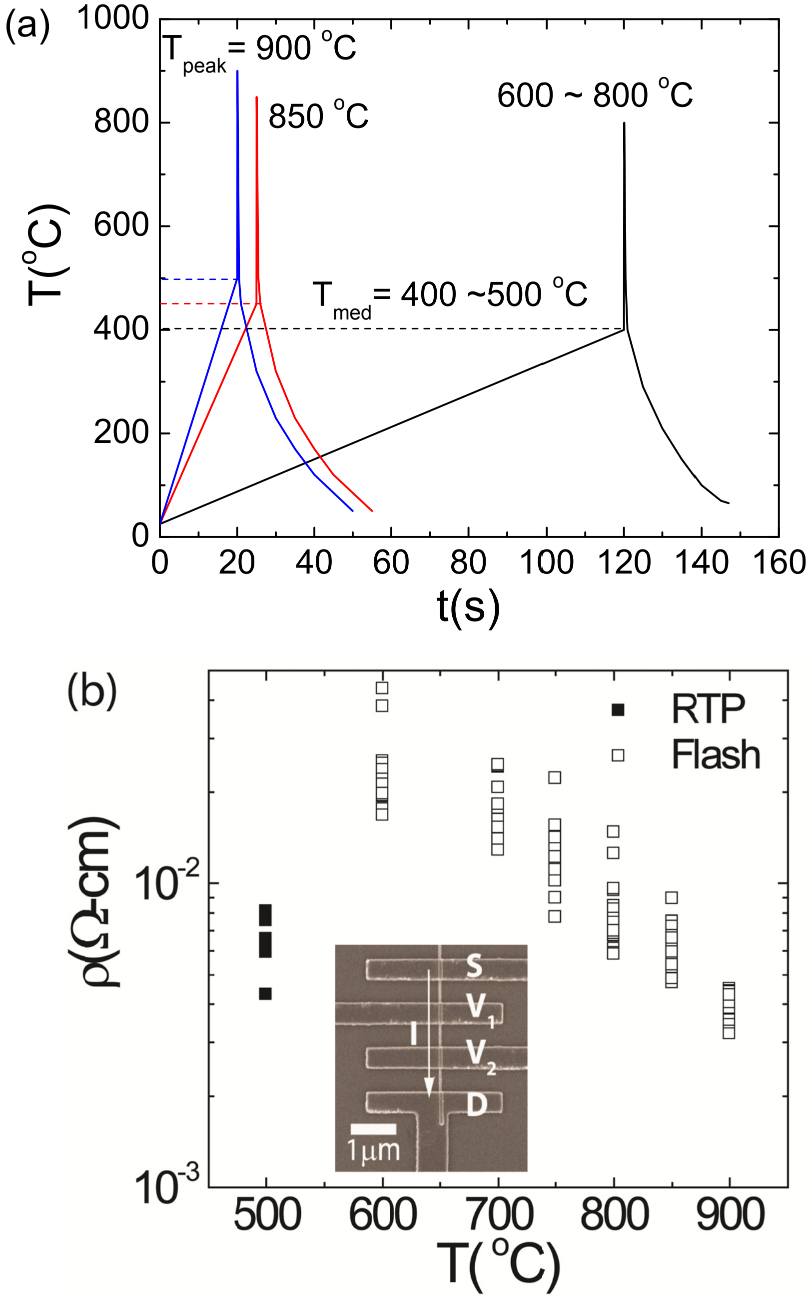


Figure 4-11: (a) Temperature *vs* time profiles used for the activation of the P-implanted NWs. (b) Resistivities (ρ) of phosphorus-doped Ge-Si_xGe_{1-x} core-shell NWs vs the activation temperature (T). The NWs are P-implanted with a dose of 10^{15} cm^{-2} at the energy of 6 keV. (Inset) Scanning electron micrograph of a NW device with multi-terminals. The current (I) flows from S to D, and V_1 and V_2 are used to probe the voltage drop along the NW. [95]

Table 4-2: P-implanted NW resistivities and NW-to-Ni contact resistances

Dopant, Dose (cm^{-2})	Activation Temperature (˚C)	Resistivity (Ω·cm)	Contact resistance (Ω)	Specific contact resistance (Ω·cm^{-2})
P, 10^{15}	RTP, 500 (5 min)	$6.3\pm2.2 \times 10^{-3}$	1050±760	$9.7\pm9.5\times 10^{-9}$
	fRTP, 600	$23\pm7.3 \times 10^{-3}$	2450±890	$7.9\pm6.0\times 10^{-8}$
	fRTP, 700	$17\pm4.0 \times 10^{-3}$	1950±660	$4.2\pm2.0 \times 10^{-8}$
	fRTP, 750	$13\pm4.2 \times 10^{-3}$	3040±1030	$13\pm8.0 \times 10^{-8}$
	fRTP, 800	$7.9\pm2.2 \times 10^{-3}$	300±190	$2.9\pm2.3 \times 10^{-9}$
	fRTP, 850	$6.3\pm1.4 \times 10^{-3}$	260±200	$2.5\pm2.1 \times 10^{-9}$
	fRTP, 900	$3.9\pm0.4 \times 10^{-3}$	520±210	$3.1\pm1.1 \times 10^{-9}$

First, Ge-Si$_x$Ge$_{1-x}$ core-shell NWs are dispersed on a SiO$_2$ (28nm) / Si (*p*+) substrate and ion-implanted with P at the energy of 6 keV with a dose of 10^{15} cm^{-2}. The dopants are then activated using fRTP at temperatures from 600 ˚C to 900 ˚C. Figure 4-11(a) shows the applied thermal profiles at each activation temperature. The thermal process consists of an intermediate temperature anneal, which allows for full recystallization of the implanted region with minimal dopant diffusion, followed by a 1 ms anneal at the nominal fRTP temperature for the activation of implanted dopants. For fRTP temperatures between 600 ˚C and 800 ˚C, the intermediate temperature of 400 ˚C is reached in 2 min. For fRTP at 850 ˚C and 900 ˚C, the intermediate temperatures of 450 ˚C and 500 ˚C are reached in 25s and 20s, respectively. The recrystallization of the implanted region is completed in a few seconds at these temperatures []. Next, the ρ values were determined by four-point measurements on multi-terminal devices with Ni contacts, where the current (*I*) flows from *S* to *D*, and V_1 and V_2 are used to probe the voltage drop along the NW the devices as described in Chapter 2.3.4 [Fig. 4-11(b) (inset)].

Figure 4-11(b) summarizes the ρ values of P-implanted Ge-Si_xGe_{1-x} core-shell NWs for different flash anneal temperatures and Table 4-2 summarizes the metal (Ni) to NW specific contact resistances for each flash temperature. For comparison, the resistivities of P-implanted Ge-Si_xGe_{1-x} core-shell NWs from the Table 2-2 were also plotted in Fig 4-11(b), where dopants are activated by a conventional RTP at 500 ˚C for 5 min, a condition typically used for P activation. It shows that the resistivity of P-implanted NWs, fRTP-activated at 900 ˚C, is $3.9 \pm 0.4 \times 10^{-3}$ Ω·cm with the Ni-NW specific contact resistivity of $3.1 \pm 1.1 \times 10^{-9}$ Ω·cm^{-2} and contact resistance of 520±210 Ω. On the other hand, the resistivity of P-implanted NWs, RTP-activated at 500 ˚C for 5 min, is $6.3 \pm 2.2 \times 10^{-3}$ Ω·cm with the Ni-NW specific contact resistivity of $9.7 \pm 9.5 \times 10^{-9}$ Ω·cm^{-2}, corresponding to contact resistances of 1050±760 Ω. These results clearly show that fRTP provides a higher dopant activation level in NWs, compared with RTP.

4.6 ENHANCED PERFORMANCE OF GE-SI_XGE_{1-X} CORE-SHELL NW TFETS USING FLASH-ASSISTED RAPID THERMAL PROCESS

Two Ge-Si_xGe_{1-x} core-shell NW TFETs were fabricated using the same process shown in Chapter 4.1. The source of both NW TFETs were P-implanted with a dose of 10^{15} cm^{-2} at the energy of 6 keV while the drain regions were B-implanted with a dose of 10^{14} or 10^{15} cm^{-2} at the energy of 3 keV. The dopants in the S/D regions of NW TFETs were then fRTP activated at 900 ˚C, a temperature chosen according to Figure 4-11(b) data.

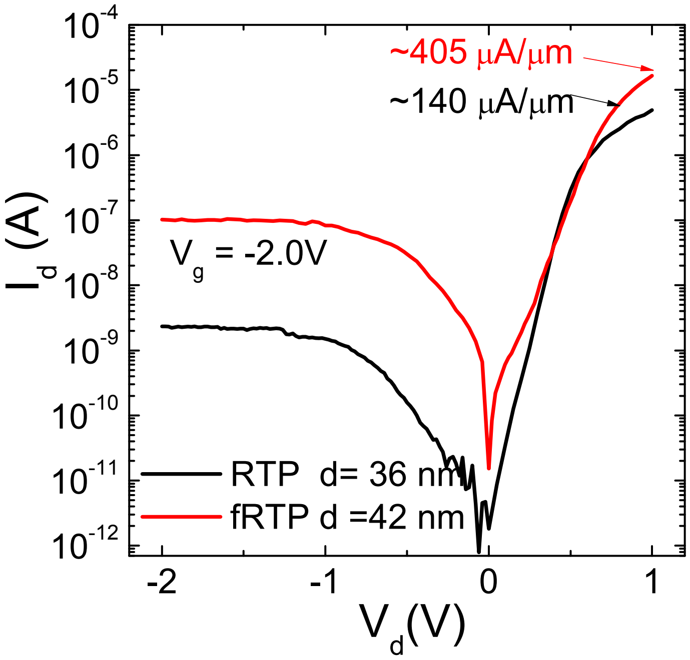


Figure 4-12: Diode characteristics of Ge-Si_xGe_{1-x} core-shell NW TFETs: The I_d - V_d characteristics of NW TFETs on a log-lin scale, measured at V_g = -2.0V. The red (black) solid line represents a fRTP- (RTP-) activated NW TFET. The phosphorous and boron implant doses are the same in both devices (P : 10^{15}cm^{-2}, B : 10^{15} cm^{-2}). Recombination dominates the current in forward bias, while BTBT dominates the current in reverse bias.

Figure 4-12 shows the *p-i-n* diode characteristics of two representative NW TFETs, where the red solid line represents the fRTP-activated NW TFET and the black solid line represents the RTP-activated NW TFET shown in Figure 4-3, having a diameter of d = 42 nm and d = 36 nm, respectively. The source (*n*+) and drain (*p*+) regions of both NW TFETs were ion-implanted with phosphorus and boron at a dose of 10^{15} cm^{-2}. Figure 4-12 shows I_d vs. V_d data measured from -2.0 V to 1.0 V at constant V_g = -2.0 V. In forward bias (V_d > 0V), where the drain (*p*+) is positively biased, the currents for the fRTP-activated device at V_d = 1.0 V is ~405 μA/μm which is approximately three times higher than that of the RTP-activated device, ~140 μA/μm. In the reverse bias region ($V_d < 0$) where the current is controlled by carrier BTBT at the source-channel junction, the fRTP-activated NW TFET shows at least one order of magnitude higher current compared with the RTP-activated device. This result clearly demonstrates the better dopant activation realized by fRTP.

The device characteristics of NW TFETs were further investigated in the reversed biased regions. Figure 4-13 shows the output ($I_d - V_d$) and transfer ($I_d - V_g$) characteristics of the fRTP-activated Ge-Si_xGe_{1-x} core-shell NW TFETs. To compare the enhanced performance using fRTP, the data of the RTP-activated NW TFETs shown in Figure 4-4 and 4-5 were plotted together. Here, the solid lines (red) and the dotted lines (black) represent the electrical characteristics of NW TFETs, having the same *S/D*-doping condition, activated by fRTP and RTP, respectively. The data in Figure 4-13(a) and (b) show the electrical characteristics of NW TFETs with asymmetric *S* (P*:* 10^{15} cm^{-2}) and *D* (B*:* 10^{14} cm^{-2}) doping. The NW diameters (*d*) in these devices are 45 nm. The right *y*-axis of the I_d-V_d graph shows the I_d values normalized by *d*. The maximum current of the fRTP-assisted TFET at V_d = -3.0 V, V_g = -3.0 V is ~28 μA/μm, approximately one order of magnitude higher current than the ~2 μA/μm of a similar, RTP-activated TFET. Figure 4-13(b) shows the I_d-V_g characteristics of NW TFETs. Both devices show unipolar behavior thanks to a lower *D*-doping (B: 10^{14} cm^{-2}), which results in a wider tunnel barrier at the drain-channel junction. An improved *SS* value from 560 mV/dec (RTP) to 440 mV/dec (fRTP) is also observed.

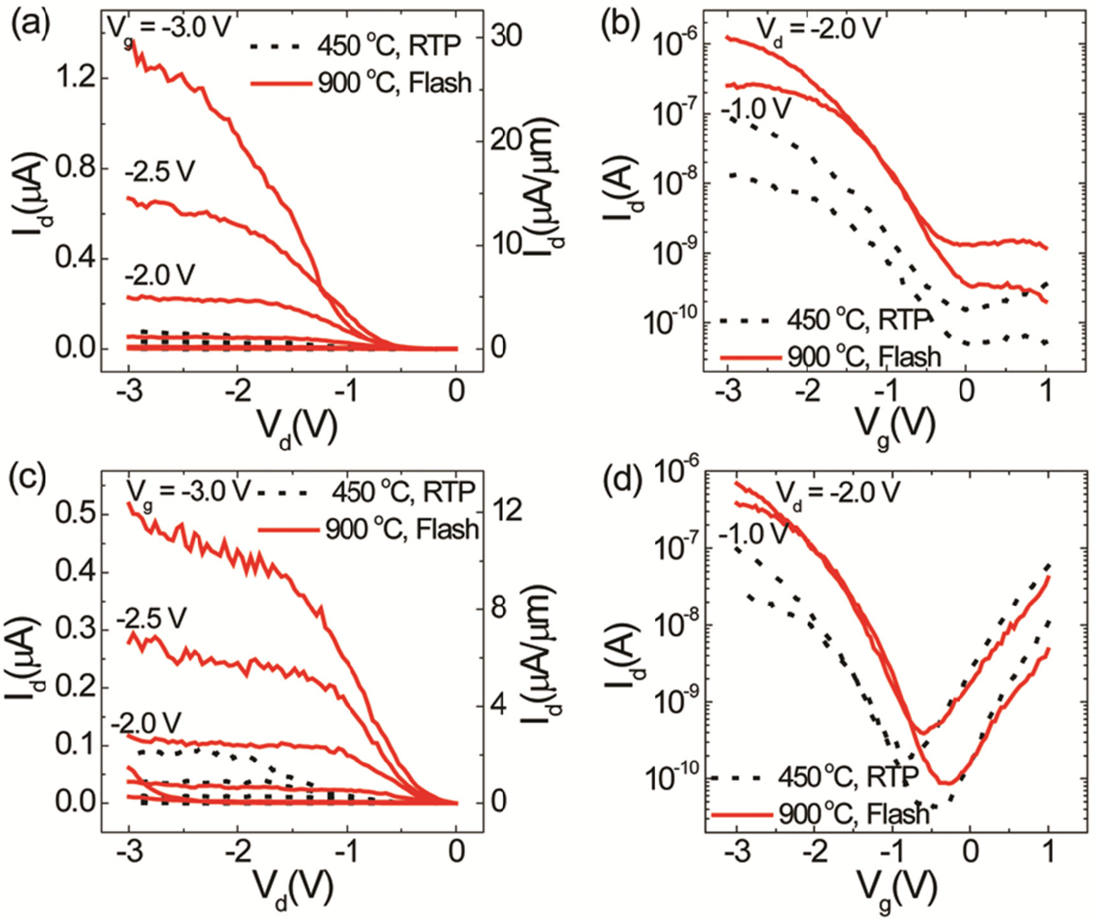


Figure 4-13: Electrical characteristics of Ge-Si_xGe_{1-x} core-shell NW TFETs (a) Output ($I_d – V_d$) and (b) transfer characteristics ($I_d – V_d$) of two devices with (P: 10^{15} cm^{-2}, B: 10^{14} cm^{-2}) *S/D* doping. (c) Output and (d) transfer characteristics of NW TFETs with (P: 10^{15} cm^{-2}, B: 10^{15} cm^{-2}) *S/D* doping. The solid (red) lines correspond to fRTP-annealed devices, while the dotted (black) lines correspond to devices where RTP was used for dopant activation. The gate length is 600 nm for all devices. The right *y*-axis of the $I_d – V_d$ graphs show I_d normalized to the NW diameter.[95]

Figure 4-13(c) and Fig. 4-13(d) show the electrical characteristics of NW TFETs with high *S/D* doping (P: 10^{15} cm^{-2}, B: 10^{15} cm^{-2}). The NW diameters for these devices are 36 nm (RTP-activated) and 42 nm (fRTP-activated), corresponding to maximum I_d / d values at V_d = -3.0 V of ~2 μA/μm and ~12 μA/μm; the V_t values for RTP- and fRTP-assisted devices are -1.5 V and -1.68 V, respectively. The decrease of *SS* value, from 360 to 320 mV/dec, was also observed, which is consistent with the observations of Fig. 4-13(a), (b). The electrical characteristics of Fig. 4-13(d) show ambipolar behavior, expected as the drain-channel junction becomes sufficiently thin for BTBT. The slightly lower I_d values for the devices of Fig. 4-13(c), (d), by comparison to Fig. 4-13(a), (b) data stem from the difference in gate overdrive voltage ($|V_g-V_t|$). For the same gate overdrive of 1.0 V at V_d = -2.0V, the drain currents for an unipolar and ambipolar (fRTP-assisted) are ~ 8 μA/μm and ~10 μA/μm, respectively.

Lastly, the results show that while the fRTP does provide an improvement in the TFET ON-current, the *SS* values remain relatively high and negatively impact the ON/OFF ratio, a finding attributed to interface traps in the gate stack. The interface traps have two adverse effects on the TFET device performance. First, they reduce the gate control of the channel, as the interface trap states add a series component to the dielectric capacitance. Secondly, because the BTBT at the source depends on the longitudinal electric field in the channel, the reduced gate control of the channel translates into a reduced carrier injection.

4.7 SUMMARY

In this chapter, the fabrication process and the performance of Ge-Si_xGe_{1-x} core-shell NW TFETs were demonstrated. The NW TFETs were fabricated by using a conventional CMOS process, employing low energy ion implantation to dope the S/D with different polarities of dopant. The diode characteristics of NW FETs were first investigated and the results confirmed the formation of gated *p-i-n* diode structure and proper dopant activation both in the source and drain. The device characteristics of NW TFETs were carefully investigated, including temperature dependent device characterization, which indicates that the main carrier injection mechanism in NW TFETs is BTBT. In addition, the ambipolar behavior was successfully suppressed by lowering the drain B-doping concentrations, widening the tunneling barrier at the drain-channel junction. To improve the performance of NW TFETs, the fRTP was employed for the activation of dopants in the source and drain. Thanks to fRTP, the ON-state current in NW TFET was increased about one order of magnitude by comparison to RTP-activated NW TFETs. The maximum current level in the NW FETs is one of the highest up to date among TFETs. However, the *SS* values of the device are still relatively high, attributing to the high interface trap density. Thus, to further enhance the device performance, it is necessary to improve the interface quality between the NW and the gate oxide.

CHAPTER 5

Summary and Future works

5.1 THESIS SUMMARY

The scaling of MOSFETs has been stymied by the increased power dissipation and performance loss due to short channel effects. In order to mitigate the problems and extend the device scaling, numerous investigations have been made in these days. In this effort, this thesis mainly focused on fabrication and characterization of high performance Ge-Si_xGe_{1-x} core-shell NW FETs and NW TFETs, based on optimized NW-doping technique using ion implantation.

In Chapter 1, the scaling trend of MOSFETs was briefly reviewed and the challenges of device scaling were addressed. The non-planar geometries, high mobility channel materials, and TFETs were suggested as alternate options to replace planar Si MOSFETs. As a channel material to examine such device options, the advantages of Ge-Si_xGe_{1-x} core-shell nanowires were explained, where GAA device geometry can be easily achieved on a NW and Ge's high hole mobility and low bandgap are also suitable to realize high performance FETs and TFETs.

In Chapter 2, we describe the growth of Ge-Si_xGe_{1-x} core-shell NWs, using a combination of VLS Ge NW growth and UHV CVD SiGe growth. The boron- and phosphorus-doping of the NWs using low energy ion implantation were systematically investigated. The analysis of the grown NWs demonstrates the successful epitaxial Ge-Si_xGe_{1-x} core-shell NWs growth and unveiled the thicknesses and compositions of the Ge core and the Si_xGe_{1-x} shell. To realize high performance NW FETs or TFETs using the grown NWs, however, one essential requirement is to establish reliable NW-doping techniques. Among the available NW-doping methods, ion implantation was the suitable way to realize such devices since it provides the most accurate doping modulation along a NW compared with other approaches. Thus, using the grown NWs, ion implantation and dopant activation conditions were optimized for both boron and phosphorus. Here, a key to successful NW-doping was to determine the proper ion energies and doses, not fully-amorphizing the entire NW body. The results showed that successful NW-doping using boron and phosphorus ion implantation, exhibiting a doping concentration as high as 2×10^{20} cm^{-3} with specific contact resistances as low as 4×10^{-10} $\Omega\cdot$cm^{2} in the B-doped NWs. Similarly low channel resistances and contact resistances in the P-doped NWs. However, relatively high NW resistivities and a NW-Ni contact resistance were observed in P-doped NWs, which is attributed to high trap density near the conduction band in Ge. In addition, the activation of B-implanted NWs was insensitive to the temperature above 400 ˚C, while P activations depend more on the applied activation temperatures. These finding paved the way to realize NW-based FETs and TFETs using conventional CMOS process.

In Chapter 3, the fabrication process of Ge-Si_xGe_{1-x} core-shell NW FETs with highly doped source and drain was demonstrated, where the highly doped S/D were realized by low energy boron ion implantation. The performances of these devices, namely ON-current and ON/OFF ratio, were improved by comparison to *undoped* S/D NW FETs, showing two orders of magnitude higher drive currents and a ten-fold increase in ON/OFF ratio. To substantiate the characteristics of high performance Ge-Si_xGe_{1-x} core-shell NW FETs, scaling properties of the devices were systematically investigated using the NW FETs with different channel lengths, which allow to extract key device parameters, such as intrinsic channel resistance, carrier mobility, effective channel lengths, and external contact resistance, as well as to benchmark the device switching speed and ON/OFF current ratio. The results show that the mobilities of these devices are a three-fold higher than Si MOSFETs with high-κ dielectrics, and ON/OFF characteristics are comparable to or excelling the most recent planar Ge MOSFETs. TCAD simulation was also employed to better understand the performance degradation factors in the devices, indicating that high interface trap density in the devices is responsible for the performance degradation. Lastly, the role of Si_xGe_{1-x} *shell* composition on device performance was investigated.

In Chapter 4, the fabrication process and the performance of Ge-Si_xGe_{1-x} core-shell NW TFETs were demonstrated. The NW TFETs were fabricated by using the similar process used for the NW FET fabrication, employing low energy ion implantation to dope the S/D with different polarities of dopants. The diode characteristics of NW FETs were first investigated and the results confirmed the formation of gated *p-i-n* diode structure and proper dopant activation both in the source and drain. The device characteristics of NW TFETs were carefully investigated, including temperature dependent device characterization, which indicates that the main carrier injection mechanism in NW TFETs is BTBT. In addition, the ambipolar behavior was successfully suppressed by lowering the drain B-doping concentrations, widening the tunneling barrier at the drain-channel junction. To improve the performance of NW TFETs, the fRTP was employed for the activation of dopants in the source and drain. Thanks to fRTP, the ON-state current in NW TFET was increased about one order of magnitude by comparison to RTP-activated NW TFETs. The maximum current level in the NW FETs is one of the highest up to date. However, the *SS* values of the device are still relatively high, attributing to the high interface trap density. Thus, to further enhance the device performance, it is necessary to improve the interface quality between the NW and the gate oxide.

5.2 SUGGESTION FOR FUTURE WORK

One common performance degradation factor in both Ge-Si_xGe_{1-x} core-shell NW FETs and NW TFETs is high density of interface traps between a NW surface and gate dielectric. High D_{it} degrades the *SS* characteristics and DIBL in the NW FETs, and it also worsens ON-current and the *SS* in the NW TFETs. Therefore, better passivation process for Ge-Si_xGe_{1-x} core-shell NW should be further investigated.

Second, smaller NW diameters need to be employed to further scale down NW FETs and to improve NW TFET performances. In NW FETs, a thinner NW body thickness enhances the gate electrostatic control over the channel and thereby extends device scaling limits by suppressing the short channel effects. In NW TFETs, it helps to strongly couple the gate to the channel ($C_{ox} \approx C_{inv}$), improve the energy band profile modulation in the *intrinsic* NW segment, and increases BTBT currents.

Third, the C-V measurement techniques on an individual nanowire need to be established. Due to the reduced dimensions of NWs, C_{ox} was calculated using TCAD simulation, which may overestimate or underestimate the actual capacitance values. The direct measurement of gate capacitance will allow to more accurately extract transistor performance factors such as intrinsic delay and mobility.

Fourth, the Si_xGe_{1-x} *shell* thickness and composition are needed to be optimized. In Chapter 3.5, the mobilities of the NW FETs were changed closely with the Si_xGe_{1-x} *shell* composition. Thus, by optimizing Si_xGe_{1-x} shell, high mobility channel material can be engineered to realize high performance the NW FETs. In addition, the engineering of Si_xGe_{1-x} shell is also important to minimize defects generation due to lattice mismatch as well as improve interface quality for the gate oxide deposition.

Lastly, NW doping methods should be further explored to provide sharper junction profiles. They will help to improve ON-currents of NW TFET and extend the scaling of NW FETs. Besides, different NW-doping method other than ion implantation may also be necessary to dope NWs with extremely small diameters.

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Vita

Junghyo Nah is from Republic of Korea. He received the Bachelor of Science degree in Electrical and Computer Engineering (ECE) Department from Ajou University, Suwon, Korea in 2005, *Summa cum Laude* (ranked 1st in the Dept). During his B.S study, he received all-expense-paid scholarship for eight consecutive semesters, awarded based on College Scholastic Ability Test score (within 2% in the nation). In 2007, he received M.S. degree in the Electrical and Computer Engineering at the University of Texas at Austin, where he continued for Ph.D. degree. During his graduate study, he received National Fellowship from the Korea Research Foundation in 2005. He also received *Ben Streetman Prize for outstanding research in electronic and photonic materials and devices* in 2009. He worked as a summer intern in Component Research at Intel Corp. Hillsboro, Oregon in 2010. He continues his career as a postdoctoral researcher at University of California at Berkeley.

Permanent address:
5217 Old Spicewood Springs Rd. 810, Austin, TX 78731, U.S.A.
This dissertation was typed by the author.