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Materials and Processes for Advanced Lithography Applications

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Materials and Processes for Advanced Lithography Applications

by

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To my family.

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Materials and Processes for Advanced Lithography Applications

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Step and Flash Imprint Lithography (S-FIL) is a high resolution, next-generation lithography technique that uses an ambient temperature and low pressure process to replicate high resolution images in a UV-curable liquid material. Application of the S-FIL process in conjunction with multi-level imprint templates and new imprint materials enables one S-FIL step to reproduce the same structures that require two photolithography steps, thereby greatly reducing the number of patterning steps required for the copper, dual damascene process used to fabricate interconnect wirings in modern integrated circuits. Two approaches were explored for the implementation of S-FIL in the dual damascene process: sacrificial imprint materials and imprintable dielectric materials.

Sacrificial imprint materials function as a pattern recording medium during S-FIL and a three-dimensional etch mask during the dielectric substrate etch, enabling the simultaneous patterning of both the via and metal structures in the dielectric substrate. Development of sacrificial imprint materials and the associated imprint and etch processes are described. Application of S-FIL and the sacrificial imprint material in a commercial copper dual damascene process successfully produced functional copper interconnect structures, demonstrating the feasibility of integrating multi-level S-FIL in the copper dual damascene process.

Imprintable dielectric materials are designed to combine the multi-level patterning capability of S-FIL with novel dielectric precursor materials, enabling the simultaneous deposition and patterning of the interlayer dielectric material. Several candidate imprintable dielectric materials were evaluated: sol-gel, polyhedral oligomeric silsesquioxane (POSS) epoxide, POSS acrylate, POSS azide, and POSS thiol. POSS thiol shows the most promise as functional imprintable dielectric material, although additional work in the POSS thiol formulation and viscous dispense process are needed to produce functional interconnect structures. Integration of S-FIL with imprintable dielectric materials would enable further streamlining of the dual damascene fabrication process.

The fabrication of electronic devices on flexible substrates represents an opportunity for the development of macroelectronics such as flexible displays and large area devices. Traditional optical lithography encounters alignment and overlay limitations when applied on flexible substrates. A thermally activated, dual-tone photoresist system and its associated etch process were developed to enable the simultaneous patterning of two device layers on a flexible substrate.

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Overview

The work described herein encompasses the motivations for new lithographic techniques, their underlying material and process development, and their applications. Chapter 1 provides a primer on the history of microlithography and an overview of the current microlithographic technologies. The advantages and limitations of the existing lithographic processes inspired the development of new lithography techniques that are described in the subsequent chapters.

Chapter 2, 3, and 4 describe the application of multi-level Step and Flash Imprint Lithography (S-FIL®) in a dual damascene fabrication process. Chapter 2 outlines the key components of the S-FIL process and their functions. The S-FIL process development protocols that I employed during the formulation and evaluation of sacrificial imprint materials and imprintable dielectric materials are detailed in chapter 2.

Chapter 3 describes the motivation, development, and evaluation of S-FIL integration with sacrificial imprint material in a copper dual damascene fabrication process. My involvement in this work includes formulation of candidate sacrificial imprint materials, development of a multi-level S-FIL protocol for patterning of dual damascene structures, and preparation of functional, imprinted samples for etch development and electrical testing.

Chapter 4 describes the development of imprintable dielectric materials to combine the three-dimensional patterning capability of S-FIL with the deposition of permanent dielectric material. Synthesis and study of several classes of materials as IDM had been previously reported by other members of our research group. My work includes formulation and evaluation of the POSS azide and POSS thiol candidate imprint materials, and development of the viscous dispense procedure for use with POSS thiol material.

Chapter 5 outlines the motivation for developing a lithographic patterning process on flexible substrates, where conventional photolithography encounters layer-to-layer alignment limitations. My work in this project includes formulation of a functional dual-tone photoresist, development of dual-tone photolithographic and etching processes, and successful demonstration of the dual-tone lithography on a flexible substrate. Finally, chapter 6 summarizes the projects described above and provides recommendations for future work.

Chapter 1: Introduction

The invention of the transistor in 1947 is considered to be one of the greatest creative discoveries of the twentieth century. Originally developed in AT&T Bell Labs to replace inefficient vacuum tubes for signal amplification in telephony equipment [1], the transistor has since become the fundamental building block in almost all modern electronic devices. Today, transistor-based electronic devices range from complex supercomputers used in weather prediction, to simple digital clocks and appliances found in everyday life, to modern conveniences such as personal computers, internet, and cellular phones. The pervasiveness of these electronic devices in modern society is best illustrated by the 2006 studies that found more than 80% of the US population carried a cell phone [2], and at least 30 countries around the world had already exceeded 100% per capita cell phone usage [3]. The rapid development of the transistor from a laboratory curiosity to an integral part of everyday life is made possible by the microelectronics industry and its continuous drive to make smaller, faster, and cheaper transistor devices.

Smaller transistors are desirable for two reasons: increased speed and reduced cost. A smaller transistor size contributes to a faster switching rate in the metal-oxide-semiconductor field-effect transistors (MOSFET). The first MOSFET was demonstrated in 1960 by Dawon Kahng at AT&T Bell Labs [4]. The MOSFET allows low cost of production and ease of integration [5], and today it is the most common transistor in both digital and analog devices. As the feature size of a MOSFET device is scaled down, its gate capacitance is reduced due to the smaller gate size, resulting in a lower RC delay and a faster switching rate of the transistor gate. The increase in MOSFET switching rate translates into a faster calculation speed of the electronic device. However, as the size continues to shrink for state-of-the-art MOSFET devices, the delays in other portions of the device begin to dominate, diminishing the benefit of shrinking transistor size [6].

More importantly, smaller transistor size allows more transistors to be packed into a given surface area, increasing the transistor density of the device. This results in a smaller chip with the same functionality and more chips per wafer. Since the per-wafer cost of semiconductor fabrication is relatively fixed, smaller transistor size directly translates into lower production cost per chip and lower transistor cost [7]. The microelectronic industry's constant push to make smaller transistors is reflected in the logarithmic trends in transistor cost and speed, shown in Figure 1.1.

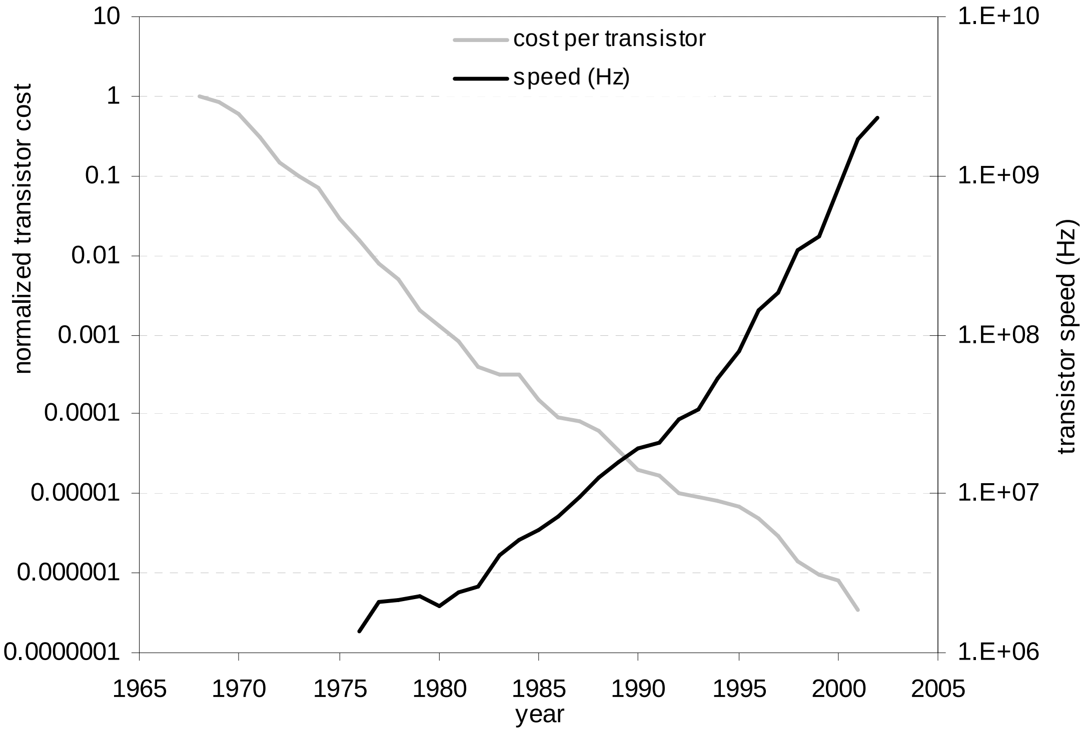

Figure 1.1: Historical trends in transistor cost and speed. The cost per transistor, normalized to the 1968 value, has been decreasing logarithmically with time. During the same time period, the transistor switching speed has grown exponentially [8-9]. *Data courtesy of Intel Corporation.*

A modern electronic device, such as the microprocessor shown in Figure 1.2, contains as many as hundreds of millions of transistors and multiple levels of wiring to connect those transistors to one another and to the outside world. This multi-layer stack is commonly built from the bottom up: starting with the deposition of a layer of material, then the microlithography to create the circuit design, and finally the completion of the circuit structures with wafer processes such as implant, metallization, polish, etc. These steps are then repeated for each new layer of circuit structures, forming the complex circuitry in modern electronic devices. A state-of-the-art microprocessor, such as the one shown in Figure 1.2A, may contain more then twenty circuit layers and requires several hundreds of process steps to complete.

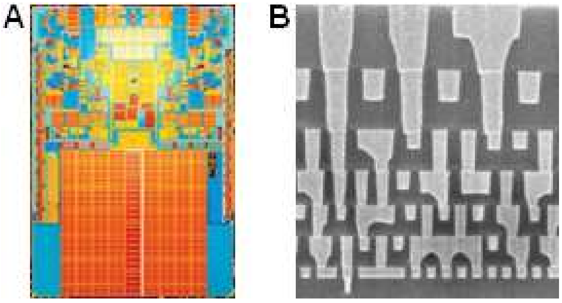

Figure 1.2: Modern electronic devices contain large numbers of transistors and require many layers of circuit structures to connect those transistors. A. Top-down view of Intel 45nm dual-core Penryn processor die, showing 410 million transistors in a 107 mm^2 area. B. Cross-sectional view of the Intel Northwood processor, showing seven layers of interconnects [9-10]. *Image courtesy of Intel Corporation*.

Among the many unit operations in integrated circuit fabrication, the microlithography process stands out as the technical limiter for transistor size and thus device performance and cost [11]. Microlithography is the process used to create large numbers of microscopic circuit elements in transistor devices. The modern microlithography process was first developed in the 1960s following the invention of integrated circuits in 1958 [12]. Since then, advances in the microlithography process have been the driving force behind the exponential growth in transistor technology, allowing the creation of smaller and smaller transistor circuit elements. This, in turn, enables more functionality to be packed into smaller electronic devices at lower costs, allowing the application of electronics in ways never thought possible a mere generation ago. Future advances in microelectronics will require innovations in materials and processing to address the new challenges in the microlithography process.

1.1 THE MICROLITHOGRAPHY PROCESS

The microlithography process duplicates the circuit design from a master pattern source, such as a photomask, onto a substrate. Figure 1.3 outlines the basic microlithography process in semiconductor fabrication.

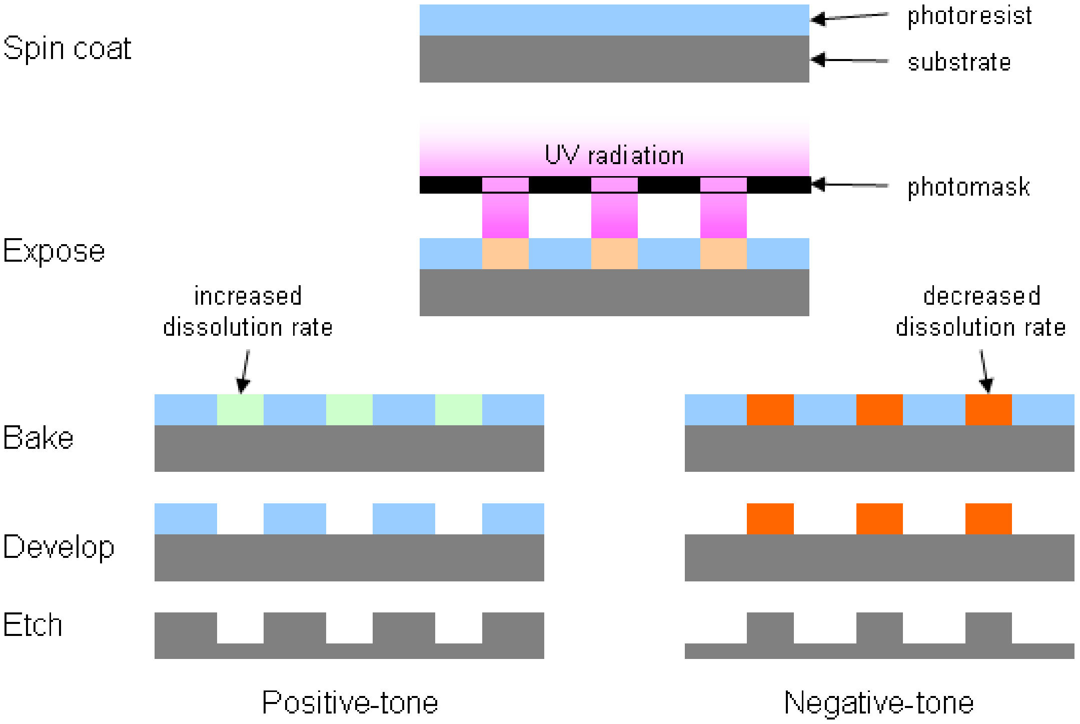

Figure 1.3: The lithographic patterning process for positive and negative tone photoresists.

The substrate to be patterned (polysilicon, silicon oxide, metal, etc.) is first spin coated with a thin film of photosensitive material known as a photoresist. The photoresist film provides two important functions: a recording medium for the photographically projected circuit pattern, and a barrier material to protect the underlying substrate during the later etching process.

Once coated with the photoresist, the substrate is exposed to actinic radiation through a photomask. The photomask contains the desired circuit design as arrangements of opaque and transparent regions. Projection of actinic radiation, commonly ultraviolet light, through the photomask and onto the substrate duplicates the circuit pattern from the photomask onto the photoresist film on the surface of the substrate. The portion of the photoresist exposed to the radiation undergoes photochemical reactions, and with the subsequent bake step, alters the dissolution rate of the exposed area of the photoresist film in the developing solvent. For the positive-tone photoresist, the exposed areas dissolve more quickly in the developer solvent. For the negative-tone photoresist, the exposed areas dissolve more slowly in the developer solvent. It is this photochemically induced dissolution rate change that allows the photoresist to store the projected circuit pattern.

During the develop step, the regions of the photoresist film with higher dissolution rate are dissolved away by the developer solvent, exposing the underlying substrate material to the subsequent etch process. The etch process selectively removes the exposed substrate material, transferring the circuit pattern from the photoresist film into the substrate. Overall, the combination of exposure and etch processes allows the duplication of the circuit design from the photomask into the substrate, whose polysilicon, silicon oxide, or metal materials could not have been patterned directly by radiation. After the etch process, the remaining photoresist is removed and the substrate is ready for the next processing steps to complete the required device.

The basic semiconductor microlithography process has changed little since its initial development in the 1960s. The exponential improvements in transistor fabrication can be attributed to continuous innovations in the materials and processing of the individual steps. This is especially true for the lithography steps that are responsible for the patterning of the transistor circuits. As the industry continues to shrink transistor sizes, the lithography systems have evolved a long way from their original 1960s incarnations to attain higher patterning resolutions and fidelities demanded by the rigorous modern manufacturing requirements.

1.2 THE EVOLUTION OF PHOTOLITHOGRAPHY

The first practical microlithography process for high volume integrated circuits fabrication was developed in 1959 by Robert Noyce at Fairchild Semiconductor [13]. In his microlithography process, the duplication of the master circuit design into the silicon wafer was accomplished using photolithography. Since then, innovations in the photolithography process have enabled it to meet the challenges of the ever shrinking transistor size. Today, photolithography continues to be the dominant exposure technology in integrated circuits fabrication.

1.2.1 Contact Lithography

The first mass produced integrated circuits had features on the order of 200 micrometers and were printed using contact lithography. In contact lithography, a quartz photomask with an opaque chromium pattern is placed in direct contact with the photoresist film and exposed to ultraviolet light from a mercury arc lamp. The photomask covers the whole substrate to be printed, for example a silicon wafer, and simultaneously patterns the entire wafer. Contact lithography offers the simplest exposure hardware requirement and good image resolution. However, the direct physical contact between the photoresist and the photomask renders contact lithography highly susceptible to particulate contamination and defect accumulation. Any dust or particle caught in between the photoresist and the photomask distorts the optical image in the photoresist and/or damages the photomask, causing yield loss and process down time. For this reason, proximity lithography was developed to address the particle liability of contact lithography.

1.2.2 Proximity Lithography

In proximity lithography, the quartz photomask is brought into close proximity of the photoresist film (10~20 µm) and exposed to ultraviolet light. Because no actual contact is made between the photomask and the photoresist, proximity lithography generates fewer defects and improves the wafer yields (i.e. proportion of devices produced which function correctly). Proximity lithography has poorer resolution than contact lithography due to the air gap allowing more near field diffraction to occur between the photomask image and photoresist plane, but it is sufficient for production of features size down to 5 micrometer scale [14].

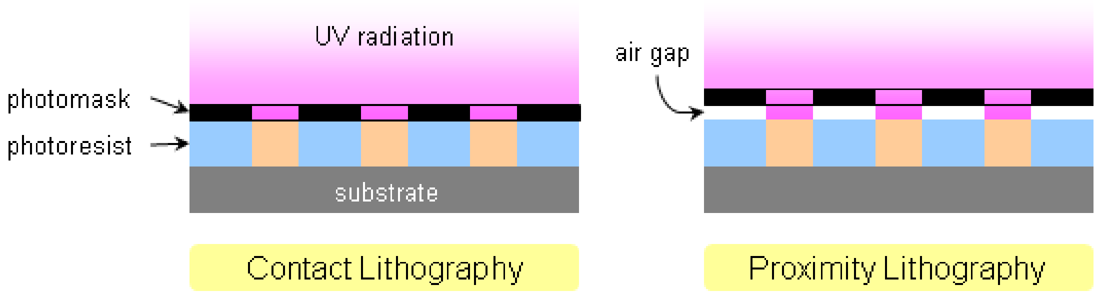

Figure 1.4: Contact and proximity lithography. A. In contact lithography, the photomask is in direct contact with the photoresist film. B. In proximity lithography, the photomask is held 10~20 µm above the photoresist film to reduce its particle liability.

Similar to contact lithography, proximity lithography requires the photomask to cover the entire wafer and patterns the whole wafer simultaneously, transferring the photomask pattern as-is into the wafer. This whole wafer process technique provides higher throughput for the transistor device fabrication, but it also imposes several limitations. The simultaneous patterning of an entire wafer requires the incident ultraviolet light to be uniform across the entire wafer and the photomask to align accurately to the full wafer. The transference of the photomask pattern as-is into the substrate, commonly referred to as the 1x technique, limits the patterning resolution to what is available on the photomask. As microlithography technology progressed to larger wafers and smaller feature sizes, it became increasingly difficult for proximity lithography to overcome these limitations. A new lithography system was needed.

1.2.3 Projection Lithography

A major advance came in 1978 with projection lithography [15], in which the photomask is placed far away from the substrate. The ultraviolet light from a mercury lamp is filtered and focused into a narrow stripe of light, then projected through the photomask into the photoresist coated substrate. The photomask and the substrate move in parallel through the focused beam, scanning the photomask design into the photoresist film (Figure 1.5A). The narrow light strip reduces the aberration and defect sensitivities of the optics system, and the non-contact nature of the projection process reduces the wafer and photomask's liability to particulate contaminations, greatly improving the process yields. However, this form of projection lithography is still limited by the constraints of the 1x patterning process, where the feature size in the photoresist is limited by what is available on the photomask. As the wafer size continued to grow and the circuit size continued to shrink, the cost effectiveness of the 1x projection system declined until the development of step-and-repeat projection lithography.

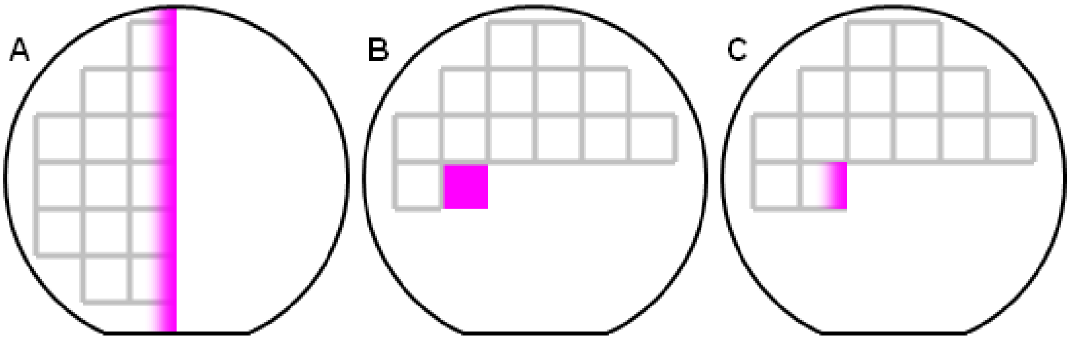

Figure 1.5: Three types of projection lithography [16]: A. Early projection system uses 1x optics and scans across the entire wafer. B. Step-and-repeat system uses reduction optics, steps through the wafer field-by-field, and exposes the entire field during each step. C. Step-and-scan system uses reduction optics, steps through the wafer field-by-field, and scans the field during each step.

1.2.4 Step-and-Repeat Lithography

Step-and-repeat lithography was developed in the early 1980s to address the limitation of the 1x projection process. Reduction optics were added to the projection system to scale down the photomask images before they were projected into the photoresist film. Reduction factors up to 10x were available, allowing much smaller features to be imaged into the photoresist than what is available on the photomask. In these systems, the wafer is exposed one portion at a time instead of all at once, with each portion referred to as a field (Figure 1.5B). As the wafer is exposed one field at a time, the photomask only needs to contain the circuit design of a single field, instead of the entire wafer. The step-and-repeat lithography and its reduction optics allowed smaller photomasks with larger features and smaller lens sizes, lowering the system cost and enhancing the pattern resolution [17].

1.2.5 Step-and-Scan Lithography

In the mid-1990s, as the microelectronic industry continued its push to make smaller transistors, the lens elements of the step-and-repeat projection system grew in size and became increasingly cost prohibitive. To alleviate the increasing lens requirements, the scanning technique of the previous 1x projection lithography was adopted into the step-and-repeat systems (Figure 1.5C). The resulting step-and-scan projection system continues to be used in the most advanced lithography processes today.

1.3 EXPOSURE WAVELENGTH

The early contact and proximity lithography systems commonly used the broadband radiation from a high pressure mercury vapor arc-discharge lamp as the exposure light. The mercury arc lamp produces primarily ultraviolet emissions, as shown in Figure 1.6. The spectral emission characteristic of the mercury arc lamp makes it ideal for the early generations of photoresists, such as the poly(cis-isoprene) based negative-tone photoresist and the novolak / diazonapthaquinone based positive-tone photoresist [18].

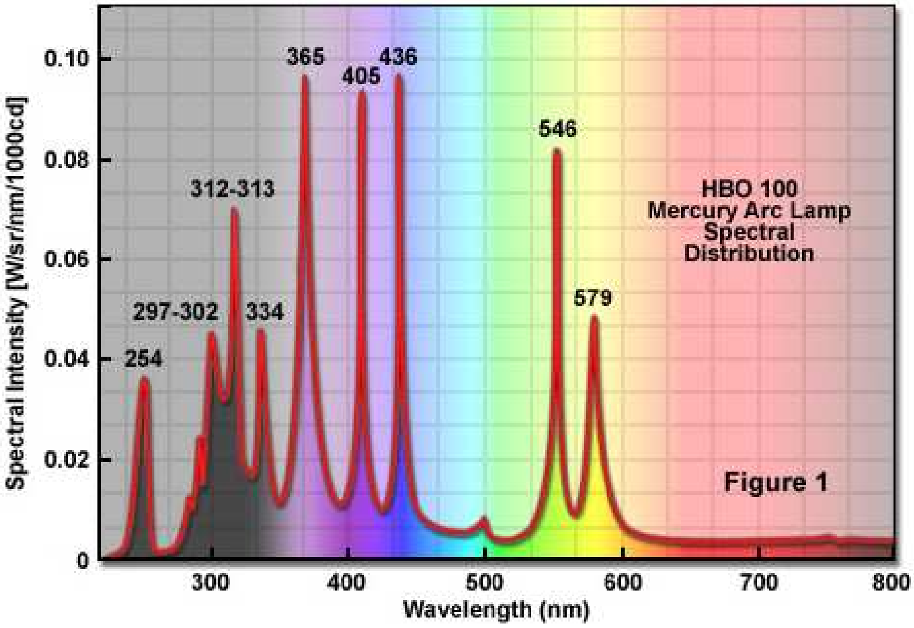

Figure 1.6: The emission spectrum of a high pressure mercury vapor arc-discharge lamps, used as a source of ultraviolet radiation in lithography tools [19]. *Image courtesy of Carl Zeiss, Inc.*

The introduction of projection lithography and the use of reduction optics between the photomask and photoresist film requires a narrower band of ultraviolet light wavelengths to minimize the effects of lens chromatic aberration. The reduction optics of the projection lithography systems also enable imaging of smaller features in the photoresist film than what is available on the photomask. The minimum feature resolution (R) of a projection system is described by the Rayleigh criterion [18],

$$R \propto k_1 \frac{\lambda}{NA}$$

where k_1 is a process factor derived from the particular imaging and post-processing techniques in use, with nominal value in the range of 0.25 to 0.7; λ is the wavelength of the actinic radiation used in the exposure; and NA is the numerical aperture of the lens system, which relates to the size of the lens and how much of the diffracted radiation is captured and focused onto the photoresist.

As the Rayleigh criterion suggests, the minimum resolution of the projected circuit images can be improved (reduced) by increasing the numerical aperture of the lens system and/or reducing the wavelength of the exposure light. For this reason, advances in light sources, optics technology, and the accompanying photoresist materials have been the major driving forces behind the improvements in projection lithography.

The early projection systems continued to use mercury arc lamps as the exposure light source. Optical filters were used to isolate high intensity peaks from the mercury arc lamp emission for lithographic imaging. The first projection systems used the 436 nm emission peak as the exposure source. These were succeeded by the 365 nm systems as the semiconductor industry progressed to smaller minimum resolution of the projected images. When the 365 nm systems approached their resolution limits, the 254 nm systems were developed for projection lithography. However, the comparatively low intensity of the 254 nm emission peak from the mercury arc lamp, as shown in Figure 1.6, significantly reduced the lithography process throughput and would not be a viable option for use in production systems.

The challenge of low exposure light intensity was answered by the introduction of the chemically amplified photoresist. Invented in the IBM Almaden Lab [20-21], the chemically amplified photoresist consists of an acid-generating photoinitiator (the photoacid generator, or PAG) and a resin polymer with acid-labile pendant groups. Upon exposure to ultraviolet radiation, the PAG undergoes photolysis, producing strong acid as a latent image. During the subsequent heating of the photoresist, the acid reacts with the surrounding acid-labile pendant groups, causing a change in the photoresist's solubility in developer solvent. A single acid molecule generated by the PAG photolysis can catalyze many such reactions, providing a catalytic amplification of the initial photochemical event. This chemical amplification greatly increases the photoresist’s sensitivity to the exposure energy, enabling the use of low intensity 254 nm exposure sources without adverse impact to the lithography process throughput.

Excimer lasers were developed in the late 1980s as an alternative exposure light source for photolithography systems. The krypton fluoride (KrF) excimer laser generates ultraviolet laser light at the 248 nm wavelength with much higher light intensity than what is available from the mercury arc lamp at 254 nm. This higher exposure light intensity enables increases in the lithography process throughput, leading to the widespread adoption of the KrF excimer laser as the photolithography exposure source in the 1990s. In the early 2000s, the excimer laser using argon fluoride (ArF) gas was developed to replace the KrF excimer laser system. The ArF excimer laser generates ultraviolet light at 193 nm wavelength. This shorter wavelength light allows further improvements in the minimum resolution of photolithography systems, and the 193 nm ArF excimer laser continues to be used as the exposure light source in the state-of-the-art photolithography systems today.

Several other wavelengths of ultraviolet light had also been considered during the evolution of the photolithography exposure light sources. The 405 nm emission peak of the mercury arc lamp offered comparable intensity level to the 436 nm (Figure 1.6), but was skipped by most manufacturers because it offered negligible resolution improvement over the previous 436 nm light source. The 157 nm fluorine excimer laser was developed to succeed the ArF excimer laser in step-and-scan lithography systems. However, persistent technical challenges with the lens and photoresist materials, the high cost of the 157 nm exposure equipment, and the advent of novel resolution enhancement techniques for the existing 193 nm systems led the microelectronic industry to discontinue implementation of the 157 nm excimer laser as the exposure source [22]. The viability of a potential exposure system is often as much an economical consideration as it is technical.

1.4 FUTURE OF LITHOGRAPHY

As the microelectronic industry continues to push the limits of the lithography technology, various patterning concepts are examined for their potential use in semiconductor fabrication. Figure 1.7 illustrates the microelectronic industry's current projection of future transistor sizes and some of the prospective next-generation lithography (NGL) technologies that are being developed to meet those transistor size targets.

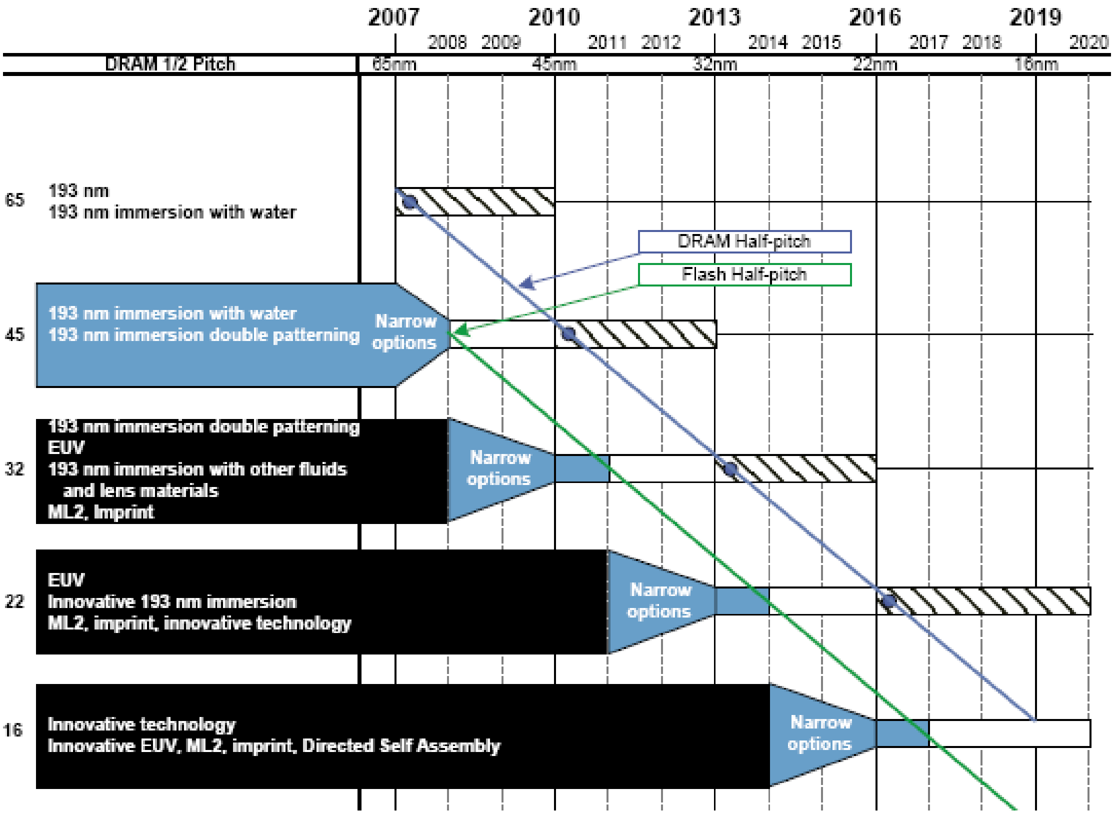

Figure 1.7: Potential next-generation lithography technologies [23]. *Image courtesy of ITRS.*

Amongst the potential NGL technologies being considered, two frontrunners are extreme ultraviolet light (EUV) lithography and nanoimprint lithography (NIL). Each of these technologies brings their own benefits and limitations, and much research is still underway to address these challenges and evaluate the feasibility of their integration into the commercial manufacturing process.

Incidentally, the NGL candidates' strongest competition comes from the extension of current 193 nm photolithography. The enormous development and capital costs of the contemporary lithographic technologies have driven manufacturers to exhaust the resolution capability of an existing optical projection technology before investing in any new system [18]. Resolution enhancement techniques (RETs), such as optical proximity correction, off-axis illumination, and phase-shift masks, have been employed to improve the minimum resolution of the existing photolithography technologies and extend their useful lifetime. Some of the prospective "next-generation" RETs, such as immersion lithography and double patterning lithography, potentially offer resolution improvements comparable to the NGLs without the need to develop new tools and systems. Ultimately, it is often a combination of technical, economical, and strategic considerations that determines the best potential lithography solution.

1.4.1 Immersion Lithography

Immersion lithography is a RET for the photolithography process. In the current immersion lithography system, the air gap between the final lens element and the wafer surface is filled with purified water, which has a higher refractive index than air at the 193 nm exposure wavelength (Figure 1.8). The higher refractive index medium enables the higher diffraction order light from the photomask image to arrive at the wafer instead of being internally reflected. This allows the lens numerical apertures to increase above

1.0 (the theoretical limit of air exposures), improving the image resolution and the depth of focus of the exposure system [24].

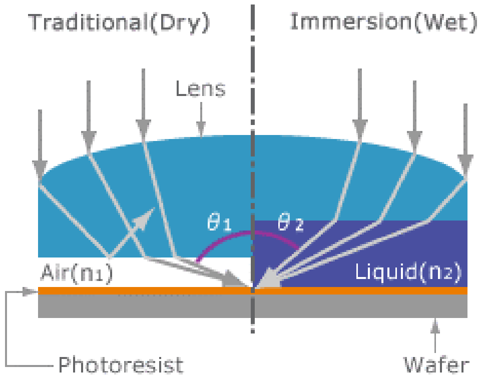

Figure 1.8: Comparison between traditional (dry) lithography and immersion (wet) lithography, illustrating the difference in the amount of higher diffraction order light successfully arriving at the wafer [25]. *Image courtesy of NEC Electronics.*

Immersion lithography technology has been adopted by the microelectronic industry for the 45 nm transistor technology. Companies such as IBM and AMD implemented immersion lithography in their 45 nm transistor fabrication process [26]. Likewise, Intel Corp is expected to implement immersion lithography in its 32 nm transistor process by 2009 [27]. However, the lack of suitable higher index immersion fluids and lens materials limit further resolution improvement from immersion lithography. Therefore, immersion lithography is expected to be used only as a temporary solution until the commercial implementation of other NGL process can be achieved (Figure 1.7).

1.4.2 Double Patterning Lithography

Double patterning is a process-intensive RET technology that has been debated for years for its use in photolithography process. In a double patterning process, a high resolution design is split into two halves, each with lower image resolution then the original and each half is separately exposed and processed (Figure 1.9). The combined patterns from the two imaging passes recreate the original design in the substrate, achieving the desired high resolution pattern without the high resolution demand on the individual lithography pass. Thus, double patterning extends the resolution capability of the existing lithography systems at the cost of an increased number of patterning steps.

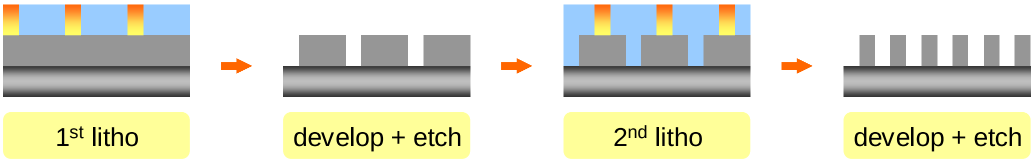

Figure 1.9: Overview of the double patterning process. Two halves of the original design is separately imaged and processed into the substrate. Their combined results recreate the original high resolution design.

As the existing 193 nm lithography system approaches its maximum numerical aperture (~0.93 in air and ~1.35 in water) and the readiness of other NGL technologies remains uncertain, double patterning is expected to be implemented by the microelectronic industry to extend the resolution capability of the existing 193 nm exposure technology. Leading manufacturers such as Samsung and Intel are already applying double patterning in their latest fabrication process [28-29]. Furthermore, the double patterning technique is expected to be applicable to other lithography technologies such as electron beam lithography, allowing immediate opportunity to improve image resolution.

1.4.3 Extreme Ultraviolet Lithography

EUV lithography is one of the potential NGL technologies being pursued for the 22 nm transistor technology and beyond. Conceptually, EUV lithography operates in a manner similar to traditional photolithography systems, using 13.4 nm wavelength soft x-ray as the actinic radiation. Although very high theoretical resolutions can be attained using this wavelength, the high energy of the 13.4 nm photon presents several unresolved challenges that limit its practical implementation. EUV resolution limiters include the uncontrollable dose variations (statistical shot noise) due to the low number of photons per exposure [30] and the contrast loss (proximity effect) due to the random secondary electrons generation by the EUV radiation [31]. Furthermore, all matter strongly absorbs EUV radiation, requiring the EUV exposure to take place in a high vacuum and precluding the use of refractive optical elements, in either the lenses or the photomask.

Full wafer EUV systems have been built using multiple Mo/Si multilayer interference mirrors (Figure 1.10), with more than 25% per-reflection loss and 85% overall loss [32]. The extremely high cost of the EUV tool, the low photon efficiency of the EUV optics, and the lack of a practical high intensity EUV light source [33] cause many manufacturers to remain uncertain of EUV lithography's throughput capability and commercial viability.

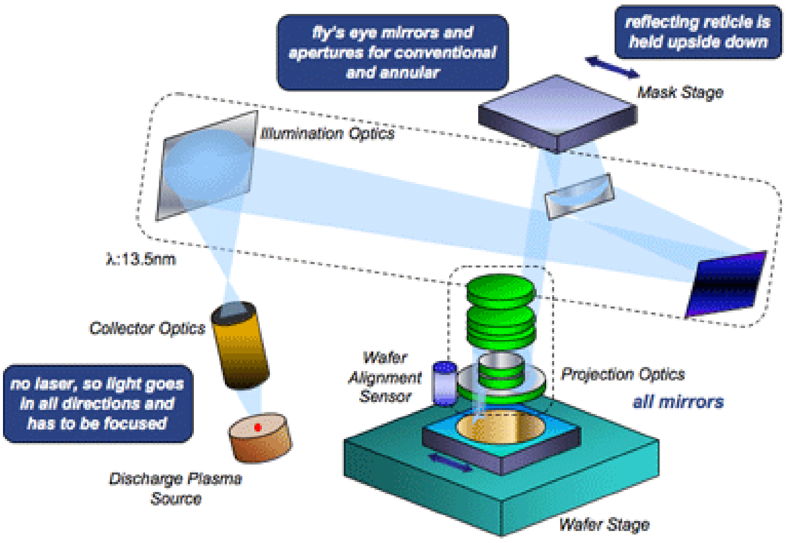

Figure 1.10: Generic EUV system design, showing the reflective optics between EUV source and the wafer. The entire optical path needs to be in a high vacuum to avoid absorption of EUV by air [34]. *Image courtesy of Nikon Precision, Inc.*

1.4.4 Nanoimprint Lithography

Imprint lithography was first adopted for nanofabrication by Stephen Chou at University of Minnesota [35]. Essentially a stamping process, the NIL process mechanically deforms an imprint medium using a three-dimensional mold with the desired pattern. The imprint medium is then hardened to produce a negative of the mold pattern. Several variations of NIL technology have since been developed for different applications. In the Step and Flash Imprint Lithography (S-FIL) process developed by Colburn, et al. [36], a photocurable fluid is used as the imprint medium and a rigid quartz template is used as the mold. The imprint fluid is dispensed onto the substrate and pressed with the template. The fluid fills the mold and is then solidified by a brief UV exposure, forming the desired pattern as shown in Figure 1.11. This process is repeated across the wafer, similar to the step-and-repeat lithography process.

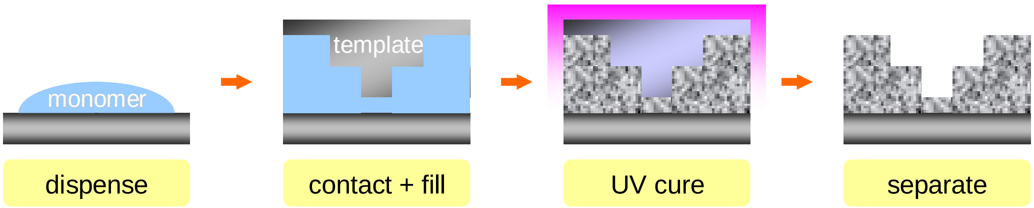

Figure 1.11: Overview of the Step and Flash Imprint Lithography (S-FIL) process.

Two main benefits of the NIL technology are lower cost and high resolution patterning. The physical pattern transfer process of NIL removes the need for complex projection optics and light source, simplifying equipment and cost. The resolution limit of the NIL process may only be limited by the ability to produce the mold. Work by Rogers et al. at the University of Illinois at Urbana-Champaign demonstrated successful replication of the shape of a carbon nanotube using an imprint process [37], as shown in Figure 1.12.

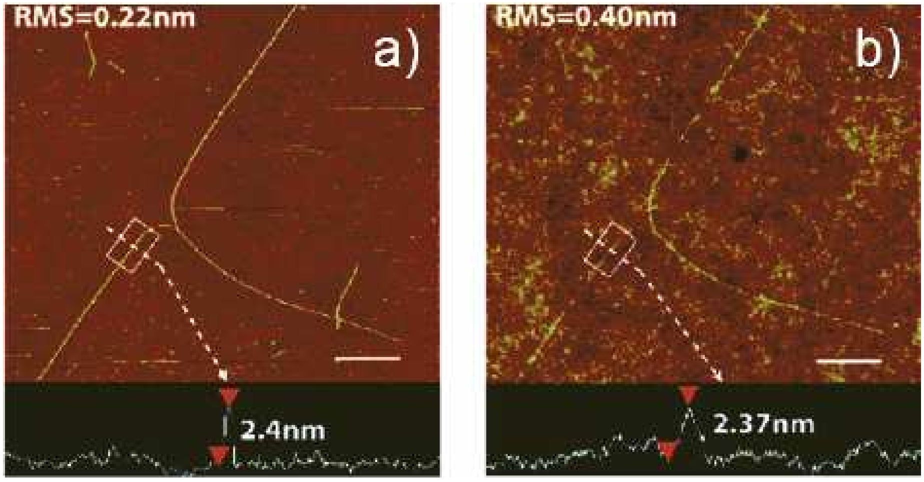

Figure 1.12: Replication of the shape of a carbon nanotube by imprint process by Rogers et al. at the University of Illinois at Urbana-Champagne. The carbon nanotube master is shown in a) and the imprinted replica is shown in b) [37]. *Reprinted with permission from John A. Rogers*.

Challenges of implementing NIL in semiconductor manufacturing include its lower throughput of the existing NIL equipment and difficulties in mold fabrication, due to NIL's nature as a 1x contact patterning process. There is also defectivity concern regarding the contact print nature of the S-FIL process. Several studies are underway to address these concerns, with some manufacturers already developing commercial processes using NIL technology [38].

1.5 BEYOND MICROELECTRONICS

In the five decades since the invention of transistors, innovations in lithography have time and again overcome predictions of "an impossible roadblock to further miniaturization," fueling the microelectronics industry's relentless drive to produce smaller, faster, and cheaper devices. These advances in microelectronics have revolutionized computing and communications technologies and profoundly changed many aspects of modern life. As demonstrated by the evolution of lithography, the combination of economical, strategic, and technical considerations will determine the best lithography solution for future generations of fabrication process.

While the microelectronic industry strives for smaller devices, there are applications that are not well addressed by the conventional microelectronics technology. Macroelectronics is the technology where the electronic devices are distributed and integrated over a large area. The most visible example of macroelectronics is the active matrix flat-panel displays, where the control electronics are required at each display pixel and the pixels may cover an area as large as 1 m^2 [39].

One particular emphasis of the macroelectronics technology is the use of flexible substrates, enabling properties such as flexibility, portability and low-cost. Unlike the rigid substrate of the conventional microelectronics, for example silicon wafers, a flexible substrate allows conformal application of macroelectronic devices onto any physical structure, improves the durability of the devices, and facilitates cost effective production processes such as roll-to-roll printing. Examples of the flexible macroelectronics are shown in Figure 1.13.

Figure 1.13: Examples of flexible macroelectronic applications: flexible display, large aperture radar, and roll-to-roll fabrication process.

The fabrication of electronic devices on flexible substrates is vital to the development of macroelectronic devices. Traditional microelectronics lithography relies heavily on the rigid substrate for precise alignment and overlay control between device layers. New processes and materials are required to address the distortions of the flexible substrate during lithography processing.

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Chapter 2: Step and Flash Imprint Lithography

Step and Flash Imprint Lithography (S-FIL) is a novel nanoimprint lithography (NIL) process that is capable of replicating high aspect-ratio, sub-50 nm patterns. Unlike the earlier NIL techniques that are based on the high pressure and temperature embossing process, the S-FIL process uses a low pressure and ambient temperature molding process to generate the target structures from a low-viscosity UV-curable imprint resist. The simplicity of the S-FIL process and equipment requirements offers a lower cost of ownership compared to other nanolithography techniques.

2.1 NANOIMPRINT LITHOGRAPHY

Nanoimprint lithography (NIL) is one of the potential Next-Generation Lithography (NGL) technologies being developed for the fabrication of sub-50 nm structures. Based on the embossing technique known since the bronze age, the NIL process uses a three-dimensional imprint mold to mechanically deform an imprint medium, creating a negative replica of the mold's design in the imprint material. This imprinted pattern is then further processed to produce the desired structures [1].

Essentially a stamping process, the physical pattern replication process of NIL is not limited by the diffraction of light or the photoresist chemistry, as in optical photolithography. The high resolution patterning capability of NIL is demonstrated in the work by Rogers *et al.* at the University of Illinois at Urbana-Champaign, which showed successful replication of the shape of a 2.4 nm wide carbon nanotube [2] using an imprint process (Figure 2.1). The resolution limit of the NIL process is driven primarily by the minimum feature size on the imprint mold, which is in turn defined by the resolution limit of the template fabrication process. Since a single template can produce a large number of products in a typical NIL manufacturing process, time and resources can be concentrated on the imprint mold fabrication to attain the targeted pattern resolution and quality [3].

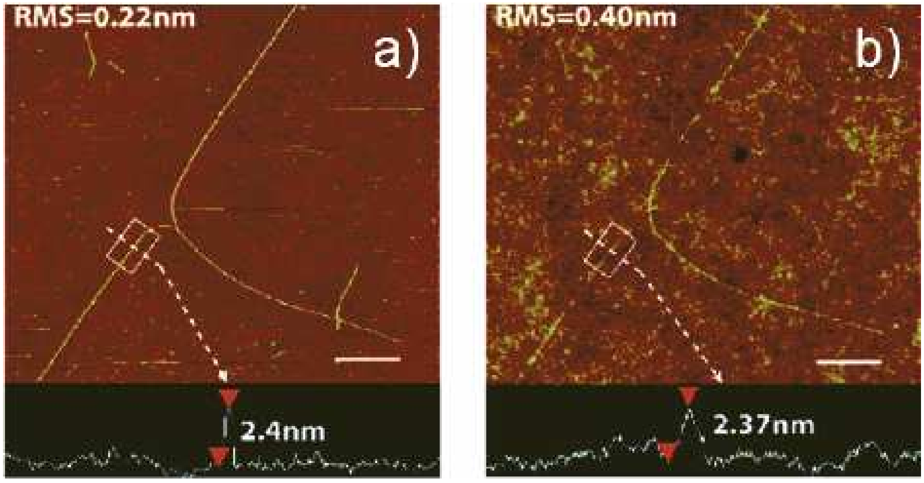


Figure 2.1: Replication of the carbon nanotube shape by an imprint process. The carbon nanotube master is shown in a) and the imprinted replica is shown in b) [2]. *Reprinted with permission from John A. Rogers*.

The use of the physical pattern replication in the NIL process also eliminates the complex projection optics and high energy radiation sources of the conventional photolithography system, significantly reducing the equipment and process costs. The low cost and simplicity of the NIL process, and its demonstrated high resolution patterning capability, makes NIL an attractive technology for many nanolithography applications. Examples of NIL applications under development include patterned magnetic media memory, solid state memory, photonic crystal optical devices, biosensor microarrays, and microfluidic channels [4-7].

Several variations of the NIL technique have been developed in the years since Stephen Chou's demonstration of the NIL concept [1]. The following sections provide an overview of the leading NIL techniques.

2.1.1 Thermal Imprint Lithography

Thermal imprint lithography is the original NIL process described by Stephen Chou in 1995 [8]. In the thermal imprint process (Figure 2.2), a thin layer of thermoplastic polymer is spin coated onto the substrate to serve as the imprint resist. A rigid imprint mold with the desired 3-dimensional patterns is pressed into the thermoplastic polymer film while the polymer film is heated above its glass transition temperature (Tg). The heated polymer softens and deforms to take up the shape of the imprint mold under high pressure. The polymer film is then cooled below Tg and the imprint mold is removed, leaving the patterned polymer on the substrate. A subsequent etch process transfers the embossed patterns from the imprint resist into the substrate, completing the lithography process. Work by Chou *et al.* have demonstrated replication of contact hole arrays 60 nm deep and 10 nm in diameter in poly(methyl methacrylate) imprint resist using the thermal imprint process [9].

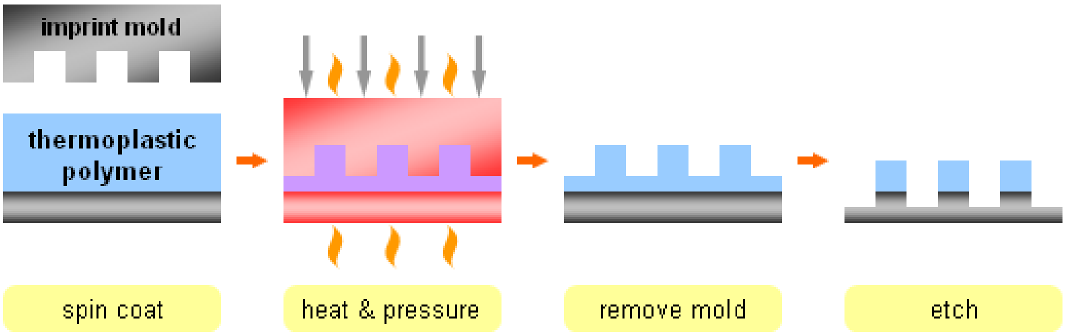


Figure 2.2: Overview of the thermal imprint lithography process.

Thermal imprint lithography provides a simple nanolithography process with low equipment cost and high resolution patterning capability. However, the time required for the highly viscous polymer melt to deform and fully replicate the mold patterns results in low process throughput, especially for high aspect ratio or non-periodic patterns [3]. The high temperature and pressure embossing process also introduces distortions in the polymer imprint resist, caused by the thermal expansion coefficient mismatch between the mold, the thermoplastic polymer, and the substrate layers. The thermal distortions adversely impact the alignment and overlay accuracy between successive layers, an aspect of the patterning process that is crucial to the fabrication of multi-layer devices. Thermal imprint lithography has found applications in fabrication of photonic crystal and microfluidic channel devices, while throughput and alignment limitations have impeded its use in the fabrication of multi-layer devices such as integrated circuits.

2.1.2 Soft Lithography

Soft lithography refers to a group of NIL techniques that use soft conformable imprint molds for pattern replication. Soft lithography was first developed by George Whitesides in 1994 as a simple laboratory technique for producing high resolution structures at extremely low costs [10-11]. In the soft lithography process, a flexible, elastomeric polymer such as poly(dimethylsiloxane) (PDMS) is used as the imprint stamp material. The soft imprint stamp is made by curing the liquid pre-polymer against a patterned master, forming a negative of the master pattern [12]. The soft imprint stamp is then used to pattern the substrate using a variety of techniques such as capillary filling with low viscosity fluid polymer precursors (Figure 2.3A), solvent assisted embossing of polymer films (Figure 2.3B), or contact printing of functional ink compounds (Figure 2.3C).

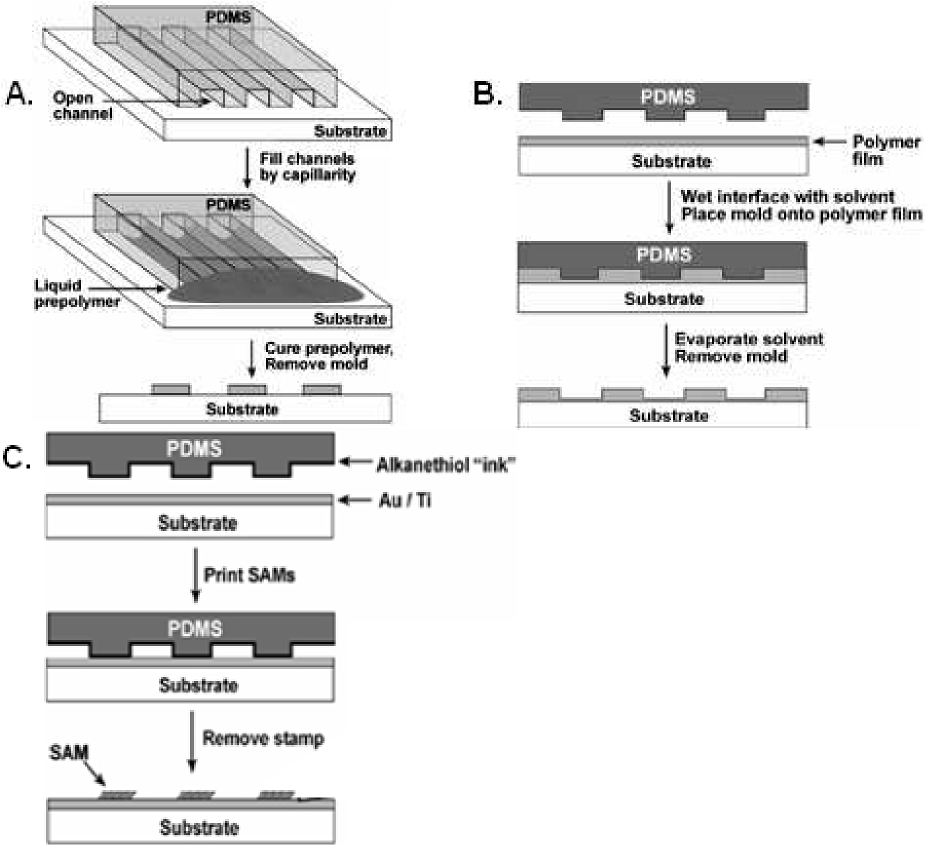


Figure 2.3: Overview of the soft lithography process with various pattern transfer schemes: A. pattern transfer using capillary to fill the PDMS stamp patterns with a low viscosity fluid; B. pattern transfer using solvent assisted embossing of polymer films; C. pattern transfer by contact printing of functional ink materials [13]. *Reprinted with permission from George M. Whitesides.*

The low cost and high resolution capability of soft lithography and the ease of the soft lithography stamp fabrication have led to its use in biosensor microarrays [14-16] and microfluidic channel device fabrications [17-18]. The flexible nature of the elastomeric imprint stamp enables application of soft lithography to pattern non-planar surfaces [19-20]. However, the soft, elastic imprint stamps cannot provide the precise alignment that is required in the fabrication of multi-layer devices common in IC technology [21].

2.1.3 Step and Flash Imprint Lithography

Step and Flash Imprint Lithography (S-FIL) was pioneered by Matthew Colburn and C. Grant Willson to address the alignment limitations of the previous NIL techniques [22]. In the original S-FIL process (Figure 2.4), a rigid transparent imprint template with low aspect-ratio topography is brought into close proximity of a planarized substrate, forming a narrow air gap. A low-viscosity UV-curable imprint resist is introduced at the edge of the air gap and allowed to fill into the gap. Once the imprint resist has completely filled the template patterns, it is exposed to UV radiation through the transparent template, activating a cross-linking reaction to solidify the molded imprint resist. Finally, the template is removed to leave behind an inverse replica of the template relief pattern made of cross-linked imprint resist. A subsequent etch process transfers the molded patterns from the cross-linked imprint resist into the substrate, completing the lithography process. This procedure is repeated field-by-field across the remainder of the substrate, similar to the step-and-repeat photolithography process.

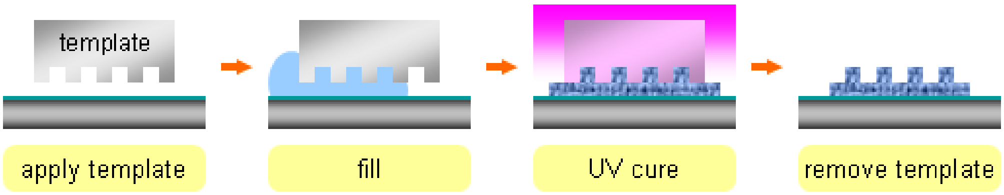


Figure 2.4: Overview of the original Step and Flash Imprint Lithography (S-FIL) process [22].

Similar to the other NIL techniques, the simplicity of the S-FIL process and equipment offers a lower cost of ownership compared to the other next-generation lithography technologies [23]. The S-FIL technology has demonstrated high resolution, sub-50 nm patterning capability [24-25], as shown in Figure 2.5. The use of a low-viscosity UV-curable imprint resist in the S-FIL enables a low pressure and room temperature imprint process, addressing the overlay and alignment limitations of the heated press embossing process in thermal imprint lithography [3]. The rigid transparent imprint template enables the use of existing through-template optical alignment techniques found in conventional photolithography. The rigidity of the imprint template and the low pressure imprint process also minimize template deformation during patterning, further reducing alignment errors in the S-FIL process [26].

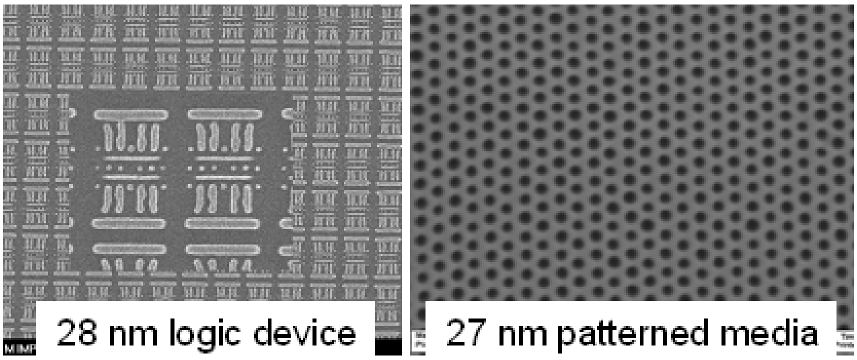


Figure 2.5: High resolution imprinted structures made with the S-FIL process [25]. *Reprinted with permission from Gerard M. Schmid.*

Some of the current challenges of implementing S-FIL in a commercial manufacturing process include concerns about the increased defect liability, difficulties in the fabrication of 1x imprint templates [21, 27], and the comparatively lower throughput of the current S-FIL equipment. Many studies are underway to address these issues, and there are several emerging applications for S-FIL in the patterned media non-volatile memory, solid state memory, and photonic crystal optical devices [4-5], as well as conventional CMOS fabrication [25].

2.2 S-FIL PROCESS DEVELOPMENT

Since its original development in 1999, S-FIL has evolved from a simple laboratory scale nanolithography technique into a production scale nanolithography process, and various production grade tools and materials tailored for a diverse range of applications are now available. In the state-of-the-art S-FIL process (Figure 2.6), a low-viscosity UV-curable imprint formulation (the imprint resist) is dispensed onto the substrate in discrete droplet arrays, instead of a single large drop or a conventional spin coated film, to serve as the patterning medium. A rigid transparent imprint template with the desired three-dimensional relief structures is brought into contact with the imprint resist at minimal pressure and ambient temperature. The low-viscosity imprint resist flows, driven by capillary force to spread out across and fill up the gap between the imprint template and substrate, taking up the shape of the imprint template topography. Once the fill process is complete, the imprint resist is exposed to UV radiation through the transparent template to initiate polymerization and cross-linking reactions, locking in the molded patterns. Once the imprint resist is fully vitrified into a solid polymer film, the imprint template is removed to produce a patterned film with an inverse replica of the template topography. The procedure is then ready to repeat for the next imprint field. Finally, the patterned polymer film is etched by an anisotropic reactive ion etch (RIE) process to transfer the molded patterns into the substrate [26].

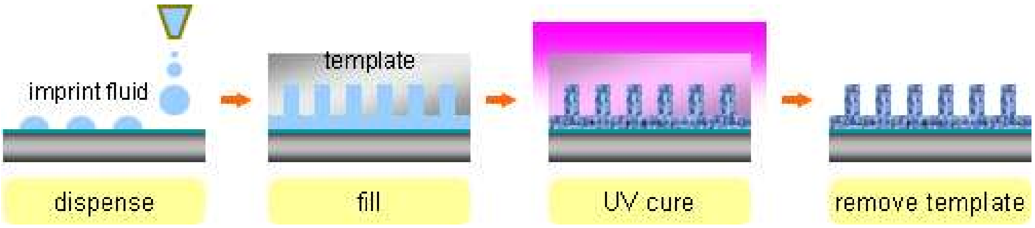


Figure 2.6: Overview of the Step and Flash Imprint Lithography (S-FIL) process.

Successful integration of S-FIL into a production process requires an imprint tool to perform the fluid dispense, template alignment, and UV exposure, a high resolution imprint template with the target features, and an imprint formulation that meets the demands of both the imprint and the etch processes. The following sections will provide an overview of these S-FIL components.

2.3 IMPRINT FORMULATION DISPENSE SYSTEM

In most microlithography technologies, the predominant method of applying the patterning medium such as the photoresist or thermoplastic polymer onto the substrate is the spin coating process. During spin coating, an excess of the patterning medium is placed on the substrate, which is then rotated at high speed in order to spread the fluid by centrifugal force. On a flat substrate, spin coating is capable of producing uniform, adherent, and defect-free film across large surface areas with minimal film thickness variations. The simplicity and consistency of spin coating provides a low cost process with precise control over a wide range of film thicknesses. However, spin coating is an extremely inefficient process, in which most of the initial material is simply flung off the substrate and wasted. In a conventional spin coating setup, more than 90% of the initial material is lost [28], while an improved design such as extrusion spin coating still reports 60% material loss [29].

One of the innovative features of S-FIL technology is its use of an inkjet dispense system instead of the conventional spin coating process (Figure 2.6). In the S-FIL process, the low-viscosity UV-curable imprint resist is delivered as arrays of tiny discrete droplets by piezoelectric inkjets (Figure 2.7) onto the substrate. The template is then brought to close proximity with the substrate and contacts the imprint resist droplet arrays. The array of droplets flows and coalesces driven by the capillary action in the narrow gap between the imprint template and substrate, forming a continuous film and taking up the shape of the imprint template. Thus, the use of the inkjet dispense system permits placement of the required volume of imprint resist precisely where it is needed, effectively eliminating the material waste of the spin coating process [30].

Figure 2.7: A single-point piezoelectric inkjet dispense tip similar to the one installed in the Imprio 55 imprint tool and an example of the inkjet firing fluid droplets [31]. *Image courtesy of MicroFab Technologies Inc.*

For the S-FIL application, the inkjet dispensing system must be capable of producing a drop size of 100 pL or smaller. Smaller drop sizes allow higher resolution in the placement and volume distribution of the fluid within the imprint field. The minimum single drop volume depends on the volatility of the imprint resist, time delay between dispense and imprint, and the design of the inkjet tips [32]. The piezoelectric inkjets used in the S-FIL system have demonstrated drop size as small as 6 pL, and multiple inkjet arrays have been developed to enable parallel dispense of imprint resist and increase the throughput of the inkjet dispense process. The speed of the dispense process is an important factor in minimizing the evaporative loss of the imprint resist and improving the overall S-FIL throughput. Inkjet technology for S-FIL is an active area of research and development.

2.3.1 Residual Layer

The placement and volume of the droplet arrays are important aspects of the control of the fluid volume and distribution within the imprint field, which directly affect the speed of the fluid fill process [33], the thickness and uniformity of the residual layer, and the overall quality of the imprint results. The residual layer is a thin film of the imprint resist that remains at the closest contact areas between the imprint template topography and the substrate. This residual layer is formed during the imprint fill process (Figure 2.8), when the imprint resist coalesces and spreads in the narrow gap between the imprint template and the flat substrate.

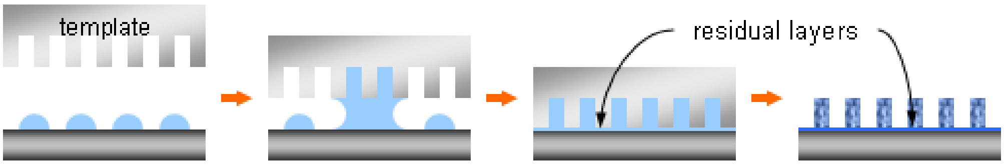


Figure 2.8: Formation of residual layer during the imprint fill process.

Since minimal pressure is applied to the imprint template during the fill process, the flow of the imprint resist is primarily driven by the capillary action of the narrow gap [33] and opposed by the viscous resistance to fluid flow in the same narrow gap space. The effect of the gap distance on the viscous resistance to the fluid flow can be approximated as a laminar flow in a narrow slit and described by the following expression:

$$\frac{\Delta P}{L} = \frac{12\varpi\mu}{B^3 W\rho}$$

where ΔP/L describes the pressure drop due to viscous resistance, B is the distance of the gap between imprint template and substrate, ω is the mass flow rate of the fluid, ρ and μ are the density and viscosity of the fluid, and W is the cross-sectional width of the flow.

As the finite volume of imprint resist continues to spread out and cover more area of the gap, the thickness of the fluid film decreases due to conservation of mass and further narrows the gap between the imprint template and the substrate. As equation 2.1 shows, the decreasing gap distance exponentially increases the viscous resistance to the flow of imprint resist in the gap. Eventually, a balance is reached between the capillary driving force of flow and the viscous resistance to flow; and the imprint fill process stops. The thin film of imprint resist that remains in the narrow gap between the heights of the imprint template topography and the substrate becomes a residual layer of imprint resist following the UV curing and template removal steps.

As Figure 2.9 illustrates, the thickness and uniformity of the residual layer have a significant impact on the quality of the subsequent etch results. A thicker residual layer requires more breakthrough etch to clear out the excess imprint materials, causing additional erosion and faceting of the imprinted patterns. An uneven residual layer causes non-uniform removal of the residual film during the breakthrough etch, resulting in the inconsistent etch transfer of the imprint pattern into the substrate. An ideal residual layer would be thin and uniform across the entire imprinted area to facilitate accurate etch transfer of the imprinted patterns into the substrate.

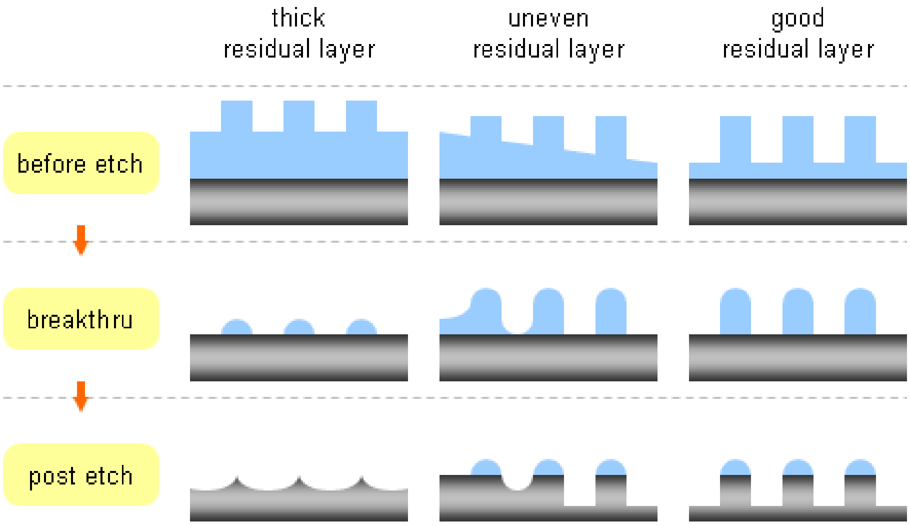


Figure 2.9: Effect of residual layer on imprint resist etch.

2.3.2 Drop Pattern

Since the thickness and uniformity of the residual layer is strongly dependent on the volume and distribution of the imprint resist within the imprint field, the design of the imprint resist dispense pattern, also known as the drop pattern, is critical to the patterning quality of the S-FIL process. A typical drop pattern begins with a design to enhance the spread and coalescence of the imprint resist droplets during the fill process, while avoiding local entrapment of gas bubbles as the droplets fill the patterned area of the imprint template. To achieve a uniform and thin residual layer, the imprint resist drop pattern must also be optimized to account for the feature size, geometry, and pattern density variations in the particular imprint template designs.

Currently, the design and optimization of the imprint resist drop pattern on our laboratory tools is an iterative process, with successive cycles of drop pattern adjustments based on the observed voids, extrusions, or residual layer thickness variations in the test imprints. Figure 2.10 is an example of an iteratively developed drop pattern for the dual damascene S-FIL project. The overall star shape of the drop placements is implemented to reduce gas entrapment by providing escape paths as the imprint resist spreads and the droplets coalesce. The variations in the drop size compensate for the pattern density variations in the particular imprint template design. A well optimized drop pattern may require dozens of iterations and days of test imprints and thickness measurements to produce imprints with low residual layer thickness and good uniformity. Consequently, an automated drop pattern generation program was developed by Molecular Imprints, Inc. to create imprint drop patterns based on the template design and fluid fill simulations. This system has been implemented on production S-FIL tools.

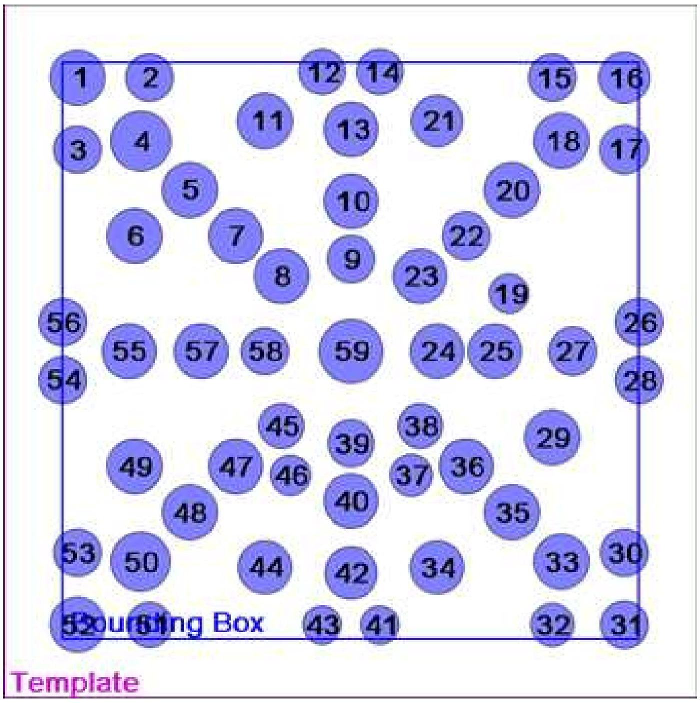


Figure 2.10: A drop pattern design for the dual damascene S-FIL project. The number on each drop location denotes the sequence of drop placement, and the size of the circle correlates to the volume of imprint resist at each drop location.

2.3.3 Alignment

Alignment of lithography images to the previous layer patterns on the substrate is critical to the fabrication of multi-layer structures such as IC devices. The S-FIL process was developed with specific consideration for the necessity of accurate layer to layer alignments. The rigid imprint template and the low pressure and ambient temperature imprint process in S-FIL address the compressive and thermal distortions found in previous NIL techniques [3, 26]. The transparency of the imprint template enables the use of established through mask optical alignment techniques.

The pattern alignment in S-FIL is measured by an interferometric technique [34] that was originally developed for x-ray lithography in 1977 [35]. During the pre-imprint alignment, grating type alignment marks on the imprint template are superimposed in close proximity onto the matching gratings in the previous layer pattern. The overlapping gratings and their multiple diffractions generate an interference pattern known as the moiré pattern. The intensities and positions of the fringes within the moiré pattern correlate to the displacement between the gratings, providing a highly sensitive measure of the template to substrate alignment.

The S-FIL alignment system has undergone many improvements since its original inception, evolving from simple dry alignments with manual correction systems, to the modern in-liquid alignment with automatic correction algorithms. The dry align procedure performs the pattern alignment before the imprint resist dispense, which requires the substrate stage to travel between dispense and imprint locations before the actual imprint is performed. As a result, the accuracy of the dry alignment is reduced by the stage's positional accuracy capability. In contrast, the in-liquid align procedure performs the pattern alignment after the imprint resist dispense, immediately before the imprint fill step and avoid any stage movement inaccuracy. State-of-the-art S-FIL systems have demonstrated 10 nm, 3 sigma alignment capabilities [26], and there are continuing efforts to further improve the alignment accuracy and precision.

2.4 IMPRINT TEMPLATES FOR S-FIL

The imprint templates used in S-FIL contain the master patterns to be transcribed by the imprint process, serving a similar function to the photomasks in optical lithography. The ability to fabricate high resolution and low defect imprint templates is crucial to the implementation of S-FIL in commercial device fabrication processes. Unlike conventional projection photolithography, the physical pattern replication process of S-FIL precludes the use of 4x image reductions and requires the imprint template features to be identical to the target design. Consequently, the resolution and quality of the three-dimensional relief patterns on the imprint templates directly determine the resolution and quality of the S-FIL process, placing heightened demands on the template fabrication process and treatment protocols.

2.4.1 Template Fabrication

S-FIL imprint templates are constructed from rigid, UV-transparent, optically flat, fused silica plates. The three-dimensional relief structures are created using a method similar to the fabrication of phase-shift photomasks for photolithography. Figure 2.11 illustrates an example of the S-FIL imprint template fabrication process [36]. An industry standard fused silica plate (6025 mask blank) is coated with a very thin layer of chromium to serve as a silica etch hardmask, and then a film of resist is coated to serve as the chromium etch mask. The resist is typically patterned using electron beam lithography to provide the high feature resolution required of the imprint template [25]. The exposed electron beam resist is developed to form the desired relief patterns. The resist patterns are then transferred into the chromium and subsequently into the fused silica using reactive ion etch processes to create the desired topography in the fused silica. After the completion of the etch processes, the remaining chromium and resist are stripped off, leaving only the three-dimensional relief of the desired device structures. The depth of the etched features on the fused silica template surface is limited by the maximum reliable aspect ratio of the imprint process, typically 2:1 for the smallest imprinted features [37]. The entire patterning process may be repeated to produce an additional level of structures on the fused silica plate surface [38-39].

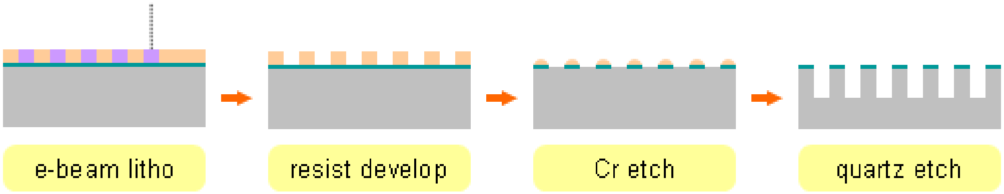


Figure 2.11: Schematic of a Cr based template fabrication process [36].

Once the device patterns have been created, a conventional photolithographic process is used to protect the patterned area of the imprint template with a coat of photoresist, while the surrounding featureless fused silica plate is etched down 15 μm using buffered hydrofluoric acid etchant solution (Figure 2.12). The raised patterned area of the imprint template, known as the template mesa, ensures that only the patterned portion of the imprint template interacts with substrate during the S-FIL process. Finally, the patterned fused silica plate is diced and polished into the 65 mm square form factor that is now the standard for the S-FIL imprint templates.

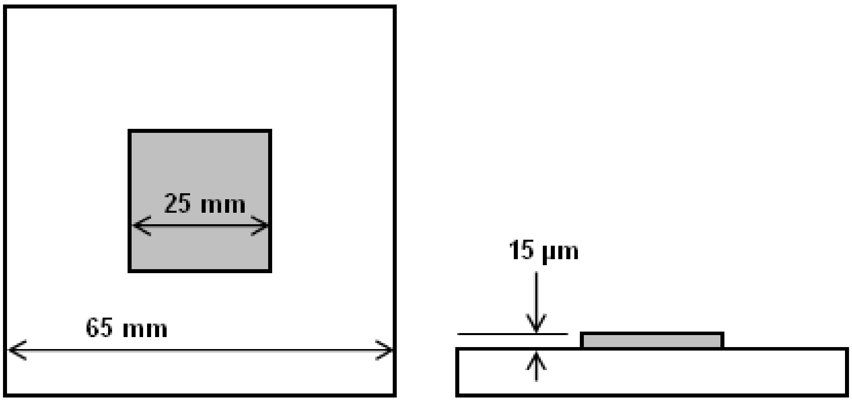


Figure 2.12: Schematic of an S-FIL imprint template, showing the 25 mm x 25 mm patterned device area and the 15 μm mesa offset from the rest of the template surface [40].

An S-FIL imprint template fabrication process was established at the Microelectronics Research Center (MRC) at The University of Texas at Austin in collaboration with SEMATECH, Inc. In the MRC template fabrication process, the fused silica substrate is first coated with 15 nm of chromium using electron beam evaporative metal deposition, then spin coated with 150 nm of an electron beam resist such as the ZEP-520 or PMMA. The electron beam resist film is patterned using a 50 keV Gaussian electron beam lithography tool, then developed in solvent to form the target device patterns. The resist patterns are transferred into the chromium film by reactive ion etch using a chlorine / oxygen etch chemistry. The patterned chromium film is then used as the etch mask for the fused silica reactive ion etch using a CF_4 / helium etch chemistry, creating the desired topography in the fused silica substrate. Subsequent processing completes the fabrication of the S-FIL imprint template. The establishment of the imprint template process at the MRC enables local, rapid productions of imprint templates for use in the various nano-structures research projects on campus.

The similarity between the fabrication of the S-FIL imprint template and a conventional phase-shift photomask has facilitated the development of the template production capability by several commercial photomask suppliers. Several studies have been conducted to improve the resolution and decrease the write time of the electron beam lithography. Template features as small as 18 nm have been successfully demonstrated (Figure 2.13A) using non-chemically amplified electronic beam resists and Gaussian beam electronic beam lithography [41]. An example of an imprint of a 30 nm template pattern into the imprint resist is also shown in Figure 2.13.

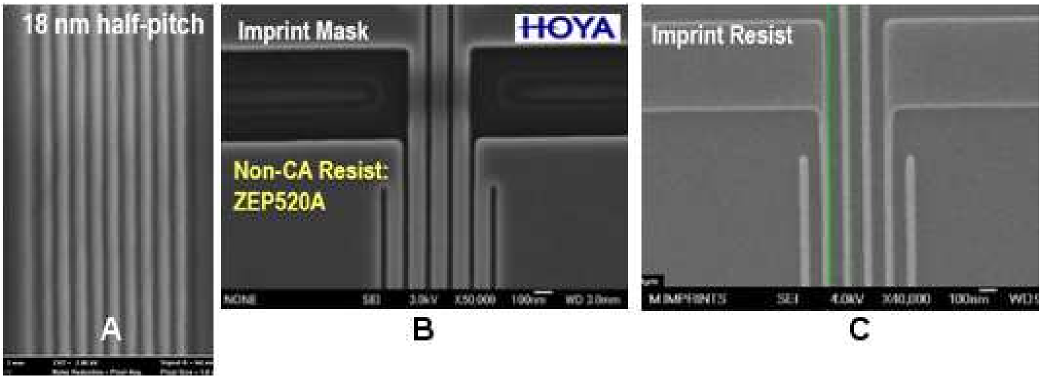


Figure 2.13: A. SEM image of 18 nm half-pitch lines written and developed with the ZEP-520A electron beam resist; B. SEM image of a 30 nm trench pattern in the template; C. SEM image of the same 30 nm line patterns imprinted into the imprint resist [41]. *Reprinted with permission from Gerard M. Schmid.*

2.4.2 Template Separation

The nature of S-FIL necessarily exposes the patterned surface area of the imprint template to the imprint resist and any other process debris during the imprint cycles. As illustrated in Figure 2.14, the separation and release of the S-FIL imprint template from the polymerized imprint resist is crucial to the quality of the imprint patterns. The template separation is initiated by the application of tensile forces on the imprint template away from the substrate, subjecting the polymerized imprint resist to tensile stress. Ideally, a crack would be initiated and propagated along the interface between the fused silica and the polymer, on the often complex topography of the imprint template patterns.

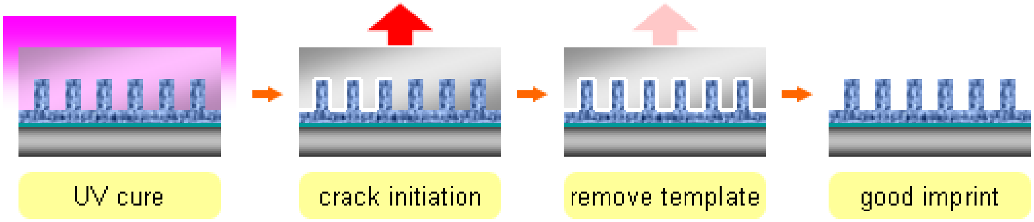


Figure 2.14: Template separation process.

Several failure modes are possible during the template separation process (Figure 2.15), such as cohesive failure in the imprint resist, adhesive failure between the imprint resist and the substrate, and the particulate contamination of the imprint template [42]. These separation failures can generate defects on both the imprinted patterns and the templates, producing poor imprints and potentially fouling the template such that the defects are reproduced in subsequent imprints. Therefore, specialized surface treatment protocols have been developed to mitigate template separation failures and contamination during the imprint process.

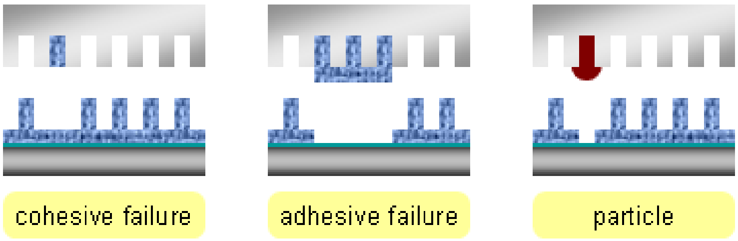


Figure 2.15: Examples of template separation failure modes: cohesive failures of the imprint resist, adhesive failures between imprint resist and the substrate, and particle contamination of the imprint template.

2.4.3 Template Surface Treatment

The most common surface modification technique applies a fluorinated, self-assembled mono-layer (FSAM) onto the S-FIL imprint template. The FSAM reagent (Figure 2.16A) reacts with the free silanol groups on the fused silica template surface in a condensation reaction to form a single layer of perfluorinated alkyl chains [42]. A typical solution phase FSAM treatment process starts with cleaning the template surface with brief low-power oxygen plasma. The cleaned template is then placed in a 0.5~1 wt% solution of FSAM reagent in toluene, covered and left to react for a minimum of 1 hour. The treated template is removed from the toluene solution, rinsed to remove any excess reagent, dried with compressed air, and readied for imprint. The surface mono-layer of perfluorinated alkyl chains decreases the surface energies of the fused silica imprint template and reduces the interactions between the imprint resist polymer and the fused silica template. The reduced interaction between the polymer and the fused silica lowers the interfacial adhesion and encourages separation between the template and the imprint resist.

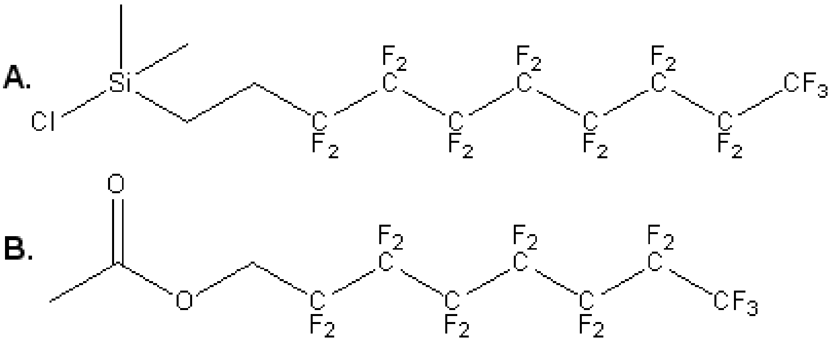


Figure 2.16: A. The fluorinated self-assembled mono-layer (FSAM) reagent, (tridecafluoro-1,1,2,2-tetrahydrooctyl)dimethylchlorosilane. B. The fluorinated surfactant additive, perfluorooctanoate.

The effect and the durability of the FSAM treatments layer have been studied using liquid droplet contact angle, imprint separation force, and x-ray photoelectron spectroscopy (XPS) measurements. The measurement data show that the fluorinated mono-layer coverage and quality are highly dependent on both the FSAM application methods and the imprint resist materials used in the particular S-FIL application. The effect of the FSAM treatments are also found to degrade after repeated imprints, suggesting a breakdown or erosion of the fluorinated mono-layer [43]. Imprint formulations are therefore supplemented with fluorinated surfactants (Figure 2.16B) to replenish the template's FSAM treatments lost during S-FIL process [43-46].

In applications with large open spaces or high aspect ratio features, the ability of the imprint resist to wet and fill the template topography becomes more critical to the success of the patterning process than the separation of the imprint template from the polymerized imprint resist. In these applications, a high fluid contact angle with the treated template surface causes “fluid pinning” to occur at feature edges, slowing or stopping the spread of the imprint resist during the fill process [33, 47]. The fluid pinning effects manifest as slower or incomplete filling of the template features during imprint, which adversely impacts the yield and quality of the S-FIL process. To mitigate fluid pinning, the template surface is treated with different reagents that improve the wetting and lower the contact angle of the imprint resists to the fused silica template surface. Examples of such treatment reagent include hexamethyldisilazane (HMDS) and trimethylchlorosilane (Figure 2.17).

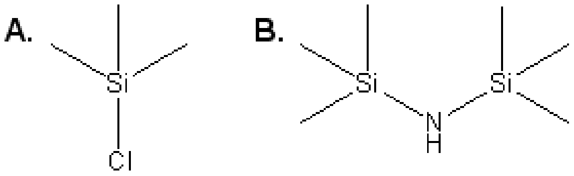


Figure 2.17: Surface treatments reagents to improve wetting and lowers the contact angle of the imprint resists on the fused silica template: A. trimethylchlorosilane; B. hexamethyldisilazane.

Figure 2.18 illustrates the difference in the contact angles and imprint fill results between FSAM and HMDS treated templates. The first row of images are optical measurements of the liquid contact angle of a glycerol droplet on the treated templates. The FSAM treated templates have appreciably larger contact angles. The second row of images are imprints made from the same treated templates, with the HMDS treated template showing significantly improved feature filling compared to the FSAM treated template.

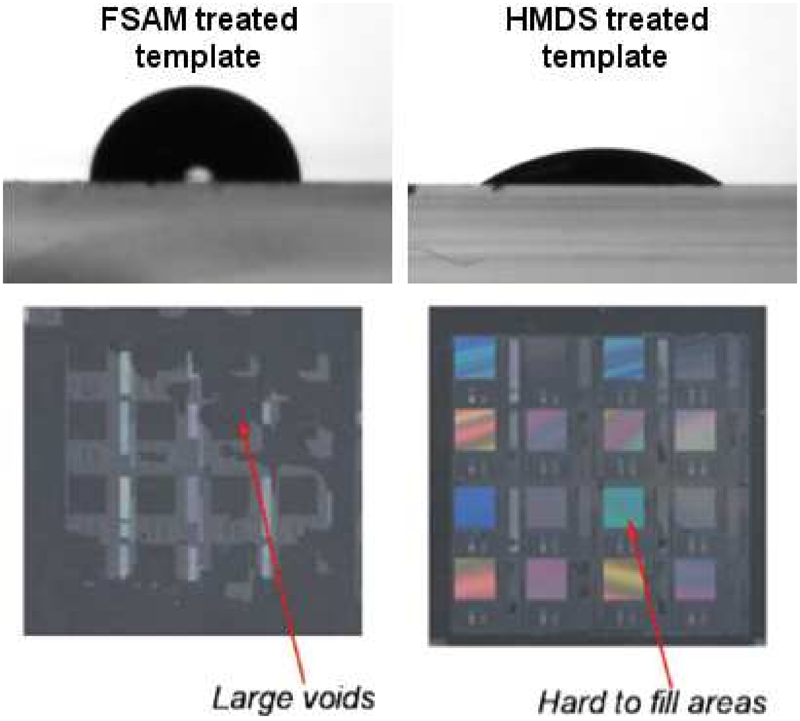


Figure 2.18: Contact angles (top row goniometer images) and imprint results (bottom row optical images [48]) comparisons between FSAM and HMDS treated imprint templates.

2.5 IMPRINT FORMULATIONS FOR S-FIL

The imprint formulations serve as the patterning medium to record the desired device patterns from the imprint templates and transfer the pattern onto the substrates. Consequently, the development of the imprint formulations has significant impact in all aspects of the S-FIL process: the imprint and etch process parameters, the resolution and quality of the imprinted structures, the template and substrate surface treatment chemistry, the defectivity, and the throughput of the overall process.

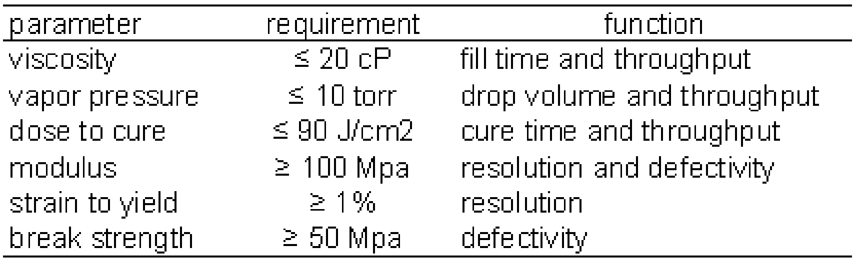
2.5.1 Imprint Resists

The majority of the imprint formulations function as imprint resist, serving functions analogous to the photoresist in the photolithography and etch processes.

During the S-FIL process, the imprint resist molds to the topography of the imprint template and stores the pattern information as three-dimensional relief structures on the imprint resist film. In the subsequent etch process, the imprint resist functions as an etch mask for the transfer of the desired device pattern into the substrate. Once the lithography is complete, any remaining imprint resist is removed from the substrate.

The common S-FIL imprint resist properties include low viscosity, low vapor pressure, low dose to cure, and minimal shrinkage during cure [30, 49]. The low viscosity of the imprint resist is necessary to enable the inkjet dispense technique and the low pressure capillary fill process, hallmarks of the S-FIL technology. The low vapor pressure of the imprint resist allows smaller droplet size to be used in the inkjet dispense, which increases the drop pattern resolution and volume control, and improves the over process throughput. The imprint resist needs to be photocurable with low curing dose and fast curing rate, to enable the ambient temperature imprint process and improve the overall throughput. The imprint resist needs to have minimal volume shrinkage during the polymerization and cross-linking reactions, to prevent pattern distortions and crack formations during the UV curing.

Additionally, good mechanical strength and thermal stability of the UV cured imprint resist film are necessary to maintain the pattern resolution and survive the environmental stress during the imprint and etch processes [30, 49]. Some of the typical imprint resist properties and requirements are listed in Figure 2.19.



parameter	requirement	function
viscosity	≤ 20 cP	fill time and throughput
vapor pressure	≤ 10 torr	drop volume and throughput
dose to cure	≤ 90 J/cm2	cure time and throughput
modulus	≥ 100 Mpa	resolution and defectivity
strain to yield	≥ 1%	resolution
break strength	≥ 50 Mpa	defectivity

Figure 2.19: S-FIL imprint resist properties and typical values [48].

The imprint resists are often formulated from the above process requirements with additional modifications tailored for the specific application. Common imprint resist formulations consist of bulk polymerizable organic monomers, a cross-linking reagent, a photoinitiator, and additional silicon containing monomers, surfactants, or other additives based on application needs. The bulk polymerizable organic monomers typically include acrylates, vinyl ethers, or epoxide monomers (Figure 2.20), which have low-viscosity and can be rapidly polymerized. The cross-linking reagent improves the mechanical strength and the thermal stability of the polymerized imprint resist. The photoinitiator enables the polymerization and cross-linking reaction of the imprint resist by UV irradiation. The silicon containing monomers and surfactants can be added to provide oxygen-etch resistance and improve template separation, respectively.

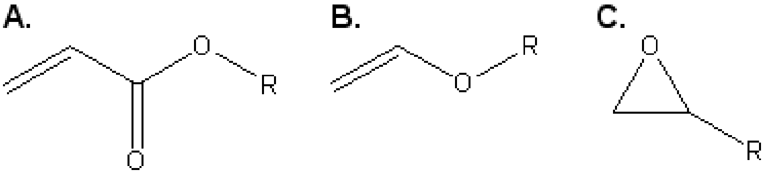


Figure 2.20: Polymerizable functional groups for S-FIL imprint resist formulations: A. acrylate; B. vinyl ether; C. epoxy [50-51].

The imprint resist formulation used in our S-FIL studies consists of 78 wt% of isobornyl acrylate as the bulk monomer, 20 wt% of ethyleneglycol diacrylate as the cross-linker, and 2 wt% of 2-hydroxy-2-methyl-1-phenyl-1-propanone (Darocur 1173) as the UV-photoinitiator (Figure 2.21). All three components are readily available from commercial sources (Sigma-Aldrich and Ciba Specialty Chemicals). The imprint resist is prepared by simply mixing the three components and then filtering with 0.1 µm pore syringe filter.

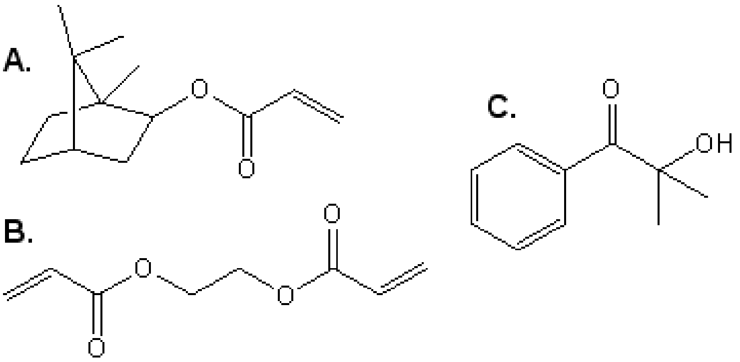


Figure 2.21: Imprint resist formulation: A. isobornyl acrylate (78 wt%, Sigma-Aldrich); B. ethyleneglycol diacrylate (20 wt%, Sigma-Aldrich); and C. 2-hydroxy-2-methyl-1-phenyl-1-propanone (2 wt%, Ciba).

2.5.2 Functional Imprint Materials

Unlike the conventional photolithography process, the physical replication of the imprint mask relief structures in the S-FIL process enables direct patterning of three-dimensional structures [38]. This three-dimensional patterning capability enables the use of functional imprint materials in S-FIL and introduces novel patterning applications. The functional imprint materials are designed to be patterned and remain as a permanent, functional part of the imprinted device, in contrast to the conventional imprint resist which function as the S-FIL equivalent of a sacrificial photoresist. Examples of such new applications are photonic crystals and patterned dielectric materials for CMOS interconnect layers (Figure 2.22) [4-5, 52]. The next two chapters will discuss new imprint material designs and the process development for direct patterning of dielectric materials in CMOS devices.

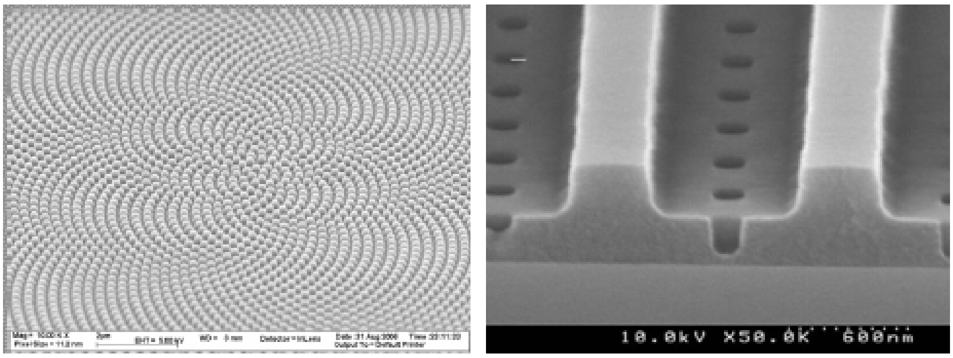


Figure 2.22: Example of functional imprint resist materials applications: A. imprinted photonic crystal array [4]; B. imprinted via and trench structures for dual damascene process [52]. *Reprinted with permission from Gerard M. Schmid.*

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Chapter 3: S-FIL for the Dual Damascene Interconnects Fabrication

An approach to dual damascene processing using Step and Flash Imprint Lithography (S-FIL) in conjunction with novel imprint materials offers the ability to simultaneously pattern two levels of device structures. By using a multi-level imprint template built with both the via and trench structures, one nanoimprint lithography step can produce the same structure that would otherwise require two photolithography steps, greatly reducing the number of patterning steps required to build interconnect structures.

Two approaches are being explored for the implementation of S-FIL in the dual damascene process: sacrificial imprint materials and imprintable dielectric materials. The sacrificial imprint material enables the simultaneous patterning of both via and trench structures by serving as a three-dimensional etch mask for the patterning of CVD, low-k insulator materials in the subsequent etch process. The imprintable dielectric material strategy takes this one step further, combining the patterning of interconnect structures and the application of the dielectric material into one process step. This offers the potential to further streamline the dual damascene process.

3.1 INTERCONNECTS

In integrated circuit (IC) fabrication, the various semiconductor circuit elements such as diodes, transistors, resistors and capacitors need to be interconnected to form the desired electrical circuits and devices. The metal wirings that provide the electrical connectivity amongst the transistors within the IC chip and connect those transistors to systems outside the IC chip are known as interconnects (Figure 3.1). The creation of the metal wiring and the dielectric insulation between the wiring are commonly referred to as the Back End of Line (BEOL) portion of the IC fabrication process.

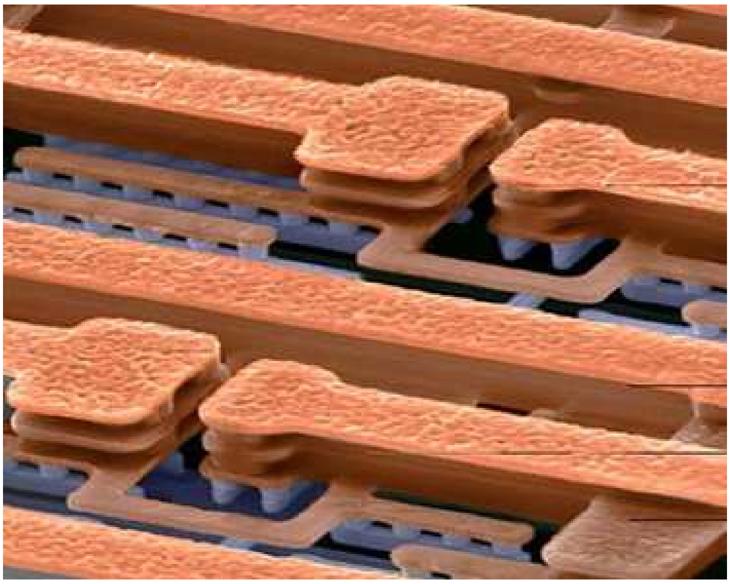


Figure 3.1: Metal interconnects in an integrated circuit device [1]. *Image courtesy of IBM.*

3.1.1 Early Interconnect Designs

The concept of metal lines built into the monolithic integrated circuits was first invented by Robert Noyce in 1959 [2]. By replacing the “flying-wire” connections of the earlier IC designs with the metal lines deposited on top of the protective oxide coating, complete electrical circuits could be built on a single silicon chip. The incorporation of metal line interconnects into monolithic integrated circuits enabled a practical method to mass produce solid state integrated circuits (Figure 3.2).

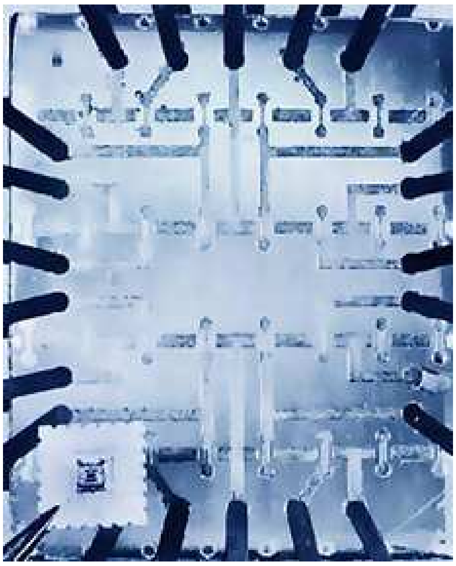


Figure 3.2: Early 16-transistor MOS integrated circuit (lower left) held in front of an enlarged image of the IC [3]. *Image courtesy of RCA Inc.*

Early monolithic integrated circuits were large size devices, allowing sufficient area between the circuit elements to route the metal wiring in a single plane (Figure 3.2). As the microelectronics industry continued to drive for smaller transistors and packed more devices into a smaller area, the size of the metal wiring decreased while the density and complexity of the wiring increased accordingly. By the 1980s, shrinking device size outpaced the reduction in the interconnect size, leaving insufficient space for single plane interconnects and limiting the size of the IC device [4]. Analogous to the vertical building development in high density urban areas, the limitation of the single plane interconnect design was overcome by the introduction of the multi-level interconnect scheme [4].

3.1.2 Multiple-Level Interconnects

The multiple levels of wiring enabled intricate interconnect designs to accommodate the ever increasing device density and complexity. The wiring levels (also known as the metal levels or trench levels) are isolated from each other by an interlayer dielectric (ILD) material, which provides both the electrical insulation and mechanical support between the metal wires. The connections between the wiring levels are made by arrays of vertical connections known as vias. Each pairing of a metal wire level and its corresponding via level is collectively known as a layer (Figure 3.3).

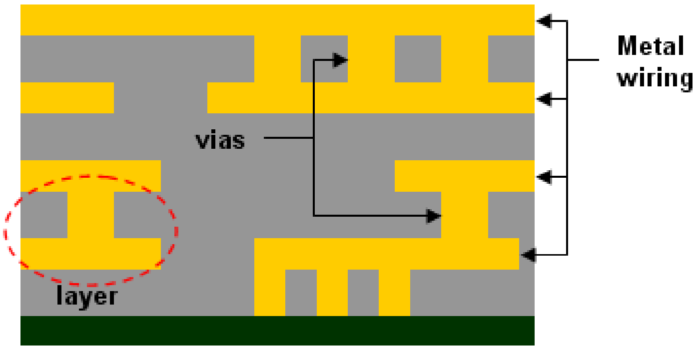


Figure 3.3: Cross sectional view of a multi-level interconnect structure. The metal interconnects are shown as the yellow structures, with several metal and via levels. The levels are isolated from each other by the ILD materials in grey.

As the transistor size and density continues to scale exponentially with time, the complexities and levels of wiring necessary to interconnect microelectronic devices continues to grow. State-of-the-art microprocessors require nine or more levels of interconnect wiring, and the fabrication of interconnects plays an increasingly significant role in the overall cost and performance of IC devices [5].

3.1.3 Aluminum Interconnects

Until recently, IC interconnects were predominantly made of aluminum (Figure 3.2), using a subtractive metallization technique [4]. In the subtractive aluminum process (Figure 3.4), a blanket film of aluminum is first deposited onto the substrate, patterned with conventional photolithography, and then etched to remove the unneeded regions of the aluminum film; producing the desired aluminum wire pattern. A film of dielectric material is then deposited over the exposed aluminum wiring to provide the electrical insulation and mechanical support between the wires. The process is then repeated for each successive level of via and metal structures to complete electrical circuits and devices.

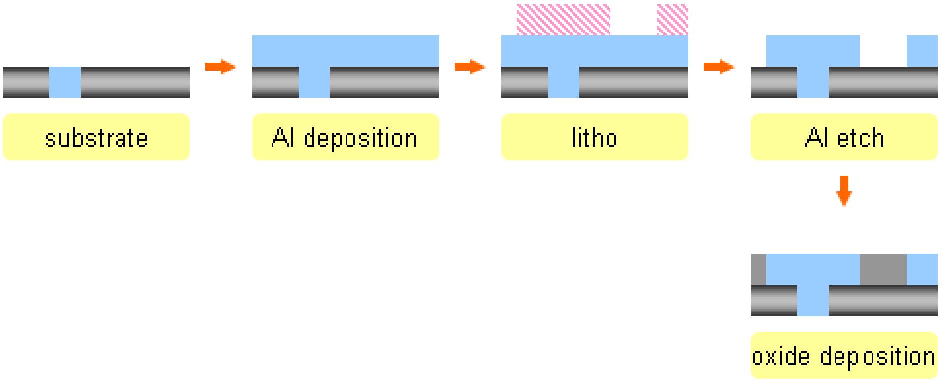


Figure 3.4: Overview of the subtractive aluminum metallization process.

The aluminum interconnects enable a simple fabrication method that is compatible with the semiconductor manufacturing process. However, as the modern microelectronic devices continue to shrink in size and grow in transistor density, the size of the interconnect wires necessarily decreases and the number of interconnect levels increases. The effects of the smaller interconnect wires can be approximated by the following expression:

$$R = \rho \cdot \frac{L}{A}$$

where R is the resistance of the wire, L is the distance of the wire, ρ is the electrical resistivity of the wire material, and A is the cross sectional area of the wire.

As equation 3.1 shows, the combined effects of the smaller interconnect wires and longer wiring distances from the larger number of interconnect levels translate into an increased electrical resistance of the interconnect wires. The larger electrical resistance, in turn, increases the RC delay within the microelectronic devices, adversely limiting the signal propagation rate and processing speed of the device. To mitigate the increasing interconnect resistance and the RC delay limitation, copper interconnects were developed to take advantage of copper's lower electrical resistivity (1.72×10^{-8} Ω·m) compared to that of aluminum (2.82×10^{-8} Ω·m) [6].

3.1.4 Copper Interconnects

The first fully integrated CMOS device with copper interconnects was demonstrated in 1997 at IBM, using a damascene metallization technique [7]. In the copper damascene process (Figure 3.5), a blanket film of dielectric material is first deposited onto the substrate, patterned with conventional photolithography, and then etched to create the trenches and/or holes for the desired wiring patterns. A film of copper material is then deposited onto the patterned dielectric film and polished to form the copper interconnect structures. The process is then repeated for each successive level of via and metal structures to complete electrical circuits and devices.

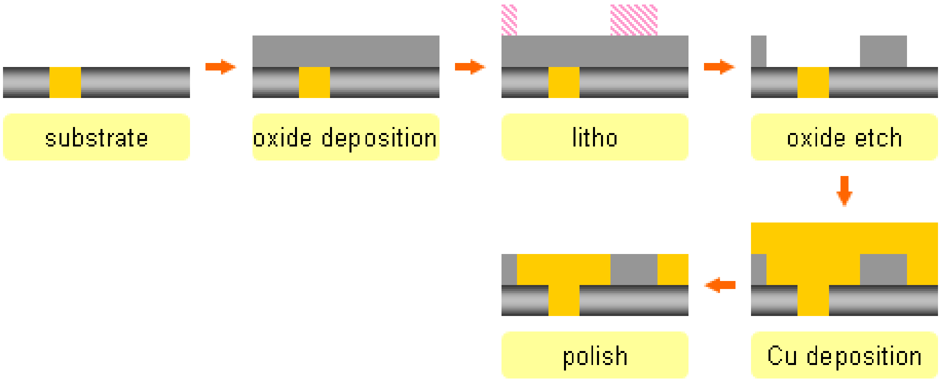


Figure 3.5: Overview of the copper damascene metallization process.

In addition to the lower electrical resistivity and the reduced RC delay, the use of copper interconnects also improves the electromigration resistance of the IC devices. Electromigration is the material transport in electrical conductors due to the momentum transfer between the conducting electron flow and the diffusing metal atoms, causing the metal conductor to change shape and bringing about the eventual loss of electrical connection [8]. Electromigration decreases the reliability of IC devices as the device size shrinks and current density increases. The use of alloyed copper interconnect wiring improves the electromigration resistance of the device due to the higher electromigration activation energy levels of copper, which is in turn caused by copper's superior electrical and thermal conductivity as well as its higher melting point [8-9].

The use of the damascene metallization technique also enables cost reduction in the BEOL process. In the "single damascene" process (Figure 3.5), the dielectric material is deposited, patterned, and etched before the deposition of the metal conductor material. The process is then repeated for each level of vias and metals. However, it is possible to define both via and metal structures in one dielectric film before the deposition of copper, resulting in the simultaneous formation of both via and metal levels (Figure 3.6). Such a "dual damascene" process reduces the number of lithography steps required to complete the interconnect structures and lowers the cost of the BEOL process.

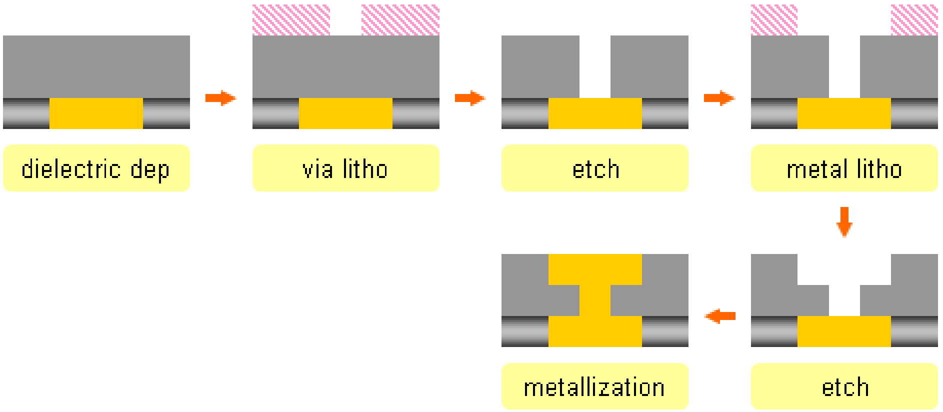


Figure 3.6: Overview of the copper dual damascene process.

The combination of a modest decrease in electrical resistivity, improvement in electromigration resistance, and reduction in process cost drove full-scale development and implementation of copper interconnect technologies for high performance microelectronic devices (Figure 3.1). Today, copper dual damascene processes continue to be the state of the art for the semiconductor BEOL fabrication.

3.2 MULTI-LEVEL S-FIL FOR DUAL DAMASCENE

As the microelectronics industry continues to drive for smaller transistors and higher device density to pack more functionality into a smaller area, the complexity of the wiring and the number of interconnect layers continues to grow. A modern microprocessor contains as many as nine layers of interconnect wiring and vias [10], and the performance and cost of the BEOL process becomes increasingly important as a result. As a physical patterning process, S-FIL has demonstrated replication of three dimensional structures into the imprint material [11]. Therefore, an approach to the BEOL dual damascene process using S-FIL with an imprint template built with both via and metal level patterns would enable the simultaneous patterning of both via and metal structures into the substrate (Figure 3.7). The replication of the dual damascene structures in one S-FIL step instead of two photolithography steps reduces the number of process steps in the interconnect fabrications and lowers the overall BEOL cost [12].

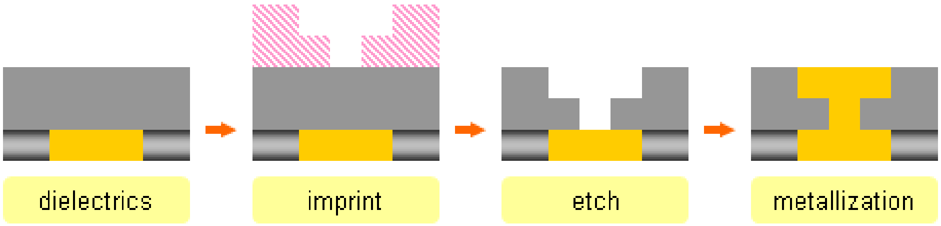


Figure 3.7: Example of a copper dual damascene process with multi-level S-FIL [5].

3.2.1 Multi-Level S-FIL Process

Figure 3.7 provides an example of the dual damascene process using multi-level S-FIL. Similar to the conventional dual damascene process (Figure 3.6), the multi-level

S-FIL process starts with a substrate with a film of deposited dielectric material. The substrate is imprinted in one S-FIL step to produce an imprint resist with three dimensional relief patterns of both the metal and via level structures. The patterned imprint resist acts as an etch mask, transferring both the metal and the via level structures into the dielectric film in a reactive ion etch (RIE) process. Lastly, the copper is deposited into the etched metal and via level structures in the dielectric film, producing the same final dual damascene structure as that of the conventional photolithography process (Figure 3.6-3.7).

Successful integration of a multi-level S-FIL patterning process into the dual damascene fabrication flow requires imprint tools to perform the S-FIL process, dual damascene templates with both the metal and via structures, an etch process that can accurately transfer the imprinted metal and via structures into the dielectric substrate, and imprint materials that meet the demands of both the imprint and the etch processes. The imprint tools and templates are both commercially available. For the development of the multi-level S-FIL process, imprints were made using the Molecular Imprints' Imprio 55 and Imprio 100 S-FIL equipment. The dual damascene S-FIL templates were designed in collaboration with the Advanced Technology Development Facility (ATDF) in Austin, TX, and made by Toppan Photomask [5].

3.2.2 Dual Damascene Template

The dual damascene S-FIL template consists of both via 1 and metal 2 interconnect structures and is intended for use with patterned metal 1 wafers prepared by ATDF. The template design incorporates learning from previous templates with multiple level features [13-14], and includes standard BEOL electrical test structures such as via chains, SEM arrays, and serpentines lines, etc. Each test structure is repeated at several dimensions, ranging from 2000 nm to 120 nm. Eight duplicates of the test patterns are included on each template, covering a total patterned area of 25 mm x 25 mm (Figure 3.8). Unused spaces between the structures are filled with dummy features to minimize pattern density variation and improve CMP uniformity. The via and metal interconnect structures were patterned by Toppan Photomask [14], using a process similar to that of the commercial phase-shift photomask technology (Figure 3.9). The template mesa definition and dicing were done by Molecular Imprints. The cleaning and surface treatment of the dual damascene templates follow the standard S-FIL template protocols (chapter 2, section 4).

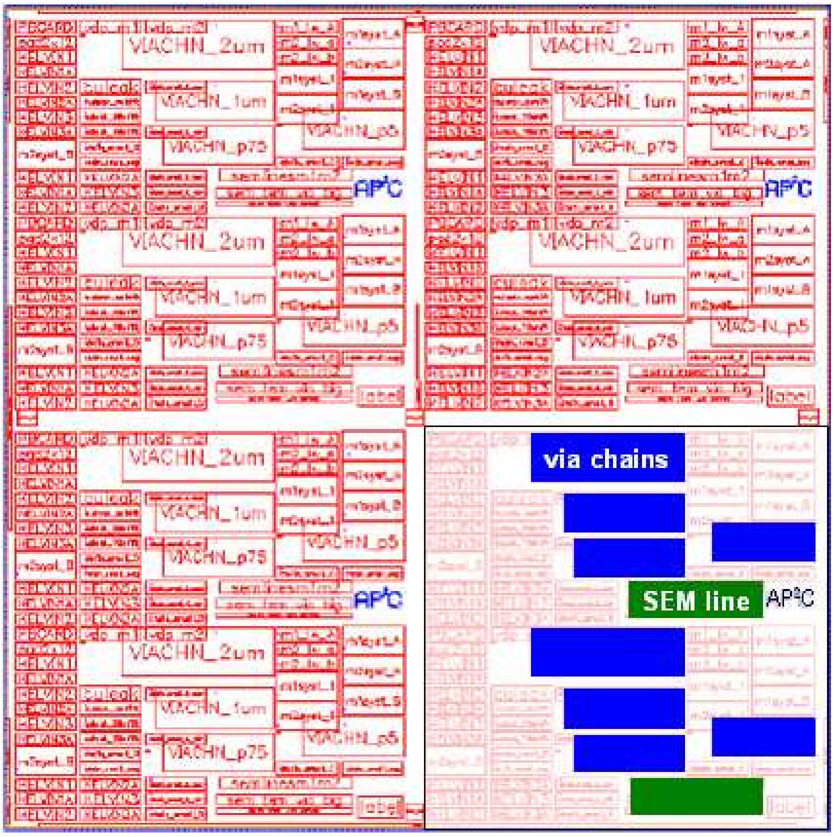


Figure 3.8: The ATDF 811AZ dual damascene template layout, containing both via 1 and metal 2 structures. Each quadrant of the template is a duplicate of the test design. The key via chains and SEM test structures are highlighted in the lower right quadrant. *Image courtesy of ATDF.*

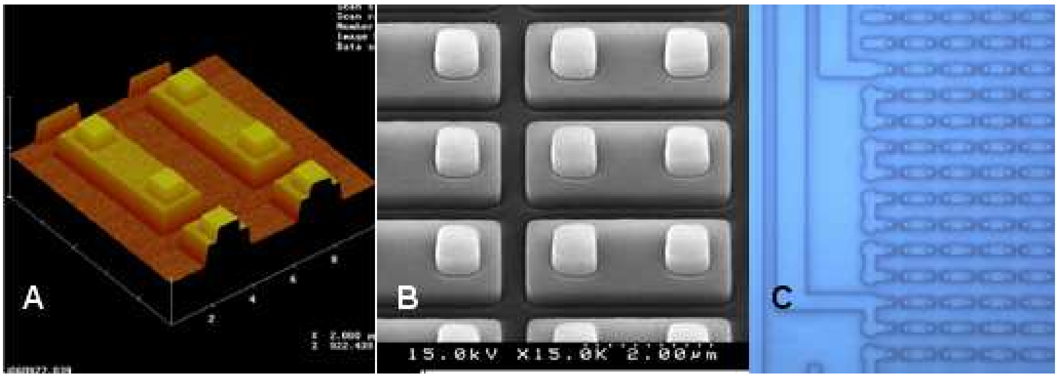


Figure 3.9: AFM (A), SEM (B), and optical microscope (C) images of the via chain structure on the dual damascene S-FIL template, showing both metal and via levels of the interconnect structures. *Images courtesy of Toppan Photomask.*

3.2.3 Imprint Materials for Multi-Level S-FIL

Two imprint material designs were explored for the implementation of S-FIL in the dual damascene process: sacrificial imprint materials and imprintable dielectric materials. The sacrificial imprint material stores the dual damascene structures as three dimensional relief patterns during the imprint step and then functions as an etch mask during the subsequent dielectric etch steps. This allows the simultaneous patterning of both via and metal structures, reducing the number of lithography operations in a dual damascene process. The development of sacrificial imprint material will be presented in the remainder of this chapter.

The imprintable dielectric material also stores the dual damascene structures as three dimensional relief patterns during the imprint step, but is converted into a permanent dielectric material with suitable post-imprint processing. The use of imprintable dielectric material combines the patterning of via and metal interconnect structures and the application of the dielectrics, further streamlining the dual damascene process. The development of imprintable dielectric material will be presented in chapter 4.

3.3 SACRIFICIAL IMPRINT MATERIAL

The development of the sacrificial imprint material (SIM) and the associated process aims to evaluate the feasibility of integrating S-FIL into the copper dual damascene technology. In the SIM process (Figure 3.10), the substrate is first coated with a layer of dielectric material. The dielectric coated substrate is patterned using S-FIL, where the metal and via interconnect design from the dual damascene template is stored as three dimensional relief patterns in the SIM film. The imprinted substrate is then etched with a RIE process to transfer the dual damascene structures into the dielectric material, using the patterned SIM film as a three dimensional etch mask. In effect, the sacrificial imprint material provides analogous functions to the conventional photoresists. The use of S-FIL with SIM enables the patterning of both via and metal structures in one S-FIL step, compared to the two separate photolithography steps of the conventional dual damascene process. The SIM approach also retains full use of the existing dielectric material and technologies, with no new material becoming a permanent part of the device.

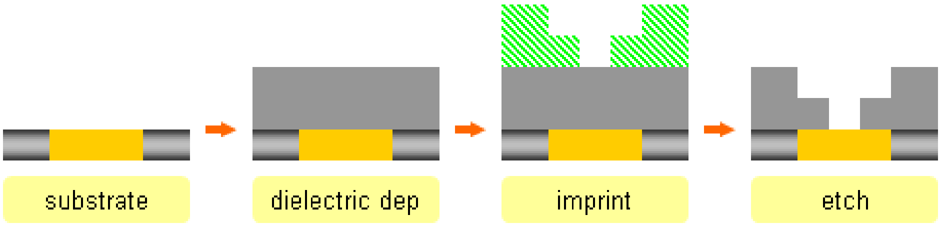
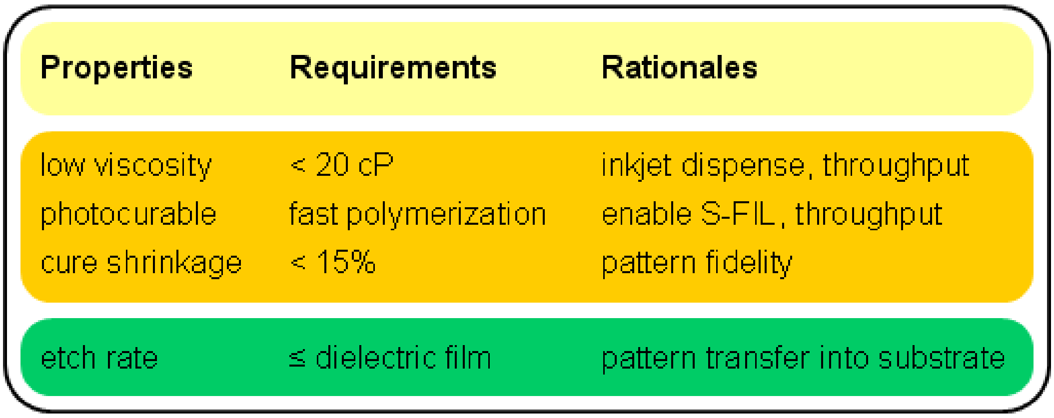


Figure 3.10: Overview of the multi-level S-FIL with sacrificial imprint material.

3.3.1 Sacrificial Imprint Material Formulation

In order to function effectively as both the imprint medium and the etch mask, the SIM formulation needs to meet the requirements of both the S-FIL and etch processes. As summarized in Figure 3.11, the S-FIL process requires an imprint formulation with low viscosity, fast photo polymerization rate, and minimal volume shrinkage during polymerization. The etch process requires the polymerized SIM film to have an etch rate equal to or lower than the etch rate of the dielectric substrate material. The dielectric materials used for the SIM process development were the industry standards, Black Diamond from Applied Materials and Coral from Novellus. These are proprietary doped SiO_2 materials deposited by chemical vapor deposition (CVD) process.



Properties	**Requirements**	**Rationales**
low viscosity	< 20 cP	inkjet dispense, throughput
photocurable	fast polymerization	enable S-FIL, throughput
cure shrinkage	< 15%	pattern fidelity
etch rate	≤ dielectric film	pattern transfer into substrate

Figure 3.11: Overview of the SIM formulation requirements.

Development of the SIM formulation started with a two-component system consisting of an organic monomer and a silicon containing cross-linker. The organic monomer has higher resistance to the dielectric etch process, while the silicon containing cross linker has lower etch resistance. By varying the ratio of the two components in the SIM formulation, the etch rate of the SIM could be tuned to match the etch rate of the dielectric material and optimize the transfer of the imprinted structures into the substrate.

Several organic materials were evaluated for their application as the organic monomer component of the SIM formulation. The etch rates of films of the organic materials in a standard Black Diamond etch condition were measured at ATDF and compared against that of the dielectric materials. Of the organic materials tested, poly(isobornyl acrylate) and poly(vinyl acetate) had the highest etch rates, ~22 Å/s for poly(isobornyl acrylate) and ~25 Å/s for poly(vinyl acetate); but their etch rates were still well below the 40 Å/s etch rate of the Black Diamond (Figure 3.12). Isobornyl acrylate was picked for its known compatibility with the S-FIL process and good miscibility with the silicon containing cross-linker.

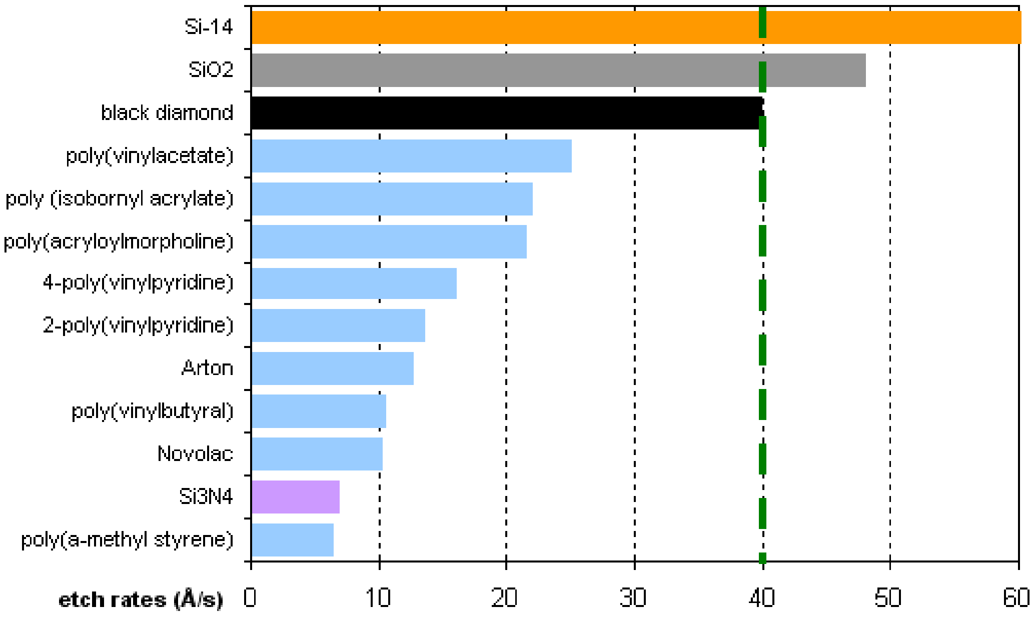


Figure 3.12: Etch rates of SIM component candidates in the standard Black Diamond etch process.

The silicon containing cross-linker candidate for the SIM formulation, a branched poly(dimethyl siloxane) known as Si-14 (Figure 3.13) was synthesized by my colleagues [15]. It is a low viscosity (<20 cP) and low vapor pressure liquid at room temperature, that readily undergoes radical polymerization with high polymerization reactivity and is well-suited for the S-FIL process. Si-14 contains high amount of silicon (33 wt%) comparing to other existing silicon containing imprint materials, giving it a high etch rate in the Black Diamond etch condition.

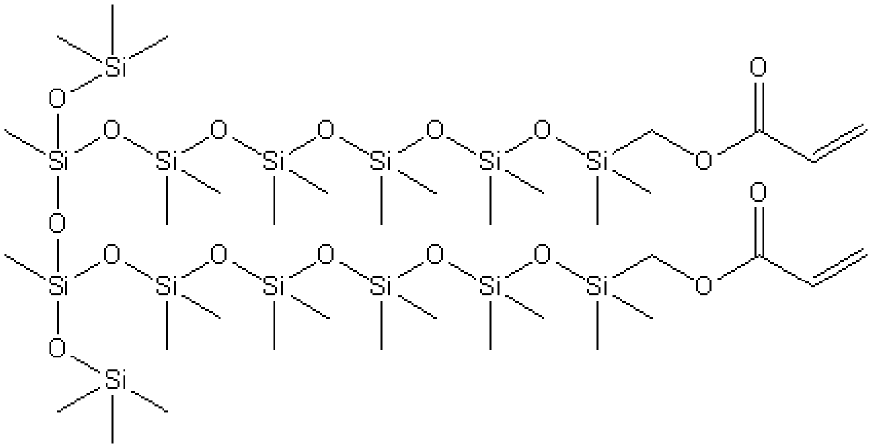


Figure 3.13: The branched poly(dimethyl siloxane) cross-linker, Si-14 [15].

Several SIM formulations with different ratios of the Si-14 to isobornyl acrylate were made and their etch rates characterized (Figure 3.14). From the etch simulation, it was found that for a one step etch process, a low SIM etch rate would result in the via punching through the entire dielectric layer before the metal structures could be properly etched into the dielectric. Conversely, a high SIM etch rate would result in a reduction in the feature aspect ratio, effectively flattening the etched dual damascene structures (Figure 3.15). The etch model was experimentally verified with etch tests of different SIM formulations (Figure 3.16). Based on these data, it was concluded that a one-step etch process requires matching the etch rate of the SIM and the dielectric material in order to accurately transfer the dual damascene pattern from the imprinted SIM into the dielectric substrate.

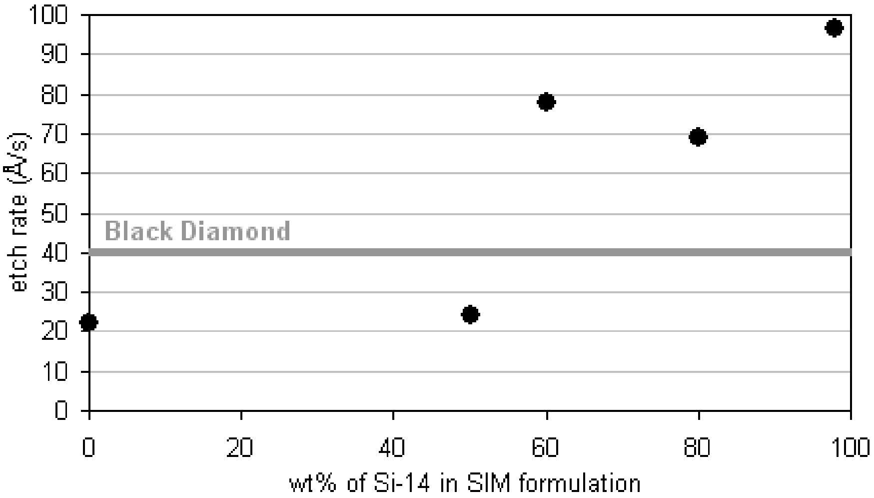


Figure 3.14: Etch rates of different ratios of Si-14 / isobornyl acrylate SIM formulations.

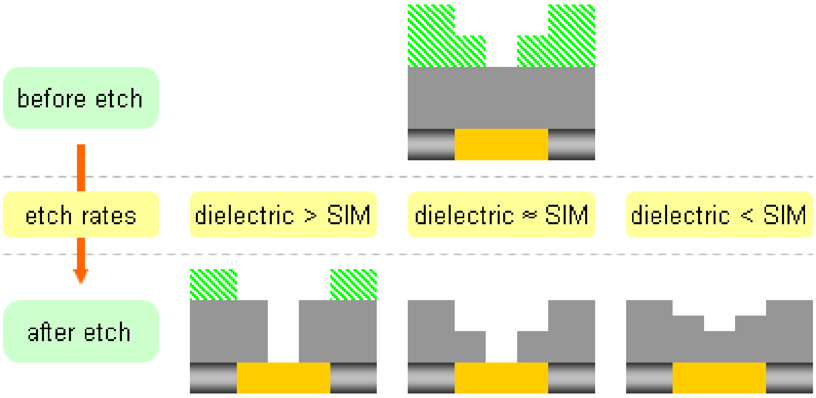


Figure 3.15: The effects of the SIM etch rates on the quality of the etched dual damascene structures, using a single-step etch process.

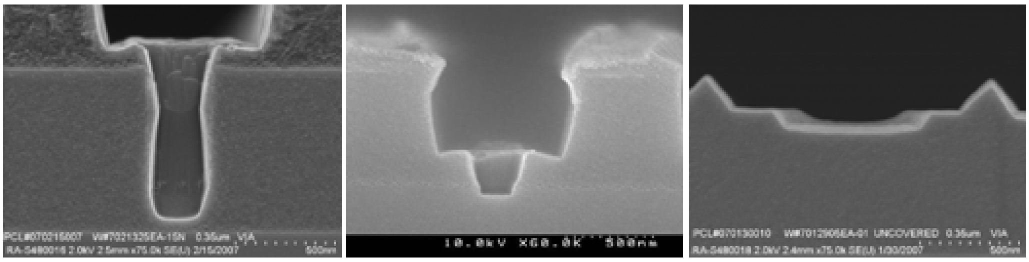


Figure 3.16: Cross section SEM image of etch results with different ratios of Si-14 / isobornyl acrylate SIM formulations. From left to right, high SIM etch rate, optimized SIM etch rate, low SIM etch rate.

However, a multi-step etch process provides additional control of the pattern transfer etch process, allowing the use of SIM materials with an etch rate equal to or less than that of the dielectric material (Figure 3.17). The relaxed etch requirement on the SIM enabled a simplification of the SIM formulation, removing the need for these custom synthesized, low etch resistance silicon containing component.

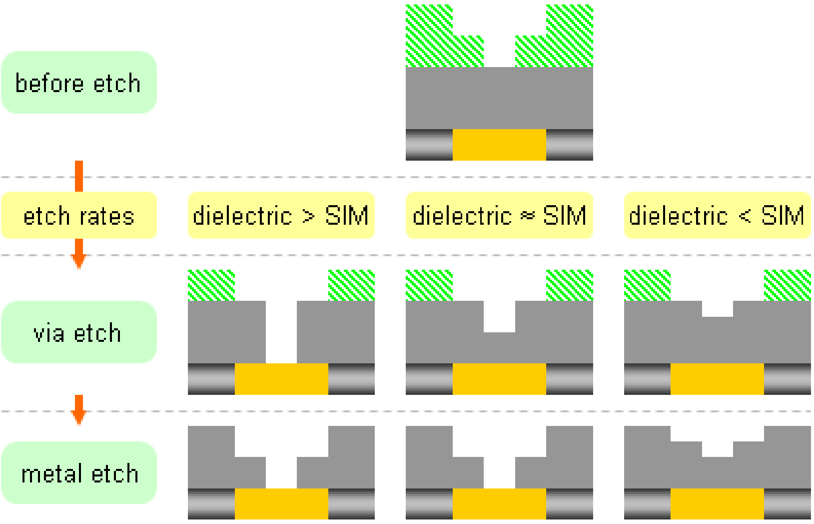


Figure 3.17: The effects of the SIM etch rates on the quality of the etched dual damascene structures, using a multi-step etch process.

Based on the evaluation of many candidate materials, the functional SIM formulation was set to consist of 78 wt% of isobornyl acrylate as the bulk monomer, 20 wt% of ethyleneglycol diacrylate as the cross-linker, and 2 wt% of 2-hydroxy-2-methyl-1-phenyl-1-propanone (Darocur 1173) as the UV-photoinitiator (Figure 3.18). All three components are readily available from commercial sources (Sigma-Aldrich and Ciba Specialty Chemicals). This SIM formulation is prepared by simple mixing the three components and then filtered with 0.1 µm pore syringe filter. It was used for all subsequent SIM imprint and etch process development and functional device testing.

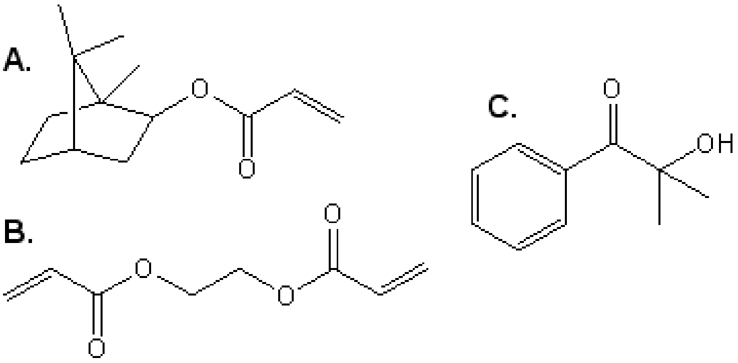


Figure 3.18: Functional SIM formulation: A. isobornyl acrylate (78 wt%, Sigma-Aldrich); B. ethyleneglycol diacrylate (20 wt%, Sigma-Aldrich); and C. 2-hydroxy-2-methyl-1-phenyl-1-propanone (2 wt%, Ciba).

3.3.2 Imprint Process Development

Imprint of the dual damascene structures in SIM utilizes the standard S-FIL procedure (chapter 2 section 2) in conjunction with dual damascene templates. Compared to the conventional single-level S-FIL imprints, the dual damascene imprints contain larger and deeper spaces, which requires dispensing a higher volume of imprint material (Figure 3.19). The higher imprint material volume requires additional efforts to optimize the template back pressure, the imprint material drop pattern, and the imprint fluid spread time, in order to produce a good imprint quality with good residual layer thickness and uniformity control.

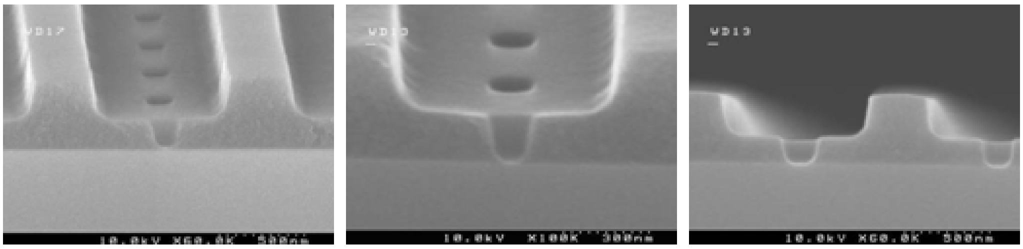


Figure 3.19: Imprints of the dual damascene template in SIM, showing both the metal level trench and via level holes.

The template back pressure slightly bows the S-FIL template during imprint (Figure 3.20). A higher template back pressure (Figure 3.21A) bows the template convex and generates concave imprints, while lower template back pressure (Figure 3.21B) bows the template concave and generates convex imprints [16]. A slightly convex template shape is preferred during the imprint fill step. The convex surface curvature facilitates capillary flow and coalescence of the low viscosity imprint material from the center to the edge of the template, thereby improving the fill speed and reducing air entrapment during fill, but the curvature also results in residual layer thickness variations in the imprinted patterns. Production S-FIL tools minimizes the template induced residual layer variations by dynamically modifying the shape of the template during imprint process, reducing its curvature as the imprint fluid spread progress during an imprint. Our laboratory S-FIL tools do not have this capability, so we had to set the template curvature and setting was utilized during the entire process.

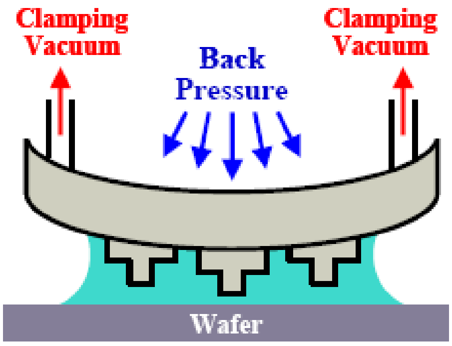
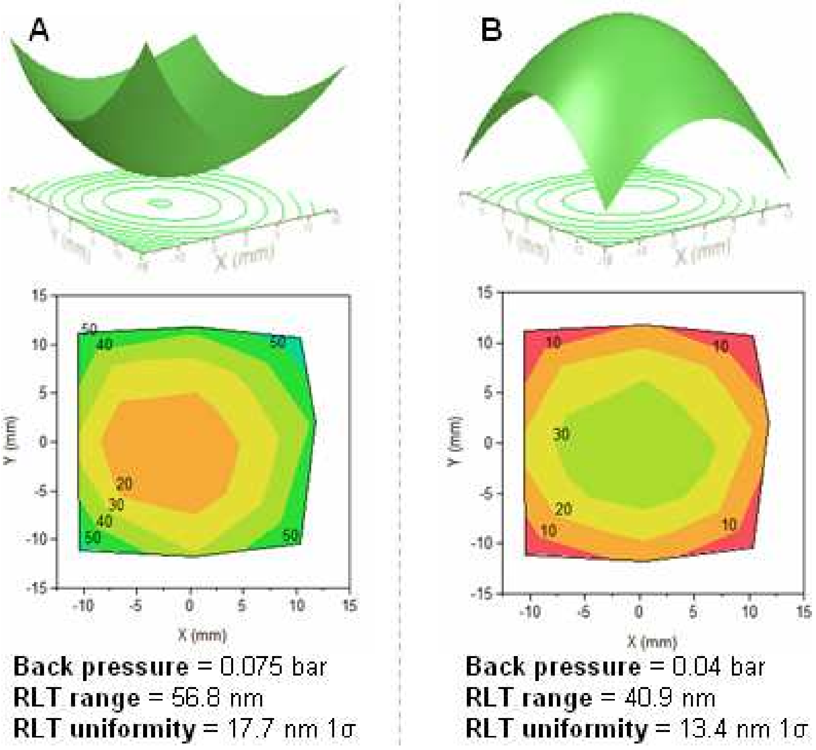


Figure 3.20: Illustration of template back pressure and its effect on the imprint template curvature [16]. *Reprinted with permission from Brook Chao.*



Back pressure = 0.075 bar
RLT range = 56.8 nm
RLT uniformity = 17.7 nm 1σ

Back pressure = 0.04 bar
RLT range = 40.9 nm
RLT uniformity = 13.4 nm 1σ

Figure 3.21: Comparison of high and low template back pressure and their effects on the thickness uniformity of the imprint residual layer [16]. *Reprinted with permission from Brook Chao.*

In addition to the template back pressure adjustments, the optimization of imprint material drop patterns allows fine tuning of the SIM volume distribution to compensate for the density variations in the dual damascene patterns (chapter 2 section 3.2). The combination of template back pressure and SIM drop pattern optimization were able to reduce the RLT to less than 50 nm and the RLT uniformity as low as 8.8 nm 1σ (Figure 3.19 and Figure 3.22). This improved RLT and uniformity came at the cost of long imprint fluid spread time. The tolerance on the RLT was calculated from etch transfer experiments [16]. The maximum acceptable RLT uniformity for our etch process is 16 nm 1σ. We were able to meet that requirement.

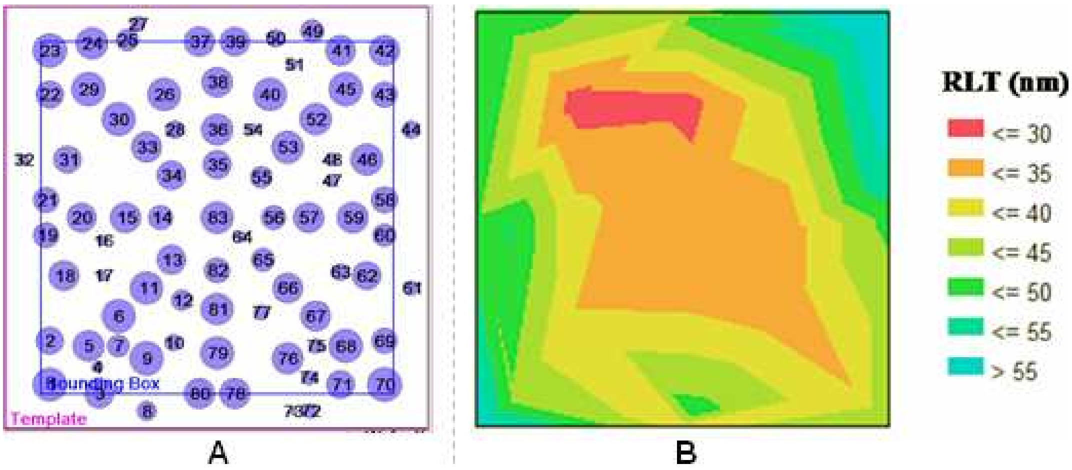


Figure 3.22: Optimized drop pattern (A) and the resulting residual layer thickness contour (B). The residual layer thickness were measured using spectroscopic ellipsometry, with uniformity of 8.8 nm 1σ [16]. *Reprinted with permission from Brook Chao.*

3.3.3 Etch Process Development

Development of an etch process for the etch transfer of the imprinted dual damascene pattern from SIM into the dielectric substrate started with a single-step etch using the standard Black Diamond etch condition. Initial etch tests with the single-step etch process encountered three major limitations to the quality of the etched patterns: etch rate mismatch, imprint residual layer uniformity, and etch artifacts (Figure 3.23).

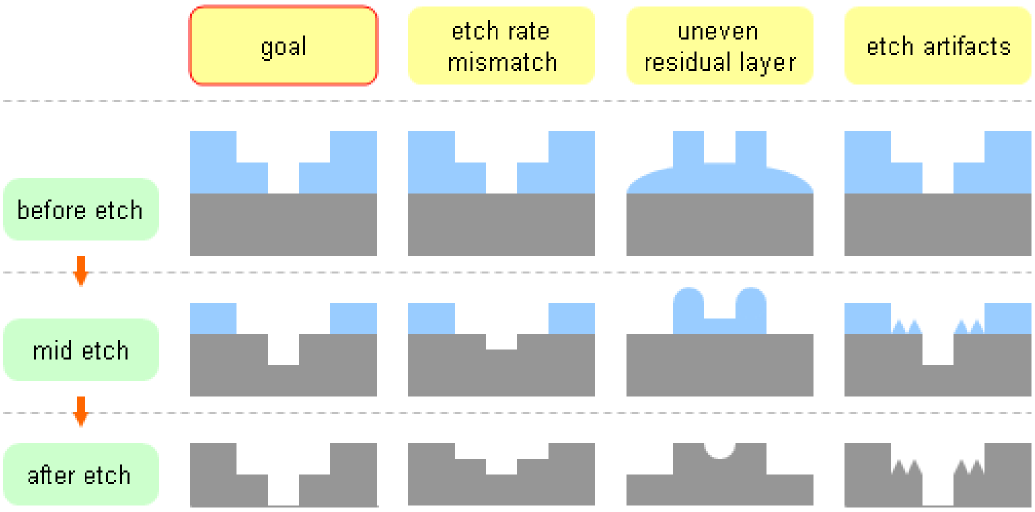


Figure 3.23: The effects of etch rate mismatch, imprint residual layer uniformity, and etch artifacts on the quality of the etched dual damascene structures, using a single-step etch process.

The etch rate mismatch between SIM and dielectric material caused vertical distortion in the feature aspect ratio as it was being etched (Figure 3.23). In a single-step etch of the dual damascene structures, the increased etch depth required to transfer both the metal and via interconnect structures amplified the aspect ratio distortion from the etch rate mismatch.

The variability in the imprint residual layer caused non-uniform removal of the residual layer during the breakthrough etch, resulting in the inconsistent etch transfer of the imprint pattern into the substrate (Figure 3.23). The increased etch depth required for etch of both the metal and via interconnect structures amplified the impact of the imprint residual layer variations in the etched dual damascene pattern.

A highly polymerizing etch chemistry was used in the standard Black Diamond etch process to maintain a vertical sidewall and improve etch anisotropy. Such polymerizing etch chemistry also roughened the exposed top surface of the imprint material due to concurrent etch residue deposition and physical ion ablation. In the conventional dual damascene process with photolithography, the via and metal structures were patterned and etched separately. The photoresist was never fully consumed during etch and the photoresist surface roughness did not affect the etched dielectric patterns. However, in a single-step etch of the imprinted dual damascene structures, portions of SIM at the bottom via level needed to be fully consumed in order to allow the subsequent etch transfer of the metal level structures (Figure 3.23). Consequently, surface roughness on the SIM film generated during the via etch was replicated into the dielectric film during the subsequent metal etch, manifesting as random etch artifacts in the etched dual damascene structures. The etch artifacts compromised the performance and reliability of the interconnect structures and must be avoided.

To address the limitations of the single-step etch process caused by etch rate mismatch, imprint residual layer uniformity, and etch artifacts, an in-situ, multi-step etch process was developed for the etch of dual damascene imprints with SIM (Figure 3.24). The in-situ, multi-step etch process started with residual layer breakthrough, followed by via transfer, metal trench descum, metal transfer, and lastly a SIM ash. The details and etch conditions of each etch step are described below:

1. The residual layer breakthrough etch step used a H_2/N_2 etch chemistry to remove the imprint residual layer at the bottom of the imprinted via structures (Figure 3.24). The H_2/N_2 etch chemistry provided high selectivity of SIM over the dielectric material, reducing the field-to-field variation of the residual layer thickness.
2. The via transfer etch used a $C_4F_8/Ar/N_2$ etch chemistry to transfer the via structures into the dielectric substrate (Figure 3.24). The $C_4F_8/Ar/N_2$ etch chemistry produced nearly vertical sidewalls at the cost of a highly polymerizing etch process and substantial surface ablation. Therefore, the etch condition was optimized to balance the need for vertical etched profile with the impact of surface roughening and pitting

on the exposed top sides of the imprinted SIM and micro-trenching at the bottom of line structures. The via transfer etch was terminated before these undesirable etch artifacts were transferred into the dielectric substrate.

3. The metal trench descum used H_2/N_2 etch chemistry to remove any residual SIM and etch artifacts from the bottom of the metal lines (Figure 3.24). The high selectivity of the H_2/N_2 etch chemistry removed the SIM surface roughness and the micro-trenching generated during the via transfer etch, clearing the exposed dielectric film for the subsequent metal transfer etch.
4. Unlike the conventional dual damascene process with separate via and metal patterning and etch steps, the simultaneous etch transfer of both via and metal structures in S-FIL dual damascene process required a careful balance between etch of metal structures and protection of the exposed via structures. The metal transfer etch used a mixture of C_4F_8/CF_4 to transfer the metal pattern into the dielectric substrate (Figure 3.24). The combination of the anisotropic C_4F_8 etch chemistry and the less anisotropic CF_4 etch chemistry provided a good balance between accurate etch transfer of the pattern and minimizing facet formation on the exposed via pattern.
5. Once the metal pattern transfer etch was complete, any remaining SIM was removed in an ash process using H_2/N_2 etch chemistry (Figure 3.24). The high selectivity of the H_2/N_2 etch chemistry helped to protect the patterned dielectric material and did not oxidize the exposed metal.

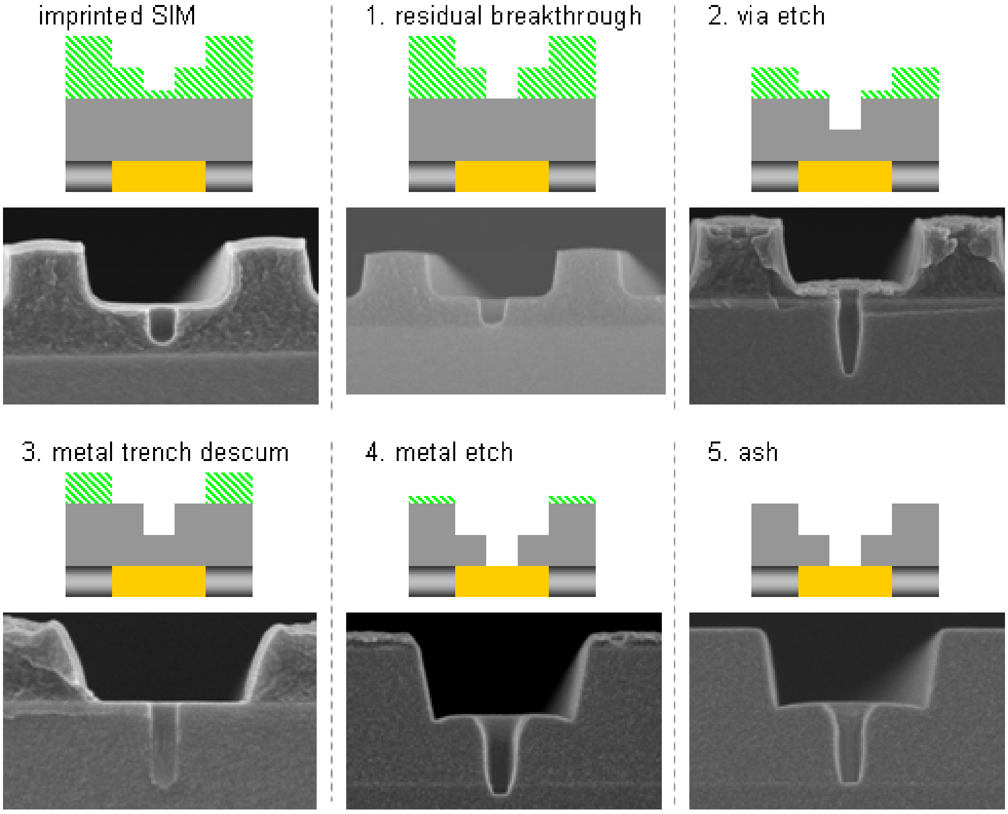


Figure 3.24: Illustration and SEM images of the in-situ multi-step etch process for the etch transfer of the imprinted dual damascene structure from SIM into dielectric substrate.

The use of multiple etch steps allows individual tuning of each etch step to meet specific etching requirements and tailoring precise feature profiles, while minimizing the impacts on other levels of the dual damascene structures. The multi-step etch process was optimized to overcome the challenges of etch rate mismatch, imprint residual layer non-uniformity, and etch artifacts. Consequently, the multi-step etch process provides greatly improved tolerance of imprint residual layer uniformity (16 nm 1σ) [16], improved etch profile control, and improved etch process flexibility.

All five etch steps are run in a single RIE chamber which provides excellent process throughput. The in-situ multi-step etch process is fully compatible with the conventional BEOL etch process and equipment. The development of the SIM etch process was done at ATDF using Tokyo Electron's Unity IIe RIE system with two DRM (Dipole Ring Magnet) chambers [16].

3.3.4 Electrical Test Data

After the completion of the multi-step etch process, the dual damascene structures were metallized and polished using the standard BEOL processes at ATDF, forming the complete via 1 and metal 2 interconnects (Figure 3.25). The electrical connectivity of the dual damascene interconnects was tested using the via chain electrical test structures by probing (Figure 3.8 and Figure 3.25A).

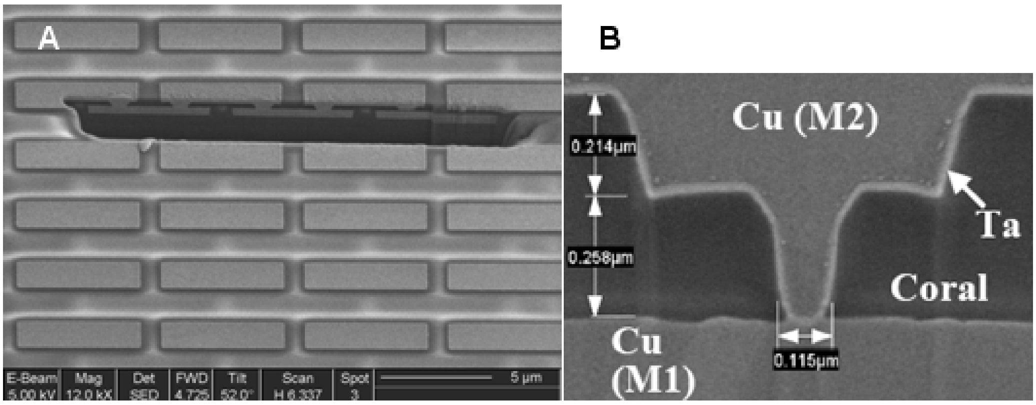


Figure 3.25: A. FIB cross section images of a 200 nm via chain. B. SEM cross section images of a 120 nm via before CMP.

Early electrical test results showed excellent connectivity in large structures but poor yield of the 120 nm via chains, the smallest structure on the 811AZ dual damascene template. The root cause was determined to be the slower etch rate at the bottom of small vias due to the high aspect ratio of the small via holes (Figure 3.25B). The reduced etch rate at the bottom of small vias caused inconsistent breakthrough of the barrier layer between the dielectric material and the metal 1 copper, resulting in unreliable electrical connection between the via 1 and the metal 1 structures. The particular RIE equipment used for the SIM process development was unable to compensate for the variations in etch rate due to the large range of pattern geometries in the 811AZ dual damascene design. More modern etch tools have the ability to etch such structures, but we did not have access to those tools. Therefore, the metal transfer etch conditions were adjusted to deliberately induce faceting of the via holes, which improves the etch rate of the barrier layer at the bottom of via bottoms (Figure 3.26) [16].

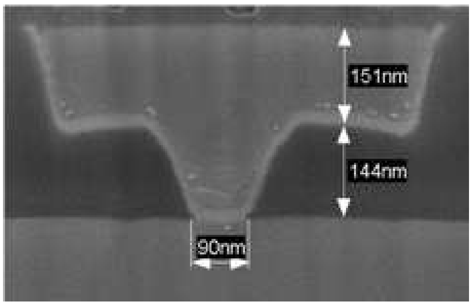


Figure 3.26: SEM cross section images of a 120 nm via, with intentional faceting of the top of via hole to improve the barrier layer etch rate at the bottom of via.

The change to the metal transfer etch condition and the resulting via hole facets enabled reliable breakthrough of the barrier layer between the dielectric film and the underlying metal 1 copper. The chain resistance of 120 nm 1000-via chains on dual damascene wafers made with the modified etch process showed greatly improved electrical connectivity results (Figure 3.27). The yield of via chain is calculated by measuring the electrical resistance of via chain modules and comparing with the acceptable electrical resistance parameters of functioning devices. The electrical test data show low site-to-site and across-wafer variations in the chain resistance measurements, with overall 1000-via chain yield up to 96.83% and an equivalent individual via yield of 99.9968% [16], successfully demonstrating process yield including all aspects of the dual damascene process: S-FIL patterning, etch, metallization, and CMP.

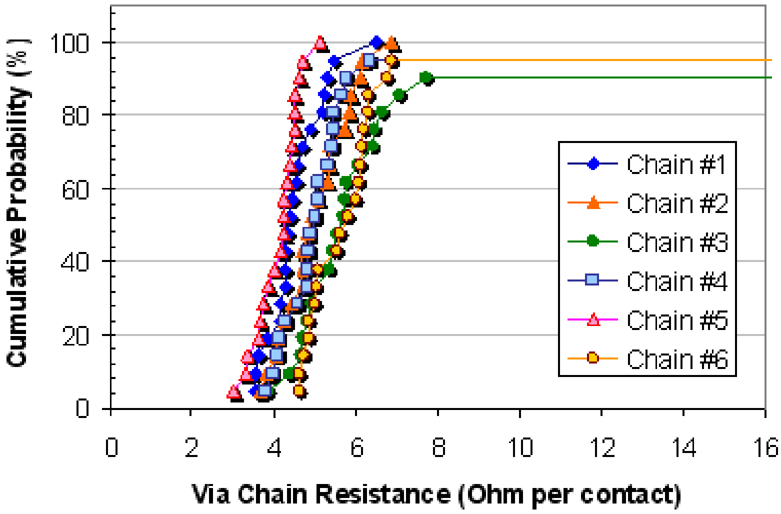


Figure 3.27: Electrical test measurement of 1000-via chain resistance. The sample is imprinted using S-FIL with SIM, etched using an in-situ five-step etch process with faceting of via holes, and post processed using standard ATDF dual damascene process. The overall yield of the measured via chains is 96.8% [16]. *Reprinted with permission from Brook Chao*.

3.4 CONCLUSION

Multi-level S-FIL of a sacrificial imprint material and an etch process were developed for the simultaneous fabrication of via and metal level interconnects in commercial dielectric materials. By using a dual damascene imprint template built with both the via and metal interconnect patterns, one S-FIL step reproduced the same dual damascene structures that would otherwise require two photolithography steps. An in-situ, multi-step etch process was developed that accurately transfers the imprinted via and metal patterns into a commercial dielectric material. The feasibility of multi-level S-FIL and etch integration in a commercial copper dual damascene process was successfully demonstrated with electrical test measurements. The successful integration of S-FIL into the dual damascene process simplifies the BEOL process flow and offers the potentials of increased throughput and reduced process cost [12].

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Chapter 4: Imprintable Dielectric Material

The physical patterning nature of Step and Flash Imprint Lithography (S-FIL) enables the replication of three dimensional structures in a lithography process. As demonstrated in the development of sacrificial imprint material, one S-FIL step can reproduce the same structure that would otherwise require two photolithography steps, greatly reducing the number of lithography steps necessary to build the via and metal interconnect structures in the copper dual damascene process.

The development of an imprintable dielectric material (IDM) would combine the multi-level patterning of the via and metal interconnect structures with the application of the permanent dielectric material, thereby further reducing the number of unit process steps required to construct interconnects. By combining the three dimensional patterning capability of S-FIL, with novel dielectric precursor formulations, dielectric materials with the desired dual damascene structures can be simultaneously deposited and patterned onto the wafer substrates.

4.1 IMPRINTABLE DIELECTRIC MATERIAL PROCESS

In the IDM process (Figure 4.1), the substrate is patterned using S-FIL to create the metal and via interconnect design as three dimensional relief patterns in the IDM film. The imprinted substrate is then thermally cured to convert the patterned IDM into a functional dielectric material. The patterned and cured IDM becomes a permanent part of the interconnect structure, unlike the conventional photoresist or SIM which simply functions as an etch mask. In effect, the imprintable dielectric material functions as both a storage medium for the dual damascene structures during the imprint step and a precursor material for the formation of a permanent, dual damascene dielectric. The IDM process reduces the need for separate pattern transfer etch steps and further streamlines the dual damascene fabrication process.

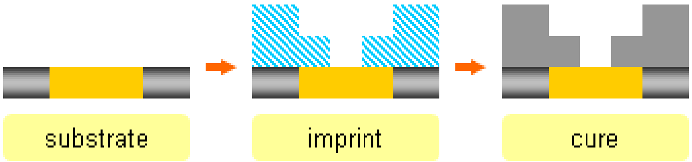
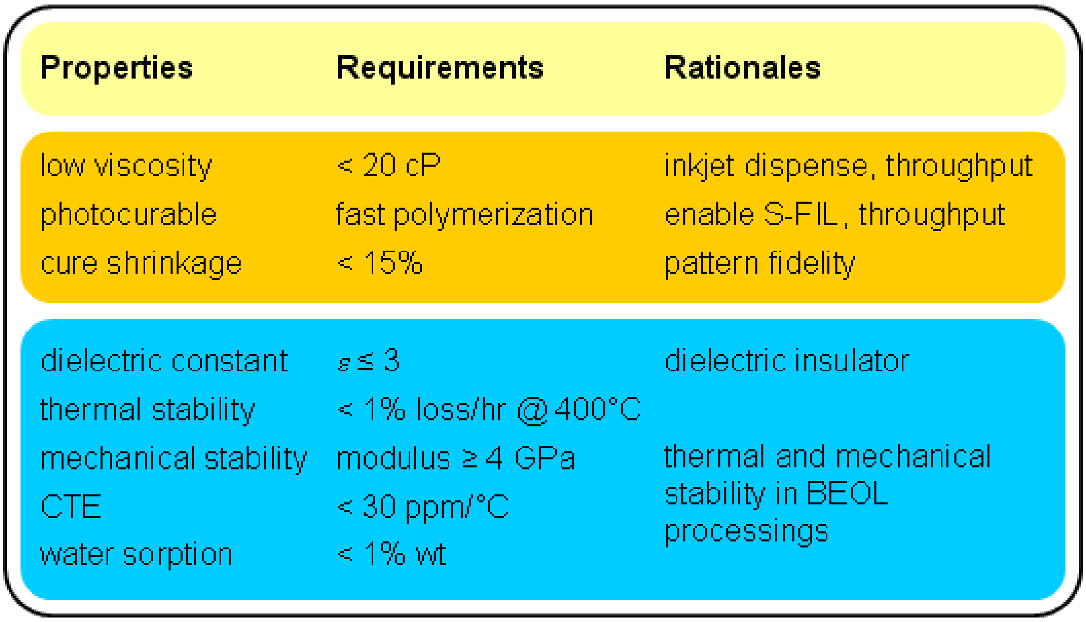


Figure 4.1: Overview of the multi-level S-FIL with imprintable dielectric material.

4.2 IMPRINTABLE DIELECTRIC MATERIAL REQUIREMENTS

In order to perform effectively as both the imprint medium and the permanent dielectric material, the IDM formulation needs to meet the requirements of both the S-FIL process and the dielectric function.



Properties	Requirements	Rationales
low viscosity	< 20 cP	inkjet dispense, throughput
photocurable	fast polymerization	enable S-FIL, throughput
cure shrinkage	< 15%	pattern fidelity
dielectric constant	$\varepsilon \leq 3$	dielectric insulator
thermal stability	< 1% loss/hr @ 400°C	
mechanical stability	modulus ≥ 4 GPa	thermal and mechanical stability in BEOL processings
CTE	< 30 ppm/°C	
water sorption	< 1% wt	

Figure 4.2: Overview of the IDM formulation requirements. The top section describes the material requirements of the S-FIL process and the bottom section outlines the material requirements of the dielectric function.

As summarized in Figure 4.2, the S-FIL process requires an imprint formulation with low viscosity, fast photopolymerization, and minimal volume shrinkage during curing. The dielectric requirements for a modern CMOS device application include a low dielectric constant, good thermal stability, mechanical strength, low coefficient of thermal expansion, and low water sorption. The thermal and mechanical stability requirements are derived from the process conditions of a standard BEOL dual damascene process flow.

Several classes of materials were studied for their application as IDM formulations in S-FIL. In particular, our research group has previously evaluated the suitability of sol-gel, epoxy functionalized polyhedral oligomeric silsesquioxane (POSS), and dually functionalized POSS material. My work on the POSS systems with azide and thiol-ene cross-linking chemistries will be presented in the later part of this chapter. All of these works were carried out in collaboration with chemists and chemical engineers in our research group. Their specific contributions are gratefully acknowledged. A project of this scope cannot be completed efficiently by a simple researcher.

4.3 SOL-GELS

The sol-gel process is a solution deposition technique used for the fabrication of ceramic materials from chemical solutions. A formulation of reactive precursors dissolved in a solution phase undergoes polymerization reactions to form colloidal particles, which then coalesce into an integrated network solid (a gel). Applications of the sol-gel process include molding the gel into the desired geometry, then drying or curing the formed gel to produce a solvent-free porous material. Typical sol-gel precursors include metal alkoxides and metal chlorides, which undergo various forms of hydrolysis and condensation reactions. Extensive studies and publications on the chemistry and applications of sol-gel process already exist, and a wide range of sol-gel precursor materials are available commercially [1-2].

Silica derived sol-gels are formulated from hydroxysilanes or alkoxysilanes with an appropriate solvent, water and an acid or base catalyst to initiate the polymerization reactions in the sol. Methylated-hydrogen silsesquioxane (MSQ), tetraethyl orthosilicate (TEOS), and methyltrimethoxysilane (MTMS) sol-gel processes have been studied for their applications in the fabrication of porous, low-k dielectric materials [3]. Previous work on lithographic patterning of sol-gel derived films has been demonstrated using the thermal NIL technique [4]. Advantages of sol-gel systems include the demonstrated thermal stability of 400 °C or higher [4-5] and the compatibility with porogen modification techniques to further reduce its dielectric constant [6]. One of the main challenges of sol-gel derived materials is the formation of internal tensile stress and cracks during the curing and densification process [7].

4.3.1 Sol-Gel Formulations

The formulation of sol-gel IDM was an iterative design process carried out by Dr. Frank Palmieri in our research group [8]. Candidate sol-gel materials were prepared from commercially available alkoxysilanes (Figure 4.3) and first screened for photopolymerization and pattern replication quality to eliminate those with poor imprint properties. The sol-gels with good polymerization and pattern replications were then evaluated in a standard S-FIL process, followed by thermal curing of the imprinted structures. Most of the test formulations did not meet the imprint portion of the IDM requirements, but a few of the sol-gel formulations did exhibit good S-FIL compatibility, thermal stability, and mechanical strength.

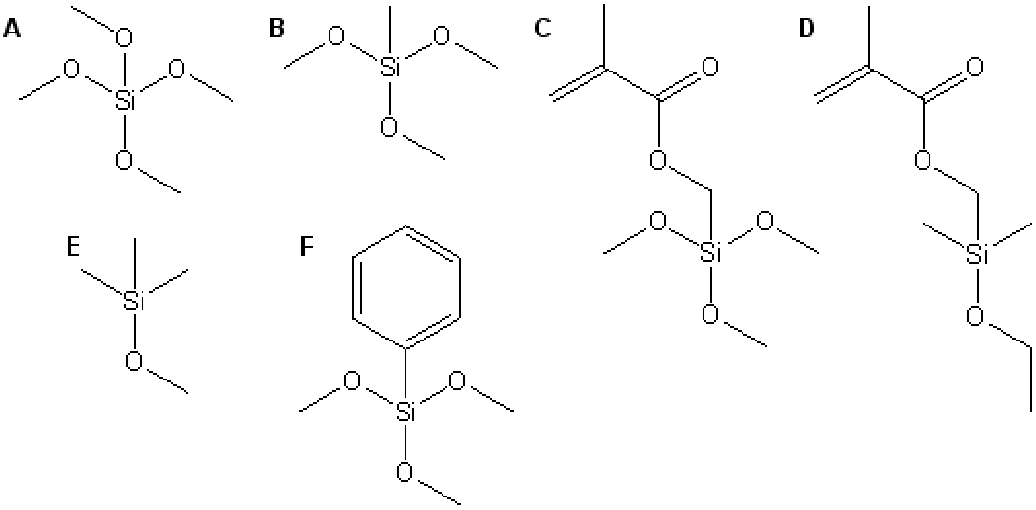
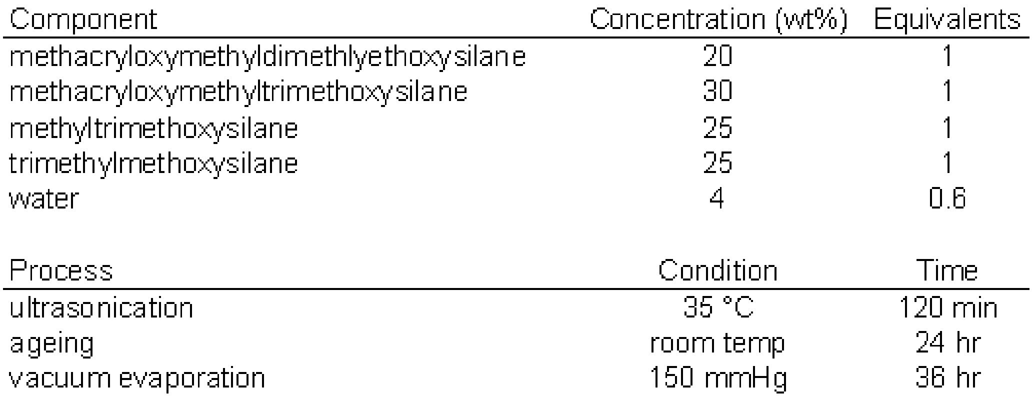


Figure 4.3: Commercially available alkoxysilanes used in sol-gel IDM formulations [8].

Due to the time and cost limitations, only one functional sol-gel formulation was tested for integration into the standard ATDF copper dual damascene process. The composition and processing conditions of the functional sol-gel IDM are presented in Figure 4.4.



Component	Concentration (wt%)	Equivalents
methacryloxymethyldimethlyethoxysilane	20	1
methacryloxymethyltrimethoxysilane	30	1
methyltrimethoxysilane	25	1
trimethylmethoxysilane	25	1
water	4	0.6

Process	Condition	Time
ultrasonication	35 °C	120 min
ageing	room temp	24 hr
vacuum evaporation	150 mmHg	36 hr

Figure 4.4: Composition and processing conditions of the sol-gel IDM [8]. *Reprinted with permission from Frank Palmieri.*

4.3.2 Sol-Gel Evaluations

Early attempts at metallization and CMP of the sol-gel IDM patterned wafers resulted in faceting of the via and metal structures during barrier layer breakthrough etch, significant dishing of the top side of sol-gel material during CMP, and inconsistent via connection to the substrate metal structures (Figure 4.5). Modifications to the barrier layer etch process reduced the faceting of the via holes and improved the via connections to the substrate metal, yet still resulted in very low interconnect yields (Figure 4.6).

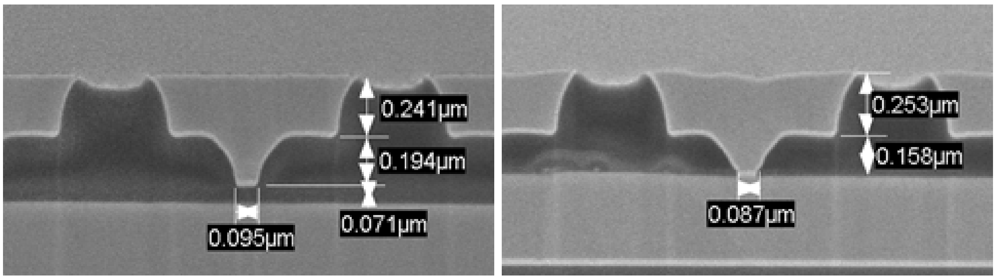


Figure 4.5: SEM images of dual damascene structures with sol-gel dielectrics, showing significant faceting of the via hole and dishing of the top side of sol-gel material. *Reprinted with permission from Brook Chao*.

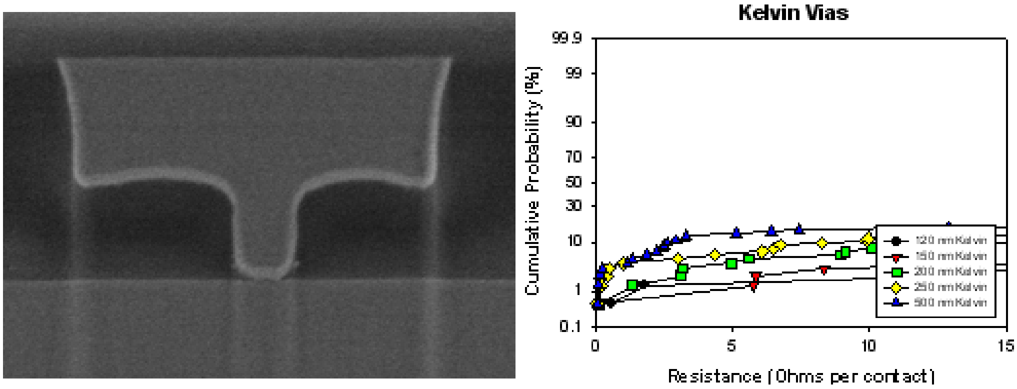


Figure 4.6: SEM images of dual damascene structures with sol-gel dielectrics, using modified barrier etch condition to better preserve the dual damascene profile. However, the electrical test data still shows very low via yields. *Reprinted with permission from Brook Chao*.

Further analysis of the electrical test data and SEM imaging of the processed wafers indicated three causes for the low interconnect yields: imprint residual layer thickness non-uniformity, misalignment of the imprints, and defects on the metal 1 substrate. The variability in the imprint residual layer thickness causes non-uniform removal of the residual layer and breakthrough of the barrier layer during the etch process. As described in chapter 3 section 3.3, this results in inconsistent electrical connection between the via and substrate metal structures. The misalignment of the small vias resulted in vias landing off the target substrate metal structure, producing open connection or high electrical resistance. The misalignment is especially pronounced for the 120 nm and 250 nm via chains structures, which are well below the alignment accuracy of the Imprio 55 (~1 µm) used in the development of sol-gel IDM. Lastly, the metal 1 substrate used in the development of IDM contained random pit defects on the metal structures, caused by errors in the initial production of the metal 1 fabrication and the subsequent rework process. The metal 1 defects are large enough to cause open circuits when a via lands directly upon them, reducing the electrical test yields (Figure 4.7). We believe that higher yields could have been demonstrated but our access to the processing facility was terminated due to sale of the facility and expiration of the group.

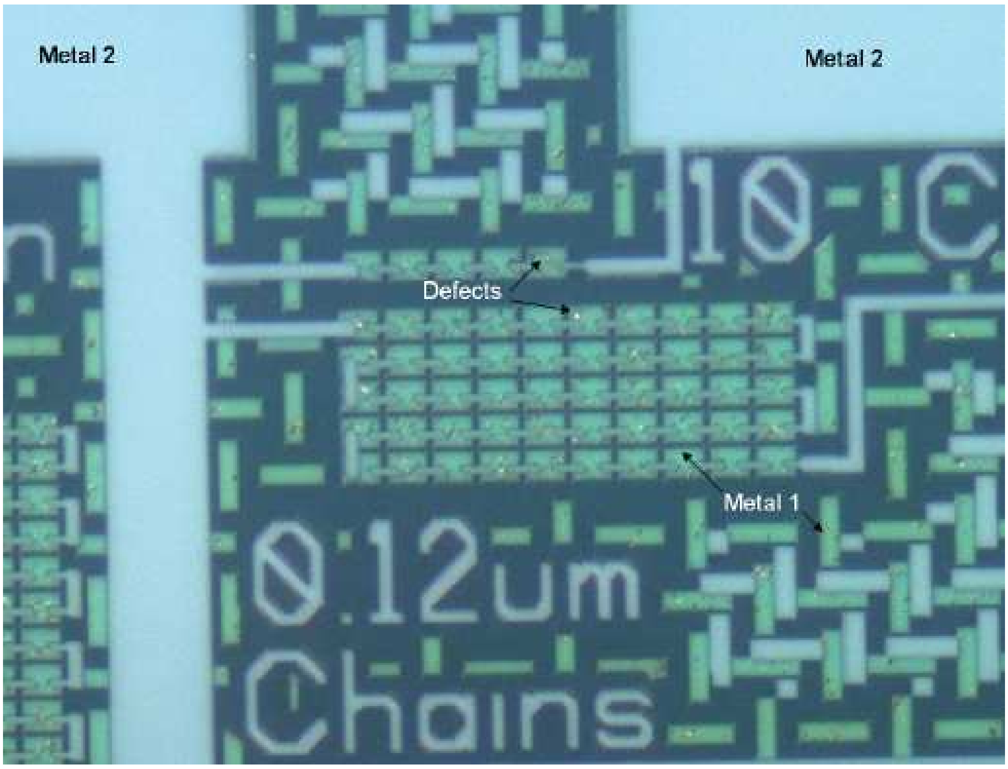


Figure 4.7: Optical microscope images of metallized and polished sol-gel IDM wafer, showing significant number of defects in the substrate metal 1 structures. The metal 1 defects are large enough to cause open circuit or high resistance interconnect failures. *Reprinted with permission from Frank Palmieri.*

4.3.3 Sol-Gel Summary

The sol-gel IDM material was successfully applied into a multi-level S-FIL process for the fabrication of dual damascene interconnect structures. The imprinted wafers were integrated into the standard ATDF BEOL process to complete the dual damascene interconnect structures. Electrical test data showed low interconnect yields of the imprinted sol-gel dielectric test samples. Modification of the breakthrough etch condition were able to reduce the via profile faceting, but imprint limitations such as residual layer non-uniformity and pattern misalignment continue to impact the interconnect yields. We believe that higher yields could be demonstrated, but the high mass loss and volume shrinkage of the sol-gel material during the imprint and thermal cure process require improvement to minimize the risk of crack formation in the imprinted structures.

4.4 POLYHEDRAL OLIGOMERIC SILSESQUIOXANE

Polyhedral oligomeric silsesquioxanes (POSS) are a class of silsesquioxane oligomers with a cage structure composed of the empirical formula $RSiO_{1.5}$, where R can be simply hydrogen or a wide range of organic functional groups. POSS compounds represent a hybrid (inorganic-organic) architecture, with an inner inorganic framework made up of silicon and oxygen, and an external layer of organic functional groups [9]. The eight-silicon version of the POSS compound can be thought of as the smallest unit cell of silica network (Figure 4.8), the material that has been the foundation of dielectric materials for the semiconductor industry. Unlike silica or silicon oxide films, the functional groups of the POSS molecule can be modified to impart various surface and reactive properties to the bulk POSS material. The combination of the inorganic silica core stability with the organic pendant group versatility enables novel applications of the POSS materials, and one such application is as an IDM.

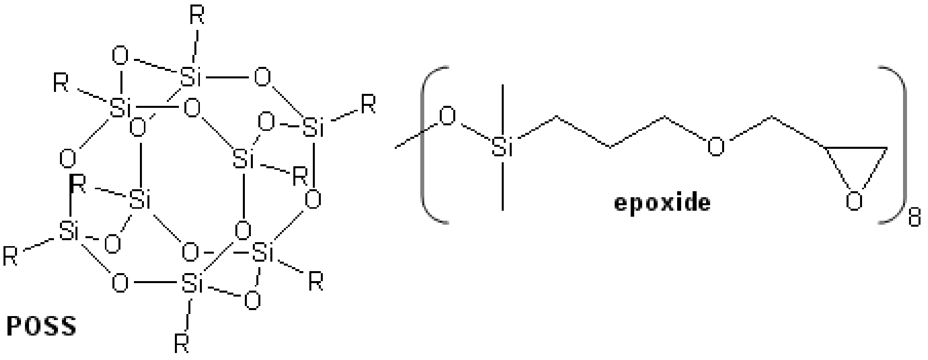


Figure 4.8: Structures of the POSS epoxide materials. The R pendant moieties on the POSS structure denote the locations of the epoxide functional groups.

4.4.1 POSS Epoxide Formulations

Most of the functionalized POSS materials are solid crystalline powders, which are not compatible with the S-FIL process. However, selected POSS derivatives with bulky pendant groups have been demonstrated to remain in liquid phase at room temperature. Work by Professor Laine at the University of Michigan at Ann Arbor has demonstrated a series of photo-sensitive, liquid POSS materials based on epoxy, acrylic, and methacrylic groups [10-12]. A sample of POSS material with epoxide functional groups (Figure 4.8) was obtained from Dr. Laine's laboratory for evaluation as a possible IDM candidate [12]. Addition of 2 wt% of a photoacid generator enabled photopolymerization of the epoxy POSS material.

4.4.2 POSS Epoxide Evaluations

The high viscosity of the POSS epoxide formulation (600+ cP) prevented the use of inkjet dispense on the S-FIL equipment. Manual imprints were made to assess the imprint quality of the POSS epoxide formulation. SEM images of the imprinted POSS epoxide samples showed well resolved multi-level structures (Figure 4.9).

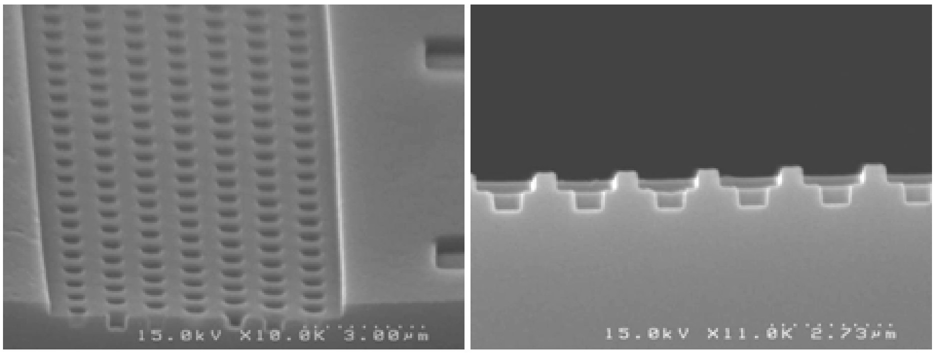


Figure 4.9: SEM images of imprints made with POSS epoxide IDM.

TGA measurement of polymerized POSS epoxide material shows onset of mass loss at 200 °C, which is much lower than the expected thermal stability of the silsesquioxane core and lower than the IDM requirements. The poor thermal stability was attributed to decomposition of the epoxide cross-links catalyzed by the residual acid from the photopolymerization. The mechanical and dielectric properties of polymerized POSS epoxide samples were measured with the assistance of the IBM Almaden Research Center. The material has a density of 1.28 g/cm^3, tensile modulus of 6.21±0.08 GPa, and dielectric constant of 3.16±0.64 [8].

4.4.3 POSS Epoxide Summary

The POSS epoxide material was evaluated for its use as an IDM. The imprinted POSS epoxide demonstrated good pattern quality using a manual imprint process, good mechanical strength, and promising dielectric property. However, the high viscosity of the POSS epoxide prevented its use in the standard S-FIL process, and the thermal stability of the polymerized POSS epoxide fell short of the dielectric material requirements. Based on the POSS epoxide learning, subsequent IDM developments retained the use of POSS material while modifying the exterior functional groups to improve viscosity and thermal stability.

4.5 POSS ACRYLATE

POSS acrylate was developed to address the low thermal stability of the POSS epoxide formulation. The POSS cage was functionalized with a mixture of acrylate and benzocyclobutene (BCB) functional groups (Figure 4.10). The acrylate moiety enables rapid photopolymerization upon exposure with addition of a photoinitiator, but is susceptible to mass loss at elevated temperatures due to thermal decomposition and shrinkage during polymerization. The BCB moiety does not undergo photo-induced polymerization, but can be thermally cured in a ring opening polymerization reaction to increase the thermal stability and mechanical strength of the POSS material with very low shrinkage. By adjusting the ratio of acrylate and BCB moieties, the thermal stability of the POSS material could be improved while maintaining compatibility with the S-FIL process.

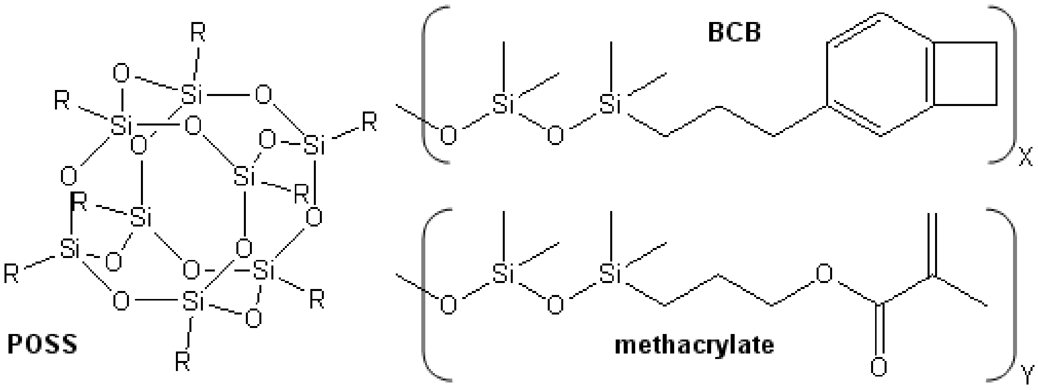


Figure 4.10: Structures of the POSS acrylate materials. The R pendant moieties on the POSS structure denote the locations of the methacrylate and BCB functional groups.

4.5.1 POSS Acrylate Formulations

Synthesis of POSS, acrylate, and BCB has been previously reported by other members of our research group [13]. Functionalization of the POSS molecule with the acrylate and BCB groups was done using a platinum catalyzed hydrosilylation reaction between the silane pendant groups of the POSS molecule and the allyl derivatives of BCB and acrylate groups [13-14]. A series of POSS acrylate compounds with varying ratios of acrylate and BCB functional groups were prepared and first screened for photopolymerization and pattern replication quality to determine their suitability as imprint material. Photopolymerization was tested by adding 1-5 wt% of a photoinitiator such as Darocur 1173 from Ciba Specialty Chemical to the formulation and pressing a drop of the POSS acrylate formulation between two glass slides to isolate the system from air. Exposure to a broadband mercury arc lamp UV source initiated the photopolymerization reaction. Excess exposure was used to ensure a complete reaction during initial screening of candidate formulations.

The dual functional groups design of the POSS acrylate formulation allows tuning of its material properties by adjusting the ratio of acrylate and BCB groups. The acrylate moiety provides good imprint quality at the cost of thermal stability. In contrast, the BCB moiety improves thermal stability but does not photopolymerize during S-FIL processing. Based on the initial imprint screening of the candidate POSS acrylate formulation, the best balance of imprint quality and thermal stability is found in the POSS acrylate system with an average of three acrylate and five BCB groups per POSS molecule.

4.5.2 POSS Acrylate Evaluations

Manual imprints were made to assess the imprint quality of the functional POSS acrylate formulation. SEM images of the imprinted and thermally cured POSS acrylate samples showed accurate pattern replication and good image quality (Figure 4.11).

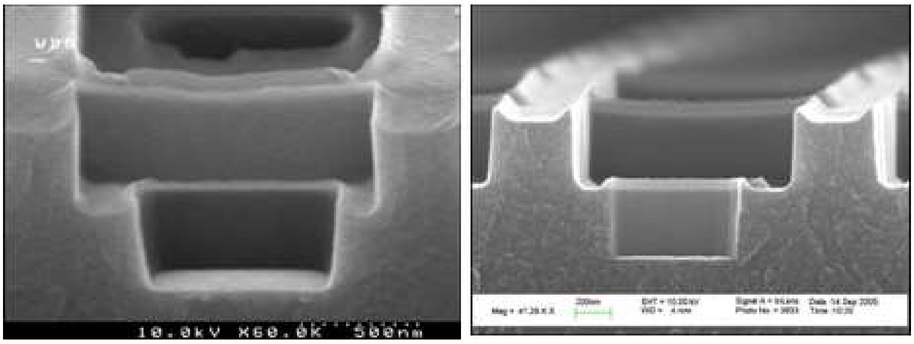


Figure 4.11: SEM images of imprints made with POSS acrylate IDM. The ridges at the crest of the imprinted sidewalls are replications of the micro-trench defects in the imprint template and demonstrate high resolution patterning capability of the multi-level S-FIL process.

The high viscosity of the functional POSS acrylate formulation (600+ cP) prevented its use in the standard S-FIL inkjet dispenser, requiring the development of a new viscous fluid dispense system. The thermal stability and coefficient of thermal expansion of thermally cured POSS acrylate samples were found to be 344 °C and 32 ppm/°C respectively [8], significantly improved from the POSS epoxide formulation and closer to the dielectric material requirements. The mechanical and dielectric properties of thermally cured POSS acrylate samples were measured with the assistance of the IBM Almaden Research Center. The material has a density of 1.217 g/cm^3, tensile modulus of 4.52±0.08 GPa, and dielectric constant of 2.76±0.22 [8].

During the imprint tests, the properties and performances of the synthesized POSS acrylate material was found to vary batch-to-batch. Separate batches of the POSS acrylates made with the same starting ingredients, compositions, and synthetic techniques produced materials with noticeably different imprint characteristics. Initial analysis of the POSS acrylate materials with standard spectroscopic techniques were unable to determine the source of the discrepancy between batches, until samples of the POSS acrylate materials were analyzed using mass spectrometry with matrix-assisted laser desorption/ionization technique (MALDI).

MALDI is a soft ionization technique that minimizes fragmentations and allows the analysis of large organic molecules in mass spectrometry. MALDI mass analysis revealed that as expected, the synthesized POSS acrylates contained a mixture of POSS molecules with different ratios of acrylate and BCB functional groups (Figure 4.12). The distribution of POSS acrylates resulted from the single-pot reaction used in the POSS functionalization, in which both acrylate and BCB functional groups were simultaneously added and reacted with the POSS molecules. A statistical distribution of acrylate to BCB ratios on the POSS structure was produced from the coupling reactions. The bulk average of the acrylate to BCB ratio was similar between batches of the same reaction composition, but the spread of the acrylate to BCB ratio distribution varied, resulting in different properties of the synthesized POSS acrylate.

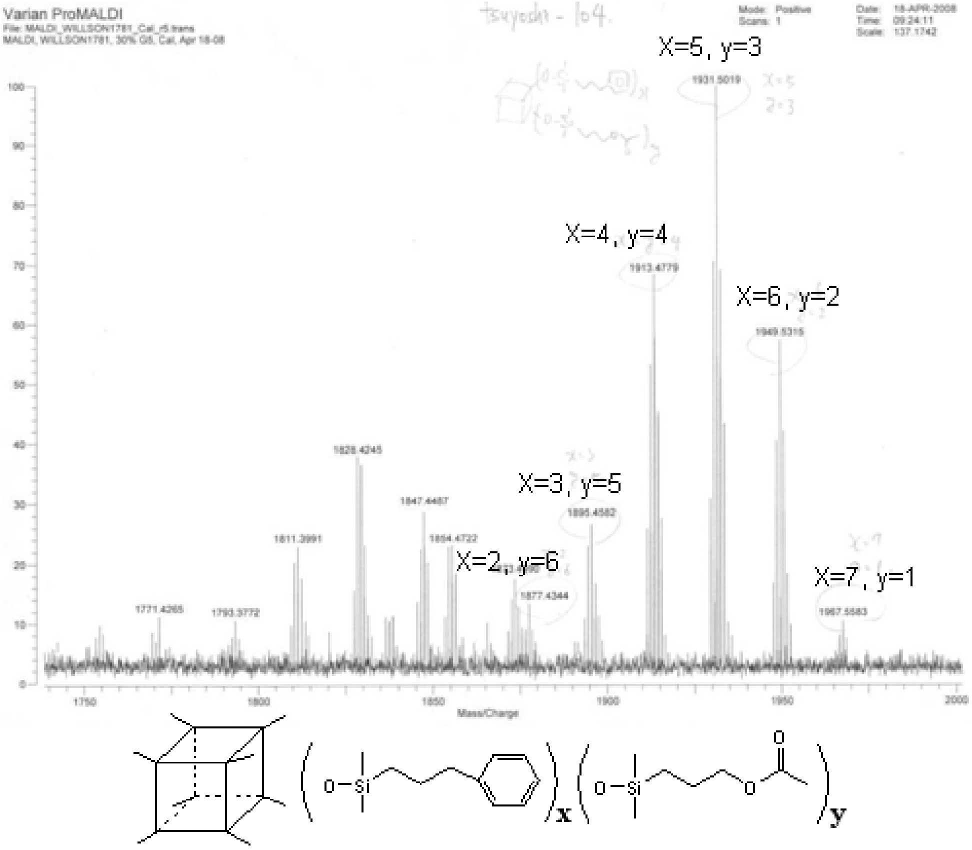


Figure 4.12: MALDI mass spectrum of a POSS acrylate model compound. The benzyl and acrylic functional groups of the model compound were used for their ease of synthesis, compared to the BCB and methacrylate functional groups. The NMR analysis calculated an acrylate to benzo group ratio of 4.8:3.2, while mass spec data measured a distribution of six POSS compounds ranging from 2:6 to 7:1.

4.5.3 POSS Acrylate Summary

POSS acrylate formulations were synthesized and evaluated for use as IDM. The heterofunctional design of the POSS acrylate material allows tuning of its material properties to meet both the S-FIL and dielectric requirements of the IDM. The imprinted

POSS acrylate samples demonstrated accurate pattern replication using a manual imprint process, good mechanical strength, and excellent dielectric properties. The POSS acrylate's thermal stability of 344 °C is significantly improved from the POSS epoxide formulation and closer to the dielectric material requirements.

Several challenges remain in the application of POSS acrylate as IDM. The high viscosity of the functional POSS acrylate formulation requires a new viscous fluid dispense system to enable its integration into the S-FIL process. The synthesis and repeatability of the heterofunctional POSS acrylate material requires considerable improvements to maintain a consistent formulation baseline for further process development. Lastly, the residual platinum catalyst from the acrylate and BCB coupling reactions of the POSS molecule is incompatible with the IC dielectric process, and the complete removal of the platinum catalyst from POSS acrylates remains unresolved. The POSS acrylate material also has limited shelf-life. An inhibitor system needs to be developed to prevent polymerization during storage.

4.6 POSS AZIDE

The synthetic difficulty of the heterofunctional POSS acrylate prompted efforts to explore homofunctionalized POSS formulations that can be prepared without metal catalysts. POSS azide was explored as one such formulation, consisting of a mixture of vinyl functionalized POSS and bis-azide cross-linker (Figure 4.13). The POSS component provides the thermal stability, mechanical strength, and the dielectric properties necessary for the dielectric function. The azide component provides photosensitivity and cross-linking polymerization with the vinyl groups, eliminating the need for additional photoinitiator and enabling the photopolymerization necessary for the S-FIL patterning process.

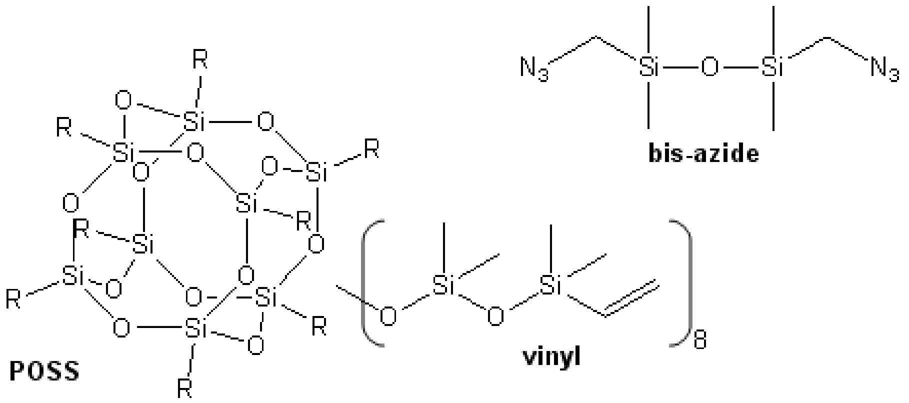


Figure 4.13: Structures of the POSS azide materials [15]. The R pendant moieties on the POSS structure denote the locations of the vinyl functional groups.

4.6.1 POSS Azide Evaluations

Photopolymerization of the POSS azides was tested by placing a drop of the POSS azide formulation on top of a glass slide and exposing to broadband UV radiation from a mercury arc lamp. The POSS azide formulation polymerized upon exposure, producing a free standing solid film. However, manual imprint tests revealed significant outgassing during the polymerization reaction, with visible generation of gas bubbles during the UV exposure process. The outgassing was attributed to the cross-linking reactions between the vinyl and azide functionalities, which generated a stoichiometric amount of nitrogen gas from the photolysis of azide into reactive nitrene intermediates. The nitrogen gas became trapped between the substrate and the imprint template during the manual imprint, forming visible bubbles and foams under the transparent imprint template. The formation of nitrogen bubbles disrupted the capillary fluid fill process during imprint and prevented the replication of template patterns. Therefore, the cross-linking chemistry between vinyl and azide functional groups was found unsuitable for the S-FIL process, and alternative cross-linker material was sought for use with the vinyl functionalized POSS.

4.7 POSS THIOL

A POSS thiol-ene system was developed to address the outgassing issue of the azide chemistry and continue the study of homofunctional vinyl POSS for IDM application. Similar to POSS azide, the POSS thiol formulation consists of vinyl functionalized POSS, but with the addition of a thiol cross-linker (Figure 4.14). The POSS component provides the thermal stability, mechanical strength, and the dielectric properties necessary for the dielectric function. The thiol cross-linker undergoes photolysis upon exposure to UV radiation to generate thiyl radical, which can then cross-link with the vinyl groups of the POSS component to in a thiol-ene addition reaction. The thiol-ene chemistry provides the photopolymerization necessary for the S-FIL patterning process and is not susceptible to oxygen inhibition comparing to the acrylate cross-linking chemistry. Addition of a photoinitiator provides a supplemental source of reactive radicals to increase the rate of thiyl radical generation during the UV exposure, improving the polymerization rate of the POSS thiol formulation.

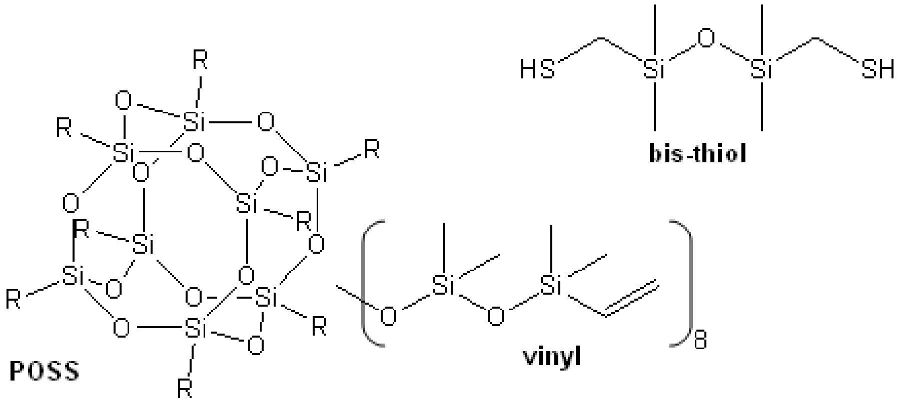
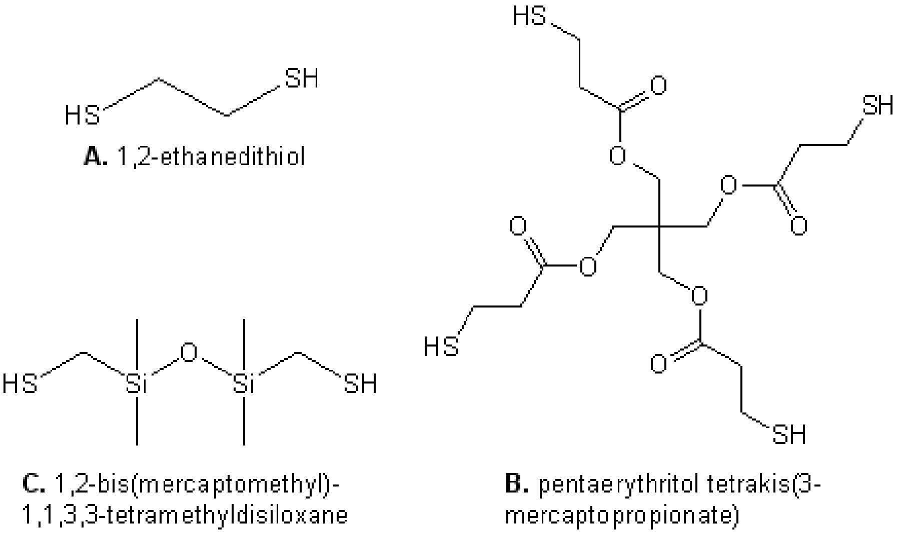


Figure 4.14: Structures of the POSS thiol materials [15]. The R pendant moieties on the POSS structure denote the locations of the vinyl functional groups.

4.7.1 POSS Thiol Formulations

Several POSS thiol formulations with different thiol cross-linkers were prepared and screened for suitability as imprint material (Figure 4.15). Photopolymerization was tested by adding 5 wt% of the Darocur 1173 photoinitiator to the formulation, placing a drop of the POSS thiol formulation on top of a glass slide, and exposing the droplet sample to broadband UV radiation from a mercury arc lamp. Excess exposure was used to ensure a complete reaction during the initial screening.



A. 1,2-ethanedithiol

C. 1,2-bis(mercaptomethyl)-1,1,3,3-tetramethyldisiloxane

B. pentaerythritol tetrakis(3-mercaptopropionate)

Figure 4.15: Structures of the thiol compounds tested for cross-linker application in a POSS thiol formulation: A. ethanedithiol, B. tetra-thiol, C. bis-thiol.

Formulation with ethanedithiol (Figure 4.15A) produced a polymerized film upon UV exposure, but the miscibility of the ethanedithiol and vinyl POSS components was poor. Phase separation between the liquid components was observed in the mixture within a day of the sample preparation, indicating short shelf life of the material. The tetra-thiol (Figure 4.15B) is completely immiscible with the vinyl POSS even after prolonged ultrasonication. The bis-thiol (Figure 4.15C) is miscible but requires ultrasonication to promote complete mixing of the viscous components. Once properly mixed, imprints with the bis-thiol cross-linker formulations demonstrated good pattern quality (Figure 4.16). Based on the initial screening results, a functional POSS thiol formulation consisting of the vinyl functionalized POSS, the bis-thiol cross-linker, and a photoinitiator was defined.

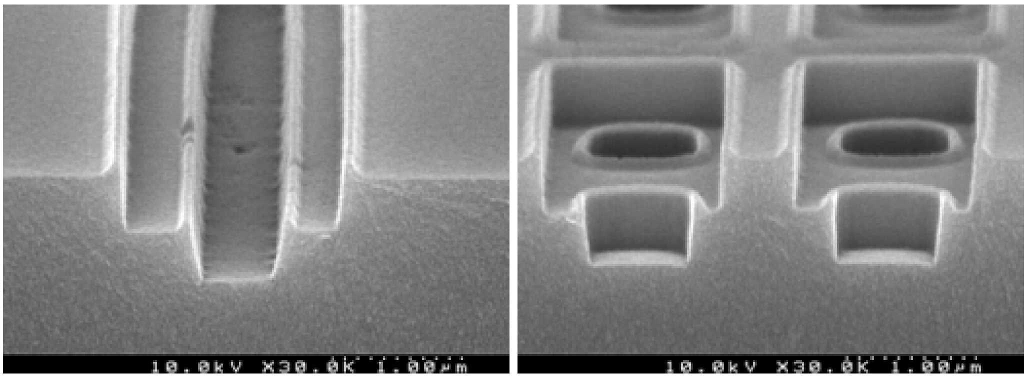


Figure 4.16: SEM images of manual imprints made with vinyl POSS and bis-thiol formulation.

4.7.2 POSS Thiol Evaluations

Manual imprints were made to establish the S-FIL process parameters. The minimum exposure doses required to fully cross-link the imprint samples were found to inversely correlate with the bis-thiol loading in the POSS thiol formulation (Figure 4.17). Since the maximum exposure time on the Imprio 55 tool is limited to 120 sec per imprint, a 25 wt% bis-thiol loading was used for subsequent functional POSS thiol evaluations.

bis-thiol loading			
(wt%)	24.9	20.4	15.8
exposure time (sec)			
Novacure	2	5	> 60
Imprio	90	120	N/A

Figure 4.17: Samples of exposure time versus bis-thiol loading data in the POSS thiol formulations.

During the evaluation of POSS thiols, noticeable variations in the minimum exposure dose requirements were seen between different batches of the vinyl POSS and bis-thiol material. Further analysis of the material and the synthesis procedure attributed the variations to the catalyst used in the synthesis. Early batches of the POSS materials were synthesized using catalyst with decayed reactivity, resulting in an inconsistent product. Later batches of the material made using newly purchased catalyst have produced consistent results.

Manually imprinted POSS thiol film samples were baked at high temperatures in a nitrogen environment to screen for thermal stability. Initial bake tests produced extensive fracturing of the POSS thiol film (Figure 4.18). Based on these results, several adjustments were made to the imprint, bake, and SEM techniques. The fluid volume was reduced to minimize the residual layer thickness and reduce the film stress generated during bake. The post-bake cooling time was increased to reduce thermal shock of the polymerized POSS thiol material. The samples were cleaved before bake to avoid fracturing of the film caused by post-bake cleave. Subsequent bake tests with the updated process produced good pattern quality after a 300 °C bake for 60 min (Figure 4.19), but the films still fractured at 400 °C. The polymerized POSS thiol material is clearly too brittle. Efforts will be made to improve the mechanical properties by modifying the thiol components.

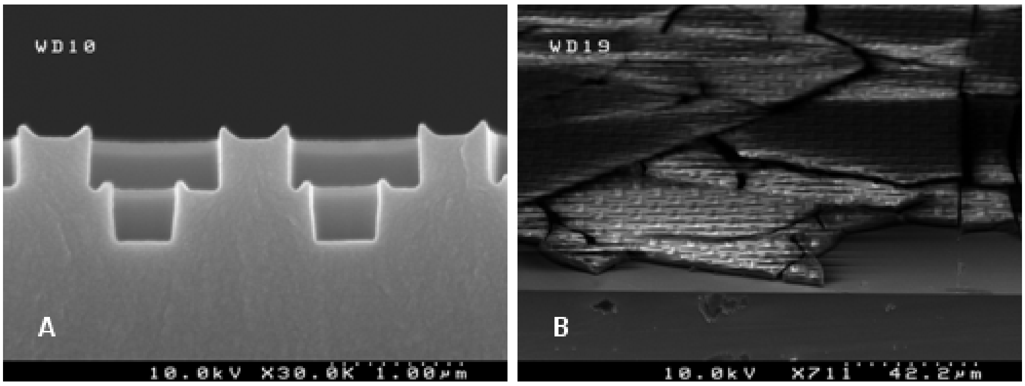


Figure 4.18: SEM images of the imprinted POSS thiol sample before bake (A) and after (B) 60 min bake at 300 °C.

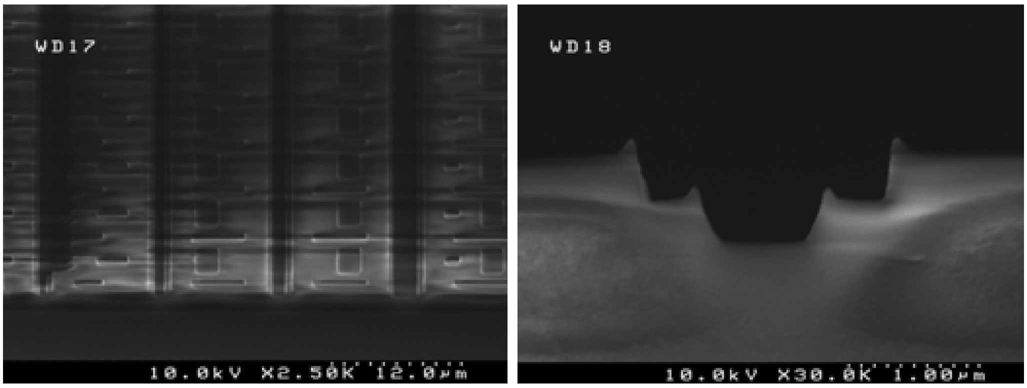


Figure 4.19: SEM images of the imprinted POSS thiol sample after 60 min bake 300 °C, with modified imprint, bake, and SEM process.

The POSS thiol formulation has lower viscosity than the POSS acrylate material, but it is still much too viscous for use in the Imprio 55 inkjet system. A viscous dispense system from nScrypt Inc. was therefore designed and installed on the Imprio 55 to enable controlled imprint with high viscosity fluids such as the POSS thiol formulation (Figure 4.20). Unlike the inkjet system's projection of fluid droplets onto the substrate, the viscous dispense system uses a pneumatic-driven single-nozzle pump to extrude the viscous fluids onto the substrate. Fluid with viscosity up to 10^6 cP can be used with this system. The volumetric control is dependent on the nozzle size, fluid surface tension, and wetting properties [16]. A motorized overhead gantry enables three dimensional movement of the pump for positioning relative to the wafer and distribution of the fluid. Similar to the inkjet dispense, a fluid drop map is designed to control the placement and volume distribution of the high viscosity fluid during each imprint.

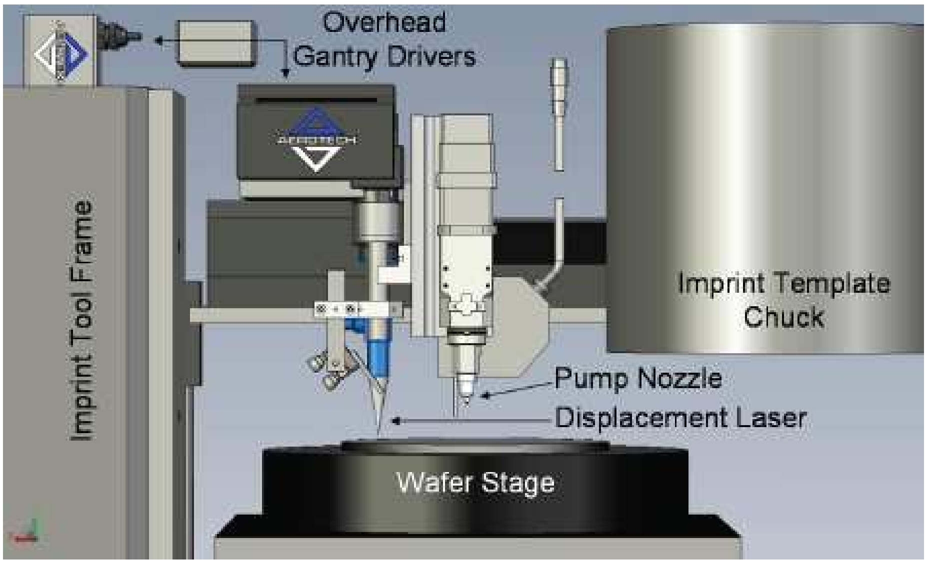


Figure 4.20: Illustration of the viscous fluid dispense system. It is designed to fit inside a Molecular Imprints Inc. Imprio 55 and consists of an overhead gantry, laser position sensor, and pneumatic pump. *Image courtesy of nScrypt.*

During establishment of the viscous dispense condition for POSS thiol material, the imprint formulation was observed to occasionally undergo polymerization without UV exposure. The root cause was found to be a stainless steel catalysis of the thiol-ene cross-linking reaction. Since several of the viscous pump parts are made of stainless steel, two approaches were taken to address the unintended polymerization of the POSS thiol material: addition of an inhibitor to the imprint formulation and surface passivation of the exposed stainless steel pump parts.

Several radical inhibitors were tested to evaluate their potential in suppressing the stainless steel catalyzed POSS thiol polymerization (Figure 4.21). 1,4-benzenediol, 1,3-

benzenediol, and a proprietary inhibitor NPAL were found to be immiscible with the POSS thiol mixture. 4-Hydroxy tempo formed a precipitate after short time in the POSS thiol mixture. 1,2-Benzenediol showed no inhibition effect, while butylated hydroxyanisole completely inhibited the polymerization reaction, rendering the formulation inert to UV exposure. Only m-cresol displayed a slight inhibition effect, delaying the onset of detectable POSS thiol polymerization by stainless steel catalysis to 5 days.

Several common surface treatment techniques were tested to determine their effectiveness in passivating the exposed stainless steel surface and preventing the polymerization of POSS thiol. HMDS, FSAM, and propanethiol surface treatments did not prevent the steel catalyzed POSS thiol polymerization. Evershield, an aviation steel surface passivation agent, produced a visible glossy coating on the stainless steel test surface, but still did not prevent the POSS thiol polymerization.

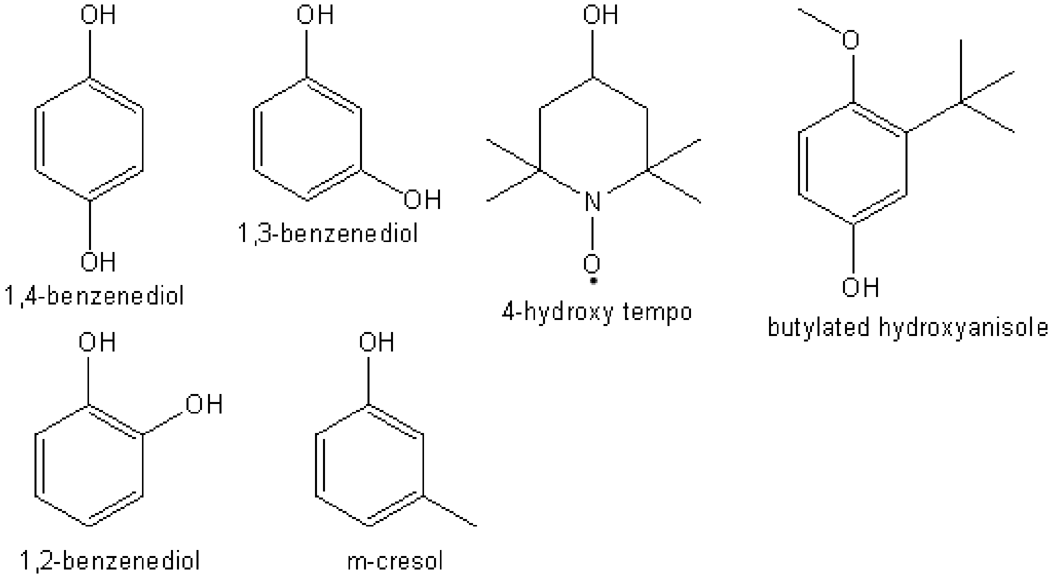


Figure 4.21: Radical inhibitors tested for suppression of the stainless steel catalyzed POSS thiol polymerization.

The polymerization of the POSS thiol formulation by the stainless steel pump parts caused a reduced shelf life of the POSS thiol material in the Imprio 55. Nevertheless, imprints were made to continue development of the dispense recipe and S-FIL process condition while reformulation of the POSS thiol material was pursued. Figure 4.22 shows SEM images of imprinted POSS thiol dual damascene structures, showing good pattern replication.

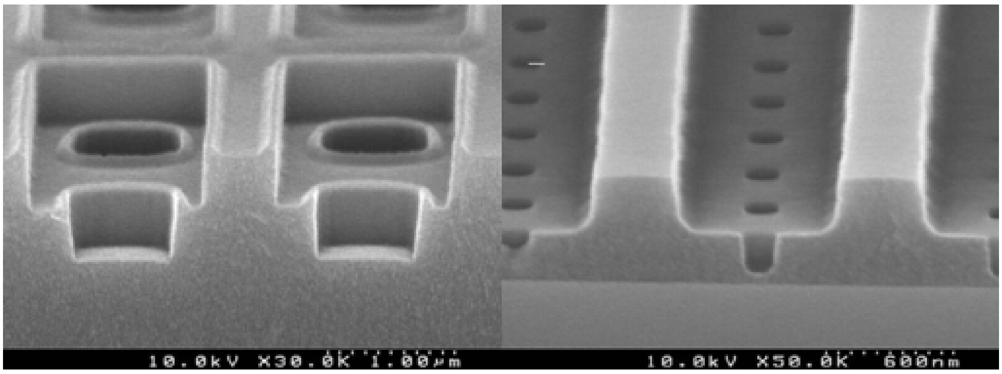


Figure 4.22: SEM images of imprinted POSS thiol samples using the viscous dispense system on Imprio 55.

4.7.3 POSS Thiol Summary

POSS thiol formulations were evaluated for use as an IDM. The use of the homofunctionalized vinyl POSS component improved the synthesis repeatability and avoided the platinum catalyzed coupling reaction compared to the previous dually functionalized POSS acrylate system. The use of a thiol cross-linker and a photoinitiator enabled the photopolymerization of vinyl functionalized POSS without the nitrogen outgassing of the previous POSS azide formulation. The imprinted POSS thiol samples have shown good pattern replication quality. However, several areas of improvement remain before a viable IDM is available.

Current efforts in the development of POSS thiol as IDM focus on improving the imprint quality, thermal stability, and shelf life. Evaluation of alternative thiol compounds with more thiol functional groups per molecule may provide enhanced network density and improve the thermal stability of the cross-linked POSS thiol. Inclusion of siloxane reactive diluents as plasticizers in the POSS thiol formulation may provide improved resistance to crack formation during the high temperature cure process and further reduce the viscosity of the formulation.

Further study of inhibitors is warranted or changes of the viscous dispense pump parts to non-stainless steel material will be required to avoid the steel catalyzed polymerization of the POSS thiol and improve its shelf life in the S-FIL system. Continuing development of viscous dispense and S-FIL process parameters are required to produce imprint samples with uniform and thin residual layers for integration in a copper dual damascene process.

4.8 SUMMARY AND FUTURE WORK

Application of IDM and S-FIL in a copper dual damascene process would reduce the number of deposition, lithography, and etch steps, greatly streamlining the BEOL process and enabling significant potential cost saving.

Several classes of materials have been studied for application as an IDM formulation in S-FIL. The functional sol-gel formulation demonstrated compatibility with the S-FIL process and provided good imprint quality, but suffers from significant mass loss and volume shrinkage during thermal processing. Sol-gel dielectrics were also limited by low mechanical strength, resulting in dishing of the dielectric material during CMP processing. The POSS epoxide formulation demonstrated good imprint pattern quality, good mechanical strength, and promising dielectric properties, but the thermal stability is low. The POSS acrylate formulations nearly met all of the S-FIL and dielectric material requirements of IDM. They demonstrate significantly improved thermal stability compared to POSS epoxide. The repeatability of the synthesis requires improvement and residual platinum catalyst from the POSS acrylate preparation process ultimately precludes its use in functional devices.

POSS azide and POSS thiol were developed to address the synthetic and purification challenges of the POSS acrylate system. POSS azide was quickly found unsuitable for the S-FIL patterning process due to the stoichiometric generation of gaseous nitrogen during the photopolymerization process. The POSS thiol formulation avoided the outgassing of the azide chemistry through use of a thiol cross-linker, enabling the photopolymerization of vinyl silane functionalized POSS. The use of the homofunctional vinyl POSS improved the synthesis repeatability and avoided the platinum catalyzed coupling reaction of the POSS acrylate system. The imprinted POSS thiol samples have shown good pattern replication quality.

Continuing development of the POSS thiol material is warranted but improvements in mechanical properties and storage stability are required. Several approaches are being explored to solve these problems, including reformulation of the POSS thiol with new multi-thiol cross-linkers and reactive diluent plasticizers, changing of pump parts to avoid exposure of POSS thiol to stainless steel surfaces, and study of other potential inhibitor additives. To demonstrate the feasibility of the imprintable dielectric material strategy, improvement of the viscous dispense and S-FIL process parameters is needed to produce functional IDM imprint samples with uniform and thin residual layers. The mechanical, thermal, and electrical properties of the imprinted, cured, and metallized IDM interconnect structure need to be tested to determine its applicability in a manufacturing BEOL process.

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Chapter 5: Dual-Tone, Thermally Activated Photoresist for Flexible Substrates Patterning

The fabrication of electronic devices on flexible substrates represents an opportunity for the development of display technologies, large area devices, and roll-to-roll manufacturing processes. Traditional photolithography encounters alignment and overlay limitations when applied to flexible substrates. One solution is the imaging of two device layers in a single lithographic exposure. Prior work on dual-tone photoresists introduced formulations capable of storing two independent images. However, the reported systems are incompatible with the reactive ion etch processes commonly used today. A new dual-tone photoresist system was developed to enable the simultaneous patterning of two device layers in one layer of photoresist, distinguished by the incident exposure light wavelength, while remaining compatible with the reactive ion etch process.

5.1 INTRODUCTION

The invention of thin-film transistors (TFT) in 1962 [1] closely followed the invention of metal-oxide-semiconductor field-effect transistors (MOSFET) in 1960 [2]. While both are variants of field-effect transistors, the TFT is made by deposition of all components including the semiconductor upon an insulating substrate. This is in contrast to the conventional MOSFET where the semiconductor material typically is the substrate, such as a silicon wafer. The TFT was first demonstrated in 1962 by Paul Weimer and proposed as an alternative technique for integrated circuits fabrication [1]. The use of an insulating substrate such as glass plates permits an array of circuits of nearly unlimited size to be fabricated on a single continuous support, whereas the size of a MOSFET device is limited by the size of the available single crystalline silicon wafers.

In the five decades since the invention of MOSFET and TFT, the microelectronics technology has revolutionized all aspects of computing and communication. MOSFETs found widespread use as the most common transistor in both digital and analog electronic devices. The dominance of the MOSFET design can be attributed to the microelectronics industry's continuous drive for miniaturization. The design of MOSFET permits an increase in computing power and a decrease in production cost as the device size shrinks [3], allowing the MOSFET devices to fully benefit from the ever shrinking microelectronic lithography technology. In contrast, the large area capability of the TFT design does not benefit from miniaturization efforts, relegating TFT technology to niche applications.

In recent years, development of enlarged system scales has renewed interest in the TFT technology. An example of such large scale electronic devices is the flat-panel display. In the modern active-matrix LCD flat-panel displays, the active display area of a common 60 inch LCD TV is 9924 cm^2, which greatly exceeds the 707 cm^2 surface area of the largest commercial silicon wafers (Figure 5.1) and excludes the use of the MOSFET process. The fabrication of these large scale electronics, known as macroelectronics, represents an opportunity for developing novel lithography technology.

Figure 5.1: Comparison of the surface area of a common 60 in LCD flat screen TV to a 300 mm silicon wafer. Illustrations are drawn to scale.

5.1.1 Macroelectronics

Macroelectronics are electronic devices in which the electronic circuitries are distributed and integrated over large area substrates. Examples of macroelectronics applications include flat-panel displays, solar cell arrays, and medical x-ray imagers. In these applications, the device requires control circuitries at every functional element (display pixel, solar photo diodes, and x-ray sensor) spread out over a large surface area, with sizes much bigger than the conventional semiconductor wafers. Consequently, most of the macroelectronics are made by the TFT techniques.

As originally developed by Paul Weimer, most current TFT macroelectronics are built on rigid insulating substrates such as glass [1]. The rigid substrate provides electrical isolation between the electronics and structural support to the entire device. The transistor layer provides power, switching, computation and communication. The functional front plane is built on top of the transistors. The function may be a liquid crystal, a photovoltaic cell, light sensing device, etc. A cap layer seals the device and protects it. Because of the comparatively thin transistor and functional layers, the bulk of the macroelectronics device is due to the substrate and cap layer [4]. Therefore, there is a growing effort to develop alternatives to the bulky rigid substrates.

5.1.2 Flexible Substrate

One of the emerging technologies in electronics fabrication is the manufacturing of the electronic devices directly on a flexible substrate, such as metal foil or polymer film. The flexible substrate offers several benefits over the conventional rigid substrate, such as flexibility, durability, portability, and reduced packaging size. The flexibility of the device allows its application to variable surface and structure contours, improves its ruggedness to the day-to-day handling, permits its folding or rolling up for storage and transportation, and reduces the need for extra protective casing to shield the substrate [5].

A flexible substrate also enables the use of a roll-to-roll manufacturing technique, providing a large area continuous fabrication process and lower production cost.

The growing applications of macroelectronics and the benefits of flexible substrates have spurred developments that combine these two technologies. In addition to improving the existing macroelectronics products, some of the potential new applications of flexible macroelectronics, such as flexible display, printable thin-film photovoltaic cell, large aperture radar, etc. are shown in Figure 5.2.

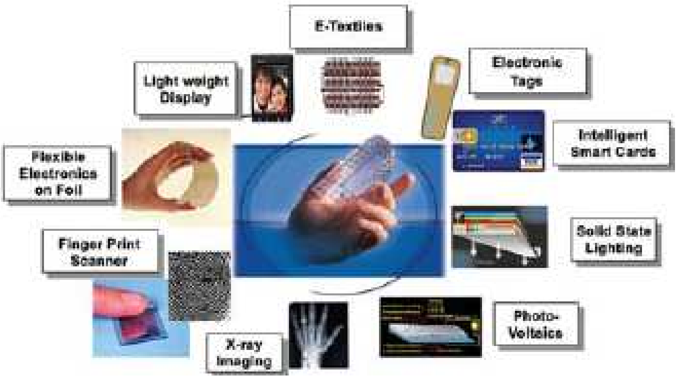


Figure 5.2: Potential applications of flexible macroelectronics [5]. *Image courtesy of IEEE.*

5.1.3 Overlay and Alignment Challenges

The patterning of electronic structures on a pliable substrate is one of the key challenges to the development of flexible macroelectronics. Traditional microelectronics lithography relies heavily on the rigid substrate to provide a dimensionally stable platform for accurate alignment and overlay control between the layers of electrical structures (Figure 5.3). With a flexible substrate such as a metal foil or polymer film, the mismatch in the coefficient of thermal expansion between the substrate and the semiconductor layers combined with the environmental stress that occurs during the semiconductor processing and handling produces variable distortions in the patterned structures (Figure 5.4). These distortions significantly reduce the accuracy of alignment and overlay that is required between lithography steps to obtain smaller feature sizes and higher performances [6,7].

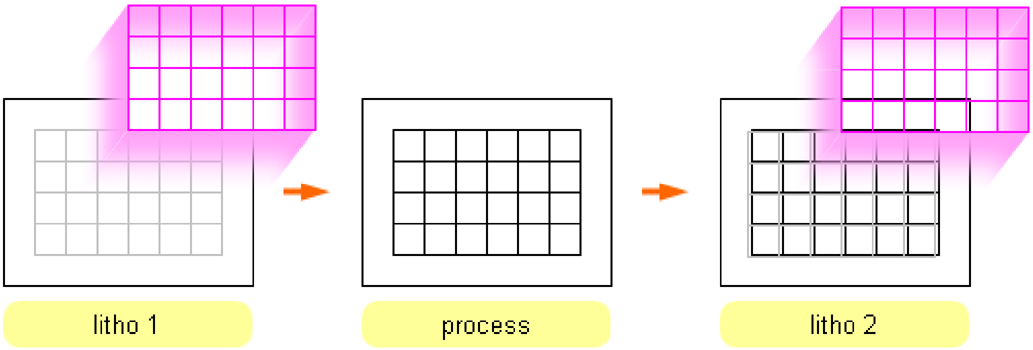


Figure 5.3: Lithography on rigid substrates such as silicon wafers or glass plates. The stiffness of the substrate provides a dimensionally stable platform to accurately align successive layers of patterns.

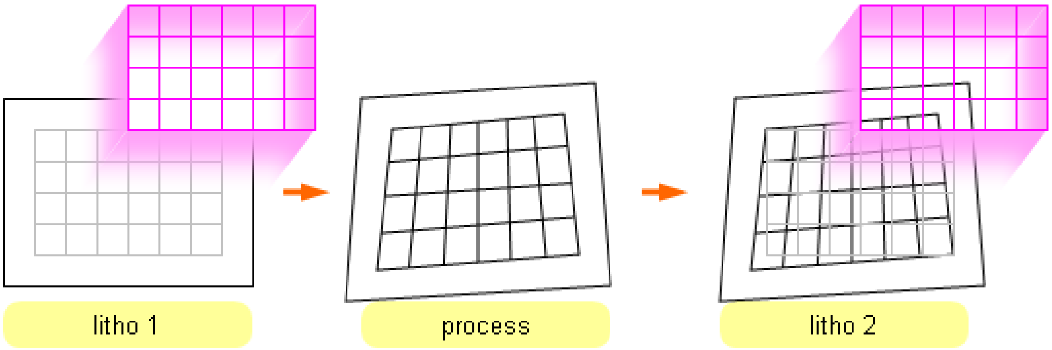
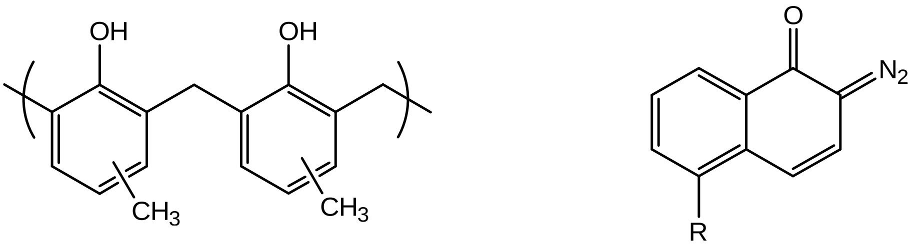


Figure 5.4: Lithography on flexible substrates such as polymer films or metal foils. The flexibility of the substrate produces variable distortions from the stress generated during the semiconductor processing. The distortions adversely impact the alignment accuracy between successive layers of patterns.

One solution to the challenge of overlay alignment on flexible substrates is the use of self-aligned photolithography that patterns two layers of device structures in one lithographic exposure step [8]. The simultaneous imaging of two device layers minimizes the impact of substrate distortions on the device overlay errors, moving control of the layer-to-layer overlay error to on-mask feature alignment or mask-to-mask alignment during the one lithographic step and thereby improving the overlay capability of the process.

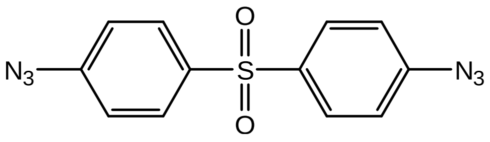
5.2 DUAL-TONE PHOTORESIST

To enable the simultaneous imaging of two device layers, a new photoresist system was needed, one capable of storing two different latent images and correctly transferring them into the substrate during the subsequent etch processes. Hinsberg *et al.* have reported an example of such a system [8,9] (Figure 5.5) composed of a novolak polymer resin, a positive-tone diazonapthaquinone (DNQ) photoactive compound (PAC), as well as a negative-tone sensitizer, 4-4'-bis(azidophenyl)sulfone.



novolak polymer

diazonapthaquinone (DNQ)



4-4'-bis(azidophenyl)sulfone

Figure 5.5: Components of the dual-tone photoresist system by Hinsberg *et al.* [8], consisting of novolak polymer, DNQ PAC, and 4-4'-bis(azidophenyl)sulfone photosensitizer.

Such a dual-tone photoresist system exhibits spectral selectivity, as its exposure response is determined by the wavelength of the incident UV light. In the photoresist system reported by Hinsberg *et al.*, areas exposed to only near-UV wavelength light undergo photo-decomposition of the DNQ PAC. In these areas the novolak polymer becomes more soluble in aqueous base developer, producing the positive-tone image. In areas exposed with mid-UV wavelength light, the novolak polymer undergoes cross-linking reactions mediated by the bis(azidophenyl)sulfone sensitizer, reducing photoresist's solubility in basic developer and producing the negative-tone image. Lastly, in areas exposed to both near-UV and mid-UV light, the dissolution inhibition effect of the cross-link reactions is found to overwhelm the dissolution promotion effect of photo-decomposed PAC, such that the photoresist responds in negative-tone.

This spectral selectivity enables the dual-tone photoresist to store two distinct latent images based on the wavelength of the incident exposure light, allowing the patterning of two device structures in one lithographic exposure step.

5.2.1 Lithographic Process with Dual-tone Photoresist

An example of a self-aligned lithography process with dual-tone photoresist is shown in Figure 5.6. During the exposure step (Figure 5.6a), a dichromatic photomask containing two sets of device designs simultaneously exposes different photoresist regions to different wavelengths of UV light. One set of the design is transmitted by the filtered sections of the photomask, producing the positive-tone response in the dual-tone photoresist. The second set of the design is transmitted by the transparent of the photomask, producing the negative-tone response in those regions of the photoresist [9]. The photoresist is first developed to realize the positive-tone latent images (Figure 5.6b) and then etched (Figure 5.6c) to transfer the positive-tone structures into the substrate. The photoresist is then developed again to realize the negative-tone latent images (Figure 5.6d) and etched (Figure 5.6e) to transfer the negative-tone structures on top of the previous positive-tone structures.

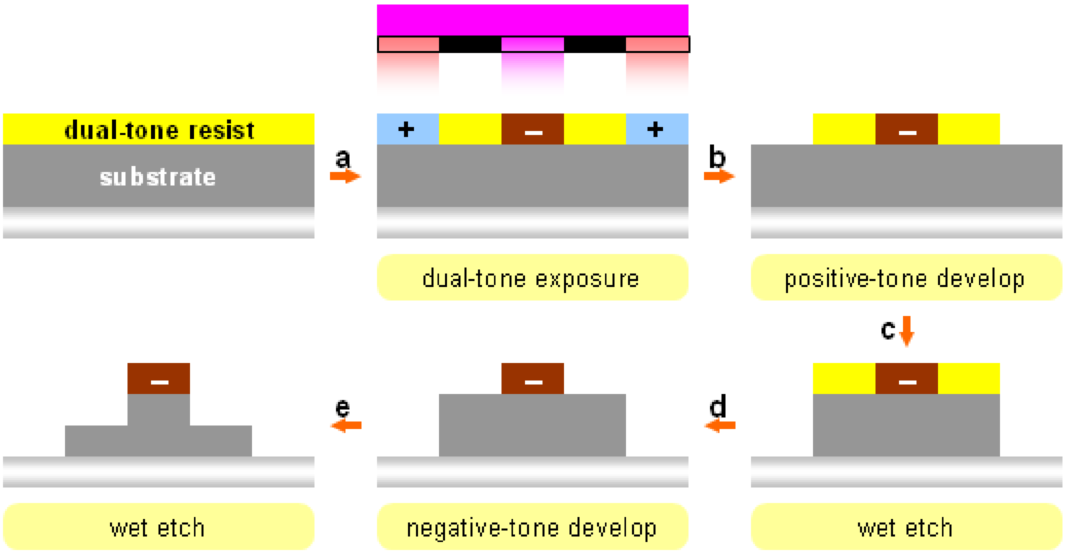


Figure 5.6: Overview of the dual-tone lithography for patterning of self-aligned structures.

As illustrated in Figure 5.6, two device designs are simultaneously imaged into the dual-tone photoresist using a dichromatic photomask. The simultaneous imaging of the two device layers avoids the effects of substrate distortions between conventional photolithography layers and moves the control of the layer-to-layer overlay errors to on-mask feature alignments. Since the typical on-mask feature alignment errors are considerably smaller then the layer-to-layer misalignments or substrate distortions, the dual-tone lithography with dichromatic photomask significantly improves the overlay capability of the process.

Alternatively, it is possible to carry out dual-tone exposure using binary photomasks instead of dichromatic photomask. Instead of single exposure with one dichromatic photomask to produce both the positive-tone and the negative-tone latent images (Figure 5.7a), the dual-tone photoresist is exposed sequentially using two binary photomasks and different wavelengths of UV light to produce the similar positive-tone and negative-tone latent images (Figure 5.7b).

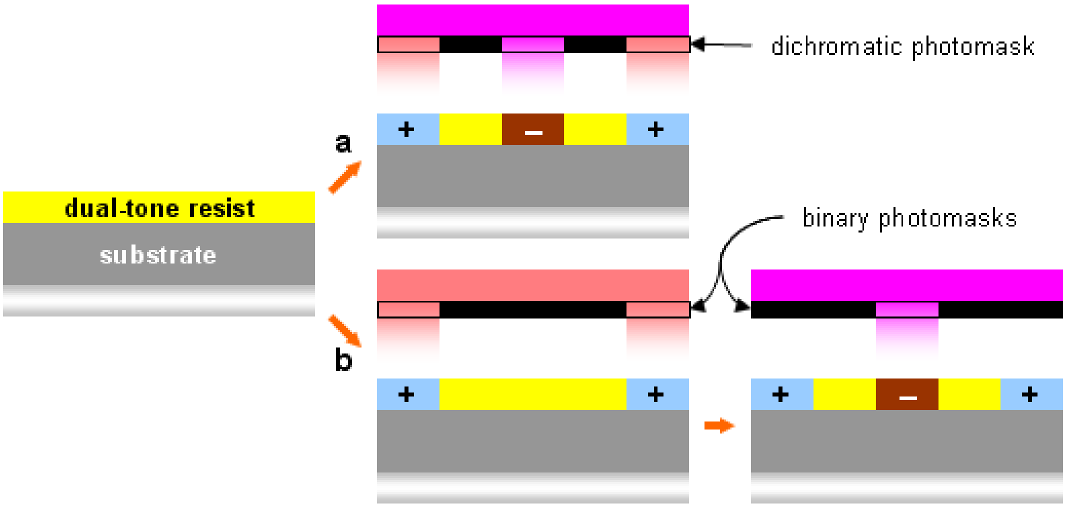


Figure 5.7: Two dual-tone exposure schemes: a. Single exposure with one dichromatic photomask. b. Two sequential exposures with two binary photomask and different wavelengths of UV light.

The sequential aligned exposures with two binary photomasks are usually done without unloading the substrate between the exposures in a typical manufacturing process. This minimizes the effect of substrate distortion and incurs only mask-to-mask alignment errors between the two patterns. While the typical mask-to-mask misalignment is slightly worse than the on-mask alignment error of a single photomask, it is still significantly better than the layer-to-layer misalignments in a flexible substrate, thereby improving the overlay capability of the process.

The use of two binary photomasks offers potential savings on the photomask costs due to their simple chromium on glass fabrication process, but increases the operating cost of the exposure step due to its need for two UV exposures (one exposure for each binary photomask). For the dual-tone photoresist development, sequential exposures with binary photomasks are used for the print tests described in the following sections.

5.2.2 Reactive Ion Etch Process Compatibility

Note that in the process described in Figure 5.6, a portion of the unexposed and the negative-tone latent image photoresist must withstand the develop and etch steps (Figure 5.6b and Figure 5.6c). In the photoresist system reported by Hinsberg *et al.*, a wet etch process was used to transfer the positive-tone image into the substrate, while maintaining the negative-tone image in the photoresist. However, when a reactive ion etch (RIE) process is applied for the same etch transfer of positive-tone image, the negative-tone latent image is lost. The loss of the latent image is attributed to the production of UV radiation by the etchant gas plasma during the RIE process, resulting in the unintentional flood exposure of the photoresist as it is being etched. This flood exposure activates the cross-linking reaction between the novolak polymer and the negative-tone sensitizer, producing a negative-tone response in the entire photoresist film and erasing the negative-tone latent image, as shown in Figure 5.8.

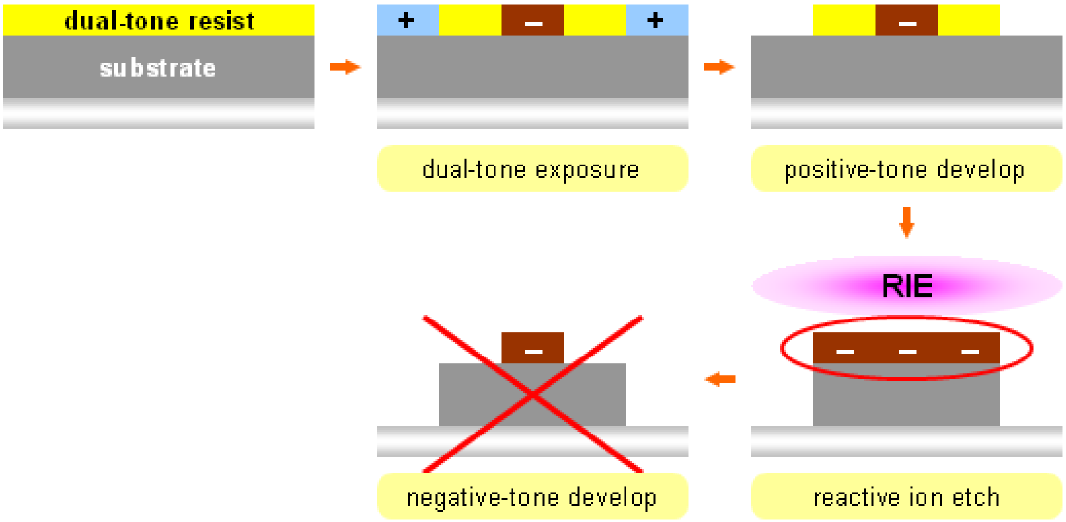


Figure 5.8: The dual-tone lithography with reactive ion etch. The UV radiation generated by the etchant plasma during the RIE process flood exposes the dual-tone photoresist, resulting in the lost of the negative-tone latent image.

5.3 DUAL-TONE, THERMAL ACTIVATED PHOTORESIST

To mitigate the lost of the negative-tone latent image during the RIE plasma etch process, we designed a variation on the above-mentioned novolak/PAC based dual-tone photoresist system, which incorporates a thermally activated, chemically amplified cross-linker and a photoacid generator. In this design, the photoacid generator provides the spectral selectivity for the negative-tone response, while the thermally activated cross-linker imposes an additional bake requirement for the activation of the cross-link reaction and the realization of the negative-tone latent images.

5.3.1 Lithographic Process with Dual-tone, Thermally Activated Photoresist

Figure 5.9 illustrates a self-aligned lithography process using the dual-tone, thermally activated photoresist. The post-exposure bake step enables the acid-catalyzed cross-linking reaction between the cross-linkers and the novolak polymer, completing the negative-tone response of the photoresist. In contrast, the lack of a bake step after the RIE process prevents the cross-linking reaction from occurring in the flood exposed photoresist, thereby allowing the negative-tone latent image to survive the RIE process. Consequently, the post-exposure bake requirement of the cross-linker provides differentiation between the intentional negative-tone exposure of the dual-tone lithography and the unavoidable flood exposure during the RIE process.

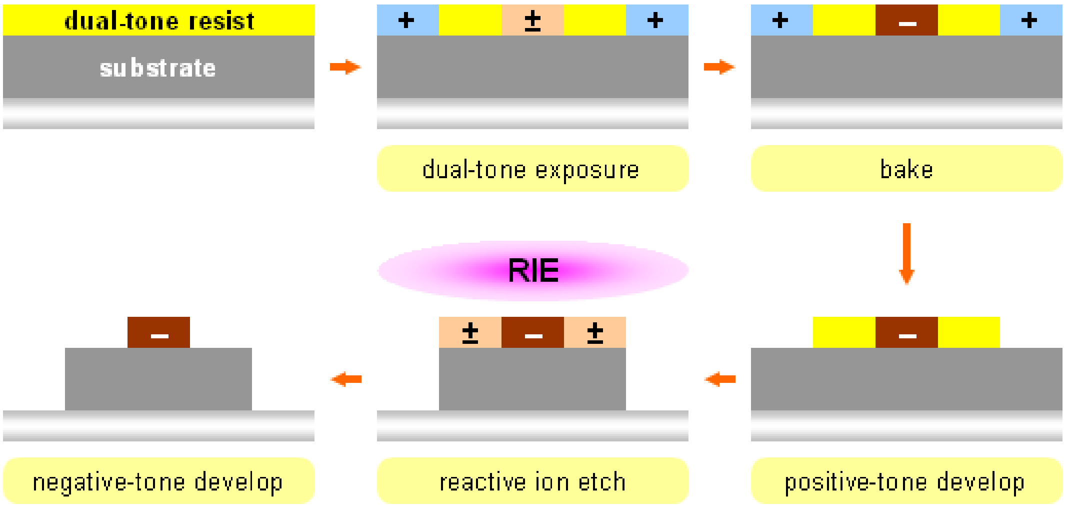
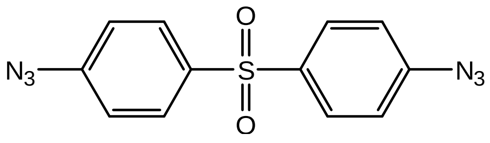


Figure 5.9: The dual-tone, thermally activated photoresist with reactive ion etch process. The post-exposure bake requirement for the negative-tone response provides the differentiation between the intentional negative tone patterning and the flood exposures in the RIE process.

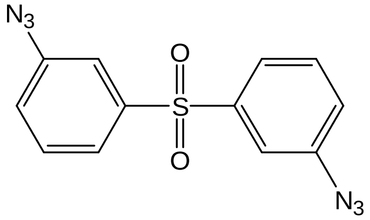
Several chemicals were evaluated for their suitability as the cross-linker and PAG in the development of the dual-tone photoresist. The results of these experiments are described in the following sections.

5.3.2 Cross-linker

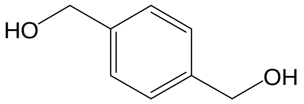
The cross-link additive enables the novolak resin in the photoresist to undergo cross-linking, reducing its solubility in the developer solvent and imparting a negative-tone response into the photoresist system. Several candidate compounds, shown in Figure 5.10, were tested for their compatibility with the novolak / DNQ photoresist formulation and their cross-linking performance.



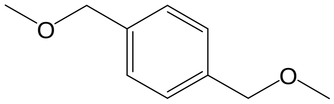
bis(4-azidophenyl) sulfone



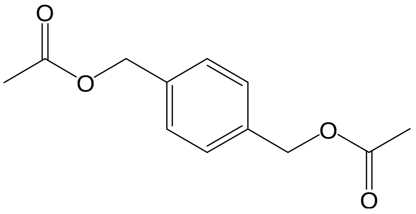
bis(3-azidophenyl) sulfone



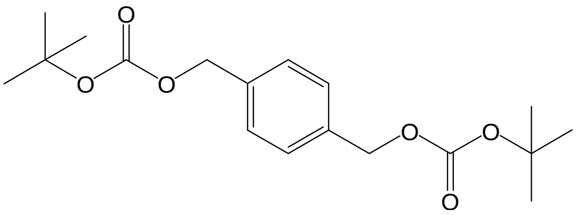
1,4-benzenedimethanol



1,4-bis-methoxymethyl-benzene



1,4-bis-acetoxymethyl-benzene



1,4-bis-tertbutoxycarbonyloxymethyl-benzene

Figure 5.10: Cross-linker candidates for the development of dual-tone photoresist.

Both bis(4-azidophenyl) sulfone and bis(3-azidophenyl) sulfone cross-linkers had poor solubility in PGMEA, a standard solvent for the commercial novolak photoresist; as a result neither formulation produced sufficient cross-linking to enable a negative-tone photoresist response.

The 1,4-benzenedimethanol and its derivatives (1,4-bis-methoxymethyl-benzene, 1,4-bis-acetoxymethyl-benzene, and 1,4-bis-tertbutoxycarbonyloxymethyl-benzene) all have moderate solubility in PGMEA, and successfully produced a negative-tone response with the application of acid and heat. The derivatives differ in the acid labile protecting group used to cap the methanol cross-link functionality: methoxy, acetoxy, and tertbutoxycarbonyloxy (t-boc). The influence of the protecting groups on the negative-tone response of the dual-tone photoresist was measured by the change in the threshold post exposure bake (PEB) temperature required for the negative-tone cross-link reaction. The effects of the different protecting groups were found to be less than expected. As shown in Figure 5.11, the change in threshold PEB temperature across the four different cross-linkers was less than 20 °C, and all of the structures were able to produce sufficient cross-linking reactions at 110 °C PEB temperature to realize the negative-tone image. As a result, the commercially available 1,4-benzenedimethanol (Sigma-Aldrich Co), was chosen for all subsequent dual-tone photoresist formulations.

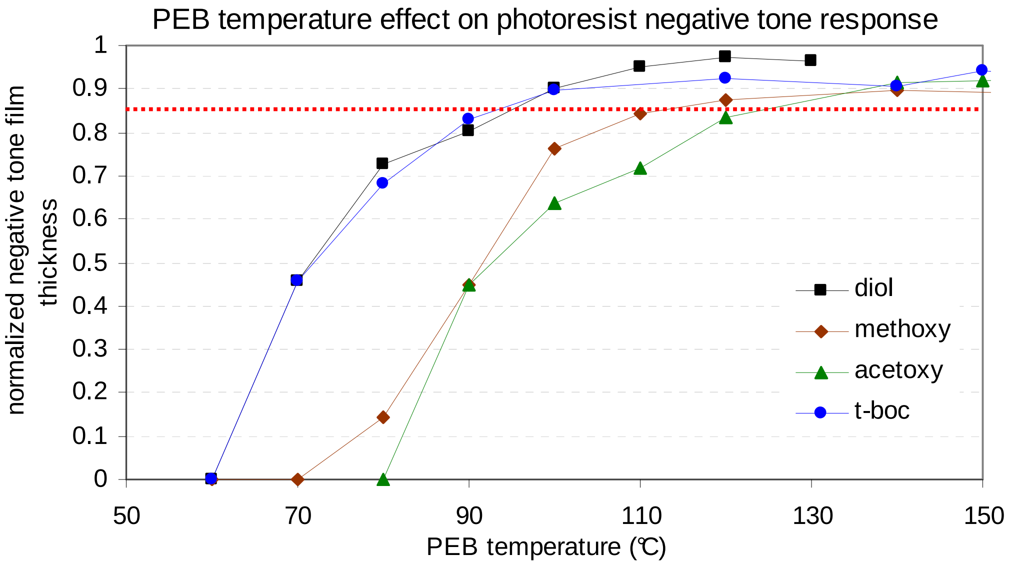


Figure 5.11: Negative-tone exposure response as a function of post-exposure bake (PEB) temperature for cross-linkers with different protecting group.

5.3.3 Photoacid Generator

The photoacid generator (PAG) additive provides the acid catalyst that initiates the negative-tone exposure response of the photoresist. During UV light exposure, the

PAG undergoes photolysis, producing a latent image of strong acid. Upon subsequent heating of the photoresist, the acid generates benzylic carbocations from the cross-linkers. These carbocations can react with the phenolic units of the novolak polymer, forming ether linkages in addition to performing electrophilic aromatic substitution chemistry yielding carbon-carbon bond cross-links within the polymer matrix [10]. The cross-linked novolak polymer becomes less soluble to the aqueous base developer, producing the negative-tone image. The PAG and its UV absorption spectrum were chosen to allow spectral differentiation of the negative-tone exposure response from that of the positive-tone PAC.

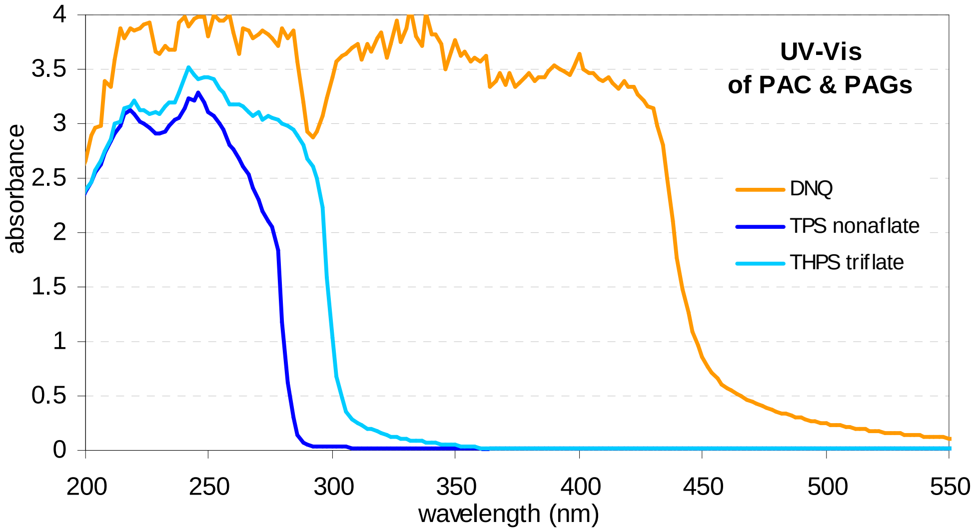


Figure 5.12: UV-Vis absorption spectra of photoacid generators (TPS nonaflate and THPS triflate) and photoactive compound (DNQ).

As shown in Figure 5.12, the positive-tone additive, DNQ has a broad absorption from 200 to 440 nm, while triphenylsulfonium perfluorobutanesulfonate (TPS nonaflate), a commercially available PAG, absorbs only up to 290 nm. Initial print tests of dual-tone photoresist with TPS nonaflate demonstrated good negative-tone exposure response, produced the negative latent image as designed and were capable of tolerating the RIE process. However, it was soon noted that the addition of the negative-tone additives into the novolak / DNQ formulation significantly reduces the dissolution rate of the novolak polymer in aqueous base developer, suppressing the photoresist's positive-tone exposure response. Early attempts to compensate for the reduced dissolution rates included larger exposure doses and develop times, but produced other problems such as blurred images and photoresist swelling. A series of test prints were performed to evaluate the impact of various negative-tone additives on the positive-tone dissolution rate of the novolak / DNQ photoresist after exposure.

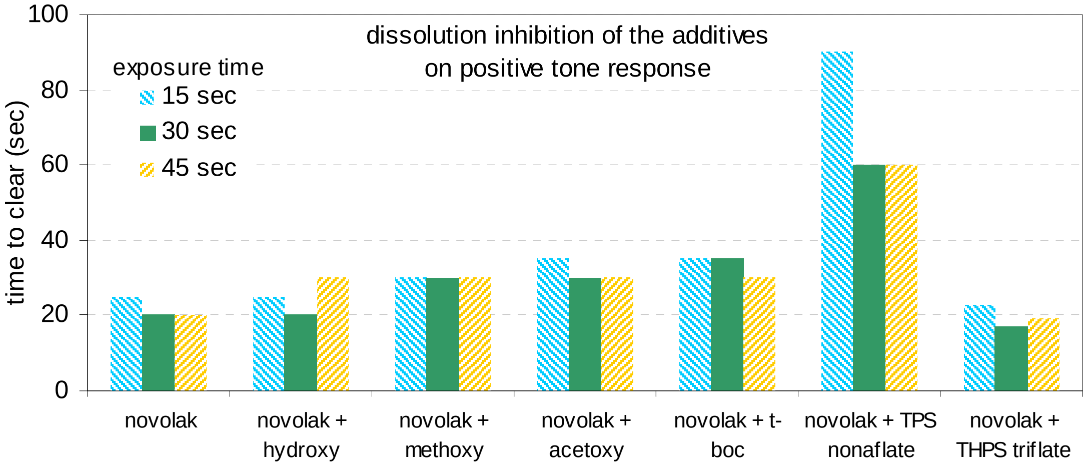
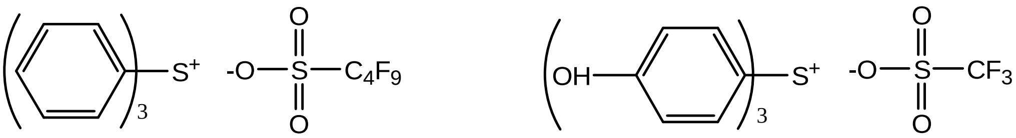


Figure 5.13: Positive-tone dissolution rates of the novolak / DNQ photoresists with various cross-linker and PAG additives.

Figure 5.13 shows the time required for the positive-tone exposed region to fully dissolve in the aqueous base developer for several combinations of novolak / DNQ photoresist with PAGs and cross-linkers. The addition of the TPS nonaflate was found to be the most significant contributor to the suppression of the positive-tone dissolution rate, tripling the required develop time; while the cross-linkers yielded comparatively minor increases in develop time. This phenomenon has been reported previously and exploited in the design of positive-tone photoresists by Chambers *et al.* [11].



triphenylsulfonium perfluorobutanesulfonate

tris(4-hydroxyphenyl)sulfonium trifluoromethanesulfonate

Figure 5.14: PAG candidates for the development of dual-tone photoresist.

The dissolution inhibition effect of the TPS nonaflate can be mitigated by rendering the PAG molecule base soluble. This was accomplished by introducing phenolic hydroxyl groups on the phenyl groups of the PAG as shown in Figure 5.14. The resulting compound, tris(4-hydroxyphenyl)sulfonium trifluoromethanesulfonate (THPS triflate), is freely soluble in aqueous base and has a UV absorption drop off around 310 nm (Figure 5.12), similar to that of TPS nonaflate. This enabled spectral differentiation of THPS triflate from the positive-tone DNQ during the exposure process. In print tests, THPS triflate did not exhibit any dissolution inhibition effects. The dual-tone photoresist formulation with THPS triflate PAG had a positive-tone development rate comparable to the original novolak resins (Figure 5.13), while maintaining its negative-tone response capability.

Although the THPS triflate PAG is ideally suited for the dual-tone photoresist application, it is not yet commercially available. Therefore, functional formulations of the dual-tone photoresist for process development and patterning tests were prepared using TPS nonaflate as PAG. Several formulations were prepared with different amounts of TPS nonaflate PAG and printed to optimize the effects of TPS nonaflate loading on the photoresist's exposure responses. The positive-tone dissolution inhibition effects were quantified by measuring the fraction of the positive-tone exposed photoresist film remaining after the development in aqueous base developer. The negative-tone exposure response was quantified by the fraction of the negative-tone exposed photoresist film lost during the same development period. These data are presented in Figure 5.15.

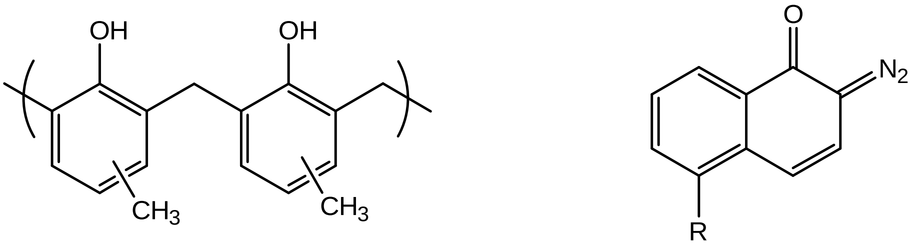
wt% of TPS-Nf	develop time	original film	positive-tone		negative-tone	
			film	% remain	film	% loss
12.07	180	1370	120	8.8	1360	0.7
12.07	180	1400	300	21.4	1370	2.1
12.07	180	1300	360	27.7	1230	5.4
4.98	60	1170	300	25.6	1150	1.7
4.98	60	1150	590	51.3	1150	0.0
3.98	60	1040	0	0	960	7.7
3.98	60	1070	0	0	1000	6.5
2.97	60	1020	0	0	990	2.9
2.97	60	1000	0	0	990	1.0

Figure 5.15: TPS nonaflate PAG loading test data.

Reducing the TPS nonaflate PAG loading reduces its positive-tone inhibition effect. Both the 3% and the 4% PAG loading samples developed completely. The TPS nonaflate loading does not show strong influence on the negative-tone photoresist film loss during development. Therefore, a 3 wt% loading of TPS nonaflate PAG was used in all functional formulations of the dual-tone photoresist.

5.3.4 Dual-tone, Thermally Activated Photoresist Formulation

Based on the evaluation of the candidate cross-linkers and PAGs, the functional formulation of the dual-tone, thermally activated photoresist consists of a commercial novolak polymer with DNQ PAC in PGMEA solvent, 3 wt% of TPS nonaflate PAG, and 5 wt% of 1,4-benzenedimethanol cross-linker (Figure 5.16). This photoresist was used for the subsequent dual-tone lithography and etch process development and functional device print tests.



novolak polymer

diazonapthaquinone (DNQ)

1,4-benzenedimethanol

triphenylsulfonium

perfluorobutanesulfonate

Figure 5.16: Components of the dual-tone, thermally activated photoresist system, consisting of novolak polymer, DNQ PAC, 1,4-benzenedimethanol cross-linker, and TPS nonaflate PAG.

5.4 EXPERIMENTAL

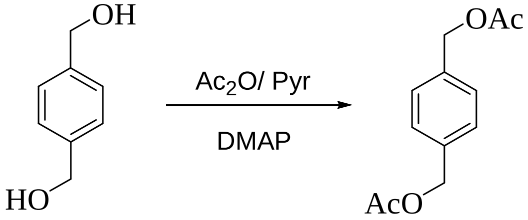
5.4.1 Material Sources and Synthesis Methods

The i-line positive-tone photoresist (notebook 1856-7C2, lot 1911-111, Hoechst Celanese Corp, AZ Photoresist Products), consisting of novolak polymer and DNQ PAC in PGMEA solvent, and a sample of TPS nonaflate was obtained as a generous gift from the AZ Electronic Materials. The 1,4-benzenedimethanol cross-linker was purchased from Sigma-Aldrich and used as received. The AZ 300 MIF base developer, consisting of aqueous tetramethylammonium hydroxide (TMAH) solution, was purchased from the AZ Electronic Materials USA.

A sample of tris(4-hydroxyphenyl)sulfonium chloride was obtained as a generous gift from the BASF SE company. Synthesis of the THPS triflate was done by anion metathesis of tris(4-hydroxyphenyl)sulfonium chloride and silver trifluoromethanesulfonate.

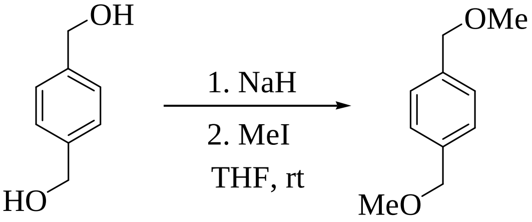
The 1,4-benzenedimethanol derivative cross-linkers were prepared with the following synthesis methods: All reactions were conducted under a positive nitrogen atmosphere with oven-dried glassware unless otherwise stated. Dry DCM, TEA, and pyridine were obtained by distillation over CaH_2 while dry THF was obtained by distillation over Na/benzophenone. All ^{1}H and ^{13}C NMR spectra were recorded on a Varian Unity Plus 300 MHz instrument. All chemical shifts were reported in ppm downfield from TMS using the residual protonated solvent as an internal standard ($CDCl_3$, ^{1}H 7.26 ppm and ^{13}C 77.0 ppm). HRMS (CI) was obtained on a VG analytical ZAB2-E instrument. IR data were recorded on a Nicolet Avatar 360 FT-IR and all peaks are reported in cm^{-1}. All chemicals were purchased from Sigma-Aldrich and used as received unless otherwise stated.

1,4-bis-acetoxymethyl benzene:



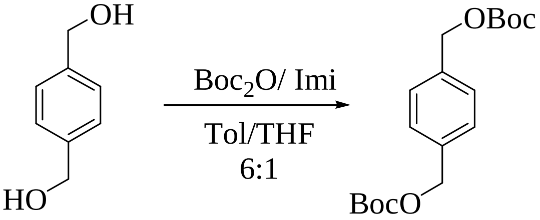
A 50 mL RBF was charged with dimethylaminopyridine (88 mg, 0.7 mmol), acetic anhydride (13.7 mL, 145.0 mmol), pyridine (11.7 mL, 145.0 mmol), 1,4-benzenedimethanol (2.0 g, 14.5 mmol), and a stir bar. This solution was stirred at rt for 24 h then diluted with ether (200 mL). The organic layer was thoroughly rinsed with 1 *M* KOH (4 x 100 mL), followed by rinsing with 1 *M* $CuSO_4$ (2 x 50 mL). The organic layers were combined, dried over $MgSO_4$, and concentrated *in vacuo* to yield 1,4-bis-acetoxymethyl-benzene as a white crystalline solid (mp = 54-56 °C) (20.7 g, 89%); ^{1}H NMR ($CDCl_3$) δ ppm: 7.351 (s, 4H), 5.094 (s, 4H), 2.090 (s, 6H); ^{13}C NMR ($CDCl_3$) δ ppm: 170.736, 135.932, 128.386, 65.811, 20.909; IR (NaCl) cm^{-1}: 2960, 2897, 1722, 1227, 1018; HRMS (CI): 245.0787 calc, 245.0784 found.

1,4-bis-methoxymethyl benzene:



A 50 mL RBF was charged with NaH (2.3 g, 57.9 mmol, 60% dispersion in mineral oil), THF (10 mL), and a stir bar. The suspension was vigorously stirred as 1,4-benzenedimethanol (2.0 g, 14.5 mmol) was added slowly at rt. Upon complete evolution of gas, iodomethane (9.0 mL, 145 mmol) was slowly added. The solution was stirred for 24 h, and then the excess iodomethane was removed *in vacuo*. The remaining suspension was dissolved in ether, and the salts were removed by filtration. 1,4-bis-methoxymethyl-benzene was isolated by distillation (75-77 °C, 0.83 torr) in good yield (2.0 g, 81%) as a clear liquid; ^{1}H NMR ($CDCl_3$) δ ppm: 7.301 (s, 4H), 4.425 (s, 4H), 3.351 (s, 6H); ^{13}C NMR ($CDCl_3$) δ ppm: 137.406, 127.546, 74.189, 57.784; IR (NaCl) cm^{-1}:2982, 2925, 2852, 1380, 1123, 1099, 809; HRMS (CI): 165.0916 calc, 165.0922 found.

1,4-bis-tertbutoxycarbonyloxymethyl benzene:



A 100 mL RBF was charged with imidazole (40 mg, 0.6 mmol), di-tert-butyl di-carbonate (758 mg, 3.5 mmol), toluene (30 mL), THF (5 mL), and a stir bar. After stirring for 10 min, 1,4-benzenedimethanol (200 mg, 1.5 mmol) was added, and the reaction was stirred at rt for 48 h. DCM was added to the reaction which was then rinsed with brine, dried over $MgSO_4$, and concentrated *in vacuo*. This crude mixture was subjected to flash column chromatography (9:1 Hex:EtOAc) to yield 1,4-bis-tertbutoxycarbonyloxymethyl-benzene as a white crystalline solid in moderate yield (234 mg, 49.6%); mp = 71-74 °C; ^{1}H NMR ($CDCl_3$) δ ppm: 7.364 (s, 4H), 5.079 (s, 4H), 1.482 (s, 18H); ^{13}C NMR ($CDCl_3$) δ ppm: 153.368, 135.772, 128.373, 82.331, 68.246, 27.739; IR (KBr) cm^{-1}:2984, 1738, 1396, 180, 1157, 1087; HRMS (CI): 339.1808 calc, 339.1810 found.

Procedure adapted from Basel, Y.; Hassner, A. *J. Org. Chem.* **2000,** *65,* 6368-6380.

5.4.2 Lithography Development

Silicon wafers were used for the initial photoresist print tests, and stainless steel foils were used for the final testing of the photoresist on a flexible substrate. The substrates were treated with a commercial adhesion promoter (AP310, Silicon Resources Inc.) to ensure good adhesion between the photoresist and the substrate surface. The photoresists were spin-coated and baked to produce 1um films, then measured using a stylus profilometer (Dektak 6M, Veeco).

The exposures were done with a broadband UV curing system (Novacure, EXFO) operating at 8 mW/cm^2 at the substrate plane. A 345 nm long pass filter was applied above the photomask for the positive-tone exposure, limiting the exposure UV light to those greater then 345 nm wavelengths in the positive-tone regions. Broadband exposure was used for the negative-tone exposure without any filter.

The dual-tone exposure and bake conditions were optimized to allow the positive-tone latent image to develop in less than 60 seconds in the aqueous TMAH developer, while maintaining the negative-tone film loss at less than 5%. The positive-tone image development was marked by the complete dissolution of the photoresist film in the positive-tone exposed region. The negative-tone film loss was measured as the ratio of the negative-tone exposed photoresist film thickness before and after the positive-tone development. Increasing the exposure time and/or dose favorably reduced both the positive-tone develop time and the negative-tone film loss, but adversely lowered the throughput of the dual-tone lithography process. Increasing the post-exposure bake temperature and/or time favorably reduced the negative-tone film loss (Figure 5.11), but had minimal impact on the positive-tone develop time.

Subsequent to development of the positive-tone image, a broadband flood exposure was applied to the entire sample without additional bake to activate the unexposed portion of the photoresist. This flood exposure rendered the unexposed region of the photoresist soluble to aqueous base developer, which was later removed to realize the negative-tone image from the dual-tone exposure step.

5.4.3 Etch Development

The positive-tone and the negative-tone patterns in the photoresist were each transferred into the silicon oxide substrate using the RIE process. A reactive ion etcher (Oracle III, Trion Technology) located in the Microelectronics Research Center (MRC) cleanroom of the J. J. Pickle Research Campus was used for the transfer etch portion of the dual-tone photoresist print tests.

The initial etch condition was based on the previous work by Shahrukh Khan *et al*. at Lehigh University. The etch recipe consisted of a 15 sccm CF_4 and 5 sccm O_2 gas composition, 250 mTorr chamber pressure, and 100 W etch power. This produced a silicon oxide etch rate of 60~70 nm/min on the March etcher at Lehigh University. However, when this etch condition was reproduced on the Trion etcher at the MRC cleanroom, the observed silicon oxide etch rate was only 10 nm/min (Figure 5.17). The root cause of this etch rate discrepancy was determined to be due to the hardware differences between the March plasma etcher at Lehigh University and the Trion RIE etcher at the University of Texas at Austin.

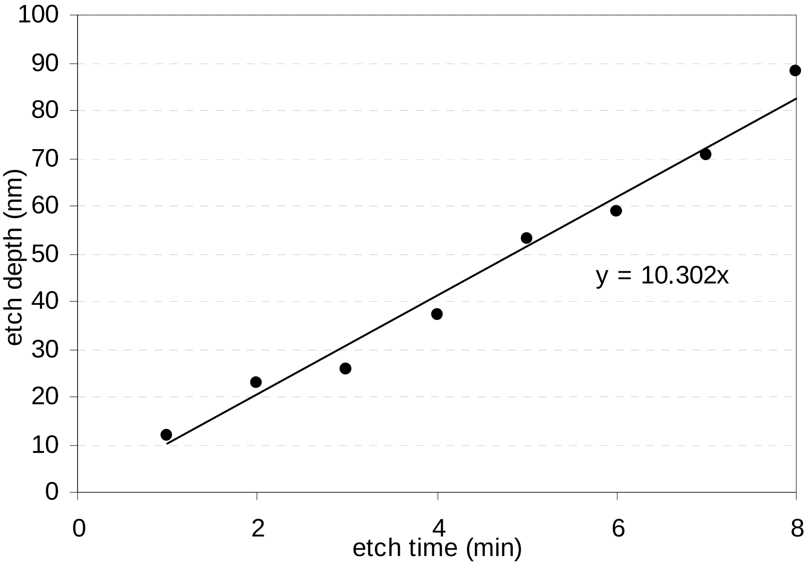


Figure 5.17: Silicon oxide etch rate in the Trion etcher. The etch rate increased linearly with etch time. The following parameters were held constant: 15 sccm CF_4, 5 sccm O_2, 250 mTorr, and 100 W.

In order to establish a baseline process as the starting point for further etch process development, it was necessary to match the etch rates between the Trion and the March etchers. Since it was not feasible to obtain the same March etcher as that of the Lehigh University, a new etch recipe was needed to reproduce the 60~70 nm/min silicon oxide etch rate on the Trion etcher. Several etch experiments were run on the Trion etcher to evaluate etch rates of the silicon oxide / dual-tone photoresist stack as a function of etcher power (Figure 5.18) and etch chamber pressure (Figure 5.19).

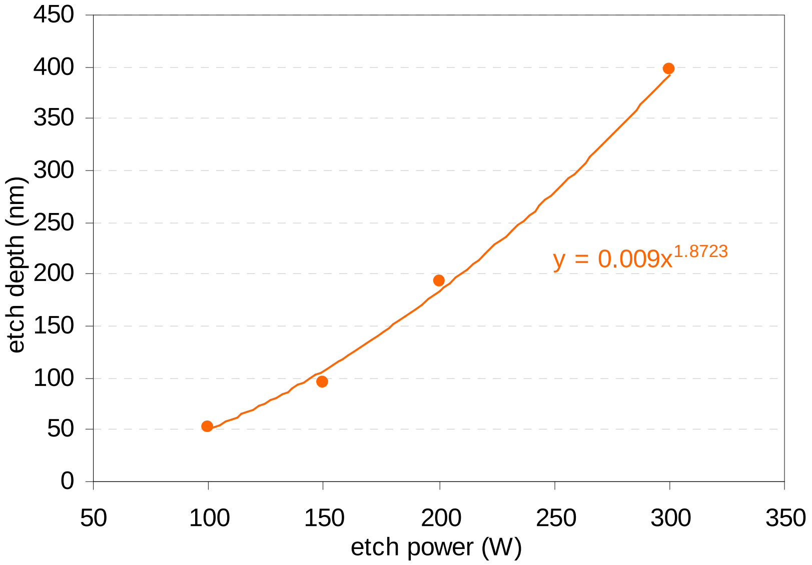


Figure 5.18: Silicon oxide etch depth as a function of etch power in the Trion etcher. The following parameters were held constant: 15 sccm CF_4, 5 sccm O_2, 250 mTorr, and 5 min.

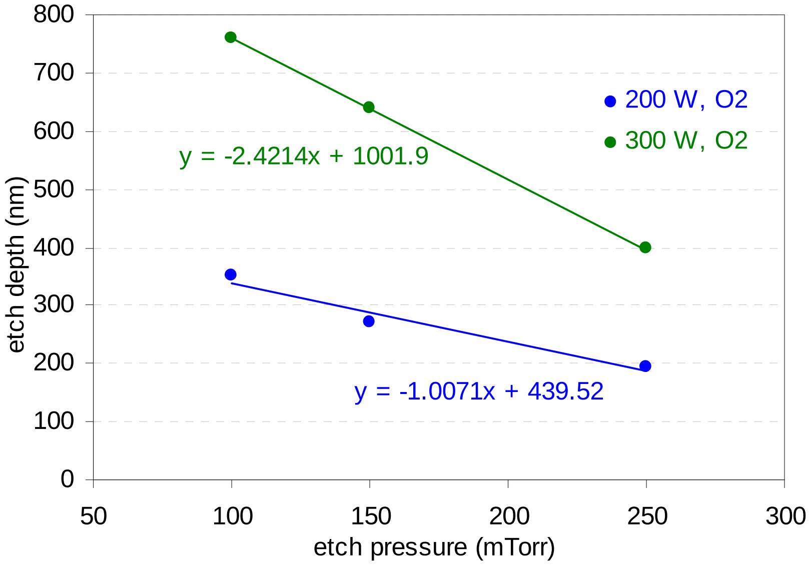


Figure 5.19: Silicon oxide etch depth as a function of etch pressure in the Trion etcher. The following parameters were held constant: 15 sccm CF_4, 5 sccm O_2, and 5 min.

Based on the experimental etch data from the Trion etcher, the etch rate of the silicon oxide film increased exponentially with increasing etch power and decreased linearly with increasing etch pressure. Therefore, the silicon oxide etch rate on the Trion etcher could be increased by increasing the etcher power and decreasing the etch chamber pressure. A new etch recipe of 15 sccm CF_4, 5 sccm O_2, 100 mTorr, and 200 W would provide an etch rate of 70 nm/min, comparable to that of the March etcher. However, closer inspection of the etched wafer samples revealed significant photoresist loss during the silicon oxide etches. Figure 5.20 plots the fraction loss of the photoresist film, showing increasing photoresist loss with the increasing silicon oxide etch rate, as indicated by the increasing etch power and decreasing etch pressure. The photoresist film was lost completely at the 300 W etch power setting, thus capping the fraction of photoresist lost at 1.

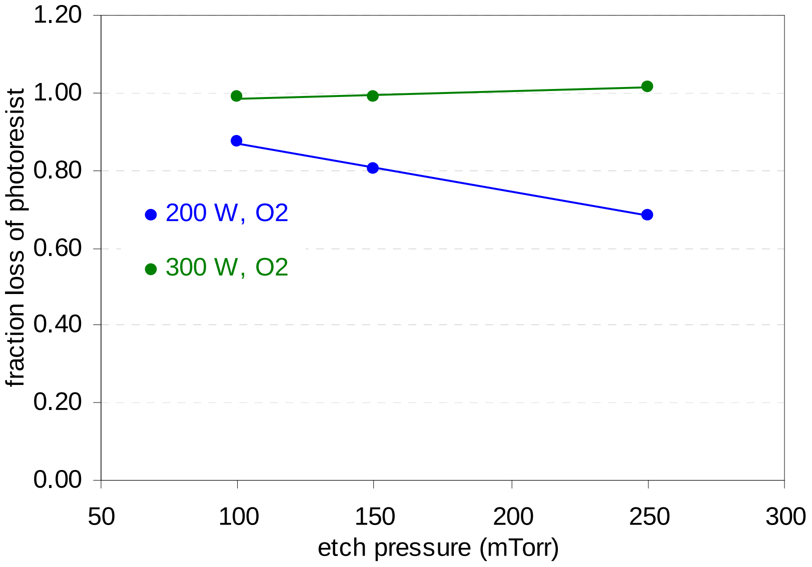


Figure 5.20: Normalized photoresist film lost during silicon oxide etches in the Trion etcher. The following parameters were held constant: 15 sccm CF_4, 5 sccm O_2, and 5 min.

The loss of the photoresist film during the etch process adversely impacted the depth and quality of the etched pattern. As a result, alternative etch gas mixtures were evaluated to study their effects on the photoresist loss (Figure 5.21) and their silicon oxide etch rates (Figure 5.22).

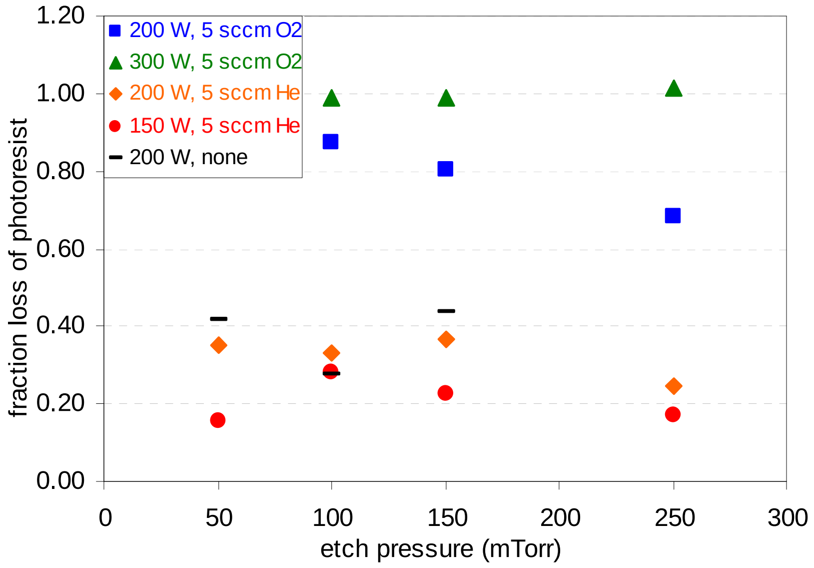


Figure 5.21: Photoresist loss as a function of gas compositions in the Trion etcher. The CF_4/He gas mixture had significantly less photoresist loss than the CF_4/O_2 gas mixture. The following parameters were held constant: 15 sccm CF_4 and 5 min.

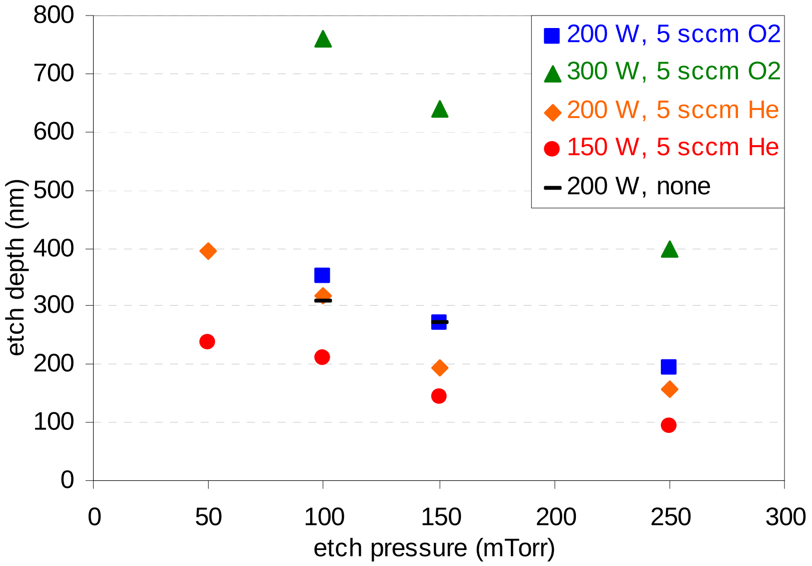


Figure 5.22: Silicon oxide etch rates as a function of gas compositions in the Trion etcher. The choice of the secondary etch gas had no significant impact on the etch rate for a given etch power and pressure. The following parameters were held constant: 15 sccm CF_4 and 5 min.

The etch data shown in Figure 5.21 suggests that the CF_4/He gas mixture had the highest selective between silicon oxide etch and photoresist film loss at a given etch power and pressure, compared to that of the CF_4/O_2 mixture and the pure CF_4 etch gas. Based on the etch data in Figure 5.22, the etch recipe of 15 sccm CF_4, 5 sccm O_2, 50 mTorr, and 150 W has the least photoresist film loss during etch, while producing an etch rate comparable to that of the March etcher. This etch recipe was used for all subsequent dual-tone photoresist print tests.

Etch tests with the patterned photoresist samples also revealed the formation of an insoluble crust on top of the previously unexposed regions of the photoresist film, as shown in Figure 5.23. The aqueous base developer visibly undercuts the photoresist (Figure 5.23B), leaving behind an insoluble crust (Figure 5.23C). This insoluble crust impeded the subsequent negative-tone etch process, introducing irregular etch defects in the etched negative-tone pattern.

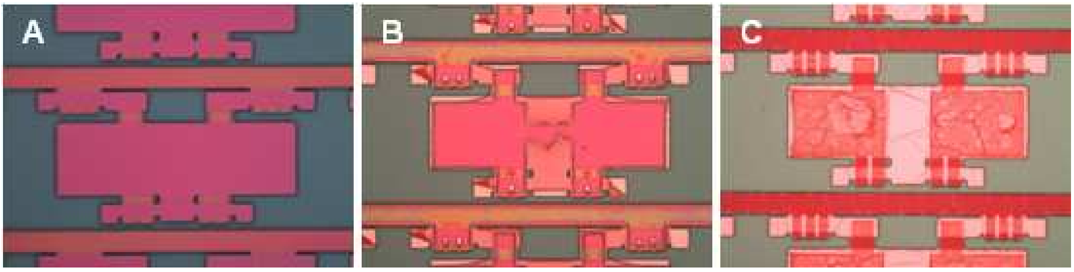


Figure 5.23: Optical microscope image of the patterned dual-tone photoresist samples: A. before development; B. during development; and C. after development.

Two process changes were made to mitigate the etch crust and its effect on the negative-tone image development. The flood exposure of the previously unexposed dual-tone photoresist was moved to precede the positive-tone etch step instead of following the said etch step, ensuring that the crust formed during etch did not interfere with the flood exposure of the photoresist. A short O_2 plasma ash was also added right after the positive-tone etch step to remove the crust prior to the negative-tone image development. The combination of the two changes was able to overcome the insoluble photoresist crust and enabled etching of the negative-tone images into the substrate (Figure 5.24).

In summary, the positive-tone photoresist patterns were transfer etched into the silicon oxide substrate using a RIE process with 15 sccm CF_4 and 5 sccm He gas mixture, 150 W etch power, 50 mTorr etch pressure, and a 4 min etch time. The RIE was done on a Trion RIE etcher. After the CF_4/He etch, a short O_2 plasma ash was applied in the same etcher to remove any of the residual photoresist and etch crust. The O_2 ash process used 20 sccm O_2 gas flow, 150 W etch power, 50 mTorr etch pressure, and 30 sec etch time. The photoresist was then developed again in the TMAH developer solution to remove the previously unexposed region, leaving behind only the negative-tone patterns. Once developed, a brief O_2 plasma descum is applied to remove any residual photoresist from the aqueous development. The O_2 descum process used 10 sccm O_2 and 10 sccm He gas mixture, 100 W etch power, 50 mTorr etch pressure, and 20 sec etch time. The negative-tone patterns were transferred into the substrate using the same CF_4/He RIE process as before (15 sccm CF_4 and 5 sccm He gas mixture, 150 W etch power, 50 mTorr etch pressure, and 4 min etch time). Once completed, any remaining photoresist was removed using an acetone and isopropanol solvent rinse.

5.4.4 Print Tests

Figure 5.24 shows optical microscope images and the corresponding profilometer traces of a patterned photoresist sample on a silicon wafer at several process stages. A top-down optical microscope image in row 2 shows a sample device area, with the dark blue line denoting the profilometer scan area across the positive-tone photoresist. The profilometer trace shows a 900 nm tall photoresist structure after the positive-tone development.

The sample was then etched by RIE to transfer the positive-tone image into the substrate, and developed again to remove previously unexposed photoresist, leaving behind the negative-tone device image. Row 3 shows a top-down image of the dual-tone photoresist sample with the positive-tone image etched into the substrate and negative-tone photoresist image left. The profilometer trace shows approximately 550 nm of photoresist remaining after the positive-tone structures are etched into the silicon substrate.

Finally, the sample was etched again by RIE to transfer the negative-tone image into the substrate, then stripped of the photoresist, leaving behind the two aligned layers of device structures in the substrate. Row 4 shows a top-down image of the dual-tone photoresist sample with both positive-tone and negative-tone images etched into the substrate. The profilometer trace shows ~100 nm tall positive-tone structures and ~200 nm tall negative-tone structures.

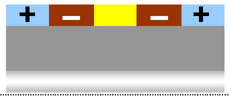
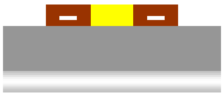
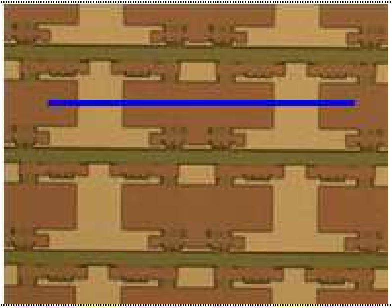
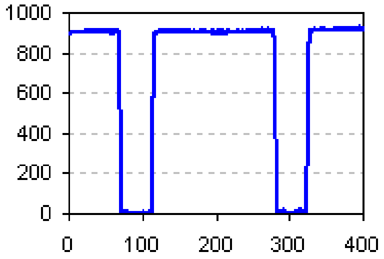
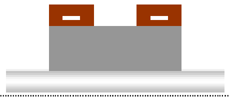
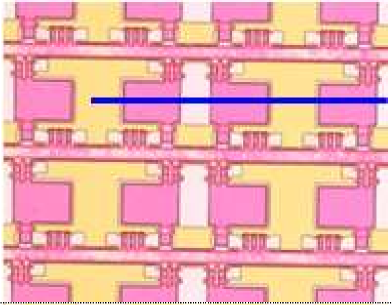
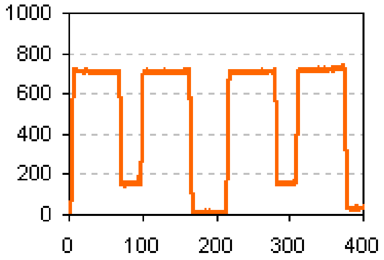
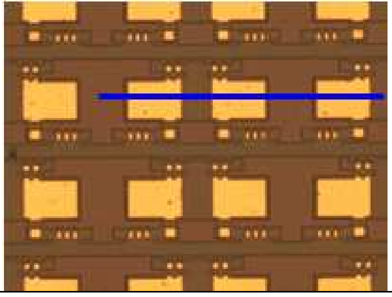
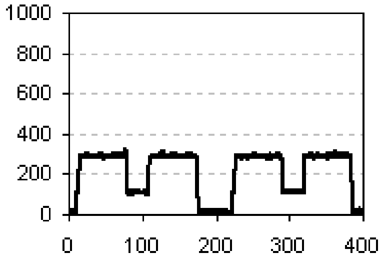
Substrate with dual-tone images.  	Top-down optical microscope images (blue line denotes the region traced by the profilometer)	Profilometer traces
Develop of positive-tone latent image.  		
Etch transfer of positive-tone image and develop of negative-tone latent image.  		
Etch transfer of negative-tone image and photoresist strip. 		

Figure 5.24: Optical microscope and profilometer trace of a patterned dual-tone photoresist sample.

5.5 CONCLUSIONS

A dual-tone, thermally activated photoresist with tolerance to the reactive ion etch process has been developed. Its functional formulation consists of a commercial positive-tone novolak / DNQ photoresist to which is added TPS nonaflate PAG and benzenedimethanol cross-linker. The dual-tone photoresist has been successfully applied in a self-aligned patterning process flow, demonstrating the simultaneous imaging of 2 device layers and the subsequent transfer of those images into the substrate. The successful integration of the dual-tone photoresist addresses the overlay and alignment challenges in the photolithographic patterning of flexible substrate materials.

5.6 REFERENCES

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Chapter 6: Conclusions and Recommendations

6.1 SACRIFICIAL IMPRINT MATERIAL

The direct, physical imprint process of Step and Flash Imprint Lithography (S-FIL) enables patterning of three dimensional structures. A multi-level S-FIL process using an imprint template built with both the via and metal interconnect patterns was developed to evaluate the application of S-FIL in the copper dual damascene interconnect fabrication. Using a sacrificial imprint material (SIM), one S-FIL step produced the same dual damascene structures that would otherwise require two photolithography steps, while retaining the use of the existing dielectric material and technology. Functional electrical test device samples were made using SIM in an S-FIL process and etched using an in-situ, multi-step etch process.

Successful integration of S-FIL in the copper dual damascene process was demonstrated by the fabrication of functional electrical test samples with good yields. The combination of the three-dimensional patterning capability of S-FIL and an in-situ, multi-step etch scheme greatly reduced the number of patterning steps necessary to build the via and metal interconnect structures in the copper dual damascene process. Additional improvement in the resolution capability and throughput of the multi-level S-FIL process will be required before implementation in a high-volume, commercial dual damascene fabrication process.

6.2 IMPRINTABLE DIELECTRIC MATERIAL

The development of an imprintable dielectric material (IDM) combines the multi-level patterning of the via and metal interconnect structures with the deposition of the permanent dielectric material, thereby further reducing the number of deposition, lithography, and etch steps required to construct interconnects. Several classes of materials had been studied for application as an IDM. Vinyl silane functionalized POSS material was developed to improve the synthetic consistency of the POSS compound and avoid the platinum catalyzed coupling reaction of the POSS acrylate formulation. Photopolymerization of the vinyl silane functionalized POSS material was enabled by the addition of azide and thiol cross-linkers, creating the POSS azide and POSS thiol formulations respectively. The POSS azide formulation was found to generate significant amounts of nitrogen gas during the photopolymerization process, resulting in poor pattern replication quality. The POSS thiol formulation utilized the thiol-ene chemistry to enable the photopolymerization of the vinyl silane functionalized POSS, avoiding the nitrogen outgas limitation of the POSS azide formulation. The imprinted POSS thiol samples have shown good pattern replication quality.

Improvements in the mechanical properties and storage stability of the POSS thiol material are required for the formulation of a functional IDM. Several approaches are being explored to address these issues, including reformulation of the POSS thiol with new multi-thiol cross-linkers and reactive diluent plasticizers, changing of pump parts to avoid exposure of POSS thiol to stainless steel surfaces, and study of other potential inhibitor additives. To demonstrate the feasibility of the IDM strategy, improvements in the viscous dispense and S-FIL process parameters are needed to produce functional IDM imprinted samples with good residual layer uniformity. The mechanical, thermal, and electrical properties of the imprinted, cured, and metallized IDM interconnect structure need to be tested to evaluate its applicability in a commercial dual damascene process.

6.3 DUAL-TONE, THERMALLY ACTIVATED PHOTORESIST

A dual-tone, thermally activated photoresist with tolerance to the reactive ion etch process was developed to overcome the alignment and overlay limitations of the traditional photolithography on flexible substrates. The functional dual-tone, thermally activated photoresist consisted of a commercial positive-tone novolak / DNQ photoresist, a TPS nonaflate PAG, and a benzenedimethanol cross-linker. The use of a dual-tone photoresist enabled the simultaneous patterning of two device layers in one layer of photoresist, distinguished by the incident exposure light wavelength. The thermal activation requirement provides compatibility with the reactive ion etch process.

The dual-tone photoresist was successfully applied in a self-aligned patterning process flow. A dual-tone lithography process imaged two separate device designs in one photoresist film on a flexible substrate. Subsequent reactive ion etch processes sequentially transferred the two designs into the flexible substrate, forming the desired device structures. The successful development of the dual-tone photoresist and the associated lithography and etch processes enabled aligned, photolithographic patterning of flexible substrate materials.

Further development of a photoacid generator without the dissolution inhibition effect will reduce the exposure dose requirement and improve the throughput of the exposure process. Improvements in the exposure, develop, and etch processes will be required to improve the dual-tone photoresist process latitude before commercial implementation of dual-tone photolithography on flexible substrates.

Appendix A: S-FIL Template Fabrication at UT-MRC

The low cost and high resolution patterning capabilities of Step and Flash Imprint Lithography (S-FIL) have attracted much interest for application in nanotechnology research and development. The University of Texas Microelectronics Research Center (UT-MRC), in conjunction with Molecular Imprints, Inc. and The National Nanotechnology Infrastructure Network (NNIN), installed an Imprio 100 S-FIL tool in 2005 to provide nanolithography capability for both academic research projects in the university and technology development for industrial partners.

In 2005 and 2006, a project was undertaken to develop a template fabrication process at UT-MRC in collaboration with SEMATECH Advance Material Research Center (AMRC) division, SEMATECH Lithography division, NNIN, and our research group. The advantages of the UT-MRC template fabrication process over commercial sources are the reduced cycle time and cost. The existing deposition, etch, electron beam lithography, and analytical equipments at UT-MRC's cleanroom facility enable design and fabrication of an imprint template at UT-MRC in substantially shorter time and lower cost, compared to the 2 to 6 month delivery time and $30000 to $70000 cost of commercial S-FIL template suppliers.

The trade off for the lower cycle time and cost at the UT-MRC is higher template defectivity and lower pattern quality. The fabrication protocols at UT-MRC involve more manual handling of templates and less optimized lithography and etch processes, therefore are liable to greater particle contamination and patterning errors than that of a commercial supplier. In addition, the electron beam lithography tool at UT-MRC is a Gaussian beam vector scan design, resulting in very slow write speed and precluding practical generation of large areas of patterns. Nevertheless, for the majority of research that only requires parts for proof of concept demonstrations, the ability to rapidly fabricate parts for concept evaluation far outweighs the lower process yield. The following sections detail the established process flow for S-FIL template fabrication at UT-MRC.

A.1 EQUIPMENT LIST

Figure A.1 lists the key equipment and their usage in the imprint template fabrication process. Training and certification by UT-MRC staff are required before operating any of the equipment; see the NNIN staff or the Facility Manager for more details.

JEOL e-Beam aligner	Pattern writer for features down to 20nm on template or wafers
CHA	e-beam evaporator for metal deposition
Trion Oracle RIE	Reactive ion etcher for descum, chrome etch, and quartz etch
HMDS Oven	HMDS treatment to improve resist adhesion on template or wafer substrates
8 Inch Spinner/Hotplate	e-beam resist coating and develop
Acid Hood	Safe location for Work with acid and base
Solvent Hood	Safe location for Work with organic solvents
Imprio 100	Nanoimprint tool
Alphastep - Tencor	Profilometer for mesa height and quartz etch depth check
Ellipsometer	Photoresist and thin film thickness metrology
Laser Microscope	General template inspection and chrome etch end-point inspection

Figure A.1: Equipment list for imprint template creation.

A.2 TEMPLATE BLANK PREPARATION

The template fabrication equipment at UT-MRC are set up to process one standard S-FIL imprint template at a time (Figure A.2). The template blanks can be either purchased directly from Molecular Imprints or prepared from conventional 6025 photomask plates. The following section outlines the procedure to produce S-FIL imprint template blanks from 6025 photomask plates. This procedure assumes that the blank 6025 photomask plate has no existing photoresist or chromium. For blank photomask plates with existing films of photoresist and chromium (common of commercial 6025 photomask plates) and known processing conditions, skip or modify the appropriate process steps accordingly.

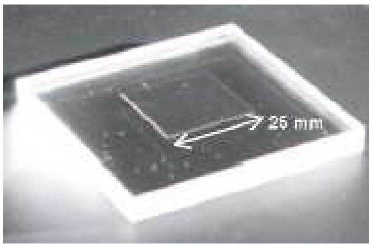

Figure A.2: A blank S-FIL template.

A.2.1 Chromium Deposition

The 6025 photomask plate is cleaned using a piranha or SC-1 clean in the Acid Hood immediately prior to the chromium deposition to ensure a contamination free surface. A film of chromium is deposited using CHA, an evaporative metal deposition tool, to provide a hard mask for quartz etch. A magnetic holder for the 6025 plate is available that allows the sample to be held in the CHA without use of tape. For the chromium deposition, aim for chromium film thickness of 500~600 Å and a deposition rate of 5 Å/sec or less to ensure complete coverage of the quartz surface. A slower deposition rate produces a smoother film with fewer voids and pin-holes, which better protects the quartz surface during the quartz etch.

A.2.2 Photoresist Coat and Softbake

Using the solvent hood spinner in the south cleanroom, attach the 6 inch photomask chuck and line the spinner with wipes to catch any photoresist run off. Set the spinner timer to the maximum value on the control panel, and set the hotplate to 120 °C. Prepare AZ 5209E photoresist (found in the refrigerator next to the solvent hood or in the north cleanroom refrigerator) or any positive-tone novolak-DNQ photoresist, and isopropyl alcohol (IPA) for spin coating.

Spin the photomask at 500 rpm with the chromium side up and pour in IPA until the blank photomask plate is fully covered by IPA. Change the spin speed to 150 rpm and hand pour the photoresist in the center of the photomask to cover about a three inch circle. The photoresist should visibly push a front of IPA outward as it spreads out. Turn the spin speed up to 900 rpm and spin for 90 sec. After a 900 rpm 90 sec spin, slow the spin speed gradually to decelerate the heavy quartz plate. Verify for complete photoresist coverage of the photomask plate. If necessary, the plate can be reworked by spinning it at 500 rpm and remove the photoresist with acetone spray. Remove the coated photomask plate from the chuck and bake directly on the hotplate for 5 minutes. Cool the mask on an unused hotplate for 5 minutes. Clean up the spin coater of any residual photoresist.

A.2.3 Mesa Lithography

Two masks are available for mesa lithography, a 10 and a 25 mm^2 mesa mask. Place the mesa mask on top of the photoresist coated photomask plate, with the patterned chromium side in contact with the photoresist side. Flood expose the photomask plate using Novacure for 6 min at 10000 mW power setting. Carefully remove the mesa mask by lifting it straight up and away from the photoresist surface; avoid lateral sliding of the plates to minimize scraping of the exposed photoresist film.

Develop the exposed photoresist with the appropriate developer, using either the puddle or dip develop technique. Wait until the areas outside the mesa visually clear of photoresist, about 1 min. Once the open areas clear, quench with DI water to wash away the developer. Spin or air dry the photomask plate, then hardbake the plate for 5 min at 120 °C.

A.2.4 Chromium Wet Etch

The chromium wet etch is done in the north cleanroom in the acid/metal hood. Using a large glass container (a 1 ft^2 casserole dish), pour in enough chromium etch solution to cover the 6025 photomask plate, and then place the plate into the etch solution. Use a Teflon or glass wand to gently agitate the solution. Once all of the chromium has been dissolved from the exposed areas, remove the photomask plate and quench in DI water rinse. Follow proper disposal procedure for the chromium etch solution.

A.2.5 Quartz Wet Etch

The quartz wet etch is done in the north cleanroom in the acid hood. Using a large Teflon container, pour in enough Buffered Oxide Etch 6:1 mixture (found in the acid cabinet) to cover the 6025 photomask plate. The target 15 µm etch depth requires approximately three hours of etch time. After the completion of etch time, remove the photomask plate and rinse thoroughly with DI water. Follow proper disposal procedure for the Buffered Oxide Etch solution.

A.2.6 Protective Resist Coat and Softbake

Thoroughly clean the etched photomask plate with acetone to remove any residual photoresist. Coat and softbake a layer of photoresist onto the mesa side of the photomask plate using the procedure described in section A.2.2 to protect the mesa surface during the shipping and dicing process.

A.2.7 Template Dice

See NNIN staff or Molecular Imprints for suggestion on a qualified vendor to perform the template dicing.

A.2.8 Resist Strip, Chromium Etch, and Wet Clean

Once diced, the individual templates are stripped of photoresist by soaking in an acetone bath overnight. Then the chromium film is removed using the procedure described in section A.2.5. Finally the template is cleaned using a piranha clean in the Acid Hood, producing a clean blank template with a predefined mesa.

A.3 TEMPLATE PATTERNING

The S-FIL template fabrication process at UT-MRC uses electron beam lithography for pattern generation and reactive ion etch for pattern transfer into the quartz substrate. A thin film of chromium is first deposited before application of the electron beam resist, to serve as both the charge dissipation medium during electron beam lithography and a hard mask for quartz etch.

A.3.1 Template Chromium Deposition

See section A.2.1 for the chromium deposition procedure. The target thickness for the chromium film is 150 Å, using a deposition rate of 3 Å/sec or less to produce a uniform and smooth chromium film on the quartz surface. The exact thickness of the chromium film is dependent on the chromium RIE etch selectivity and the e-beam resist film thickness, which is in turn dependent on the e-beam pattern feature size. Smaller e-beam features require thinner e-beam resist film, which in turn limits the chromium film thickness for the given chromium etch selectivity.

A.3.2 E-beam Resist Coat and Softbake

A uniform e-beam resist thickness over the template mesa is crucial in the e-beam pattern size uniformity across the mesa. A specially made template chuck is available for use on the 8 Inch Spinner/Hot Plate to provide good template hold during spin coating. Once the chromium coated template is loaded onto the spin chuck, the following coat steps are used to coat the e-beam resist, ZEP520-A.

Spray IPA onto the template while spinning the template at 200 rpm speed, 200 rpm/sec acceleration, and 3 sec time to fully cover the template with IPA. Spin the template at 700 rpm speed, 500 rpm/sec acceleration, and 4 sec time to remove excess IPA. Dispense ZEP520-A using a plastic syringe in the center of mesa to the size of a quarter, while spinning the template at 30 rpm speed, 1000 rpm/sec acceleration, and 15 sec time. Slowly dispense the resist to avoid bubbles and close the spin coater lid once the resist has been applied. Spin the template at 1500 rpm speed, 3000 rpm/sec acceleration, and 3 sec time to remove excess resist. Ramp up the spin speed to 4000 rpm, 3000 rpm/sec acceleration, and 60 sec time to equilibrate the resist film thickness. Decelerate the template at 1500 rpm/sec to stop the spinning. Finally, softbake the template in oven at 180 °C for 10 min then set on a room temperature surface to cool.

A.3.3 E-beam Lithography

The UT-MRC template fabrication process uses the JEOL JBX-6000FS/E e-beam writer to pattern the templates. There is a specially designed chuck for the JEOL e-beam writer that allows loading of the diced template. The e-beam exposure can take many hours to complete depending on the feature size and total pattern area. It is recommended to test run a small job first to verify the e-beam recipe and pattern quality before processing the full sample. See MRC staff for the e-beam lithography operation procedure and training.

A.3.4 E-beam Resist Develop

Once written, the template with ZEP520-A e-beam resist is loaded into the 8 Inch Spinner/Hot Plate. Pour on enough ZED-N50 developer to cover the template, while spinning the template at 100 rpm speed, 100 rpm/sec acceleration, and 3 sec time to fully cover the template with ZED-N50 developer. Close the spin coater lid and hold for 85 sec to let the pattern develop. Spin the template at 800 rpm speed, 400 rpm/sec acceleration, and 5 sec time to remove the bulk of developer and stop the development. Spray IPA onto the template while spinning the template at 100 rpm speed, 100 rpm/sec acceleration, and 15 sec time to fully rinse the template with IPA. Spin the template at 800 rpm speed, 400 rpm/sec acceleration, and 20 sec time to remove IPA and dry. Decelerate the template at 400 rpm/sec to stop the spinning.

Inspect the developed template using an optical microscope to verify the finely resolved patterns, before performing the subsequent etch process. If the patterns are found unacceptable, the e-beam resist can be removed using acetone rinse and piranha clean without damage to the chromium film, and the patterning conditions can be adjusted.

A.3.5 E-beam Resist Descum

The e-beam resist descum is done using the Trion Oracle RIE tool to remove any resist residue left on the exposed template surface. The RIE conditions are 10 sccm O_2 gas, 70 sccm He gas, 20 mTorr pressure, 35 W RF power, and 90 sec etch time.

A.3.6 Chromium Dry Etch

The chromium dry etch is done using the Trion Oracle RIE tool to remove chromium film in the exposed area of the template. The RIE conditions are 10 sccm O_2 gas, 40 sccm Cl_2 gas, 30 mTorr pressure, 80 W RF power, and 140+ sec etch time. The chromium RIE is performed as a timed etch. The etch rate is dependent on the feature size and density. Large features clear quickly (140 sec) while smaller features need a longer etch time (680 sec for sub 50 nm features). Incremental etching and inspection is used to verify etch completion in the high resolution features. Inspections are done on the Laser Microscope by visual observation of the shiny residual chromium film.

A.3.7 Quartz Dry Etch

The quartz dry etch is done using the Trion Oracle RIE tool to remove quartz film in the exposed area of the template. The RIE conditions are 15 sccm CF_4 gas, 40 sccm He gas, 15 mTorr pressure, 130 W RF power, and 300+ sec etch time. Similar to the chromium etch, the quartz RIE is performed as a timed etch with etch rate dependent on the feature size and density. Incremental etching and inspection are used to verify etch completion in the high resolution features.

A.3.8 Resist Strip, Chromium Etch, and Wet Clean

Once etched, the template is stripped of e-beam resist by acetone rinse and/or piranha clean. The chromium film is removed using the wet etch procedure described in section A.2.5. Finally the template is again cleaned with piranha clean, producing a clean patterned template ready for surface treatment.

A.4 TEMPLATE PATTERN CHECK

The template pattern can be verified either by SEM imaging or an imprint test. Figure A.3 shows SEM images of S-FIL template generated at UT-MRC, demonstrating good pattern resolution of 70 nm structures on the template.

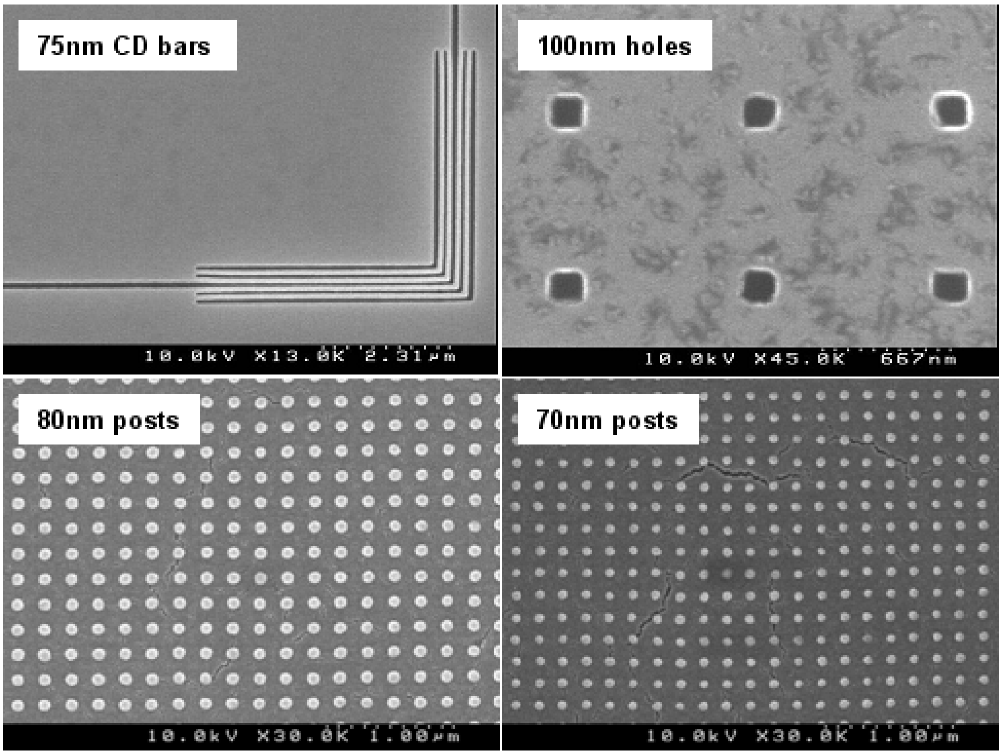

Figure A.3: SEM images of S-FIL template generated with the UT-MRC process.

Appendix B: Publications

Jen, Wei-Lun, Frank Palmieri, Brook Chao, Michael Lin, Jianjun Hao, Jordan Owens, Ken Sotoodeh, Robin Cheung, and C. Grant Willson. "Multilevel step and flash imprint lithography for direct patterning of dielectrics." Proceedings of the SPIE 6517.2 (2007): 65170K.1-65170K.9.

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Hao, Jianjun, Michael W. Lin, Frank Palmieri, Yukio Nishimura, Huang-Lin Chao, Michael D. Stewart, Austin Collins, Kane Jen, and C. Grant Willson. "Photocurable Silicon-based Materials for Imprinting Lithography." Proceedings of the SPIE 6517.2 (2007): 651729.1-651729.9.

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"Timeline of Intel Microprocessors." Intel Corporation. 10 June 2009 <http://www.intel.com/technology/timeline.pdf>.

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