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A dual gate transistor was fabricated using a self-assembled monolayer as the semiconductor. We show the possibility of processing a dielectric on top of the self-assembled monolayer without deteriorating the device performance. The two gates of the transistor accumulate charges in the monomolecular transport layer and artifacts caused by the semiconductor thickness are negated. We investigate the electrical transport in a dual gate self-assembled monolayer field-effect transistor and present a detailed analysis of the importance of the contact geometry in monolayer field-effect transistors. © *2010 American Institute of Physics*. [doi:10.1063/1.3379026]

Organic flexible integrated circuits are in development for applications such as displays,[1] sensors,[2] and contactless radio-frequency identification transponders.[3] For unipolar organic circuits, the performance is severely limited by the parameter spread inherent to organic semiconductors. The important parameter is the threshold voltage (V_{th}) of the individual transistors, which is crucial to ensure low power operation and an acceptable noise margin for the logic gates.[4,5] As a remedy, dual gate transistors are used to increase the noise margin of logic gates by changing the threshold voltage of organic transistors.[6] These dual gate transistors can also be used to improve the current drive and subthreshold slope.[7] Other potential applications include various types of sensors[2] and the integration of a logic gate into a single transistor.[8]

Organic dual gate transistors generally have semiconductor layers thicknesses in the order of tens of nanometers. Charge transport in organic transistors takes place in the first few nanometers from the dielectric interface in the semiconductor.[9] Conventional dual gate transistors have two conducting channels, one for the top and one for the bottom gate. When the semiconductor is thicker than approximately 10 nm, the individual transport channels are spatially separated. Only when the semiconductor is a single layer, the two transport channels will have a spatial overlap and the charges are confined to a single monolayer.

To study the interplay between the top and bottom channel of a dual gate transistor, an ultrathin semiconductor is required. Up to now the fabrication of such a transistor was hampered by the morphology of the first monolayers. Effective charge transport was hindered by the lack of in-plane order of the ultrathin semiconductor on the dielectric interface that prevented detailed study of the transport through the first interface layer. In a self-assembled monolayer transistor (SAMFET) the semiconductor consists of only a single sheet of molecules.[10] The layer thickness is comparable to that of the accumulation layer, i.e., ~3 nm. The electrical transport is then by definition two-dimensional. By using a monolayer semiconductor in a dual gate transistor, it is possible to simultaneously accumulate charges from the top and bottom gate in one monomolecular charge transport layer. A prerequisite is then that a dielectric can be processed on top of a SAMFET without deteriorating the charge transport through the monolayer. The additional advantage of monolayer dual gate transistors is that the capacitance of the depleted semiconductor can be neglected for calculating the effective threshold voltage shift.[11] Here we investigate the electrical transport in a dual gate SAMFET and present a detailed analysis of the importance of the contact geometry.

Dual gate transistors were fabricated on heavily *n*-type doped Si wafers as the bottom gate electrode. The bottom gate dielectric was a 1.2 μm thermally oxidized SiO_2 layer. The Au source and drain electrodes were defined by photolithography on a 5 nm Ti adhesion layer. The length and width of the resulting finger transistors were 10 μm and 10 mm, respectively. A 1% HF dip was used to activate the SiO_2 surface prior to applying the SAM molecule. The semiconducting monolayer of chloro[11-(5‴-ethyl-2,2:5′,2″:5″,2‴:5‴,2⁗-quinquethien-5-yl)undecyl] dimethylsilane was self-assembled from a toluene solution. On the SAM-layer, the top gate insulator AF-1600 (amorphous Teflon derivative, Sigma-Aldrich), was spincoated from the fluorinated solvent FC-40 (3M). The resulting layer had a thickness of approximately 350 nm. The top gate Au electrode was evaporated through a shadow mask and had a thickness of roughly 140 nm. After each step the bottom gate transistors were measured to look for signs of degradation but none were found. Hence we conclude that it is indeed possible to process additional functional layers on top of a self-assembled monolayer without affecting the transistor performance. A schematic of the dual gate transistor layout is presented in Fig. 1 together with a scanning electron microscopy (SEM) image of the actual device. From the bottom to the top, the n^{++} doped Si, SiO_2, Au source and drain contacts, Teflon, Au top gate and a layer of sputtered Pt can be identified. The Teflon contains holes, which is an artifact in the image due to damage caused by the focused ion beam (FIB) milling. Since the holes are also present above the gold elec-

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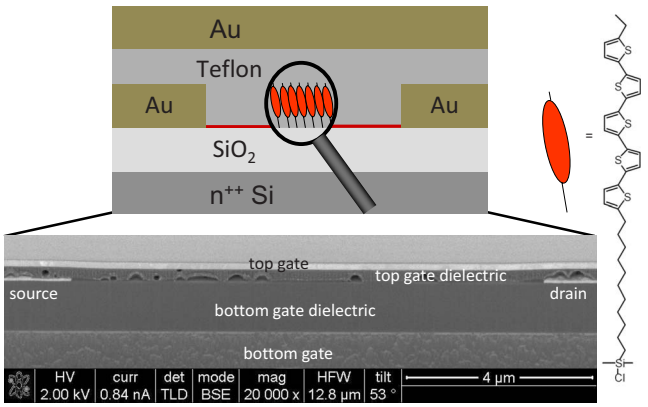

FIG. 1. (Color online) A schematic of the dual gate SAMFET is provided with a SEM image (20 000× magnification) of a FIB cross section of the actual device below. The holes in the Teflon layer in the SEM image are an artifact caused by the high energy ions used for milling in the FIB process. The chemical structure of the self-assembling molecule is shown on the right.

trodes and at the top of the Teflon layer, dewetting can be excluded as the origin of the irregularities.

The electrical transport was determined in vacuum ($\sim 5\times10^{-4}$ mbar) at room temperature using an HP-4155C semiconductor parameter analyzer. The resulting bottom and top gate transfer curves are presented in Figs. 2(a) and 2(b), respectively. For both gates the opposite gate was fixed at −6, −3, 0, 3, and 6 V bias, yielding a linear shift in the threshold voltage according to, as follows:

$$\Delta V_{\mathrm{th}} = \frac{C_2}{C_1} V_{g2}, \tag{1}$$

where C_1 and C_2 are the dielectric capacitances per unit area for the swept gate and the opposite gate, respectively, and

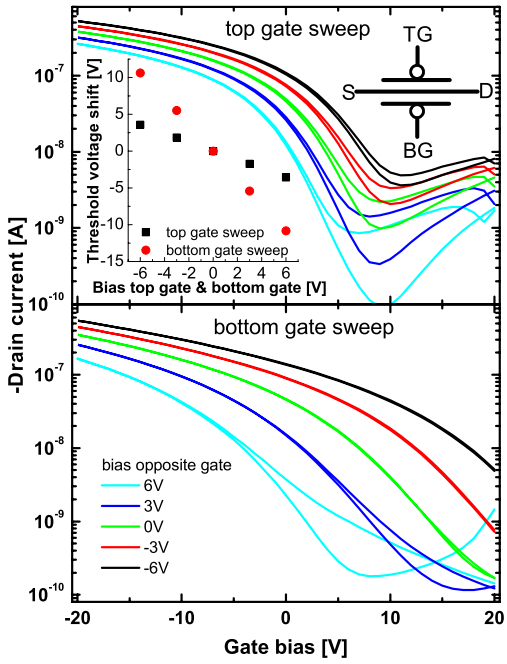

FIG. 2. (Color online) Transfer characteristics for the top (above) and bottom (below) gate are presented for a drain bias of −2 V. The channel length and width are 10 μm and 10 000 μm, respectively. For both gate sweeps, the opposite gate is varied in steps of 3 V from −6 to +6 V. The inset shows the resulting threshold voltage shift vs the applied bias on the opposite gate.

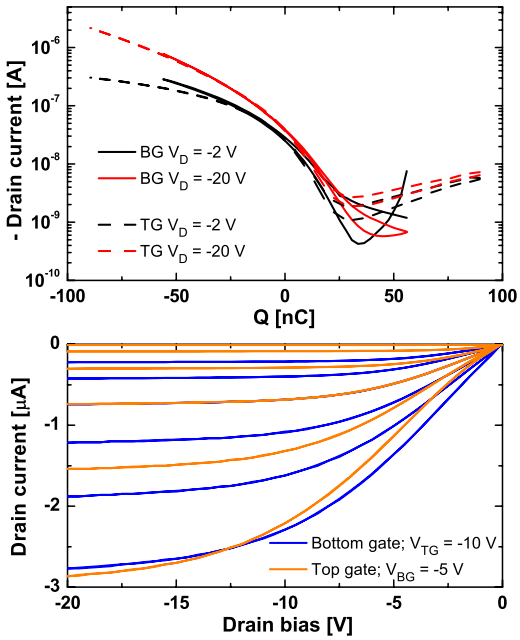

FIG. 3. (Color online) (a) The drain current of the transistor is plotted vs the accumulated charge (Q) for both the bottom (solid line) and top (dashed line) gate. For the linear regime, at −2 V (the two lower curves) drain bias, the top gate yields a lower current than the bottom gate for the same induced charge. In the saturated regime, at −20 V (upper curves), both gates show the same current for equivalent charge. (b) Output curves of the top and bottom gate. For both gates, the gate voltage was varied in 5V steps from 5V to −20 V. For the top gate drain sweeps, the bottom gate bias was at −5 V and for the bottom gate drain sweeps the top gate bias was −10 V. The out curves for both gates are presented for similar drain currents by tuning the opposing gate's bias, to ease comparing the two measurements.

V_{g2} is the applied bias to the opposite gate. The transfer curves of the bottom gate shift more than the top gate, because the top gate capacitance is larger than the capacitance of the bottom gate. From the threshold voltage shift as depicted in the inset of Fig. 2 and Eq. (1), we extract a value of 4.6 nF/cm^2 for C_t, given the known value of 2.8 nF/cm^2 for C_b. The latter value was calculated from the layer thickness and dielectric constant of SiO_2. The capacitance of the top gate is in agreement with the capacitance derived from the measured thickness of the Teflon layer. Figure 2 shows that the shape of the transfer curves does not change with the variation in the top gate. The main effect of the top gate bias is a shift in the threshold voltage. The transfer curves are parallel. In a SAMFET the semiconductor capacitance can be disregarded and, therefore, the transfer curves show an equidistant shift.[6,11]

The top gate yields a higher current and steeper subthreshold slope, both associated with the higher gate capacitance. However, the top gate also shows a higher contact resistance than the bottom gate. This is illustrated in Fig. 3(a) by plotting the IV-characteristics versus the total accumulated charge calculated by multiplying the capacitance of the gate dielectric with the applied gate bias. For the linear regime, at a drain bias of −2 V, the top gate shows a significantly lower current than the bottom gate for the same accumulated charge. In the saturated regime, where the drain bias is −20 V, the two gates show the same normalized transfer curves. The converging currents for the top and bottom gate for higher drain bias are indicative for a contact resistance. To confirm the presence of a contact resistance, the output curves for both gates were measured, as shown in Fig. 3(b).

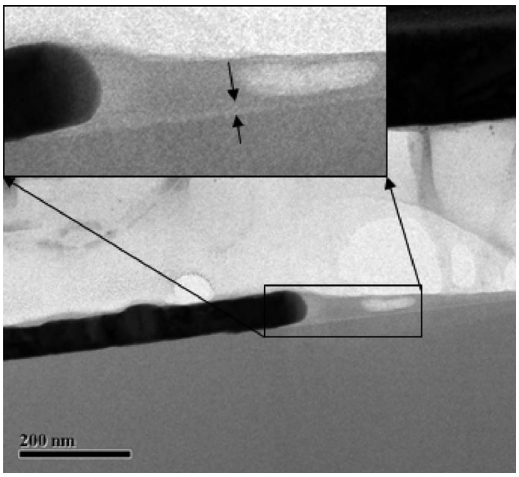

FIG. 4. A TEM image of a cross section of the dual gate SAMFET. The dark field image depicts the electrode as a black line protruding from the left side of the picture. The Teflon has varying shades of gray because of the damage it received from the focused ion beam used to drill the slice from the substrate. The two arrows in the inset indicate the SAM layer, which is visible as a faint gray line on the surface of the SiO_2 dielectric. The layer has a thickness of (3 ± 1)nm, which is in good agreement with the calculated length of the molecule. The injection region for the top gate is shielded by the overhanging part of the electrode, hampering charge accumulation.

The output curves for both gates are presented for similar drain currents by tuning the opposing gate's bias, to ease comparing the two measurements. The top gate drain sweep shows a clear s-shape in the output curve, indicating a larger contact resistance for the top gate transistor than for the bottom gate transistor.[12] We note that this is highly remarkable since the charges are injected in both cases from the same electrode into the same charge transport layer. Even more striking is that for previously reported organic field-effect transistors,[13,14] a top gate—bottom contact layout generally shows a *lower* contact resistance than a bottom gate—bottom contact design. This is because for transistors with the gate and electrodes on opposite sides of the semiconductor, the effective injection region is orders of magnitude larger than for devices with the gate and contact on the same side of the semiconductor, where the injection region is only the side of the contact next to the nanometer-scale transport channel.[15]

In the device reported here, we counterintuitively observe a higher contact resistance for the top gate. To elucidate the controversy, we imaged the contact using transmission electron microscopy (TEM) as depicted in Fig. 4 and its magnification in the inset. A cross section of the dual gate SAMFET is presented near a contact. It shows that the electrode is under-etched as reported previously.[16] The injection region for the top gate is then shielded by the overhanging part of the electrode, preventing field-enhanced injection. The depleted region of the semiconductor near the electrode causes an additional resistance for the charges accumulated by the top gate, as evidenced by the transport measurements.

Concluding, we demonstrate a dual gate transistor where the semiconductor is only as thick as the charge transport channel. Previous dual gate transistors contain two channels which are spatially separated and are tuned independently. In a dual gate SAMFET the accumulated charge carriers spatially overlap and form a single conduction channel. We show that the transistor behaves electrically as a single channel OFET where the effective charge accumulation is a superposition of the two gate biases modified by their capacitances. Distinct evidence of electrostatic interplay between the top and bottom channel of the dual gate transistor was not observed. Additionally, we demonstrated that for monolayer transistors, a bottom contact—top gate layout is disadvantageous because the contacts screen the gate field of the top gate.

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