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Recursive Receiver Down-converters with Multiband Feedback and Gain-reuse for Low-power Applications

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Recursive Receiver Down-converters with Multiband Feedback and Gain-reuse for Low-power Applications

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To My Beloved Family

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Power minimization in wireless transceivers has become increasingly critical in recent years with the emergence of standards for short-distance applications in the 900 MHz and 2.4 GHz industrial, scientific and medical (ISM) radio bands. The demand for long battery life and better portability in such applications has led to extensive research on low power radio architectures.

This dissertation introduces receiver topologies for low-power systems and presents a theoretical performance analysis of the topologies. Two fully integrated receiver down-converters that demonstrate the concept are implemented in a 0.13-μm CMOS technology. These topologies employ merged mixers and IF amplifiers in order to reduce power dissipation for a given dynamic range performance. In the described topologies, the input stage of a mixer is used to simultaneously provide conversion gain and baseband amplification. This is achieved by applying the down-converted IF signal to input

of the mixer. Consequently, the effective conversion gain of the design is greatly enhanced with current requirement primarily determined by the input transconductor. Potential degradation mechanisms related to instability and second-order distortion are identified and solved by the use of appropriate circuit techniques. Noise and linearity performance of the down-converters is analyzed and compared to that of conventional cascaded design counterparts. The potential for enhancement of IIP3 performance through cancellation of nonlinear products is discussed. Potential extensions of the above work including feedback-based architectures that exploit multiple loops for further maximizing the power efficiency of receiver front-ends are also presented.

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Chapter 1

Introduction

1.1 Motivation

In recent decades, several wireless communication systems have been standardized for a diverse set of applications. Recent advances in wireless systems include the development of standards for wireless sensor networks, wireless personal area networks, new standards for long-range cellular systems as well as systems for very high data-rate short-distance communications. These systems span a wide range of data-rates. The power-dissipation and dynamic range requirements also vary greatly depending on the targeted application. The highest data rate systems for applications such as wireless multichannel video and high-speed internet access support rates of the order of a Giga bits-per-second. Examples of such systems include Ultra Wideband (UWB) [1–3] and high-speed wireless LAN (e.g. IEEE 802.11n [4]). Another set of applications emphasize ultra-low power dissipation and are intended for low average data rates such as those required in for industrial and home automation and consumer electronics. These systems often require transceivers capable of operating for more than a year on a single battery. A summary of several wireless systems is provided in Table 1.1

Table 1.1: Main characteristics of wireless systems

Characteristics	GSM	UWB	IEEE 802.11n	IEEE 802.11g	IEEE 802.15.4	Bluetooth
Frequency allocation	880-960 MHz(Cell.) 1850-1990 MHz(PCS)	3.1-10.6 GHz	2.4 GHz/ 5 GHz	2.4 GHz (ISM)	868 MHz/ 910 MHz/ 2.4 MHz	2.4 GHz (ISM)
Channel bandwidth	0.2 MHz	>500 MHz	20 MHz	25 MHz	0.3 MHz/ 0.6 MHz/ 2 MHz	1 MHz
Number of RF channels	124	$1-15$	3/24	3	1/10/16	79
Maximum data rate	270 Kbit/s	>100 Mbit/s	540 Mbit/s	54 Mbit/s	24 Kbit/s 40 Kbit/s 250 Kbit/s	1 Mbit/s
Modulation type	GMSK	BPSK/ QPSK	BPSK/ QPSK	OFDM + CCK	BPSK/ OQPSK	GFSK
Required sensitivity	-102 dBm	-	-	-76 dBm	-85 dBm	-70 dBm
App. PHY power	>5 BT	~ 3 BT	~ 4 BT	~ 4 BT	$<$ BT	BT

$*$ Acronyms used: BT=reference Bluetooth device

Progressively stringent performance requirements as well as considerations related to cost and power dissipation have led to increasingly aggressive requirements for the radio frequency (RF) transceivers used in many of the applications. These goals are often driven by the needs for portability, high data rate, and compaction of the system. Recent research has focused on the development of monolithic transceiver architectures, particularly in low-cost complementary metal oxide semiconductor (CMOS) technologies. CMOS technology enables the integration of both analog and digital circuitry on the

same chip and helps to achieve a high level of integration, which leads to lower fabrication cost [5]. In fact fully integrated transceivers have been recently demonstrated for several applications including cellular (such as GSM and WCDMA) [6, 7], and short-range data and sensor networks (such as IEEE 802.15.4 and Bluetooth) [8–11]. The focus of this dissertation is the study and analysis of power-efficient designs and circuit techniques for radio receiver design. We describe front-end down-conversion receivers capable of achieving a very high gain per unit power dissipation and minimal area requirement. These designs also seek to maximize a key figure of merit, namely the dynamic-range performance per unit power dissipation. The designs and techniques are intended for systems such as IEEE 802.15.4 (Zigbee) and other short-distance applications involving the ISM band where the requirement for low power is critical. The dynamic range requirements are modest in these systems in comparison to those of transceivers for long-range applications such as cellular telephony, however as mentioned above battery life is of paramount importance.

1.2 Organization

This dissertation is organized as follows. Chapter 2 describes the functionality and design considerations of conventional receiver down-converters, along with a description of key receiver metrics related to noise, linearity and dynamic range performance. In chapter 3 we provide an overview of state-of-the-art power-efficient architectures and circuit techniques that have been

reported for the design of low-power receiver front ends. The proposed down-converters based on multiband signal feedback are presented in chapter 4 with considering architectural drawbacks. Chapter 5 details the practical implementations of proposed topology and analyzes their characteristics with respect to stability, noise and linearity performance. Chapter 6 summarizes the measurement results of the down-converters that are implemented for verifying the proposed topology using 0.13-μm CMOS technology. Chapter 7 concludes the dissertation with discussions on future work.

Chapter 2

Design of Receiver Down-converters

In this chapter, we will describe the general considerations for the design of conventional receiver down-converters and investigate in detail the key design metrics related to the noise performance, conversion gain, third-order nonlinearity and gain compression. Receiver down-converters are critical power-consuming blocks in a receiver chain. Based on functionality, the down-converters typically include several active or passive subcircuits. The specific design approach employed will depend on the requirements of the standard, which will also determine the power consumption.

2.1 General Considerations

A conventional heterodyne architecture is shown in Fig. 2.1 and is used to describe several key metrics and receiver requirements. The RF front-end band selection filter is typically utilized at the input of receiver and is used to attenuate undesired out-of-band signals. This is followed by a low-noise amplifier (LNA) that reduces the input-referred noise contribution from the circuits that follow. The image rejection (IR) filter following the LNA attenuates unwanted signals in the image band. Depending on the chosen intermediate

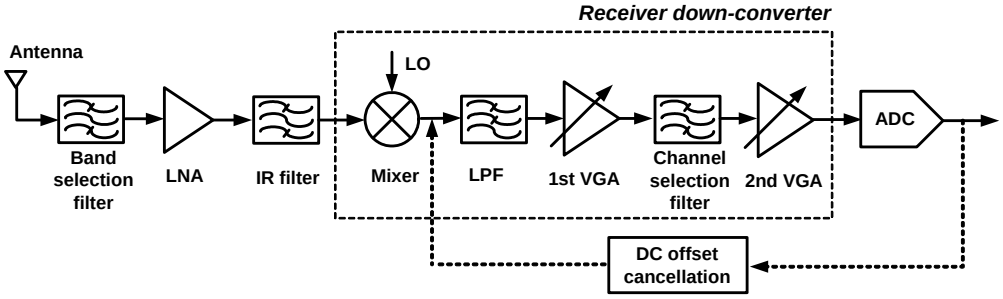


Figure 2.1: Conventional receiver chain

frequency (IF), a trade-off is usually inevitable between the channel selectivity and the image rejection ratio. As the image band appears at a difference of 2IF from the carrier frequency, the choice of a low IF requires an IR filter to possess a high quality factor (high-Q) effectively attenuating images with minimum loss of the desired signal. Nevertheless this alleviates the requirement of channel selection filters. A mixer driven by an local oscillator (LO) can perform the frequency down-conversion of the received signal to obtain the desired IF frequency band. The function of the channel selection is performed by high-Q discrete filters that are similar to the image rejection filters. Subsequently, baseband amplifier stages with variable gain capability are used to achieve a sufficiently large signal level before the data conversion process.

The inset box in Fig. 2.1 depicts the down-converter. The down-converter is typically implemented after low-noise amplification and image rejection. The major objectives of the receiver down-converter are: (1) translation of the received high-frequency signals to the IF band; (2) rejection of undesired out-of-channel interferers; and (3) additional amplification to

achieve a sufficient signal level for subsequent analog-to-digital conversion. Programmable gain control is usually embedded into the mixer or a series of baseband amplifiers in order to avoid saturating the baseband analog-to-digital converter (ADC). The typical analog downconverter thus consists of a mixer, circuits for LO generation, channel-selection filters and baseband variable-gain amplifiers (VGAs). Optionally, feedback DC offset cancellation circuits can be implemented to eliminate the DC offsets in the chain. This is especially important in direct down-conversion receivers, which use an IF at DC.

Two critical receiver metrics can be understood in the context of the above overview of heterodyne receivers. These include sensitivity and selectivity. Sensitivity is the smallest signal at the receiver input that is required to provide sufficient signal-to-noise ratio (SNR) for acceptable signal detection e.g. to achieve the specified bit error rate (BER) at the receiver output. It mainly depends on the gain, bandwidth and noise performance of the receiver. Selectivity is the receiver's ability to distinguish the desired signal around the carrier frequency from signals at other frequencies. It is primarily determined by baseband and IF filter performance, e. g. filter stop-band attenuation and roll-off characteristics. Additionally, it is also related to receiver non-linearity performance such as the third-order intermodulation (IM), image rejection ratio (IRR) and local oscillator (LO) phase noise. Sensitivity is a design capability to detect the smallest signal at a receiver input to attain sufficient signal-to-noise ratio (SNR) and the specified bit error rate (BER) at the receiver output for signal detection. It mainly depends on the achievable gain,

bandwidth and noise performance of systems.

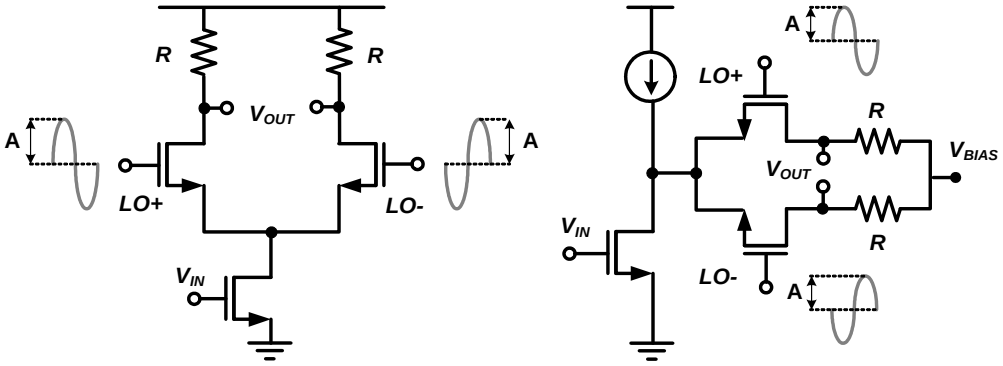
The above requirements are derived from system level specifications. For a given architecture, e. g. heterodyne or fully integrated direct conversion type receivers, these requirements set the limits on minimum power dissipation and the overall cost constraints. Design choices play a large role in deciding the efficiency of the implementation and thus the architecture needs to be carefully optimized for a given set of requirements. For example, issues such as the choice of IF, LO amplitude required for mixing, the partitioning of filters between passive and active stages are critical in minimizing power dissipation. Metrics relating to the above requirements are described below.

2.2 Design Issues

2.2.1 Noise Performance

The noise characteristic of down-converters is the one of the important factors that determines system performance. To maximize the SNR requirement, the noise contribution from various noise sources needs to be minimized. Noise contributors within the receiver degrade the SNR that is incident at its input, and the relative degradation is quantified by the Noise Figure, which is defined as the ratio of the SNR at the input of the receiver to the SNR at its output, that is

$$NF = \frac{SNR_{in}}{SNR_{out}} = \frac{N_o}{GN_i} = 1 + \frac{N_c}{GN_i} \tag{2.1}$$



(a) (b)

Figure 2.2: Typical single-balanced switching (a) active mixer and (b) passive mixer

where N_i, N_c and N_o are the noise power of the source resistance, noise power contributed by the circuit and total output noise power at the output, respectively. NF is expressed using the dB scale and is specified at a given value of source resistance.

For the cascaded system, the input-referred noise contributed by a given stage is reduced by the cascaded gain of all the stages that precede it. The first stage of the cascaded system is thus often critical in setting overall NF. This is the main reason that a LNA is typically required as the first stage in a receiver chain.

The first down-conversion mixer is also a critical block with respect to noise because it is also a significant contributor to the overall noise figure. Fig. 2.2a shows a typical active single-balanced switching mixer, comprising an input transconductance, switches and an output load. The white noise of

transconductor and switches and the flicker noise of switches are the dominant noise contributors at the output. Assuming ideal square-wave switching, the total white noise at the mixer output is given by [12, 13]

$$\overline{v_{on,wh}^2} = 8KT\gamma g_m R^2 \left(1 + \frac{2I_B}{\pi A_{LO} \cdot g_m}\right) \tag{2.2}$$

where γ is a channel noise factor, which is approximately 2$\sim$3 for short channel MOSFETs due to hot carrier effects [14], I_B is the bias current of the switch, and A_{LO} is the amplitude of the LO signals. The first term of Eq. (2.2) is the output noise due to frequency translation of the RF input transconductor, and the second term is due to two switches. The flicker noise originating in switches is expressed as [12, 13]

$$\overline{v_{on,1/f}^2} = \frac{I_B}{\pi A_{LO}} \cdot V_n\left(f\right) \tag{2.3}$$

where $V_n(f)$ is the referred gate voltage of one switch which is given by the time-average inversion layer charge in the channel. From Eqs. (2.2) and (2.3), it is apparent that to minimize the noise figure of the mixer, the transconductance (g_m) of the RF input device and the amplitude of the LO signals must be maximized with an increase in the power consumption, and the bias current of the switching devices must be reduced. In practice, the double-balanced configuration has been extensively used in several communication systems due to the high level rejection of LO and even-order harmonics at the output. However, the power consumption is doubled to achieve an equivalent conversion gain as compared to its single-balanced counterpart.

In the limit that the bias current is reduced to zero, a passive mixer core (Fig. 2.2b) is realized. Unlike the active configuration (Fig. 2.2a), the mixing operation is performed by voltage commutation instead of current commutation. Due to zero bias current through the switches, a low corner frequency for flicker noise is achieved [9, 15]. The conversion gain of this design is typically lower than the current-commutating mixer.

2.2.2 Conversion Gain

As depicted in Fig. 2.1, the overall conversion gain of a receiver down-converter is given by the multiplication of the gains of the mixer, channel-selection filter, and the 1^{st} and 2^{nd} VGAs, i. e.

$$G_T = G_M \cdot G_{BB1} \cdot G_{BPF} \cdot G_{BB2} \tag{2.4}$$

where G_T denotes the overall conversion gain of the down-converter and G_{BPF} is less than unity for a passive implementation. The down-converter is required to provide sufficient gain to compensate for the losses of the preceding BPF/duplexer and IR filter and to maximize the dynamic range of the entire system. The down-converter gain and dynamic range are critical to overall power dissipation as mentioned earlier.

Gain partitioning of the down-converter is very critical in the case where strong desired signals or strong adjacent interferers/blockers are applied to the input of the receiver. Generally the conversion gain of the mixer helps to reduce the noise contribution from the IF stages. However, a very large gain

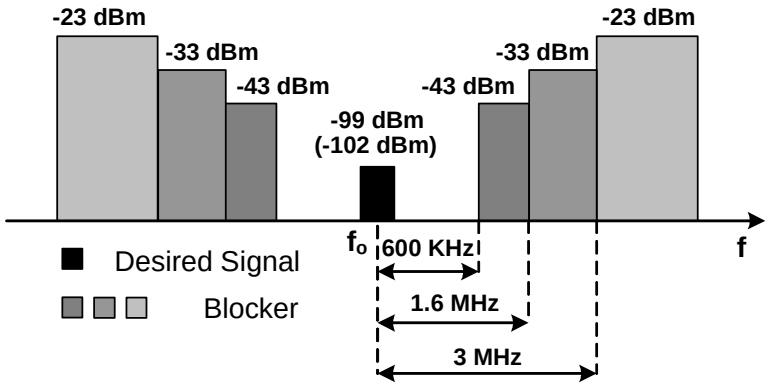


Figure 2.3: Template of blocking signal levels specified by the GSM standard

allocation in the mixer may saturate the output of the mixer in the presence of interferers.

Especially significant are strong interferers/blockers near the RF frequency that are not well attenuated by the band-selection filter, and in a heterodyne receiver are rejected in a series of channel-selection steps utilizing IF filters. The GSM standard, for example, specifies the template for blocking signal levels as depicted in Fig. 2.3 [16]. At 3 MHz away from the desired signal channel, a blocker level of -23 dBm is specified at the receiver front end, while the sensitivity of the desired signal is -99 dBm. In a 50 Ω system, this translates to an input voltage level of -33 dBV. Typically a band-selection filter or a duplexer provides some attenuation. However for a typical combined gain of approximately 30 dB for the LNA and mixer the blocker may drive the output of the mixer into compression, especially in low-voltage technologies. Some degree of filtering is essential at the output of the mixer, before the incident

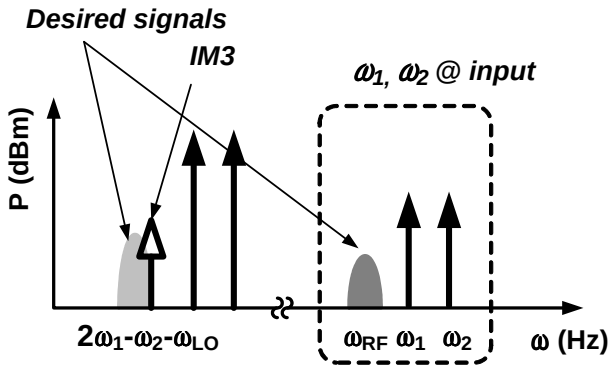


Figure 2.4: Corruption of a desired signal caused by third-order intermodulation (IM3) between adjacent interferers

signal is amplified in the next stage. Therefore, a typical receiver employs a multiple -step down-conversion stage with proper frequency planning and the use of IF filters or a series of gain stages with intermediate filters to relax the design specifications of the baseband in the presence of the interferers. The placement of gain and filtering functions is critical in determining the receiver power dissipation.

2.2.3 Third-order Nonlinearity

Third-order intermodulation (IM3) products have a detrimental effect in RF communication systems. These are caused by the inherent nonlinearity of active devices. Third-order intermodulation can generate unwanted beat products from out-of-band signals and cause them to appear within the signal band. Such a case is shown in Fig. 2.4, where one of the IM3 products given by third-order nonlinearity appears within the desired channel and corrupts the

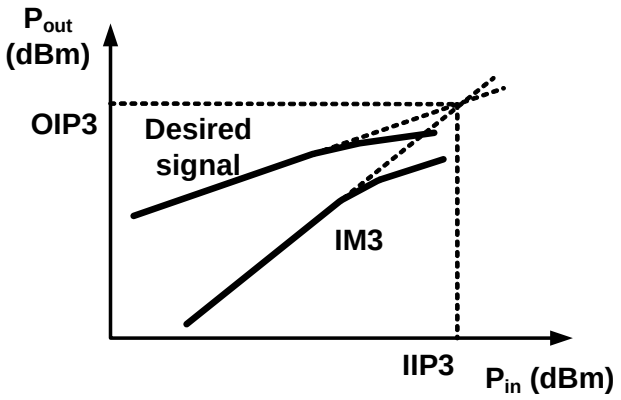


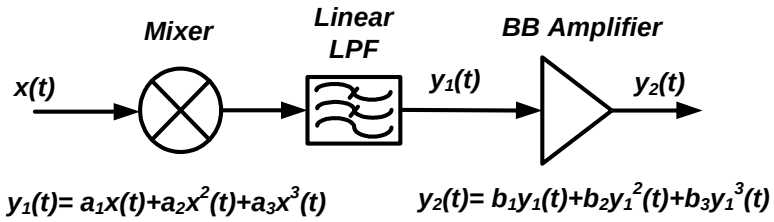
Figure 2.5: Definition of third-order intercept point (IP3)

desired signal. If we apply two tones at two adjacent channel frequencies, ω_1 and ω_2, the IM3 products of a down-converter are generated at the frequencies $(2\omega_1 - \omega_2 - \omega_{LO})$ and $(2\omega_2 - \omega_1 - \omega_{LO})$, where ω_{LO} is the frequency of the LO signal.

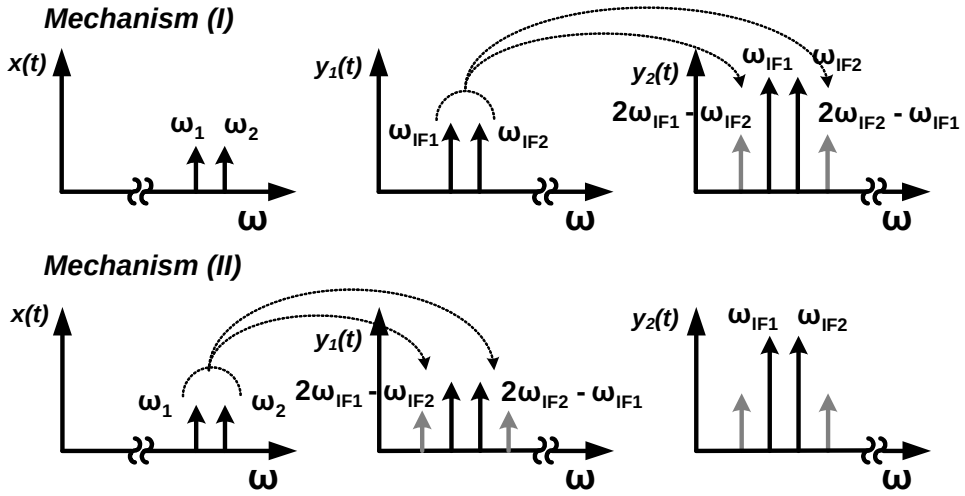
Third-order nonlinearity of receiver systems is commonly characterized by a third-order intercept point (IP3) (Fig. 2.5). For simplicity, assuming that our system is memoryless, each stage of the cascaded down-converter can be modeled by a polynomial nonlinearity of the form,

$$y(t) = p_1 x(t) + p_2 x^2(t) + p_3 x^3(t) + \cdots \tag{2.5}$$

where $p_{(n)}$ is the n-th order nonlinear coefficient. Fig. 2.6a shows the nonlinear characteristics of the two-stage down-converter in cascade, which consists of a mixer, an LPF and a baseband amplifier. Let us consider two-tone signals at the input with amplitude 'A', i.e. $x_{\omega_{1/2}}(t) = A \cdot (\cos \omega_1 t + \cos \omega_2 t)$ and assume



(a)



(b)

Figure 2.6: (a) Nonlinear block diagram and (b) third-order intermodulation

that the LPF is perfectly linear. In this case, two mechanisms are primary contributors to the IM3 at the output, as depicted in Fig. 2.6b. (i) The mixer amplifies the two tone signals and down-converts them to $(\omega_1 - \omega_{LO})$ and $(\omega_2 - \omega_{LO})$. The third-order distortion of the following amplifier generates IM3 products at $(2\omega_1 - \omega_2 - \omega_{LO})$ and $(2\omega_2 - \omega_1 - \omega_{LO})$. (ii) IM3 products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are generated by the third-order nonlinearity of the mixer for the applied two-tone signals at ω_1 and ω_2 and the IM3 products are further amplified in the following baseband amplification step. Thus the combined IM3 product at $y_2(t)$ is given by

$$IM3 = \frac{3}{4}\Big(a_1^3 b_3 + a_3 b_1\Big) \cdot A^3 \tag{2.6}$$

From Eq.(2.6), the overall third-order input intercept point (IIP3) is obtained as follows.

$$\frac{1}{IIP3_T^2} = \frac{\sqrt{3 \cdot (a_1^2 b_3/b_1 + a_3/a_1)}}{2} \cong \frac{1}{IIP3_{Mixer}^2} + \frac{a_1^2}{IIP3_{Amp}^2} \tag{2.7}$$

where $IIP3_T$ is the third-order input intercept point of the cascaded down-converter. Eq.(2.7) is readily extended to a general expression for the multi-stage down-converter (Fig. 2.1):

$$\frac{1}{IIP3_T^2} \cong \frac{1}{IIP3_{Mixer}^2} + \frac{G_{Mixer}^2}{IIP3_{BB1}^2} + \cdots + \frac{G_{Mixer}^2 G_{BPF}^2 G_{BB1}^2}{IIP3_{BB2}^2} \tag{2.8}$$

In the later discussion we will assume a current-steering type MOSFET based mixer. In such a design, the nonlinear sources that primarily determine the third-order distortion behavior include the transconductance (g_m)

nonlinearity in the driving MOSFET transistors of the mixer and baseband amplifiers and nonlinearity of the switching pair within the mixer. In the case of the transconductance, the drain current of a common-source FET can be expressed in terms of the small-signal gate-source voltage, which is given by the Taylor series expansion [17–19], i.e.,

$$i_d = g_1 \cdot v_{gs} + g_2 \cdot v_{gs}^2 + g_3 \cdot v_{gs}^3 + \cdots = g_m \cdot v_{gs} + g_m' \cdot v_{gs}^2 + g_m'' \cdot v_{gs}^3 + \cdots \quad (2.9)$$

where $g_m^{(n)}$ is the n-th order derivative of transconductance with respect to v_{gs}. Due to the critical impact of third-order nonlinear transconductance on IM3 of the mixer and baseband amplifiers, the overall IP3 is capable of being determined by the combination of the third-order coefficients of each stage, as derived in Eq. (2.6). To improve the linearity performance linearization techniques such as derivative superposition method to cancel the third-order term have been employed in the input stages [17, 18]. Switching pair nonlinearity is considerably more complex to analyze and it can be treated as a nonlinear time-varying circuit where the operating point of switches varies periodically. At a low frequency where the capacitive effects become negligible, the nonlinear behavior of the switching pair can be simply described by time-invariant power series because it is memoryless system [20]. However, at a high frequency, a time-varying Volterra series [21, 22] is required to analyze the intermodulation performance of the switching pair.

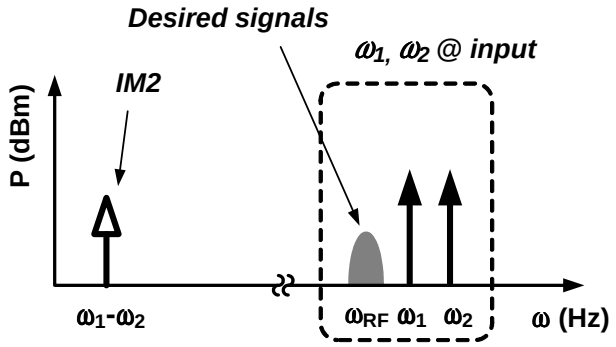


Figure 2.7: Second-order intermodulation between adjacent interferers

2.2.4 Second-order Nonlinearity

The beat products given by the second-order nonlinearity also introduce undesirable spectral components. In the receiver front-end, both a LNA and a mixer can cause the second-order intermodulation (IM2) distortions.

Second-order linearity performance can be similarly characterized by second-order intercept point (IP2), as shown in Fig. 2.8. Only difference in this case is that IM2 distortion increases two-times faster with the applied signal amplitude compared to the fundamental signal such that slope difference is two instead of three.

IM2 can lead to amplifier and mixer desensitization as discussed below. For instance, let us consider a nonlinear LNA exhibiting second-order nonlinearity. Suppose, as depicted in Fig. 2.9, a desired signal at ω_{RF} and a close-in strong interferer at ω_{INT} are applied to the input, the IM2 between low frequency noise such as $1/f$ noise, and an adjacent interferer creates spec-

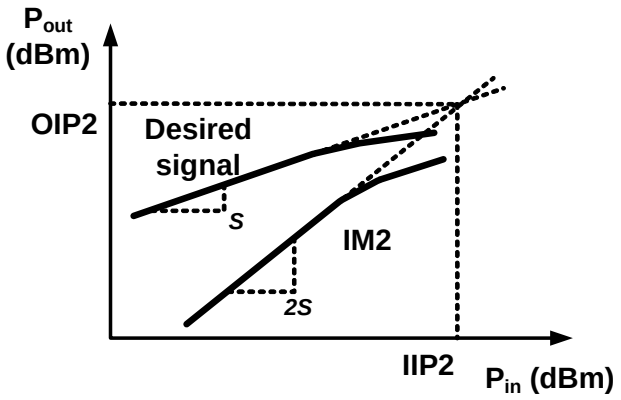


Figure 2.8: Definition of second-order intercept point (IP2)

tral components around ω_{INT}, causing the up-conversion of $1/f$ noise to close to RF frequency band. Consequently, the desired signal can be significantly corrupted by the tail of up-converted $1/f$ noise [23]. This phenomenon is problematic in both a heterodyne receiver and a direction conversion receiver.

To minimize the signal corruption caused by above mentioned mechanism, a LNA and a mixer can be designed in a fully differential manner in order to mitigate even-order distortion [24–26]. However, due to the typically single-ended output of an antenna, additional circuitry such as a lossy balun is required in order to perform a single-to-differential conversion with doubling power consumption. Additionally, the mismatches given by mixer switches and LO signals exhibit an undesired direct leakage path to the mixer output without frequency translation. Specifically this direct feedthrough effect is detrimental in the case of a direct conversion receiver. We will show a simple example in the following chapter.

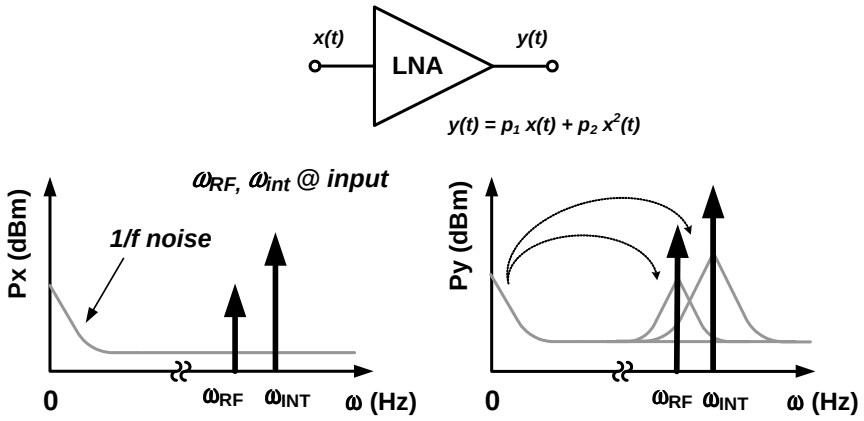


Figure 2.9: Definition of second-order intercept point (IP2)

2.2.5 Gain Compression

The small-signal conversion gain of down-converter remains at a constant value for small input signals. However, for large input power levels, the gain typically decreases due to saturation. The 1-dB compression point (P1dB), at which the gain decreases by 1 dB in comparison to the small-signal gain, is a critical performance metric (Fig. 2.10). Compression may arise as a consequence of small-signal nonlinearity of devices, or through voltage headroom limiting both of which can be caused by a large in-band signal or an out-of-band blocker.

The odd-order nonlinearity of a device can compress the conversion gain of a down-converter. If we assume $x(t) = A \cdot \cos \omega_1 t$ at the input third-order nonlinearity (Eq. 2.5) generates an additional term with the amplitude $(3/4) \cdot p_3 A^3$ that contributes to the fundamental amplitude at the desired fre-

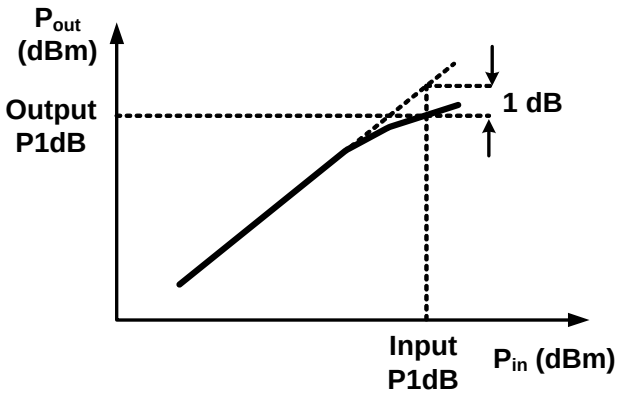


Figure 2.10: Definition of 1-dB compression point (P1dB)

quency $\omega_1 - \omega_{LO}$. Thus, the conversion gain is modified to $p_1 + (3/4) \cdot p_3 A^2$. When $(3/4) \cdot p_3 A^2$ becomes comparable to p_1, the gain begins to decrease as a function of A, for negative p_3. To maximize P1dB in down-converter designs, mostly contributed by above-mentioned mechanism, the third-order nonlinear coefficient p_3 must be minimized by applying proper circuit linearization techniques. A similar gain compression is also observed with large out-of-band blockers.

Gain compression is also caused by the limited voltage headroom of circuits. For MOSFETs, the amplified output signal must stay within the range where devices stay in the saturation region. If the input signal exceeds the limit of the power level at which devices enter the triode region, the transconductance of the devices decreases sharply. This leads to compression of the overall conversion gain. For the desired signal to achieve the maximum value at the output, the DC voltage of the signal path nodes should be chosen to be

in the middle of possible range. This compression mechanism is dominant in very high gain or low-supply voltage receivers.

Chapter 3

Review of Power-saving Techniques

There has been considerable research in recent years on low-power receivers that seek to increase battery lifetime and improve portability, while minimizing the impact on other system performance metrics such as dynamic range, noise and linearity. The problem has been approached from several perspectives including improvement of device performance, development of new circuit topologies and optimization at the architectural level. This chapter includes a short summary of recent work in this area along with a discussion of the merits and potential limitations of each approach.

3.1 Device Power Optimization

The power requirement of the receiver down-converter is directly related to the process technology used for the design. Scaling of CMOS technology has led to a significant improvement in the performance at RF. Assuming the scaling factor of technology is α, that is channel length and gate oxide are scaled by α, the transconductance and unity current gain frequency f_T at constant drain current per unit width are scaled by α and α^2, respectively [27, 28]. The f_T depends on the transconductance g_m and the intrinsic capacitance

of device, as given by Eq.(3.1)

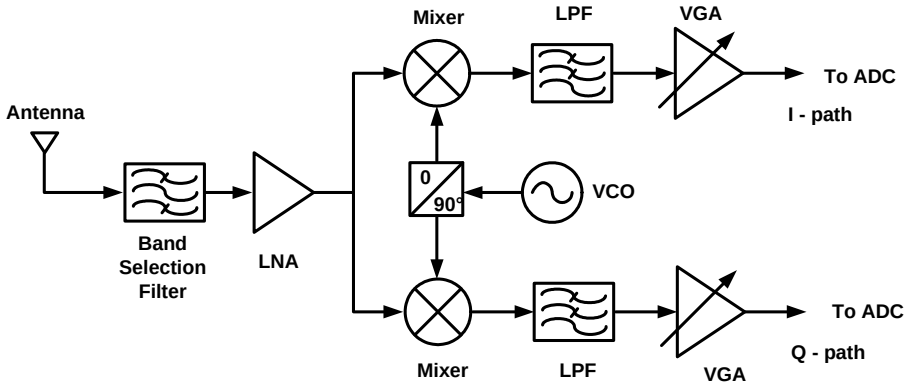
$$f_T = \frac{1}{2\pi} \cdot \frac{g_m}{C_{gg} + C_{gso} + C_{gdo}} \tag{3.1}$$

where, C_{gg}, C_{gso} and C_{gdo} represent the parasitic gate bulk capacitance and the gate-source and gate-drain overlap capacitance, respectively. With the scaling of CMOS technologies the power requirement for achieving a given gain decreases with the feature size of the technology. This aspect has been a significant factor in the continuous improvement in power efficiency of radio transceivers.

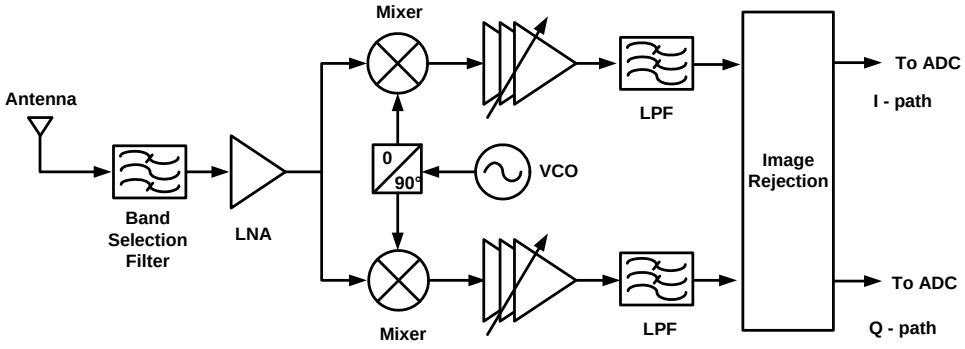
3.2 Power Efficient Receiver Architectures

Proper choice of receiver architecture for the given application, and optimal partitioning of the gain, noise, linearity, and selectivity of the receiver are critical for power minimization [24]. The selection of receiver architecture is determined by various system level requirements, such as power dissipation, selectivity, complexity, cost, and the number of external components. The heterodyne receiver architecture described in the previous chapter (Fig. 2.1) has been widely used in several high dynamic range applications such as GSM and WCDMA due to its excellent linearity performance that results from the use of passive discrete filters for rejection of interferers.

Integrated architectures such as direct-conversion [26, 29] and low-IF [10, 30–33] topologies have been used in several high-dynamic range systems in recent years as well. Fig. 3.1a shows a direct-conversion receiver architecture,



(a)

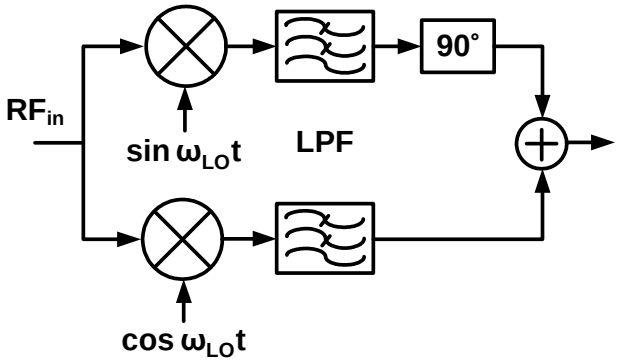


(b)

Figure 3.1: (a) Direct conversion receiver architecture (b) low-IF receiver architecture

which is also known as homodyne or zero-IF architecture. In this scheme, the RF signal is directly down-converted to baseband. These receivers have significantly lower complexity compared to heterodyne receivers. Several aspects of the direct conversion topology also serve to reduce power dissipation. Since the IF is located at DC, the need for an image-reject (IR) filter is inherently eliminated. The direct connection of the LNA to the mixer eliminates the need to drive a low-impedance load of an IR filter, which is advantageous since it helps in lowering the power dissipation in the LNA. Additionally, due to nearly zero IF frequency, integrated high-order low-pass active filters at baseband can replace high-quality band pass discrete components for the selection of the desired channel and the suppression of nearby interferers. Further variable gain amplification is implemented at baseband instead of a higher IF.

However, this topology has some well-known drawbacks related to DC offsets, LO leakage, $1/f$ noise and I/Q mismatch, which are not problematic factors in a heterodyne receiver [24]. Even-order distortion is another major issue in direct conversion receivers. A specific problem relates to the response of the receiver in presence of AM interferers. For example, a large AM interferer $m(t)\cos(\omega_{int}t)$ after being squared in the front-end generates a term at baseband that is proportional to $m^2(t)$. If the mixer switches are imbalanced or if there is an offset in the LO path, this baseband signal can leak to the output of the down-converter and degrade the baseband SNR. This is a very serious issue, since the interferer can potentially be at any frequency relative to the desired RF input.



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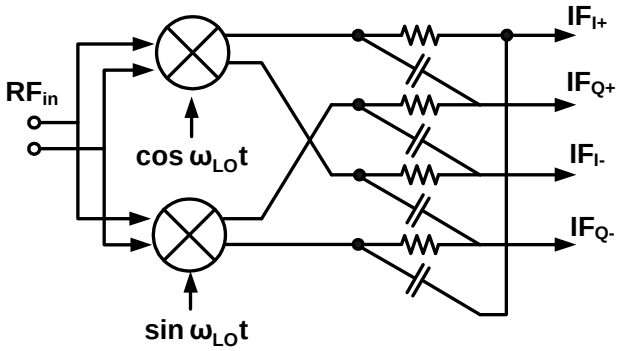

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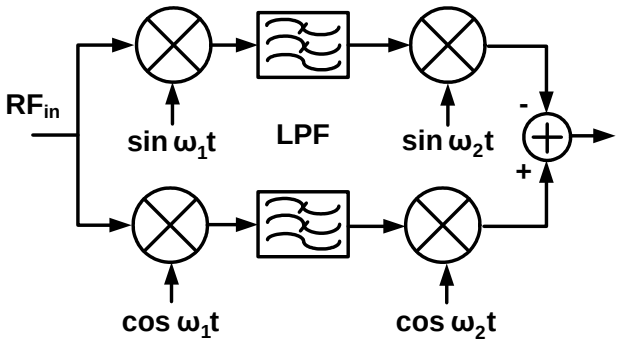


(c)

Figure 3.2: (a) Hartley (b) poly-phase filtering based on image-rejection (c) Weaver architecture

Low-IF receiver architecture may be used as an alternative approach (see Fig. 3.1b), and can alleviate at least some of the above mechanisms for performance degradation. The goal of this architecture is to combine the advantages of both heterodyne and direct conversion receivers. These can be considered to be integrated heterodyne receivers, where the IF frequency is chosen to be low, often of the order of one or two times the channel bandwidth. This is a desirable fact with respect to our power reduction objective because a higher IF frequency typically raises the power dissipation of the IF circuits. This design approach retains some of the advantages of a heterodyne receiver, such as immunity against the signal corruption caused by DC offset and $1/f$ noise. However, the image rejection can be a severe challenge, since the image frequency is relatively close to the RF signal frequency. Architectures, based on Hartley [34] and Weaver [35] down-converters (Fig. 3.2a and c) can be employed. Quadrature at baseband can be improved through the use of polyphase filters (Fig. 3.2b) [36]. However, these approaches are often limited to specific systems where it is a priori known that the power level at the image band is limited. Both Hartley and Weaver topologies are susceptible to phase mismatch and increasing the order of poly phase filters degrades noise performance.

3.3 Circuit Design Techniques

In addition to improving the power efficiency at the architectural level, there have been several studies that address the minimization of power con-

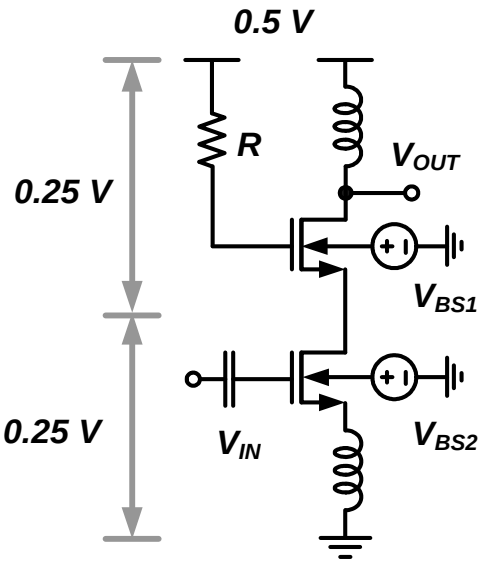


Figure 3.3: Design of an amplifier with 0.5 V supply

sumption at the circuit level. The use of low-voltage and bias-current reuse techniques, for example, have allowed for the design of ultra low-power receivers, that are compatible with certain system applications.

Operating the receiver at lower voltage can prove beneficial, especially for receivers with a large digital content. Digital power scales quadratically with the supply voltage. Thus in such cases, low supply voltage application is highly desirable. From the technological viewpoint, a decrease in the feature size of a transistor entails a lower supply voltage. Analog circuits operating in Class A mode also benefit decrease in supply voltage, provided adequate headroom is maintained.

Various circuit techniques have been proposed for low-voltage analog

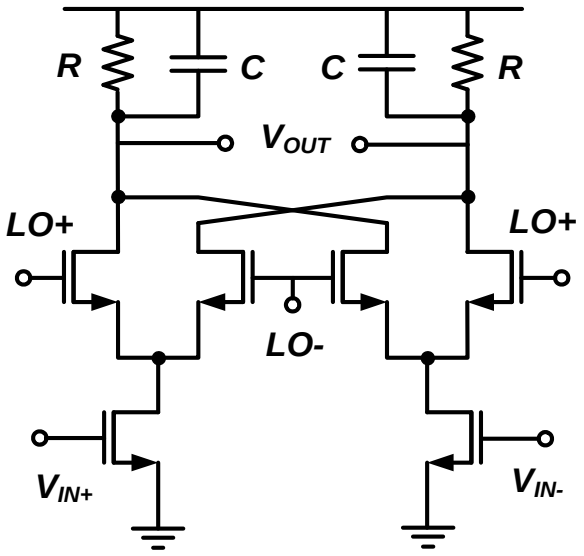


Figure 3.4: A conventional current commutating mixer

operation. For example, Stanic *et al.* [37, 38] recently reported a receiver front end that operates with a nominal supply voltage of 0.5 V, as shown in Fig. 3.3. By precisely controlling the overdrive voltage of devices, two stacked devices can be used in the front-end amplifier. In order to achieve a sufficient amount of amplification, the operation of devices needs to be retained at the edge of moderate or weak inversion. For this purpose, the threshold voltage (V_T) of devices is maintained at approximately 200 mV. Voltage headroom at the output is limited due to the 0.5 V supply.

The double-balanced Gilbert-type current commutating mixer shown in Fig. 3.4 has been widely used in several applications for frequency down-conversion due to its good performance with respect to the gain, NF and linearity. However since the DC current needs to flow through at least three

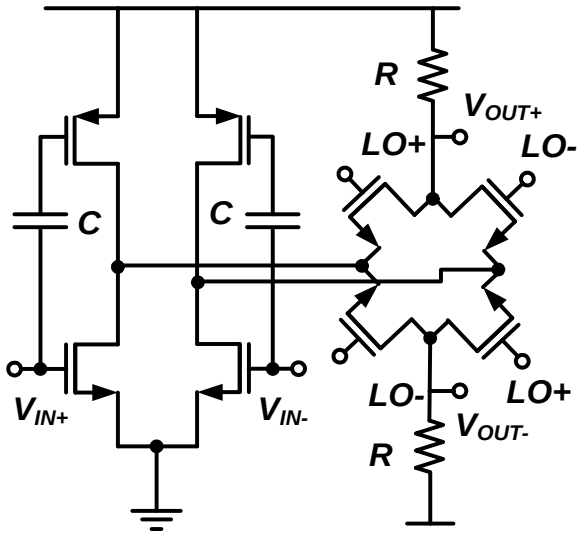


Figure 3.5: Design of a folded-switching mixer

stacked devices consisting of transconductors, switching transistors, and load resistors (see Fig. 3.4), low-voltage operation is challenging. In order to achieve a certain gain, sufficient current is required for the transconductance of the input devices. However, the voltage drop of the load resistors and switching stage becomes critical in low-voltage applications because stacked transistors need to operate in their saturation region.

The designs based on folded switching mixer topologies have been shown in [39, 40]. The design presented in [40] is shown in Fig. 3.5, where only a small part of the DC current flows through the switching devices and load resistors. In this design, the DC voltage drop across the load resistors can be linearly reduced by adjusting the ratio of current through load resistors to current through transconductors. As another example of a low-voltage

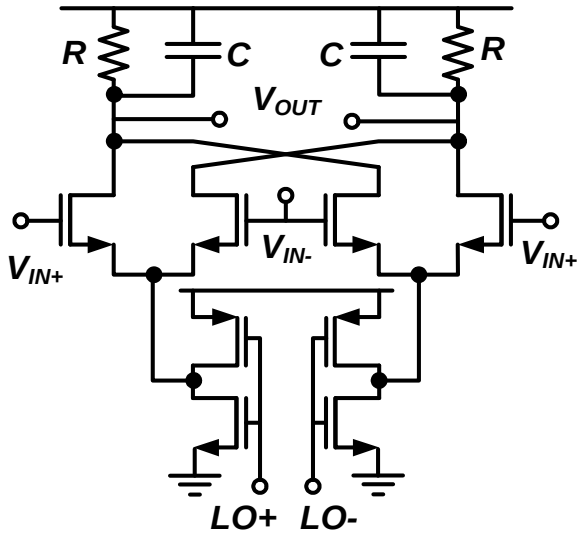


Figure 3.6: Design of a switched transconductor mixer

design for frequency translation, a switched transconductor mixer design was introduced by Klumperink [41] (depicted in Fig. 3.6). By employing low ohmic inverters as the source of the input devices, a square-wave transconductance function with a period of $1/f_{LO}$ was achieved. It eliminates the additional switching stage of the conventional mixer configuration. The mixer topologies presented above are able to successfully operate at low-supply voltages. However, to improve switching capability of the design Fig. 3.6, LO devices need to be sufficiently large, leading to more parasitic capacitance at the sources of the RF devices, thus reducing the LO signal levels.

A number of current-reuse techniques have also been introduced. A common technique is to share the bias between two circuit blocks such as amplifiers or amplifiers and mixers. Fig. 3.7a shows an example of a two-stage

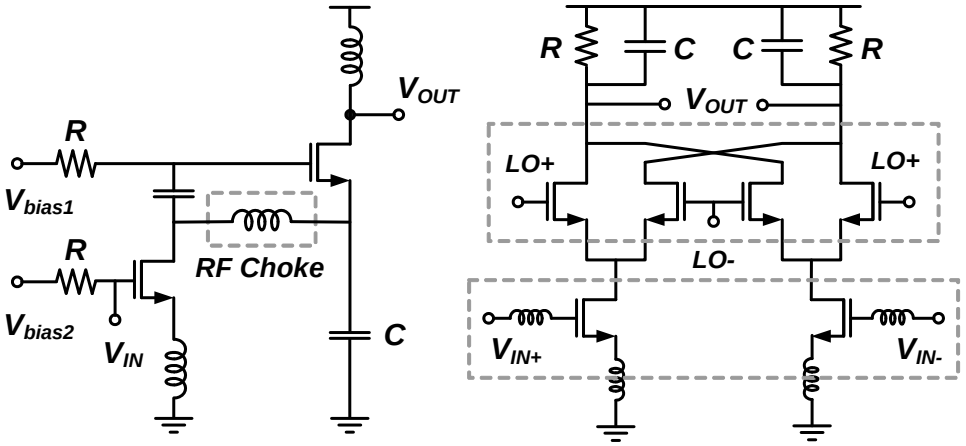


Figure 3.7: Design of stacked bias arrangement: (a) cascaded amplifiers (b) combined LNA and mixer

common source-amplifier [42]. The DC bias is shared between two transistors through an RF choke, thereby providing a large reactance for RF signals. In a different way, the RF is amplified by a cascade of two common-source amplifiers. In this case, assuming that the required transconductance is identical in the two transistors, power consumption is reduced by a factor of 2. This concept of stacking arrangement has been also applied to combine other functional blocks such as LNAs and mixers as shown in Fig. 3.7b [43]. By stacking the mixer switching stage on the top of transconductance devices, the bias current is reused instead of employing additional current-voltage and voltage-current (I-V and V-I) conversion steps.

In dual-band applications, the concept of current-reuse techniques has been extended to multiband reuse of the same bias current [44]. Typically, the

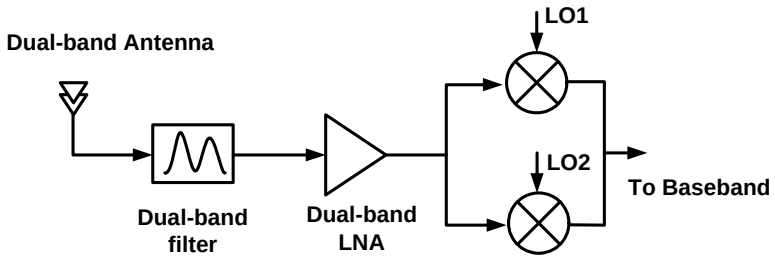


Figure 3.8: Concurrent dual band receiver architecture

implementation of concurrent dual-band receiver architecture consists of two independent receiver paths where each receiver path involves its own specific frequency band. However, for concurrent reception, both receiver paths need to be turned on and this leads to doubling the bias current consumption in comparison to the case where a single path is utilized for receiving a single band. However, if the receiver building blocks are shared to simultaneously handle two different frequency bands, the power efficiency of a concurrent receiver can be improved. Such as approach was suggested for example in [44] and is depicted in Fig. 3.8. A dual-band input filter is used to simultaneously amplify two-bands without increasing power dissipation.

In this chapter, various power saving techniques for low power applications have been reviewed from the viewpoint of both architecture and circuit design. In the following chapters, we propose a new current-reuse technique to implement low-power receivers, which is based on multiband signal feedback at orthogonal frequency bands.

Chapter 4

Low-power Receiver Down-converters with Signal Recursive

Design issues pertaining to a receiver down-converter and power-saving design techniques were presented in the previous chapters. Here we propose the concept of a multiband receiver down-converter where the signal is fed-back in a recursive manner into the gain stages of the circuit. We also estimate the power-saving capability in comparison to a conventional receiver counterpart. The low-power down-converter topology incorporates frequency translation, channel selectivity, and variable gain, while significantly decreasing the current requirement for a given gain and dynamic range. Two possible implementations are introduced.

4.1 Low-power Merged Mixer and Baseband Amplifier Utilizing Multiband Feedback

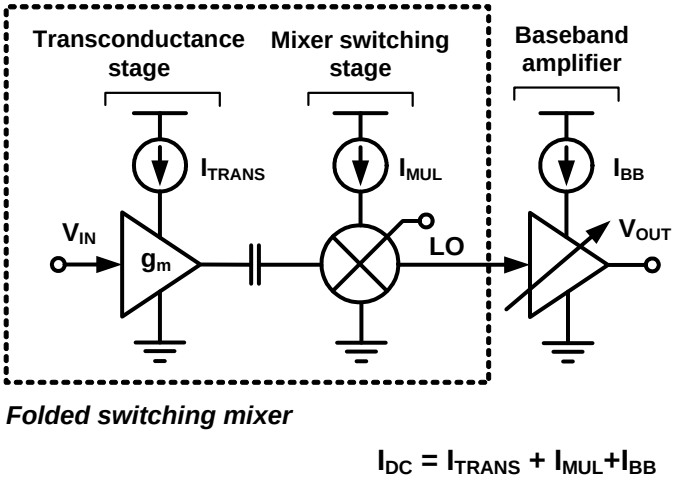
4.1.1 Principle of Operation

A key goal in our design is to minimize power dissipation in the receiver. In order to do so, a down-converter design is implemented that allows for significant power reduction by sharing the bias current for different tasks,

including mixing and baseband amplification. In principle, a receiver that shares the bias current for multiple tasks is very attractive, provided that the current sharing does not degrade the dynamic range.

The design of the down-converter is fundamentally based on the folded switching mixer shown in Fig. 4.1. Other implementations of folded swithcing mixer topologies is also shown in [39, 40]. It consists of two major components: an independent transconductance stage and a mixer switching core. This topology offers several advantages in comparison to a stacked current-commutating mixer, including the ability to operate at lower supply voltages and to independently optimize the performance of the transconductors and mixer switching stages through independently adjustable bias currents. While the transconductor current I_{TRANS} is set by the gain and dynamic-range requirement, a lower DC current in the switching stage, I_{MUL}, helps to reduce the noise contribution of the switching devices. Thus, the total bias current required can be similar to that of a stacked current-commutating mixer since I_{MUL} can be considerably smaller than I_{TRANS}. In the typical IF stage of receiver down-converter, a baseband amplifier (often with variable gain) follows the down-conversion mixer. In this case, the DC current requirement is $I_{TRANS} + I_{MUL} + I_{BB}$ (Fig. 4.1a).

The gain of the folded mixer can be significantly enhanced if the down-converted IF signal at the output of the switching stage is fed back to the input transconductance stage. In the design of Fig. 4.1b, the transconductance stage is connected to the mixer core through an ac-coupling capacitor, and it



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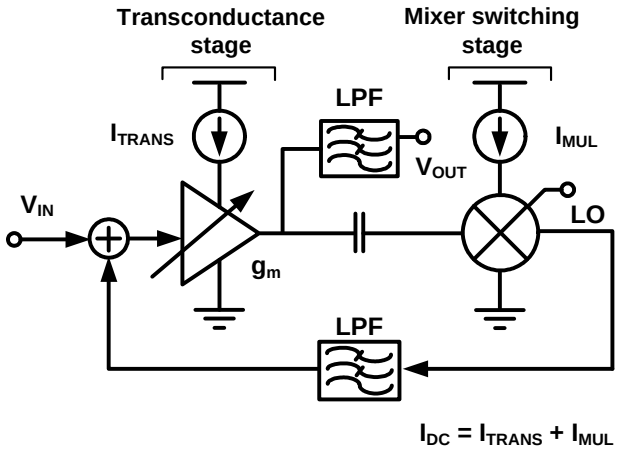


(b)

Figure 4.1: Conceptual views of (a) cascaded folded switching mixer and baseband amplifier and (b) merged mixer and baseband amplifier

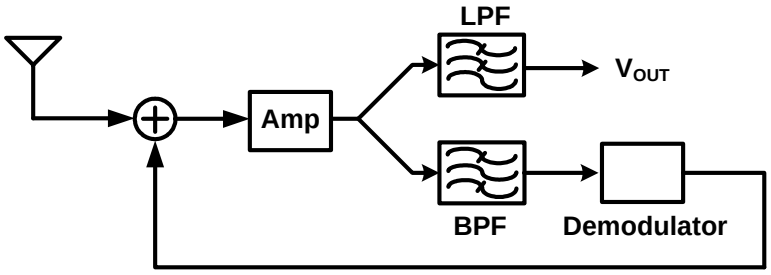


Figure 4.2: Block diagram of a reflex receiver

converts the RF signal into a small-signal RF current. The coupling capacitor serves to block DC and low frequencies. The switching core driven by an oscillator signal LO translates the narrow-band RF current to baseband. The design of Fig. 4.1b also incorporates a signal path introduced from the output of the mixer to the input of the transconductance stage through a bilateral low-pass filter LPF1. Since the down-converted IF signal at the output of the switching-stage is fed back to the input, the transconductance stage is reused for IF signal amplification. Thus, the bias-current of the folded mixer is used for the simultaneous amplification of both RF and IF signals. The ac-coupling capacitor located between the two stages provides a high impedance at the IF signal so that the final IF signal appears at the output through the low-pass filter LPF2. The required DC bias current is given by $I_{TRANS} + I_{MUL}$. Assuming the same amount of achievable gain for both designs, the power consumption of the proposed topology can be reduced by a significant factor because an additional baseband amplifier is not required.

The proposed topology is conceptually similar to a *Reflex Receiver circuit* whose concept was introduced in the early 1920s (Fig. 4.2) [45]. Reuse of the input amplifier helped to reduce the number of active devices, namely vacuum tubes, that could be expensive and bulky. By contrast, the key goal in this study is to reduce the power dissipation. Further, as described in detail in the following chapter, a key innovation in this work is that the topology eliminates the requirement for discrete filters through appropriate circuit techniques that are required in a reflex receiver type design in order to isolate the RF and IF bands. The use of these techniques makes integrated CMOS implementation of the architecture feasible.

The proposed design exploits orthogonality in the frequency domain to reuse the transconductance stage and its bias current to decrease the power dissipation. The operating principle is distinct from that of other front-ends that employ current reuse, such as [44, 46] that allow the simultaneous reception of two narrow-band channels in a single amplifier and [47] wherein separate amplifiers process signals in a single band while sharing the amplifier bias. This implementation of current reuse does not require the vertical stacking of circuits [42, 43], which can lead to a decrease in the available headroom.

The design is particularly suitable for low-voltage short-channel CMOS devices that have a relatively low intrinsic gain ($g_m r_o$) since it allows us to significantly enhance the achievable gain for a given bias current.

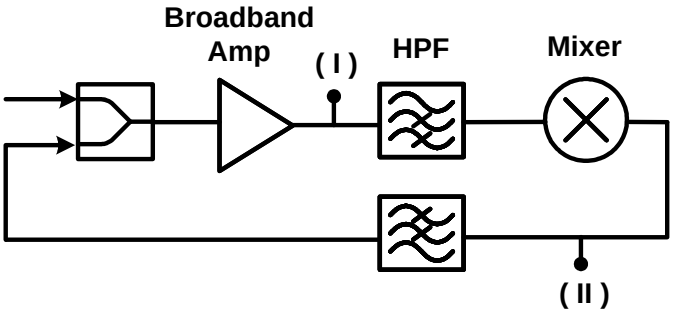


Figure 4.3: Prototype measurement setup

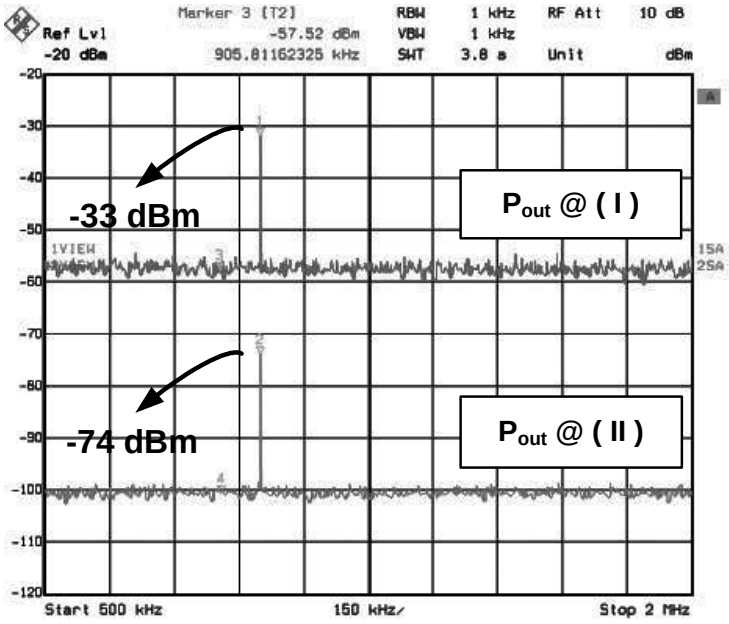


Figure 4.4: Measured gain in a discrete prototype

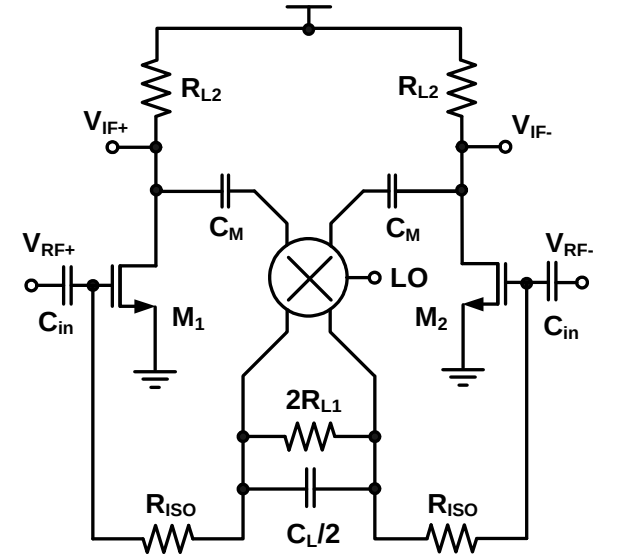
4.1.2 Prototype Measurements

The operating principle of the down-converter of Fig. 4.1b was verified in a prototype built from discrete components [48], consisting of two broadband amplifiers, a mixer, low-pass and high-pass filters and power splitters (Fig. 4.3). The RF gain of broad amplifiers is 40 dB. The results from a spot measurement are shown in Fig. 4.4. With an RF input power of -105 dBm at 900 MHz and an LO at 901 MHz, the output power at baseband after the mixer (II) is -74 dBm, which implies a conversion gain of 31 dB. This includes the cascaded gain of the amplifiers and the conversion loss of the mixers and the insertion loss of filters and splitters. The signal at the output of the mixer is applied to a low-pass filter and coupled back to the input of the amplifier through a power splitter. The IF signal at the amplifier output has a power level of -33 dBm, which implies an overall IF gain of 72 dB. Consequently this prototype measurement verifies the concept of the architecture described below and indicates the possibility of implementation in an IC form where a broadband amplifier can be reused for baseband amplification in order to reduce the power consumption.

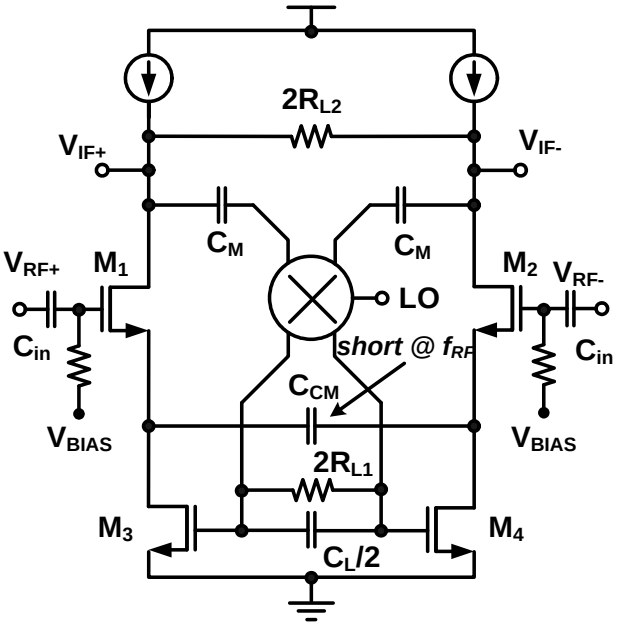
4.2 Basic Implementation

4.2.1 Receiver Down-converter with Transconductance Reuse

To realize the proposed topology, two basic differential configurations are shown in Fig. 4.5. In the design of the circuit in Fig. 4.5a, the input



(a)



(b)

Figure 4.5: Basic differential feedback-based configuration with (a) transconductance (g_m)-reuse and (b) current-source (CS)-reuse

transconductors (M_1 and M_2) are reused for both RF and IF signal amplification. The design principle relies on the broadband nature of the transconductance of the input devices. The device is capable of providing independent linear gains at multiple distinct frequencies, provided that the signal at any one frequency is not sufficiently large to drive the device into compression. The drains of the input devices in Fig. 4.5a are AC-coupled to the inputs of the differential down-conversion mixer through the capacitor C_M. The input impedance of the mixer switching stage is designed such that it is considerably smaller than the load resistors R_{L2} so that the majority of the RF signal current in the input transconductors flows into the mixer with minimum signal attenuation. A first-order low-pass network at the output of the mixer attenuates undesired high-frequency leakage components such as RF and LO leakage and their harmonics. The conversion gain from the input of the transconductor to the output of the mixer is related to the expression $g_m R_{L1}$, where the transconductance of M_1 and M_2 is given by g_m.

The IF signal is fed back and coupled to the inputs of the transconductors through a resistor R_{ISO} that prevents the incoming RF signal from being loaded by the output impedance of the mixer. In the absence of this resistor, the RF signal will be attenuated by the capacitors C_{L1}. The input AC-coupling capacitors C_{in} present a high impedance at the IF so that the IF at the output of the mixer can appear unmitigated at the input of the RF transconductor and be reamplified. The reactance of the capacitors C_M is large at the IF. Hence, the IF current provided by the input transconductors is converted into

a differential voltage at the load resistors R_{L2}. Consequently, the net gain of the design is related to the product of the conversion and low-frequency gains, i.e.,

$$A_v \propto g_m^2 R_{L1} R_{L2} \tag{4.1}$$

Thus, the total gain is enhanced by a factor of $g_m R_{L2}$ as compared to the conventional folded mixer topology without an increase in the current consumption.

4.2.2 Receiver Down-converter with Current Source Reuse

Fig. 4.5b depicts another approach that reuses the current source (CS) devices (M_3 and M_4) that are used to bias the RF devices for IF signal amplification. The input device M_1 and current source M_3 (and similarly M_2 and M_4) share the same bias currents and provide better isolation between the RF input and the mixer output. Thus, the feedback resistor R_{FB} used in Fig. 4.5a can be eliminated. The transistors M_1 and M_2 convert the RF input voltage into a current that is down-converted by the mixer. The capacitor C_{CM} is assumed to be a short at RF and open at IF. After the frequency down-conversion, the IF output of the mixer is applied to the gates of M_3 and M_4, which operate as common source amplifiers, and is further amplified. The net gain of this configuration is given as follows:

$$A_v \propto g_m g_{m,CS} R_{L1} R_{L2} \tag{4.2}$$

where $g_{m,CS}$ is the transconductance of M_3 and M_4. Compared to the previous approach, this approach allows for the independent optimization of the RF and

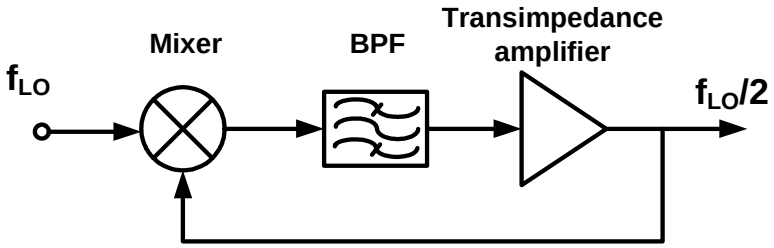


Figure 4.6: Block diagram of a regenerative frequency divider

baseband transconductors by adjusting the size of the devices. Both the above approaches can also be implemented in a single-ended form.

4.2.3 Potential Mechanisms for Degradation

The architecture proposed above can provide a very high gain in a tightly coupled feedback loop and hence stability is a potential concern in the design. In fact, it can be observed, from the perspective of the LO input to the mixer switching stage, that the architecture of Fig. 4.1b is similar to that of a regenerative frequency divider (Fig. 4.6) [49]. In the basic implementation of Fig. 4.5a-b, the out-of-band suppression provided by the first-order low-pass (R_L and C_L) and high-pass (C_M) filters is non-ideal. Thus, as graphically explained in Fig. 4.7, the residual IF current can leak into the mixers through the coupling capacitors, be up-converted to RF, and be fed back to the input stage again. This will interfere with the incoming RF signal at the input, potentially leading to instability.

From Fig. 4.5a, the gain for the conversion from RF to baseband at the

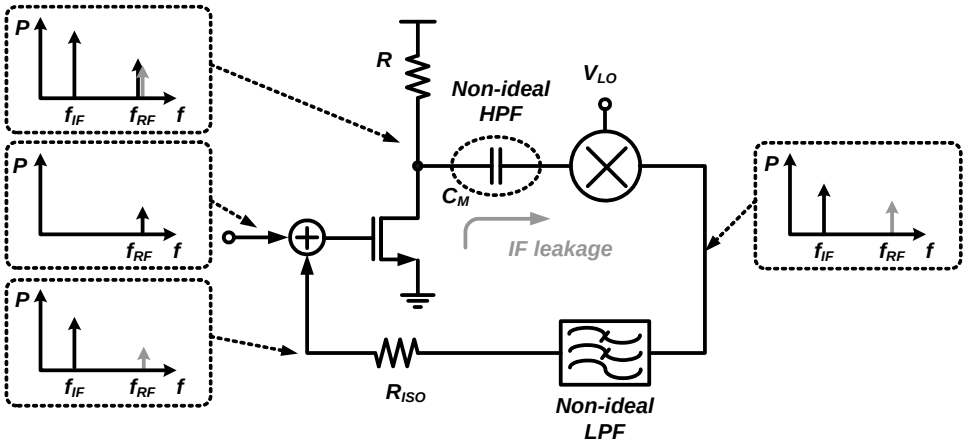


Figure 4.7: Potential instability mechanism caused by nonideal out-of-band attenuation

input is given by

$$A_{v,RF\rightarrow IF} \cong K \cdot g_m \left(R_{L1} \parallel 1/j\omega_{IF}C_L\right) \tag{4.3}$$

if we ignore the impedance of R_{ISO}. K is a scaling constant related to the switching behavior of the mixer (e.g., $2/\pi$ for switching with a square wave). The IF at the input is amplified by the transconductor, is up-converted to RF, and reappears at the input with a gain

$$\begin{aligned} A_{v,IF\rightarrow RF} \cong K g_m &\left(\frac{j\omega_{IF}C_M R_{L2}}{1+j\omega_{IF}C_M R_{L2}}\right) \\ &\cdot\left(\frac{R_{L1}}{(1+j\omega_{RF}C_L R_{L1})\cdot(1+j\omega_{RF}C_{in}R_{ISO})+(j\omega_{RF}C_{in}R_{L1})}\right) \end{aligned} \tag{4.4}$$

which includes the RC low-pass formed by R_{ISO} and C_{in}. A sufficient condition for the loop to be stable is that $A_{v,RF\rightarrow IF} \cdot A_{v,IF\rightarrow RF}$ has to be less than unity [50].

The loop gain of above spurious feedback can be minimized by the use of sharp higher-order filters, in place of the simple first-order sections formed by R_{L1} and C_L, and C_M and R_{L2}. However, on-chip implementations of such filters would increase power dissipation, and off-chip implementations are unattractive due to area and cost considerations. A solution of this issue will be addressed in the final implementation by means of circuit techniques in chapter 5.

Another key consideration in the design is the potential for the degradation of the linearity owing to spurious products that arise as a consequence of the multiband feedback topology. For example, consider a close-in interferer at ω_{INT} near the desired RF frequency band along with the IF signal at the input of the transconductor stage that is not readily attenuated by the band-selection filter (Fig. 4.8). In the case of Fig. 4.5a, the beat products of a strong interferer associated with the previously amplified IF signal will generate second-order distortion products due to the nonlinearity of the input devices; the distortion products are given by

$$\begin{aligned}\left[A_{INT}\cdot\cos\left(\omega_{INT}t+\theta\right)+A_{IF}\cdot\cos\left(\omega_{IF}t\right)\right]^2 \\ \rightarrow A_{INT}\cdot A_{IF}\cdot\cos\left(\omega_{INT}+\omega_{IF}\right)t\end{aligned} \tag{4.5}$$

where A_{INT} and A_{IF} are the amplitudes of the interferer and IF signal at the input, respectively. The term θ denotes the unknown relative phase of an interferer. When $\omega_{INT}+\omega_{IF}\approx\omega_{RF}$, the spectrum of the beat product can overlap with the RF signal, thereby resulting in the degradation of the

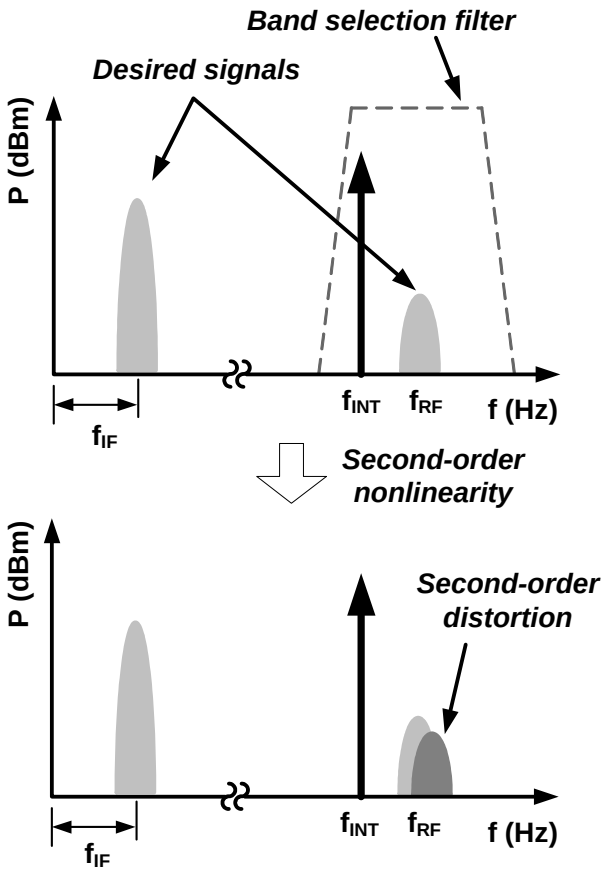


Figure 4.8: Second-order intermodulation distortion of down-converter with g_m-reuse

effective signal-to-noise ratio.

The presence of the IF at the input along with external interferers can also lead to the possibility of degradation in the third-order IM product through similar mechanisms that occurs in the case of second-order distortion. This is discussed in depth in the following chapter. Unique characteristics of the design with respect to third order IM are also analyzed.

The above potential impairments in the multiband feedback based design need to be mitigated through proper design techniques. This is discussed in the next chapter, where actual circuit implementations utilizing the basic architectural principles presented here are shown.

Chapter 5

Implementation

Two circuit topologies that utilize the multiband feedback principle of chapter 4 are demonstrated here in a short-channel CMOS technology [48, 51–53]. As shown below, the topologies avoid issues related to linearity degradation and stability. One of the topologies also has the ability to cancel third-order intermodulation distortion. In this chapter, we analyze various aspects of down-converters' performance. The discussion includes the frequency response of the down-converters, as well as the dynamic range performance including, gain, noise and linearity.

5.1 Pseudo Differential Architecture

5.1.1 Basic Configuration

As discussed in chapter 4, inadequate rejection available from high-pass or low-pass filters at the input and output of the mixer respectively, can lead to the potential for instability in a practical implementation. One way to guarantee stability is to employ sharp high-order passive or active filters, which would imply an increase in area, cost and power dissipation. This would go against the basic motivation for attempting this topology.

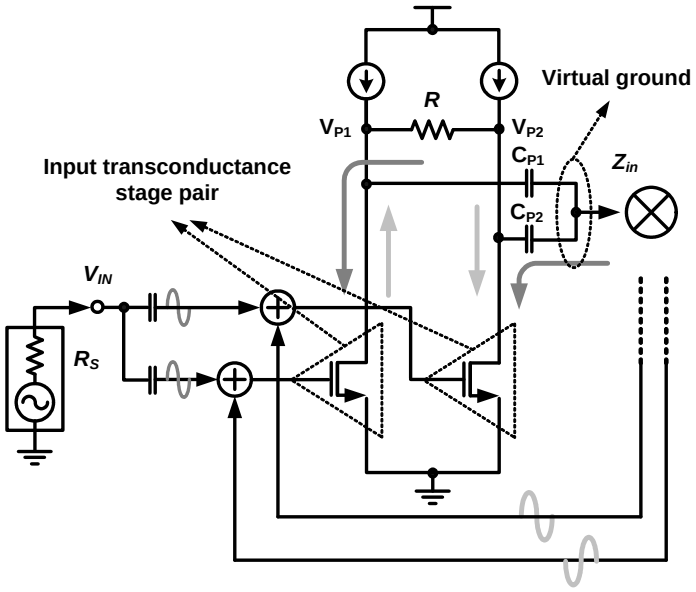


Figure 5.1: Pseudo-differential configuration

Fig. 5.1 shows a conceptual view of a pseudo-differential architecture that can be used to implement the proposed topology without the use of such filters. As illustrated in Fig. 5.1, two identical input devices are utilized as a combined RF input stage instead of a single device. These devices are sized to be half of a single device that would provide the required transconductance at the desired current bias. The inputs and outputs of the devices of the transconductance pair are AC-coupled through identical capacitors such that they can operate as a single device at RF. Since the RF currents supplied by the input stages are in-phase, the resistor R does not contribute any loading to the RF signals; therefore, the combined RF current flows into the mixing stage and is down-converted to IF. As explained previously, the transconductance of the

input stages provides gain at both the RF and the IF. The differential outputs of the mixer are fed back to the input pair through differential feedback paths. At IF, the input pair amplifies the signals as a differential amplifier. Thus the input device pair operates in-phase at RF, and in a pseudo-differential mode at IF. Consequently, dualband utilization of transconductance is realized where both in-phase RF and anti-phase IF signals simultaneously appear at the signal paths of the input transconductance pair.

5.1.2 Stability Enhancement

The pseudo differential configuration of the input device pair at base-band, yields a significant benefit with regards to stability. In Fig. 5.1, the IF signals at nodes V_{P1} and V_{P2} are antiphase. Therefore, any residual IF leakage through capacitors C_{P1} and C_{P2} is canceled at the input of the mixer assuming that the devices are perfectly matched. The loop gain $A_{v,RF\rightarrow IF} \cdot A_{v,IF\rightarrow RF}$ given by the product of Eqs. (4.3) and (4.4) thus becomes zero since the term $A_{v,IF\rightarrow RF}$ is ideally set to zero. Consequently, the potential for instability is ideally eliminated.

In practice, a small residual IF may still appear at the mixer input due to capacitor mismatches and at the second-order harmonic of IF that arises from second-order nonlinearity in the tail current sources in the CS-reuse design or the input devices in the g_m-reuse design; however, these terms are expected to be small. As mentioned previously, instability can be caused by the external signals as well as the noise at frequencies where coupling through

C_{P1}-C_{P2} may be substantial. Since this technique allows us to implement transconductance reuse without requiring sharp passive low-frequency filters for the isolation of the RF and IF signals, it is a key enabler for the scheme.

5.2 Pseudo Differential Down-converter with Input Transconductance Reuse

5.2.1 Circuit Description

The detailed schematic diagram of the implemented down-converter that relies on the g_m-reuse principle depicted in Fig. 4.5a is shown in Fig. 5.2. In order to implement a fully differential receiver down-converter, two input device pairs are utilized. The input devices M_1 and M_2 are replaced by device pairs (M_{1a}, M_{1b}) and (M_{2a}, M_{2b}) that employ identical transistors and are used as the RF input transconductors. These devices are self-biased through resistors R_X and R_Y. The drain bias currents are provided by PMOS current mirrors that present a large output impedance at the drain nodes of (M_{1a}, M_{1b}) and (M_{2a}, M_{2b}). A double-balanced current-commutating PMOS mixer is employed for frequency translation. The drains of the input devices are directly AC-coupled to the mixer switching core at nodes V_X and V_Y. The mixer is also biased using PMOS current sources to provide a small DC bias current in the switching devices, primarily to ensure that the devices are nominally in the saturation region when they turn on. The RF impedance at nodes V_X and V_Y is set by the impedance looking into the PMOS switches, which is of the order of $1/g_{m,PMOS}$ and is thus small as compared to the loads at the drains of the

input devices. Therefore, this ensures that the RF drain current of (M_{1a}, M_{1b}) and (M_{2a}, M_{2b}) flows preferentially into the PMOS switches, which minimizes RF signal attenuation from the parasitic impedance at the drain nodes. The outputs V_{IF+} and V_{IF-} of the mixer are differentially connected to the inputs of the device pairs (M_{1a}, M_{2a}) and (M_{1b}, M_{2b}) through identical isolation resistors R_{ISO}. The DC voltage level at the output nodes of the mixer is thus equal to the gate voltage of the input devices. A control voltage V_{BIAS} is used to set the bias current in M_{3a-b} equal to that of the mixer switches. Transistor M_{AGC} is connected across the differential outputs of the mixer. The gain of the down-converter can be varied by controlling its on-resistance through its gate voltage. The baseband outputs of the down-converter are sensed differentially across the drains of (M_{1a}, M_{1b}) and (M_{2a}, M_{2b}) by using unity-gain low output impedance buffers.

The small-signal RF and IF voltages at the gates of M_{1a}, M_{1b}, M_{2a}, and M_{2b} are given by (v_{in+}, v_{ifg+}), (v_{in+}, v_{ifg-}), (v_{in-}, v_{ifg+}), and (v_{in-}, v_{ifg-}), respectively. As before, the devices (M_{1a}, M_{1b}), and similarly (M_{2a}, M_{2b}), process the RF signal in-phase and operate as pseudo-differential amplifiers at baseband.

By assuming ideal square-wave switching in the mixer, the net in-band gain, which represents the gains from V_{IN} to V_{OUT}, is given by

$$A_{v,g_m-reuse} \cong \frac{2}{\pi} g_{m1/2}^2 R_X R_Y \tag{5.1}$$

where $g_{m1/2}$ is the input device transconductance, as shown in Fig. 5.2. Ideally,

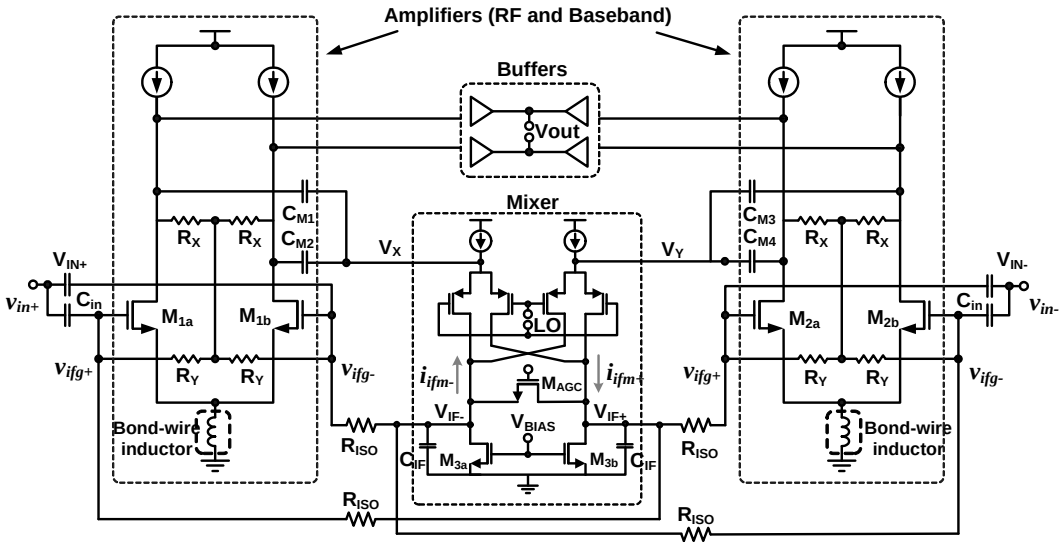


Figure 5.2: Pseudo-differential down-converter with g_m-reuse

R_{ISO} does not affect the gain. Since $A_{v,g_m-reuse} \propto g_{m1/2}^2$ in Eq. (5.1), for square-law devices, the gain increases linearly with the bias current I_{bias} rather than $\sqrt{I_{bias}}$ as in the case of a basic common-source amplifier which allows for a significantly greater gain per unit power dissipation.

The input impedance Z_{IN} of the stage looking into v_{in+} at RF is given by

$$Z_{IN} \cong \frac{R_X + R_Y}{2\left(1 + g_{m1/2}/g_{m,PMOS}\right)} \parallel \frac{R_{ISO}}{2} \tag{5.2}$$

to the first order. The mixer input impedance is assumed to be $1/g_{m,PMOS}$.

5.2.2 Frequency Response

After frequency down-conversion, the baseband signal in this topology can be shown to be effectively filtered by a third-order low-pass filter. As

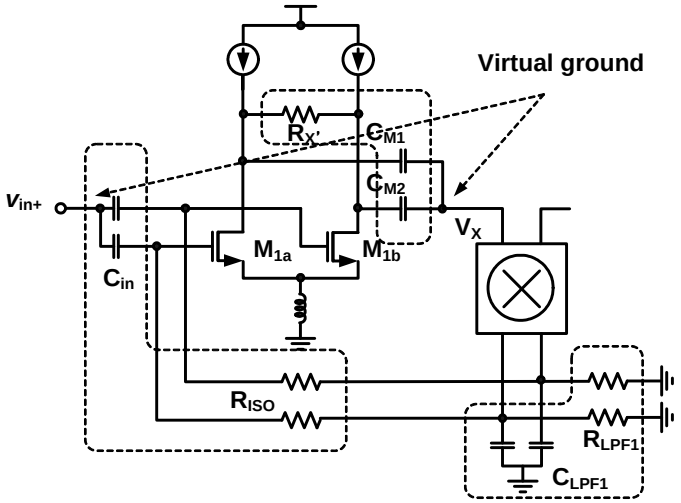


Figure 5.3: Built-in third-order low-pass responses produced by the simplified down-converter with g_m-reuse

discussed below, an interesting feature of this design is that the capacitors that are used for AC-coupling at RF also provide low-frequency poles at IF, and increase the order of filtering available from the down-converter.

The left half of the simplified schematic of Fig. 5.2 is shown in Fig. 5.3. A first-order low-pass filter is implemented by the parallel combination of R_Y and C_{IF} at the mixer output. From Fig. 5.3, it can be observed that due to the pseudo differential nature of the input device pair, the external RF input and input of the mixer can be considered to be virtual grounds for differential baseband signals. Therefore, two additional poles are observed to result from R_{ISO} and C_{in} and R_X and $C_{M1/2}$ at the inputs of the device pair and the mixer, respectively, which results in an overall third-order low-pass response.

The RF signal v_{in+} is converted to in-phase RF currents in M_{1a} and

M_{1b} and coupled into the mixer at V_X through C_{M1} and C_{M2}. Similarly, the devices M_{2a} and M_{2b} convert the opposite-phase RF signal v_{in-} to an RF current, which is also coupled to the mixer. The RF current is translated to IF in the mixer. The IF currents (i_{ifm+} and i_{ifm-}) flow through resistors R_{ISO} and are converted to a differential voltage (v_{ifg+} and v_{ifg-}) across the gates of the device pairs (M_{1a}, M_{1b}) and (M_{2a}, M_{2b}) in resistor R_Y. Therefore, the conversion gain from the RF input to the IF output voltage is proportional to $g_{m1/2}R_Y$, where $g_{m1/2}$ is the transconductance of M_{1a-b} and M_{2a-b}. R_{ISO} does not affect the conversion gain.

The transfer function from the IF current to the IF voltage appearing at any one of the gates of the input devices (v_{ifg}), ignoring polarity, is given by

$$\frac{v_{ifg}(s)}{i_{ifm}(s)} = \frac{R_Y/2}{1 + s\Big\{C_{in}R_Y + \frac{C_{IF}}{2}(R_{ISO} + R_Y)\Big\} + s^2 C_{in}\frac{C_{IF}}{2}R_{ISO}R_Y} \tag{5.3}$$

This is a second-order low-pass transfer function. The input capacitors that couple the RF signal contribute to additional low-pass response at baseband. The final IF voltage outputs are obtained across the drains of (M_{1a}, M_{1b}) and (M_{2a}, M_{2b}), where the IF currents in transistors (M_{1a}, M_{1b}) and (M_{2a}, M_{2b}) are converted to voltages by the impedance of the parallel combination of R_X and C_M. Therefore, the transfer function from i_{ifm} to v_{out} is given by

$$\frac{v_{out}(s)}{i_{ifm}(s)} = \frac{R_Y/2}{1 + s\Big\{C_{in}R_Y + \frac{C_{IF}}{2}(R_{ISO} + R_Y)\Big\} + s^2 C_{in}\frac{C_{IF}}{2}R_{ISO}R_Y} \cdot \frac{g_m R_X}{1 + sR_X C_M} \tag{5.4}$$

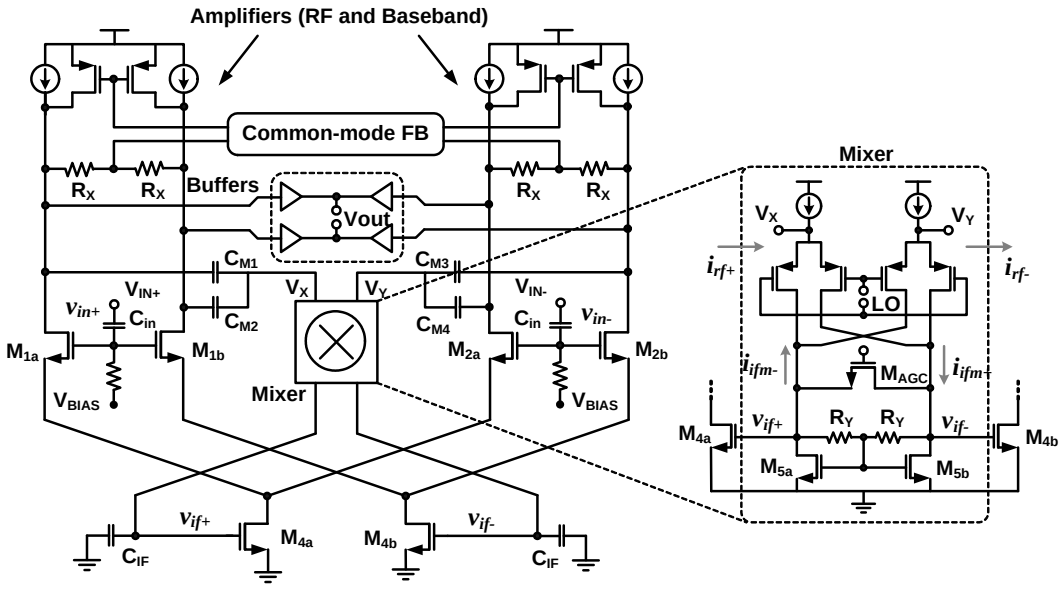


Figure 5.4: Pseudo-differential down-converter with CS-reuse

This is a third-order low-pass transfer function and it can be effectively used for enhancing the channel selectivity. Since the capacitors used for AC coupling the RF signal are reused for providing low-pass filtering, additional area is not required for increasing the selectivity at baseband.The corner frequency of this third-order LPF can be adjusted by choosing the values of the capacitors (C_{in}, C_{IF}, and C_M). The conversion gain is determined by the values of the resistors R_X and R_Y, as seen in Eq. (5.4).

5.3 Pseudo Differential Down-converter with Current Source (CS)-reuse

A pseudo-differential feedback-based receiver down-converter using the CS-reuse principle is shown in Fig. 5.4. This is the practical implementation of the design of Fig. 4.5b. As in the previous case, two differential input pairs comprising identical devices (M_{1a}, M_{1b}) and (M_{2a}, M_{2b}) are used as the RF input transconductors. The gates of these devices are externally biased by resistors with large values. Transistors M_{4a} and M_{4b} are current source devices that are used to bias these input differential pairs. Since these transistors have a high output impedance, the RF differential amplifiers exhibit substantial common-mode rejection. The resistors R_X do not contribute to the gain at RF since the RF voltages at the drains of (M_{1a}, M_{1b}) and (M_{2a}, M_{2b}) are in-phase. The RF currents produced by these device pairs are coupled into a PMOS double-balanced current commutating mixer through capacitors C_{M1}-C_{M4} in a manner similar to the implementation shown in Fig. 5.2. The mixer loads comprise of self-biased NMOS transistors M_{5a} and M_{5b}. These are biased through resistors R_Y at the mixer output. The DC in these devices is mirrored in the mixer tail current sources M_{4a} and M_{4b}. The mixer load is differentially given by $2R_Y$. The down-converted amplified differential signals v_{if+} and v_{if-} appear at the gates of transistors M_{4a} and M_{4b}. The IF currents of M_{4a} and M_{4b} are equally divided in (M_{1a}, M_{2a}) and (M_{1b}, M_{2b}) and are converted to an IF voltage across the resistors R_X. The devices M_{1a}, M_{1b}, M_{2a}, and M_{2b} operate as the upper devices of a cascode amplifier at IF.

Variable-gain functionality is implemented by controlling the on-resistance of M_{AGC} through its gate voltage, as described previously. A common-mode feedback (CMFB) is applied to maintain the DC level at the drains of the input devices. The common-mode voltage is sensed by resistor R_X, and the bias currents are adjusted accordingly through the PMOS current mirrors. The input impedance of the design is set by the gate impedance of the RF input devices.

The RF input voltage is converted into a baseband current at the mixer output. The transfer function from v_{in} to i_{ifm} is given by

$$\frac{i_{ifm}(s)}{v_{in}(s)} = \frac{4}{\pi} \cdot g_{m1/2} \tag{5.5}$$

where $g_{m1/2}$ is the transconductance of the input devices (M_{1a}, M_{1b}, M_{2a}, and M_{2b}). The transfer function from i_{ifm} to v_{out} is given by

$$\frac{v_{out}(s)}{i_{ifm}(s)} = \frac{R_Y/2}{(1 + sR_YC_{IF})} \cdot \frac{g_{m4}R_X}{(1 + sR_XC_M)} \tag{5.6}$$

where g_{m4} is the transconductance of the current sources (M_{4a} and M_{4b}). Eq. (5.6) demonstrates a second-order low-pass response. This topology thus also exhibits increased baseband low-pass filter order without adding an additional passive or active LPF, which can be used for better channel selectivity. Compared to the previous implementation, RF inputs are separated from IF signal paths. Thus C_{in} does not contribute to low-pass filtering.

5.4 Noise Performance of Receivers

Unlike RF and baseband signals that are in-phase and anti-phase in the input devices respectively, the noise produced by various sources in the transconductance stage and mixer stage independently affects output noise performance, since the device noise sources are independent. Due to the reuse of the devices at RF and IF, some devices contribute noise at both LO sidebands and IF. The noise at the down-converter output is the sum of all individual noise contributions expressed in V^2/Hz. In this section, the noise performance of the down-converters with g_m- and CS-reuse, shown in Fig. 5.4, is analyzed. In the discussions below, we ignore the induced gate noise of the devices.

5.4.1 Noise Analysis of the Down-converter with g_m-reuse

The g_m-reuse design (Fig. 5.2) has three primary noise contributors: RF input devices (M_{1a-b}, M_{2a-b}), NMOS current source devices (M_{3a-b}), and mixer switches. The drain current noise of each input MOSFET device is modeled as the channel thermal current noise given by [54]

$$\overline{i_{n,1/2}^2} = 4KT\gamma g_{do1/2}\triangle f \tag{5.7}$$

where $g_{do1/2}$ is the zero-bias drain conductance of M_{1a-b} and M_{2a-b}, and γ denotes the bias-dependent coefficient of channel thermal noise. This parameter is greater than 2 for short channel devices operating in saturation [14, 55, 56].

The thermal noise of input transistors M_{1a-b} and M_{2a-b} is broadband

in nature. Thus the noise around the LO sidebands is translated through the mixer and undergoes the same amplification as the signal. Since the in-band gain of the down-converter from input to ouput is expressed as $2/\pi g_{m1/2}^2 R_X R_Y$, the transimpedance gain i_{RF} to v_{out} is $2/\pi g_{m1/2} R_X R_Y$. Thus the noise of the input devices at the output is given by

$$\overline{v_{no,1/2}^2} = 4 \times \frac{4}{\pi^2} \cdot \overline{i_{n,1/2}^2} g_{m1/2}^2 R_X^2 R_Y^2 \tag{5.8}$$

Therefore, the input referred noise of M_{1a-b} and M_{2a-b}, scaled by a factor of $\left(2/\pi g_{1/2}^2 R_X R_Y\right)^{-2}$ is expressed as

$$\overline{v_{ni,1/2}^2} = 4 \times \overline{i_{n,1/2}^2} / g_{m1/2}^2 \tag{5.9}$$

The devices comprising the switching core and the load of the mixer are also key noise contributors. The noise of these devices is further amplified by RF input devices, resulting the NMOS current source devices M_{3a-b} and the switching devices significantly affect the output noise. The flicker noise of M_{3a-b} and the thermal and flicker noise of the switches are modeled by [12, 13]

$$\overline{i_{n,3,1/f}^2} = (g_{m3}^2 k_{1/f} \triangle f)/(f_{IF} W L C_{ox}) \tag{5.10}$$

$$\overline{i_{n,SW,wh}^2} = (4KT\gamma I_{B,SW} \triangle f)/(\pi A_{LO}) \tag{5.11}$$

$$\overline{i_{n,SW,1/f}^2} = (I_{B,SW} \cdot V_{n,1/f}(f) \triangle f)/(\pi A_{LO}) \tag{5.12}$$

where W and L denote the width and length of the devices respectively, $K_{1/f}$ is the device specific constant, $I_{B,SW}$ is the DC current of the mixer switches and A is the amplitude of the LO signal. $V_{n,1/f}(f)$ indicates an input referred

voltage determined by the inversion layer charge fluctuation of switches [12, 13]. From Eq. (5.4), the output noise of these noise sources is given by

$$\overline{v^2_{no,3,1/f}} = 2 \times \overline{i^2_{n,3,1/f}} g^2_{m1/2} R^2_X R^2_Y \tag{5.13}$$

$$\overline{v^2_{no,SW,wh}} = 4 \times \overline{i^2_{n,SW,wh}} g^2_{m1/2} R^2_X R^2_Y \tag{5.14}$$

$$\overline{v^2_{no,SW,1/f}} = 2 \times \overline{i^2_{n,SW,1/f}} g^2_{m1/2} R^2_X R^2_Y \tag{5.15}$$

The flicker noise of M_{3a-b} is particularly important at the output because the noise arising from the switches is inversely proportional to $\pi \cdot A_{LO}$, typically greater than unity. Other noise contributors in the down-converter with g_m-reuse (Fig. 5.2) are summarized in Table 5.1.

In order to reduce the noise figure of the design, as shown in Eqs. 5.9-5.15, the transconductance of RF input device $g_{m1/2}$ must be maximized, and the bias current of the switch devices, $I_{B,SW}$ must be reduced. In Fig. 5.2, the input devices need to employ a short channel gate length since they provide gain at RF. However since the same devices provide gain at IF as well, their flicker noise contribution at baseband can be substantial. Additionally, the transconductance of input device can be boosted at the expense of power, but this is undesirable. For the mixer switching stage, a passive mixer core is realized when the bias current is reduced to zero. However, in this case, the input impedance looking into capacitors C_{M1}-C_{M4} increases at RF, thereby reducing the overall gain of the down-converter, which in turn increases the noise figure.

Table 5.1: Noise sources of g_m-reuse down-converter

Spectral location of noise sources: LO sidebands		
Noise Source	**Noise Description**	**Noise at Output**
Thermal noise of M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,1/2}} = 4KT\gamma g_{do,1/2}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,1/2}} R_Y^2 R_X^2 g_{m1/2}^2$
Thermal noise of PMOSs biasing M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,P}} = 4KT\gamma g_{do,P}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,P}} R_Y^2 R_X^2 g_{m1/2}^2$
Thermal noise of PMOSs biasing the mixer switches	$\overline{i^2_{n,M,P}} = 4KT\gamma g_{do,M,P}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,M,P}} R_Y^2 R_X^2 g_{m1/2}^2$
Thermal noise of R_X	$\overline{i^2_{n,R_X}} = 4KT\gamma R_X^{-1}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,R_X}} R_Y^2 R_X^2 g_{m1/2}^2$
Thermal noise of R_Y	$\overline{i^2_{n,R_Y}} = 4KT\gamma R_X^{-1}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,R_Y}} R_Y^2 R_X^2 g_{m1/2}^4$
Thermal noise of mixer PMOS switches	$\overline{i^2_{n,SW,wh}} = 4KT\gamma I_{B,SW}\Delta f/\pi A$	$4 \times \overline{i^2_{n,SW,wh}} R_Y^2 R_X^2 g_{m1/2}^2$
Spectral location of noise sources: Baseband / IF		
Noise Source	**Noise Description**	**Noise at Output**
Flicker noise of mixer PMOS switches	$\overline{i^2_{n,SW,1/f}} = I_{B,SW} \cdot V_n(f)\Delta f/\pi A$	$2 \times \overline{i^2_{n,SW,1/f}} R_Y^2 R_X^2 g_{m1/2}^2$
Thermal noise of M_{3a-b}	$\overline{i^2_{n,3}} = 4KT\gamma g_{do,3}\Delta f$	$2 \times \overline{i^2_{n,3}} R_Y^2 R_X^2 g_{m1/2}^2$
Flicker noise of M_{3a-b}	$\overline{i^2_{n,3,1/f}} = g_{m3}^2 k_f \Delta f/f_{IF} WLC_{ox}$	$2 \times \overline{i^2_{n,3,1/f}} R_X^2$
Thermal noise of M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,1/2}} = 4KT\gamma g_{do,1/2}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,1/2}} R_X^2$
Flicker noise of M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,1/2,1/f}} = g_{m1/2}^2 k_f \Delta f/f_{IF} WLC_{ox}$	$4 \times \overline{i^2_{n,1/2,1/f}} R_X^2$
Thermal noise of R_Y	$\overline{i^2_{n,R_Y}} = 4KT\gamma R_Y^{-1}\Delta f$	$4 \times \overline{i^2_{n,R_Y}} R_Y^2 R_X^2 g_{m1/2}^2$
Thermal noise of R_X	$\overline{i^2_{n,R_X}} = 4KT\gamma R_X^{-1}\Delta f$	$4 \times \overline{i^2_{n,R_X}} R_X^2$
Thermal noise of PMOSs biasing M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,P}} = 4KT\gamma g_{do,P}\Delta f$	$4 \times \overline{i^2_{n,P}} R_X^2$
Flicker noise of PMOSs biasing M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,P,1/f}} = g_{mP}^2 k_f \Delta f/f_{IF} WLC_{ox}$	$4 \times \overline{i^2_{n,P,1/f}} R_X^2$

5.4.2 Noise Analysis of the Down-converter with CS-reuse

The noise analysis of the topology of CS-reuse (Fig. 5.4) is similar to the case of g_m-reuse. However, two different RF and IF transconductors given by (M_{1a-b} and M_{2a-b}), and M_{4a-b} respectively are employed and thus need to be analyzed separately. The RF input devices (M_{1a-b} and M_{2a-b}), self-bias NMOS loads (M_{5a-b}) and mixer switches are major noise sources in this design as well. From the product of Eqs. (5.5) and (5.6), the in-band gain of the down-converter is expressed as $2/\pi g_{m4} g_{m1/2} R_X R_Y$. Therefore, the noise from each of the sources is scalded by $\left(2/\pi g_{m4} g_{m1/2} R_X R_Y\right)^{-2}$ when referred to the input.

The noise of input devices M_{1a-b} and M_{2a-b} at LO sidebands can be analyzed in a similar manner and the corresponding input referred noise is a function of $g_{m1/2}^{-2}$, as already derived in Eq. (5.9). On the other hand, for the IF amplification step, RF input devices operates as the conventional cascode arrangement of devices. Thus the contribution of IF band thermal and low-frequency $1/f$ noise of these devices is not critical assuming current source devices provide sufficiently large output impedance. Thus RF input devices can therefore be implemented using a minimum short channel length for maximizing their transconductance without any impact on low-frequency noise. Hence this configuration is advantageous in terms of independent optimization of noise performance compared to the case of g_m-reuse.

In the case of CS-reuse design (Fig. 5.4), current source devices M_{4a-b} are used to bias RF input devices, which are additional noise contributors. As

Table 5.2: Noise sources of CS-reuse down-converter

Spectral location of noise sources: LO sidebands		
Noise Source	**Noise Description**	**Noise at Output**
Thermal noise of M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,1/2}} = 4KT\gamma g_{do,1/2}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,1/2}} R_Y^2 R_X^2 g_{m4}^2$
Thermal noise of PMOSs biasing M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,P}} = 4KT\gamma g_{do,P}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,P}} R_Y^2 R_X^2 g_{m4}^2$
Thermal noise of PMOSs biasing the mixer switches	$\overline{i^2_{n,M,P}} = 4KT\gamma g_{do,M,P}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,M,P}} R_Y^2 R_X^2 g_{m4}^2$
Thermal noise of resistors R_X	$\overline{i^2_{n,R_X}} = 4KT\gamma R_X^{-1}\Delta f$	$4 \times 4/\pi^2 \overline{i^2_{n,R_X}} R_Y^2 R_X^2 g_{m4}^2$
Thermal noise of mixer PMOS switches	$\overline{i^2_{n,SW,wh}} = 4KT\gamma I_{B,SW}\Delta f/\pi A$	$4 \times \overline{i^2_{n,SW,wh}} R_Y^2 R_X^2 g_{m4}^2$
Spectral location of noise sources: Baseband / IF		
Noise Source	**Noise Description**	**Noise at Output**
Flicker noise of mixer PMOS switches	$\overline{i^2_{n,SW,1/f}} = I_{B,SW} \cdot V_n(f)\Delta f/\pi A$	$2 \times \overline{i^2_{n,SW,1/f}} R_Y^2 R_X^2 g_{m4}^2$
Thermal noise of R_Y	$\overline{i^2_{n,R_Y}} = 4KT\gamma R_Y^{-1}\Delta f$	$2 \times \overline{i^2_{n,R_Y}} R_Y^2 R_X^2 g_{m4}^2$
Thermal noise of M_{5a-b}	$\overline{i^2_{n,5}} = 4KT\gamma g_{do,5}\Delta f$	$2 \times \overline{i^2_{n,5}} R_Y^2 R_X^2 g_{m4}^2$
Thermal noise of M_{4a-b}	$\overline{i^2_{n,4}} = 4KT\gamma g_{do,4}\Delta f$	$2 \times \overline{i^2_{n,4}} R_X^2$
Flicker noise of M_{4a-b}	$\overline{i^2_{n,4,1/f}} = g_{m4}^2 k_f \Delta f/f_{IF} WLC_{ox}$	$2 \times \overline{i^2_{n,4,1/f}} R_X^2$
Thermal noise of R_X	$\overline{i^2_{n,R_X}} = 4KT\gamma R_X^{-1}\Delta f$	$4 \times \overline{i^2_{n,R_X}} R_X^2$
Thermal noise of PMOSs biasing M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,P}} = 4KT\gamma g_{do,P}\Delta f$	$4 \times \overline{i^2_{n,P}} R_X^2$
Flicker noise of PMOSs biasing M_{1a-b} and M_{2a-b}	$\overline{i^2_{n,P,1/f}} = g_{mP}^2 k_f \Delta f/f_{IF} WLC_{ox}$	$4 \times \overline{i^2_{n,P,1/f}} R_X^2$

can be seen in Fig. 5.4, the input stage of the design consist of a differential-pair amplifier. Thus the drain thermal noise of transistor M_{4a-b} around LO sidebands is ideally cancelled at the mixer input in a differential manner. Only their low frequency thermal and $1/f$ noise appears at the outputs. From Eq. (5.6), the input referred noise originating from the mixer is given by

$$\overline{v_{ni,5,1/f}^2} = 2 \times \pi^2 \cdot \overline{i_{n,5,1/f}^2}/(4 \cdot g_{m1/2}^2) \tag{5.16}$$

$$\overline{v_{ni,SW,wh}^2} = 4 \times \pi^2 \cdot \overline{i_{n,SW,wh}^2}/(4 \cdot g_{m1/2}^2) \tag{5.17}$$

$$\overline{v_{ni,SW,1/f}^2} = 2 \times \pi^2 \cdot \overline{i_{n,SW,1/f}^2}/(4 \cdot g_{m1/2}^2) \tag{5.18}$$

In the design shown in Fig. 5.4, the current source devices M_{4a-b} and mixer loads M_{5a-b} can use longer channel lengths than those used in the RF devices M_{1a-b} and M_{2a-b}, thereby lowering their flicker noise contribution. This is a key advantage of this topology. On the other hand, this design has a higher minimum headroom requirement than that of the device shown in Fig. 5.2.

Fig. 5.5 shows the total output noise spectrum measured from the implementation of the device shown in Fig. 5.4. The output noise spectrum over the frequency has a staircase shape, as also shown in the inset in the figure. The output noise level within the pass-band is determined by the product of the combined thermal noise around the LO sidebands and the noise gain G_N^2, where $G_N = 2/\pi g_{m4} R_X R_Y$. This noise is filtered by the built-in low-pass response of the stage. Outside of the pass band, the noise contribution rolls off. For example the noise contributed by the switching core decreases due

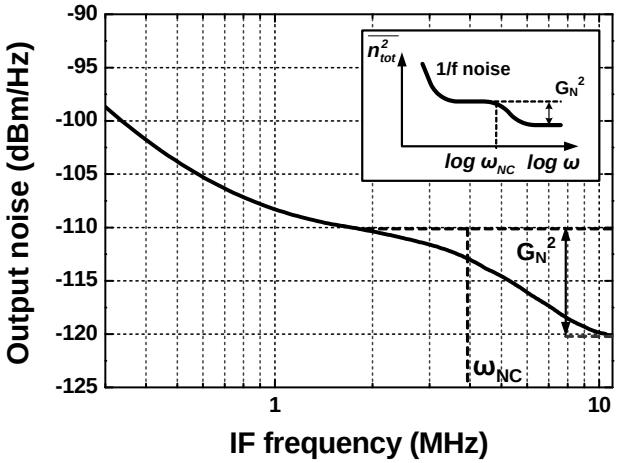


Figure 5.5: Total output noise spectrum of the receiver down-converter with CS-reuse

to the pole at the mixer load. The noise bandwidth ω_{NC} is set by the corner frequency of the low pass response of the design. Similar output noise spectrum can be observed from the output of g_m-reuse design. In this case, the third-order low pass response provides a sharper roll-off characteristic.

5.5 Distortion Performance of Receivers

5.5.1 Second-order Nonlinearity

The use of differential input pairs M_{1a-b} and M_{2a-b} instead of single devices affords an additional advantage with regard to the second-order distortion. As shown in Fig. 4.8 and described in Eq. (4.5), the beat product of a

strong close-in interferer with the IF signal arising from second-order nonlinearity can appear within the signal band and corrupt the incoming RF signal. The beat product of the interferer with the RF signal can also overlap with the down-converted IF signal. However, this effect is not critical as compared to the second-order distortion produced by the interferer and the IF signal because the signal power level of IF is significantly higher than that of RF.

The input devices M_{1a-b} and M_{2a-b} amplify the interferer in-phase similar to the RF in Figs. 5.2 and 5.4. For consistency, consider an equivalent interferer at ω_{INT} with phase "θ" and an IF signal at ω_{IF} with amplitudes "A_{INT}" and "A_{IF}", respectively, which are used in Eq.(4.5). The second-order distortion at the inputs to the mixer (nodes V_X and V_Y in Figs. 5.2 and 5.4) is proportional to

$$\begin{aligned}&\big(A_{INT}\cdot\cos\left(\omega_{INT}t+\theta\right)+A_{IF}\cdot\cos\left(\omega_{IF}t\right)\big)^2\\&\quad+\big(A_{INT}\cdot\cos\left(\omega_{INT}t+\theta\right)-A_{IF}\cdot\cos\left(\omega_{IF}t\right)\big)^2\end{aligned}\tag{5.19}$$

The interferer appears in-phase, while the IF signal is out-of-phase at the inputs of the devices comprising the input pair. By expanding Eq. (5.19), we observe that the beat-frequency terms arising from the second-order intermodulation of IF and RF signals are canceled at the input to the switching pairs of the mixer. Other square terms such as $\cos^2\left(\omega_{INT}t+\theta\right)$ and $\cos^2\left(\omega_{IF}t\right)$ are also rejected at the mixer input since these appear as common-mode terms. Therefore, if the input stages are perfectly matched, very high IIP2 is achieved.

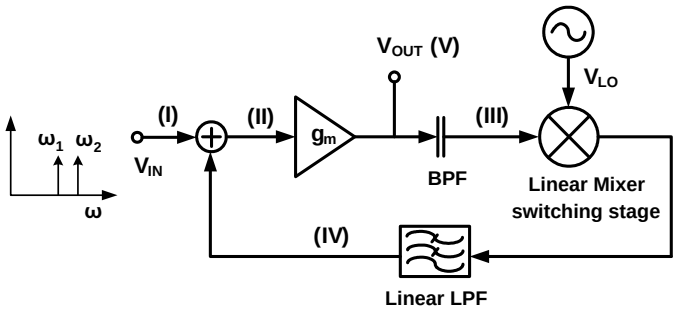


Figure 5.6: Simplified nonlinear block diagram of g_m-reuse down-converter

5.5.2 Third-order Nonlinearity

The mechanisms responsible for the third-order intermodulation of the down-converter with g_m-reuse and CS-reuse are discussed separately below. Since the IF is reapplied to the input in both cases, nonlinearity in the input stage produces beat products of the IF and RF signals. Various nonlinear IM mechanisms are identified below in the g_m-reuse design, which also occur in the CS-reuse design. A detailed analysis of the nonlinearity is presented for the CS-reuse design (Fig. 5.4), which exhibits a cancellation of third-order IM products, due to the contribution of the beat product of the second-order nonlinearity of the CS device with the fundamental term in the input differential pair.

Let us consider a conceptual view of the g_m-reuse receiver, as shown in Fig. 5.6. We assume that the mixer switches and filters are perfectly linear and the input stage is the only source of nonlinearity. Consider a two-tone signal at the input with amplitude "A," applied at the input i.e., $v_{\omega_1,\omega_2} =$

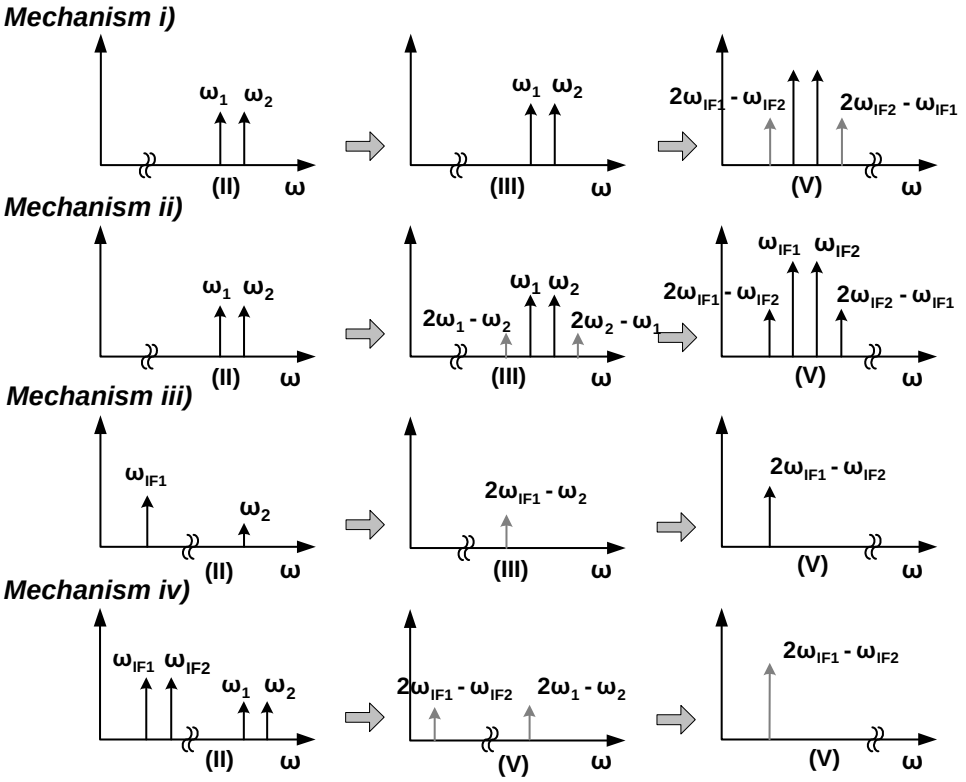


Figure 5.7: Third-order intermodulation mechanisms of g_m-reuse down-converter

$A \cdot (\cos\omega_1 t + \cos\omega_2 t)$. The nonlinearity of the the down-converter generates IM3 products at $2\omega_{IF1} - \omega_{IF2}$, and $2\omega_{IF2} - \omega_{IF1}$, where $\omega_{IF} = \omega_1 - \omega_{LO}$ and $\omega_{IF2} = \omega_2 - \omega_{LO}$. These terms can be generated through several mechanisms that are shown in Fig. 5.7 and described below.

(i) The input transconductance stage amplifies two-tone signals at ω_1 and ω_2. The tones are downconverted to ω_{IF1} and ω_{IF2}, respectively. The third-order distortion of the input-stage generates IM3 products at $2\omega_{IF1} - \omega_{IF2}$ and $2\omega_{IF2} - \omega_{IF1}$ from down-converted signals at ω_{IF1} and ω_{IF2}.

(ii) IM3 products at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ for the applied two-tone signal with tones at ω_1 and ω_2 are generated by the input stage and further amplified in the subsequent baseband amplification step.

(iii) The incoming signal ω_2 and down-converted ω_{IF1} create a third-order distortion term at $2\omega_{IF1} - \omega_2$. This is a high frequency component that is down-converted by the mixer to produce an IM3 product at $2\omega_{IF1} - \omega_{IF2}$. A similar interaction is observed between ω_1 and down-converted ω_{IF2}.

(iv) Since both RF and IF signals at ω_1, ω_2, ω_{IF1} and ω_{IF2} simultaneously appear at the input of the g_m stage, the triple-beat terms of (ω_1, ω_2 and $\omega_{IF1,2}$), and ($\omega_{1,2}$, ω_{IF1} and ω_{IF2}), contribute IM3 products at the output.

Among the above mechanisms, (i) and (ii) exist in the conventional cascaded down-converter, as already described in Fig. 2.6b. However, (iii) and

(iv) are additional distortion product terms that appear in this topology due to the interaction of IF and RF at the input.

The nonlinearity of the input common source MOSFETs of Fig. 5.2 can be expressed as a small-signal power-series, $i_{ds} = b_1 v_{gs} + b_2 v_{gs}^2 + b_3 v_{gs}^3 + \cdots$, where v_{gs} is the small-signal gate-to-source voltage and i_{ds} is the small-signal drain current. The small-signal voltage v_{gs} includes IF and RF signals in the implementation. The linear term b_1 is the transconductance (g_m) of the input device.

Assuming ideal square-wave switching, IM3 products of g_m-reuse design given by mechanism (i) and (ii) are

$$IM3_{g_m,(i)} = \frac{6}{\pi^3} \cdot R_X R_Y^3 b_1^3 b_3 A^3 \tag{5.20}$$

$$IM3_{g_m,(ii)} = \frac{3}{2\pi} R_X R_Y b_1 b_3 A^3 \tag{5.21}$$

, respectively. In the case of mechanism (iii), the third-order intermodulation of v_{ω_2}=$A\cos\omega_2 t$ and $v_{\omega_{IF1}}$=$(2/\pi)R_Y b_1 A\cos\omega_{IF1}$ creates a spectral component at $2\omega_{IF1} - \omega_2$ with the amplitude of $(3/\pi^2 R_Y^2 b_1^2 b_3 A_3)$. Through the additional down-conversion step, third-order distortion of mechanism (iii) is given by

$$IM3_{g_m,(iii)} = \frac{6}{\pi^3} R_X R_Y^3 b_1^3 b_3 A^3 \tag{5.22}$$

Based on above-mentioned mechanism (iv), two triple-beat product terms of (ω_1, ω_2 and ω_{IF1}), and (ω_1, ω_{IF1} and ω_{IF2}) contribute IM3 products at $2\omega_{IF1} - \omega_{IF2}$ and $2\omega_1 - \omega_2$, respectively. Like mechanism (iii), the second term

undergoes additional down-conversion. Thus IM3 product given by mechanism (iv) is

$$IM3_{g_m,(iv)} = \frac{3}{\pi} R_X R_Y b_1 b_3 A^3 + \frac{12}{\pi^3} R_X R_Y^3 b_1^3 b_3 A^3 \tag{5.23}$$

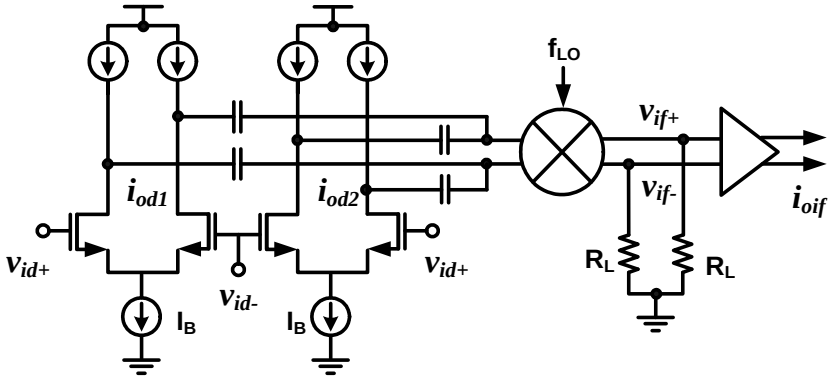
From Eq. (5.20)-(5.23), the combined third-order distortion product of the g_m-reuse down-converter can be shown to be given by

$$IM3_{g_m-reuse} = \frac{9}{2\pi} R_X R_Y b_1 b_3 \left(1 + \frac{16}{3\pi^2} \cdot b_1^2 R_Y^2\right) \cdot A^3 \tag{5.24}$$

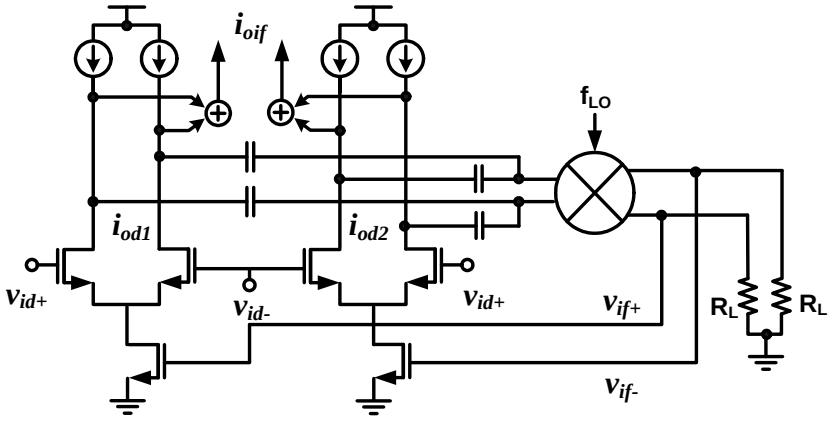
The above equation assumes broadband nonlinearity. The low-pass response at baseband helps in attenuating out-of-band interferers at IF before they are reapplied to the input stage. In particular, the IM3 component caused by mechanism (i) is reduced due to the filtering of IF at the mixer output before it is applied to the input devices (see Eq. (5.3)). A possible approach to improve linearity is to use frequency-selective degeneration in the input transistors that linearizes the design at baseband.

Similar IM3 products are present in the down-converter with CS-reuse, as shown in Fig. 5.4. However, a very advantageous feature of the design is that IM3 products can be mitigated significantly through the cancellation of nonlinearity. A detailed analysis of the CS-reuse stage is presented below assuming square-law devices in the input differential pairs. The analysis is not exact since short-channel devices do not exhibit ideal square-law behavior, and is primarily meant to illustrate the cancellation principle.

We first consider a cascade of an RF differential amplifier, a mixer and an IF amplifier, as shown in Fig. 5.8a. This can be recognized as the "opened"



(a)



(b)

Figure 5.8: (a) Conventional cascaded down-converter comprising different pair, mixer, and baseband amplifier stages and (b) simplified feedback-based down-converter with CS-reuse

version of the design shown in Fig. 5.4. As before, the mixer switching core and filters are considered to be ideally linear. The output current of the differential pairs for square-law devices is given by [27]

$$i_d = i_{d1} - i_{d2} = \alpha \cdot v_{id} \cdot \sqrt{I_B - \gamma \cdot v_{id}^2} \tag{5.25}$$

The factors α and γ are given by $\sqrt{k_n'(W/L)}$ and $k_n'(W/L)/4$, respectively. I_B is the tail current of the differential pairs. In the design shown in Fig. 5.8a, a total RF output current $i_{od} = 2 \cdot \alpha \cdot v_{id} \cdot \sqrt{I_B - \gamma \cdot v_{id}^2}$ thus flows into the mixer and is down-converted to IF. The differential voltage at the mixer output is defined as $2v_{if} = v_{if+} - v_{if-} = G \cdot i_{od}$, where G is the product of the current conversion gain and load resistor R_L. Assuming ideal square-wave switching at the mixer, G is given by $(2/\pi)R_L$. If we express the nonlinearity of the subsequent IF amplifier as a power series $i_{oif} = \beta_1 v_{if} + \beta_2 v_{if}^2 + \beta_3 v_{if}^3 + \cdots$, the overall nonlinearity at the output of the IF amplifier is given by

$$i_{oif} = 2\beta_1 \Big(G\alpha \cdot v_{id} \cdot \sqrt{I_B - \gamma \cdot v_{id}^2} \Big) + 2\beta_3 \Big(G\alpha \cdot v_{id} \cdot \sqrt{I_B - \gamma \cdot v_{id}^2} \Big)^3 \tag{5.26}$$

By employing a Taylor-series expansion, Eq. (5.26) can be rewritten as

$$i_{oif} = \big(2\beta_1 G\alpha \sqrt{I_B} \big) \cdot v_{id} + \left(2\beta_3 G^3 \alpha^3 I_B^{3/2} - \frac{\beta_1 G \alpha \gamma}{\sqrt{I_B}} \right) \cdot v_{id}^3 + \cdots \tag{5.27}$$

The dominant nonlinearity is contributed by the third-order term β_3 since the signal at the device input is amplified by the conversion gain of the mixer.

In the case of the simplified feedback-based down-converter with CS-reuse shown in Fig. 5.8b, the down-converted signals are applied to the gates

of the tail current source devices of the input differential amplifiers for IF amplification. Due to this feedback connection, Eq. (5.25) needs to be modified to include the current variation caused by v_{if}. Therefore, for this case,

$$i_{od1} = \alpha \cdot v_{id} \cdot \sqrt{I_B + f\left(v_{if}\right) - \gamma \cdot v_{id}^2} \tag{5.28}$$

$$i_{od2} = \alpha \cdot v_{id} \cdot \sqrt{I_B + f\left(-v_{if}\right) - \gamma \cdot v_{id}^2} \tag{5.29}$$

where, $f\left(v_{if}\right) = \beta_1 v_{if} + \beta_2 v_{if}^2 + \beta_3 v_{if}^3 + \cdots$ models the nonlinear small-signal dependence of the tail current on the IF voltage at the mixer output. For proper comparison, the CS devices are assumed to have identical nonlinear polynomial coefficients compared to the IF amplifier shown in Fig. 5.8a. The differential IF voltage v_{if} in Eqs. (5.28) and (5.28) must also satisfy the equation $2v_{if} = G \cdot (i_{od1} + i_{od2})$. We thus have

$$2v_{if} = G\alpha v_{id}\sqrt{I_B}\left[\sqrt{1 + \frac{f\left(v_{if}\right) - \gamma v_{id}^2}{I_B}} + \sqrt{1 + \frac{f\left(-v_{if}\right) - \gamma v_{id}^2}{I_B}}\right] \tag{5.30}$$

By applying a Taylor expansion, Eq. (5.30) can be expressed as

$$2v_{if} = G\alpha v_{id}\sqrt{I_B}\left[2 + \left(\frac{\beta_2}{I_B} - \frac{\beta_1^2}{4I_B^2}\right)v_{if}^2 + \frac{\gamma\beta_2 v_{if}^2 - 2\gamma}{2I_B}v_{id}^2 + \cdots\right] \tag{5.31}$$

By employing the approximation $v_{if} = c_1 v_{id} + c_3 v_{id}^3$ and solving for c_1 and c_3, we obtain

$$c_1 = G\alpha\sqrt{I_B} \tag{5.32}$$

$$c_3 = \frac{G^3\alpha^3\sqrt{I_B}}{2}\left(\beta_2 - \frac{\beta_1^2}{4I_B}\right) - \frac{G\alpha\gamma}{2\sqrt{I_B}} \tag{5.33}$$

Since the differential IF output current is given by $i_{oif} = 2\beta_1 v_{if} + 2\beta_3 v_{if}^3$, we have

$$\begin{aligned} i_{oif} &= \left(2\beta_1 G\alpha\sqrt{I_B}\right)\cdot v_{id} + \left[G^3\alpha^3\beta_1\sqrt{I_B}\left(\beta_2 - \frac{\beta_1^2}{4I_B}\right)\right. \\ &\quad \left. +2\beta_3 G^3\alpha^3 I_B^{3/2} - \frac{\beta_1 G\alpha\gamma}{\sqrt{I_B}}\right]\cdot v_{id}^3 + \cdots \end{aligned} \tag{5.34}$$

By comparing Eq. (5.27) with Eq. (5.34), it can be observed that an additional term $G^3\alpha^3\beta_1\sqrt{I_B}\left(\beta_2 - \beta_1^2/4I_B\right)$ contributes to the third-order nonlinear distortion. Typically, in MOSFETs biased in saturation, β_2 is a positive quantity and β_3 is negative [17]. Therefore, the overall third-order nonlinear characteristics can be adjusted by controlling the second-order nonlinear coefficient β_2. When $\beta_2 = \beta_1^2/4I_B$, the IM3 product of the feedback-based down-converter becomes equal to that of its cascaded counterpart in Fig. 5.8a. By setting β_2 to be considerably greater than $\beta_1^2/4I_B$, its third-order nonlinearity term can be further reduced. The physical interpretation for the above is that the second-order nonlinearity of the current source devices can be used to improve their third-order nonlinearity due to the interaction of the linear and second-order terms in the input differential pair.

In addition to the inherent second-order nonlinearity of the current source devices, an additional second-order term can also be introduced into the tail current source by means of a dedicated circuit with a variable output if required. An approach is shown Fig. 5.9, that comprises two common-source devices fed by the differential outputs of the mixer, with their drains tied

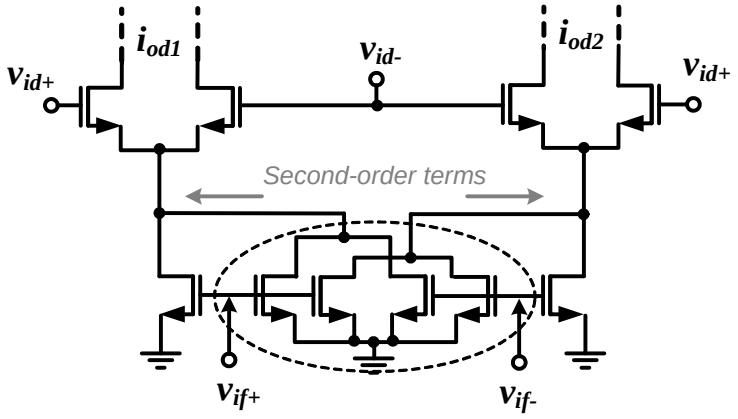


Figure 5.9: Simple design modification using two common-source amplifiers

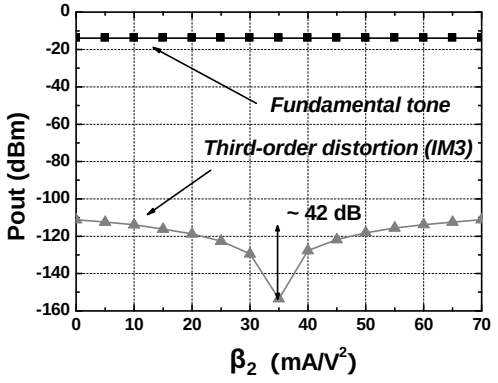
together. The net output current would primarily consist of the second-order term, which could be fed back into the tail current of the input differential pairs. By controlling the amount of second-order current that is fed back, a controllable second-order term can be synthesized.

The IF does not flow into the mixer. Thus the nonlinearity of the mixer is not degraded by the presence of large IF signals, unlike the input stage. The mixer core however does contribute IM3 in response to the RF inputs. Eq. (5.34) does not consider this non-linearity. Further, this analysis assumes broadband nonlinear mechanisms. Therefore, frequency-dependent phase shifts generated by various nonlinear terms are not considered. These will limit the degree of cancellation that is achievable. However, if the base-band LPF and HPF corner frequencies are significantly higher than the highest IF of interest and sufficiently lower than the RF, the impact of the phase shift is minimized.

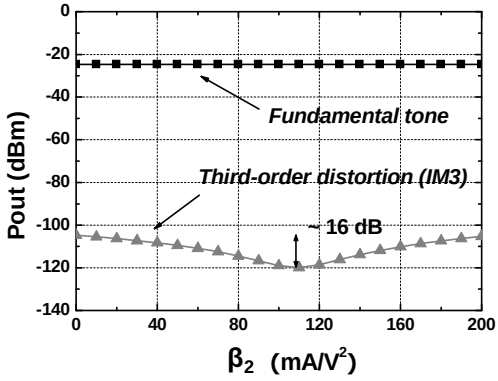
The above derivation was verified in simulation using Cadence SpectreRF in a UMC 0.13-μm RF CMOS process. A two-tone linearity test was performed with a nominal supply voltage of 1.2 V. IM3 products at 2 MHz were evaluated using two tones of 905 and 908 MHz and an LO signal of 900 MHz.

In order to verify the above derivation, we first consider the receiver down-converter with an ideal input stage and mixer, modeled as a polynomial nonlinear transconductor and a linear two-input multiplier, respectively. The amount of injection of the second-order term (β_2) is suitably controlled by employing an ideal polynomial nonlinear model. Fig. 5.10a shows the shows the simulated first- and third-order terms at the output achieved by sweeping β_2 within the expected range obtained from manual calculations. As observed in Fig. 5.10a, the IM3 is minimized for $\beta_2 = 35$ mA/V^2. The fundamental tone on the other hand, is observed to be almost independent of β_2. A nearly ideal attenuation of approximately 42 dB was observed in the simulation of the IM3 products.

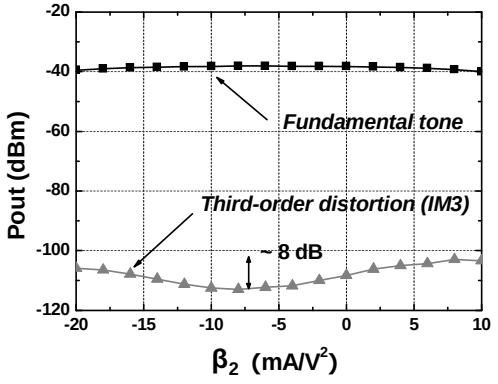
A similar linearity improvement was also verified in other two different models: the receiver down-converter with an ideal mixer and the receiver down-converter with a folded Gilbert cell switching mixer (Fig. 5.10b and c). The differential input pair, the tail currents and Gilbert cell switching mixer use physically modeled 0.13-μm CMOS devices. For an equivalent comparison, the second amplification stage of both the designs provides identical nonlinear characteristics. Fig. 5.10b and c shows the simulated attenuation of third-



(a)



(b)



(c)

Figure 5.10: First- and third-order terms versus a second-order nonlinear coefficient of a down-converter (a) with an ideal polynomial input stage and an ideal switching core, (b) with an ideal switching core and (c) with a folded Gilbert cell switching core

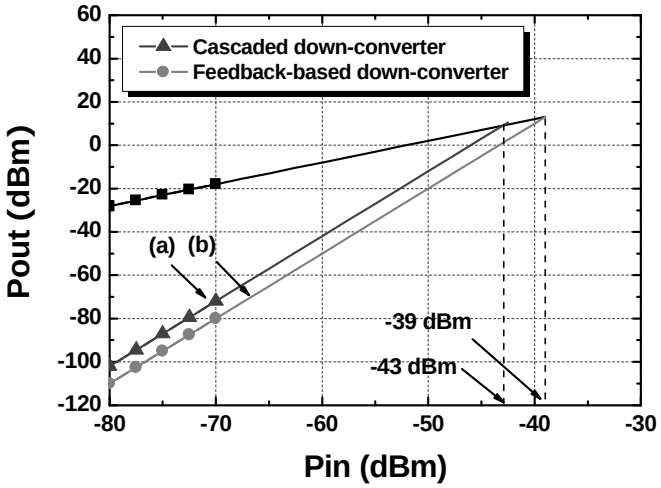


Figure 5.11: Simulated IIP3 for (a) cascaded down-converter and (b) feedback-based down-converter

order distortion term for the case of an ideal and real mixer were 16 dB and 8 dB, respectively.

The simulation result of feedback-based down-converter was compared to that of the cascaded design (Fig. 5.8a). For consistency, both the designs utilized identical nonlinear characteristics of the second amplification stage and overall conversion gain. Fig. 5.11 shows the simulated first- and third-order terms of this design by sweeping the second-order term (β_2) in the same manner. As observed in Fig. 5.11, the obtained IIP3s of the cascaded and feedback-based down-converters were -39 dBm and -43 dBm for the same simulation condition, respectively. Due to the cancellation mechanism pro-

vided by the intrinsic second-order nonlinearity of the tail current sources, the IIP3 is improved by approximately 4 dB. As mentioned previously, the third-order intermodulation distortion attributed to mixer switching devices limits the improvement However this improvement is very beneficial. Future research can address improvements in the non-linearity of the switching devices.

Chapter 6

Experimental Results

In chapter 5, the complete design of receiver down-converters with g_m- and CS-reuse has been presented along with the detailed analyses of receiver characteristics such as gain, filtering response, noise, and linearity. In this chapter, experimental results for both designs are presented and analyzed.

6.1 Measurement Setup

Both down-converters were fabricated on the same die using UMC 0.13-μm CMOS technology. All signal and bias pads were electrostatic discharge (ESD) protected using reverse-biased diodes. The core active chip area for each design, excluding bond pads was 0.6 mm$\times$0.16 mm, which is less than 0.1 mm^2. The designs did not employ integrated on-chip spiral inductors. The ICs were packaged in a 48-pin ceramic quad flat pack (CQFP48). All measurements were performed using an assembled printed circuit board (PCB), on which the package was bonded with all required external surface-mounted components as shown in Fig. 6.1. Flame-resistant 4 (FR-4) material was used as the PCB substrate. RF and LO signals were applied externally using commercial off-chip broadband passive baluns for single-to-differential conversion.

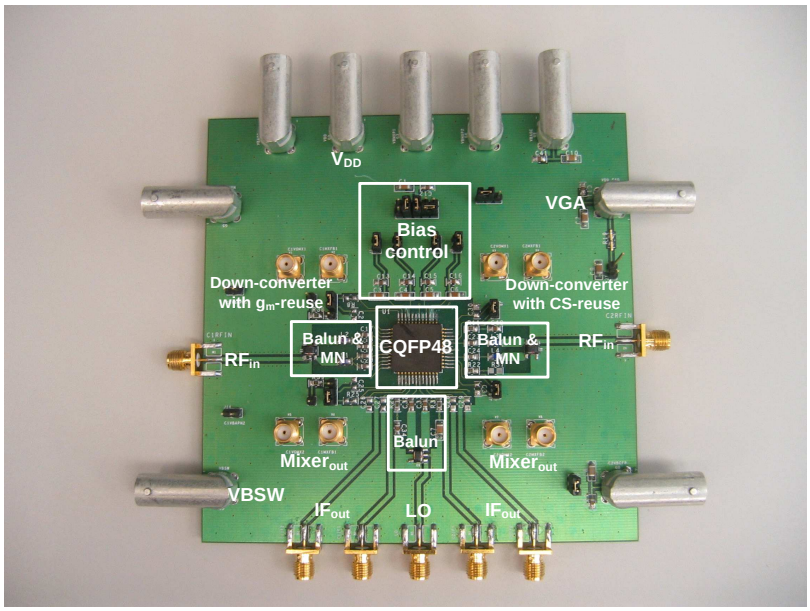


Figure 6.1: Assembled printed circuit board

A combined balun insertion loss and input PCB signal trace loss of 4.2 dB was measured at the desired frequencies in a replica measurement set up and it was used for compensating the measured results. For matching networks (MNs), off-chip inductors and capacitors were properly selected to maintain the input matching condition at the band of interest with S11 of -8 dB at 900 MHz. A coplanar waveguide with a ground (CPWG) structure was used to implement differential 50-Ω microstrip lines for the input and output signal traces. Both designs were measured using the same board with only one down-converter enabled during a measurement. The baseband output signals were measured by using PCB-mounted external OP-AMPs that were configured as unity-gain differential-to-single converters. Within the band of interest, the noise contri-

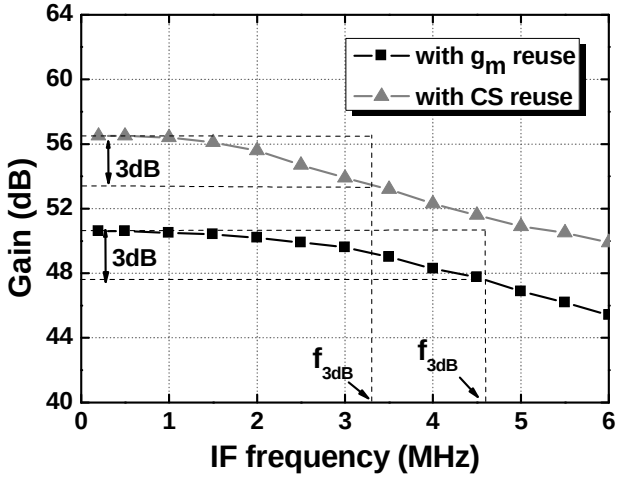


Figure 6.2: Measured gain versus IF frequency

bution from the OP-AMPs was negligible. The results are characterized by an Agilent Spectrum analyzer (Agilent E4448A).

6.2 Measurement Results

The down-converters with g_m- and CS- reuse have a current dissipation of 2.9 mA and 2.1 mA, respectively, with a nominal supply voltage of 1.2 V. In both cases, only 0.7 mA is used in the mixer switching stage and majority of the current is consumed in the transconductor stages. Fig. 6.2 shows the frequency response of the peak gain measured by sweeping the RF input frequency at around 900 MHz. The measured peak gains at an IF frequency of 2 MHz are observed to be nearly 50 dB and 56 dB for the g_m- and CS-reuse designs,

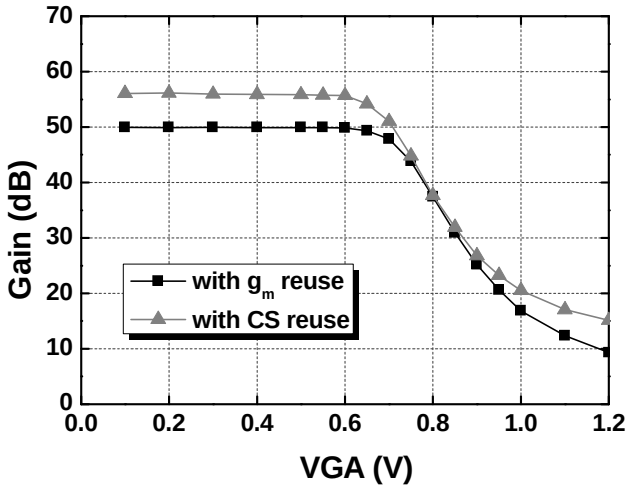


Figure 6.3: Variable gain capability

respectively. The 3-dB corner frequency of the gain response is around 3∼5 MHz, which is controlled by the values of the capacitors and resistors at the output of the mixer and down-converter. As shown in Fig. 6.3, the overall gain can be varied in both designs by over 40 dB by varying the control voltage of the gate of M_{AGC} from 0.6 to 1.2 V (Figs. 5.2 and 5.4).

Two different methods for noise figure measurement were employed and compared: direct noise floor measurement, that utilized the equation $NF = P_{N,OUT} - (-174(dBm/Hz) + 20\log_{10}(BW) + Gain)$, and the Y factor method using a noise source such as HP346A/B. Both methods provide almost identical noise figure results. Fig. 6.4 shows the single side band (SSB) noise figure as a function of the IF. As observed in Fig. 6.4, the g_m-reuse down-converter

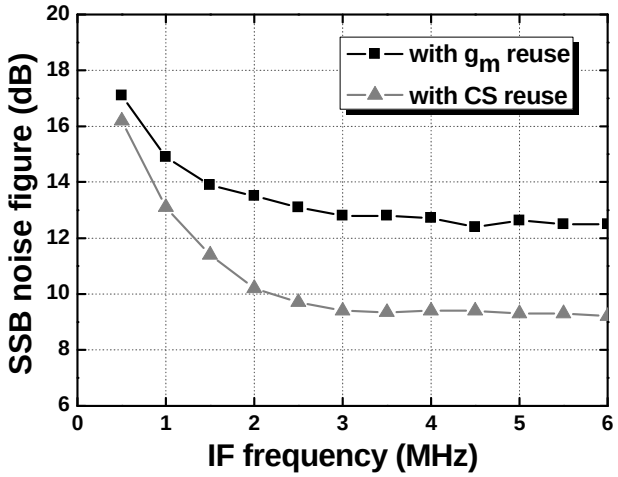
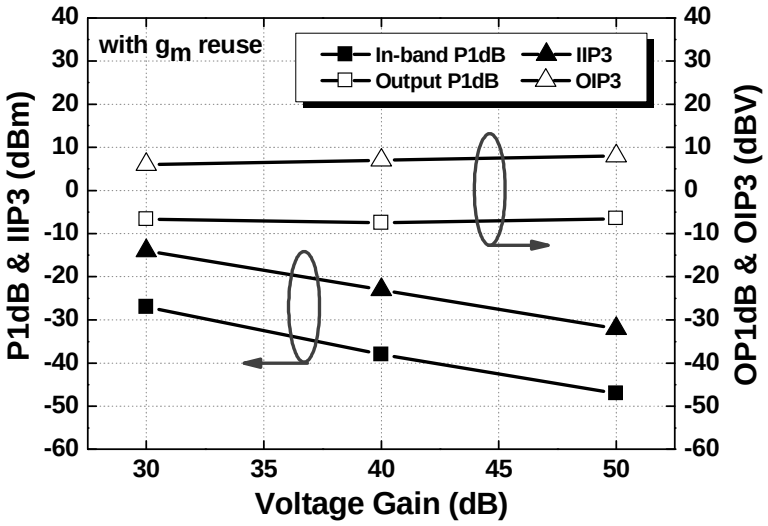
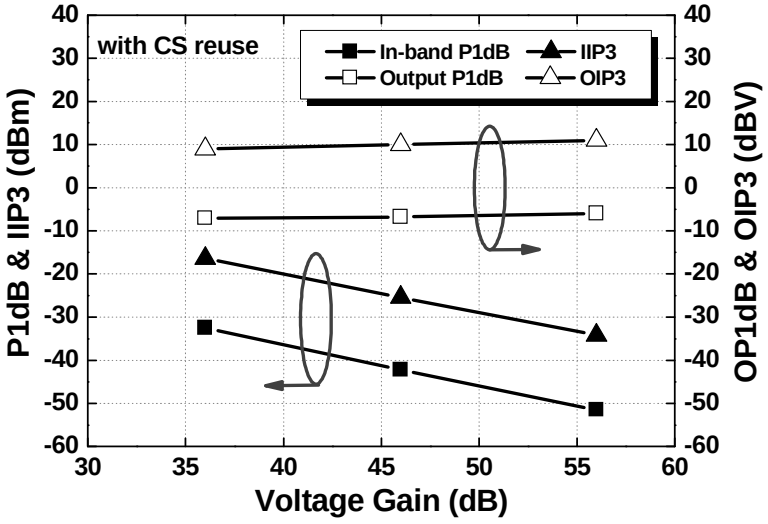


Figure 6.4: Measured SSB noise figure versus IF frequency

exhibits a noise figure of 13.5 dB SSB or 10.5 dB DSB at an IF frequency of 2 MHz, and 12.7 dB SSBNF (9.7 dB DSBNF) at an IF frequency of 4 MHz. The measured SSB noise figure for the CS-reuse design is 10.2 dB (7.2 dB DSBNF) at an IF frequency of 2 MHz and 9.4 dB at 4 MHz (6.4 dB DSBNF). As described in chapter 5.4, the primary noise contributors are the thermal noise of RF input devices (M_{1a-b} and M_{2a-b}), and the $1/f$ noise sources of the mixer switching devices and active mixer loads (M_{3a-b}) of the g_m-reuse design, and current sources (M_{4a-b} and M_{5a-b}) of the CS-reuse design. In particular, $1/f$ noise is further amplified at baseband by the input transconductors and it therefore severely degrades the overall noise figure especially at low frequencies. In this design, the tail current source devices used a maximum channel length



(a)



(b)

Figure 6.5: Linearity performance with (a) g_m-reuse and (b) CS-reuse for three different gain settings (f1 = 905 MHz and f2 = 908 MHz)

of 0.36-μm, due to certain device sizing restrictions. However, a significantly longer channel length can be used in the tail current devices, which would greatly decrease the $1/f$ noise contribution.

The nonlinearity of down-converters is investigated at three different gain settings: peak gain, 10 dB gain, and 20 dB gain attenuation. The down-converter gain is of the order of 50 dB for the g_m-reuse design. The in-band 1-dB compression point (P1dB) for three gain conditions (30, 40, and 50 dB) measured at 2 MHz is -27.2, -38, and -47 dBm, respectively (Fig. 6.5a). As shown in Fig. 6.5a, the corresponding compression point defined as $P1dB(dBm) - 10 + CG - 1$ is nearly identical (-7 dBV$_p$) for three small-signal gain settings and ranges from 0.4$\sim$0.45 V. This indicates that the in-band compression performance is limited at the output of the down-converter. This is typical of high-gain receivers. A similar output compression voltage is observed for open-loop mixer operation without baseband reuse.

The measured input P1dB of the down-converter with CS-reuse is -32.5, -42.2, and -51.5 dBm for small-signal gain settings of 36, 46, and 56 dB, respectively (Fig. 6.5b). This corresponds to an output P1dB of -6 dBV$_p$ or approximately 0.5 V. In addition, Table 6.1 also shows the out-of-band P1dBs with 5 and 10 MHz offset interferers for the two implemented down-converters. Obtained P1dBs were improved compared to in-band P1dBs, depending on the frequency response of the gain of the designs; however, the corresponding OIP3s were approximately identical.

Fig. 6.5 also shows the input and output IP3s of receiver down-converters

Table 6.1: Linearity Performance with three different gain settings

Down-converter with g_m reuse			
Gain settings	**Peak gain**	**10 dB gain attenuation**	**20 dB gain attenuation**
P1dB / OP1dB			
In-band	-47 / -6.5	-38 / -7.5	-27.2 / -6.7
5 MHz offset f_{INT}	-45 / -7.7	-35.5 / -7.3	-26.5 / -8.3
10 MHz offset f_{INT}	-44 / -8.3	-34.9 / -8.7	-26 / -9.8
IIP3 / OIP3			
with 903 MHz, 904 MHz	-35.4 / 4.8	-26.1 / 4.1	-17.1 / 3.1
with 905 MHz, 908 MHz	-32.1 / 8.1	-22.7 / 7.5	-14.3 / 5.8
with 907 MHz, 912 MHz	-29.3 / 10.9	-20.2 / 10	-11.7 / 8.5
Down-converter with CS reuse			
Gain settings	**Peak gain**	**10 dB gain attenuation**	**20 dB gain attenuation**
P1dB / OP1dB			
In-band	-51.5 / -6	-42.2 / -6.8	-32.5 / -7.1
5 MHz offset f_{INT}	-46 / -6.7	-36.9 / -7.6	-28 / -8.7
10 MHz offset f_{INT}	-42 / -7.5	-32.5 / -8.4	-23.5 / -9
IIP3 / OIP3			
with 903 MHz, 904 MHz	-38.7 / 6.9	-29.9 / 5.7	-20.9 / 4.7
with 905 MHz, 908 MHz	-34.3 / 11.3	-25.4 / 10.2	-16.4 / 9.2
with 907 MHz, 912 MHz	-30.5 / 15.1	-21.8 / 13.8	-12.9 / 12.7

Table 6.2: Performance comparison with other reported mixers and receiver front-ends

References	[40]	[57]	[37]	[58]	**This work**	**This work**
Frequency (MHz)	2400	900	900	900	**900**	**900**
Vdd (V)	1.8	0.9	0.5	1.2	**1.2**	**1.2**
Design	Folded Mixer	Mixer	Front-end LNA+ Mixer	Front-end LNA+ Mixer	**Merged Mixer+ Baseband Amplifier**	**Merged Mixer+ Baseband Amplifier**
NF(dB)	12.9(SSB)	13.5(SSB)	9(DSB)	8.6(DSB)	**12.7(SSB)**	**10.2(SSB)**
Gain(dB)	15.7	2	12	29	**50**	**56**
OP1dB(dBV)	-	-16	-21	-	**-7**	**-6**
OIP3(dBV)	6.7	-4.5	-12	1.8	**8**	**11**
Current(mA)	4.5	5.2	6.4	1.8	**2.9**	**2.1**
FOM(dB) [40]	11.4	7.5	7	15.9	**15.1**	**21.8**
Technology	0.18-μm CMOS	0.35-μm CMOS	0.18-μm CMOS	0.35-μm CMOS	**0.13-μm CMOS**	**0.13-μm CMOS**
Core Area (mm^2)	0.032	0.05	$\sim$0.33	$4.32^{(1)}$	$<$ **0.1**	$<$ **0.1**

(1) : Total die area

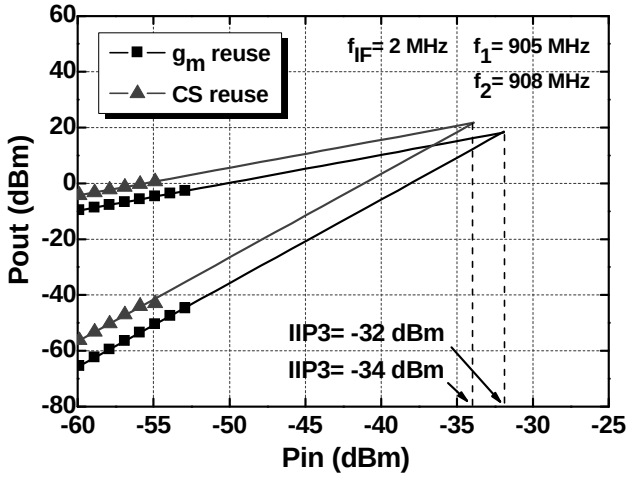


Figure 6.6: Measured IP3s for peak gain ($f_1 = 905$ MHz and $f_2 = 908$ MHz)

with g_m- and CS-reuse for three different gain conditions with two tones at 905 MHz and 908 MHz. IM3 products are measured at an IF frequency of 2 MHz. A two-tone linearity test is performed with sufficiently small RF inputs to ensure that devices are not saturated. The IIP3s of down-converters with g_m- and CS-reuse are -32 and -34 dBm for the peak gain (Fig. 6.6), corresponding to nearly identical OIP3s of 8 and 11 dBV_p, respectively (Fig. 6.5). The IIP3s and OIP3s of both designs are also measured with various two-tone sets and gain conditions and they are summarized in Table 6.1. As observed in Figs. 6.5 and 6.6 and Table 6.1, the obtained IIP3s increase as the gain decreases nearly dB-per-dB again indicating that the primary limitation to linearity is at the output.

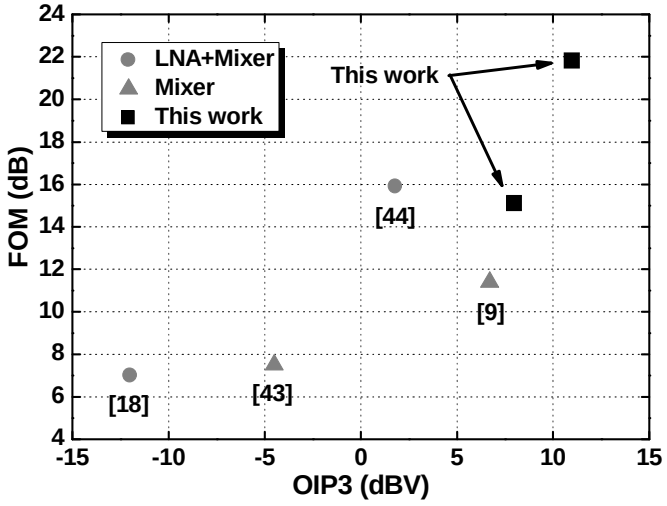


Figure 6.7: Comparison of reported OIP3s versus FOMs

The measured performance of the two reported down-converters and other reported implementations are compared in Table 6.2. The figure of merit (FOM) [40] used to compare the designs is defined as

$$FOM\,(dB) = 10 \cdot \log\left(\frac{10^{OIP3(dBV)/20}}{10^{NF(dB)/10} \cdot P_{DC}\,(mW)}\right) \tag{6.1}$$

where P_{DC} is the total power consumption. The FOM of receivers with g_m- and CS-reuse are 15.1 and 21.8 dB, respectively. In order to determine this FOM, IIP3 is determined using two tones at 5 and 8 MHz. Since the 3-dB bandwidth of the designs is approximately 4 MHz, the two tones could be considered to be adjacent and next-to-adjacent channel interferers. Using IIP3 with both tones generating an in-band IF, the respective FOM measures are 11 dB and 15 dB.

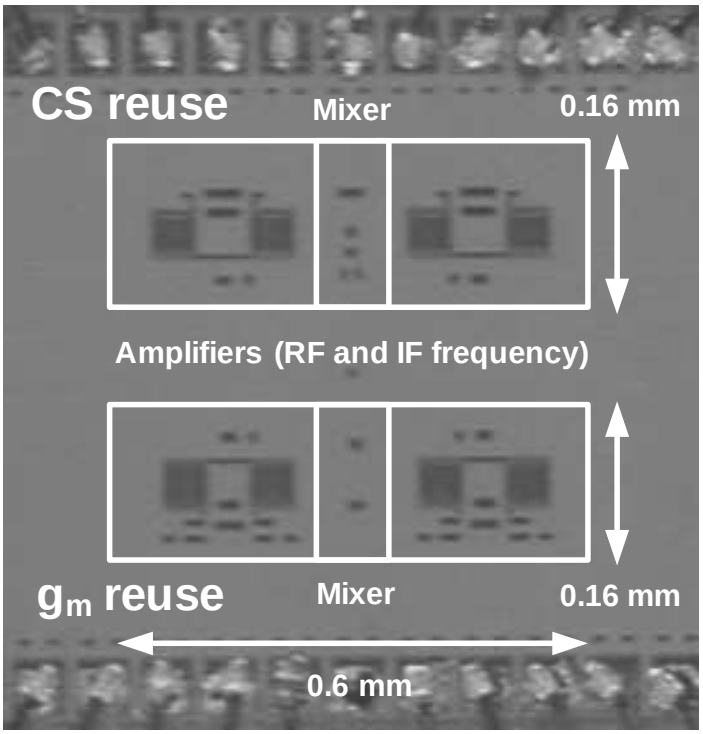


Figure 6.8: Microphotograph of the IC chip

This indicates a performance that is better than or comparable to other state-of-art low-power receiver designs, as shown in Fig. 6.7 (e.g. [37, 40, 57, 58]). The die microphotograph is shown in Fig. 6.8.

Chapter 7

Conclusion

7.1 Conclusion

As portability becomes a key requirement in the definition of wireless systems, the importance of low-power implementations has increased in most application areas. Significant performance gains have been achieved through CMOS technology scaling. Additionally, several techniques for power reduction have been demonstrated in the area of analog and RF circuit design.

This dissertation has focused on designing receiver front-ends for low-power applications. In particular, we have presented new low-power receiver down-converters with multiband signal feedback. The input-stage in this approach is effectively operates in cascade with itself at two different frequencies, thus processing signals in a recursive manner. The input transconductance stage of the down-converter has been reused for RF and IF amplification while maintaining orthogonality between the two bands. Consequently, the power efficiency of the designs is greatly improved as compared to prior work. The topologies include innovative design approaches to mitigate potential problems of instability and degradation of linearity.

Fully differential receiver down-converters are implemented using 0.13-

μm CMOS technology and measured using a fully assembled test board in order to validate the concept. The implemented designs are shown to achieve high conversion gain in excess of 50 dB, with a low power requirement while demonstrating an inherent high-order low-pass frequency response with variable gain capability. Both topologies demonstrate excellent FOM that is defined as the dynamic-range normalized to the power dissipation. The potential for further improvement in the IIP3 performance based on the inherent cancellation of nonlinear terms is expected to further improve the FOM. The measured performance of the specific implementations discussed make them very well-suited for short-distance wireless communication systems e. g. Bluetooth and IEEE 802.15.4. However the topologies can be potentially used to implement power-efficient front-ends for several systems, including high dynamic range systems such as cellular applications for example, if a high-quality low-noise amplifier precedes the feedback-based amplification step.

7.2 Future Work

This research can be extended to additional innovative schemes for implementing receiver down-converters. Some possible examples of future work that could utilize the research presented here are discussed here.

7.2.1 Optimization of Proposed Topology

While the demonstrated method provides an elegant way to obtain relatively large gain with low bias current requirements, the noise performance

of the feedback based topology needs to be further optimized. In chapter 5, the primary sources of noise were identified in both designs: the $1/f$ noise of mixer switches and mixer loads. These noise sources appeared at the mixer output and are re-amplified by the input devices. The design modification employing long channel devices or passive switching devices substantially reduces the effect of $1/f$ noise; however, it will provide additional trade-off issues between power and noise due to the degradation of the achievable overall gain. Additional techniques that reduce these noise sources at the output thus need to be investigated.

7.2.2 Fully Integrated Multiband Recursive Receiver Front-end

The basic principle introduced in chapter 4 can be further exploited for gain enhancement. In this study by using an LO equal to the input signal, dual-band reuse of the input stage was demonstrated here. If the LO frequency is selected to be half that of the RF input, triple-band gain reuse can be implemented. Thus, for a given gain, the power dissipation of the system can be reduced by a factor of three. Theoretically, the feedback-based receiver front-end is capable of being extended to a configuration consisting of multiple loops, as depicted in Fig. 7.1. According to this model, the circuit topology basically requires the following functional blocks: (1) a broadband amplifier independently providing gain for multiple distinct signals, (2) a broadband mixer simultaneously performing the frequency down-conversion, and (3) an array of frequency selection filters for each desired band. It should be noted

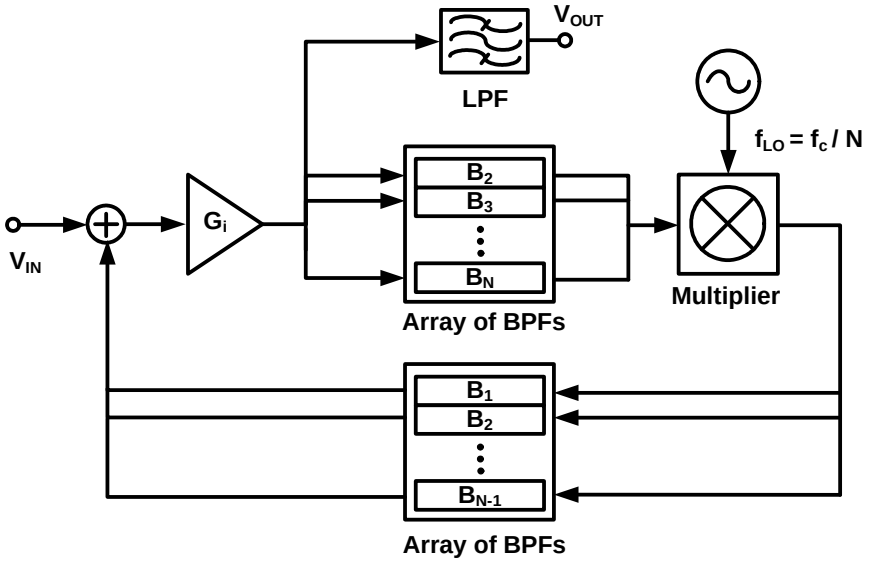


Figure 7.1: A multiband recursive receiver configuration

that for a carrier frequency of f_C and bandwidth B, in theory, a single device can provide a gain of the order of G_i^N by utilizing a multiband feedback, where N is of the order of f_C/B. The required LO frequency can be determined by f_C/N and G_i is the gain of the device from band $f_C - iB$ to $f_C - (i+1)B$. The final output is obtained through a low-pass filter from the amplifier output.

The topology represents a recursive signal loop. The signal is cycled through the same input transconductors at multiple bands, until it reaches baseband, at which point the recursion is terminated. In fact, it can be recognized that the down-converters reported in this work implement a simple two-step recursion, where the signal recursion stops at the input to the mixers, through cancellation of the differential IF signals.

7.2.3 Enhancement in Third-order Intermodulation (IM3)

The possibility for improving IM3 performance through optimal sizing of the tail current devices in the CS-reuse design was demonstrated in Chapter 5. This aspect of the work was not tested in the ICs reported earlier. Cancellation of IM3 represents a powerful approach for improving the IIP3 without enhancing power dissipation. Further research is needed in implementing this aspect of the design. As described in chapter 5, linearity of the g_m-reuse approach can be potentially improved through the use of frequency-selective degeneration in the input devices. Additionally the g_m-reuse technique has the capability to operate at lower voltage supplies. Consequently, such improvements could yield a highly attractive low-voltage and high dynamic-range down-converter topology.

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