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Scaling and Process Effect on Electromigration Reliability for Cu/low k Interconnects

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Scaling and Process Effect on Electromigration Reliability for Cu/low k Interconnects

by

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Dedication

To my family

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Scaling and Process Effect on Electromigration Reliability for Cu/low k Interconnects

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The microelectronics industry has been managing the *RC* delay problem arising from aggressive line scaling, by replacing aluminum (Al) by copper (Cu) and oxide dielectric by low-k dielectric. Electromigration (EM) turned out to be a serious reliability problem for Cu interconnects due to the implementation of mechanically weaker low-k dielectrics. In addition, line width and via size scaling resulted in the need of a novel diffusion barrier, which should be uniform and thin. The objective of this dissertation is to investigate the impacts of Ta barrier process, such as barrier-first and pre-clean first, and scaling of barrier and line/via on EM reliability of Cu/low-k interconnects. For this purpose, EM statistical test structures, having different number of line segments, line width, and via width, were designed. The EM test structures were fabricated by a dual-damascene process with two metal layers (M1/Via/M2), which were then packaged for EM tests. The package-level EM tests were performed in a specially designed vacuum chamber with pure nitrogen environment.

The novel barrier deposition process, called barrier-first, showed a higher $(jL)_c$ product and prolonged EM lifetime, compared with the conventional Ta barrier deposition process, known as pre-clean first. This can be attributed to the improved uniformity and thickness of the Ta layer on the via and trench, as confirmed by TEM. As for the barrier thickness effect, the $(jL)_c$ product decreased with decreasing thickness, due to reduced Cu confinement. A direct correlation between via size and EM reliability was found; namely, EM lifetime and statistics degraded with via size. This can be attributed to the fact that critical void length to cause open circuit is about the size of via width. To investigate further line scaling effect on EM reliability, SiON (siliconoxynitride) trench-filling process was introduced to fabricate 60-nm lines, corresponding to 45-nm technology, using a conventional, wider line lithograph technology. The EM lifetime of 60-nm fine lines with SiON filling was longer than that of a standard damascene structure, which can be attributed to a distinct via/metal-1 configuration in reducing process-induced defects at the via/metal-1 interface.

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Chapter 1: Introduction

RC delay problem accelerated the industry-wide move to replace aluminum (Al) interconnects with copper (Cu) interconnects for its superior electrical conductivity. However, compared with the natural passivating oxide that forms over Al free surfaces, Cu oxide layer cannot act as a self-protecting barrier layer to Cu due to its unstable and weak mechanical properties. Chemical Mechanical Polishing (CMP), which comprises one of the unit processes in the Cu damascene interconnect fabrication, generates significant amount of process defects on the upper surface of Cu lines. These two factors make the top interfaces of Cu to become the dominant diffusion path. To further improve the *RC* delay, conventional oxide dielectric was replaced by low-k dielectrics in the industry. With continued line scaling and the implementation of low-k dielectrics, the current density and interface area to volume ratio further increased. This increases the interfacial diffusion and decreases the electromigration (EM) lifetime. Therefore, it is important to investigate the scaling effect and the related process effect on EM reliability in Cu/low-k interconnects.

1.1 ELECTROMIGRATION FUNDAMENTAL

Electromigration (EM), known to be the most serious and persistent reliability issue, describes an atomic diffusion phenomenon in metal (such as Al, Cu) caused by an external direct current (DC) driving force [1]. Without the external driving force, metal atoms are in the state of random motion. With the electrical current flow through the metal wire, electrons collide with metal ions leading to an electron wind force as shown in Figure 1.1.

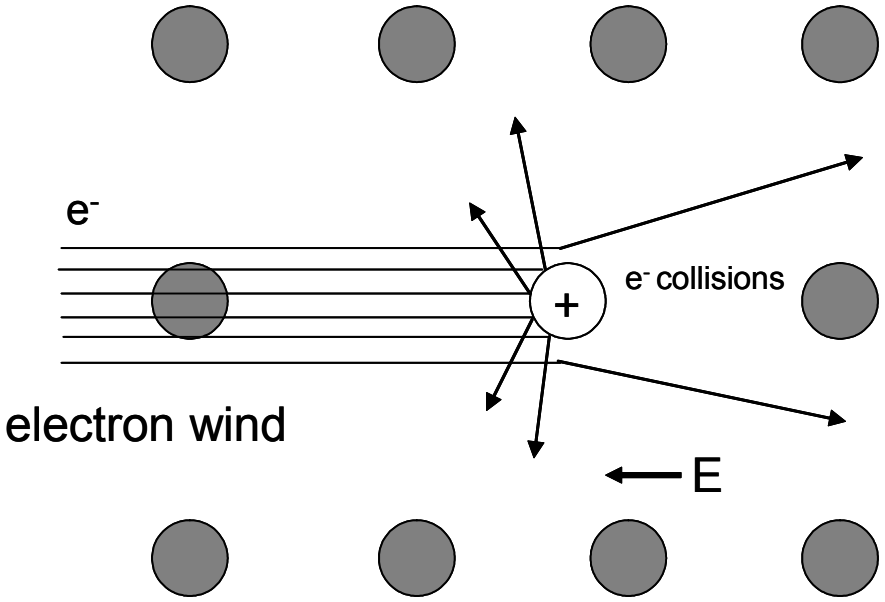

Figure 1.1 Schematic of the driving force of electromigration in metal wire. With the electric field E, electrons collide with metal atoms in the electron flow direction resulting in EM phenomenon.

The electron wind force causes the cathode of the metal line to become depleted. The EM driving force can be expressed as

$$F_e = Z^* eE = Z^* e\rho j \,, \tag{1.1}$$

where E is the electric field, e is the charge of an electron, Z^* is the effective charge number, ρ is the electrical resistivity, and j is the current density. The atomic flux (J_e) driven by the EM driving force (F_e) can be written as

$$J_e = nv_d \,, \tag{1.2}$$

where n is the atomic density, and v_d is the drift velocity. The drift velocity of moving metal ions can be expressed using the Nernst-Einstein relation:

$$v_d = \mu F_{eff} = \frac{D_{eff}}{kT} Z^* eE = \frac{D_{eff}}{kT} Z^* e\rho j \,, \tag{1.3}$$

where μ is the atomic mobility, D_{eff} is the effective diffusivity of metal ion and k is the Boltzmann constant, and T is the absolute temperature. Two parameters in Equation 1.3 determine the drift velocity of metal atoms and in turn the EM lifetime. The first is current density j which will continue to increase with line scaling as outlined by the *International Technology Roadmap for Semiconductors* (ITRS) [2]. The second is the effective diffusivity D_{eff} of moving ions. Basically, EM phenomenon is a result of metal mass transport, therefore, mass-transport pathway is a major parameter to consider. EM can occur through a number of pathways such as surface, interface, grain boundary, and lattice. The effective diffusivity D_{eff} in Cu interconnects can be expressed by combining all these pathways as [3]

$$D_{eff} = n_B D_B^* + D_I^* \delta_I \frac{1}{h} + D_S^* \delta_S \left(\frac{2}{w} + \frac{1}{h} \right) + D_{GB}^* \left(\frac{\delta_{GB}}{d} \right) \left(1 - \frac{d}{w} \right), \qquad (1.4)$$

where the subscripts identify pathways of diffusion by B = bulk, I = Cu/Ta interface, S = un-coated Cu surface, GB=grain boundary. δ_I is the width if the interface, δ_s is the width of the surface, and δ_{GB} is the width of grain boundary, d is the grain size, w is the line width, and h is the line thickness: and n_B, δ_I/h, $\delta_s(2/w+1/h)$, $(\delta_{GB}/d)(1-d/w)$ are the fraction of atoms diffusing through the bulk, interface, surface, and grain boundary of the line, respectively.

To reduce *RC* delay, new metals and dielectrics are needed to maintain the IC performance. Industry wide, copper (Cu) interconnects have replaced aluminum (Al) for their superior electric conductivity and thermal stability [1,4]. In addition, materials with low dielectric constant (low-k) were developed to replace the silicon oxide which has higher k [5]. Figure 1.2 shows a significant reduction of *RC* delay with incorporation of Cu and low-k dielectric compared with Al and silicon oxide [6,7].

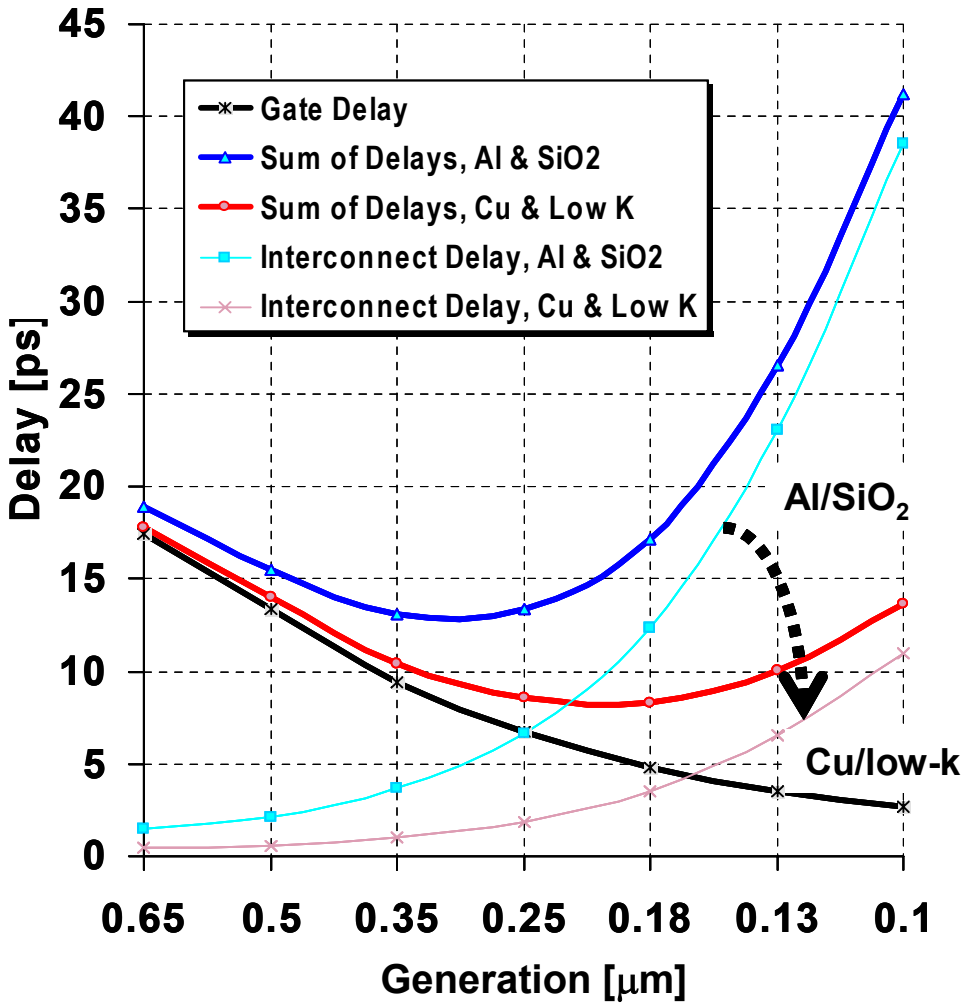

Figure 1.2 Gate and interconnects delay as a function of generation. With implementation of Cu and low-k dielectrics, the total delay was significantly reduced, compared with Al/SiO_2 interconnects [6].

The traditional subtractive etching approach used to form Al metal lines can not be used to form the Cu interconnect structure due to the difficulty of RIE of Cu structures [4]. To build a Cu interconnect, a damascene process was developed by the industry. The comparison between conventional RIE process for Al interconnects and single damascene

process for Cu interconnects is shown in Figure 1.3. The advantage of the damascene process is that this process can be extended to deep submicron line dimensions with a high aspect ratio. However, the damascene process is a high-cost manufacturing process which requires accurate process control.

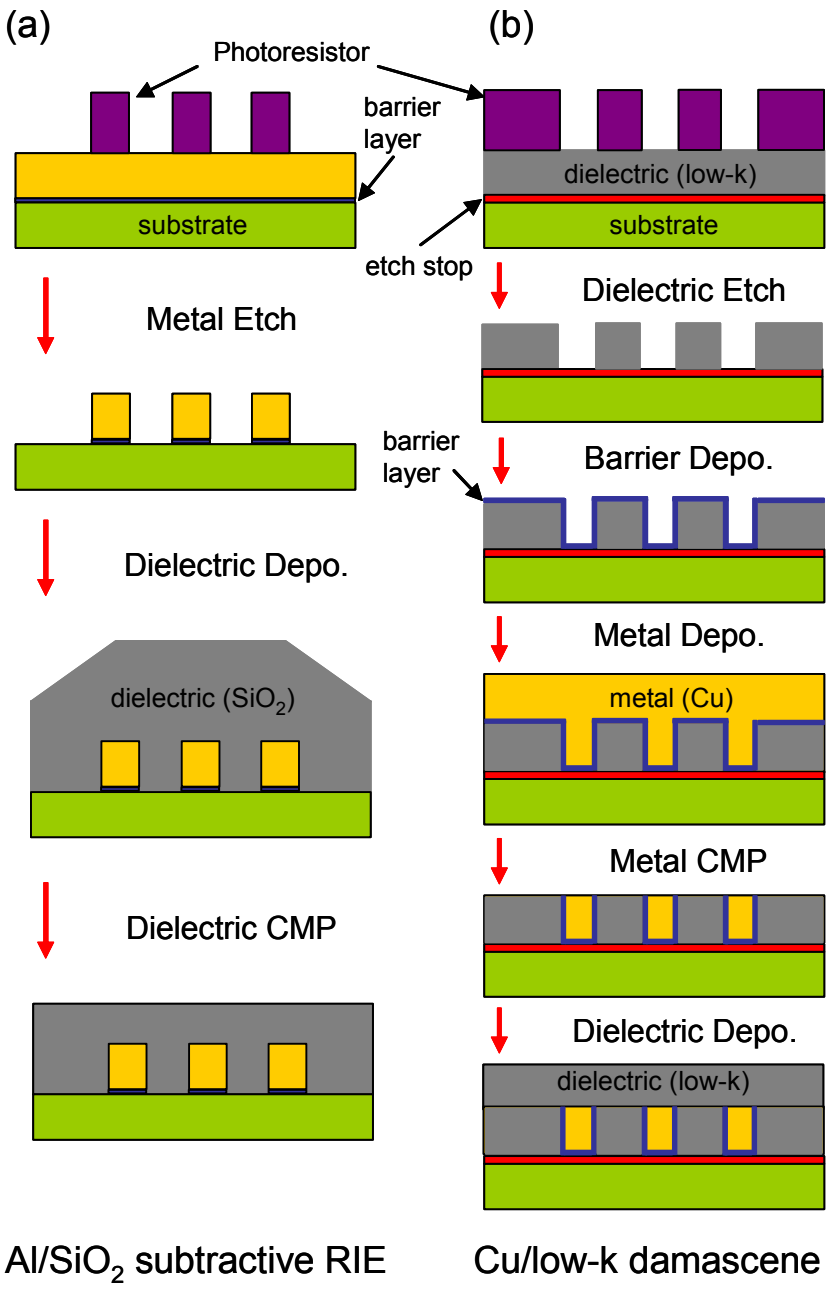

Figure 1.3 Comparison of (a) conventional RIE process for Al interconnects with (b) damascene process for Cu interconnects.

Several dual damascene integration schemes have been developed, which can generally be categorized as either “via first” or “trench first” depending on which pattern is initially delineated [4]. Via first approach has been widely adopted for small geometry devices. In the dual damascene process, the conductor (trench) and via are formed prior to deposition of the metal barrier/Cu seed/Cu fill. Therefore, only one metal fill and one metal CMP step are required for each level of interconnect, resulting in lower via resistance and improving reliability over that of the single damascene process. The disadvantages of the dual damascene approach include higher aspect ratios for etch/fill and more complicated integration schemes.

In addition to Cu metallization, implementation of low-k dielectric is one of the prominent aspects of the advanced interconnects. The implementation of low-k material to replace silicon oxide resulted in further reduction of the *RC* delay in a microelectronics device, and eventually reduced the number of metal levels for the same amount of device functionality. However, the low-k dielectric generated a number of problems including thermally or mechanically induced cracking or delamination [8], moisture absorption [9], current leakage and voltage breakdown reliability issues [10], poor mechanical strength, process complexity, and etch damage.

Compared with Al/oxide, Cu/low-k interconnects offered significant performance and reliability improvement but presented integration and reliability challenges. Since Cu atoms diffused into low-k dielectrics easily, Cu lines must be encapsulated with metallic (such as Ta, TaN) and dielectric (such as SiN, SiC) diffusion barriers to avoid corrosion and electric leakage between adjacent metal lines [11-15]. This requires optimization of fabrication processes such as dielectric etch, chemical mechanical polishing, copper/barrier metal deposition process and dielectric barrier deposition in order to produce chemically and mechanically stable interconnects.

1.2 STATISTICAL ANALYSIS OF EM USING MULTI-LINKED STRUCTURE

1.2.1 Statistical Measurement of EM Threshold in Cu Interconnects

Under EM stress, the atomic flux driven by EM generates a back flow of metal atoms in the direction opposite to the EM flux. Suppose a Cu line is completely encapsulated by a capping layer on top and barrier layer at the sidewall and bottom as shown in Figure 1.4. During EM testing, the EM electron wind force pushes the Cu atoms toward the anode end while vacancies migrate toward the cathode end. Accordingly, the stress state becomes gradually compressive at the anode and tensile at the cathode compared with the initial stress (σ_o) state [16].

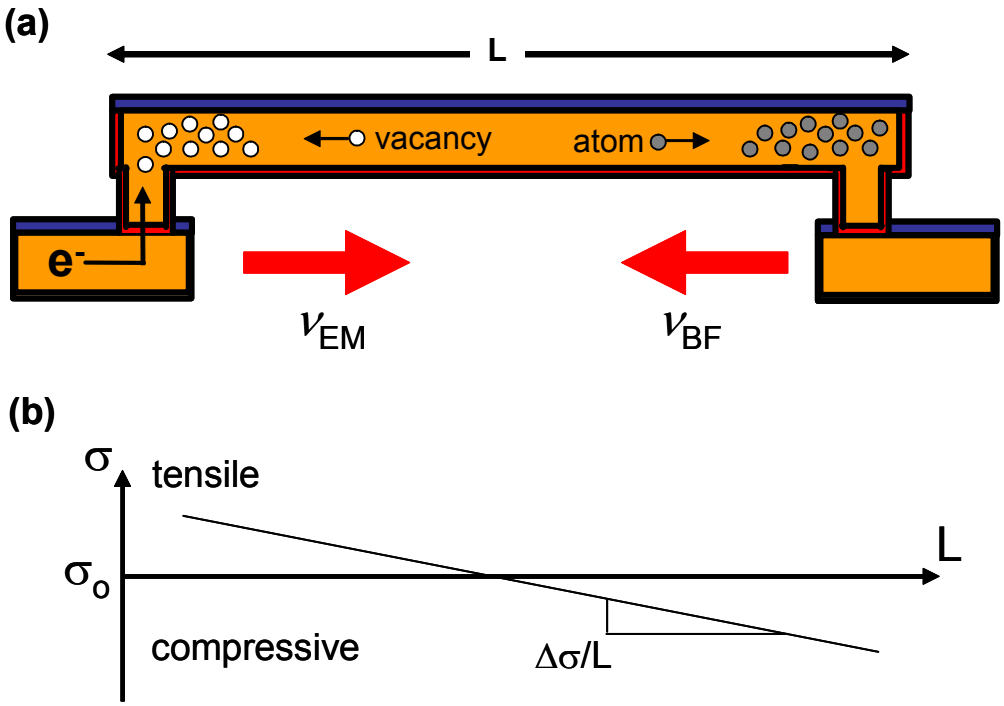

Figure 1.4 (a) Mass transport in the Cu line encapsulated by the capping layer and barrier layer. (b) Stress state for the Cu line under EM upon reaching steady-state stress.

During EM, the drift velocity of moving ions, v_{EM}, can be expressed using the Nernst-Einstein relation:

$$v_{EM} = \frac{D_{eff}}{kT} Z^* ej\rho , \tag{1.5}$$

where D_{eff} is the effective diffusivity, Z^* is the effective charge, e is the electronic charge, j is the current density, ρ is the electrical resistivity of metal (Cu), k is Boltzmznn's constant, T is the ambient temperature. As shown in Figure 1.4, the back-flow stress generated by atoms with a drift velocity (v_{BF}) opposes the net EM drift velocity. Accordingly, the net atomic drift velocity (v_d) under EM can be expressed by the Blech model as the following [45,46]:

$$v_d = v_{EM} + v_{BF} = \frac{D_{eff}}{kT}\left[Z^* ej\rho - \frac{\Omega \Delta\sigma}{L} \right], \tag{1.6}$$

where Ω is the atomic volume, $\Delta\sigma$ is the back-flow stress induced by EM, L is the metal line length.

As the metal line length decreases under a constant back-flow stress, $\Delta\sigma$, the steady-state stress gradient, $\Delta\sigma/L$ increases. Once the back-flow stress gradient becomes large enough to compensate the EM flux, the net metal atomic flux will be zero [17-20]. The critical product $(jL)_c$ defined for this condition can be deduced from Equation (1.6).

$$(jL)_c = \Omega\, \Delta\sigma / Z^* e\rho , \tag{1.7}$$

The $(jL)_c$ product of Cu/low-k interconnects can be dominated by the confinement of the surrounding layers including the barrier and capping layers, while the mechanically weak low-k dielectric provides little confinement. Obviously, to improve EM lifetime, the net atomic drift velocity needs to be reduced. One way to reduce the net atomic drift velocity is to increase the stress gradient in the Cu line, $\Delta\sigma/L$. Thus, a conformal and reasonably thick barrier and capping layers will increase the effective modulus to improve the EM lifetime for Cu/low-k interconnects.

1.2.2 Statistical Measurement of Early Failure in Cu Interconnects

The early failure, so-called weak-mode failure, occurs at an earlier time than expected according to a mono-modal failure distribution [21-25]. Normally, the weak-mode failure shows about one order of magnitude shorter lifetime and smaller population than those of the strong-mode failure. Thus, the presence of weak-mode failures can seriously degrade EM reliability for Cu/low-k interconnects. The advantage of the multi-linked test structure is that an extremely small population of early failures can be detected. For example, using only single link (N=1) structures, it would take 1,000 samples to yield 3 early failures, on the average, to detect 0.3 % early failure. However, the same result can be reached by only 10 samples of N=100 multi-linked structure. Therefore, the testing time can be significantly reduced by multi-linked structures. In these test structures, long 150-μm M2 lines were connected to short 10-μm M1 lines and vias. Ten (N=10) and one-hundred (N=100) single component test structures were connected in series. EM tests using both single component and multi-linked test structures were performed to determine the statistics of the weak-mode failure and the strong-mode failure separately.

Figure 1.5 shows a Cumulative Failure Distribution (CDF) plot for 0.25-μm Cu/low-k interconnects. The EM test was performed at 330 ℃, with a current density of 1.0 MA/cm^2. With increasing number of line segments, the probability of line failures increased, and the EM lifetime decreased. It was clearly seen that two different failure mechanisms were involved in the test samples. Monte Carlo simulation was used to derive the lifetime and failure statistics for the strong-mode and the weak-mode as a function of number of line segment, N [26-29]. Monte Carlo simulation generates random lifetimes for N line segments. Since the N line segments are connected in series, the first failed segment determines the lifetime for the whole structure. In such system, the random-failure time can be expressed as

$$\tau = \min [\tau_1, \ldots, \tau_N] , \tag{1.8}$$

where τ_i (=1, . . . , N) are the potential random failure times from a population of N interconnects. This idea comes from the so-called Weakest Link Approximation (WLA) so that the weakest link in the multi-linked structure determines the failure of the entire chain

$$F_N(t) = 1-(1-F_1(t))^N , \tag{1.9}$$

where N is the number of elements in the series and $F_1(t)$ is the CDF for single elements. Thus, if the CDF for single elements is identified, CDFs with N elements in series can be generated using Equation (1.9).

Statistical parameters include strong-mode lifetime (t_{50}), strong-mode standard deviation (σ), weak-mode lifetime (t_{50}), weak-mode standard deviation (σ), and the

population of weak-mode. To derive the parameters, two failure modes need to be considered as independent to each other. As shown in Figure 1.5, Monte Carlo simulation can be performed successfully by fitting the experimental CDF plot. Using this method, the t_{50}'s from the simulation according to the experimental data was found to be 130 hrs and 13 hrs for strong-mode and weak-mode, respectively. In addition, the weak-mode failure for N=1 was found to be 0.3 % of the failure statistics.

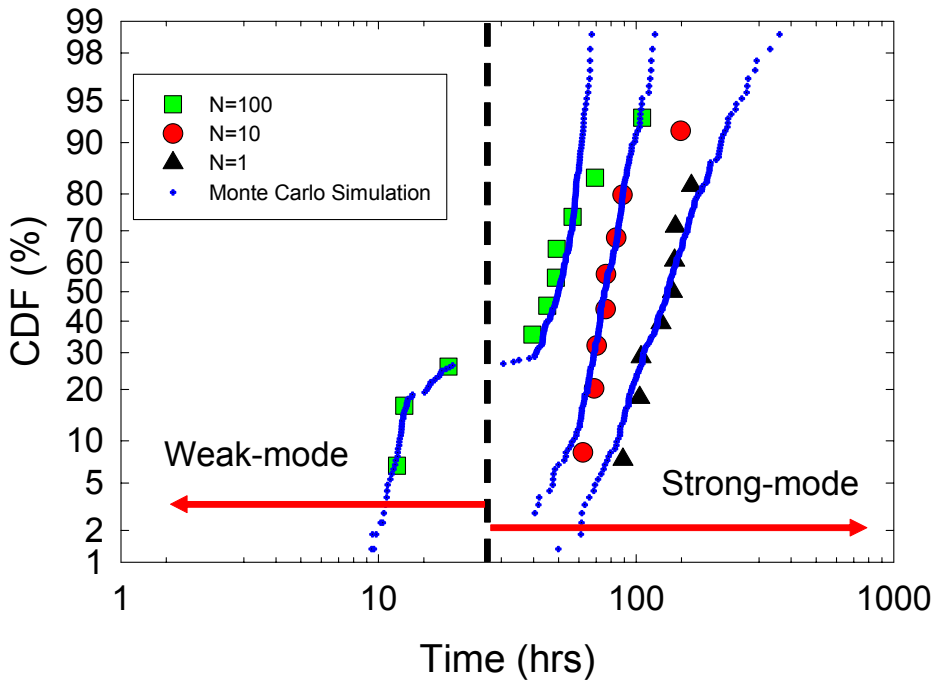

Figure 1.5 Cumulative failure distribution (CDF) plots of experimental and Monte Carlo simulation results. The electromigration test was performed at 330 ℃, with a current density of 1.0 MA/cm^2. The weak-mode population was about 0.3 %.

1.3 EM RELIABILITY ISSUES RELATED SCALING AND LOW-K DIELECTRICS

The dominant EM flux occurs along the Cu/capping layer interface [3, 30-33]. This makes EM reliability more serious for Cu interconnects with line scaling due to the increase in surface to volume ratio. Note that, in the case of Al interconnects, the EM performance can be improved with line width scaling due to a stronger "bamboo" like grain structure. This reduces grain boundary network along the metal line through which EM flux can occur. The EM flux in Cu interconnects can be further accelerated by defects caused by chemical mechanical polishing (CMP), which is a necessary step in the damascene process as shown in Figure 1.3(b). For this reason, most recent studies have focused on reducing surface diffusion by adding a capping layer such as CoWP, Pd, CoSnP, Cu_3Sn etc., on top of the Cu layer after the CMP [34-38]. With surface diffusion so contained, efforts are now focused on a few other areas for controlling EM, such as barrier thickness and via processing. Among these areas, barrier thickness continues to scale according to the *International Technology Roadmap for Semiconductors* (ITRS) [2] shown in Figure 1.6.

Process-related issues on reliability have been observed, including a decrease in early failure lifetime and increase in reliability degradation for Cu/low-k interconnect with line scaling due to the difficulty in process control [39]. Therefore, with the continued scaling of line widths, significant efforts have been focused to develop novel barrier materials and barrier deposition processes [40-42]. Since Ta barrier thickness needs to be reduced to satisfy the projected interconnect performance, the development of a new barrier deposition process for thinner barrier and the evaluation of EM reliability for such process became equally important for the future interconnects [43]. Different Ta barrier deposition processes can lead to different profiles of via bottom, which is the most probable failure initiation site for process-induced early failures [44]. Since most of the

process defects occur at the thin diffusion barrier layer, a uniform and stable barrier is essential for improving EM reliability of Cu interconnects.

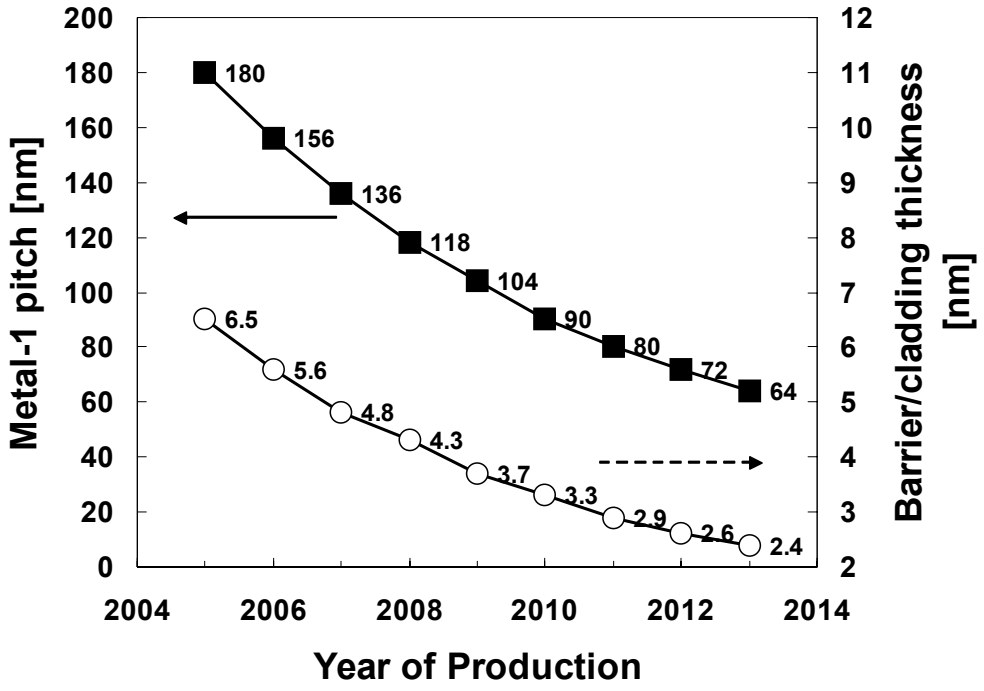

Figure 1.6 Metal line and barrier thickness scaling for MPU and ASIC according to the *International Technology Roadmap for Semiconductors* (ITRS) 2006 updated [2].

The metal line scaling will lead to increase in current density, which increases the reliability risk due to EM. As shown in Figure 1.7, the operating current density for the intermediate wire will be 3.08 MA/cm^2 with the 59 nm wide interconnects, which is about three times as large as a typical EM test condition for 90 nm node [2]. The trend of increasing current density will be continued for the future microelectronics devices. The

industry is very concerned on the EM reliability issues relating to line width scaling, barrier thickness scaling, and implementation of low-k dielectrics.

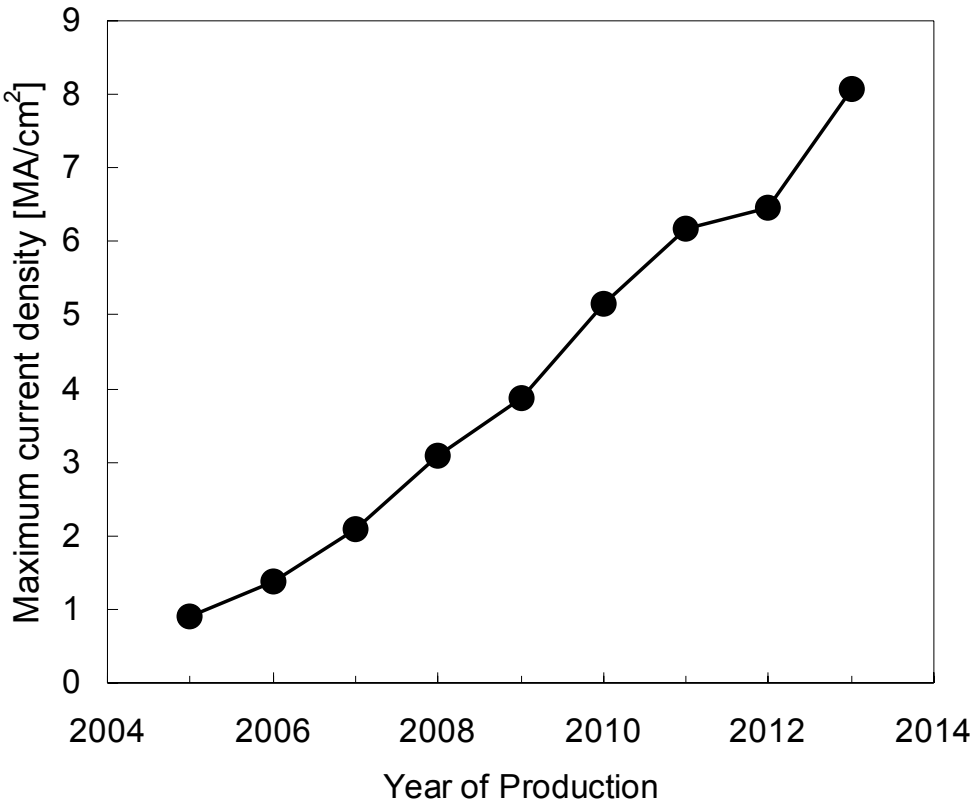

Figure 1.7 Maximum current density for MPU and ASIC at 105 ℃ according to the *International Technology Roadmap for Semiconductors* (ITRS) 2006 updated [2].

A schematic view of EM reliability issues, relating to line scaling and low-k dielectric, is shown in Figure 1.8. The critical length effect leading to the $(jL)_c$ product was first advanced by I. A. Blech [45,46], and many studies of Cu/oxide and Cu/low-k interconnects followed [47-51]. They reported that the $(jL)_c$ product of the Cu/low-k interconnects was lowered because the low-k dielectric was mechanically weaker than

oxide. In addition, as barrier thickness continues to scale down, the confinement of the Cu line will decrease and the $(jL)_c$ product will be lowered.

For Cu dual-damascene structure, the upper level trench (Metal-2) and via are formed simultaneously before Cu filling. Therefore, there is no flux divergence at the Metal-2/via interface. However, the dual-damascene process places the flux divergence at the Metal-1/via interface for up-current and down-current situations. This via-bottom flux divergence usually causes reliability problem because only a small amount of material depletion is needed for void formation to cause failure. As the via size shrinks further, via processing can exacerbate plasma damage and process-induced defects at the via bottom and uneven coverage of the barrier layer at the sidewall. These problems are manifested in EM early failures and stress migration failures [52]. It was reported that EM early failure was caused by local defects, which were related to processes such as liner deposition, pre-clean or trench etch [44].

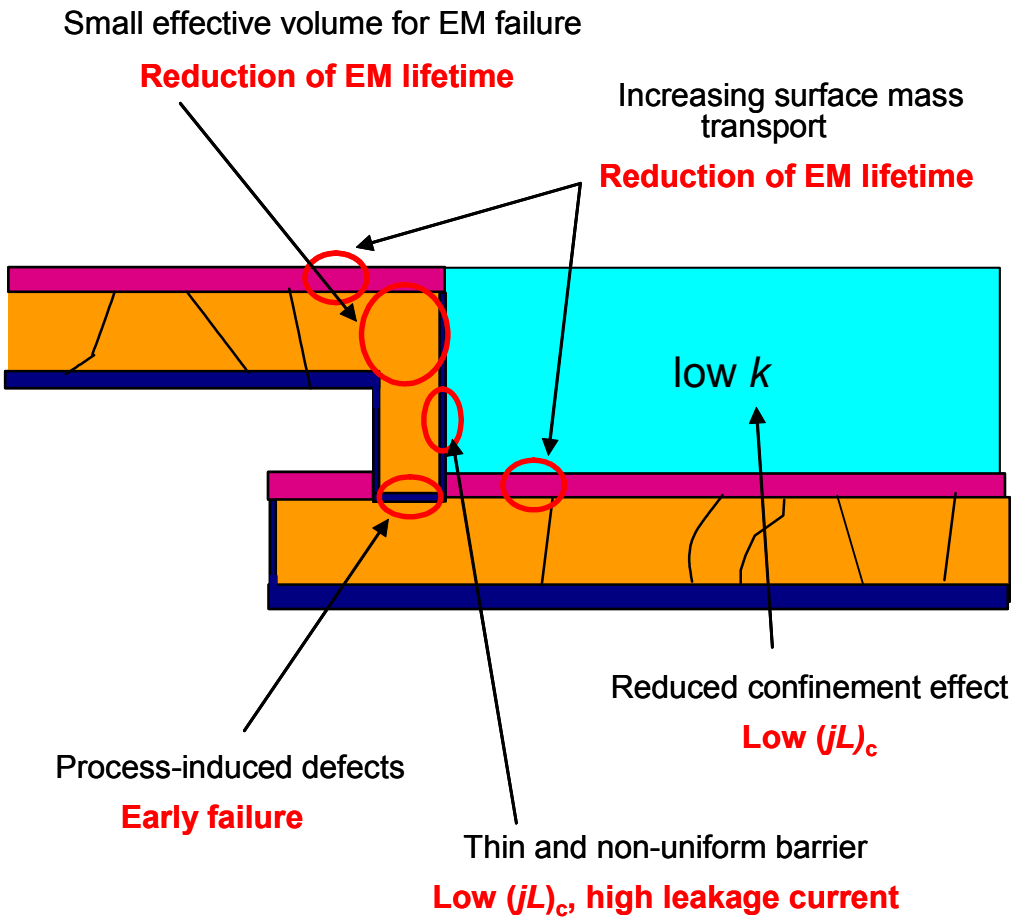

Figure 1.8 Degradation of EM reliability in dual damascene Cu/low-k interconnects due to line scaling and an implementation of low-k dielectrics.

1.4 RECENT EM STUDIES

As discussed so far, with decreasing line dimension, the surface to volume ratio of Cu lines increases, and the effective void volume to cause line failure decreases. Therefore, the EM lifetime and the allowable current density will be reduced for future interconnects. Many studies have focused on reducing diffusion along the surface

between Cu and capping layer, such as SiN, known to be the most dominant mass transport path in Cu interconnect. C.-K Hu *et al.* [53] reported an EM lifetime improvement for the Cu lines capped with a 10-nm thick, electroless CoWP layer compared with the Cu lines capped with a 35-nm thick SiC_xH_y layer. The improvement of lifetime was about two orders of magnitude. The activation energy for EM with CoWP was 1.9 eV for bamboo-like grain structure, compared with 0.90 eV for SiC_xH_y capping [54].

Via width effect on EM reliability was reported, showing longer EM lifetime and tighter distribution of EM lifetime for a wider via [34]. This was attributed to the stable liner connection between via and underlying Cu line.

Using multi-linked EM test structure, observation of early failure was made [55,56]. An EM-induced voids causing weak-mode failure were frequently observed at the via bottom. The post-EM physical failure analysis showed that the less material is required for via voiding compared to that which is required for trench voiding. The activation energy for the weak-mode (early failure) was found to be 1.00 ± 0.05 eV, which was consistent with interface dominant diffusion mechanism [26].

The EM lifetime of Cu/porous low-k interconnects is generally shorter than that of Cu/oxide interconnects under similar EM test conditions and identical test structure dimensions [27], which can be attributed a smaller back flow stress due to less thermomechanical confinement in Cu/low-k interconnects. The lower back-stress is consistent with a smaller effective modulus, which increases the net mass transport and in turn reduces EM lifetime. This led to a small value of $(jL)_c$ product for Cu/low-k interconnects. The statistics of EM lifetimes and the origin of the lognormal standard deviation of Cu interconnects were reported [57, 58]. In this study, they investigated the effect on EM lifetime statistics due to the variations in void sizes, geometrical and

experimental factors of EM experiment, and differences in the interface diffusivity between lines. This report demonstrated that an optimum grain size and orientation distribution can improve the standard deviation of EM lifetime. Such an optimization is challenging for the deep submicron interconnects.

1.5 PROPOSED WORK

Electromigration (EM) is a serious reliability concern for Cu interconnects, particularly with continued scaling and the implementation of porous low-k dielectrics. The ratio of surface and interface area to volume of Cu interconnect will continue to increase with further line width and via scaling. The implementation of porous low-k dielectric weakens the interconnect structure, which further degrades EM performance of the Cu interconnects. The objective of this work is to investigate the effects of process and scaling on EM reliability for Cu/low-k interconnects. EM test structures and EM experimental procedure will be described in Chapter 2. The barrier process effect on EM will be discussed in Chapter 3, and then the effect of barrier thickness and line/via scaling on EM will be discussed in Chapter 4 and 5, respectively. EM reliability for 60 nm wide lines corresponding to 45-nm technology will be investigated for future devices in Chapter 6. Finally, summary and recommendation will be given to conclude this work in Chapter 7.

In Chapter 3, an important and recently introduced Ta barrier deposition process, the so-called barrier-first process, which was developed to produce a more uniform Ta barrier, will be evaluated. A systematic study of the barrier-first process effect on EM has not been previously reported. Since the Ta barrier thickness needs to be reduced in order to satisfy the projected interconnect performance, the development of a new barrier deposition process for thinner barrier and the evaluation of EM reliability for such

process will be equally important for the future development of Cu lines. Different Ta barrier deposition processes based on barrier-first and pre-clean-first will be used to study the barrier process effect on EM reliability. Different barrier processes can lead to different profiles of the via bottom, which is a suspect region for failure initiation in a process-induced early failure. Statistical multi-linked EM test structures will be used to determine the statistics of the weak-mode early failures and the strong-mode failures separately. In this way, the small population of the early failures can be detected. Statistical $(jL)_c$ product will be determined for samples with different Ta barrier processes to understand how the barrier processes affect the confinement of Cu/low-k interconnects. The microstructures including Ta barrier morphology and EM-induced voids will be analyzed by transmission electron microscopy (TEM) and focused ion beam (FIB) microprobe.

In Chapter 4, the barrier thickness effect on EM reliability for Cu/low-*k* interconnects will be investigated using multi-linked test structures. The critical $(jL)_c$ product for Cu/low-*k* interconnects with Ta barriers ranging from 75 Å to 175 Å in thickness will be measured. In addition, multi-linked early failure structures will be used to quantify the failure statistics for the intrinsic strong-mode failures as well as for the extrinsic weak-mode failures for the different barrier thicknesses. The weak-mode failures are particularly important since the overall lifetime of multi-linked interconnects is controlled by the weakest link, which in practice is dominated by extrinsic process-induced defects.

In Chapter 5, the effects due to via scaling and line scaling on EM reliability for Cu/low-k interconnects will be investigated. Three types of EM test structures varying in line width and via size will be designed for this study. Two types of up-stream electron flow condition and one type of down-stream electron flow condition will be included.

The M2 line width and the via size will be both scaled down from 175 nm to 90 nm for up-stream electron flow condition, while the M1 line width and the via size will be both scaled down from 175 nm to 125 nm for down-stream electron flow condition

In Chapter 6, the EM behavior of ultra fine lines, ~60 nm will be studied. With aggressive device size scaling, the metal-1 half pitch in the interconnects will be reduced to 59 nm in two years. However, EM reliability studies for the fine lines, ~60 nm has not been conducted widely due to the difficulty of processing. In this study, the EM test structure was fabricated by a novel process of pre-filling the trenches with SiON which can delineate 60-nm metal lines using a conventional, wider line lithograph technology. The new process provides a unique metal-1/via interface structure which can eliminate the most probable void formation site responsible for early failures. This projection will be put to test through statistical treatment of the failure data. To investigate the trench-filling SiON effect on EM reliability, samples with and without SiON filling layer will be tested. Three different line widths; 60 nm, 110 nm, and 185 nm will be fabricated for this purpose. The activation energies for EM in Cu interconnects with different processes need to be determined in order to understand the dominant diffusion pathway. Also, the current density effect on EM reliability, particularly at high current density, will be investigated. This is because the current density continues to increase with the new design rules for microelectronics devices.

Chapter 2: Experimental Procedure

In this chapter, the details of EM experiments are described. The sequence of EM testing is illustrated in Figure 2.1. EM test structures were designed to investigate EM reliability of Cu interconnects. Based on the design, wafer fabrication for two-level interconnects (M1/via/M2) was done on 300 mm wafers using a dual-damascene process. The wafer was diced, the dies mounted on a ceramic package, and the connections between the die and the package were made by wire bonding. EM tests of the packaged samples were performed in a high vacuum chamber. The resistance traces were monitored to determine EM lifetime and study the EM failure mechanisms. From the lifetime data, Cumulative Failure Distribution (CDF) curves were constructed. Physical failure analysis was performed using transmission electron microscopy (TEM) and focused ion beam (FIB). In addition, statistical multi-linked EM test structures are discussed. Using these test structures, the critical line length and statistics of early failure were determined. Finally, the behavior of resistance traces during EM test was discussed.

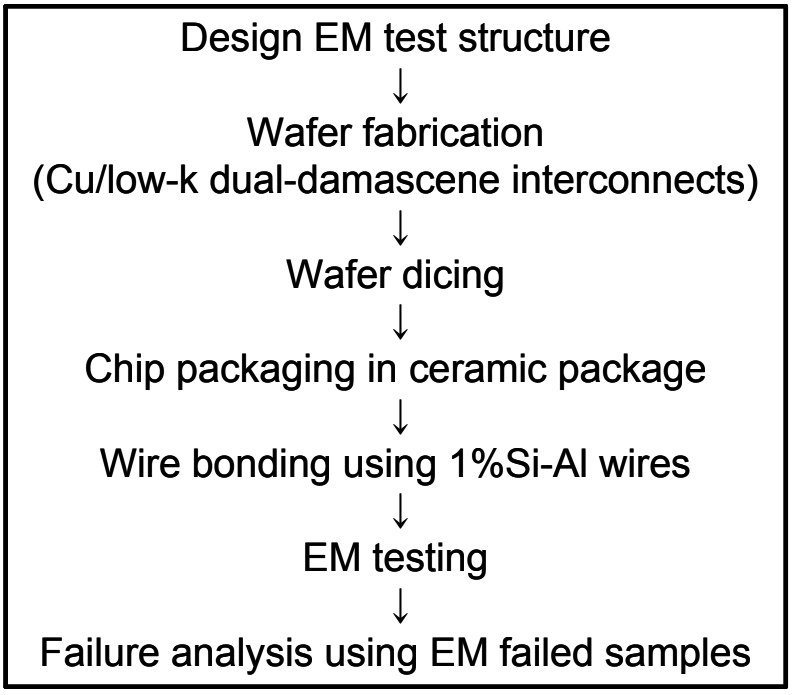

Figure 2.1 Summary of electromigration testing procedure.

2.1 EM TEST STRUCTURE DESIGN

Two-level (M1, via, and M2) EM test structures were designed to investigate EM reliability for Cu interconnects. The EM test structures used are summarized in Table 2.1. Four to six EM patterns were included in a module. The minimum line/via width was 90 nm. Three line widths: 175, 125 and 90 nm were included corresponding to the 130, 90 and 65-nm nodes, respectively. Basic single line EM structures, denoted as DV, occupied six modules. Variations of line length, line width, and current direction were incorporated in the DV modules. To investigate the effect of via scaling on EM reliability, EM structures with different M2 line widths under identical via size were designed. These

structures were included in the VJ module. The details of the VJ structures will be described further in chapter 5.

Up stream electron flow structure is shown in Figure 2.2 (a). In this structure, electrons flowed from a wide and short M1 line to a narrow and long M2 line. Thus EM-induced damage for M1 lines can be minimized. Using the up-stream electron flow structure, the void formation and line failure either in the M2 line or in the via can be observed. As shown in Figure 2.2 (b), the down stream electron flow structure was also designed to investigate the void formation and line failure in the M1 line. In this case, EM electrons flowed from the wide and short M2 level to the narrow and long M1 level. In addition to the single line structure which had one stressed line, two types of multi-linked EM structures, denoted by EF and LC in the first column of Table 2.1, were included in the EM test modules to investigate critical line length effect and the statistics of early failure in Cu/low-k interconnects. The schematic side views of early failure (EF) and critical length (LC) are shown in Figure 2.3. The first multi-linked structure is an early failure (EF) structure, which contained different number of serial line segments comprising of one (N=1), ten (N=10) and one-hundred (N=100) test elements, respectively. The second multi-linked structure is a critical length (LC) structure, which comprises six repeating sets of multi-linked elements, where each set had the stressing metal 2 (M2) lengths varied from 10 μm to 300 μm, while the connecting metal 1 (M1) line length remained fixed at 5 μm in order to minimize EM damage in the M1 line. As shown in Figure 2.3 (c), 14 different line lengths are included in one set of interconnects with the line lengths of 10, 15, 20, 25, 30, 35, 40, 45, 50, 75, 100, 150, 200 and 300 μm. The schematics shown in Figure 2.2 are up-current electron flow test structures which are designed to investigate EM damage in the trench and/or via on the M2 level. In this structure, stressed M2 lines are narrow and long, while connecting M1 lines remains wide

and short. In addition, down-current test structures are designed for EM tests on the M1 level with the pattern of line dimensions reversed to target failures at M1 rather than M2.

Table 2.1 Summary of EM testing structures including up-stream and down-stream electron flow conditions.

Module	Test Pattern					
1 (DV_N1_M1_0090)	L=10 μm	L=25 μm	L=50 μm	L=75 μm	L=100 μm	L=300 μm
2 (DV_N1_M2_0090)	L=10 μm	L=25 μm	L=50 μm	L=75 μm	L=100 μm	L=300 μm
3 (DV_N1_M1_0125)	L=10 μm	L=25 μm	L=50 μm	L=75 μm	L=100 μm	L=300 μm
4 (DV_N1_M2_0125)	L=10 μm	L=25 μm	L=50 μm	L=75 μm	L=100 μm	L=300 μm
5 (DV_N1_M1_0175)	L=10 μm	L=25 μm	L=50 μm	L=75 μm	L=100 μm	L=300 μm
6 (DV_N1_M2_0175)	L=10 μm	L=25 μm	L=50 μm	L=75 μm	L=100 μm	L=300 μm
7 (VJ)	M2=0.090 μm		M2=0.125 μm	M2=0.175 μm		M2=0.250 μm
8 (VJ_M2_0250)	W=0.090 μm		W=0.125 μm	W=0.175 μm		W=0.250 μm
9 (VJ_via_0090)	M2=0.090 μm		M2=0.125 μm	M2=0.175 μm		M2=0.250 μm
10 (LC_M1)	W=0.125 μm		W=0.175 μm	W=0.250 μm		W=0.500 μm
11 (LC_M2)	W=0.125 μm		W=0.175 μm	W=0.250 μm		W=0.500 μm
12 (EF_M1_0090)	N=1		N=10	N=100		Temp. monitor
13 (EF_M2_0090)	N=1		N=10	N=100		Temp. monitor
14 (EF_M1_0125)	N=1		N=10	N=100		Temp. monitor
15 (EF_M2_0125)	N=1		N=10	N=100		Temp. monitor
16 (EF_M1_0175)	N=1		N=10	N=100		Temp. monitor
17 (EF_M2_0175)	N=1		N=10	N=100		Temp. monitor

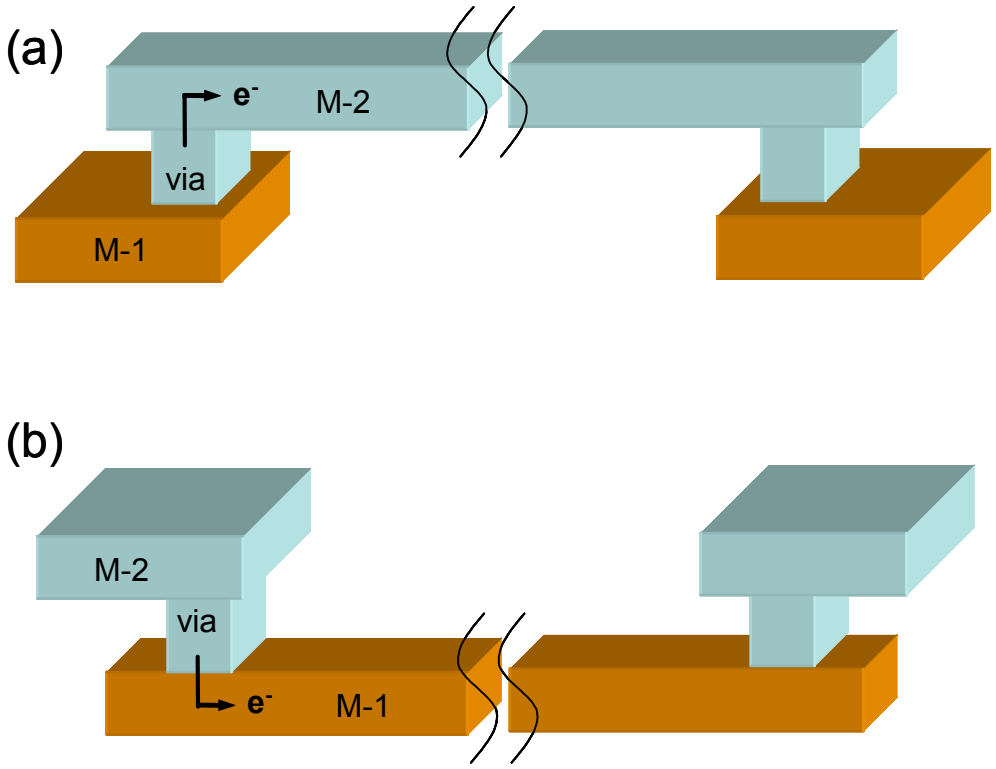

Figure 2.2 Schematics of EM test structure with (a) up-stream electron flow, and (b) down-stream electron flow condition.

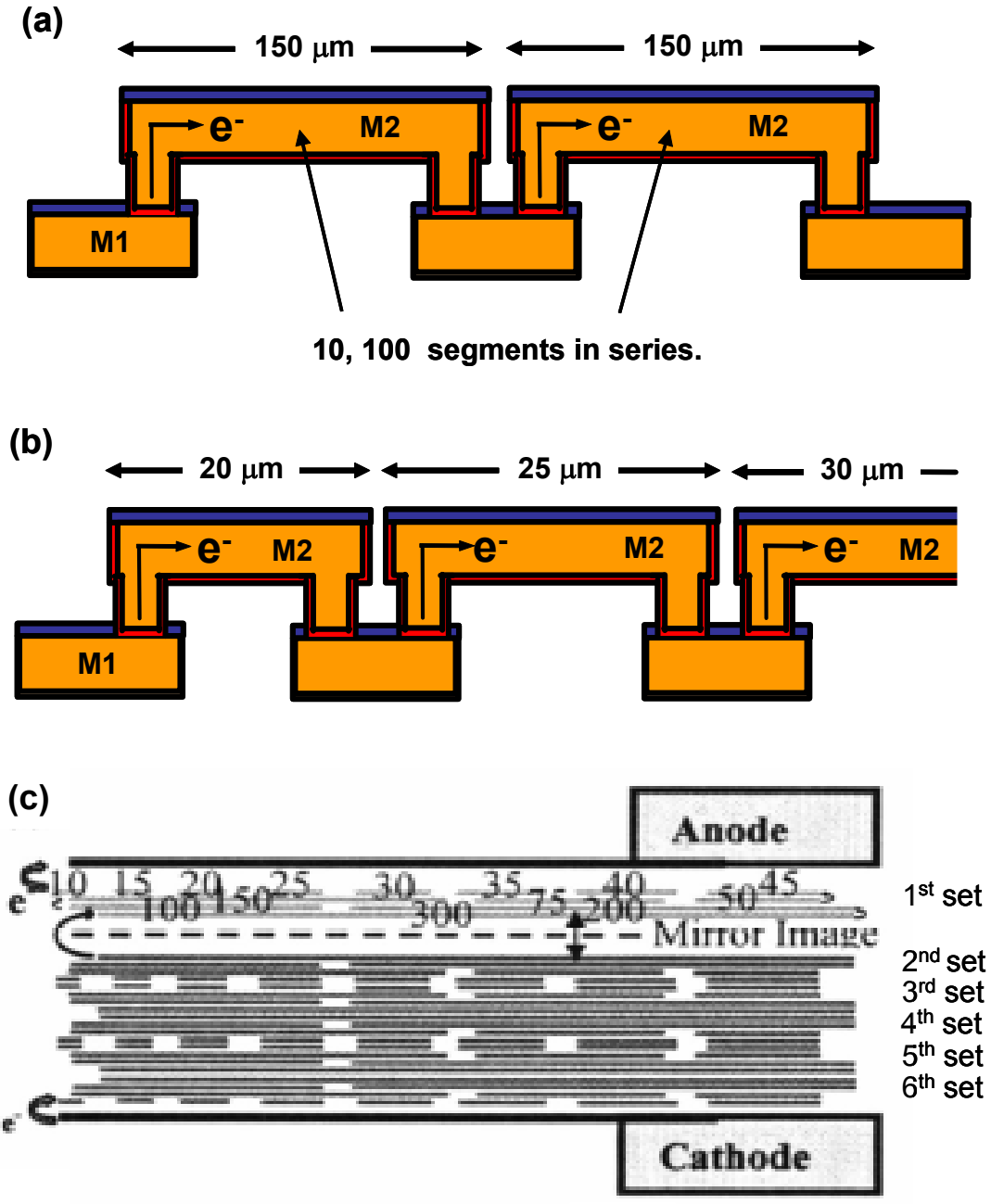

Figure 2.3 Schematics of (a) side view of early failure (EF) EM test structure, (b) side view of critical length (LC) EM test structure, and (c) top view of critical length (LC) EM test structure for up-current EM test condition.

Figure 2.4 shows one of the EM testing modules with up-stream electron flow condition. The module is 2 mm long and 0.5 mm wide. For this particular module, 24 bonding pads (12 by 2) and 4 EM test patterns are arranged. Hence, a maximum of 6 bond pads can be assigned to each test pattern. Since the inter-layer dielectric (ILD) material is porous low-k, which is susceptible to water and oxygen, a guard ring was implemented along the outside of bonding pads. 0.85 μm wide dummy M2 lines, so called extrusion monitoring lines, were inserted on each side of the stressing M2 line for detecting extrusion failure at the anode. With the dummy lines, the uniformity of chemical mechanical polishing (CMP) can be improved by reducing the dishing issue usually observed on mechanically weak low-k dielectric.

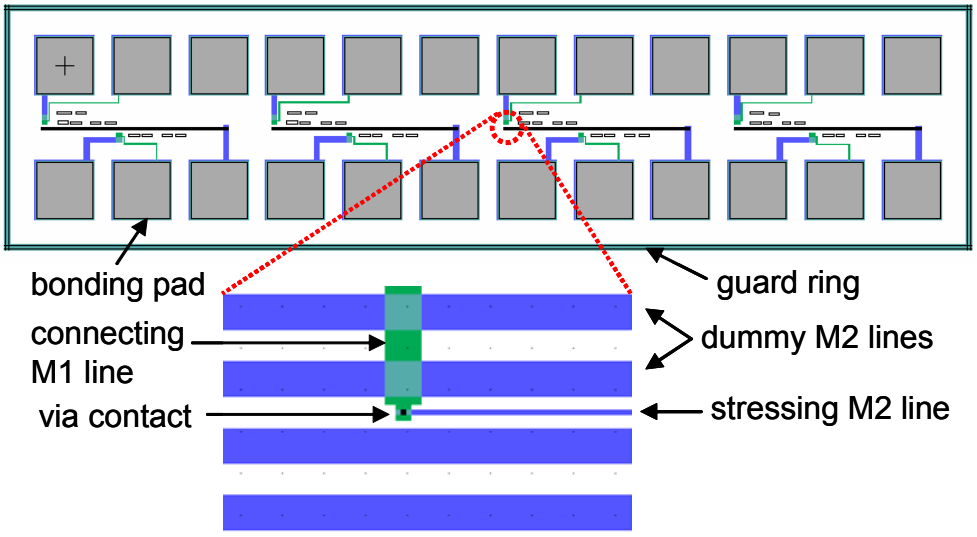

Figure 2.4 EM testing module showing a guard ring, bonding pads, and EM test patterns. An enlarged view shows EM test lines and wide dummy lines. Blue, green, and black correspond to the color of M2 line, M1 line, and via, respectively.

2.2 WAFER FABRICATION AND EM TEST

Based on the designs described so far, test samples were fabricated on 300-mm wafers using a dual-damascene process at SEMATECH. The inter-layer-dielectric (ILD) materials used for the study were porous MSQ low-k dielectric with k ~ 2.3, and silicon oxide with k ~ 3.9. The patterned wafers were diced to fit onto a ceramic package. The individual dies were attached on a ceramic package using silver paste, and then cured at 350 ℃, for 30 minutes in a vacuum oven. A packaged test structure was electrically connected to a ceramic package by wire bonding. A wedge bonder with 25 μm thin Al-1%Si wire was used for the wire bonding. The wire bonded packages were inserted in the lead frame sockets in the EM chamber.

The schematic of the wire bonding connections is shown in Figure 2.5. The ceramic package used for this study is a 16-pin side braze package from the Kyocera Corporation. Normally two test patterns were attached to a package. The upper test structure was controlled by the upper five channels on the package, and the lower test structure was controlled by the lower five channels. Blue lines represent Al wires. Constant current was generated by a constant current controller sent through the EM test structure, and the current was monitored between the I- and I+ channel. Since constant current was applied to the EM structure regardless of the resistance of EM structure, the voltage between V- and V+ increased with increasing resistance due to EM-induced voiding. EM resistance change was deduced using the voltage changes and the constant current applied to the EM test pattern. In addition, voltage change between V- and V^{ex} was monitored to detect EM sample failure by Cu extrusion at the anode.

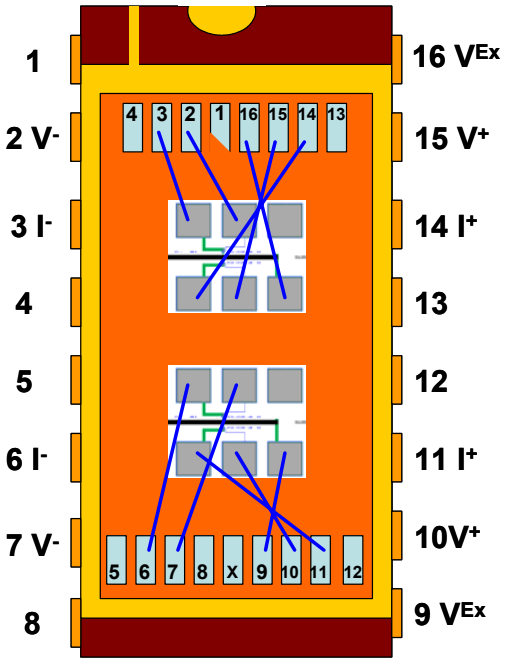

Figure 2.5 Schematic of 16-pin side braze package with two EM samples and wire bonding configuration for package-level EM test.

As shown in Figure 2.6, EM testing was performed in a vacuum chamber in a pure nitrogen environment at 20 torr. Up to 64 samples can be tested in the chamber at a time. Two heating coils were installed in the chamber. The primary heating coils located at the top and bottom plate are used to set the target test temperature. The secondary heating coils located at chamber sidewall are used to significantly reduce the temperature gradient in the chamber. The current regulator maintained the constant current density condition during the EM tests. A switching box (Keithley 7002 Switch System) selected the channel of the sample under test in sequence. A DMM (Keithley 2000 Multimeter) measured the voltage value of each channel. A PC system controller equipped with National Instruments LabView controlled data acquisition and data analysis.

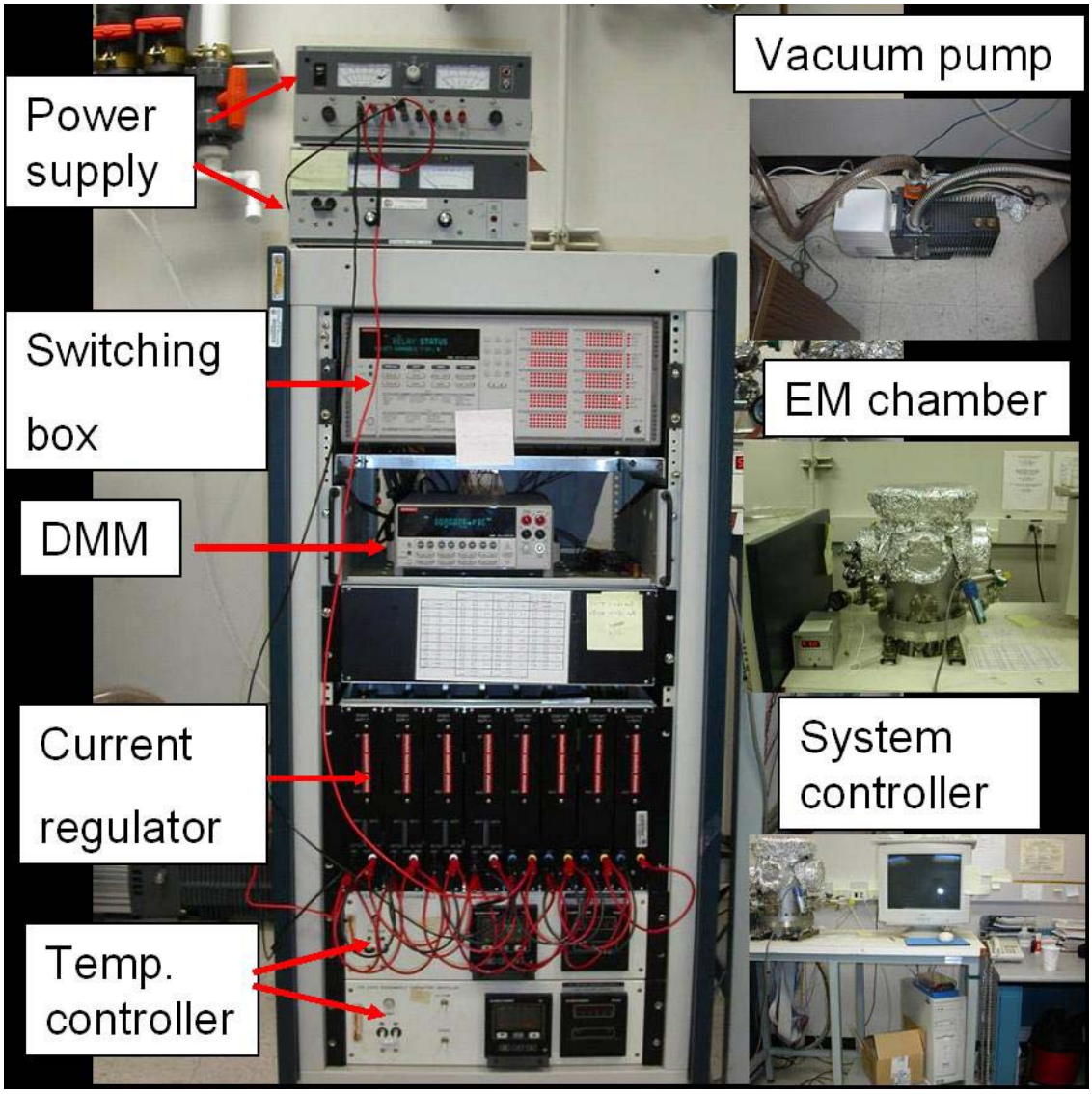

Figure 2.6 Package-level EM testing system.

Most of EM tests were performed at a current density of 1.0 MA/cm^2. The actual current value that passed through the samples was calculated by assuming uniform metal width and height. For example, the EM current for the finest lines in this study - 60 nm in width and 150 nm in height - was approximately 90 μA. To do the accurate EM testing,

the current regulator was upgraded to improve on the stability and small current sources capabilities. The measured current stability of the upgraded current regulator was 90 ± 0.001 μA for the 60-nm wide lines.

The chamber temperature was ramped up at 3 ℃/min to the target temperature. Resistance increase due to void formation was monitored to determine the EM lifetime. The time at the first appreciable line resistance increase (usually ~10 %) was taken as the EM lifetime. EM experiment was terminated after all samples failed. Some EM experiments were stopped right after EM resistance increase in order to observe EM voiding; otherwise, EM-induced void could not be found due to the severe joule heating. The observation of microstructure and EM-induced voids was performed by a transmission electron microscope (TEM) and a focused ion beam (FIB) microprobe.

2.3 MEASUREMENT OF $(jL)_C$ PRODUCT

In order to obtain a $(jL)_c$ product experimentally, the multi-linked statistical structures shown in Figure 2.3 (c) were tested under specific test conditions. After the test, EM-induced voids at the cathode end were monitored using an optical microscope. The observed image is shown in Figure 2.7 where the fine stressing lines were located between the wide extrusion monitoring lines. The cathode voids were found either at or nearby the cathode end. Since 6 repeating sets of multi-linked structures were included in a LC structure, 120 interconnects of each line length ranging from 10 to 300 μm were tested at one time when 20 samples were loaded in the EM chamber. This arrangement provided enough data to determine the $(jL)_c$ product.

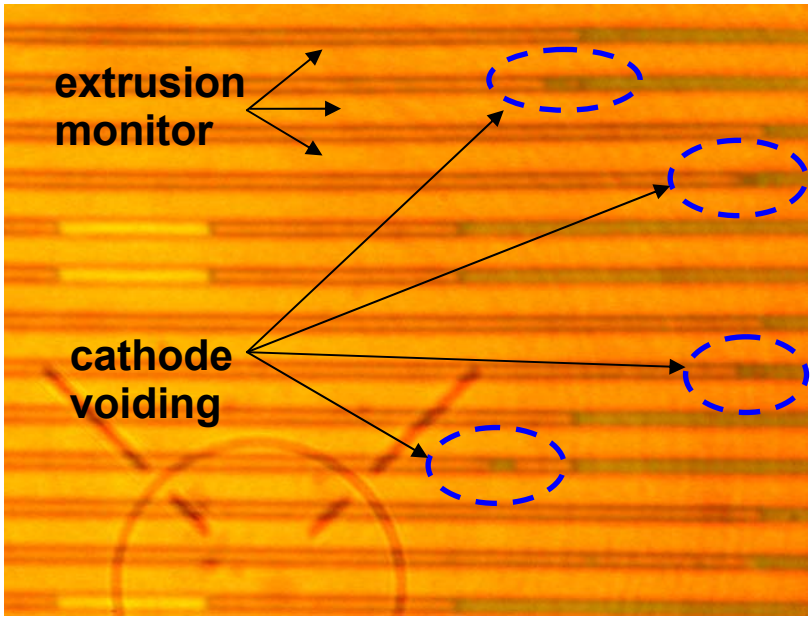

Figure 2.7 Optical microscope image showing EM-induced voiding around cathode end for a statistical multi-linked EM test structure. The stressing fine lines are located between the wide extrusion monitoring lines. The EM test was performed at 330 ℃, with a current density of 1.0 MA/cm^2.

The entire set of EM tested lines were inspected, and the number of fails normalized by the total number of the given line lengths were plotted as shown in Figure 2.8. It was assumed that each metal line was failed by open circuit when a void was found at the cathode end. As expected, the probability of void formation decreased with the decreasing line length due to increasing back-flow stress gradient in the shorter lines. Eventually, no void was found for the lines shorter than 20 μm.

In order to determine the $(jL)_c$ product value, statistical analysis was performed and the resulting regression curve was superimposed as shown in Figure 2.7. Assuming that the probability of interconnect failure under EM driving force for a given line length, L_i, and current density, j, is proportional to its average drift velocity, the failure probability, P(j,L_j) can be expressed as [26,50]

$$P(j,L_i) = C\left[\frac{v_d(j,L_i)}{v_d(j,L_M)}\right] = C\left[\frac{1-L_c/L_i}{1-L_c/L_M}\right], \qquad \text{for } L_i \geq L_c, \qquad (2.1)$$

$$= 0, \qquad \text{for } L_i < L_c, \qquad (2.2)$$

where v_d is the average drift velocity for Cu ions at a given j and L under a steady-state back stress condition, L_M is the length of the longest interconnect in the test structure (i.e., 300 μm), L_c is the critical length, and C is a normalization constant.

The normalized number of fails can be deduced from Equation (2.1)

$$\frac{P(j,L_i)}{C} = \left[\frac{1-L_c/L_i}{1-L_c/L_M}\right]. \qquad (2.3)$$

The regression fitting based on the Equation (2.3) shows that the critical length, L_c is approximately 20 μm. With a current density of 1.0 MA/cm^2, the statistical $(jL)_c$ product for this sample was approximately 2000 A/cm.

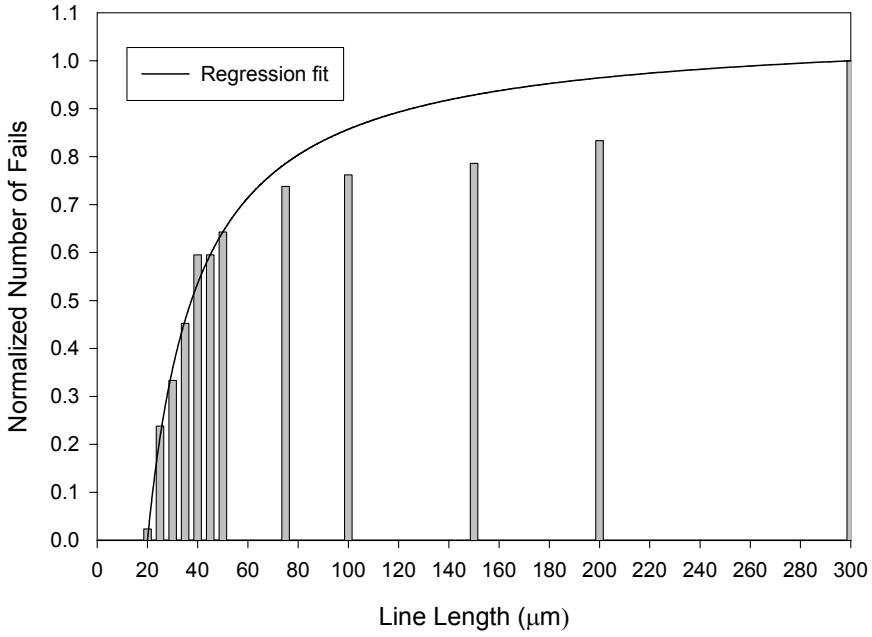

Figure 2.8 A plot of normalized number of fails as a function of line length for Cu/low-k interconnects and the matching regression fitting on the experimental results. The EM test was performed at 330 ℃ at a current density of 1.0 MA/cm^2. The probability of EM failure decreased with decreasing line length. The critical length was 20 μm, and $(jL)_c$ product was approximately 2000 A/cm.

2.4 RESISTANCE CHANGES DURING EM TEST

EM resistance changes were monitored using an electronic system controlled by PC to determine lifetime and to help identify the failure mechanism. Basically, three types of resistance changes during EM testing were observed depending on the test structure and the location of EM-induced void [59].

The three types of resistance changes are shown in Figure 2.9. An abrupt resistance increase followed by a gradual resistance increase as shown in Figure 2.9 (a) is a typical resistance change for single-linked EM structure under up-current electron flow condition. The lifetime (t_f) for this type of resistance change was determined at the time of the abrupt resistance increase. Such an abrupt resistance increase occurs when an EM-induced void forms and grows large enough to occupy the whole M2 trench. Then the EM current is shunted to Ta barrier which has a higher resistivity than that of Cu [36]. After that, the void continues to grow towards the anode until the line burns out due to severe joule heating. The gradual resistance increase can be attributed to void growth induced by EM driving force.

Abrupt resistance increase shown in Figure 2.9 (b) was found to be a via-related failure. For a down-current electron flow condition, once a void forms underneath the via, the resistance increases abruptly because there in no redundant Ta barrier to bypass the EM current around the void. Occasionally, the abrupt resistance increase was found under up-current electron flow when a process-induced defect is involved in the interconnect failure. The last resistance trace is a step-like increase, which was found for the multi-linked test structure. With electron flow through the interconnect, void formation in each line contributed to the resistance increase of the multi-linked structure. Eventually, the resistance increased to infinity and the line failed due to severe joule heating [29].

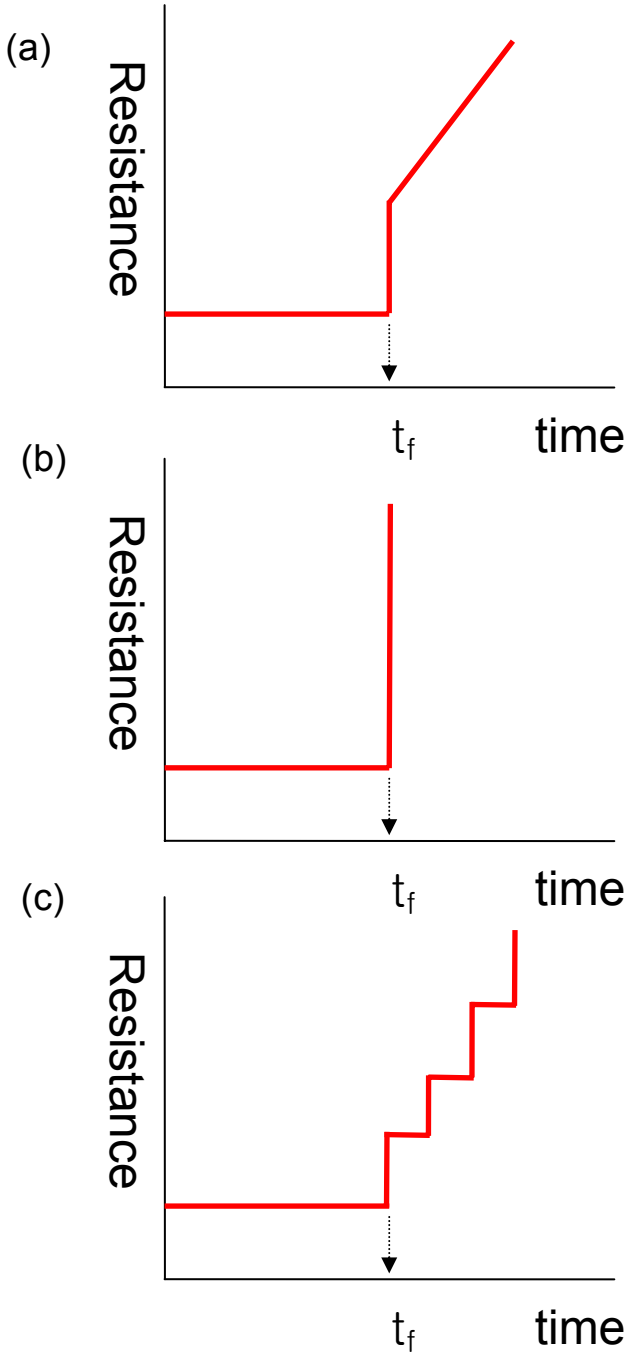

Figure 2.9 Resistance traces for Cu interconnects including (a) typical gradual resistance increase, (b) abrupt resistance increase, and (c) step-like resistance increase.

Chapter 3: Barrier Process Effect on Electromigration Reliability of Cu/low-k Interconnects

In this chapter, the electromigration (EM) reliability of Cu/low-k interconnects fabricated using a conventional pre-clean first process and an advanced barrier-first process are discussed. Compared with the pre-clean first process, extrinsic early failures were not observed using the barrier-first process. This suggests that process-induced defects, which are the most probable cause of early failures, were significantly reduced with the barrier- first process. Transmission electron microscopy (TEM) demonstrated a more uniform and thicker Ta barrier for the barrier-first process than the pre-clean first process. This led to a higher $(jL)_c$ product and prolonged EM lifetime accordingly. In addition, the pre-deposited Ta barrier during the barrier-first process protected the mechanically weak low-k dielectrics from plasma etch damage, resulting in a uniform via profile. In contrast, the via opening at the top was found to be larger than at the via bottom for the pre-clean process. The uniform via profile is another advantage of the barrier-first process from the point of view of process control.

3.1 INTRODUCTION

With the implementation of low-k dielectrics in Cu damascene interconnects, the Ta barrier formation process has become important in preventing Cu diffusion into the adjacent dielectrics. Continuous shrinkage of device features necessitates the accompanying reduction of the barrier thickness, while maintaining the required performance as a diffusion barrier and adhesion promoter. Significant efforts have been expended on developing novel barrier materials and process technologies to satisfy these requirements [60-62].

As shown in Figure 3.1, in a conventional dual-damascene process scheme, known as the pre-clean first process, the barrier layer is deposited after the Ar sputter pre-clean to remove Cu oxide and the dry etch residues. Low-k dielectrics, being mechanically weak, are more prone to plasma damage during the pre-clean process. In addition, Cu oxide or etch residues removed from the via bottom may redeposit on the via sidewall, thereby degrading reliability [63]. In contrast, the barrier-first process has been demonstrated to alleviate these problems [64]. The barrier-first process reduces the critical dimension (CD) loss and minimizes copper contamination, which was an issue in the pre-clean process. In addition, low-k dielectric is protected from Ar plasma damage during Ar etchback by the first-deposited barrier layer.

The improvement in via resistance, inter-level dielectric (ILD) reliability, via stress migration (SM) and electromigration (EM) with the barrier-first process compared with the conventional pre-clean first process was first reported by G.B. Alers *et al* [64]. However, a systematic study of the barrier-first process effect on EM has not been reported. In this chapter, the effect of the barrier-first process on EM reliability was investigated, and the results were compared to those of the conventional pre-clean first

process. In addition, the effect of Ta barrier thickness on EM using the barrier-first scheme was studied. To determine both the critical current density and line length product $(jL)_c$ and early failure statistics, multi-linked EM test structures were built and utilized.

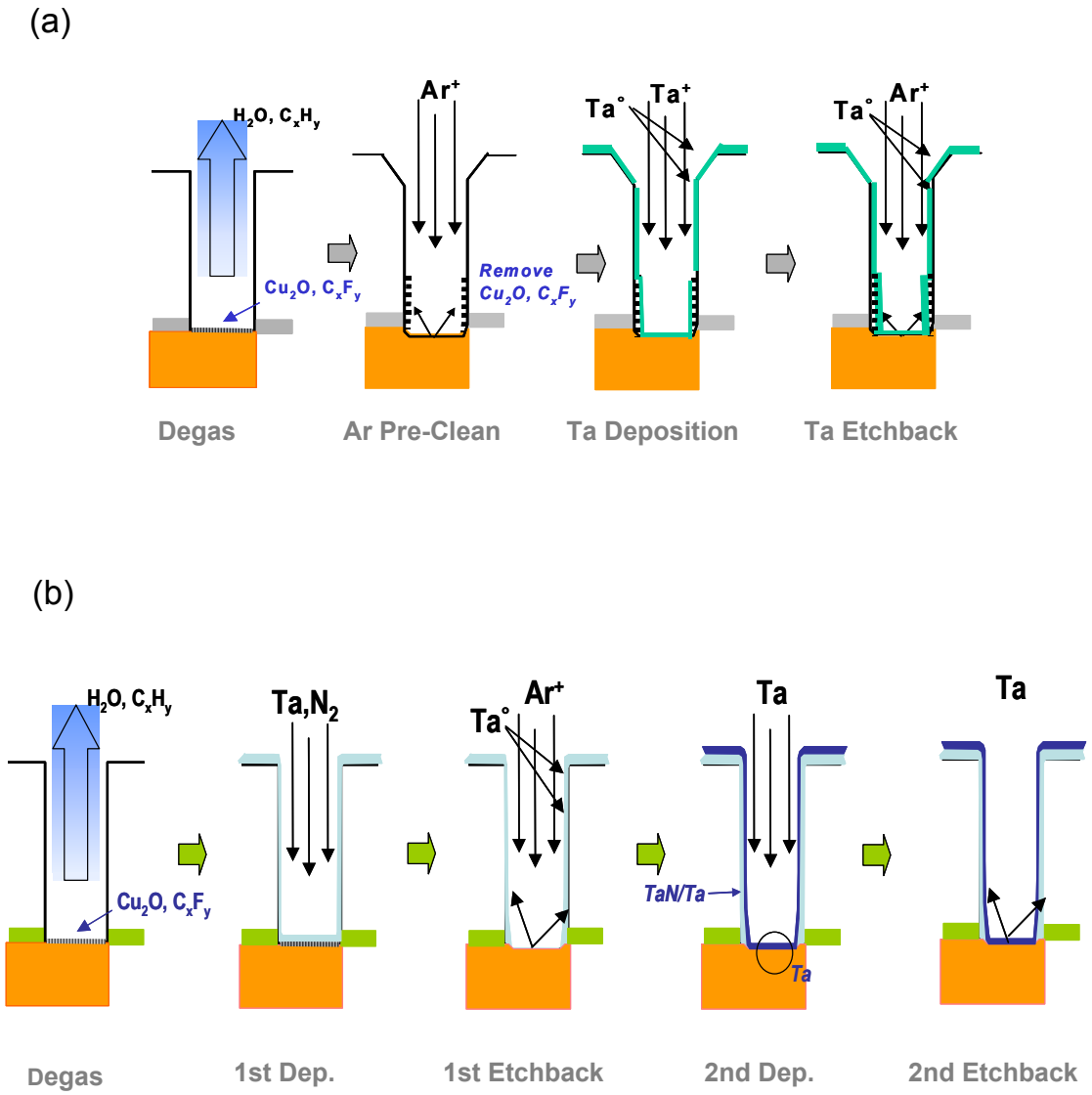

Figure 3.1 Schematics of (a) the conventional pre-clean first process, and (b) the barrier-first process [64].

Table 3.1 Summary of process flow for Ta barrier deposition using the pre-clean first and the barrier-first scheme.

Pre-clean first	Barrier first	Advantage of barrier first
Via open ↓ ***Preclean*** ↓ Barrier deposition ↓ ↓ ↓ Cu seed deposition ↓ Cu electrofill	Via open ↓ ***Barrier deposition*** ↓ RF resputtering ↓ 2nd Barrier deposition ↓ Cu seed deposition ↓ Cu electrofill	- Reduces CD loss - Improve barrier coverage - Fully compatible with low k dielectric - Reduces Ar ion damage

3.2 EXPERIMENTAL DETAILS

Test samples were fabricated at Sematech using a dual damascene process scheme. The low-k Intermetal Dielectric (IMD) layer was porous methylsilsesquioxane (MSQ), a spin-on organosilicate material with k ~2.3. Three types of Ta barriers were integrated at the M2 and via levels. The three splits included a pre-clean first scheme, a thin barrier-first scheme, and a thick barrier-first scheme. The integration procedure at the M1 level was identical for all three splits. Electromigration experiments were performed in a vacuum chamber with a pure nitrogen environment at 20 torr. Changes in resistance as a function of time were measured and recorded. From the lifetime data, the cumulative failure distribution (CDF) was obtained as a function of time. Then, Monte Carlo simulation was performed to fit CDF curves to fit the data for the entire time span. The parameters deduced from the fit were used to determine the probability of early failure

and to separate out the weak mode distribution from the strong mode. To derive the statistical $(jL)_c$ products for each split, void distributions were determined as a function of line length of the EM-failed samples using an optical microscope. The analysis of microstructure including Ta barrier morphology and electromigration-induced voids was performed by a transmission electron microscope (TEM) and a focused ion beam (FIB) microprobe.

3.3 RESULTS AND DISCUSSION

3.3.1 Early Failure Behaviors for Different Barrier Processes

The CDF as a function of time is shown in Figure 3.2 for the sample with the pre-clean first process (a) and thin barrier-first process (b). For reference, the barrier thicknesses of the various processes were obtained from TEM images and are plotted in Figure 3.6. For the pre-clean first samples, bi-modal failure distribution was observed indicating that two different EM failure mechanisms were involved. The probability of early failure derived using Monte Carlo simulation was 0.15 %. This indicated that about 1.5 interconnects out of 1000 will fail due to an extrinsic failure mode. In contrast, the CDF for the barrier-first process demonstrates a mono-modal failure distribution for all the line segments examined. It was projected that process-induced defects in the via bottom, which are a primary cause of early failures, are significantly reduced by the barrier-first process, ultimately improving EM reliability. In comparison, the pre-clean first process was affected by process-induced defects. For example, Cu contamination, caused by sputter etch pre-clean, degraded Ta barrier adhesion at via sidewall [64].

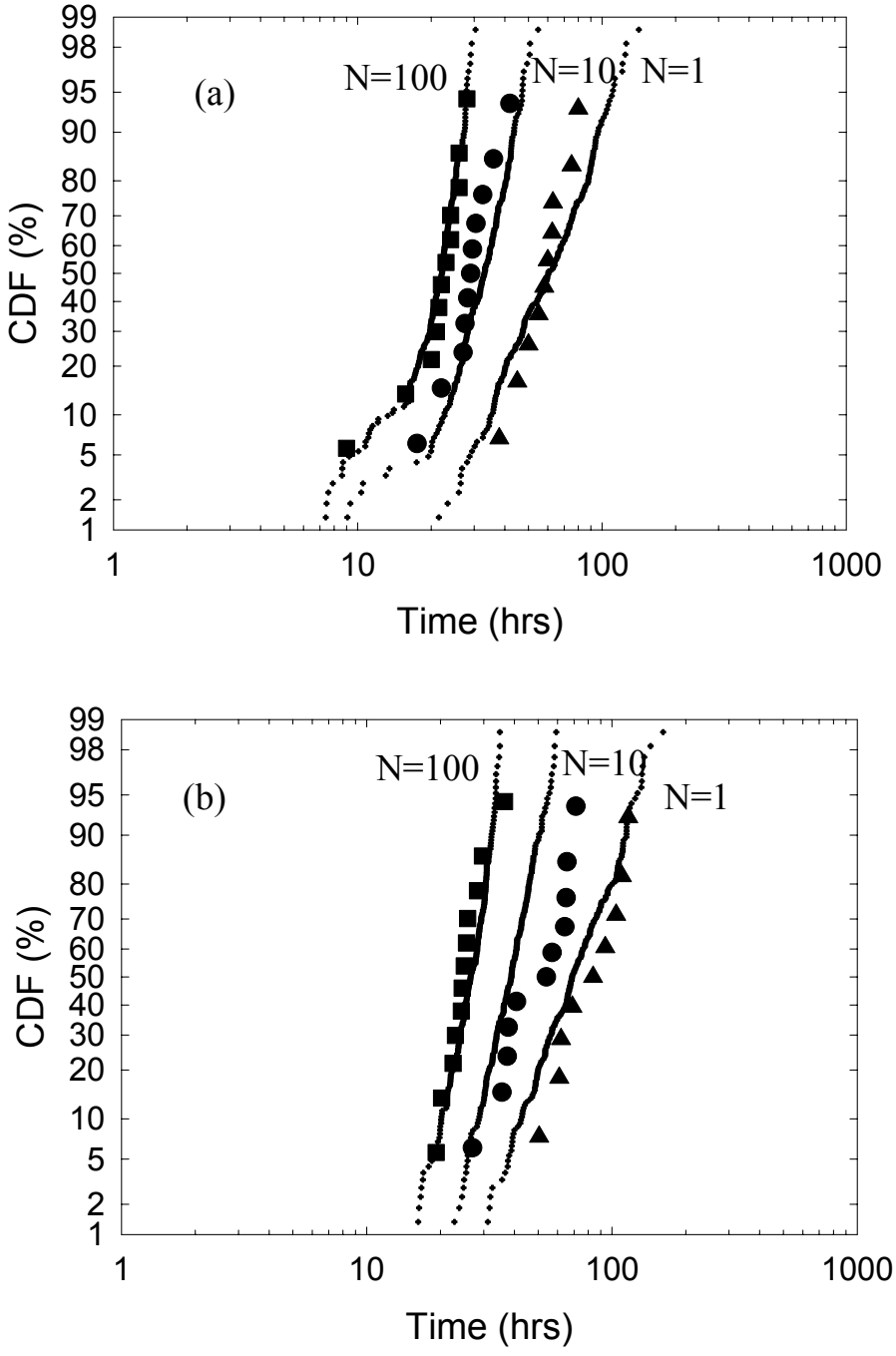

Figure 3.2 CDF plots of EM test results using Early Failure test structures with a pre-clean first process (a) showing bi-modal failure distribution, and (b) a barrier-first process showing the mono-modal failure distribution, indicating the improvement in EM reliability.

3.3.2 Observation of Microstructure Using TEM

The TEM images shown in Figure 3.3 support our interpretation of the early failure EM test results. The images clearly show the different via bottom and sidewall morphologies between the two processes. For example, the degree of via recess into the M1 is more significant in the pre-clean first process than the barrier-first process. Such a recess, attributable to the Ar plasma pre-clean, creates a notch-shaped contour as shown in Figure 3.3(a), which can increase stress concentration to exacerbate a stress-induced delamination problem under high temperature EM test conditions. This can lead to an extrinsic failure, which was not an important issue with the barrier-first process as shown in Figure 3.3 (b). The fuzzy interface of the Ta barrier shown in Figure 3.3 (a) most likely developed during the Ar plasma pre-clean, which caused damage and roughness of the low-k surface at the via sidewall. The uneven low-k surface in turn affected the Ta barrier deposition that followed.

A thin, outdiffused metal layer thought to be the Ta barrier material was found in the high resolution TEM micrograph shown in Figure 3.3(a). Copper diffusing out through a thin and uneven Ta barrier is one possible mechanism for an extrinsic early failure [65-67]. In addition, the reduced confinement effect due to the uneven and thinner Ta barrier for the pre-clean can lead to a lower $(jL)_c$ product and EM lifetime.

The via profiles shown in Figure 3.3 help explain other differences between the two processes. For the pre-clean process, the via opening at the top is larger than at the via bottom while the difference was less distinct with the barrier-first process. The uneven via profile may not affect EM reliability directly. However, it is not desirable for reducing leakage current and controlling critical dimension (CD). A large opening at the top of the via developed because the mechanically weak low-k dielectric was exposed to the Ar plasma during the pre-clean process. Such plasma etch damage was minimized in

the barrier-first samples because the pre-deposited Ta barrier protected the low-k dielectric from plasma exposure.

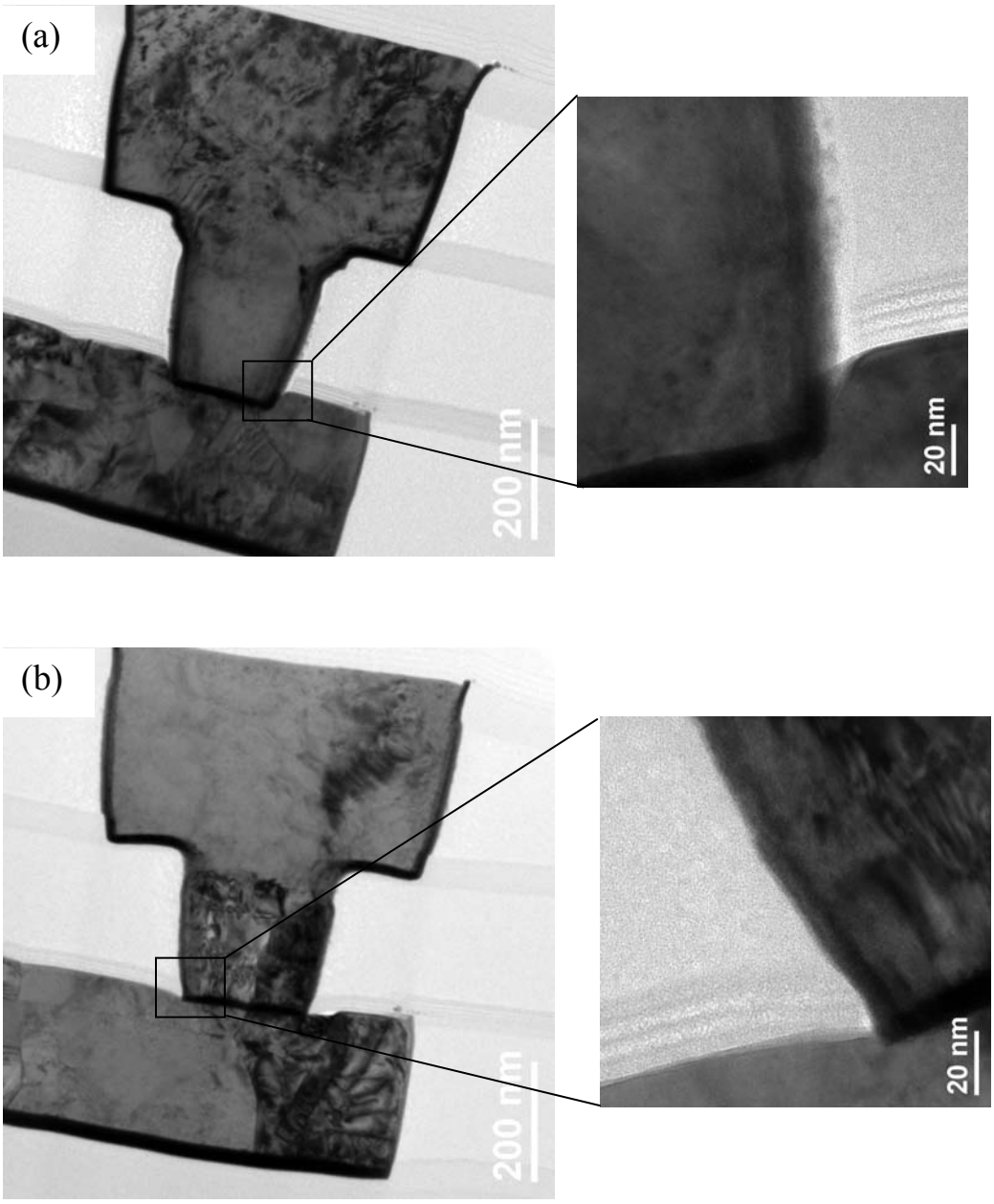

Figure 3.3 Cross-sectional transmission electron microscopy (TEM) images showing Cu/low-k interconnects fabricated by dual damascene for different barrier processes: (a) pre-clean first process, and (b) thin barrier-first process.

3.3.3 Barrier Process Effect on $(jL)_c$ Product

Voids from the EM-tested samples were searched under an optical microscope. The results were expressed in terms of the probability of void formation as shown in Figure 3.4 for a given line length for various line lengths and barrier processes. The probability for a given line length was obtained by dividing the number of lines having void by the total number of lines. For the pre-clean first process, voids were found in most of the metal lines longer than 75 μm, and the probability of void formation rapidly decreased in lines shorter than 75 μm. However, for the barrier-first process, the probability of void formation was only about half or less compared with the pre-clean first process. With increasing barrier thickness, the probability of void formation decreased further. This is related to the time to reach steady state, under which EM driving force is balanced by back-flow stress and the void growth saturates, compared with the time to fail the test structures [18]. These results suggest that the barrier process and barrier thickness significantly affected void formation in metal lines and will be reflected in the value of the $(jL)_c$ product as discussed below.

To determine $(jL)_c$ product for the different barrier processes, the normalized number of fails were plotted as a function of line length and the results are shown in Figure 3.5. Here, the regression fittings using Equation 2.4 were superimposed on the experimental plots.

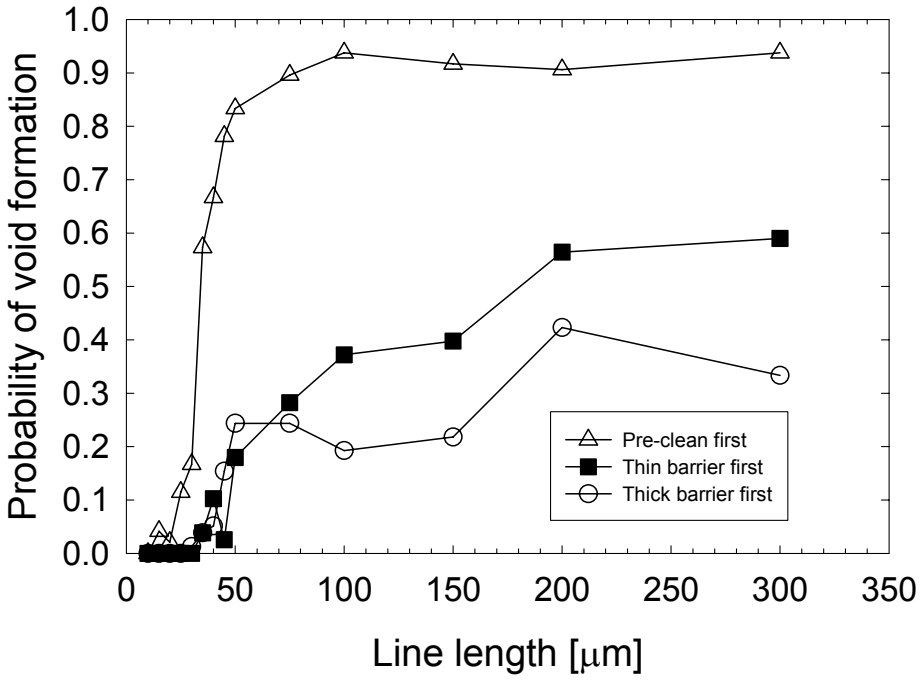

Figure 3.4 The probability of void formation as a function of M2 line length for the different barrier processes. The probability of void formation was calculated by dividing the number of lines with voids by the total number of lines. The EM test was performed at 330 ℃, with a current density of 1.0 MA/cm^2.

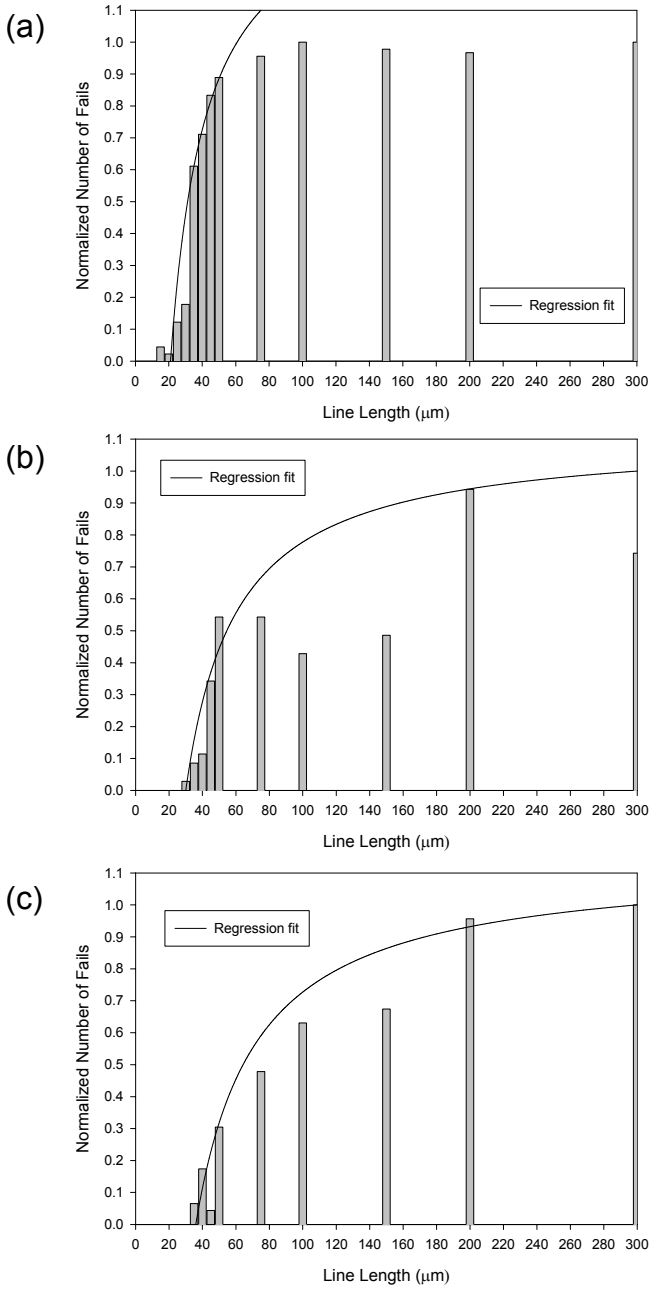

Figure 3.5 Plots of normalized number of fails as a function of line length for Cu/low- k interconnects with (a) pre-clean first, (b) thin barrier-first, (c) thick barrier first process. The EM test was performed at 330 ℃, with a current density of 1.0 MA/cm^2.

The $(jL)_c$ products for the pre-clean first, thin barrier-first, and thick barrier-first were about 2100, 3000, and 3500 A/cm, respectively as shown in Figure 3.6. The $(jL)_c$ product was higher with the barrier-first process than the pre-clean first process as expected. The difference in the $(jL)_c$ product can be attributed to the barrier thickness. The barrier thicknesses of the M2 trench sidewall obtained from TEMs of the different barrier process are superimposed on the $(jL)_c$ product in Figure 3.6.

It was also demonstrated that the increased barrier thickness resulted in an increased effective modulus leading to a greater confinement effect on the Cu/low-k interconnects. The results suggest that the Ta barrier at the trench sidewall provided the necessary confinement for the Cu lines even if they were surrounded by the weak low-k dielectric. As shown in Figure 3.6, the barrier- first process resulted in increased barrier thickness and improved $(jL)_c$ product.

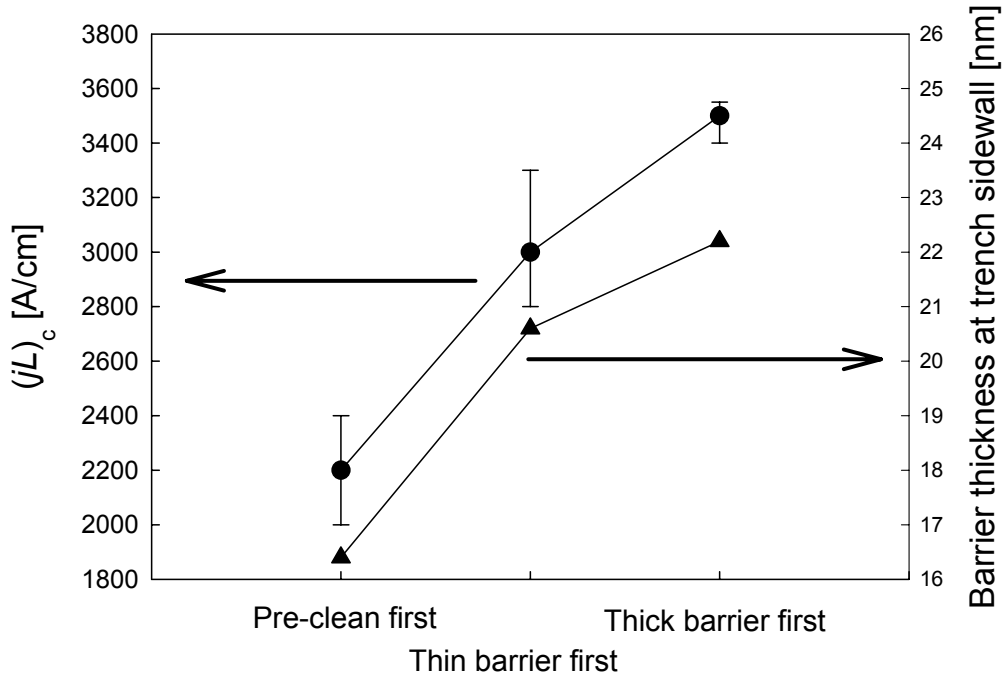

Figure 3.6 Plot of the statistically measured $(jL)_c$ product and the measured barrier thickness using TEM for different barrier processes. The $(jL)_c$ product shows good correlation with barrier thickness at the trench sidewall.

The net drift velocity (v_d) is the combination of drift velocity induced by EM stress (v_{EM}) and drift velocity induced by back-flow stress (v_{BF}), which can be expressed as [31],

$$(v_d) = (v_{EM}) + (v_{BF}) = \mu\,(Z^* e \rho j - \Omega \Delta\sigma / L) \qquad (3.1)$$

where μ is the effective mobility, Z^* is the effective charge, e is the electronic charge, ρ is the electrical resistivity, j is the current density for EM, Ω is the atomic volume, and $\Delta\sigma/L$ is the EM-induced back-flow stress gradient along the metal line. With increasing barrier thickness, the back-flow stress gradient increases for a given length (L) due to the

high elastic modulus of the Ta barrier. This leads to a high drift velocity associated with the back-flow stress (v_{BF}) and reduces the net drift velocity (v_d).

It is widely known that the dominant diffusion path for Cu interconnects is the interface between the copper and the capping layer. In this case, the EM life time can be simplified as [36]

$$\tau = \Delta L_{cr} / v_d \qquad (3.2)$$

where τ is the intrinsic EM lifetime induced by surface diffusion, ΔL_{cr} is the critical void length for line failure, and v_d is the net drift velocity. Since identical test structure for different barrier process splits was used, ΔL_{cr} was identical. Therefore, the EM lifetime was inversely proportional to the EM drift velocity.

From equations (3.1) and (3.2), It can be deduced that the EM lifetime is proportional to the $(jL)_c$ product. This relationship is borne out in the CDF plots for different barrier processes as shown in Figure 3.7. Therefore, the shorter EM lifetime for the samples that underwent the pre-clean first process, compared with the barrier-first process, can be correlated to the smaller $(jL)_c$ product.

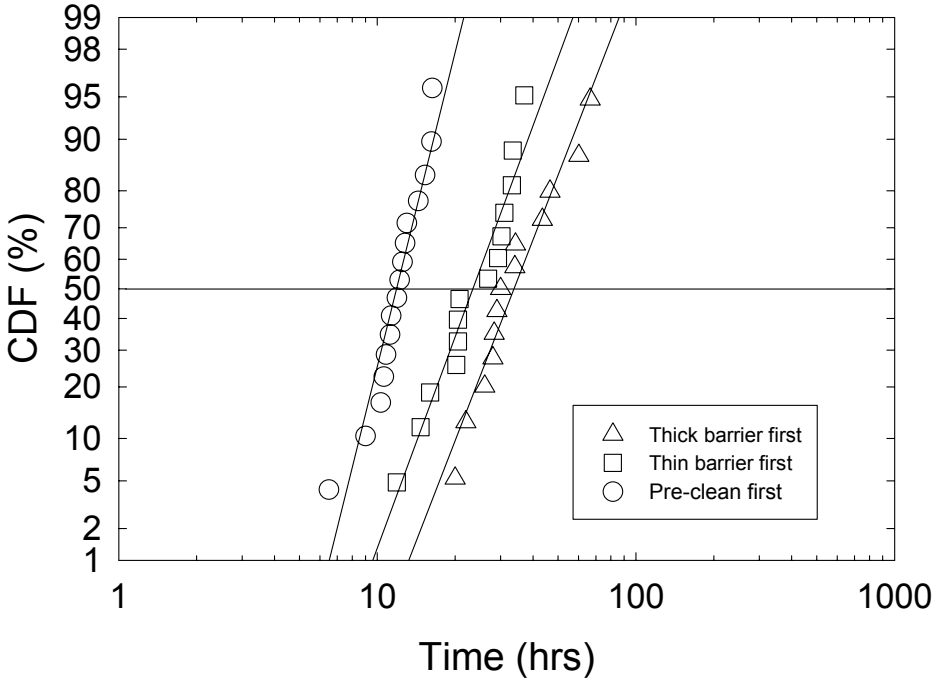

Figure 3.7 Cumulative failure distribution (CDF) plots of LC structures with different barrier processes for upstream electron flows. The EM test was performed at 330 ℃, with a current density of 1.0 MA/cm^2.

3.4 SUMMARY

The effect of the barrier process on the electromigration reliability of Cu/low-k interconnects has been investigated. Compared with a conventional pre-clean first process, extrinsic early failure was not observed in the samples with the barrier-first process. This result suggests that process-induced defects, which were the most probable cause of the early failures, were significantly reduced with the barrier-first process. In addition, TEM micrographs revealed that a more uniform and thicker barrier layer was found at the via and trench with the barrier-first process than with the pre-clean first process. The pre-deposited Ta barrier protected the mechanically weak low-k dielectrics,

leading to uniform via profiles, while via erosion was found after the pre-clean first process due to Ar plasma damage of the dielectric. The $(jL)_c$ product correlated well with the barrier thickness at the trench sidewall. TEM micrographs revealed that the barrier thickness at the M2 trench sidewall was thicker with the barrier-first process than with the pre-clean first process, leading to a higher $(jL)_c$ product. This high $(jL)_c$ product effectively increased the drift velocity induced by back-flow stress (v_{BF}), thus reducing the net EM drift velocity (v_d). The reduced net drift velocity prolonged the EM lifetime which was inversely proportional to the net drift velocity, assuming that the interface between the Cu and capping layer was the dominant diffusion path for Cu/low-k interconnects fabricated by a dual damascene process.

Chapter 4: Barrier Thickness Effect on Electromigration Reliability of Cu/low-k Interconnects

The importance of barrier process for EM reliability was described in Chapter 3. The effects of Ta barrier thickness with identical barrier process on electromigration (EM) reliability of dual-damascene Cu/porous low-k interconnects is discussed in this chapter. With decreasing Ta barrier thicknesses, the threshold product of current density and line length $(jL)_c$ was found to be reduced due to less structural confinement by thinner barriers. The effect will be accounted for by the effective modulus (B) of the structure. Results from the early failure test structures revealed a bi-modal failure distribution for the samples with 75 Å and 100 Å barriers. Focused ion beam (FIB) microprobe and transmission electron microscopy (TEM) observations revealed that the weak-mode early failure was caused by Cu out-diffusion through structural defects in the thin Ta barrier.

4.1 INTRODUCTION

With continued device scaling, electromigration (EM) remains a major reliability concern for copper interconnects, particularly with the implementation of porous low-k dielectrics. In Cu damascene interconnects, EM was found to be dominated by mass transport at the Cu/cap layer interface [67,68]. This has stimulated great interests recently to develop metal overcoating, such as CoWP, to reduce interfacial diffusion for improved EM reliability. With this approach successfully demonstrated, the barrier layer became important in controlling Cu EM reliability. The barrier is an integrated part of the damascene interface contributing significantly to the thermomechanical confinement of the low k structure to sustain EM mass transport. It also serves as a base layer for Cu seed deposition and electroplating, where processing defects in the barrier can induce early failure to degrade EM reliability [12,52]. The effects of barrier confinement and processing defects on EM reliability became an increasing concern with further scaling of barrier thickness for porous low k dielectrics.

In this chapter, the effects of barrier thickness on EM reliability for Cu interconnects with porous low-k dielectrics are investigated. The effect of barrier thickness scaling on the $(jL)_c$ product was first examined. This was followed by a study of the barrier thickness effect on EM characteristics, focusing on early failure statistics and degradation mechanisms.

4.2 EXPERIMENTAL DETAILS

A porous methylsilsesquioxane (MSQ) material with effective permittivity, k of 2.3 was used as the interlayer dielectric. Two types of dual-damascene statistical EM test structures were used in this study, which were fabricated at Sematech and designed to measure the critical length-current density product $(jL)_c$ and early failure statistics. Three Ta barrier thicknesses of 75 Å, 100 Å, and 175 Å corresponding to the 65 nm, 90 nm and 130 nm nodes, respectively, were integrated at the M2 level to examine the barrier thickness scaling effect. To delineate the barrier thickness from the line width effect, results reported here were all obtained using test structures with the same line width. The experiments were carried out in a test chamber vacuumed and backfilled with nitrogen to 20 torr. The first appreciable line resistance increase (usually ~10 %) was used to define the time to failure.

4.3 RESULTS AND DISCUSSION

4.3.1 Barrier Thickness Effect on $(jL)_c$ Product

To investigate the barrier confinement effect, the $(jL)_c$ product was measured by the critical length (LC) test structures as a function of barrier thickness. All the results reported here were for up-stream current with electron flow from the M1 to the M2 level. This arrangement forced failure to occur on the M2 level, which could be detected using a voltage contrast method in a scanning electron microscope or optical microscopy. The EM tests were performed at 310 ℃ and a current density of 1.0 MA/cm^2. The $(jL)_c$ product was determined from the statistical results of the failure probability versus line length. The results with various barrier thicknesses are shown in Figure 4.1.

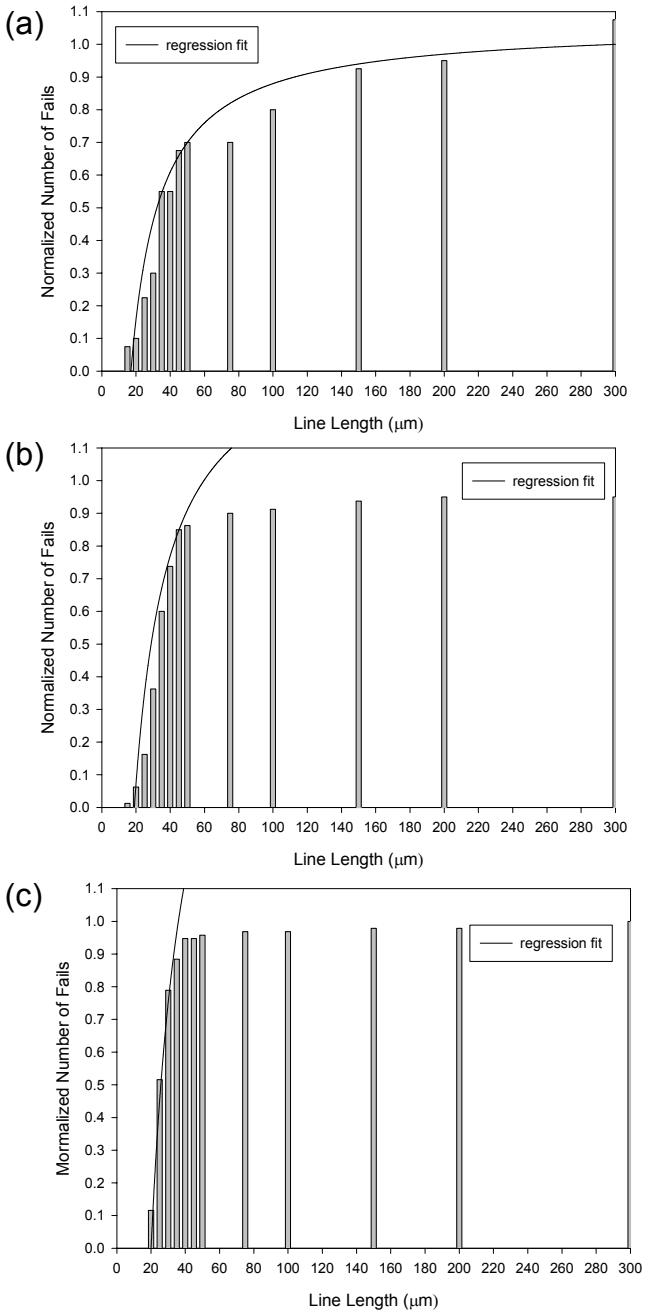

Figure 4.1 Plots of normalized number of fails as a function of line length for Cu/low- k interconnects with Ta barrier thickness of (a) 75, (b) 100, and (c) 175 Å. The EM test was performed at 310 ℃, with a current density of 1.0 MA/cm^2.

To evaluate the confinement effect on EM reliability, the effective modulus (B) was calculated using FEA [69-71]. In figure 4.2, the results of B together with the experimentally measured $(jL)_c$ product are plotted as a function of barrier thickness. As the Ta barrier thickness decreased, B became smaller as expected due to a decreasing structural confinement effect. The barrier thickness effect on the $(jL)_c$ product was consistent with the change in B, except that the $(jL)_c$ product varied over a wider range. For example, the 75 Å Ta barrier had the $(jL)_c$ product lower than expected, indicating that the Cu lines with the 75 Å barrier failed prematurely before the back-flow stress gradient had chance to be completely built up. Premature failure was probably due to the presence of structural defects. The decrease in the $(jL)_c$ product suggests a more defective 75 Å Ta barrier. Such a probabilistic nature of the $(jL)_c$ product was also reported in other EM studies of Cu interconnects [18].

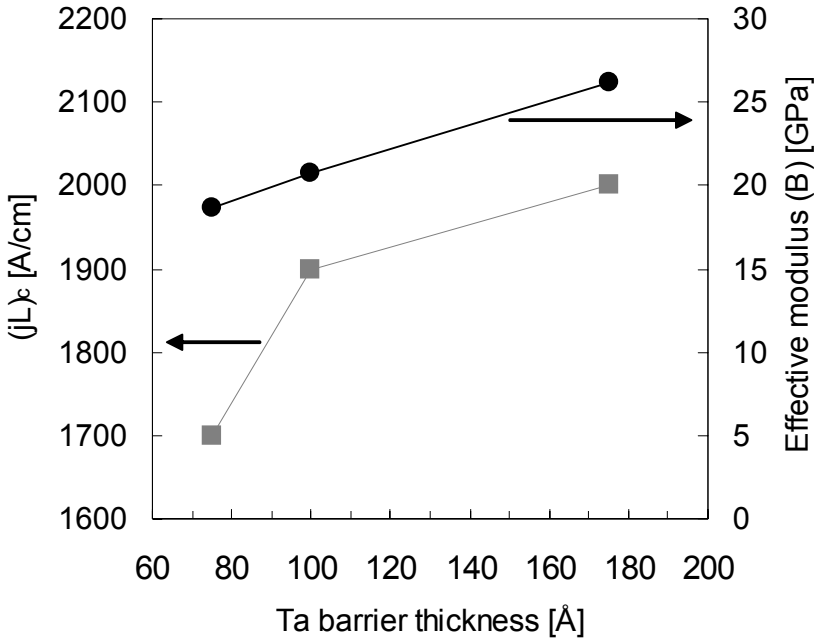

Figure 4.2 Plot of the statistically measured $(jL)_c$ product and the calculated effective modulus (B) using FEM as a function of Ta barrier thickness. The $(jL)_c$ product for the sample with 75 Å Ta barrier thickness showed considerable decrease than that expected from FEM.

4.3.2 Barrier Thickness Effect on Early Failure Statistics

The barrier thickness effect on EM reliability was further examined by investigating the early failure statistics using EF test structures shown in Figure 2.5(a). EM experiments were performed at 300 ℃ with up-stream electron current of 1.0 MA/cm^2. The cumulative distribution functions (CDF) obtained for samples with a Ta barrier thickness of 175 Å and 100 Å are plotted in Figure 4.3(a) and 4.3(b), respectively. Results in Figure 4.3(a) showed a mono-modal failure distribution indicating that strong mode void formation driven by EM was responsible for the failures. In contrast, a bi-modal failure distribution was observed in Figure 4.3(b) for the 100 Å barrier where the

weak-mode was shown to dominate the early failure statistics for the N=100 links. It is worth noting that the failure statistics for N=1 and N=10 links were similar for both barrier thicknesses indicating that strong-mode statistics was not affected by barrier thickness.

The extrinsic weak-mode failure and the intrinsic strong-mode failure can be separately determined using a Monte Carlo simulation based on the weakest-link approximation. Using this approach, it was found that the weak-mode amounted to 0.6 % of the failure statistics. Results from the EF structures with the 75 Å barrier also showed a bi-modal failure statistics with early failures dominating the N=100 links, very similar to the statistics of the 100 Å barrier test structures.

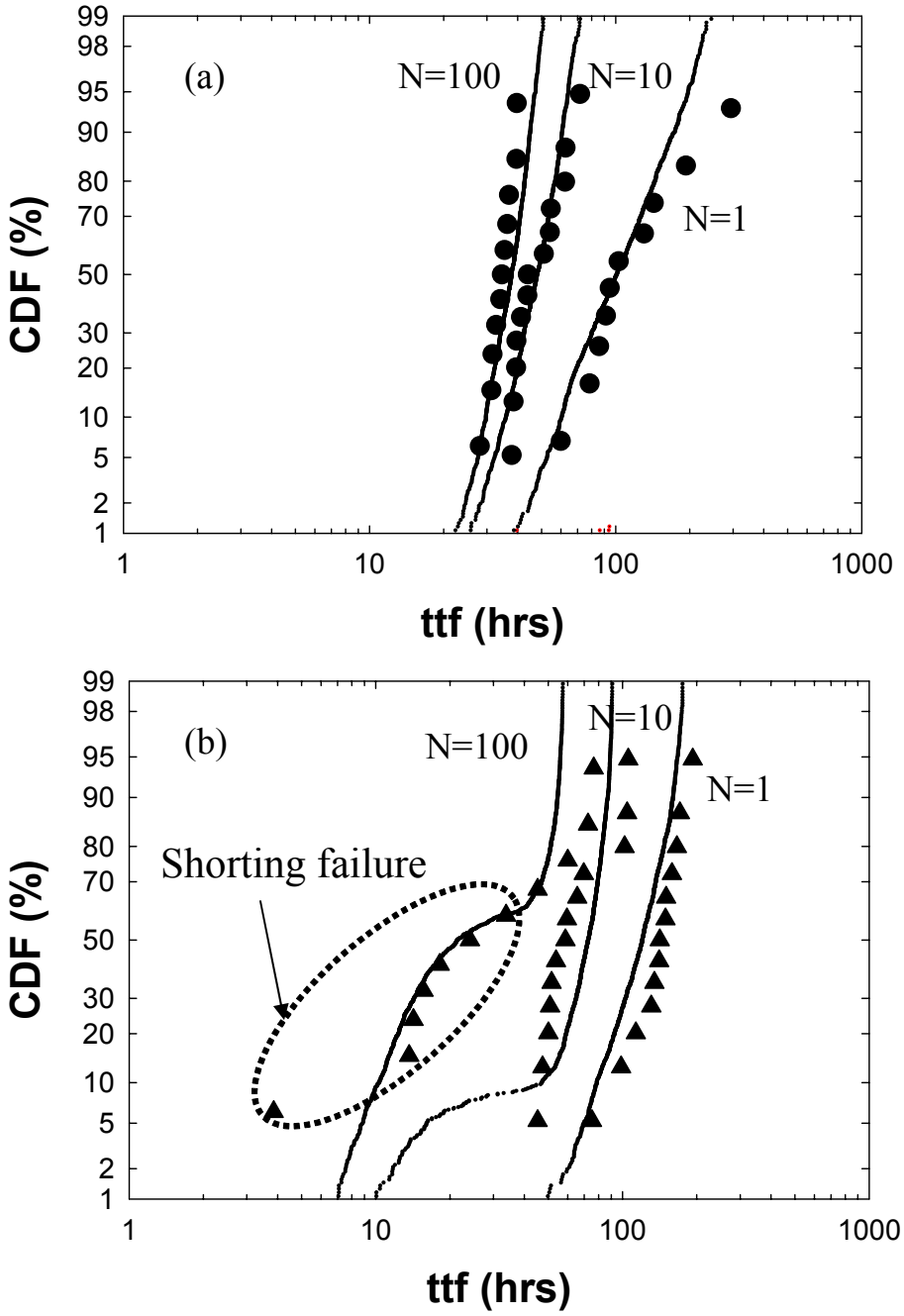

Figure 4.3 CDF Plots of EM test results using Early Failure test structures with Ta barrier thickness of (a) 175 Å showing the mono-modal distribution, and (b) 100 Å showing the bi-modal distribution due to the M2 line shorting with the extrusion monitor line [65,66, 71].

To investigate the weak-mode mechanisms, the resistance traces of the early failed samples (grouped in a circle in Figure 4.3(b)) were examined. All these structures except one were failed by shorting with the adjacent extrusion monitoring line. Figure 4.4 shows the resistance traces for strong mode failure (a) and shorting failure (b). In contrast to the strong mode failure, the step-like resistance decrease was observed in Figure 4.3(b) for the thinner barrier case. The abrupt resistance decrease can be attributed to current shunting to a wide extrusion monitoring line after the shorting failure.

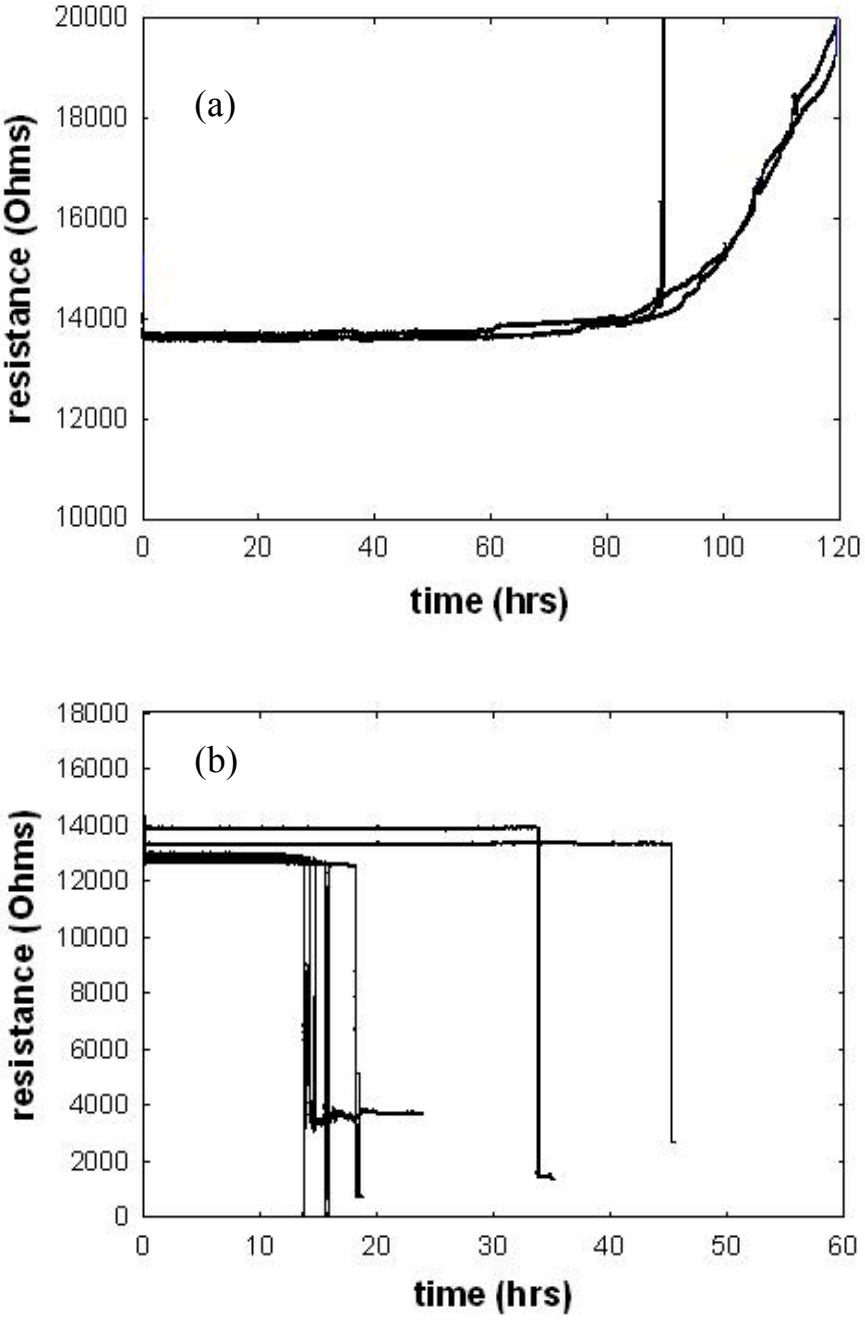

Figure 4.4 The resistance changes as a function of time of dual damascene Cu/low-k interconnects with the Ta barrier thickness of (a) 175 Å, and (b) 100 Å. The EM test was performed at 330 ℃, with a current density of 1.0 MA/cm^2 [71].

4.3.3 Physical Failure Analysis Using FIB and TEM

One of the early failed samples was examined using a focused ion beam (FIB) microprobe. As shown in Figure 4.5, it appeared that Cu atoms in the M2 line diffused out through the thin Ta barrier to the extrusion monitoring line resulting in shorting failure.

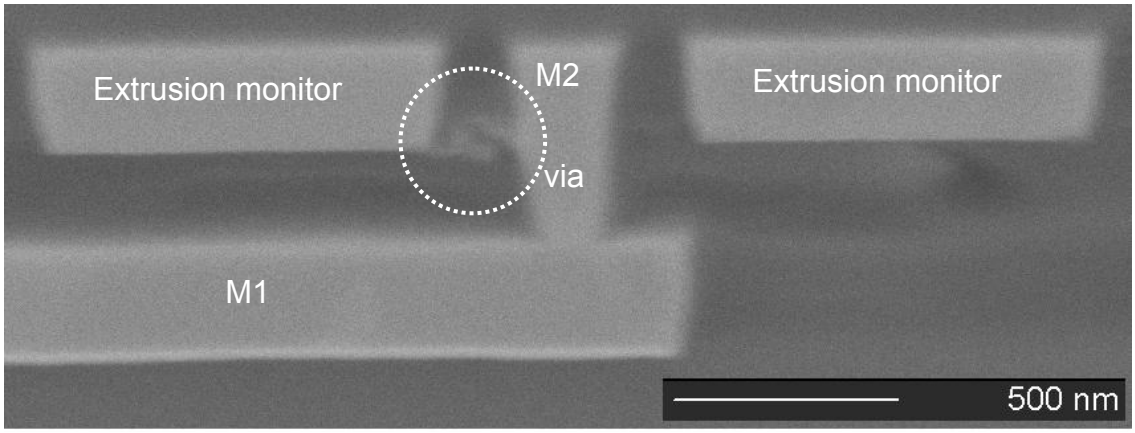

Figure 4.5 A cross-sectional focused ion beam (FIB) micrograph of EM tested Cu line and extrusion monitor lines from one of the shorting failed samples shown in Figure 4.3(b). Thin Cu layer between the M2 metal line and the extrusion monitor line is observed.

Cross sectional transmission electron microscopy (TEM) was also used to examine damage formation in EM tested sample with a thin Ta barrier. The TEM image in Figure 4.6 shows a M2 level interconnect with 100 Å Ta barrier layer and outer dark metal layers which extended from the Cu line into the porous low-k dielectric. The dark metal layer corresponded to out-diffusion of Cu driven by the elevated temperature and electrical current during EM test. The Cu out-diffusion was only observed in samples with 75 Å and 100 Å Ta barriers. FIB analysis revealed also void formation in the M2

lines near the cathode consistent with strong-mode failures observed in the EF test structures. These observations suggest that Cu out-diffusion through defects such as pinholes in the barrier caused by poor barrier integrity is an important mechanism for EM early failure, particularly with further scaling of barrier thickness. Such defects might be responsible for the small $(jL)_c$ product already observed with 75 Å Ta barrier where Cu out-diffusion caused premature failure before the back-flow stress was fully established.

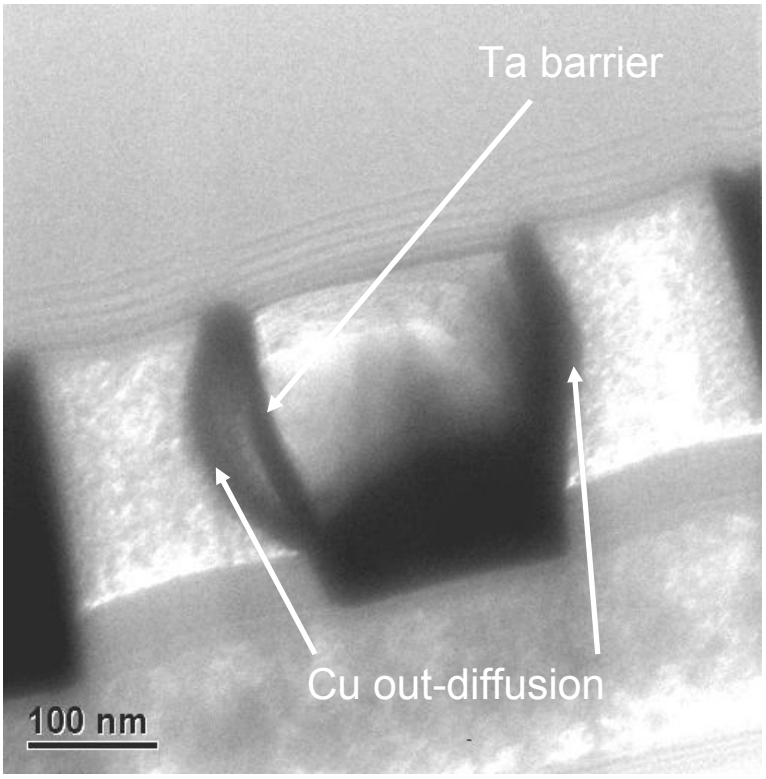

Figure 4.6 The cross-sectional transmission electron microscopy (TEM) image showing the formation of a dark outer metal layer next to the EM stressed M2 line. The Ta barrier thickness was 100 Å, and the EM test was performed at 330 ℃, with a current density of 1.0 MA/cm^2.

4.3.4 EM Activation Energies for Different Barrier Thicknesses

EM tests were performed at three different temperatures including 300, 330, and 360 ℃ to determine the activation energy for Cu interconnects with different Ta barrier thicknesses and the results are shown in Figure 4.7. Here, single-linked EM test structures were used to avoid occurrence of early failures. As expected, EM lifetime decreased with increasing temperature. EM lifetime and lifetime distribution were found to be independent of the thickness of Ta barrier. This result can be attributed to the dominant diffusion path at the interface between Cu line and the capping layer. Accordingly, the effect of Ta barrier thickness on strong-mode EM lifetime was negligible.

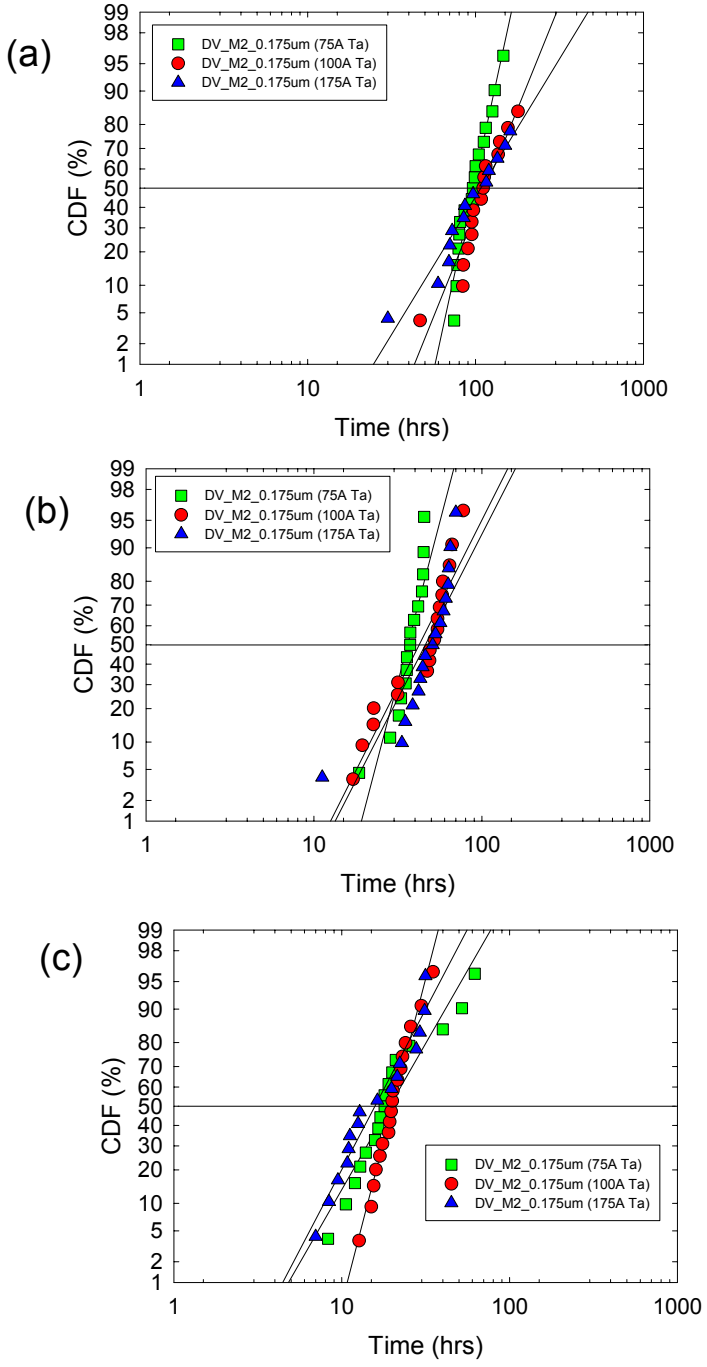

Figure 4.7 CDF plots of DV structures with different barrier thickness for up-stream electron flow. EM tests were performed at (a) 300 ℃, (b) 330 ℃, and (c) 360 ℃, with a current density of 1.0 MA/cm^2.

To determine the activation energy for the different barrier thicknesses, the Black's equation was used [72,73]:

$$t_{50} = Aj^{-n} \exp(Q_{EM}/kT) , \qquad (4.1)$$

where A is a constant, j is current density, n is the current density exponent, Q_{EM} is the activation energy for EM, k is Boltzmann's constant, T is the sample temperature. As shown in Figure 4.8, derived activation energies were similar, all in the range from 0.90 eV to 0.95 eV, indicating a similar interfacial diffusion behavior in our test structures and not affected by the barrier thickness [51,72].

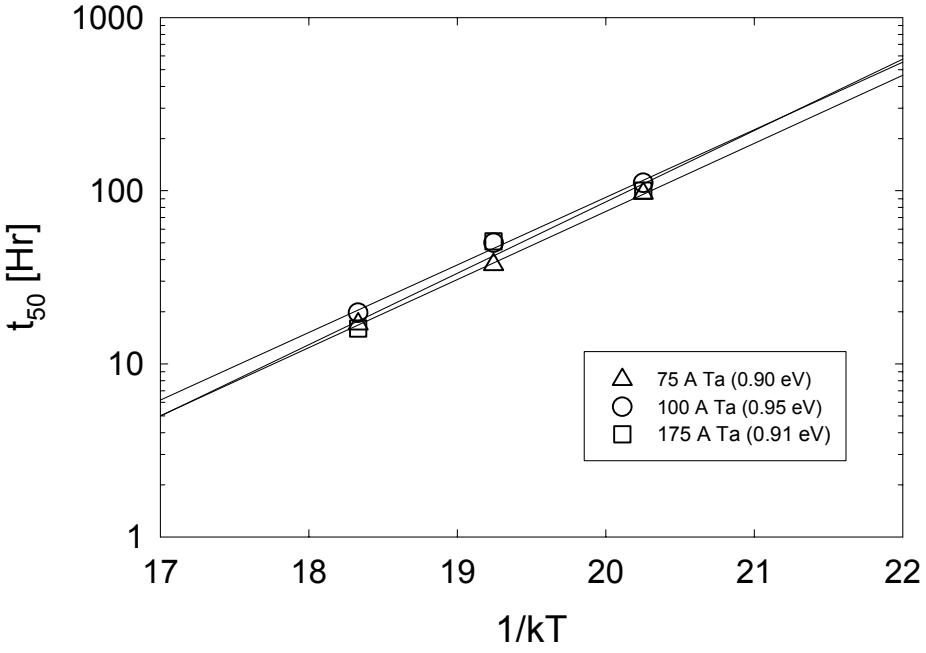

Figure 4.8 Electromigration lifetimes as a function of test temperature for the Cu interconnects with different barrier thicknesses under the current density of 1.0 MA/cm^2. The activation energies demonstrate a similar interface diffusion for different barrier thicknesses.

4.3.5 EM Resistance Traces for Different Barrier Thicknesses

The resistance changes as a function of time for the thick Ta barrier sample and thin Ta barrier sample are shown in Figure 4.9(a) and Figure 4.9(b), respectively. For the relatively thick 175 Å Ta barrier, the resistance increased slowly followed by abrupt and rapid resistance increases. As discussed previously in chapter 2.4, the initial slow resistance increase could be associated with void growth up to the via size. Beyond that point, the current was mostly shunted to the barrier layer giving rise to a step-like resistance increase as shown in Figure 4.9(a). Figure 4.9(b) shows that, for the thin 100 Å Ta barrier sample, the resistance increased slowly followed by a gradual resistance

increase. This gradual resistance increase was associated with Cu out-diffusion shown in Figure 4.10(b). The final resistance increase was due to the void growth induced by Cu mass transport along the upper surface of Cu line. Although not included, a similar resistance trace was observed for the 75 Å Ta barrier sample.

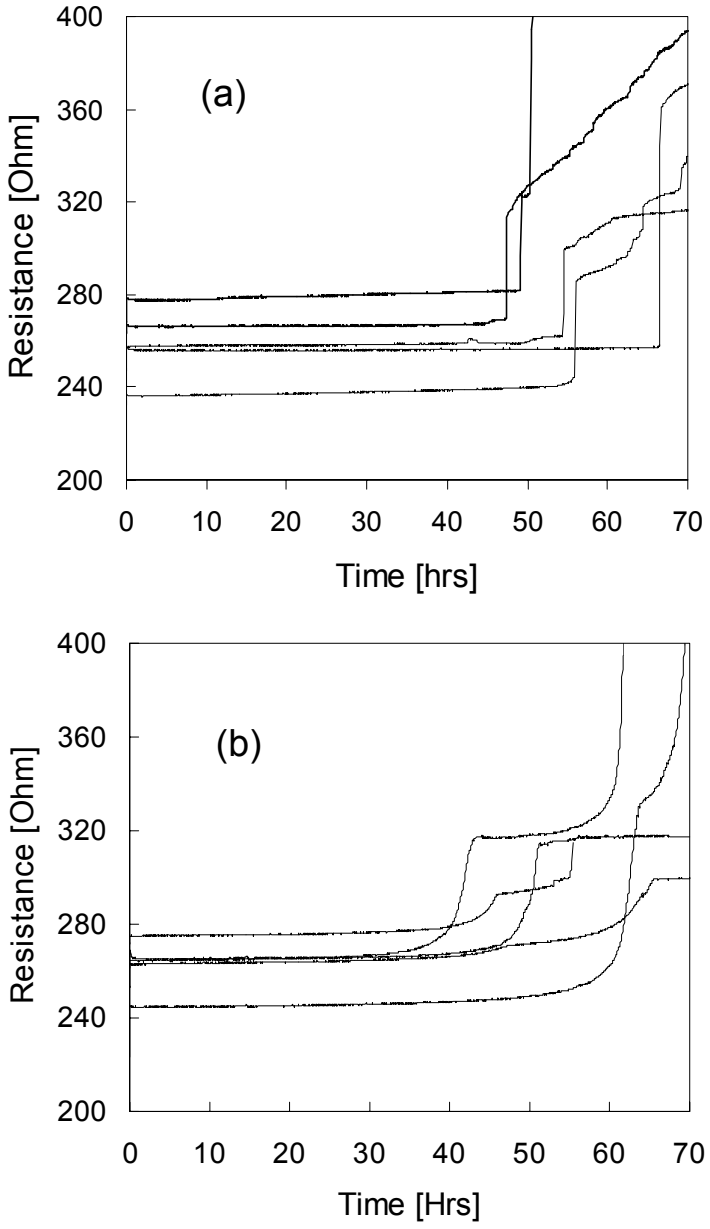

Figure 4.9 The resistance changes as a function of time of dual damascene Cu/low-k interconnects with the Ta barrier thickness of (a) 175 Å, and (b) 100 Å. The electromigration test was performed at 330 ℃, with a current density of 1.0 MA/cm^2.

Failure analysis was performed using a Focused Ion Beam (FIB) microprobe for the M2 line to investigate the reasons for the different EM resistance traces shown in Figure 4.9. The cross-sectional FIB image for 75 Å barrier in Figure 4.10(b) revealed Cu out-diffusion through the thin Ta barrier, which was not observed in the 175 Å barrier sample shown in Figure 4.10(a). This can account for the different resistance traces shown in Figures 4.9(a) and 4.9(b). These results indicate that a thin Ta barrier was not sufficient to prevent Cu out-diffusion driven by EM at high temperatures.

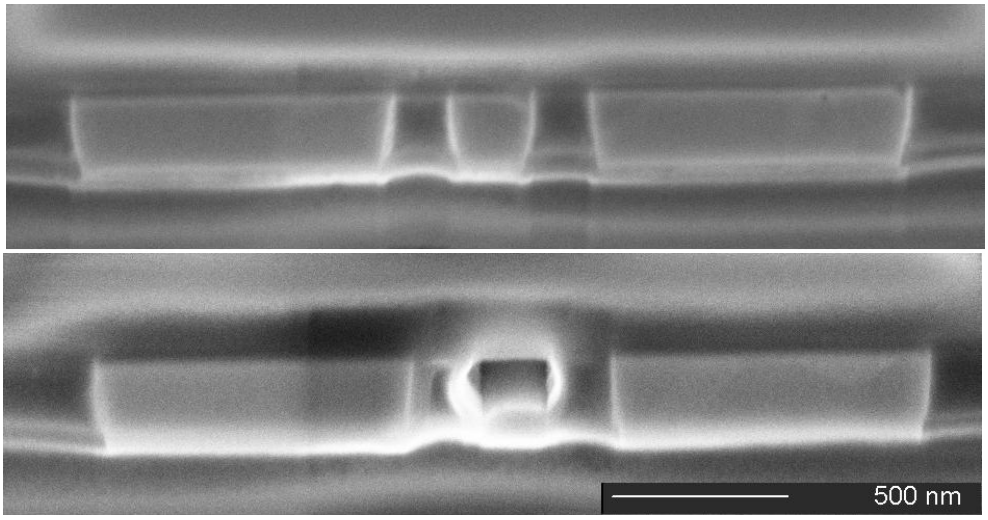

Figure 4.10 The cross-sectional Focused Ion Beam (FIB) images of Cu/low-k interconnect with the Ta barrier thickness of (a) 175 Å, and (b) 75 Å stressed at 330 ℃, with a current density of 1.0 MA/cm^2.

4.4 SUMMARY

The effects of Ta barrier thickness on electromigration reliability for the Cu/porous low-k interconnects were investigated. With decreasing Ta barrier thickness, the $(jL)_c$ product was found to decrease due to less structural confinement from thinner barriers. The effect can be accounted for by the effective modulus (B) of the structure except for the 75 Å Ta barrier, where the $(jL)_c$ product was reduced more significantly than expected probably due to the presence of defects in the barrier. Results from the early failure test structures revealed a bi-modal failure distribution for samples with 75 Å and 100 Å barriers. FIB and TEM observations revealed that the weak-mode early failure in the thin barriers was caused by Cu out-diffusion through the thin Ta barrier, shorting out the test lines with the extrusion monitoring line. The activation energies were found to be in the range from 0.90 eV to 0.95 eV independent of the barrier thickness, indicating a similar interfacial mass transport for EM for all the barrier thicknesses. The observed FIB images revealed that Cu out-diffusion from the thin barrier was responsible for the unusual EM resistance trace with gradual resistance increase observed for structures with the 75 Å Ta barrier.

Chapter 5: Via Scaling Effect on Electromigration Reliability of Cu/low-k Interconnects

The barrier process and thickness effect on EM reliability were discussed in chapter 3 and 4. Via scaling will become important in controlling EM reliability under high current density condition in the future. In this chapter, the effect of via scaling on electromigration (EM) reliability is investigated for Cu/porous low-k interconnects for via size and geometry scaling from 175 nm to 90 nm. EM failures for up-current electron flow tests were observed to be dominated by intrinsic failures, with void formation in the trench lines. A direct correlation between via size and EM reliability was found where EM lifetime and statistics degraded with via size. However, for structures with constant via size, EM lifetime and statistics were found to be independent of the M2 line width. These results can be attributed to intrinsic trench voiding where a critical void length was required for line failure which in turn was related to the via size. For down-current electron flow tests, the via size was designed to scale together with the M1 line width. Results showed that EM lifetime increased with line width because of the increasing critical void size. The trench voiding mechanism was confirmed by focused ion beam (FIB) analysis as well as resistance changes observed during EM tests.

5.1 INTRODUCTION

According to the scaling trend, the metal line and the via contact of the interconnect structure will continue to be scaled beyond the current 65-nm node [7]. Via scaling, in particular, becomes a serious reliability issue as the via plays an important role in controlling lifetime of stress-induced voiding and electromigration (EM) [8,26,52,74-77]. Line scaling caused EM lifetime to decrease due to an increase of early failures caused by process-induced defects [39]. In dual damascene interconnects, since there is no barrier layer between the via and the M2 trench, mass transport through the via and flux divergence at the via bottom are important factors contributing to EM failures. This raises a basic question concerning the effect of via processing and geometrical scaling on EM reliability. In this chapter, a systematic study of the effect of via scaling on EM reliability and lifetime statistics for Cu/porous low-k dual damascene interconnects is presented. Here, line width and via size were both scaled down from 175 nm to 90 nm.

Three different types of EM test structure were designed for up-current and down-current electron flow EM reliability tests. Using these structures, the effects on EM reliability due to via size scaling were investigated for both up- and down-stream electron flows [78]. Physical failure analysis was performed together with measurement of resistance changes during EM tests, to examine the EM failure modes and damage mechanism.

5.2 EXPERIMENTAL

Three types of EM test structures designed for the via scaling study are shown schematically in Figure 5.1, including two up-current electron flow test structures (type I and type II) and one down-current electron flow test structure (type III). In the type I

structure, denoted as VJ in Table 2.2, the M2 line widths were 90, 125, and 175 nm. The via widths and the end reservoir lengths were scaled to be the same as the M2 line width. In the type II structure, denoted VJ_via_0090 in Table 2.2, while the M2 line widths increased from 90 nm, 125 nm, to 175 nm, the via widths remained constant at 90 nm. In the type III down-current test structure, the M1 line width and the via size were scaled to be the same, decreasing from 175 nm to 125 nm. Note that all these test structures had the same line thicknesses and the cross-sectional vias were square. The two-level (M1/via/M2) EM test structures were fabricated using a dual damascene scheme. The low-k inter-metal dielectric (IMD) layer used in this study was a porous chemical vapor deposition (CVD) organosilicate material with k ~2.3.

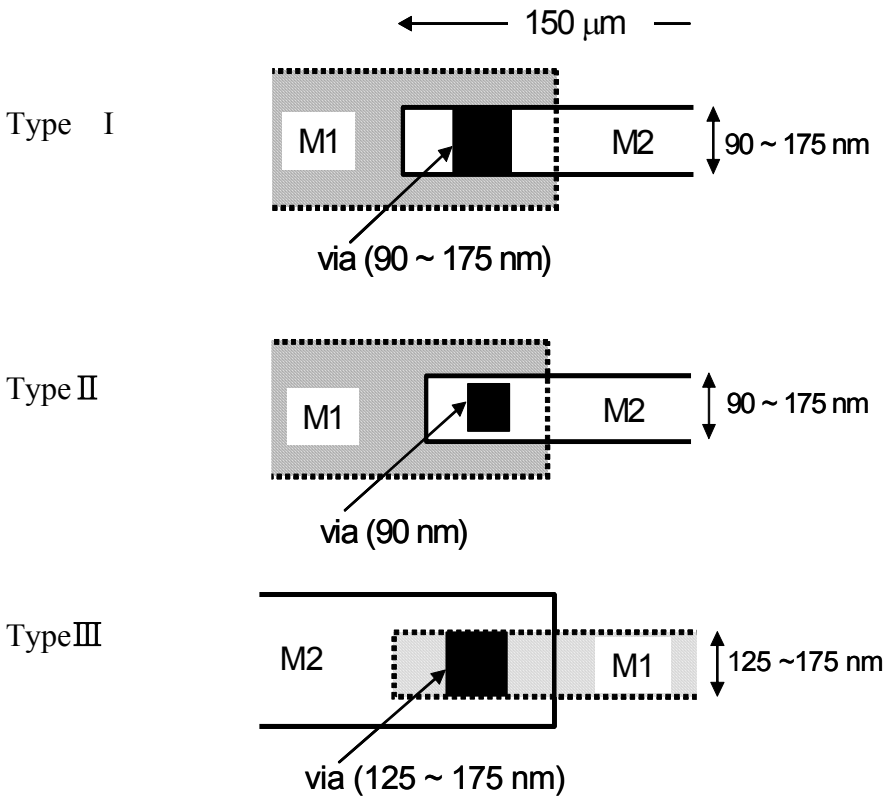

Figure 5.1 Schematics of two level (M1/via/M2) interconnect. The stressed line length was long (150 μm) and narrow, while the connecting line was short and wide to minimize the latter's EM damage. Up-current electron flow was applied to Type I and II, and down-current electron flow to Type III.

EM experiments were performed at 330 ℃ for up-current and 270 ℃ for down-current electron flow with a current density of 1.0 MA/cm^2 based on the line cross-sectional area. The test was performed in a high vacuum chamber under a nitrogen atmosphere ~20 torr. The resistance changes were recorded during EM tests, and the first significant resistance increase (~10 %) was taken to be an EM failure. Failed samples were analyzed using FIB to examine EM-induced void formation.

5.3 RESULTS AND DISCUSSION

5.3.1 Via Scaling Effect on EM Reliability for Type I Structures

The cumulative failure distribution (CDF) was obtained from lifetime data as a function of time and plotted for type I structures in Figure 5.2 for three M2 lines and via widths of 90 nm, 125 nm, and 175 nm. The EM lifetime was found to decrease with M2 and via width scaling, and the lifetime statistics became wider in distribution. These characteristics can be explained based on the following EM lifetime expression proposed by Hu et al. [76,79]:

$$\tau = \Delta L_{cr}/\nu_d = \Delta L_{cr} h kT/(\delta_s D_i F_i) \qquad (5.1)$$

where ΔL_{cr} is the critical void length required for line failure, ν_d is the net drift velocity, h is the line thickness, k is Boltzmann's constant, T is the absolute temperature, and δ_s is the effective thickness of the interface region. This expression assumes intrinsic failure mechanism where mass transport is dominated by diffusion at the Cu/cap interface with a diffusivity D_i and a driving force F_i.

In this study, all the line structures had the same cap layer interface and line thickness and were tested under the same conditions. Therefore, the EM lifetime is expected to be directly correlated to ΔL_{cr}. The line will fail due to void growth starting from the cathode end of the trench to clear across the whole via. In this case, ΔL_{cr} will be proportional to the via size for the type I test structures, thus the EM lifetime should scale with the via width. This is in good agreement with the results in Figure 5.2.

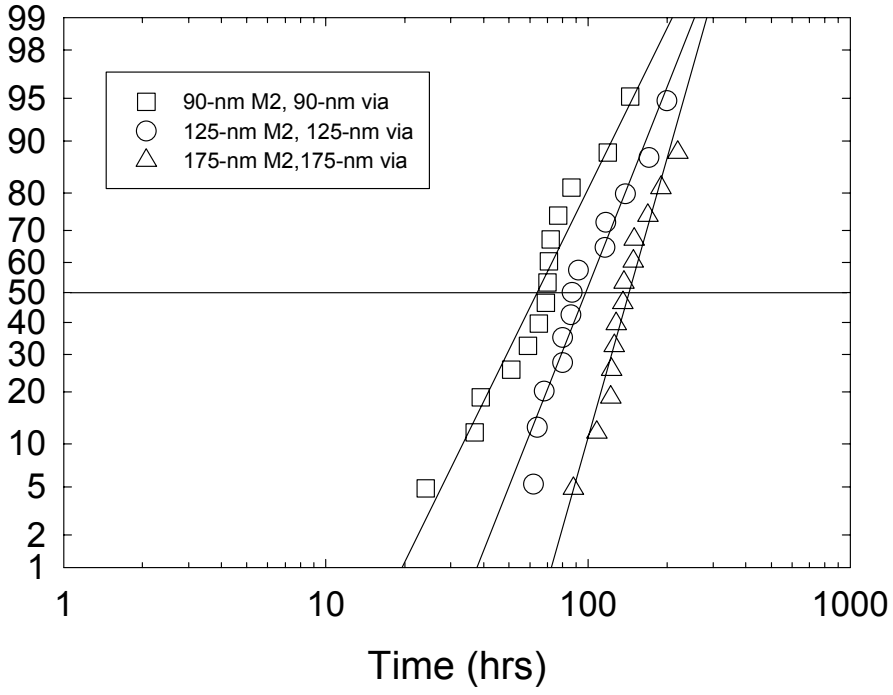

Figure 5.2 Cumulative failure distribution function (CDF) plots of type I structures with different M2 and via widths for up-stream electron flow. EM tests were performed at 330 ℃, with a current density of 1.0 MA/cm^2.

The resistance traces recorded during the EM test for the 125-nm test structures are plotted in Figure 5.3. The resistance changes showed typical intrinsic EM failure behavior where the first abrupt resistance increase occurred when a void growing from the cathode end traversed the whole via. The current was then shunted to the redundant Ta barrier, causing resistance to abruptly increase. The subsequent gradual increase in resistance was due to continuing void growth along the M2 trench. When the Ta barrier could no longer sustain the current density, the barrier burned out to cause an abrupt increase in resistance.

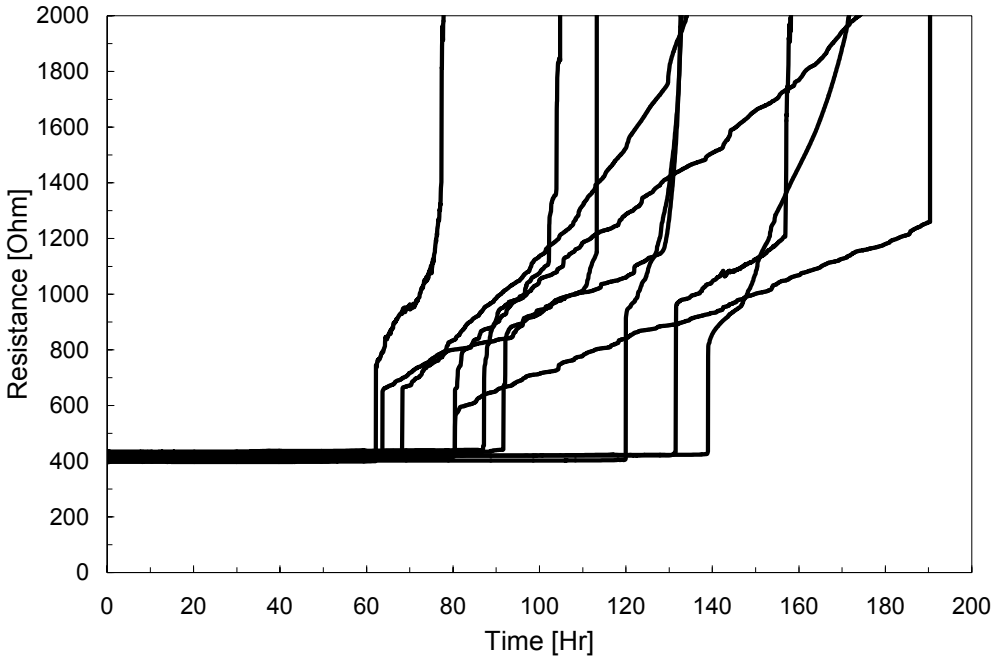

Figure 5.3 Resistance changes of 125-nm wide EM samples with type I structure.

In contrast, the resistance traces for the 90-nm wide lines in Figure 5.4, showed both gradual and abrupt increases. The abrupt resistance increases can be attributed to via bottom voiding caused by extrinsic process-induced defects, which will be shown later in failure analysis. The gradual increase can be attributed to the identical reason as described for the 125-nm lines. The combination of the two failure modes led to a wider lifetime distribution for 90-nm lines than the 125-nm and 175-nm lines, as shown in Figure 5.2.

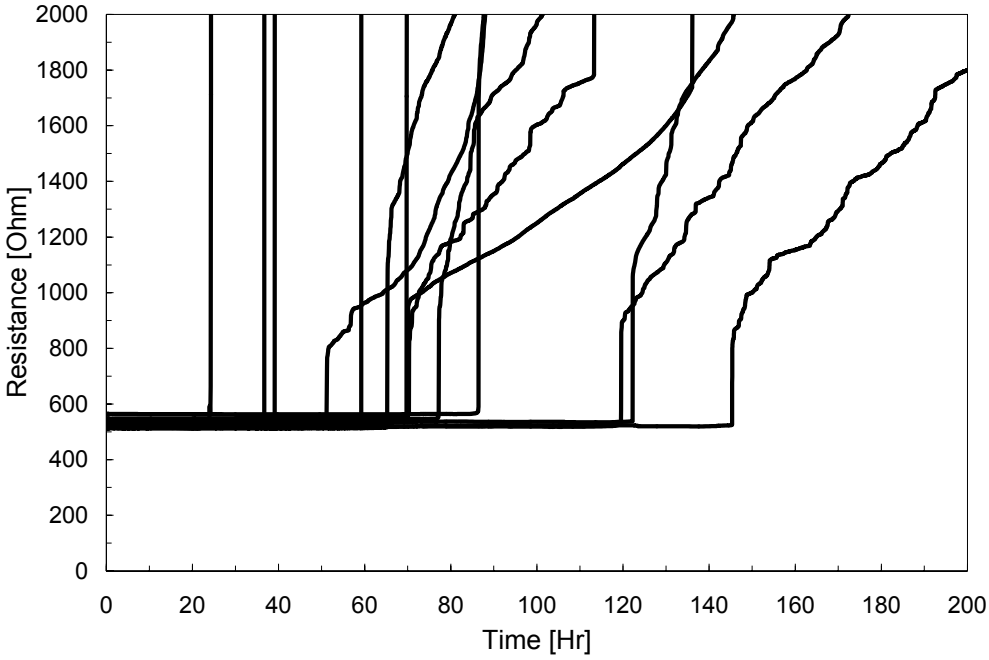

Figure 5.4 Resistance changes of 90-nm wide EM samples with type I structure.

One of the 125-nm wide EM failed samples was analyzed using FIB, and the image is shown in Figure 5.5. Even though the via structure was not clearly discernible due to severe joule heating, a large trench void at the cathode end was evident. This damage mode supports the intrinsic failure mechanism due to void formation at the cathode driven by interfacial mass transport. This is also consistent with the resistance trace shown in Figure 5.3.

Figure 5.5 Focused Ion Beam (FIB) image showing a large cathode void in M2 trench for an EM failed 125-nm wide interconnect.

5.3.2 Via Scaling Effect on EM Reliability for Type II Structures

Up-current electron flow EM tests for type II structures were performed at 330 ℃, with a current density of 1.0 MA/cm^2; the resulting CDF plots are shown in Figure 5.6. The EM lifetimes and statistics were found to be similar for these types of structures with the same via size but different M2 width and tested under identical conditions. In this case, the same current density in the M2 trench translated to a higher current density at the via for the wider 125-nm and 175-nm lines and a higher current crowding effect. Nevertheless, the EM lifetimes and statistics remained about the same, independent of the line width. This is consistent with the same intrinsic mechanism due to trench voiding (Equation 5.1) where EM lifetime was independent of the M2 line width since the critical void length was fixed. Interestingly the higher current density at the via did not cause higher rate of EM failures. This suggests that the via effect was primarily extrinsic, related to process-induced defects, and contributed little to intrinsic trench failures.

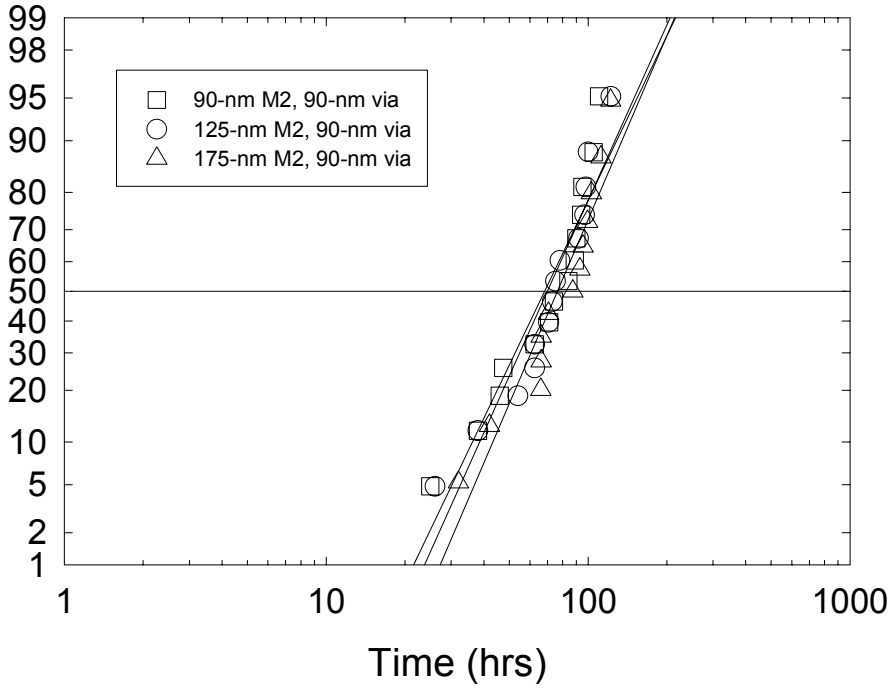

Figure 5.6 Cumulative failure distribution function (CDF) plots of type II structures with different M2 line widths for up-stream electron flow. EM tests were performed at 330 ℃, with a current density of 1.0 MA/cm^2.

5.3.3 Via Scaling Effect on EM Reliability for Type III Structures

Down-current EM tests using type III structures were performed at 270 ℃, with a current density of 1.0 MA/cm^2. The CDF plots for 125-nm and 175-nm lines are shown in Figure 5.7, where the EM lifetimes for 175-nm wide lines were longer. This result can also be attributed to the different critical void length (Equation 5.1). Since via width and M1 line width were identical, the critical void length, which was related to the via size, was longer for the 175-nm lines.

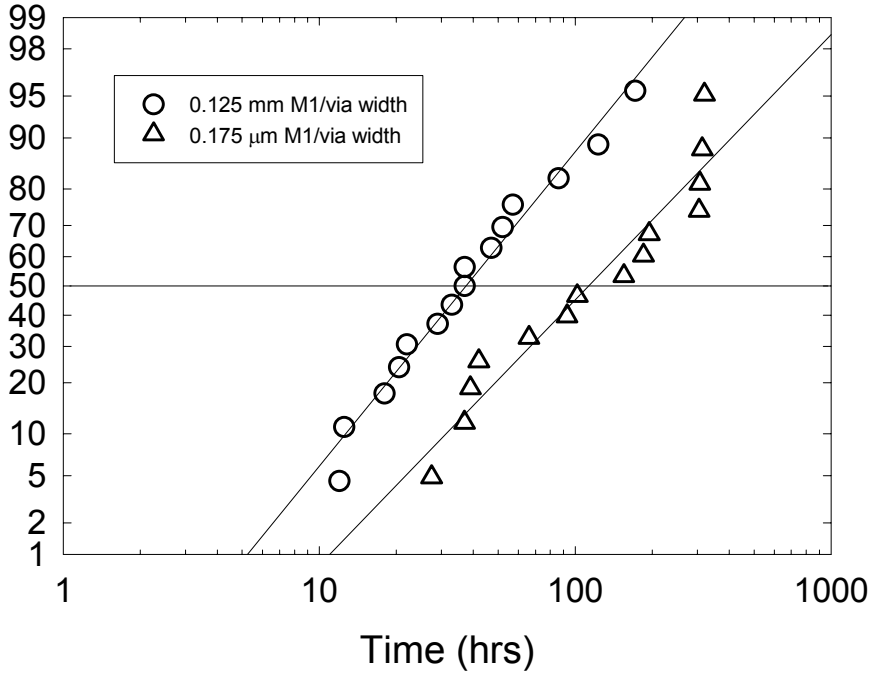

Figure 5.7 Cumulative failure distribution function (CDF) plots of type III structures with different M1 line widths for down-stream electron flow. EM tests were performed at 270 ℃, with a current density of 1.0 MA/cm^2.

To investigate the EM failure mechanism, the resistance changes for down-current EM were monitored and plotted in Figure 5.8. Compared with the up-current EM tests shown in Figure 5.3, a gradual increase in resistance was not found. The abrupt and substantial resistance increase can be associated with void formation under the via. When a void formed under the via, the resistance increased significantly because there was no redundant Ta barrier to sustain the EM current. In addition the abrupt and substantial resistance change indicated Cu mass transport through the Cu/capping interface above M1, forming a void underneath the via.

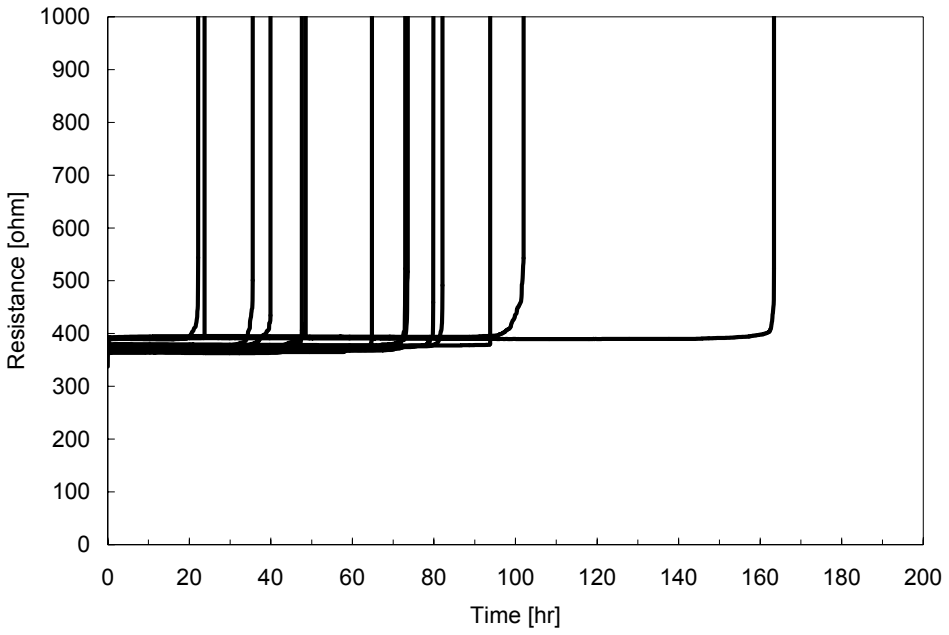

Figure 5.8 Resistance changes of down-current electron flow EM samples with type III structure.

To validate the above explanation, an EM sample carried to failure in the down-current electron flow test was examined using FIB. A large void near the cathode was observed (Figure 5.9) where Cu atoms were completely depleted. This led to an abrupt and large resistance increase as shown in Figure 5.8 and confirmed the via bottom voiding mechanism.

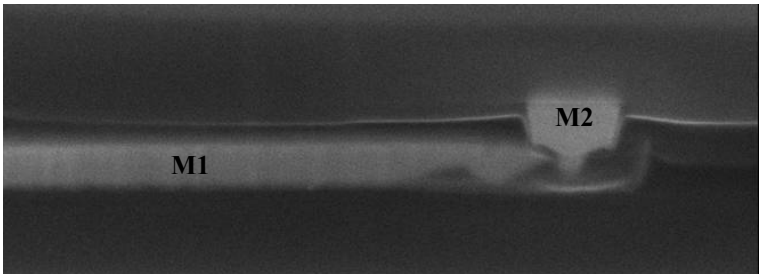

Figure 5.9 Focused Ion Beam (FIB) image showing a large cathode void in M1 trench for an EM failed interconnect.

5.4 SUMMARY

The effect of via scaling on EM reliability was investigated for Cu/porous low-k interconnects using three types of test structures designed for up-current and down-current tests. For type I structures with the up-current electron flow where line width was scaled with via size, EM lifetime and statistics degraded with via scaling. This result was attributed to an intrinsic failure mechanism due to trench voiding driven by interfacial mass transport. A critical void length was required for line failure in this case. The trench voiding in type II structures was confirmed by an up-current electron flow test of the type II samples with a constant via size, where EM lifetime and the failure statistics were found to be independent of the M2 line width due to the fixed critical void length. Void formation due to interfacial mass transport was also confirmed for down-current test of the type III structures where EM lifetime increased for wider lines due to a longer critical void length. Results of this study should provide useful guidelines for via and line scaling to improve EM reliability for Cu interconnects.

Chapter 6: Electromigration Behavior for Ultra Fine Dual Damascene Cu Interconnects

6.1 INTRODUCTION

With line scaling, EM becomes an increasingly serious reliability concern in the interconnects due to the increase of the surface to volume ratio of Cu interconnects and the increasing current density applied to devices. In chapter 5, the minimum line/via width was 90-nm, corresponding to 65-nm technology. In this chapter, SiON (siliconoxynitride) trench-filling process is introduced to fabricate ultra fine Cu lines (60 nm) at the metal-1 (M1) level, which corresponds to 45-nm technology, to investigate further line scaling effect on EM reliability. Using this novel process scheme, 60-nm lines could be delineated, albeit only in the M1 level, without having to upgrade photo lithography equipment, which was set up for 125-nm wide lines and vias [80]. The main advantage of this process is that 60-nm wide lines can be delineated using a conventional, wider line technology. Another advantage of this process is that the final trench width can be easily controlled by the thickness of the filling material. As it turned out, the trench-filling process yielded a distinct via/M1 interface, which helped eliminate the extrinsic void evolution at the via bottom. This made possible the investigation of intrinsic EM reliability for fine lines. For comparative purposes, samples with/without SiON filling layer were tested.

6.2 EXPERIMENTAL DETAILS

Two-level (M1, via, and M2) EM test structures were designed to investigate EM reliability for the Cu interconnects. The trench-filling process using SiON film was applied only to the M1 level. As shown in Figure 6.1, the EM tests performed in this study were all down-current electron flow condition, where electrons flowed from a wide and short M2 level to a narrow and long M1 level. This makes it possible to observe the void formation and line failure in the M1 line. EM test samples were fabricated using dual damascene process on 300-mm wafers. The inter-metal dielectric layer used in this study was silicon oxide.

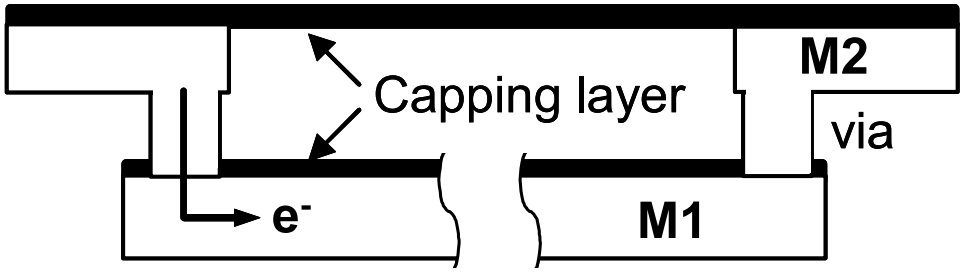

Figure 6.1 Schematic diagram of a two level (M1/via/M2) EM test structure with down current electron flow condition.

As shown in Figure 6.2, SiON filling layer was deposited after trench formation. Ta barrier deposition and Cu electro-plating followed. Using this process, the trench width was reduced from 130 nm to 60 nm. The Ta barrier thicknesses at the trench bottom and sidewall were 13 nm and 6 nm, respectively, as shown by TEM in Figure 6.2(d).

Package-level EM tests were performed in a vacuum chamber with a back-filled pure nitrogen environment at 20 torr, heated at a rate of 5 ℃/min to the target temperature, with a current density of 1.0 MA/cm^2. Resistance increase due to void formation was monitored to determine the EM lifetime. EM tests at various temperatures and current densities were performed to derive an activation energy for EM and current density exponent. The time of 10 % resistance increase was taken as the EM lifetime. Based on the lifetime data, the cumulative distribution of failure (CDF) was obtained as a function of time. The EM failed samples were analyzed by transmission electron microscopy (TEM) for in-depth understanding of damage progression.

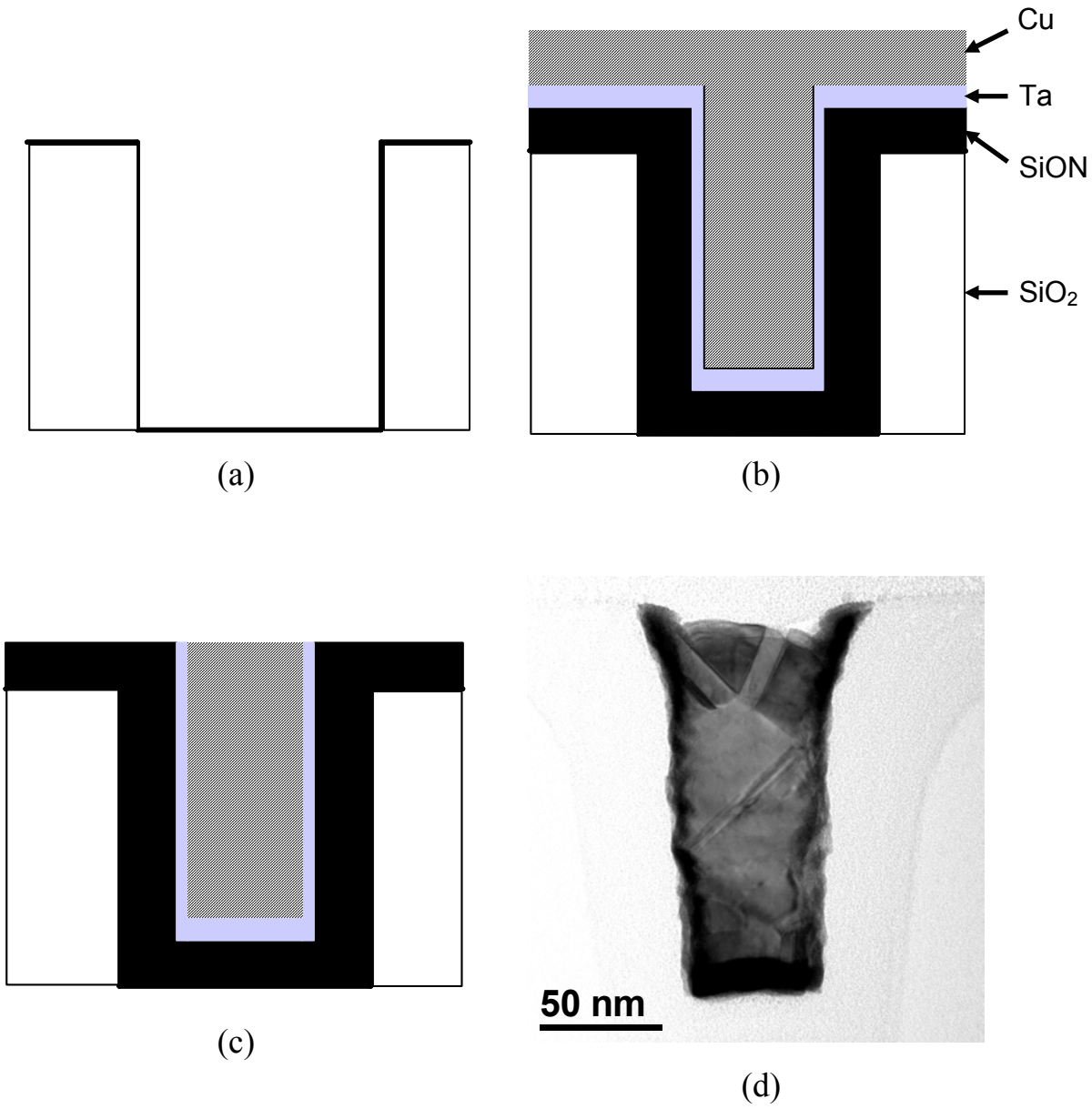

Figure 6.2 Schematics of SiON filling process scheme. (a) trench formation, (b) SiON deposition + Ta barrier deposition + copper deposition, (d) chemical mechanical polishing (CMP), (d) cross-sectional TEM image showing 60-nm M1 trench with SiON filling.

6.3 RESULTS AND DISCUSSION

6.3.1 Effect of SiON Filling on EM Reliability

The EM test was performed at 270 ℃, with a current density of 1.0 MA/cm^2. Using the EM lifetime data, the CDF plots were constructed as a function of time for the samples with SiON filling layer (60 nm) and standard samples (125 nm) as shown in Figure 6.3. The samples with SiON filling showed a longer lifetime by about two fold and somewhat larger standard deviation than the control samples without SiON filling. The somewhat larger standard deviation for the SiON-filled samples can be attributed to larger variations in critical dimension (CD) caused by adding the SiON deposition step.

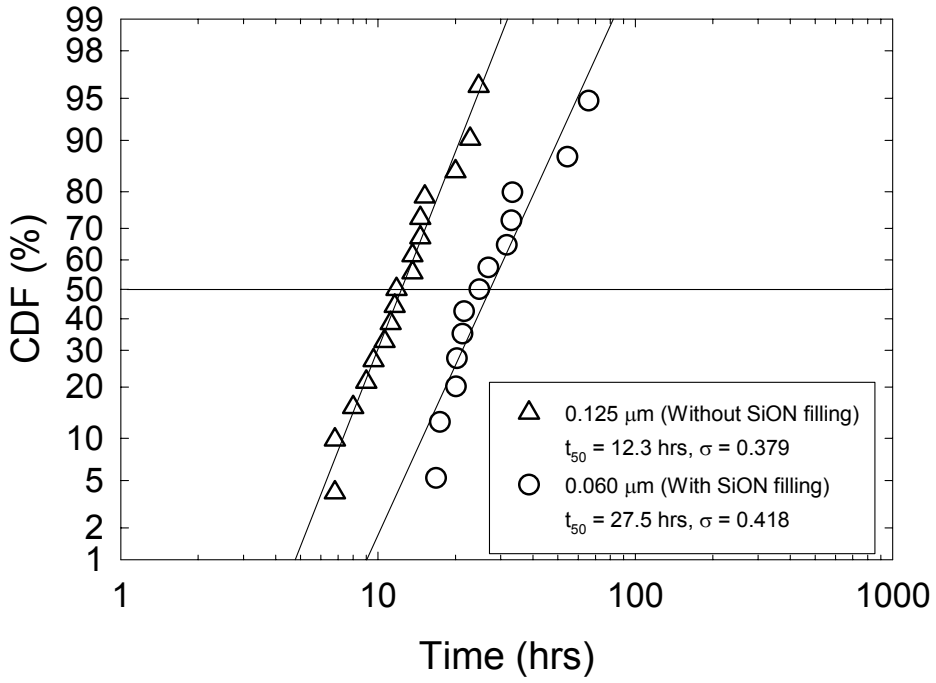

Figure 6.3 Cumulative failure distribution function (CDF) plots of down stream EM test structures with SiON filling layer (60 nm) and without SiON filling layer (125 nm). EM test was performed at 270 ℃, with a current density of 1.0 MA/cm^2.

To understand failure mechanism, resistance traces were monitored and the results for the two different line widths are shown in Figure 6.4. Compared with the 125-nm line, the 60-nm line showed more progressive resistance increase followed by abrupt increase. Such behavior can be attributed to the Ta barrier at via bottom serving as redundant layer for current flow. All the 125-nm lines without SiON filling showed abrupt resistance increases indicating void formation underneath via.

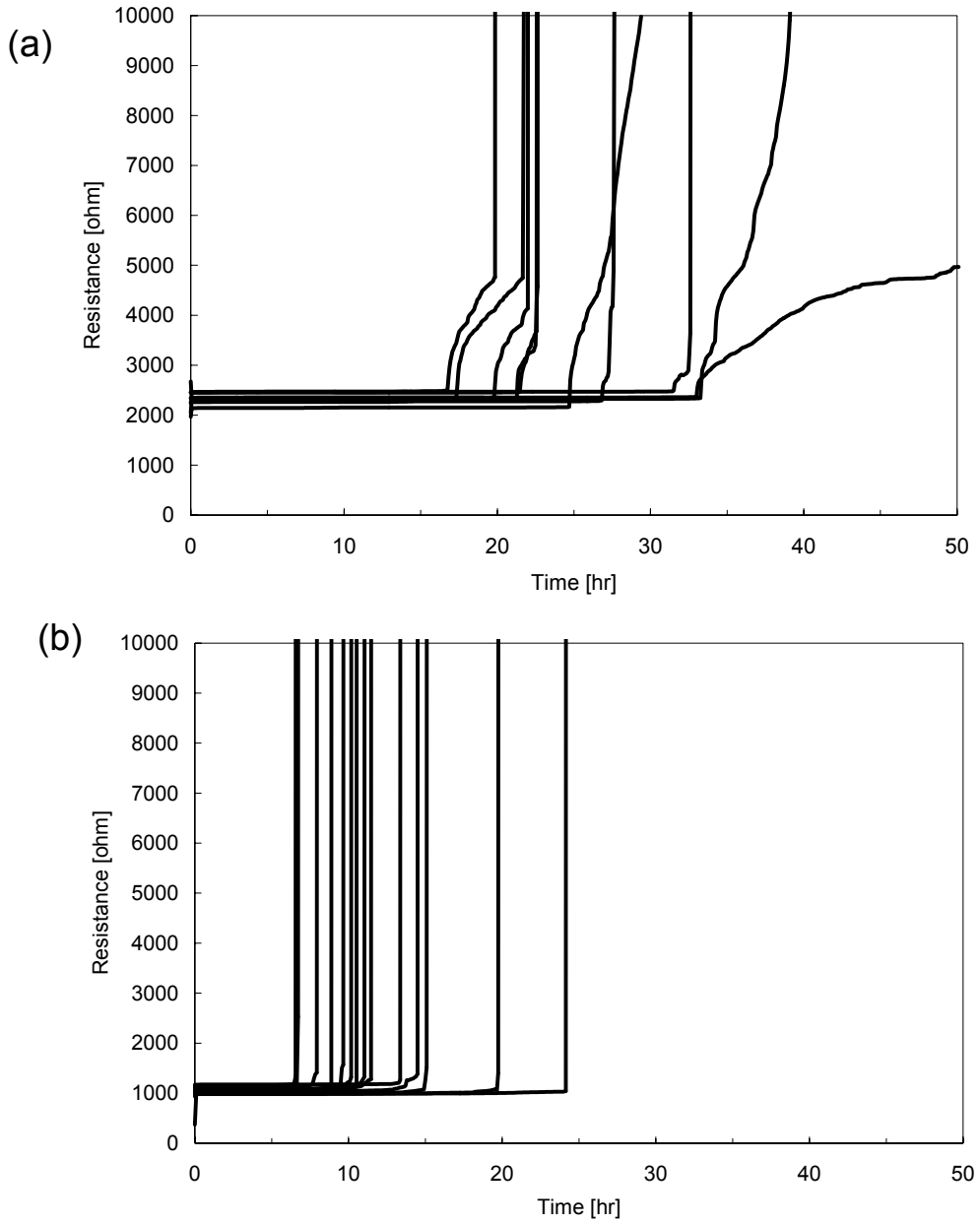

Figure 6.4 Resistance changes of down stream EM test structures (a) with SiON filling layer (60 nm) and (b) without SiON filling layer (125 nm). EM test was performed at 270 ℃, with a current density of 1.0 MA/cm^2.

6.3.2 EM Failure Mechanism

Figure 6.5 shows the cross sectional TEM images for the EM test samples as well as the schematics on the right side of each TEM image. Compared with the control sample, shown in Figure 6.5(a), SiON filling made the M1 trench width narrow enough to be fully covered by the via bottom. This unique interface structure between via and M1 enabled prolonging of the EM lifetime by about two fold as shown in Figure 6.3.

When an EM-induced void forms in a standard sample with no SiON filling and grows as wide as the M1 trench on top of the cathode end of M1, such a sample would fail by an open circuit. However, for a sample with the SiON layer, the EM current can be shunted to the Ta barrier even when the M1 trench vacated by EM-induced void. This sample will not fail until the void extends a good distance along the Ta barrier and the resistance finally becomes large enough to induce joule heating to burn out the barrier and the structure.

In addition, the unique M1/via interface structure can eliminate the most probable void formation site responsible for early failures, i.e., at the interface between the bottom portion of the via side wall and the M1 trench top. Therefore, only the intrinsic effect, devoid of extrinsic effect, of the increased mass transport on EM reliability can be investigated using the SiON-filled fine lines.

Since the current density in the M1 trench was kept constant for both samples with different M1 line widths, the higher current was needed to be applied to the wider, 125-nm line. Consequently, current density in the via was higher for the wider line than the finer line. This resulted in the higher maximum current density concentration for the wider line near the via bottom, making its current crowding zone more vulnerable to EM failure [81,82]. This might be another possible reason for the shorter EM lifetime for the wider lines without SiON filling.

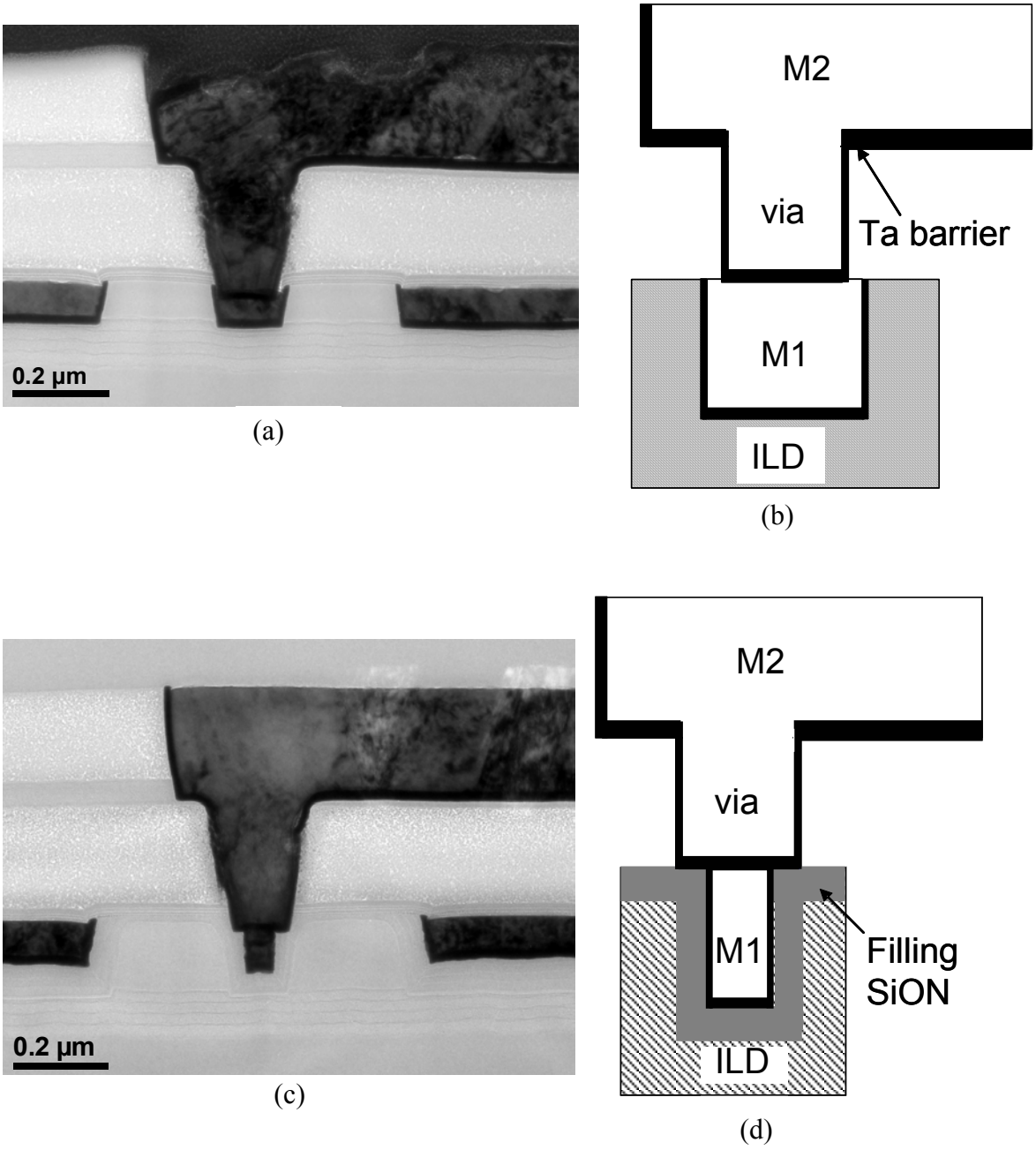

Figure 6.5 Transmission electron microscopy (TEM) images of dual-damascene Cu interconnects. M1 trench width was reduced from 130 nm (a) to 60 nm (c) using filling SiON layer, and the schematics, (b) and (d), are shown on the right hand side of each TEM picture.

An EM-failed sample with 60-nm wide line was examined using a cross-sectional TEM. As shown in Figure 6.6, a large void near the cathode was found along the M1 line as highlighted by a white boundary while the via bottom was intact, indicating that a void formed and grew extensively in the metal trench region.

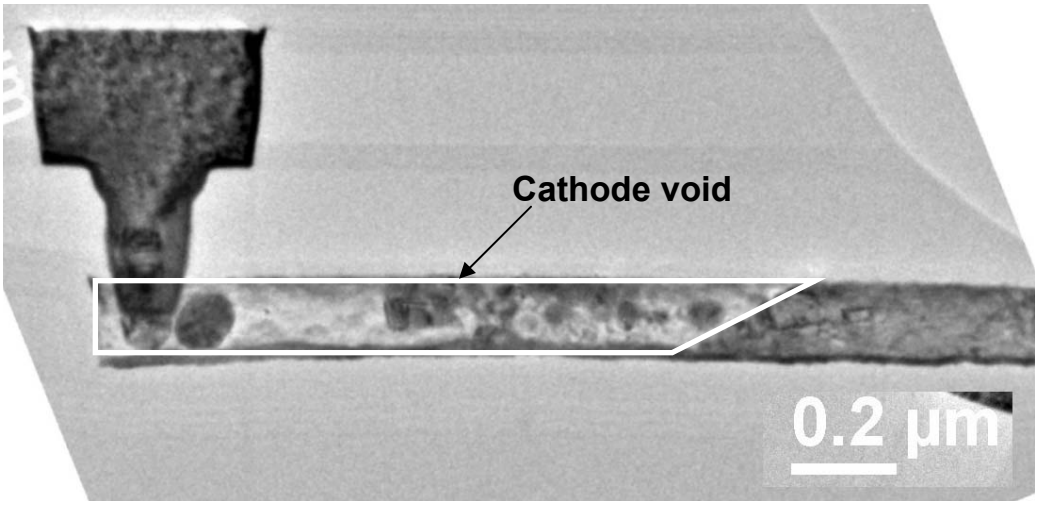

Figure 6.6 Transmission electron microscopy (TEM) image showing a large cathode void in M1 trench for an EM failed 60-nm wide interconnect.

6.3.3 Line Width Effect on EM among SiON-filled Samples

To understand the effect of line width scaling on EM for the samples with SiON trench-filling layer, EM tests with three different line widths; 60, 110, and 185 nm were performed at 300 ℃, with a current density of 1.0 MA/cm^2. The trench widths before SiON filling were 125 nm, 175 nm, and 250 nm, respectively. The CDF plots for the EM samples with three different M1 line widths are shown in Figure 6.7. The EM tests as usual were performed using the down-stream electron flow condition. The results revealed that the CDF was independent of the M1 line widths employed. The reasoning

behind the line width independence is explained in the following. Since the void was found only in the M1 trench as shown in the TEM image (Figure 6.6), this suggests that a void formed only in the M1 trench for the samples with SiON filling.

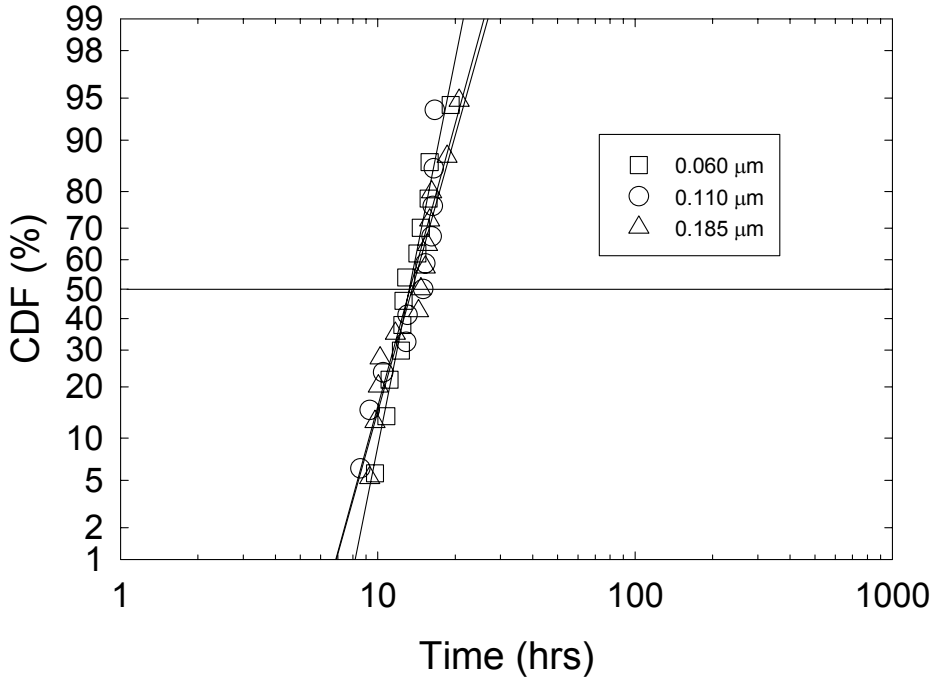

Figure 6.7 Cumulative failure distribution function (CDF) plots with different line widths for down stream electron flow. EM tests were performed at 300 ℃, with a current density of 1.0 MA/cm^2.

As discussed in chapter 5, EM lifetime can be expressed as [76]

$$\tau = \Delta L_{cr}/\nu_d = \Delta L_{cr} hkT/(\delta_s D_i F_i) , \qquad (5.1)$$

where ΔL_{cr} is the critical void length to cause line failure, ν_d is the net drift velocity, h is the line thickness, k is Boltzmann's constant, T is the absolute temperature, δ_s is the effective thickness of the interface region, D_i is the Cu/dielectric interface diffusivity, and

F_i is the EM driving force at the interface. When void formation occurred only in the trench, ΔL_{cr} could be set as a constant. EM lifetime then is only related to the metal line thickness, *h*. Since the line thicknesses are identical regardless of the line width, the lifetimes would become identical for the samples with different line widths under the same temperature and current density conditions, as shown in Figure 6.7.

The changes in normalized line resistance as a function of time for the samples with different line widths at 300 ℃, with a current density of 1.0 MA/cm^2 are shown in Figure 6.8. Compared with the 185 nm line, the 60 nm line exhibited a more cyclic behavior with gradual resistance increase after an abrupt initial resistance increase. This behavior may be associated with the different grain structure and barrier thickness of these lines. In a previous study, void formation in the line trench was found to depend on the grain orientation, which controlled the interfacial diffusivity [57,58].

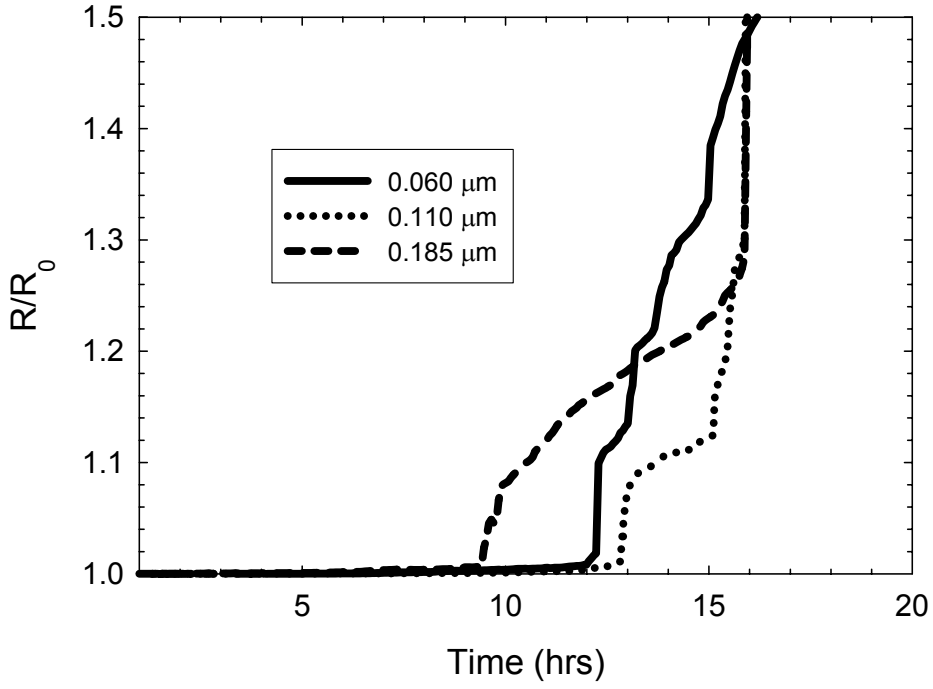

Figure 6.8 Normalized resistance changes of EM samples with different line widths. EM tests were performed at 300 ℃, with a current density of 1.0 MA/cm^2.

Under EM, the whole grain in the 60-nm line will be depleted by interfacial mass transport. At that point, resistance will increase abruptly due to current shunting to the Ta barrier layer, which has a higher resistivity than Cu. In this way, the resistance will increase, first gradually and then abruptly as one grain in the line is consumed. As shown in Figure 6.9, this sequence will repeat until an adjacent grain is depleted if the Ta barrier can sustain the current without being burnt out. The FIB image in Figure 6.10 supported the cyclic resistance traces. Such cyclic resistance increases can be more readily observed in the 60 nm line because it has a smaller grain size than a 185 nm line.

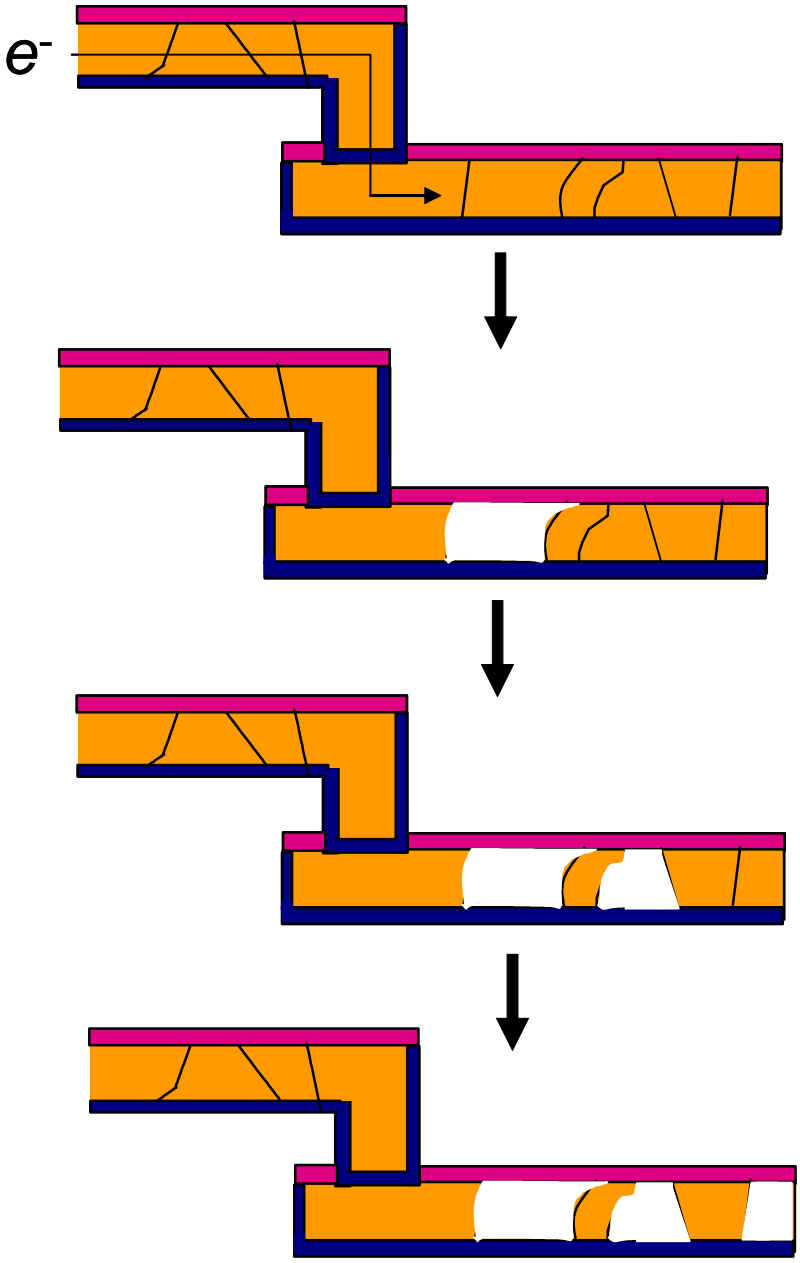

Figure 6.9 Schematics of void evolution in M1 trench for dual damascene Cu interconnects with SiON filling layer.

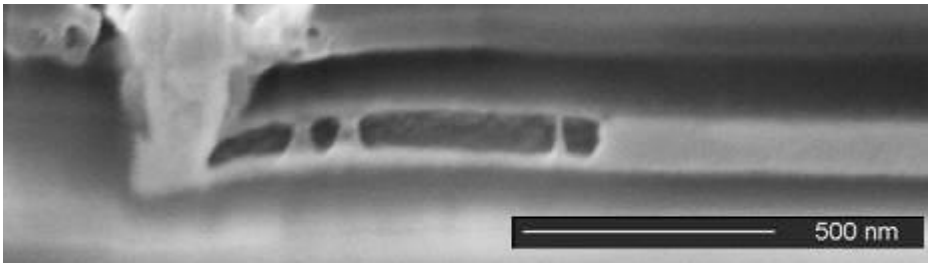

Figure 6.10 Focused Ion Beam (FIB) microscope image showing EM-induced voids near cathode in M1 trench for an 60-nm wide interconnect with SiON filling layer.

6.3.4 Barrier Process and Thickness Effects on EM Reliability

The effects of barrier process and thickness were investigated for 60 nm lines at 240 ℃, with a current density of 1.0 MA/cm^2. The CDF plots are summarized in Figure 6.11 for two processes: barrier-first and pre-clean first, and for different barrier thicknesses. Overall, the barrier effect on EM lifetime was less significant than what was observed for Cu/low-k interconnects without SiON filling layer in chapter 3 due to the more robust SiON filling layer [66]. However, the standard deviation seemed to be correlated to barrier processing with the SiON filling layer. In particular, it was smaller for the samples that underwent the barrier-first process and had a 70 Å / 70 Å barrier.

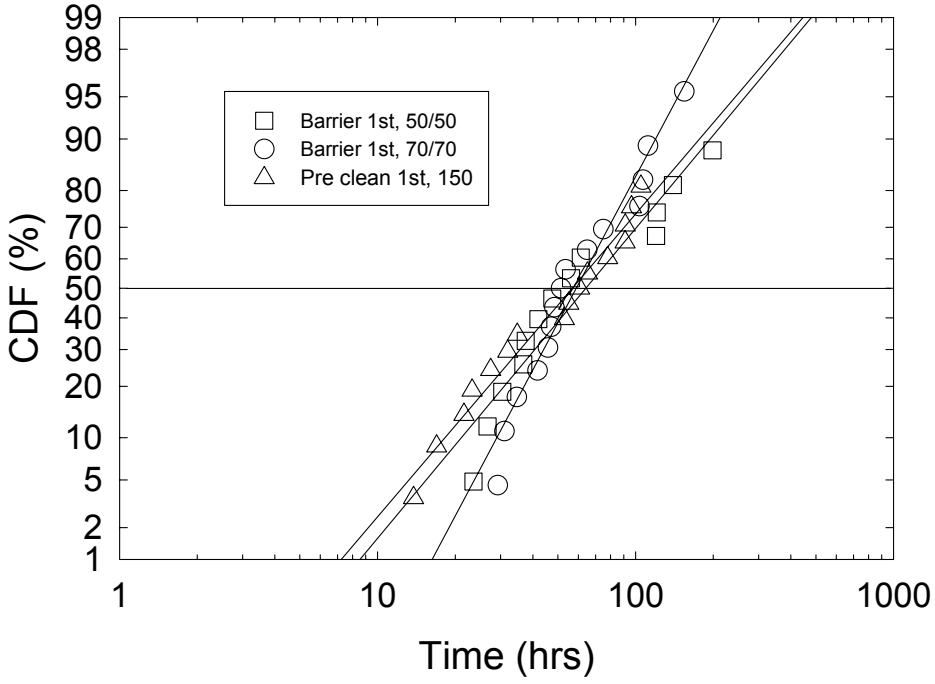

Figure 6.11 Cumulative failure distribution function (CDF) plots with different barrier processes and thicknesses for down stream electron flow for M1 width of 60 nm through SiON filling. EM tests were performed at 240 ℃, with a current density of 1.0 MA/cm^2.

6.3.5 Early Failure Behavior

To investigate SiON filling process effect on early failure, EM tests were performed using multi-linked EM test structures for down stream electron flow. The CDF plot of the EM test results, together with Monte Carlo simulation, is shown in Figure 6.12 for the 60-nm wide Cu interconnects with SiON filling. The CDF plot demonstrated approximately straight-line behavior for multi-linked structures with N=1, 10, and 100, indicating a mono-modal failure distribution for all cases. This result implies that no extrinsic factors such as process-induced defects, even if they existed, influenced this

failure. Therefore, process-induced defects in the via bottom, which were a primary cause of early failures, was no longer a factor affecting failure due to the distinct via/M1 interface configuration. The reason for the shortest life time for the N=100 samples is that, with the increasing number of line segments, the probability of failure at the weakest link for a given time increases. The experimental CDF plots did not correspond well with the Monte Carlo simulation result, suggesting statistical variations in line dimension and geometry with aggressive line scaling.

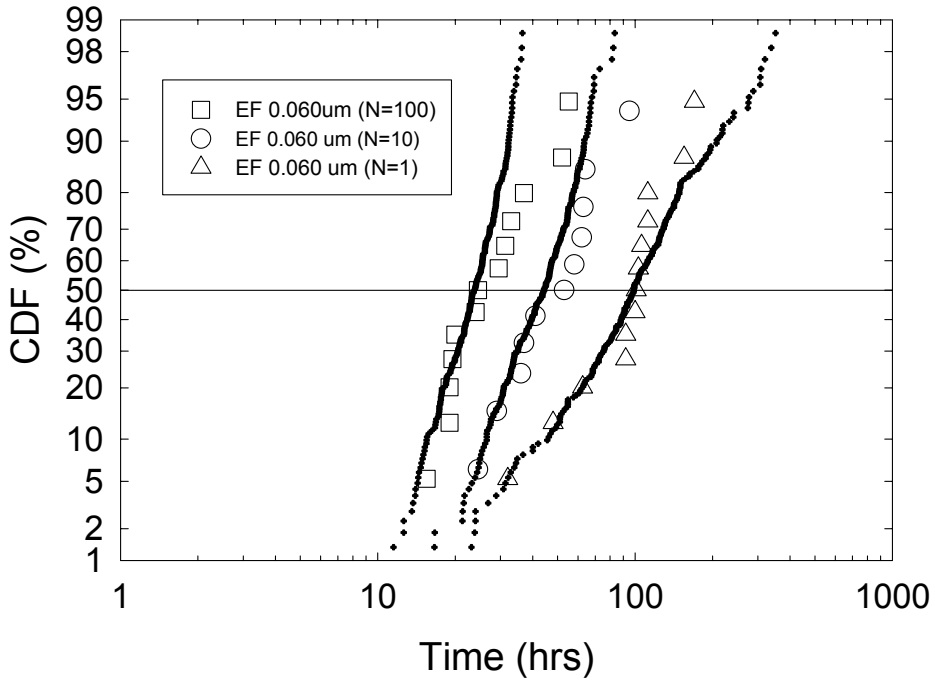

Figure 6.12 Cumulative failure distribution function (CDF) plots of multi-linked (EF) structures with different number of line segments for down stream electron flow for M1 width of 60 nm through SiON filling. EM tests were performed at 240 ℃, with a current density of 1.0 MA/cm^2.

6.3.6 Activation Energies and Current Density Exponents

To investigate the dominant diffusion mechanism for the test samples, EM tests were performed at various temperatures ranging from 210 ℃ to 290 ℃. Based on the EM lifetime data, the activation energies for Cu interconnects with 60-nm lines and 125-nm lines were determined and the results are shown in Figure 6.13. The activation energies Q, were obtained from fitting the experimental data to the Black's equation [73]. The activation energies were found to be in the range from 0.79 eV to 0.80 eV, indicating a similar interfacial diffusion mechanism for both M1 line widths in our test structures and no effect of the SiON filling process.

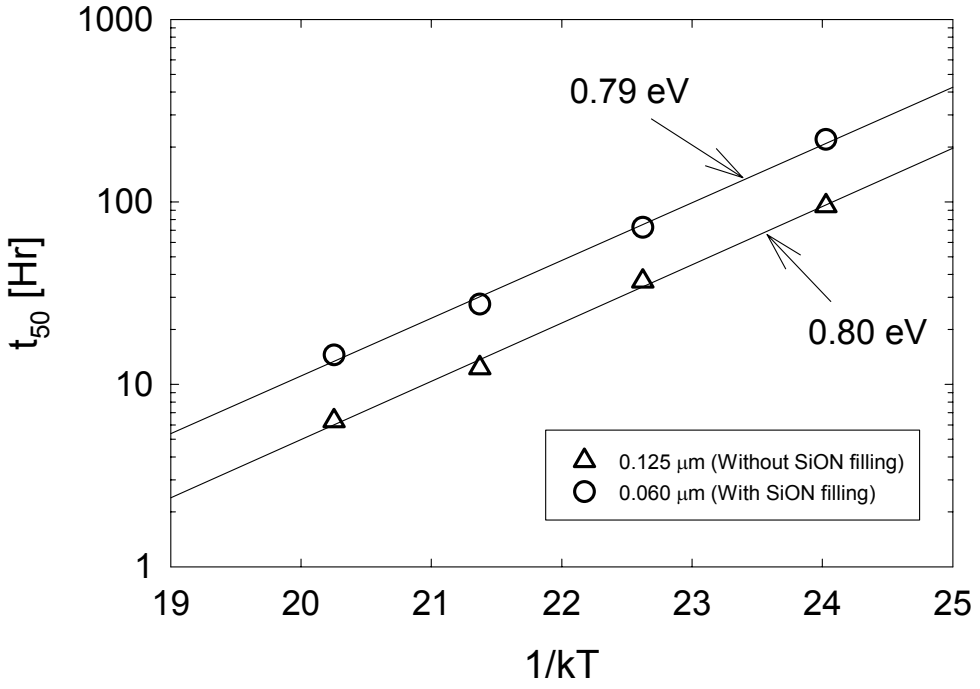

Figure 6.13 EM lifetimes as a function of test temperature for the Cu interconnects with different line widths under the current density of 1.0 MA/cm^2. The activation energies were found to be 0.79 eV and 0.80 eV for the fine lines and standard lines, respectively.

Current density exponent (*n*) values, using Equation 4.1, were obtained for the 60-nm and 125-nm lines at 240 ℃. The results are shown in Figure 6.14. The current exponents were found to be 1.44 and 1.88 for 125-nm lines and 60-nm lines, respectively, and the difference was deemed insignificant. In the case of Al interconnects, it is generally known that EM failure controlled by void growth shows a current exponent of 1 [83]. This implies that migration of void flux is directly proportional to electron flux. In contrast, EM failure controlled by nucleation of void yields a current exponent of 2 [84, 85]. Therefore, all EM failures will have the current exponent value falling between 1 and 2, because EM failure is controlled by both nucleation and growth of voids [86, 87]. The

experimentally obtained *n* values shown in Figure 6.14 agreed with the theoretical range of *n* value, between 1 and 2. However, there is no clear evidence to demonstrate that the Cu interconnect follows the same current density exponent behavior of Al interconnects. The effect of Cu microstructure did not contribute to the different *n* values observed, because the process conditions for the Cu lines were identical and the dominant EM mass transport mechanism was also identical, which was confirmed by activation energies shown in Figure 6.13.

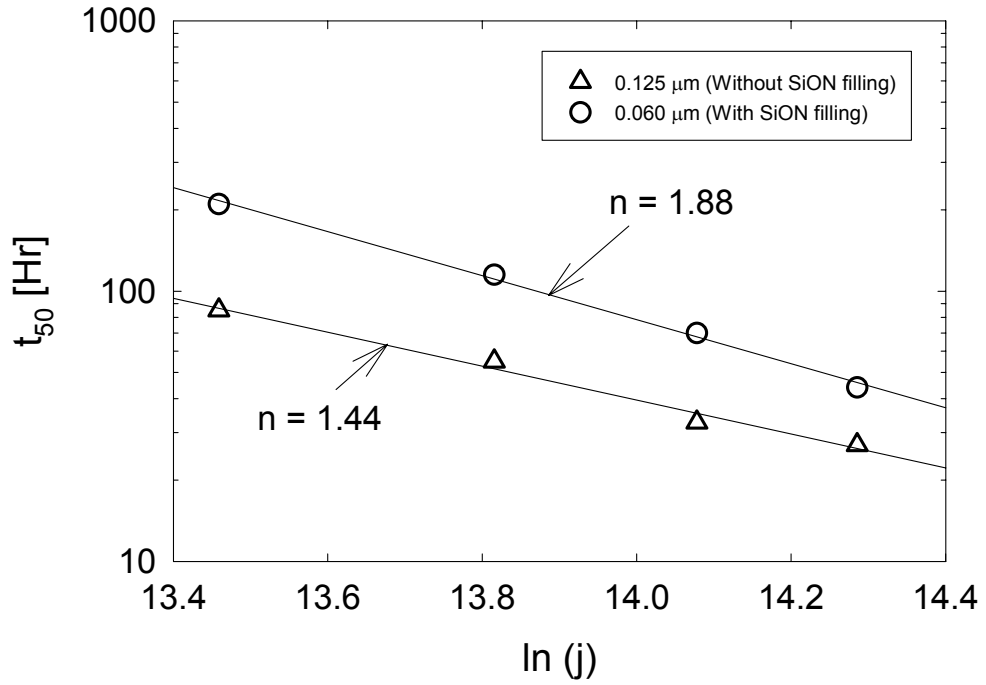

Figure 6.14 EM lifetimes as a function of current density for the Cu interconnects with different line widths at 240 ℃. The current density exponent values (*n*) were found to be 1.88 and 1.44 for the fine lines and standard lines, respectively.

6.4 SUMMARY

Cu interconnects with ultra fine M1 line were fabricated trench-filling method using SiON-filling layer in the dual damascene process and their EM reliability was investigated. Samples with 60-nm wide line by SiON filling showed longer lifetime, although a somewhat larger standard deviation resulted due to the early stage in the process refinement and aggressive line scaling. The longer lifetime can be attributed to the distinct interface structure between via and M1. In comparison, the control samples without SiON filling possessed a higher maximum current density concentration near the via bottom, which made such a current crowding zone more vulnerable to EM failure. This led to a shorter EM lifetime for the control samples. For the SiON-filled samples, EM test results using multi-linked structures showed clearly the absence of extrinsic early failure. This result suggests that the processing defects, which are the most probable cause for the early failures, was no longer a factor due to the distinct via/M1 interface structure. The activation energies were found to be in the range from 0.79 eV to 0.80 eV for both fine lines and standard 130-nm lines, indicating a similar interfacial diffusion behavior in both structures and not affected by the SiON filling process. The n values for 60-nm lines and 125-nm lines were found to be similar.

Chapter 7: Summary and Recommendations for Future Work

7.1 SUMMARY

With line scaling and implementation of low-k dielectrics in Cu damascene interconnects, EM becomes a serious reliability concern for the interconnects. Continuous shrinkage of device features increases the importance of surface diffusion due to the increasing ratio of surface and interface to volume of interconnects. The scaling effect on EM reliability for Cu/low-k interconnects based on a statistical approach using multilink test structures was investigated. This approach enabled one to quantify the failure statistics for the intrinsic strong-mode failures as well as for the extrinsic weak-mode failures. Two aspects of the scaling effect on Cu interconnects using statistical structures implemented with porous MSQ low-k dielectrics with k of ~ 2.3 were investigated. For the first part, the influences of barrier process and thickness scaling on the electromigration reliability including $(jL)_c$ product for Cu/low-k interconnects were studied. The second part of the study focused on EM failure statistics as a function of line width. Three line widths: 0.175, 0.125 and 0.090 μm, were studied corresponding to the 130, 90 and 65-nm nodes, respectively. Finally, SiON (siliconoxynitride) trench-filling process was introduced to fabricate ultra fine Cu lines (60 nm) at the metal-1 (M1) level, which is corresponding to 45-nm technology, to investigate further line scaling effect on EM reliability.

The effect of the barrier process on the electromigration reliability of Cu/low-k interconnects was investigated. Novel barrier-first process showed a mono-modal failure distribution indicating no extrinsic defect was involved in this failure. In comparison, the conventional pre-clean first process showed bi-modal failure distribution, suggesting that a small population of interconnects failed due to an extrinsic failure mode. This result

suggests that process-induced defects, which were the most probable cause of the early failures, were significantly reduced with the barrier-first process. TEM micrographs revealed a more uniform and thicker barrier layer at the via and trench with the barrier-first process than with the pre-clean first process. The pre-deposited Ta barrier protected the mechanically weak low-k dielectrics during Ar plasma etchback, leading to uniform via profiles, while contamination behind barrier and via erosion were found after the pre-clean first process due to Ar plasma damage of the dielectric. Barrier-first process showed higher $(jL)_c$ product value than that of pre-clean first process. The $(jL)_c$ product correlated well with the barrier thickness at the trench sidewall. The high $(jL)_c$ product effectively increased the drift velocity induced by back-flow stress (v_{BF}), thus reducing the net EM drift velocity (v_d). The reduced net drift velocity in turn prolonged the EM lifetime since it was inversely proportional to the net drift velocity, given that the interface between the Cu and capping layer was the dominant diffusion path for Cu/low-k interconnects fabricated by a dual damascene process.

Scaling effects of barrier thickness on EM lifetime and failure mechanism were investigated for Cu/porous MSQ interconnects. The $(jL)_c$ product was found to decrease with decreasing barrier thickness. This trend can be attributed to a decreasing confinement effect, which was correlated to an effective elastic modulus that was calculated using FEA. Results from the early failure test structures revealed a bi-modal failure distribution for samples with 75 Å and 100 Å barriers compared with a mono-modal failure distribution for samples with 175 Å barrier. FIB and TEM observations revealed that the weak-mode early failure in the thin barriers was caused by Cu out-diffusion through the thin Ta barrier, shorting out the test lines with the extrusion monitoring line. In addition, the observed FIB and TEM images revealed that Cu out-diffusion from the thin barrier was responsible for the gradual EM resistance increase

observed in test structures with the 100 Å Ta barrier compared with the abrupt EM resistance increase for 175 Å Ta barrier. The activation energies were found to be in the range from 0.90 eV to 0.95 eV independent of the barrier thickness, indicating a similar mass transport along the Cu/capping layer interface for EM.

The effect of via scaling on EM reliability was investigated for Cu/porous low-k interconnects with three line widths: 175, 125, and 90 nm. Two types (I and II) of test structures were designed for up-current EM testing. For type I structures where line width was scaled identical with via size, EM lifetime and failure statistics degraded with via scaling. This result was attributed to an intrinsic failure mechanism due to trench voiding driven by interfacial mass transport, where a critical void length in the order of via size was required for line failure. The trench voiding mechanism was confirmed by an up-current test of the type II structures with a constant via size but varying M2 width. Here, EM lifetime and the failure statistics were found to be independent of the M2 line width since the critical void length required for failure was fixed. In addition, down-current EM reliability was investigated using Type III test structures where the via size was scaled identical with M1 line width, decreasing from 175 nm to 125 nm. The EM lifetimes for 175 nm wide lines were longer than 125-nm lines. This result can also be attributed to the different critical void length. Since via width and M1 line width were identical, the critical void length, which was directly related to the via size, was longer for the 175-nm lines. A gradual increase in resistance was not found for down-current EM testing. The abrupt and substantial resistance increase in Type III can be associated with void formation underneath the via. Results of this study should provide useful guidelines for via and line scaling to improve EM reliability for Cu interconnects.

Ultra fine Cu interconnects were fabricated by dual-damascene process using trench-filling method with SiON layer. Samples with a 60-nm wide line showed longer

lifetime, albeit with somewhat larger standard deviation due to the early stage in the process refinement than the standard samples with a 125-nm wide line due to the distinct interface structure between via and M1. In comparison, the control samples without SiON filling possessed higher maximum current density concentration near the via bottom, which made current crowding zone more vulnerable to EM failure. This led to a shorter EM lifetime for the control samples. Samples with different M1 line widths were produced, all by filling with SiON material. With the identical line thicknesses, the down stream EM lifetimes were almost identical. The results were consistent with void formation in the M1 trench as observed by FIB and TEM. However, resistance changes were found to be dependent on the line width possibly due to the different grain structures. The barrier effect on EM lifetime was less significant for the samples with SiON filling layer than what was observed for Cu/low-k interconnects without SiON filling layer due to the more robust SiON filling layer than Ta layer. EM test results using multi-linked early failure test structures confirmed a mono-modal failure distribution for the 60 nm lines. This result suggests that the processing defects, which are the most probable cause for the early failures, was no longer a factor here due to the distinct via/M1 interface structure. The activation energies were found to be in the range from 0.79 eV to 0.80 eV for both fine lines and standard 125-nm lines, indicating a similar interfacial diffusion behavior in both structures and no effect of the SiON filling process. The n value for 60-nm lines and 125-nm lines were was found to be similar.

7.2 RECOMMENDATIONS FOR FUTURE WORK

Physical analysis for early failure needs to be investigated using the samples with high population of early failure. The early failure for this study was about 0.3 %, thus it was difficult to locate the early failure site to observe the nature of early failure. The location of void formation determines the failure mechanism. This indicates that the effect of Cu microstructures on EM reliability has to be investigated. The grain morphology, grain boundary direction, and grain orientation can be included in the Cu microstructure study.

The effect of line scaling on statistical $(jL)_c$ for fine lines constitutes an interesting research topic for future study. The observation of void at cathode using optical microscope came up short with line scaling. Therefore, a novel multi-linked EM test structure that enables to detect the location of void formation needs to be developed. Removing the passivation and capping layer can be another method to observe a cathode void using current EM structure. After removing the upper layer, a SEM observation for void in Cu interconnects needs to be done.

In this study, metal width and barrier thickness scaling was investigated. Reduction of metal height will be unavoidable for the future device to maintain reasonable aspect ratio for metal lines and vias. Therefore, the effect of metal height on EM reliability will be an interesting research topic. In addition, EM structures with different length of the reservoir for up-current electron flow condition were designed. The length of reservoir for the normal test structure was same as via size. However, new EM structures with 2, 3, 4, and 5-times longer reservoir length than standard EM test structure were designed. The line length and line width are identical to investigate the reservoir length effect. The comparison of EM statistics for different length of the reservoir would be a good research topic.

To reduce the effective *k* value, Cu capping with an organic material with lower *k* value than standard capping material, SiCN, was introduced. The linear relationship of EM activation energy with the intrinsic work of adhesion was reported [32]. Therefore, further investigation of the effect of organic capping material on EM reliability would be an interesting research topic in relation to the interfacial adhesion for the different capping materials.

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