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A Review on IGBT Module Failure Modes and Lifetime Testing

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ABSTRACT This article focuses on failure modes and lifetime testing of IGBT modules being one of the most vulnerable components in power electronic converters. IGBT modules have already located themselves in the heart of many critical applications, such as automotive, aerospace, transportation, and energy. They are required to work under harsh operational and environmental conditions for extended target lifetime that may reach 30 to 40 years in some applications. Therefore, addressing the reliability of IGBT modules is of paramount importance. The paper provides a comprehensive review on IGBT modules dominant failure modes, and long-term reliability. A detailed discussion on accelerated testing, and lifetime and degradation characterization considering thermo-mechanical stress is also presented in details.

INDEX TERMS Long-term reliability, IGBT failure modes, power cycling, lifetime models, degradation.

I. INTRODUCTION

According to field experience, power electronic converters are considered a weak link that has significant influence on overall electrical system reliability [1], [2]. In wind farms [3]–[5], power electronic converters used for energy conversion are responsible for about 13% of the failures and 18% of the downtime. In utility scale PV installation [6], [7], PV inverters cause about 37% of the unscheduled maintenance events.

In an industry-based survey [7], [9], semiconductor switches and capacitors are the most vulnerable components of the power converters. Unexpected overloads and system transients are main reasons for random failures, while thermal stresses followed by mechanical vibrations then humidity are the main causes for failures caused by long-term wear-out. According to motor drive manufacturers [10]–[12], drives may end up working in tough environments, which are impossible to know before leaving the factory; thereby qualification test conditions may not match field operation. As a result, motor drive component such as power switches usually do not satisfy their specified target lifetime.

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IGBT lifecycle passes through different stages [13]–[16]. It starts with qualification at the IGBT manufacturer site. Then through storage and transportation stage until it reaches the power converter manufacturer's facility. The module is then assembled into the converter and the whole system is tested for converter qualification. Afterwards, the converter is transported to the customer site for commissioning and operation. Mechanical, and temperature shock events, or incorrect handling and assembly of IGBT modules may take place before site commissioning [10], [16]. This may affects module's reliability and may cause early failures. In field, IGBT modules are subjected to a multitude of stresses [1], [17]–[20]. IGBT modules may fail due to random system overstress events such as overvoltage and overcurrent. Moreover, modules may fail under sustained loading conditions due to long-term degradation caused by wear-out failure modes.

Overstress and wear-out may cause IGBT modules to reach end-of-life early before the product target lifetime, which represents a serious challenge to both power converter and IGBT modules manufacturers [21]–[24]. The power converters manufacturers invest into improved converter design, control, and protection to mitigate the effect of system overstress events and demanding mission profiles

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on IGBT modules. Also, IGBT modules manufacturers invest in improved modules designs to withstand against harsher operating conditions.

In order to do so; both power converter and IGBT modules manufacturers respective to their targets adopt a design-for-reliability approach. This approach is meant to consider the knowledge of field failures, failure mechanisms, and the expected operational conditions into design stage. Addressing long-term reliability and making lifetime predictions is a key element in the design-for-reliability approach. Typically, accelerated lifetime tests are used in order to study long-term reliability issues. In these tests, IGBT modules are subjected to stresses higher than typical field conditions to accelerate wear-out failure modes [25]–[28].

This article provides a comprehensive review on the failure modes and long-term reliability of IGBT modules. In the first part of paper, field failure analysis is discussed in details including random failure modes, wear-out failure modes, and the interaction between different failure modes, their root causes, and their physics-of-failure. The second part of the paper provides a detailed discussion on IGBT modules' failures, accelerated lifetime testing, lifetime modes, and degradation characterization associated to electro-thermal stresses. Since a significant portion of IGBT modules' field failures are attributed to extensive electro-thermal stresses due to temperature cycling [1], [17]–[20]. The paper is organized as follows. To recap the underlying physics-of-failure, a brief review on the IGBT module's structure including chip and package is presented in section II. In section III, IGBT module failure analysis is discussed comprehensively. Section IV reviews IGBT modules' failures and reliability issues associated to electro-thermal stresses. Discussion on accelerated testing platforms is covered in section V. Section VI goes through detailed examination of long-term reliability characterization through accelerated testing. Then, section VII scrutinizes the concept of separation of failure modes. Section VIII concludes and discusses the challenges and trends.

II. IGBT MODULE STRUCTURE

A. IGBT CHIP

Typically, an IGBT chip or die is composed of several cells per chip area spaced by cell pitch [29]. The cell pitch and the number of cells per chip area determine the current density of the IGBT chip. Fig. 1 shows planar gate IGBT cells integrated to form a chip. Fig. 1a and 1b show linear and square-meshed polysilicon gate-connection layout, respectively. Gate-connection layout determines how multiple IGBT cells per unit area are connected together in parallel. Factors such as current density, cell technology, cell performance, and manufacturing affect the choice of gate. The interconnection of IGBT cells forms the active area of the device as shown in Fig. 1c. The polysilicon gate connections running across the chip underneath the emitter gate bonding pads are required to connect the gate terminal to external gate driver circuit.

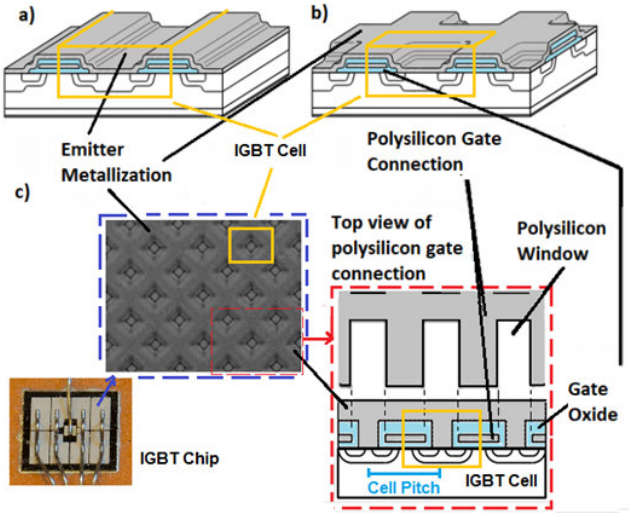


FIGURE 1. Cells layout [29]: a) linear gate connection, b) squared mesh gate connection, c) active area in zoom-in view.

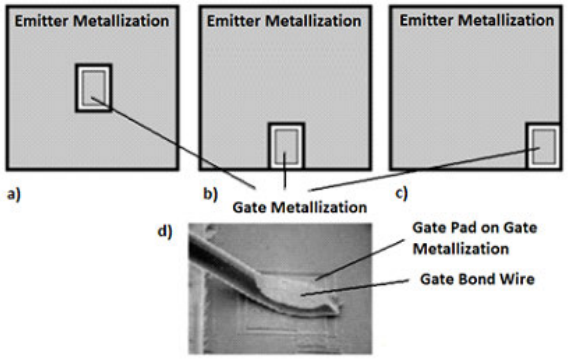


FIGURE 2. Gate metallization layout: a) centric b) edge, c) corner, d) gate metallization in zoom-in view [29].

Fig. 2a, 2b, and 2c show possible gate pad layouts. Fig. 2d shows aluminum gate bonding. The gate pad layout is determined based on the bond wire scheme used in the IGBT module design and it has an impact on the switching performance of the IGBT chip. The emitter metallization is made from aluminum alloy for aluminum wire bonding to form an electric connection between emitter and an external terminal. Most of the emitter metallization designs consider multiple bonding pads ordered in a matrix formation ($1\times1, 2\times2, 2\times3, 2\times4$ etc.) as shown in Fig. 3. The main reason behind having several emitter bonding designs is to ensure uniform current distribution on the emitter metallization and the bond wires, thereby, preventing the formation of hotspots [30]. On the other side of the chip, the collector metallization has three roles. First, it works as electrical connection between the collector and the package. Second, it acts as thermal interface between the die and the package [23]. Third, it functions as an adhesion layer between chip and the solder layer which is used to attach the chip to the package. Extra layers are added to the backside metallization to protect the die from

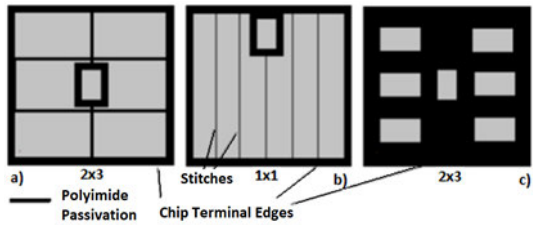


FIGURE 3. Common emitter metallization layouts [30].

contamination either by diffusion of particles coming from the solder or oxidation [23].

B. IGBT STANDARD MODULE

In IGBT modules, several IGBT chips and free-wheeling diode (FWD) chips are packaged together. One reason is to form new power electronic building blocks such as chopper, half-bridge, six-pack, etc. Another reason is to achieve higher current carrying capability through optimal paralleling IGBT cells and FWD cells of lower current carrying capability inside the module. In addition, the package provides electrical conduction paths between the IGBT/FWD chips and the external circuitry. Also, it transfers heat generated at the chips to a heat sink. Moreover, it provides a means for mechanical mounting and protection against environment.

Fig. 4a shows the architecture of a standard 34 mm IGBT module [31]. The module forms a half-bridge connection. Fig. 4b presents structure of the IGBT module [21]–[24]. The metallization layers on the top side of IGBT/FWD chips (dies) are connected to the top copper layer of DBC (direct bonded copper layer) through aluminum bond wires. This copper layer serves as power track to connect devices to each other and to module terminals. The metallization layers on the bottom side of the chips are soldered to the top copper layer of DBC. These solder layers are called die attach or chip attach which serves three functions. First, it conducts

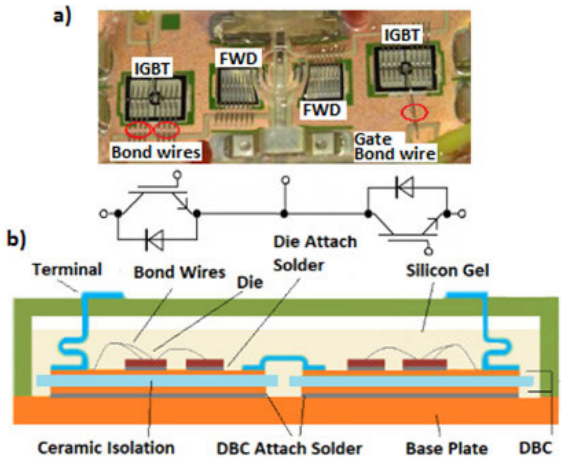


FIGURE 4. Power Module [31]: a) internal view of standard 34mm IGBT half bridge module, b) the structure of standard 34mm IGBT half bridge module.

current from the chips to top copper layer of DBC. Second, it transfers heat from the chips to DBC. Third, it fixes the chips into the DBC. DBC consists of two copper layers sandwiching a ceramic layer to provide electrical isolation between the chips and the base plate. DBC is soldered to a copper base plate. This solder layer is called DBC attach which serves two functions. First, it transfers heat from DBCs to the base plate. Second, it fixes DBCs to the base plate that is mounted on a heat sink [22], [23], [30], [32]. On mounting the module on the heat sink, thermal interface layer (TIM) is used to improve the thermal conductivity of the base plate to heat sink interface.

III. IGBT MODULE FAILURE ANALYSIS

As illustrated in the previous section, IGBT modules are complex structures of different material layers, which are brought together to form the chip and the package. Therefore, the failure of IGBT module is linked to many possible failure modes. However, there are dominant failure modes to which most of the failures are related. These failure modes can be categorized into two main groups: failure modes associated to chips and failure modes related to the package as shown in Table 1.

A. CHIP-RELATED FAILURE MODES

Chip-related failure modes can be further grouped into failures caused by overstresses and wear-out failures.

1) OVERSTRESS FAILURE MODES

Overstress failure modes are mainly due to events such as gate overvoltage, collector-emitter overvoltage, overcurrent, burnout due to cosmic rays [21], [34]. These events may cause bond wire lift-off or rupture, latch-up, loss of blocking capability, rapid rise in junction temperature (thermal runaway) due to energy shocks (high-energy dissipation), secondary breakdown in the inherent BJT structure of the IGBT [35], [41], [42]. These modes may destroy IGBT chips. Although in some cases, they cause the IGBT to show up as an open circuit, in majority of the cases IGBT ends to be a short circuit [23], [24], [35], [41], [42].

2) WEAR-OUT FAILURE MODES

The most common IGBT chip wear-out failure modes are Time Dependent Dielectric Breakdown (TDDB), and Hot Carrier Injection (HCI) [33], [34]. Both failure modes cause deterioration to the gate-oxide-layer characteristics. Nonetheless, according to [33], [34], these failure modes were considered an issue for IGBT in its old days and have not been issue anymore.

Another important wear-out failure mode is electro-chemical migration. In humid environments, under high voltage and temperature, electro-chemical migration at chip passivation layer and terminal structure cause an increase in leakage currents and gradual loss of blocking capability [36]–[40], [43]. Due to the importance of TDDB and

TABLE 1. IGBT failure mode classification.

Chip-related Failure Modes	Overstress [18, 19, 20, 21, 23, 35]	Gate overvoltage (Voltage breakdown)	System Effects: - Open circuit faults - Short circuit faults (Majority of the cases)
		Overvoltage (Voltage breakdown)	
		Overcurrent	
		Cosmic rays burnout	
	Wear-out [23, 33, 36-40]	Time dependent dielectric breakdown (TDDB)	System Effects: - Mal-operation of gate drivers & switches. - Loss of chip's voltage blocking capability
		Hot carrier injection (HCI)	
		Electro-chemical migration	
Package-related Failure Modes	Overstress [23, 24, 34]	Mechanical shock and stresses	System Effects: - Open, or short circuit faults - Accelerate wear-out - Melting & Burnouts (More common in harsh environments)
		Thermal shock	
		Thermal runaway & Flashovers	
	Wear-out [23, 24, 34,36-40]	Thermo-mechanical fatigue	System Effects: - Thermal issues (Majority of the cases). - Stray (leakage) current issues. - Loss of module's voltage blocking capability.
		Thermo-mechanical creep	
		Electro & electro-chemical migration	
		Insulation degradation	

electro-chemical migration since the dawn of IGBT, standard reliability demonstration tests have been designed to address them [23], [43].

B. PACKAGE-RELATED FAILURE MODES

Thermal shocks, mechanical shocks and stresses, and thermal runaways are the main causes of overstress package-related failures. For example, mechanical shock can cause degradation of package's internals, which compromises voltage blocking capability resulting in voltage breakdown [44], Another important cause for package overstresses is thermal runaway, that may occur under high temperature, resulting in melting of package interconnects [23], [24], [34]. In addition, in humid and contaminated environments, burnouts due to flashovers are more common [23], [24].

On the other side, thermo-mechanical fatigue, thermo-mechanical creep, electro-migration, and corrosion are the main causes of wear-out package-related failure modes [24], [34], [45]. Because of different coefficients of expansion between the package materials, temperature cycling inside the package results in thermo-mechanical fatigue. As a result, bond-wire cracks and lift-off; delamination and cracking of solder layers; and degradation of chip metallization may occur [34], [46]. Thermo-mechanical creep, caused by high operating temperature, leads to weakening of the mechanical strength of different package layers. This accelerates the process of cracks and voids formation [34], [47]. High currents cause electro-migration in bond wires and metallization layers, which leads to creation of voids and hot spots [34], [48]. High levels of humidity and corrosive chemicals existing in many industrial applications, e.g., mining, cement, oil and gas, and marine, may result in corrosion of bond wires accelerating their mechanical degradation, and eventually leading to their rupture [24], [34], [36]. In addition, humidity severely degrades the insulation characteristics of module encapsulation materials such as Si-gel [36].

C. FIELD FAILURE ANALYSIS

According to [1], [18] and the previous discussion, IGBT modules are described as one of the most vulnerable components in the power converters. However, ''vulnerable'' does not indicate inherent weakness, it indicates that power converter faults usually end to show up as IGBT modules' failures. Fig. 5 shows fishbone diagram representing field failures of IGBT modules [4], [20]–[24]. IGBT modules' field failures can be linked to manufacturing defects including chip defects, and module defects such as bond wire, solder, metallization, and insulation defects. Use and environmental conditions accelerate the latent defects into the failures [20]–[24].

Collector-emitter overvoltage may take place due to surges, control signal and measurement signal anomalies, and unexpected load condition [20], [24], [35]. Gate overvoltage may happen due to external surge, gate driver anomalies, and gate oscillation especially during short circuits [20], [24], [35], [37]. Overcurrent may occur due to internal or external faults, improper control actions, and unexpected load events [20], [24], [35].

In addition to overvoltage and overcurrent, thermal issues play a significant role in IGBT modules' field failures. They compromise both short-term and long-term reliability of IGBT modules depending on their magnitude. Energy shocks, thermal runaway, or secondary breakdown destroy IGBT modules in a short time scale [35], [49], [50].

Elevated operation temperatures and temperature cycling result in long-term issues such as the degradation of module interconnections, solder layers, and insulation layer [34], [45]–[47]. These thermal stresses may show up at the IGBT module due to defects in the cooling system design,

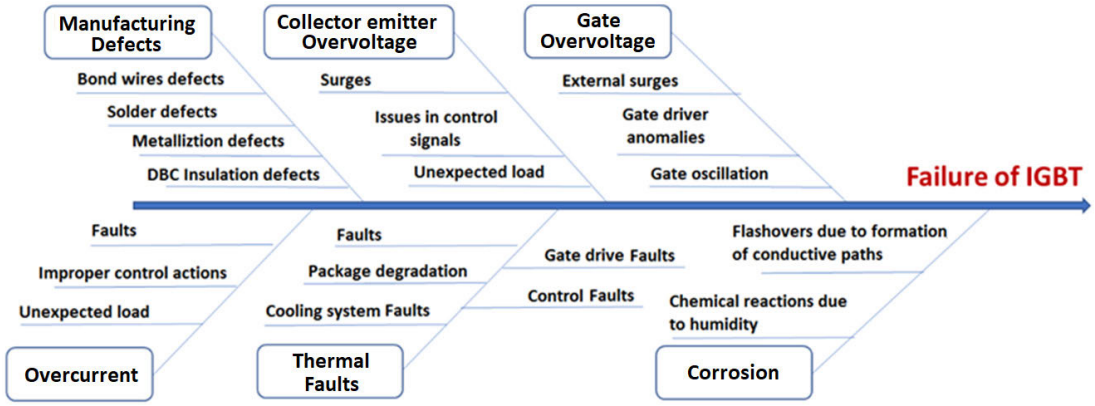


FIGURE 5. Fishbone diagram categorizing causes of field failures of IGBT modules.

improper operation of the cooling system, degradation of the thermal interface layer (TIM), improper gate voltage, gate open circuit, and abnormal switching speeds [51].

Corrosion driven by field environmental conditions is another important cause of IGBT modules' failures [34], [36]–[40]. Insufficient protection of the converter hardware against the environment leads to the build-up of salt traces and other conductive formations on IGBT module terminals and gate driver boards. They may cause flashovers and improper operation of gate driver. In addition, external particles assisted by humidity may get into IGBT modules and react with the internals, resulting in long-term degradation.

Fig. 6 presents samples of defective or failed IGBTs. Fig. 6a shows overvoltage failure. It causes a melting spot in the metallization where loss of blocking capability takes place. However, if loss of blocking capability associated with overvoltage results in overcurrent, wider scale melting happens. Fig. 6b shows large melting spots in metallization localized next to bond wires caused by overcurrent failure. In Fig. 6c, large scale melting of chip metallization and die-attach solder due to thermal runaway caused by high-energy dissipation during the fault. Fig. 6d shows cracks formed in DBC ceramic due to bending stress, which can arise from pressing the module's bowed base plate onto a flat heat sink. The development of these cracks eventually results in insulation failures. Fig. 6e shows gas bubbles formation in Si-gel under chip heating. This can lead to insulation failure due to Si-gel degradation, or the trapped gases can lead to aluminum corrosion. In Fig. 6f, weaker bond wires broke due to vibrational forces, while remaining bond wires fused due to current crowding. In Fig. 6g, bond wire lift-off took place under thermos-mechanical stresses. Fig. 6h shows defected bond wires due to manufacturing flaws, which compromises IGBT modules' reliability under thermo-mechanical stresses. Fig 6i shows IGBT chip passivation degradation due to electro-chemical migration. This reduces chip voltage blocking capability, and eventually, results in voltage breakdown. The following sections focus on long-term reliability issues

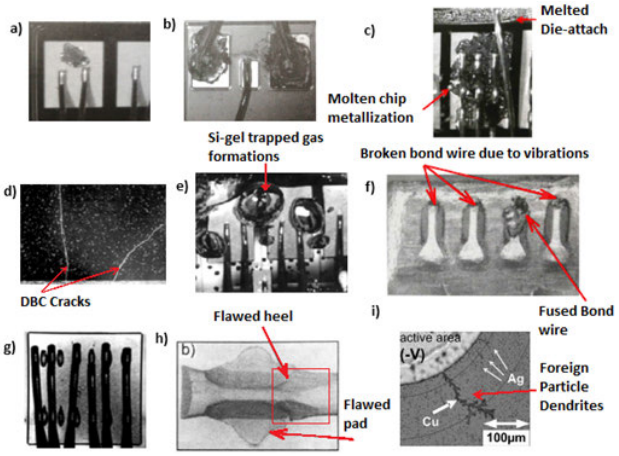


FIGURE 6. A sample of IGBT modules' field failures [23], [34], [40]: a) overvoltage, b) overcurrent, c) over-temperature, d) cracks in the ceramic layer due mechanical stresses, e) gases bubbles in Si- gel due to surface corrosion, f) cut-off of bond wires due to vibration, g) bond wire lift-off due to thermo-mechanical fatigue, h) defective IGBT module interconnections, and i) chip passivation degradation.

arising in the packages due to thermal stresses common in most applications.

IV. IGBT MODULE SUBJECTED TO THERMAL STRESSES

A. ANALYSIS OF THERMAL STRESSES IN MODULES

In normal operation, IGBTs keep switching between on and off states. Conduction and switching power losses associated with IGBT operation generate pulsating heat flux at the chip (junction). The repetitive heating and cooling of the junction results in temperature cycling. This temperature cycling caused by actively heating and cooling of the junction is called power cycling, while temperature cycling due to passive heating and cooling is called thermal cycling.

The heat flux produced at the junction flows through the thermal path across the different layers of the IGBT module towards the case (or heat sink). Since different layers of the IGBT module have different thermal conductivity and

capacitance as shown in Fig. 7, a temperature gradient along the thermal path takes place.

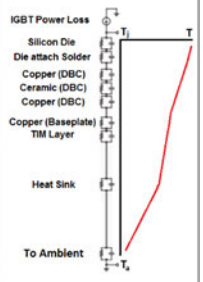
	Material	Conduct -ivity (W/mK)	Capacit -ance (J/kgK)	CTE (10^{-6}/K)	IGBT Thermal Network
Bond wire	Al-Alloy	220	896	23	
Metalli-zation					
Chip/Die	Si	100	741	3	
Die attach	Solder SnAg 3.5	28	-	57	
DBC attach					
DBC layer 1	Cu	380	381	17	
DBC layer 2					
Base plate					
DBC Ceramic	Al_2O_3	25	850-10^3	8	
	AlN	180	700-760	5	

FIGURE 7. Typical thermal properties of standard package materials and thermal network model of an IGBT [23].

Fig. 8 shows the temperature cycles at the junction and the case under power cycling. At the junction, average and the peak-to-peak temperature fluctuations are higher than that at the case. The thermal capacitance along the thermal path has a filtering effect on high frequency temperature fluctuations. Therefore, high frequency heating and cooling cause temperature fluctuations that increase in magnitude near the junction, and decrease near the case. On the other hand, the filtering nature of the thermal path is ineffective in front of the low frequency heating and cooling causing temperature fluctuations to be uniform throughout the thermal path as illustrated in Fig. 8. This filtering nature has a significant influence on the long-term reliability of the thermal path, which will be addressed later in section V.

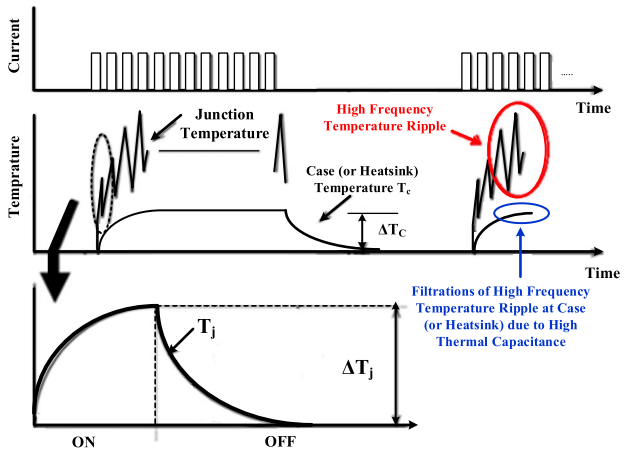


FIGURE 8. Temperature fluctuations at the junction and the case under repetitive heating and cooling of the junction [24].

Temperature fluctuations along the thermal path cause repetitive expansion and contraction of the layers forming the path. Due to the difference in the coefficient of thermal expansion (CTE) between adjacent layers in the package as shown in Fig. 7, shear stresses are exerted on interfaces between different material layers. These stresses result in thermo-mechanical fatigue of material layers of the package.

According to [52], even a package with identical CTE values in each layer would not be stress-free in the presence of a temperature gradient. It is impossible theoretically to design a stress-less package for the whole range of operation conditions. However, it is possible to optimize the selection of the materials properties of the adjacent layers to reduce stresses according to application requirements. For example, industrial modules typically use aluminum oxide as the ceramic layer and use copper base plates [23], [53]. To cope with higher thermal stresses and to account for more stringent reliability requirements, traction modules use aluminum nitride as the ceramic layer and aluminum silicon copper alloy for base plate [23], [53]. These material choices reduces the mismatch in the CTE along the thermal path [53]. However, this comes at the expense of more complex manufacturability and higher costs.

New interconnection and soldering technologies have been proposed by IGBT module manufacturers to improve long-term reliability of the module [54]–[60]. Some of these innovations are Copper bond wire, metallization and diffusion soldering used in .XT technology from Infineon [61]; and Al-clad Copper bonds, and silver sintering, baseplate-free in SKIM technology from Semikron [62]. The focus is not to produce a stress-free modules, their focus is to postpone the onset of degradation caused by thermo-mechanical fatigue beyond application lifetime requirement given the operation conditions.

B. MODULE FAILURE MODES DUE TO THERMAL STRESSES

Fig. 9 shows the interaction between several thermo-mechanical failure modes. These failure modes degrade the mechanical structure of the package and eventually cause IGBT module to fail [20], [21], [63]–[68]. Peak-to-peak temperature fluctuation at the junction degrades the bond wires due to fatigue as seen in Fig. 9a. Consequently, bond wire lift-off, heel cracks, or pad cracks take place depending on several factors including the geometry of the bond wires and the inherent manufacturing defects [34], [63]. Bond wire degradation results in increase of IGBT module collector-emitter voltage during on state due to the increase of the equivalent resistance of bond wires after the lift-off of some of them. This raises power losses, which increases the peak-to-peak temperature fluctuation at the junction causing an acceleration in degradation.

Bond wires fatigue is not a strong function of maximum or mean junction temperature. Conversely, solder degradation, metallization degradation, and bond wire stress corrosion depend strongly on junction temperature. Solder degradation is driven by temperature cycling [46], [47], [68], [69]. It either takes the form of solder cracks or solder delamination as shown in Fig. 9b. When solder temperature exceed its homologous temperature (2/5 of the solder melting point) [67], [70],

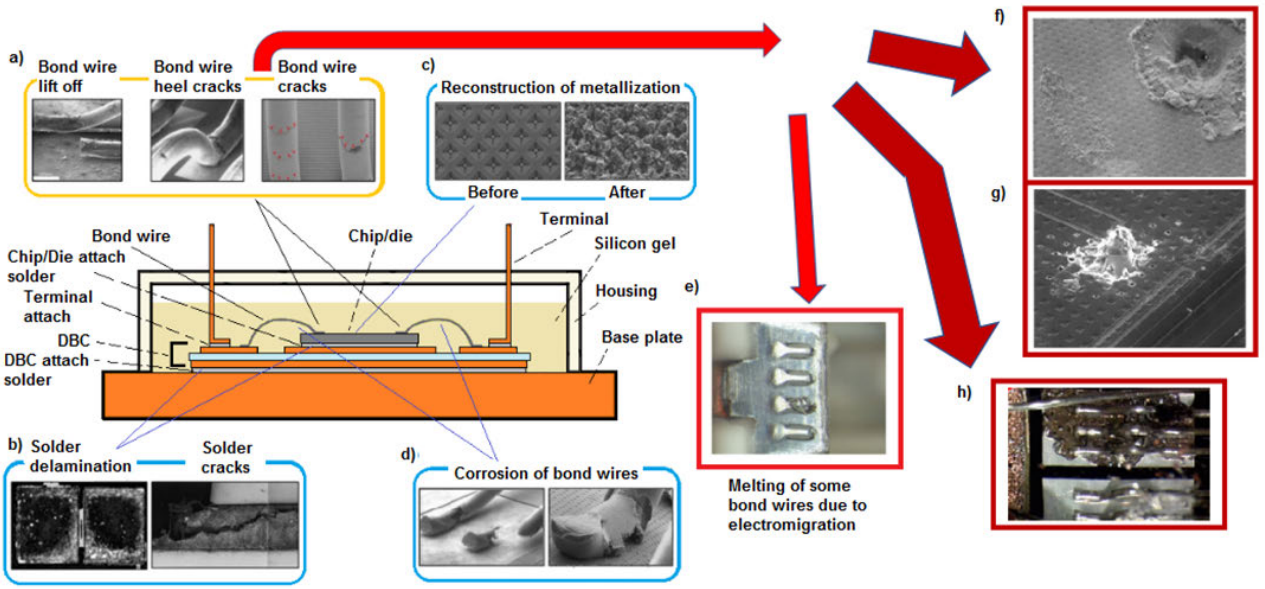


FIGURE 9. IGBT module degradation and related failures under thermal stresses [23], [34], [63]: a) bond wire degradation, b) solder degradation, c) metallization degradation, d) stress corrosion of bond wires, e) melting due to electro-migration, f) localized melting of the metallization near bond wire pads due to current crowding, g) localized melting of metallization due to hot stops formation, h) melting of metallization due to over temperature.

creep failure mechanism causes localized plastic deformation in sporadic sites. These creep sites lose strength as time proceeds accelerating the growth of micro cracks under cyclic loading, and eventually lead to solder cracks or solder delimitation. In addition to temperature value, temperature fluctuation frequency assists creep action accelerating solder degradation.

Metallization degradation takes the form of metallization reconstruction as shown in Fig. 9c. Due to the temperature cycling, tensile or compressive forces are imposed on the thin metallization layer due to the difference between the CTE of the chip and the metallization. According to [71]–[73], plastic deformation due to creep is the reason for reconstruction. There are three creep mechanisms, which are referred to as diffusion, gain boundary sliding, and dislocation creep in action. Each of these mechanisms is activated depends on certain factors including temperature. Reconstruction is more severe under elevated junction temperatures. The main consequence of reconstruction is the increase of metallization resistance raising the IGBT module's collector-emitter on-state voltage.

Corrosion of bond wires, shown in Fig. 9d, takes place due to the attack of traces of external chemicals on bond wires under elevated junction temperature. As a result, corrosion of the bond wire and their bond pads occur. Another corrosion mechanism called stress corrosion cracking do happen in bond wires under tensile stress. In this mechanism, cracks growth is driven by chemical reaction under sustained tension stress and elevated temperatures. First, it results in an increase in bond wire resistance and finally causes breaking of the bond wire. In both corrosion mechanisms, disruption of the current distribution occurs [34], [74].

C. INTERACTIONS BETWEEN FAILURE MODES

In real case situation, failure modes compete against and interact with each other to accelerate module degradation [21], [34], [75]–[78]. For example, solder degradation competes with bond wire degradation [34], [77]. The degradation of solder layer deteriorates the integrity of the thermal path causing an increase in thermal resistance. If the solder layer degradation dominates, the peak-to-peak fluctuation of the junction temperature will increase in a way that accelerates the degradation of the bond wire and accelerates the degradation of the solder as well. Failure modes keep accelerating one another until the complete deterioration of the package. Assuming a perfect solder layer that does not degrade, still the bond wires degrades due to temperature cycling. However, bond wire lift-off will start after a considerable time compared to the case when both bond wire degradation and solder degradation are present.

Another example is about the interaction between metallization degradation and bond wire degradation [35], [77]. Metallization degradation raises the resistance of the metallization leading to the increase of IGBT module collector-emitter on-state voltage. Consequently, power losses generated inside the junction increase raising the magnitude of the peak-to-peak temperature fluctuation. This in turn accelerates the bond wire degradation, which further elevates the junction temperature accelerating metallization degradation. In the end, this vicious cycle destroys the package mechanical structure. This concept of interaction and isolation of failure modes is discussed in more details in section VII.

As shown in Fig. 9, degradation of the bond wires, solder, and metallization eventually leads to more serious

consequences. Bond wire lift-off, heel cracks, or corrosion raises the current density in the intact bond wires. High current densities may cause electro-migration in the bond wires, which results in resistance increase of the intact bond wires. This gives rise to hot spots and finally leads to the melting of the bond wire as shown in Fig. 9e. Instead of the formation of the hot spots in the bond wires themselves, local hot spots may form at the bond wire pads. As a result, melting of the metallization near the intact bond wire takes place as seen in Fig. 9f. Another possibility for the formation of the local hot spots is shown in Fig. 9g, in which the current distribution formed by interaction of bond wire degradation and metallization reconstruction results in sporadic melting across the metallization. The damage shown in Fig. 9h may happen, when junction temperature reaches a level at which wide spread melting of the metallization layer starts. This may happen mainly due to severe degradation of the solder, however, it may also be caused due to wide scale metallization reconstruction.

V. ACCELERATED TESTING

A. POWER CYCLING TESTS

In order to assess long-term reliability of IGBT modules, accelerated testing is required to achieve the equivalent degradation, which may take many years in the field, in few days in lab setting [21]. Semiconductor manufacturers set reliability demonstration tests to display long-term reliability of their IGBT modules. Table 2 presents a selection of tests for standard IGBT modules to verify the long-term reliability under thermal stresses according to IEC 60749-34 [21], [23]. Power cycling tests (PCTs) can be grouped into PCT_{sec} in which the temperature cycling period (t_{cycle}) is set in the range of few seconds, and PCT_{min} in which t_{cycle} is in the range of few minutes. PCT_{min} is referred to as thermal cycling (TC) if the package is heated and cooled passively in a temperature chamber. Due to thermal capacitance of layers, few seconds are required to heat the core while few minutes are required to heat outer layers of the package as discussed in section IV. As a result, PCT_{sec} are intended to assess the reliability of bond wires, die attach solder, and metallization. PCT_{min} or TC are intended to assess the reliability of DBC attach, ceramic insulation, and mechanical assembly [21], [23], [75]–[77].

In order to keep track of degradation, degradation precursors are monitored. IGBT module collector-emitter on state (saturation) voltage is utilized as a precursor for bond wires degradation. Collector-emitter saturation voltage ($V_{CE,sat}$) measured at the IGBT module terminals is composed of IGBT chip collector–emitter saturation voltage and the voltage drop on the modules interconnects including bond wires and emitter metallization. As bond wires degrade, their equivalent resistance increases. This raises the collector-emitter saturation voltage ($V_{CE,sat}$) measured at the IGBT module terminals. IGBT chip collector-emitter saturation voltage is not affected directly by packaging degradation. However, it is affected by the increase in junction temperature caused by packaging degradation. For solder degradation, thermal resistance (R_{th}) is used as a precursor. The capability of solder layer to transfer heat from the chip to the base plate reduces in case of solder degradation, which is equivalent to the increase of overall R_{th}. It should be noted that a degradation in the thermal interface layer (TIM) increases the overall R_{th} as well. For gate oxide degradation either gate current (I_g) or gate threshold voltage (V_{th}) are used as precursors. End-of-life is reached if $V_{CE,sat}$ increases by 5%; R_{th} increases by 20%; I_g and V_{th} increase by 20% with respect to the initial healthy conditions [21], [23], [78]–[85].

In addition to reliability demonstrations, power cycling tests may be performed to study lifetime (number of stressor's cycles to a degradation limit for a given stressor level) and degradation modeling (evolution of degradation precursors with stressor's cycles under given stressor level) as seen in Fig. 10a and 10b, respectively, under a multitude of lab emulated stresses. Focusing on thermo-mechanical degradation, the stressor variable space is multidimensional including ΔT_j, T_{jmax}, t_{on}, I, etc. as shown in Fig. 10c [21], [78].

TABLE 2. Reliability demonstration for thermal stresses [21], [23].

Testing	Condition/Criteria	Failure Site
Thermal cycling (t_{cycle} ~ mins)	Internal heating, ΔT_j = 50-100K, $T_{j,max}$ = 150°C, t_{on} > 15 sec, R_{th}	- Bond wire - Die attach solder - DBC attach solder - TIM layer
Power cycling (t_{cycle} ~ secs)	Internal heating , ΔT_j = 50-100K, $T_{j,max}$ = 150°C, t_{on} < 5 sec, $V_{CE,sat}$, R_{th}	- Bond wire - Die attach solder

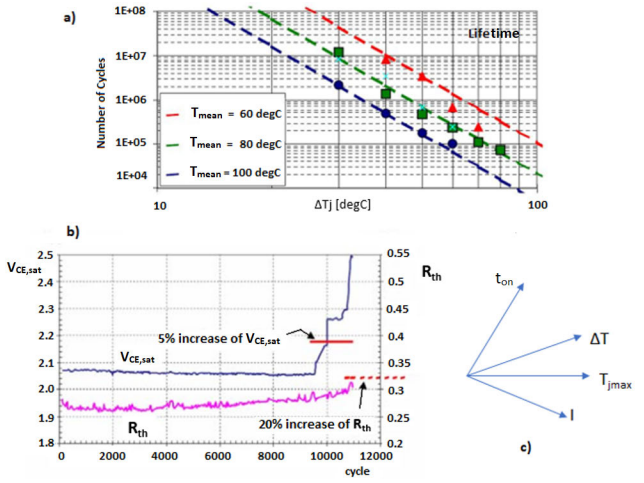


FIGURE 10. Accelerated tests: a) number of cycles to failure (time to failure) as a function of ΔT_j [78], b) variation of degradation precursors as a function of number of cycles [78], c) stressor variable [21], [78].

However, it should be noted that these variables are not independent. For example, increasing t_{on} raises the ΔT_j. Therefore, attention should be paid while setting test conditions to account for correlation of test variables.

Another important aspect of performing accelerated test for lifetime and degradation modeling is the use of stresses similar to, but higher in magnitudes than, stresses experienced by the component in the field. The purpose of applying the stresses is to accelerate one of the dominant failure modes that are seen by the component in the field.

Irrelevant stresses, either different from or of very high magnitude compared to expected field stresses, may give rise to failures that are not dominant in the field [15], [21].

B. POWER CYCLING PLATFORMS

In general, there is no standard architecture for power cycling tests [21], [86]–[89]. However, power cycling test platforms can be categorized into two main groups: DC and AC power cycling tests [90]–[92]. Table 3 compares between DC and AC power cycling tests.

In DC power cycling platforms, DC current injection induces thermal stress by forming a thermal flux in the module due to IGBT conduction losses only. In this test platform, IGBT module is kept turned on by supplying constant gate voltage, for instance 15 Volts. The required IGBT module collector current is periodically changed between zero and I with period t_{cycle} and duty cycle t_{on}/t_{cycle}. This is achieved by controlling the output voltage of the power supply connected between the collector and emitter terminals of the IGBT module, so that the required supply current is set. In addition to the main power supply, an auxiliary supply is required to flow a milliampere current through IGBT device collector for junction temperature estimation as will be discussed later in this section.

On the other side, in AC platforms, the IGBT is switched on and off repeatedly against high voltage, through imposing a PWM voltage signal to its gate terminal. Both conduction and switching losses generated in the junction creates a heat flux in the module resulting in thermal stresses. A possible implementation of AC testing platform comprises of two half bridge modules connected in H-bridge topology. Given the inductive load, the H-bridge is controlled to provide a sinusoidal current with fixed amplitude for time t_{on} and zero for t_{off}.

In comparison to DC platforms, AC platforms generate temperature cycles based on more realistic electrical stresses in power devices as they involve both conduction and switching losses and not only conduction losses. In addition, both IGBT and FWD losses contribute to the heating process, in contrast to DC test in which only IGBT losses contribute to the heating, which affects the temperature distribution inside the module. However, DC platforms are simple to set up, and more importantly, the monitoring of degradation precursors is much easier to implement. That is why semiconductor manufacturers adopt DC platforms, and most of the work on lifetime testing and degradation studies have been done using DC platforms [21], [23]. Accordingly, the focus of this article is on DC power cycling test. This does not mean that there is no interest in AC-based platforms. In fact, researchers are interested in AC platforms to study the effect of realistic electrical stresses on degradation and to compare to the degradation in case of using DC platforms. This is important for the verification of models generated from DC platforms [21], [28], [90], [91].

C. DC POWER CYCLING TESTS

In DC power cycling tests, as mentioned previously, IGBT current is switched on and off through an external circuit to produce repetitive heating and cooling in a constantly turned on IGBT. Additionally, in order to keep track of package deterioration, degradation precursors ($V_{CE,sat}$, R_{th}, and I_g) and test variables such as T_j, ΔT_j, and T_C need to be monitored.

1) TEMPERATURE ESTIMATION

There are several means to detect junction temperature including IR cameras, chip-embedded temperature sensors, etc. [93]–[100]. Nonetheless, more commonly, temperature sensitive electrical parameters (TSEPs) are used to estimate junction temperature without the need to specialized sensors. There are several candidates to employ as TSEPs such as collector-emitter saturation voltage, gate current, gate threshold voltage, etc [93]–[96]. $V_{CE,sat}$ is highly sensitive to temperature and relatively easy to measure, therefore, it is used frequently for estimating junction temperature.

Fig. 11a illustrates a typical temperature distribution across the chip. On using embedded temperature sensors, the position of the sensor on the chip affects the temperature measurements. Usually sensors are embedded in vicinity of gate

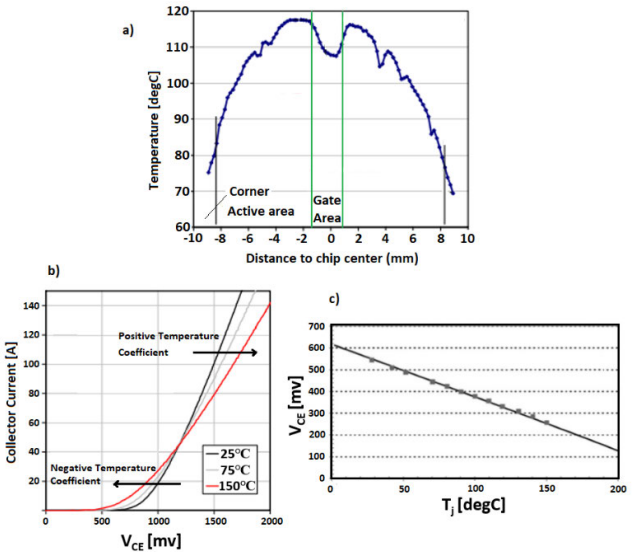
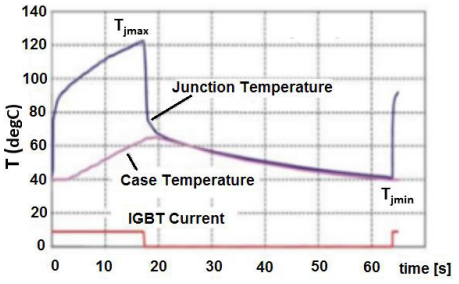
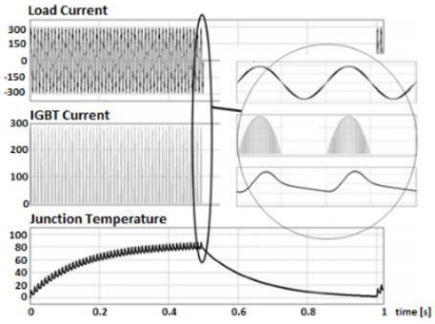
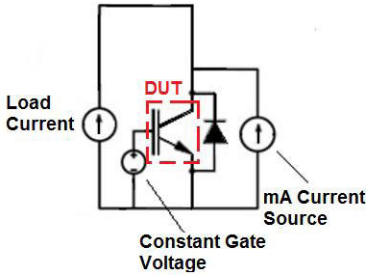
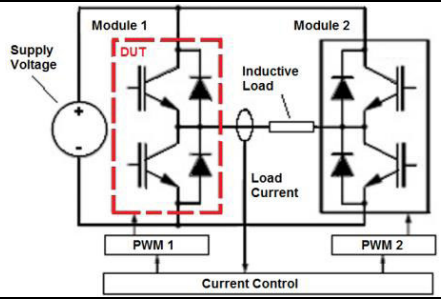
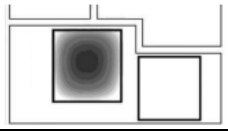
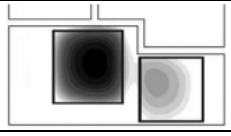
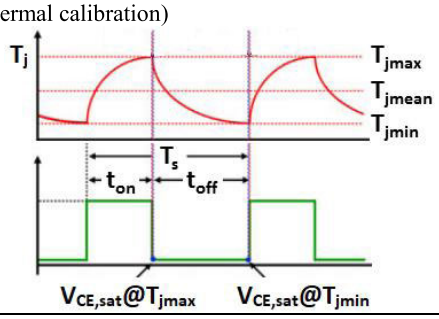
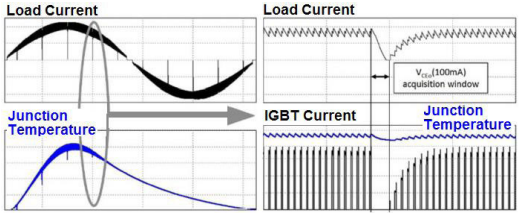
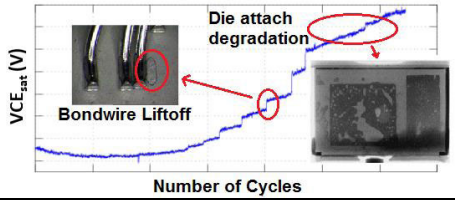
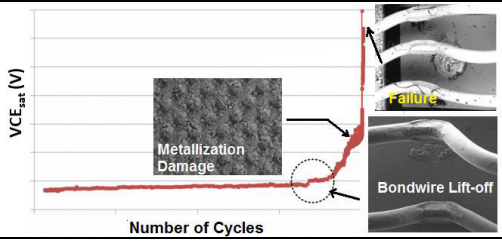


FIGURE 11. Junction temperature estimation through VCE_{sat} [21]: a) Temperature distribution across the chip, b) Relation between V_{CE} and collector current for 1200V 150A Trench field stop IGBT, c) Linear relationship between $V_{CE,sat}$ and temperature under milliampere range collector current excitation.

TABLE 3. Power cycling platforms.

	DC Platforms	AC Platforms
Power Cycle [77, 91]		
Circuit Setup [90, 91] (DUT: Device under Test)		
Heating & Stress [27, 63]	• Conduction losses • No switching and high voltage applied • Higher current than typical application levels are required to achieve a given power loss	• Conduction Losses and Switching Losses • Reproduce real application scenarios
Device under heating[27]		
Precursors [27]	($V_{CE,sat}$, R_{th}, I_g), Easier to Implement,	($V_{CE,sat}$, R_{th}, I_g), More Challenging to implement
Junction temperature monitoring [63]	$V_{CE,sat}$ measurement with low current after thermal calibration) 	$V_{CE,sat}$ measurement with low current after thermal calibration) 
Precursors measurement [27]	• Performed every cycle. • Structure function estimation performed every few thousand cycles (from 1000 to 5000, depending on the ageing process).	• Performed every few thousand cycles (from 1000 to 5000, depending on the ageing process) • PWM stopped and the high-voltage source disconnected. • A circuity for accurate low-level signals is used
Test Results [27, 101-103, 104]		

area, so they detect the temperature values at the gate area. For temperature estimation based on $V_{CE,\text{sat}}$, the measured value of temperature is equivalent to the average temperature across the chip area [99-99]. This average temperature value is commonly referred to as virtual junction temperature as shown in Fig. 11a. From now onwards, any reference to junction temperature is intended to indicate virtual junction temperature. In addition to the high sensitivity of $V_{CE,\text{sat}}$ with respect to temperature, it is sensitive to collector current.

Fig. 11b presents the relationship between $V_{CE,\text{sat}}$ and collector current. In order to isolate the effect of collector current on temperature estimation, $V_{CE,\text{sat}}$ measurement for temperature estimation should be done at very low collector current. This is achieved by sending milliampere range sense current during junction temperature estimation. This current depends on the IGBT's structure and size. Another reason for this milliampere range is that the IGBT is to be operated under the knee of its IV characteristics as shown in Fig. 11b. This guarantees a linear relationship between the junction temperature and measured $V_{CE,\text{sat}}$ as shown in Fig11.c. This relationship between temperature and $V_{CE,\text{sat}}$ is derived during the calibration process. At calibration, the IGBT module under test is kept in a temperature-controlled environment, $V_{CE,\text{sat}}$ is measured at different temperature set points while injecting the sense current into the IGBT module under test.

In addition to junction temperature, T_C is required for controlling test conditions and the estimation of R_{th}. Commonly PT100 sensors or thermocouples are used to measure T_C [21].

2) DEGRADATION PRECURSORS ESTIMATION

Fig. 12 presents a typical measurement sequence per heating-cooling cycle required to estimate degradation precursors ($V_{CE,\text{sat}}$, R_{th}, and I_g) and junction temperature [21]. $V_{CE,\text{sat}}$ is measured three times per cycle [21], [78], [110]. At time instant t_1, the supply current is diverted from the IGBT module under the test and is replaced with a milliampere current for $V_{CE,\text{sat1}}$ measurement. This is required to estimate the maximum junction temperature during the power cycle.

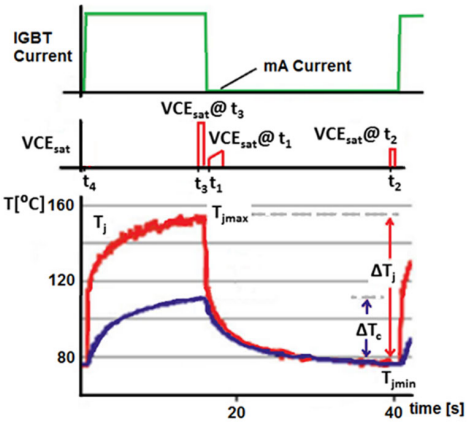


FIGURE 12. Measurements sequence for degradation precursors estimation [21].

$V_{CE,\text{sat1}}$ measurement should be taken just after diverting the main supply current. This ensures that the fall down of temperature after removing the supply is going to produce an error of less than few degrees in maximum junction estimation. Minimum junction temperature is estimated at time instant t_2 by measuring $V_{CE,\text{sat2}}$ and peak-to-peak junction temperature ripple can be calculated.

In order to use $V_{CE,sat}$ as a degradation precursor, $V_{CE,sat}$ should be measured under supply current and maximum junction temperature. Therefore, $V_{CE,\text{sat3}}$ measured at time instant t_3 is used. This ensures that the effect of bond wire degradation, and metallization degradation have been captured in the measured $V_{CE,\text{sat}}$. Also, it ensures capturing the degradation acceleration effect of junction temperature increase on both bond wire and metallization.

In order to estimate R_{th}, $V_{CE,\text{sat3}}$ is measured at time instant t_3 just before diverting the main supply current away from the IGBT. Knowing $V_{CE,\text{sat3}}$ and supply current, conduction power loss at time instant t_3 is calculated. R_{th} then can be estimated through dividing difference between maximum junction and case temperatures estimated at time t_1 by power loss estimated at time instant t_3. The trace of R_{th} with number of cycles can be used to track degradation in the thermal path.

A more insightful method to track degradation in the thermal path is through the estimation of the structure function of the package [101]–[109]. Fig. 13 illustrates the concept behind the structure function. It is a graphical representation of thermal network model estimated from transient thermal impedance. In order to estimate the structure function; after every N load cycles, where N can be fixed number or varied based on the degradation, the load cycles are halted. Subsequently, a current is injected into the IGBT module to heat the junction, then it is removed to let the junction to cool down. Based on the recorded transient variation of junction temperature, structure function is estimated. As the degradation increases with power cycling, changes in the estimated structure function take place as shown in Fig. 14.

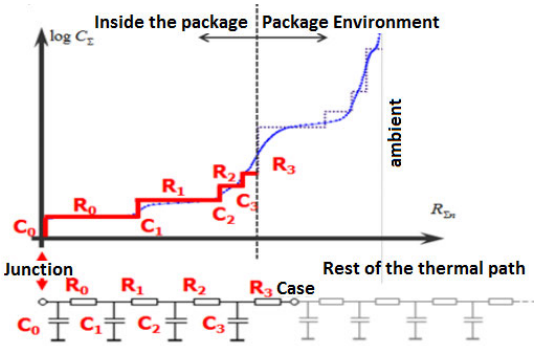


FIGURE 13. Conceptual illustration of structure function [109].

3) DC POWER CYLCLING CONTROL STRATEGIES

Four control strategies can be adopted while running DC power cycling test [110], [111]. These strategies are constant-turn-on-time, constant peak-to-peak case temperature,

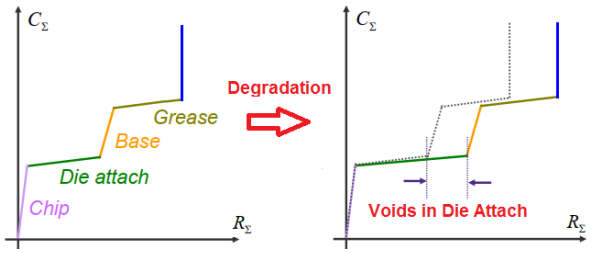


FIGURE 14. Depiction of how degradation affects the structure function [109].

constant power loss, and constant peak-to-peak junction temperature. The main idea behind these control strategies is to provide different degrees of compensation for degradation. Fig. 15 shows the number of cycles to failure under the four control strategies. Assuming an initial maximum junction temperature, as time goes through the test, the maximum junction temperature increases due to degradation. The increase in junction temperatures accelerates degradation until end-of-life as indicated by the degradation precursors.

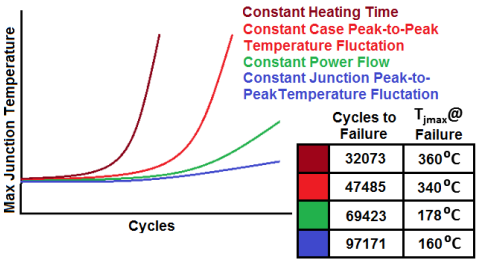


FIGURE 15. Junction temperature evolution with number of cycles due to degradation under different DC power cycling test control strategies [110].

Keeping the heating duty cycle constant is the harshest degradation scenario, as there is no compensation to reduce the rate at which degradation accelerates. This is equivalent to realistic degradation scenarios in the field. A weak act to slow down the rate of degradation is to fix the peak-to-peak case temperature. This reduces the rate of increase of peak-to-peak junction temperature and compensates for degradation in thermal interface layer (TIM). A stronger act to brake degradation rate is by fixing the dissipated power in the junction. This act compensates for the increase in power losses caused by increasing temperatures. The strongest way to cut down degradation rate is to fix peak-to-peak junction temperature. This compensates for package interconnections and thermal path degradation [110]. In sections VI and VII, PC tests are based on constant-turn-on-time control strategies.

VI. LIFETIME MODELS

Table 4 presents a summary for generic lifetime models associated with some important failure mechanisms. Lifetime models in this case are derived assuming that each failure mechanism works in complete isolation. This is not

TABLE 4. Lifetime models of important failure mechanisms.

Failure Mechanisms	Failure modes	Relevant Stressors	Lifetime Model
Fatigue	-Bond wire cracks. -Bond wire lift-off.	-Peak-to-peak temperature fluctuation	Empirical [112,113]
Surface Fatigue	-Metallization reconstruction	-Peak-to-peak temperature fluctuation -Temperature	Empirical [34, 113]
Solder Joint Fatigue	-Die-attach, -DCB-attach -Terminal lead -solder cracks and delamination	-Peak-to-peak temperature fluctuation -Temperature	Models based on Coffin-Manson [22, 113]
			Empirical as Norris-Landzberg [23, 24]
Ceramic Fatigue	-DCB substrate cracks	-Vibration -Mechanical Forces	Empirical [22, 34, 113]
Electro-Migration	-Void formation in bond wires metallization	-Current density -Temperature	Empirical as Black's law [32, 33, 113]

the case in the IGBT module. As was discussed before, several failure mechanisms compete until the end-of-life of the package. Thereby, IGBT specific lifetime models are required to capture the effect of competing failure mechanisms on life. In addition to the presence of interacting failure mechanisms, new package technologies entails changes in the manners by which the mechanisms interact [21], [23]. Therefore, in order to cope with technological advancements in package, IGBT module manufacturers run projects aiming for deriving empirical lifetime models for the state-of-art packaging technologies [21], [23]. This is required when the previous models predictions deviate from actual results of life tests as shown in Fig. 16.

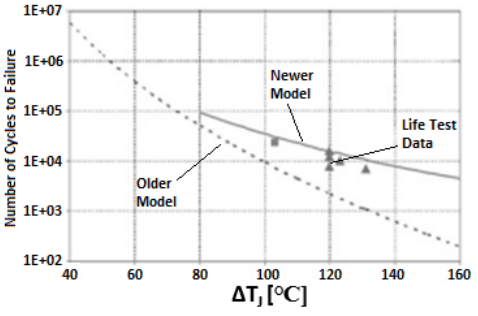


FIGURE 16. Comparison between the predicted number of cycles to failure and life test data [21].

M. Held *et al.* conducted one of the earliest attempts to generate an empirical lifetime model of IGBT module in LESIT project [21], [76], [114]. In this project, the effect of ΔT_j and t_{cycle} on module lifetime has been studied. Another attempt was done by R. Bayerer *et al.* and was published in

TABLE 5. Lifetime models of power modules under power cycling.

	LESIT [21, 77, 114]	CIPS 2008 [21, 115, 116]	SKiM63 [21, 117-120]
Test Variables	– ΔT_j – T_{jmean}	– ΔT_j, – T_{jmin} – t_{on} (heating time) – I (current per bond stitch on the chip) – V (voltage range of the device). – D (bond wire diameter)	– ΔT_j – T_{jmean} – t_{on} – ar (bond wire aspect ratio) – f_{diode} (effect of the difference in the chip thickness between igbt and fwd with same voltage class on lifetime)
Study Purpose	– Analyzing the effect of t_{cycle} on module life assuming bond wire lift-off is the main failure mode	– Analyzing the effect of different chip thicknesses, bond wires diameters, and numbers of bond wires per chip on module life.	– Analyze life of 100% solder-free modules.
Main Results	– The change of t_{cycle} causes approximately the same damage and failure modes. – Fast power cycling to reproduce millions of temperature changes in a short time. – Damage depends on $\Delta T_j, T_{jmean}$	– ΔT_j, T_{jmin}, and t_{on} alone cannot uniquely characterize the conditions of a power cycling test. – Stresses distribution and geometrical factors affects different degradation mechanisms differently.	– Degradation of the wire bond connection to the chip determines module lifetime. – The model is considered: a bond wire lifetime model.
Life Equation	$A\Delta T_j^{\alpha} e^{\left(\frac{E_a}{k_B \cdot T_{jmean}}\right)}$	$A\Delta T_j^{\beta_1} t_{on}^{\beta_3} I^{\beta_4} V^{\beta_5} D^{\beta_6} e^{\left(\frac{\beta_2}{T_{j\min}+273}\right)}$	$A\Delta T_j^{\alpha} ar^{\beta_1 T_j+\beta_0} \left(\frac{C+t_{on}^{\gamma}}{C+1}\right) e^{\left(\frac{E_a}{k_B \cdot T_{jmean}}\right)} f_{Diode}$
Usage	– Standard modules with Al_2O_3 substrates.	– Standard modules with Al_2O_3 substrates. – Not valid for modules built with AlN and AlSiC.	– Solder-free module.
Parameters	k_B [JK^{-1}] = 1.380 x 10^{-23} (Boltzman's constant) E_a [eV] = 0.618 (activation energy) α = -5.039 Packages built with 1990 technology	β_1 = -4.416, β_2 = 1285 β_3 = -0.463, β_4 = - 0.716 β_5 = -0.761, β_6 = -0.5 Packages built with 2000 technology	α = -4.923, β_1 = -9.012 x 10^{-3}, β_0 = 1.942 C = 1.434, γ = -1.208, E_a [eV] = 0.06606 f_{Diode}= 0.6204 Solder-free packages

CIPS 2008 [21], [115], [116]. In this work, a new model was proposed to cope with the advances in module technologies from the time of LESIT project. A large power cycling dataset from standard modules of different structures and geometries were analyzed.

In another important attempt, U. Scheuermann *et al.* developed the SKiM63 lifetime model based on power cycling test results performed with the SKiM63 solder-free module [21], [117]–[120]. Table 5 provides a comprehensive comparison between these models. The SKiM63 model is different from previous empirical lifetime models that do not differentiate between different failure modes [121]. If the dominant failure mode in the accelerated test differs from the dominant failure mode in the application. The extrapolation of the lifetime data generated from accelerated testing to applications conditions may lead to wrong lifetime estimations. Therefore, solder fatigue and wire bond degradation should be studied separately to isolate the individual impact on lifetime. SKiM63 lifetime model was a leading effort in the aim to separate failure modes. The main method to realize separation of failure modes is through combining advanced package technologies with classical technologies. Having so, lifetime of classical interconnections can be studied without interaction [21]. This will be discussed in detail in the next section.

So far, all lifetime models discussed are derived to represent IGBT module's lifetime subjected to identical power cycles. However, real applications are characterized by complex load profiles, resulting in complex junction temperature profiles as shown in Fig. 17a [21], [113], [12], [123], [124]. The first step for lifetime prediction is to decompose these complex profiles into sets of simpler identical power cycles as given in Fig. 17b. Commonly, this is achieved by Rainflow counting algorithm [94], [125], [126].

The second step is to estimate lifetime using cumulative degradation (damage) model [21], [23], [127], [128]. Fig. 17c summaries the process required to estimate lifetime of IGBT module subjected to electro-thermal stresses for a given mission profile. Mission profile data including load and climatic conditions (such as ambient temperature) are fed to the process. Device related characteristics (electrical and thermal) are then used to calculate IGBT module's losses and junction temperature profile. Consequently, the temperature profile is fed to cycles counting algorithms (such as Rainflow) to count junction temperature cycles at ΔT_j as shown in Fig. 17b. Then through using a lifetime model, for instance CIPS2008,

TABLE 6. Analytic cumulative degradation models.

Cumulative Damage Models	Characteristics	Model Equations
Linear damage rule (Miner's) [30, 113, 130]	• LDE, nLLD, nLSC, nLIC. • Analytic • Many Applications • Popular in IGBT lifetime). • Simplest	$D = \sum \frac{n}{N_f} = 1$
Double linear damage rule [113, 129, 130]	• LDE, LLD, LSC, nLIC. • Analytic • Many Applications • Simple	$D_I = \sum \frac{n}{N_I} = 1$ $D_{II} = \sum \frac{n}{N_{II}} = 1$ $N_I = f(N_f)$ $N_{II} = N_f - N_I$
Non linear damage rule [113, 120, 131]	• nLDE, LLD, LSC, nLIC. • Analytic • Some Applications	$D = \left(\frac{n}{N_f}\right)^{g(\Delta T_j)} = 1$
Crack growth[1] [113, 131, 132]	• nLDE, LLD, LSC, nLIC. • Some Applications • Complex	$\frac{da}{dN} = g\left(a, \Delta T_j, T_{j\max}\right)$ $D = \frac{a}{a_c} = 1$
Crack growth and retardation[2] [132 - 135]	• nLDE, LLD, LSC, nLIC. • Some Applications • Complex	$\frac{da}{dN} = C\left(\Delta T_j\right) * g\left(a, \Delta T_j, T_{j\max}\right)$ $D = \frac{a}{a_c} = 1$

LDE: linear damage evolution; LLD: load level dependent;
LSC: load sequence considered; LIC load interaction considered
[1]Damage is modeled as growth of a hypothetical crack.
[2]Damage retardation due to load interaction effect.

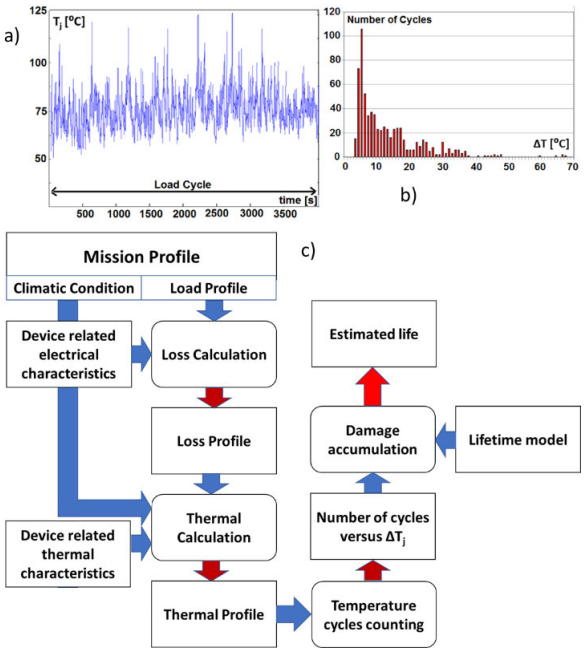


FIGURE 17. IGBT module's lifetime estimation, a) Junction temperature variations, b) Temperature variation peak counting, c) Lifetime estimation procedure (Rectangular boxes represent in/out data, Rounded cornered boxes represent calculation. Blue arrows represent input data flow. Dark red arrows represent output data flow. Red arrow represent the final estimation.)

number of cycles to failure at ΔT_j is calculated. Finally, the counted junction temperatures cycles at ΔT_j and number of cycles to failure at ΔT_j are fed to one of damage models shown in Table 6 to estimate the IGBT lifetime given the mission profile.

Miner's model, a popular damage model, assumes that the degradation caused by the contribution of each set can be aggregated linearly to obtain the accumulated damage. Nonetheless, factor such as the nonlinear relationship between cycle magnitude and damage, interaction between cycles, multiple damage stages, and, nonlinear damage evolution, limit the accuracy of prediction of lifetime made based on linear degradation theory. In addition, a modified Rainflow counting method should be used to account for load sequences. Table 6 summaries important analytic cumulative degradation models. Many cumulative degradation models have been proposed in fracture mechanics literature to account for limitations of using linear degradation rule. Nevertheless, linear degradation rule with simple Rainflow counting algorithm remains most widely used in IGBT lifetime estimation.

The estimated lifetime only considers the impact of power cycles. High humidity, corrosive environments and cosmic ray can lead to a much lower lifetime. Therefore, lifetime estimated based on power cycles represents an upper bound for the lifetime of power modules in a specific application [21].

VII. SEPARATION OF FAILURE MODES

The previous section has shed light on the importance of understanding the bond wire and solder degradation separately. This section discusses attempts to achieve this. One

attempt to study the effect of using different solders is provided in [136]. Although it does not entail an actual separation of failure modes, it represents a step to understand the interaction between bond wires and solder degradation under different solder degradation susceptibilities. For packages utilizing Pb-based solder, the number of cycles to failure along the whole range of ΔT_j is lower than that of packages based on Pb-free solder alloy as shown in Fig. 18. Focusing on packages with Pb-based solder; at lower values of ΔT_j, i.e. high values of T_{jmean}, given the same initial T_{jmax} for all test samples; solder degradation is dominant. However, at higher values of ΔT_j, bond wire degradation is dominant. On the other side, for packages with the Pb-free solder alloy, at lower values of ΔT_j, bond wire degradation is dominant. However, at higher values of ΔT_j, solder degradation is dominant. It is clear from the results shown in Fig. 18 that Pb-based solder behaves differently from the Pb-free solder. Pb-based solder degradation is caused by plastic deformation. It depends more on T_{jmean} than ΔT_j. On the other hand, the Pb-free solder alloy degradation is due to grain formation under thermal cycling, i.e. under higher ΔT_j.

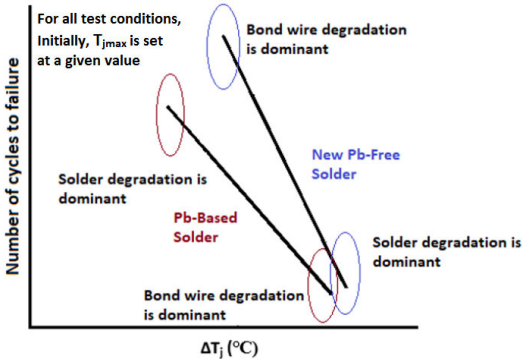


FIGURE 18. Comparison between the number of cycles to failure for samples using Pb-based solder and Pb-free solder [136].

In a study given in [137], two groups of samples of 1200 V base plate-less modules with 300 A nominal current were utilized. In group 1, silver sintered die attach and standard Al wire bonds of aspect ratio of 0.21 were used. In group 2, chips were soldered to the DBC using SnAg3.5 solder. For the chip top side contact, Al-clad copper wires were bonded to the standard Al chip surface. All samples of both groups were mounted onto identical water coolers using thermal grease as thermal interface layer (TIM). The test variables were set as follows: heating time (t_{on}) was set to 7 s, peak-to-peak junction temperature was set to 110 °C, and current was set to 300 A. Fig. 19 presents the number of cycles to failure as function of maximum junction temperature for the two groups. The results show that junction temperature only plays a minor role for the power cycling capability of Al-wire bonded sinter-modules. Conversely, it plays a major role for the power cycling capability of solder.

Fig. 20 shows test results for the same two groups subjected to another testing conditions in which t_{on} and either T_{jmax} or

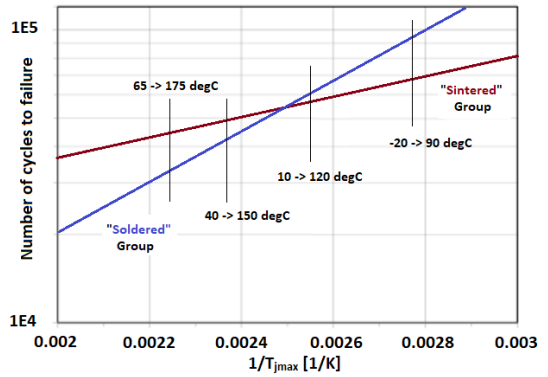


FIGURE 19. Comparison between the number of cycles to failure for "Soldered" group and "Sintered" group at different maximum junction temperatures [137].

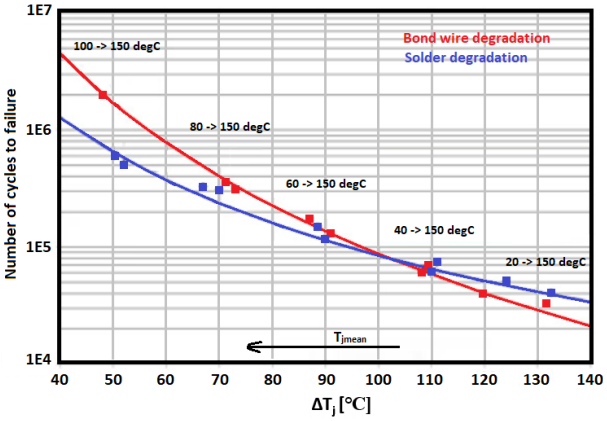


FIGURE 20. Comparison between the number of cycles to failure for "Soldered" group and the "Sintered" group at different junction temperatures [138].

T_{jmin} were the same in all tests ($T_{jmax} = 150$ °C or $T_{jmin} = 40$ °C, $t_{on} = 2$s) [138], while ΔT_j and consequently T_{jmean} were varied. It was shown that bond wire degradation is strongly dependent on ΔT_j and solder degradation is strongly dependent on T_{jmean}.

In [139], the impact of t_{on} has been analyzed. The t_{on} has been varied in a wide range. In one test, t_{on} was varied from 0.02 to 2 s, while ΔT_j was set to 70 °C and T_{jmax} was set to 150 °C. In the another test, t_{on} was varied from 2 to 10 s, while ΔT_j was set to 110 °C and T_{jmax} was set to 150 °C. For short t_{on}, the lifetime of the solder connection is lower than lifetime of the bond wire. However, for longer t_{on}, the lifetime of the solder surpasses lifetime of the bond wire. These results has shown that depending on t_{on}, different failure mechanisms in the solder layer take place.

What has been discussed previously has dealt with the number of cycles to failure. Now the discussion will focus on the evolution of degradation precursors, $V_{CE,sat}$ and R_{th}, through the power cycle test till the end-of-life indication is reached. Also, T_{jmax} can be used as a collective degradation precursor as the evolution of $V_{CE,sat}$ and R_{th} strongly

affects T_{jmax}. In a study given in [139], the impact of solder degradation and its interaction with the different bond wire failure modes has been addressed. For this, a set of samples with different chip-to-DBC solder joints and different bond wire geometries was prepared. The first group of samples (Soldered) was built with a chip solder layer using the standard SnAg-solder. For the other group (Sintered), the chip solder layer was replaced by an Ag-diffusion sinter layer. For both groups, the DBC-to-base plate connection was soldered using the same technology as the second group. In addition, there were samples of different bond wire aspect ratios among each group. The test has been set as follows: t_{on} was set to 1.2 s, ΔT_{j} was set to 70 °C, and T_{jmax} was set to 150 °C.

Fig. 21 presents the number of cycles to failure at different bond wire aspect ratios while also showing the dominant failure modes. At low bond wire aspect ratios, bond wire heel cracks are the dominant failure mode for both the Soldered and the Sintered groups. However, at high bond wire aspect ratios, bond wire lift-off is the dominant failure mode in Sintered group while solder degradation is the dominant failure mode in Soldered group.

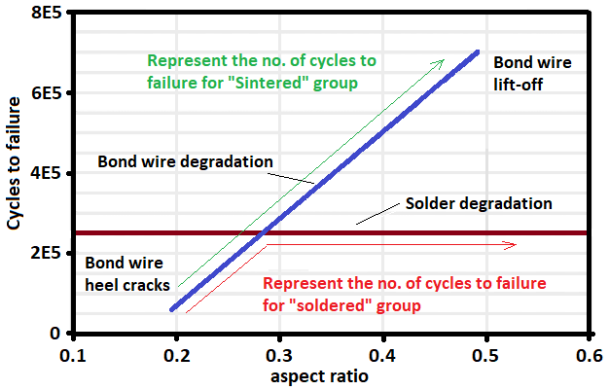


FIGURE 21. Comparison between the number of cycles to failure for "Soldered" group and the "Sintered" group at different bond wire aspect ratios [139].

Fig. 22a shows evolution of $V_{CE,\text{sat}}$ and T_{jmax} when the bond wire degradation is dominant. Bond wire degradation is characterized by abrupt change in $V_{CE,\text{sat}}$ and T_{jmax}. The evolution of $V_{CE,\text{sat}}$ and T_{jmax} associated with solder degradation is shown in Fig. 22b. Solder degradation is characterized by gradual change in $V_{CE,\text{sat}}$ and T_{jmax}. Table 7 summarizes degradation test outcomes under different test conditions.

In another study [101], [102], two tests were conducted on standard IGBT modules under constant heating current mode. In the first test, IGBT modules were in active mode and were subjected to a heating current of 25 A, initial power of 200 W, initial ΔT_j of 100 °C, t_{on} of 3 s, and t_{off} of 10 s.

Under these test conditions, IGBT modules' failures took place after about 35000 cycles and were attributed to die attach degradation as given by structure function results shown in Fig. 23a. In the second test, IGBTs were in saturation mode and were subjected to a heating current of 68 A,

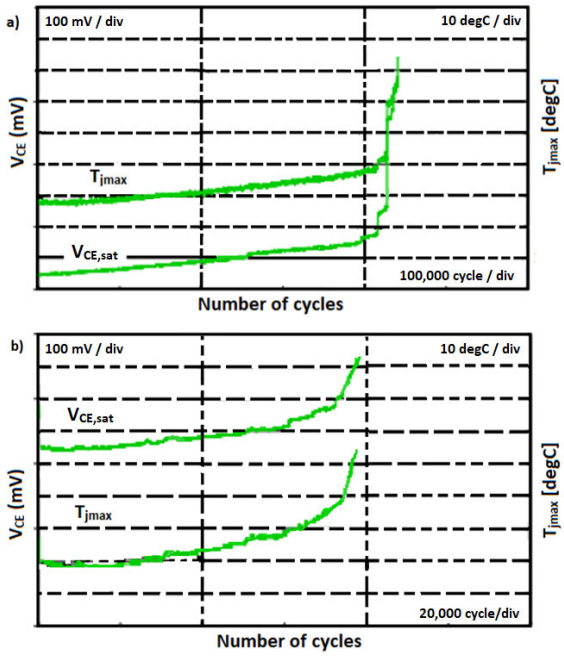


FIGURE 22. Comparison between time evolution of $V_{CE,\text{sat}}$ and T_{jmax} [139]: a) Bond wire degradation, (b) Solder degradation.

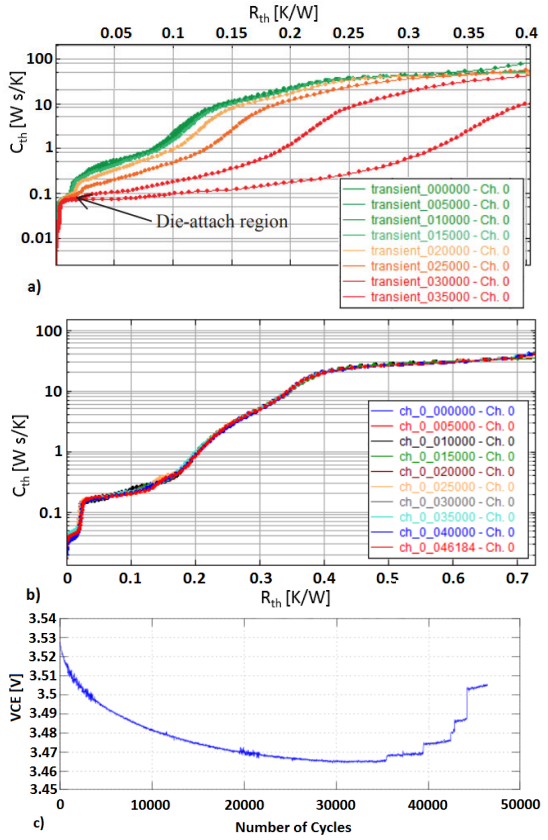


FIGURE 23. Comparison between structure functions and *VCE* [101], [102]: a) Test 1, structure function, b) Test 2, structure function, c) Test 2, VCE-time trace.

initial power of 240 W, initial ΔT_j of 105 °C, t_{on} of 3 s, and t_{off} of 17 s. IGBT modules' failures under these conditions occurred after about 46000 cycles. While there was no

TABLE 7. Degradation tests.

		Soldered Group	Sintered Group
Condition: • **Aspect ratio = 0.21** • **t_{on} = 2.1s** • **T_{jmax} = 150 °C** • **ΔT_j = 70 °C**	$V_{CE,sat}$ T_{jmax}	– Abrupt changes due to bond wire degradation – Bond wire degradation is dominant	– Abrupt changes due to bond wire degradation – Bond wire degradation is dominant
	End-of-life	About 80,000 cycles	About 80,000 cycles
Condition: • **Aspect ratio = 0.48** • **t_{on} = 2.1s** • **T_{jmax} = 150 °C** • **ΔT_j = 70 °C**	$V_{CE,sat}$ T_{jmax}	– Gradual change due to solder degradation – Abrupt changes due to bond wire degradation accelerated by solder degradation – Solder degradation is dominant	– No solder degradation – Negligible bond wire degradation below 200,000 cycles – Abrupt changes due to bond wire degradation near 600,000 cycles – Bond wire degradation is dominant
	End-of-life	About 200,000 cycles	About 600,000 cycles
Condition: • **Aspect ratio = 0.48** • **t_{on} = 13.6s** • **T_{jmax} =150 °C** • **ΔT_j = 110 °C**	$V_{CE,sat}$ T_{jmax}	– Bond wire degradation and solder degradation are interacting – Both failure modes assist each other to accelerate degradation	– No solder degradation – Abrupt changes due to bond wire degradation – Bond wire degradation is dominant
	End-of-life	About 40,000 cycles	About 50,000 cycles

evidence for degradation in the estimated structure functions as given in Fig. 23b, the trace of $V_{CE,\mathrm{sat}}$ showed jumps that are attributed to bond wire degradation as indicated in Fig. 23c. A possible explanation for the difference in failures modes is due to the difference in t_{off} resulted in the difference in T_{jmean}, and higher T_{jmean} accelerates solder degradation as discussed previously. In addition, higher currents in the second test may have led to emitter reconstruction accelerating the increase of $V_{CE,sat}$.

VIII. SUMMARY AND DISCUSSION ON CHALLENGES AND TRENDS

A comprehensive review on the faults and long-term of IGBT modules has been presented. First, IGBT modules are complex devices in terms of structure and packaging. In addition, high portion of IGBT modules' failures are originated in other converter system components, but significantly reflect on IGBT modules causing their failures. Furthermore, they are subjected to complex mission profiles that vary based on the application. As a result, IGBT modules suffer multitude of failure modes.

Classifying, separating these failure modes, and understanding the underlying physics of failure are crucial for improving the reliability of IGBT modules and the converters as a whole.

According to field experiences and comprehensive failure analyses; IGBT modules' failures modes accelerated by thermal stresses, due to repetitive heating and cooling, dominates their end-of-life. Long-term reliability assessment of IGBT modules subjected to thermal stresses is required. This assessment includes: analyzing thermal-induced failures, assessing new module designs, and generating lifetime and degradation models.

In order to assess long-term reliability, typically accelerated tests are performed. These tests are commonly performed using DC-based platforms. The emerging trend is to adopt AC-based platforms, as they generate more realistic stresses. However, they are more complex. Therefore, the ongoing researchers' interest is not to replace DC-based platforms with AC-based ones [21], [90], [91]. Nonetheless, they aim to utilize AC-based platforms to verify degradation and lifetime data generated from DC-based platforms under realistic electrical stresses.

Lifetime modeling is required to predict IGBT modules lifetime. There are two lifetime modeling approaches: empirical and physics-based lifetime models. Empirical models require experience and large power cycling tests datasets; they correlate the number of cycles to failure to the parameters of PC tests, such as T_{jmax}, t_{cycle}, t_{on}, etc. Lifetime estimations based on these models are valid under the specific test conditions on which the models have been generated. In order to make life prediction under normal operation conditions using these models, extrapolations to field conditions are required. There are issues regarding these extrapolations. Dominant failure mode at test conditions and field conditions may differ. Also, extrapolations cannot be validated experimentally. However, these extrapolations could be validated through simulation-based power cycling [21], [140].

Simulation-based power cycling and lifetime prediction is another emerging approach, that has grabbed the attention of many research groups [21], [88], [127], [140], [141]. In this approach, physics-based models are required to represent various deformation mechanisms. Given that, modeling of the stress and strain development inside the module is realized, then the deformation development is correlated to the number of cycles to failure. Although it is a simulation-based

approach, still, these models require validation and parameterization through experimental tests. Another important issue with physics-based models is that they are not suited to simulate complex mission profiles. These models involve finite element analysis to compute the internal stressors for each external load cycle, which is difficult to achieve in case of complex mission profiles. As a result, the common belief among researchers is that progress in both empirical and physics-based modeling approaches is required to achieve better lifetime estimation under field conditions.

REFERENCES

[1] H. Wang, M. Liserre, and F. Blaabjerg, "Toward reliable power electronics: Challenges, design tools, and opportunities," *IEEE Ind. Electron. Mag.*, vol. 7, no. 2, pp. 17–26, Jun. 2013.
[2] S. Peyghami, P. Palensky, and F. Blaabjerg, "An overview on the reliability of modern power electronic based power systems," *IEEE Open J. Power Electron.*, vol. 1, pp. 34–50, 2020.
[3] M. R. Wilkinson, "Reliability profiles (methods)," (Project Deliverable), ReliaWind Deliverable D.1.2., EU FP7 Reliawind Project, Tech. Rep. ReliaWind D.1.2.
[4] E. Wolfgang, "Examples for failures in power electronics systems," presented at the ECPE Tutorial 'Rel. Power Electron. Syst.', Nuremberg, Germany, Apr. 2007.
[5] K. Fischer, K. Pelka, A. Bartschat, B. Tegtmeier, D. Coronado, C. Broer, and J. Wenske, "Reliability of power converters in wind turbines: Exploratory analysis of failure and operating data from a worldwide turbine fleet," *IEEE Trans. Power Electron.*, vol. 34, no. 7, pp. 6332–6344, Jul. 2019.
[6] L. M. Moore and H. N. Post, "Five years of operating experience at a large, utility-scale photovoltaic generating plant," *Prog. Photovolt., Res. Appl.*, vol. 16, no. 3, pp. 249–259, May 2008.
[7] M. Shahzad, K. V S Bharath, M. A. Khan, and A. Haque, "Review on reliability of power electronic components in photovoltaic inverters," in *Proc. Int. Conf. Power Electron., Control Autom. (ICPECA)*, New Delhi, India, Nov. 2019, pp. 1–6.
[8] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An industry-based survey of reliability in power electronic converters," *IEEE Trans. Ind. Appl.*, vol. 47, no. 3, pp. 1441–1451, May 2011.
[9] J. Falck, C. Felgemacher, A. Rojko, M. Liserre, and P. Zacharias, "Reliability of power electronic systems: An industry perspective," *IEEE Ind. Electron. Mag.*, vol. 12, no. 2, pp. 24–35, Jun. 2018.
[10] K. Tikkanen. *Why Do Variable Speed Drives Fail and How We Test Them?* Accessed: Mar. 18, 2017. [Online]. Available: https://new.abb.com/drives/media/why-do-variable-speed-drives-fail-and-how-do-we-test-them
[11] K. J. P. Macken, I. T. Wallace, and M. H. J. Bollen, "Reliability assessment of motor drives," in *Proc. 37th IEEE Power Electron. Spec. Conf.*, Jun. 2006, pp. 1–7.
[12] K. Ma, U.-M. Choi, and F. Blaabjerg, "Prediction and validation of wear-out reliability metrics for power semiconductor devices with mission profiles in motor drive application," *IEEE Trans. Power Electron.*, vol. 33, no. 11, pp. 9843–9853, Nov. 2018.
[13] K. C. Kapur and M. Pecht, *Reliability Engineering*. Hoboken, NJ, USA: Wiley, 2014.
[14] M. G. Pecht, *Prognostics and Health Management of Electronics*. Hoboken, NJ, USA: Wiley, 2008.
[15] P. O'Connor and A. Kleyner, *Practical Reliability Engineering*. Hoboken, NJ, USA: Wiley, 2012.
[16] C. V. Pop, A. Buzo, G. Pelz, H. Cucu, and C. Burileanu, "The estimation of the lifetime variation for power devices," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 4, pp. 654–663, Dec. 2019.
[17] C. Bhargava, P. K. Sharma, M. Senthilkumar, S. Padmanaban, V. K. Ramachandaramurthy, Z. Leonowicz, F. Blaabjerg, and M. Mitolo, "Review of health prognostics and condition monitoring of electronic components," *IEEE Access*, vol. 8, pp. 75163–75183, 2020.
[18] H. S. Chung, H. Wang, F. Blaabjerg, and M. Pecht, *Reliability of Power Electronic Converter Systems*. Edison, NJ, USA: IET, 2015.
[19] A. Hanif, Y. Yu, D. DeVoto, and F. Khan, "A comprehensive review toward the State-of-the-Art in failure and lifetime predictions of power electronic devices," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4729–4746, May 2019.
[20] X. Perpiñà, *Reliability and Lifetime Prediction for IGBT Modules in Railway Traction Chains*. Rijeka, Croatia: InTechopen, 2012.
[21] J. Lutz, *Semiconductor Power Devices: Physics, Characteristics, Reliability*. Cham, Switzerland: Springer, 2018.
[22] A. Wintrich, *Application Manual Power Semiconductors*. 2nd ed. Nuremberg, Germany: SEMIKRON International GmbH, 2015.
[23] A. Volke and M. Hornkamp, *IGBT Modules: Technologies, Driver and Application*. Neubiberg, Germany: Infineon Technologies AG, 2017.
[24] *Fuji IGBT Modules Application Manual*. Accessed: Mar. 2015. [Online]. Available: https://www.fujielectric.com/products/semiconductor/model/igbt/application/box/doc/pdf/REH984c/REH984c.pdf
[25] K. A. Gray and J. J. Paschkewitz, *Next Generation HALT and HASS: Robust Design of Electronics and Systems*. Hoboken, NJ, USA: Wiley, 2016.
[26] P. Cova and F. Fantini, "On the effect of power cycling stress on IGBT modules," *Microelectron. Rel.*, vol. 38, nos. 6–8, pp. 1347–1352, Jun. 1998.
[27] V. Smet, F. Forest, J.-J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani, "Ageing and failure modes of IGBT modules in high-temperature power cycling," *IEEE Trans. Ind. Electron.*, vol. 58, no. 10, pp. 4931–4941, Oct. 2011.
[28] C. Durand, M. Klingler, D. Coutellier, and H. Naceur, "Power cycling reliability of power module: A survey," *IEEE Trans. Device Mater. Rel.*, vol. 16, no. 1, pp. 80–97, Mar. 2016.
[29] B. J. Baliga, *The IGBT Device Physics, Design and Applications of the Insulated Gate Bipolar Transistor*. Amsterdam, The Netherlands: Elsevier, 2015.
[30] W. W. Sheng and R. P. Colino, *Power Electronic Modules: Design and Manufacture*. Boca Raton, FL, USA: CRC Press, Sep. 2004.
[31] P. Sun, C. Gong, X. Du, Y. Peng, B. Wang, and L. Zhou, "Condition monitoring IGBT module bond wires fatigue using short-circuit current identification," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3777–3786, May 2017.
[32] G. Harman, *Wire Bonding in Microelectronics*. New York, NY, USA: McGraw-Hill, 2010.
[33] M. Ohring and L. Kasprzak, *Reliability and Failure of Electronic Materials and Devices*. Amsterdam, The Netherlands: Elsevier, 2015.
[34] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectron. Rel.*, vol. 42, nos. 4–5, pp. 653–667, Apr. 2002.
[35] R. Wu, F. Blaabjerg, H. Wang, M. Liserre, and F. Iannuzzo, "Catastrophic failure and fault-tolerant design of IGBT power electronic converters–an overview," in *Proc. IECON*, Vienna, Austria, Nov. 2013, pp. 507–513.
[36] C. Papadopoulos, C. Corvasce, A. Kopta, D. Schneider, G. Pâques, and M. Rahimo, "The influence of humidity on the high voltage blocking reliability of power IGBT modules and means of protection," *Microelectron. Rel.*, vols. 88–90, pp. 470–475, Sep. 2018.
[37] C. Abbate, G. Busatto, A. Sanseverino, D. Tedesco, and F. Velardi, "Measure of high frequency input impedance to study the instability of power devices in short circuit," *Microelectron. Rel.*, vols. 88–90, pp. 540–544, Sep. 2018.
[38] S. Kremp and O. Schilling, "Humidity robustness for high voltage power modules: Limiting mechanisms and improvement of lifetime," *Microelectron. Rel.*, vols. 88–90, pp. 447–452, Sep. 2018.
[39] D. Cimmino, R. Busca, S. Ferrero, F. Pirri, G. Richieri, and R. Carta, "High voltage temperature humidity bias test (THB) customized system and methodologies for reliability assessment of power semiconductor devices," *Microelectron. Rel.*, vols. 100–101, Sep. 2019, Art. no. 113319.
[40] C. Zorn and N. Kaminski, "Acceleration of temperature humidity bias (THB) testing on IGBT modules by high bias levels," in *Proc. IEEE 27th Int. Symp. Power Semiconductor Devices IC's (ISPSD)*, Hong Kong, May 2015, pp. 385–388.
[41] H.-G. Eckel and L. Sack, "Experimental investigation on the behaviour of IGBT at short-circuit during the on-state," in *Proc. 20th Annu. Conf. IEEE Ind. Electron. (IECON)*, Bologna, Italy, Sep. 1994, pp. 118–123.
[42] A. S. Bahman, F. Iannuzzo, C. Uhrenfeldt, F. Blaabjerg, and S. Munk-Nielsen, "Prediction of short-circuit-related thermal stress in aged IGBT modules," in *Proc. IEEE Energy Convers. Congr. Expo. (ECCE)*, Milwaukee, WI, USA, Sep. 2016, pp. 1–7.
[43] M. Mueller and J. Franke, "Innovative approach of efficient high humidity and high temperature reverse bias testing as significant qualification method for power electronic modules," in *Proc. IEEE 20th Electron. Packag. Technol. Conf. (EPTC)*, Singapore, Dec. 2018, pp. 116–119.

[44] X. Zhang, M. Wang, X. Li, Z. Ding, C. Ma, G.-Q. Lu, and Y. Mei, "A method for improving the thermal shock fatigue failure resistance of IGBT modules," *IEEE Trans. Power Electron.*, vol. 35, no. 8, pp. 8532–8539, Aug. 2020.

[45] M. Liedtke, G. Khatibi, B. Czerny, and J. Nicolics, "Thermomechanical reliability investigation of insulated gate bipolar transistor module," in *Proc. 41st Int. Spring Seminar Electron. Technol. (ISSE)*, Zlatibor, Serbia, May 2018, pp. 1–7.

[46] H. Yongle, L. Yifei, X. Fei, L. Binli, and T. Xin, "Physics of failure of die-attach joints in IGBTs under accelerated aging: Evolution of micro-defects in lead-free solder alloys," *Microelectron. Rel.*, vol. 109, Jun. 2020, Art. no. 113637.

[47] V. Samavatian, H. Iman-Eini, Y. Avenas, and M. Samavatian, "Effects of creep failure mechanisms on thermomechanical reliability of solder joints in power semiconductors," *IEEE Trans. Power Electron.*, vol. 35, no. 9, pp. 8956–8964, Sep. 2020.

[48] M. L. Mysore, R. Bhojani, J. Kowalsky, J. Lutz, R. Baburske, H. Schulze, and F. Niedernostheide, "Al modification as indicator of current filaments in IGBTs under repetitive SC operation," *IET Power Electron.*, vol. 12, no. 15, pp. 3893–3902, Dec. 2019.

[49] T. Yong, W. Bo, and Q. Pang, "Research on breakthrough failure of IGBT chip," in *Proc. IOP Conf.: Earth Environ. Sci.*, vol. 223, 2019, Art. no. 012025.

[50] T. Yong, W. Bo, and Q. Pang, "Thermal breakdown failure mechanisms of IGBT chips," in *Proc. IOP Conf.: Earth Environ. Sci.*, vol. 223, 2019, Art. no. 012024.

[51] U.-M. Choi, S. Jorgensen, and F. Blaabjerg, "Impact of cooling system capacity on lifetime of power module in adjustable speed drives," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 3, pp. 1768–1776, Sep. 2019.

[52] U. Scheuermann and R. Schmidt, "Impact of solder fatigue on module lifetime in power cycling tests," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Aug./Sep. 2011, pp. 1–10.

[53] T. Herrmann, M. Feller, J. Lutz, R. Bayerer, and T. Licht, "Power cycling induced failure mechanisms in solder layers," in *Proc. Eur. Conf. Power Electron. Appl.*, Sep. 2007, pp. 1–7.

[54] N. Heuck, K. Guth, M. Thoben, A. Mueller, N. Oeschler, L. Boewer, R. Speckels, S. Krasel, and A. Ciliox, "Aging of new interconnect-technologies of power-modules during power-cycling," in *Proc. 8th Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, Feb. 2014, pp. 1–6.

[55] K. Guth, D. Siepe, J. Görlich, H. Torwesten, and R. Roth, "New assembly and interconnects beyond sintering methods," in *Proc. PCIM Eur.*, 2010, pp. 232–237.

[56] S. Hartmann, V. Sivasubramaniam, D. Guillon, D. E. Hajas, and R. Schuetz, "Packaging technology platform for next generation high power IGBT modules," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2014, pp. 1–7.

[57] K. Guth, N. Heuck, C. Stahlhut, and A. Ciliox, "End-of-life investigation on the .XT interconnect technology," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2015, pp. 1–8.

[58] K. Liu, E. Yao, J. Yang, Y. Wang, and X. Hu, "The research and development of Soldering materials applied in IGBT modules packaging," in *Proc. IOP Conf.: Mater. Sci. Eng.*, vol. 740, 2019, Art. no. 012055.

[59] A. S. Khaja, "Diffusion soldering for high-temperature packaging of power electronics," Ph.D. dissertation, Dept. Mech. Eng., Univ. Erlangen-Nuremberg, Erlangen, Germany, 2018.

[60] N. Jiang, Z. Li, C. Li, Q. Wang, S. Zhang, and Y. Lin, "Bonding wires for power modules: From aluminum to copper," in *Proc. IEEE Int. Conf. Electron Devices Solid-State Circuits (EDSSC)*, Xi'an, China, Jun. 2019, pp. 1–3.

[61] A. R. Stegner, T. Auer, and A. Ciliox, "Next generation 1700 V IGBT and emitter controlled diode with .XT technology," in *Proc. PCIM Eur.*, 2014, pp. 1–8.

[62] E. Milke, R. Schmidt, and U. Scheuermann, "Al-clad Cu wire bonds multiply power cycling lifetime of advanced power module," in *Proc. PCIM Eur.*, 2012, pp. 776–783.

[63] U.-M. Choi, F. Blaabjerg, and S. Jorgensen, "Power cycling test methods for reliability assessment of power device modules in respect to temperature stress," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2531–2551, Mar. 2018.

[64] J. Lutz, T. Herrmann, M. Feller, and R. Bayerer, "Power cycling induced failure mechanisms in the viewpoint of rough temperature environment," in *Proc. 5th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2008, pp. 1–4.

[65] L. Feller, S. Hartmann, and D. Schneider, "Lifetime analysis of solder joints in high power IGBT modules for increasing the reliability for operation at 150 °C," *Microelectron. Rel.*, vol. 48, nos. 8–9, pp. 1161–1166, 2008.

[66] W. Wu, M. Held, P. Jacob, P. Scacco, and A. Birolini, "Thermal stress related packaging failure in power IGBT modules," in *Proc. Int. Symp. Power Semiconductor Devices IC's: (ISPSD)*, May 1995, pp. 330–334.

[67] W. Wu, M. Held, P. Jacob, P. Scacco, and A. Birolini, "Investigation on the long term reliability of power IGBT modules," in *Proc. Int. Symp. Power Semiconductor Devices ICs: (ISPSD)*, May 1995, pp. 443–448.

[68] M. Bouarroudj, Z. Khatir, J.-P. Ousten, and S. Lefebvre, "Temperature-level effect on solder lifetime during thermal cycling of power modules," *IEEE Trans. Device Mater. Rel.*, vol. 8, no. 3, pp. 471–477, Sep. 2008.

[69] Y. Huang, Y. Luo, F. Xiao, and B. Liu, "Failure mechanism of die-attach solder joints in IGBT modules under pulse high-current power cycling," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 1, pp. 99–107, Mar. 2019.

[70] M. Du, Q. Guo, Z. Ouyang, K. Wei, and W. G. Hurley, "Effect of solder layer crack on the thermal reliability of insulated gate bipolar transistors," *Case Stud. Thermal Eng.*, vol. 14, Sep. 2019, Art. no. 100492.

[71] B. Wong, D. Helling, and R. Clark, "A creep-rupture model for two-phase eutectic solders," *IEEE Trans. Compon., Hybrids, Manuf. Technol.*, vol. 11, no. 3, pp. 284–290, Sep. 1988.

[72] M. Ciappa and P. Malberti, "Plastic-strain of aluminium interconnections during pulsed operation of IGBT multichip modules," *Qual. Rel. Eng. Int.*, vol. 12, no. 4, pp. 297–303, 1996.

[73] E. Philofsky, K. Ravi, E. Hall, and J. Black, "Surface reconstruction of aluminum metallization–a new potential wearout mechanism," in *Proc. 9th Rel. Phys. Symp.*, Mar. 1971, pp. 120–128.

[74] D. DeVoto, "Reliability of electrical interconnects," Nat. Renew. Energy Lab., Golden, CO, USA, Tech. Rep. NREL/PR, 5400-61358, Jun. 2014.

[75] M. Sathik, T. K. Jet, C. J. Gajanayake, R. Simanjorang, and A. K. Gupta, "Comparison of power cycling and thermal cycling effects on the thermal impedance degradation in IGBT modules," in *Proc. 41st Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Nov. 2015, pp. 1170–1175.

[76] M. Schäfer, O. Schilling, and C. Yue, "Comparison between active and passive thermal cycling stress with respect to substrate solder reliability in IGBT modules with Cu baseplates," in *Proc. PCIM Eur.*, 2014, pp. 674–681.

[77] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proc. 2nd Int. Conf. Power Electron. Drive Syst.*, May 1997, pp. 425–430.

[78] R. Amro, "Power cycling capability of advanced packaging and interconnection technologies at high temperature swings," Ph.D. dissertation, Dept. Elect. Eng. Inf. Technol., Chemnitz Univ. Technol., Chemnitz, Germany, 2006.

[79] Q. Yuan, R. Endoh, T. Ima, Y. Kajita, and Y. Luo, "Failure mode verification of power IGBT under different thermal stress application conditions in power cycling test environment," in *Proc. Int. Conf. Electron. Packag. iMAPS All Asia Conf. (ICEP-IAAC)*, Apr. 2018, pp. 367–370.

[80] M. Ahsan, S. T. Hon, C. Batunlu, and A. Albarbar, "Reliability assessment of IGBT through modelling and experimental testing," *IEEE Access*, vol. 8, pp. 39561–39573, 2020.

[81] S. Peyghami, Z. Wang, and F. Blaabjerg, "A guideline for reliability prediction in power electronic converters," *IEEE Trans. Power Electron.*, vol. 35, no. 10, pp. 10958–10968, Oct. 2020.

[82] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, "Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics," *IEEE Trans. Rel.*, vol. 58, no. 2, pp. 271–276, Jun. 2009.

[83] B. Wang and C. U. School of Electrical Engineering, "Review of power semiconductor device reliability for power converters," *CPSS Trans. Power Electron. Appl.*, vol. 2, no. 2, pp. 101–117, Jun. 2017.

[84] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-failure, condition monitoring, and prognostics of insulated gate bipolar transistor modules: A review," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2413–2426, May 2015.

[85] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition monitoring for device reliability in power electronic converters: A review," *IEEE Trans. Power Electron.*, vol. 25, no. 11, pp. 2734–2752, Nov. 2010.

[86] C. van der Broeck, H. Zeng, R. D. Lorenz, R. W. de Doncker, "A test bench for thermal characterization of IGBT power modules over mission profiles," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, Jun. 2018, pp. 1–8.
[87] W. Lai, M. Chen, L. Ran, S. Xu, N. Jiang, X. Wang, O. Alatise, and P. Mawby, "Experimental investigation on the effects of narrow junction temperature cycles on die-attach solder layer in an IGBT module," *IEEE Trans. Power Electron.*, vol. 32, no. 2, pp. 1431–1441, Feb. 2017.
[88] G. Zeng, R. Alvarez, C. Kunzel, and J. Lutz, "Power cycling results of high power IGBT modules close to 50 hz heating process," in *Proc. 21st Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Genova, Italy, Sep. 2019, pp. 1–10.
[89] G. Breglio, A. Irace, E. Napoli, M. Riccio, and P. Spirito, "Experimental detection and numerical validation of different failure mechanisms in IGBTs during unclamped inductive switching," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 563–570, Feb. 2013.
[90] L. Reddy GopiReddy, L. M. Tolbert, and B. Ozpineci, "Power cycle testing of power switches: A literature survey," *IEEE Trans. Power Electron.*, vol. 30, no. 5, pp. 2465–2473, May 2015.
[91] F. Forest, A. Rashed, J.-J. Huselstein, T. Martiré, and P. Enrici, "Fast power cycling protocols implemented in an automated test bench dedicated to IGBT module ageing," *Microelectron. Rel.*, vol. 55, no. 1, pp. 81–92, Jan. 2015.
[92] H. Medjahed, P.-E. Vidal, and B. Nogarede, "Thermo-mechanical stress of bonded wires used in high power modules with alternating and direct current modes," *Microelectron. Rel.*, vol. 52, no. 6, pp. 1099–1104, Jun. 2012.
[93] N. Baker, L. Dupont, S. Munk-Nielsen, F. Iannuzzo, and M. Liserre, "IR camera validation of IGBT junction temperature measurement via peak gate current," *IEEE Trans. Power Electron.*, vol. 32, no. 4, pp. 3099–3111, Apr. 2017.
[94] M. Denk, "*In-situ* condition monitoring of IGBT power semiconductors using real-time junction temperature measurement," Ph.D. dissertation, Dept. Mechtron., Bayreuth Univ., Bayreuth, Germany, 2016.
[95] Y. Avenas, L. Dupont, and Z. Khatir, "Temperature measurement of power semiconductor devices by thermo-sensitive electrical parameters—A review," *IEEE Trans. Power Electron.*, vol. 27, no. 6, pp. 3081–3092, Jun. 2012.
[96] Z. Khatir, L. Dupont, and A. Ibrahim, "Investigations on junction temperature estimation based on junction voltage measurements," *Microelectron. Rel.*, vol. 50, nos. 9–11, pp. 1506–1510, Sep. 2010.
[97] D. L. Blackburn and F. F. Oettinger, "Transient thermal response measurements of power transistors," *IEEE Trans. Ind. Electron. Control Instrum.*, vol. IECI-22, no. 2, pp. 134–141, May 1975.
[98] U. Scheuermann and R. Schmidt, "Investigations on the V_{ce}(T) method to determine the junction temperature by using the chip itself as sensor," in *Proc. PCIM Eur.*, 2009, pp. 802–807.
[99] U. Schilling, M. Spang, and M. Kind, "Electromagnetic disturbance of thermal measurements with the V_{ce}(T)-method in power modules," in *Proc. 21st Eur. Conf. Power Electron. Appl. (EPE ECCE Europe)*, Genova, Italy, Sep. 2019, p. 1.
[100] M. H. M. Sathik, S. Prasanth, F. Sasongko, S. K. Padmanabhan, J. Pou, and R. Simanjorang, "Online junction temperature for off-the-shelf power converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, San Antonio, TX, USA, Mar. 2018, pp. 2769–2774.
[101] Z. Sarkany, A. Vass-Varnai, and M. Rencz, "Investigation of die-attach degradation using power cycling tests," in *Proc. IEEE 15th Electron. Packag. Technol. Conf. (EPTC)*, Singapore, Dec. 2013, pp. 780–784.
[102] Z. Sarkany, A. Vass-Varnai, S. Laky, and M. Rencz, "Thermal transient analysis of semiconductor device degradation in power cycling reliability tests with variable control strategies," in *Proc. Semiconductor Thermal Meas. Manage. Symp. (SEMI-THERM)*, San Jose, CA, USA, Mar. 2014, pp. 236–241.
[103] E. Dimech and J. Frederick Dawson, "Electrical parameters characterization of aged IGBTs by thermo-electrical overstress," in *Proc. 44th Annu. Conf. IEEE Ind. Electron. Soc. (IECON)*, Washington, DC, USA, Oct. 2018, pp. 5924–5929.
[104] U.-M. Choi, S. Jørgensen, and F. Blaabjerg, "Advanced accelerated power cycling test for reliability investigation of power device modules," *IEEE Trans. Power Electron.*, vol. 31, no. 12, pp. 8371–8386, Dec. 2016.
[105] X. Du, J. Zhang, S. Zheng, and H.-M. Tai, "Thermal network parameter estimation using cooling curve of IGBT module," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7957–7971, Aug. 2019.
[106] A. M. Aliyu and A. Castellazzi, "Prognostic system for power modules in converter systems using structure function," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 595–605, Jan. 2018.
[107] Y. Zhu, K. Ma, and X. Cai, "Thermal characterization method of power semiconductors based on H-Bridge testing circuit," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8268–8273, Sep. 2019.
[108] K. Wei, W. Wang, Z. Hu, and M. Du, "Condition monitoring of IGBT modules based on changes of thermal characteristics," *IEEE Access*, vol. 7, pp. 47525–47534, 2019.
[109] A. Poppe and G. Farkas, "Transient measurements to extract resistances and material properties with hands-on demonstrations," in *Proc. Presentation Mentor Graph. Mech. Anal. Division MicReD Unit, Budapest, Hungary in SEMI-THERM Symp.*, San Jose, CA, USA, 2016.
[110] S. Schuler and U. Scheuermann, "Impact of test control strategy on power cycling lifetime," in *Proc. PCIM Eur.*, 2010, pp. 355–360.
[111] S. Tran, Z. Khatir, and R. Lallemand, "Constant ΔT_j power cycling strategy in DC mode for top-metal and bond-wire contacts degradation investigations," *IEEE Trans. Power Electron.*, vol. 34, no. 3, pp. 2171–2180, Mar. 2019.
[112] H. Wang, K. Ma, and F. Blaabjerg, "Design for reliability of power electronic systems," in *Proc. 38th Annu. Conf. IEEE Ind. Electron. Soc.*, Oct. 2012, pp. 33–44.
[113] L. A. Escobar and W. Q. Meeker, "A review of accelerated test models," *Stat. Sci.*, vol. 21, no. 4, pp. 552–577, Nov. 2006.
[114] U. Scheuermann and U. Hecht, "Power cycling lifetime of advanced power modules for different temperature swings," in *Proc. PCIM Eur.*, 2002, pp. 59–64.
[115] R. Bayerer, T. Herrmann, T. Licht, J. Lutz, and M. Feller, "Model for power cycling lifetime of IGBT modules-various factors influencing lifetime," in *Proc. 5th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2008, pp. 1–6.
[116] J. Lutz, "IGBT-modules: Design for reliability," in *Proc. 13th Eur. Conf. Power Electron. Appl.*, Sep. 2009, pp. 1–3.
[117] *SKiM—100% Solder-Free Ensures Durability | SEMIKRON*. Accessed: Jun. 25, 2012. [Online]. Available: https://www.semikron.com/products/product-lines/skim.html
[118] U. Scheuermann and R. Schmidt, "Impact of load pulse duration on power cycling lifetime of al wire bonds," *Microelectron. Rel.*, vol. 53, nos. 9–11, pp. 1687–1691, Sep. 2013.
[119] U. Scheuermann and P. Beckedahl, "The road to the next generation power module–100% solder free design," in *Proc. 5th Int. Conf. Integr. Power Electron. Syst.*, Mar. 2008, pp. 111–120.
[120] U. Scheuermann and R. Schmidt, "A new lifetime model for advanced power modules with sintered chips and optimized al wire bonds," in *Proc. PCIM Eur.*, 2013, pp. 810–817.
[121] R. Schmidt and U. Scheuermann, "Separating failure modes in power cycling tests," in *Proc. 7th Int. Conf. Integr. Power Electron. Syst. (CIPS)*, Mar. 2012, pp. 1–6.
[122] U. Scheuermann and M. Junghaenel, "Limitation of power module lifetime derived from active power cycling tests," in *Proc. 10th Int. Conf. Integr. Power Electron. Syst. (CIPS)*, Mar. 2018, pp. 1–10.
[123] M. Dbeiss, Y. Avenas, H. Zara, L. Dupont, and F. A. Shakarchi, "A method for accelerated aging tests of power modules for photovoltaic inverters considering the inverter mission profiles," *IEEE Trans. Power Electron.*, vol. 34, no. 12, pp. 12226–12234, Dec. 2019.
[124] I. Vernica, H. Wang, and F. Blaabjerg, "Design for reliability and robustness tool platform for power electronic systems—Study case on motor drive applications," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, San Antonio, TX, USA, Mar. 2018, pp. 1799–1806.
[125] K. Mainka, M. Thoben, and O. Schilling, "Lifetime calculation for power modules, application and theory of models and counting methods," in *Proc. 14th Eur. Conf. Power Electron. Appl.*, Birmingham, U.K., Aug./Sep. 2011, pp. 1–8.
[126] A. Antonopoulos, S. DrArco, M. Hernes, and D. Peftitsis, "Challenges and strategies for a real-time implementation of a rainflow-counting algorithm for fatigue assessment of power modules," in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Anaheim, CA, USA, Mar. 2019, pp. 2708–2713.
[127] G. Zeng, C. Herold, T. Methfessel, M. Schafer, O. Schilling, and J. Lutz, "Experimental investigation of linear cumulative damage theory with power cycling test," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4722–4728, May 2019.
[128] C. Li, Z. Tan, Q. Huang, W. Nie, and J. Yao, "Lifetime evaluation of IGBT module in DFIG considering wind turbulence and nonlinear damage accumulation effect," in *Proc. IEEE 2nd Int. Conf. Autom., Electron. Electr. Eng. (AUTEEE)*, Shenyang, China, Nov. 2019, pp. 472–476.

[129] G. R. Halford, "Cumulative fatigue damage modeling—Crack nucleation and early growth," *Int. J. Fatigue*, vol. 19, pp. 253–260, Jun. 1997.
[130] A. Fatemi and L. Yang, "Cumulative fatigue damage and life prediction theories: A survey of the state of the art for homogeneous materials," *Int. J. Fatigue*, vol. 20, no. 1, pp. 9–34, Jan. 1998.
[131] D. G. Pavlou, "Loading sequence effects on fatigue damage accumulation of offshore structures: A deterministic approach," in *Proc. Mater. Technol.*, Trondheim, Norway, vol. 57687, Jun. 2017, p. V004T03A010.
[132] O. E. Wheeler, "Spectrum loading and crack growth," *J. Basic Eng.*, vol. 94, no. 1, pp. 181–186, Mar. 1972.
[133] D. G. Pavlou, "Prediction of fatigue crack growth under real stress histories," *Eng. Struct.*, vol. 22, no. 12, pp. 1707–1713, Dec. 2000.
[134] M. Skorupa, "Load interaction effects during fatigue crack growth under variable amplitude loading—A literature review. Part II: Qualitative interpretation," *Fatigue Fract. Eng. Mater. Struct.*, vol. 22, no. 10, pp. 905–926, 1998.
[135] S. U. Khan, R. C. Alderliesten, and C. D. Rans, "Application of a modified Wheeler model to predict fatigue crack growth in fibre metal laminates under variable amplitude loading," *Eng. Fract. Mech.*, vol. 77, no. 9, pp. 1400–1416, 2010.
[136] A. Morozumi, K. Yamada, T. Miyasaka, S. Sumi, and Y. Seki, "Reliability of power cycling for igbt power semiconductor modules," *IEEE Trans. Ind. Appl.*, vol. 39, no. 3, pp. 665–671, May 2003.
[137] R. Schmidt, F. Zeyss, and U. Scheuermann, "Impact of absolute junction temperature on power cycling lifetime," in *Proc. 15th Eur. Conf. Power Electron. Appl. (EPE)*, Sep. 2013, pp. 1–10.
[138] M. Junghaenel, R. Schmidt, J. Strobel, and U. Scheuermann, "Investigation on isolated failure mechanisms in active power cycle testing," in *Proc. Int. Exhib. Conf. Power Electron., Intell. Motion, Renew. Energy Energy Manage.*, May 2015, pp. 1–8.
[139] M. Junghaenel and U. Scheuermann, "Impact of load pulse duration on power cycling lifetime of chip interconnection solder joints," *Microelectron. Rel.*, vols. 76–77, pp. 480–484, Sep. 2017.
[140] M. Thobe, *Reliability and Lifetime of Power Modules Tutorial: Industry Best Practices in Reliability Prediction and Assurance for Power Electronics*. Neubiberg, Germany: Infineon Technologies, Sep. 2016.
[141] P. Steinhorst, T. Poller, and J. Lutz, "Approach of a physically based lifetime model for solder layers in power modules," *Microelectron. Rel.*, vol. 53, pp. 1199–1202, Sep./Nov. 2013.

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