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Published in:
IEEE Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2020.3023100

Publication date:
2022

Document Version
Accepted author manuscript, peer reviewed version

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3023100, IEEE Journal of Emerging and Selected Topics in Power Electronics

Real-Time FPGA-based HIL Emulator of Power Electronics Controllers using NI PXI for DFIG Studies

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***Abstract*—This paper presents a high-performance hardware-in-the-loop (HIL) system aimed to assist experts in developing and testing power electronics control board and their logic with Real-Time (RT) models of both electrical and mechanical components. For demonstrating the effectiveness of this system for HIL testing, a new industrial doubly-fed induction generator (DFIG) control board is tested based on a comprehensive wind energy conversion model developed in MATLAB/Simulink hardware description language (HDL) coder and LabVIEW environment. The interaction between MATLAB/Simulink and LabVIEW is accomplished by National Instrument (NI) intellectual property (IP) integration node, which loads very high-speed integrated circuit hardware description language (VHSIC-HDL or VHDL) codes (that enable those two software exchange real-time data). LabVIEW implements a VHDL code of electrical model with fixed-point variables on an R-Series reconfigurable input/output (I/O) field-programmable gate array (FPGA) module on NI-PXIe 7858R installed on NI PXIe 1062Q chassis and the mechanical models deployed in its PXIe 8133 central processing unit (CPU). Finally, through a uniquely developed interface-board, the HIL emulator connects to an external DFIG control board. In FPGA, the model and other communicational and logging components' step-time in each iteration is 5.0 µs. For verifying the results, a comparison is made between the proposed emulator system and Typhoon HIL602+ as a commercially-available HIL system. It is proved that there is little or no significant deviation between the two systems outputs. The proposed HIL emulator does not have the limitation of commercial HIL systems in adding custom-made new components.**

***Index Terms*—Doubly-fed induction generator, field-programmable gate array, hardware description language, hardware-in-the-loop, LabVIEW FPGA, MATLAB/Simulink, power electronics, Real-Time emulator.**

I. Introduction

TODAY, there are many commercial and industrial-grade HIL systems available for simulating power electronics modules, power converters, electric machines, power plants, and microgrids [1, 2]. These systems are customized to test their complicated control boards with an expanded finite-state machine (FSM) computations [3]. RTDS [4-7], Opal-RT [8, 9], and Typhoon [10] are some different types of acknowledged commercial real-time HIL testing equipment that are used widely in power systems and power electronics HIL emulation and rapid control prototyping (RCP). Also, some custom-designed HIL systems like [11, 12] are available that have used FPGA or personal computer (PC)-cluster-based solution as a Real-Time simulator. NI PXI systems are also presenting a real-time digital solution based on ordinary off the shelf standard PCs. They can be applied in controller-hardware-in-the-loop (CHIL) purposes and Real-Time power system simulation.

Commercial HIL systems are used in various studies. In [13], HIL testing has been used to validate a new fuzzy control method for DFIG in which better power oscillations damping and voltage recovery characteristics can be achieved despite unpredictability in the network parameters. In [14], a grid-side synchronous damping controller (GSDC) is proposed to stabilize the unstable sub-synchronous control interaction (SSCI) in a series compensated wind power system. This controller has demonstrated its effectiveness and robustness in RTDS-based hardware-in-the-loop tests. In [15] the HIL testing has been used to confirm the feasibility of a proposed multi-loop adaptive controller for DFIG-Wind Turbine (WT). Some proposals sub-synchronous oscillations observed in DFIG-based wind

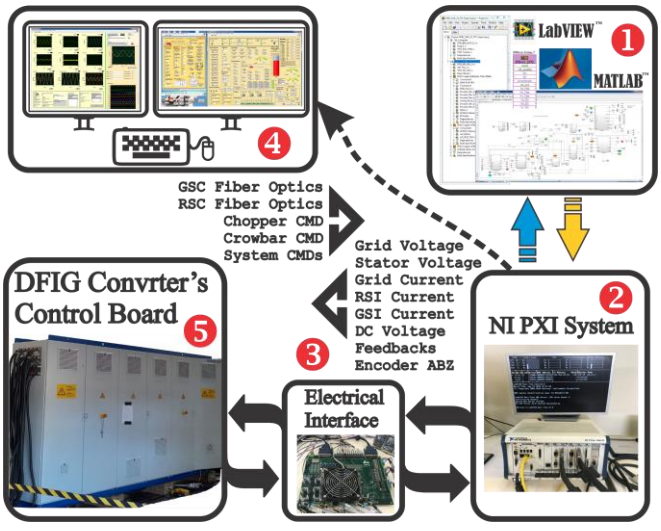

Fig. 1. Scheme of HIL and RTS's configuration

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This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/JESTPE.2020.3023100, IEEE Journal of Emerging and Selected Topics in Power Electronics

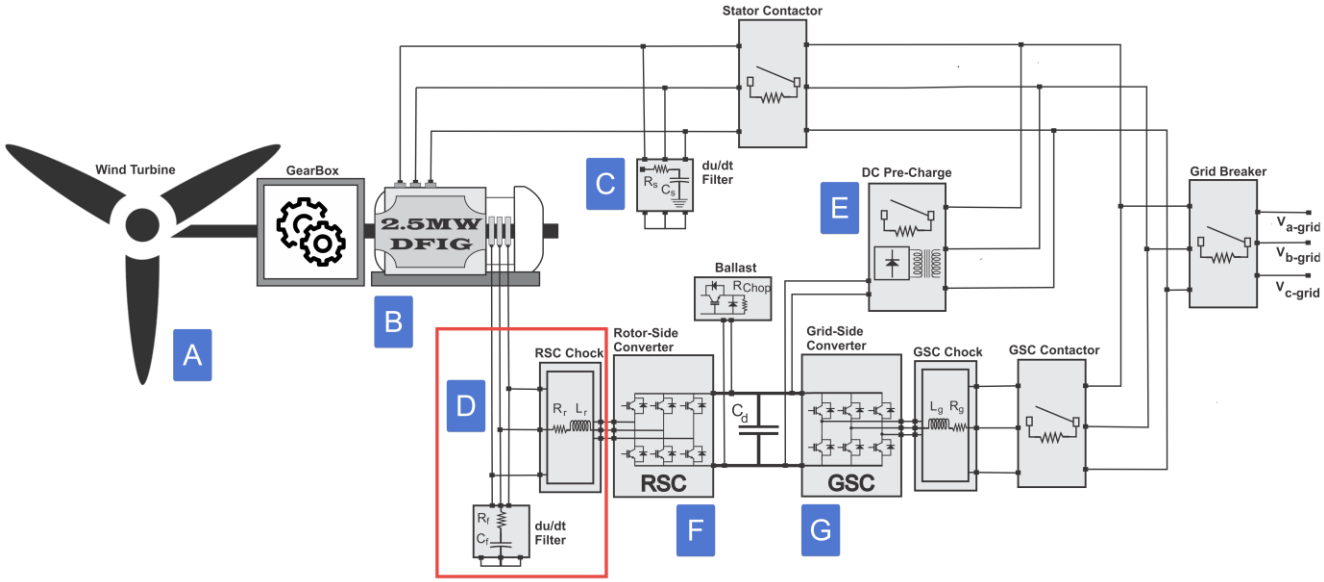

Fig. 2. Overall model of DFIG base wind power generation system.

farms, interfaced with a high-voltage including sensor-less control of DFIG and investigations such as direct current voltage-source converter (VSC-HVDC) are verified using the HIL testing system [16, 17]. A new sensor-less control method for a permanent magnet assisted synchronous reluctance motor has been proposed in [18], where authors used the Typhoon HIL system to examine the credibility of their theoretical proposal. In [19], the Typhoon HIL system has been used to investigate the stability of a typical inverter-based islanded micro-grid within a novel framework. Another example of Typhoon HIL application has been presented in [10], where the authors used the HIL system to validate their designed control loops. Authors in [20] used hardware in the loop system to analyze the mutual effects of the DFIG and power grid on the system's low-frequency oscillation. In [21], a novel control method for distributed energy resources under parallel operation with a three-phase network with unbalanced voltages is presented and verified by simulations and the HIL system. Another example of the HIL application is in [22], where two power flow control algorithms for VSC are presented and validated.

Custom made CHIL systems usually have different hardware and software architectures. In [23], a PC-cluster Real-Time simulator acquired an RT Linux operating system (OS). Still, because of CPU calculation restraints, instead of simulating switches, controlled voltage and current sources are playing the role of the insulated-gate bipolar transistors (IGBT). While 50us step-time is satisfying for RT modeling in the power system, it is relatively a long period to model switches. In this situation, representation of the rectifying effect during the pulse-block of all the converter switches is not possible. In [24] again, a PC is working as a Real-Time target and is sharing CPU resources with Ardence RTX as a Real-Time subsystem. Although this architecture is surprisingly inexpensive, as CPU cores should be divided between windows and RTX, step-time is not more than 1ms, and such structure is not recommended for power electronics CHIL studies. In [25-27], a real-time simulator and a closed-loop HIL testbed for the power system is introduced. This emulator employs engineering software MATLAB/Simulink, LabVIEW, and also presented NI PXI hardware to interact with the real environment. Depending on model size and complexity, the minimum step-time is around 150 to 300 microsecond, which again is not sufficient for switch modeling but suitable for power system dynamic modeling, including power generation, turbine, transmission line, and distribution systems modeling.

In this paper, we introduced a CHIL system with 5us step-time and 40.463ns critical path delay of the proposed DFIG model, switches, and other electrical components. Fig. 1 shows the proposed CHIL schematic for the DFIG converter control board. NI PXI embedded controller with R-series reconfigurable FPGA based I/O cards can quickly provide a high-speed real-time HIL system [28]. NI FPGA module with necessary Xilinx compilation tools is being utilized with the IP Integration Node that is capable of integrating third-party IP into LabVIEW. One of the tools that can create third-party IP is the HDL Operations library of MATLAB/Simulink. The HDL coder of Simulink generates portable, synthesizable VHDL code from established models [29]. The generated HDL code can be used for FPGA Real-Time programming in NI R-Series reconfigurable I/O cards with a 40MHz onboard clock. The advantage of this method lies in total custom design mathematical modeling, graphical programming, or even VHDL code generating (that narrows the limitation of commercial HIL systems in making new components) [30]. The developers' decision to choose appropriate discreet solvers regarding acceptable order of accuracy or adding power electronics components without minding their tight calculation restrictions and core sharing are other advantages of this method.

The remainder of this paper is organized as follows: Section II presents the mechanical and electrical models of the wind energy conversion system (WECS). RT system development and HDL code generation are discussed in Section III. Section IV elaborates on the design and implementation of the required interface systems between the control board and NI RT equipment. Section V describes the DFIG converter control structure. In Section VI, the experimental test results of the proposed Real-Time FPGA-based HIL system is presented. In section VII, a comparison between Implemented NI HIL system and a Typhoon HIL602+ is provided. Finally, conclusions are stated in Section VIII.

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II. Modeling of Wind Energy Conversion System

Mathematical models with emphasis on the main mechanical and electrical components of a 2.5 MW DFIG wind energy generation was employed to develop a Real-Time CHIL system with MATLAB/Simulink HDL Coder, LabVIEW Control design and simulation module. DFIG is a standard wound rotor induction machine that its stator is directly connected to the grid. For the rotor, a back to back converter is required to establish an electrical connection to the network. The block diagram of a DFIG-based WECS is illustrated in Fig. 2.

A. Wind Turbine

On the DFIG shaft model, according to actuator disk theory, the mechanical torque extracted from the wind is provided by [31]

$$T_m = P_m * \frac{1}{\omega_r} \quad (1)$$

where ω_r (rad/s) is the DFIG rotor, angular speed, and P_m (W) is the mechanical power which is given by

$$P_m = 0.5\, C_p \rho \pi R^2 v_{wind}^3 \quad (2)$$

where v_{Wind} (m/s) is the wind speed, R (m) is the rotor disk radius, ρ (Kg/m^3) is the air density, C_p (λ, β) is the power coefficient for pitch regulated WTs, which is a function of tip speed ratio λ and the blade pitch angle β. In literature, several models are provided for this coefficient [32], but the following equation is the most well adapted for variable speed WTs.

$$C_p(\lambda,\beta) = \left(\frac{C_2}{\lambda_i} - C_3\beta - C_4\right) e^{-\frac{C_5}{\lambda_i}} C_6\lambda \quad (3)$$

$$\lambda = \frac{\omega * R}{v_{wind}} = \frac{\omega_r}{G * v_{wind}} \quad (4)$$

where ω is the turbine's angular speed (rad/s), G is the gearbox ratio, and C_i is Beltz coefficients [33]. λ_i is also calculated by pitch angle and tip speed ratio, as is given by

$$\lambda_i = \frac{1}{\lambda + 0.08\beta} - \frac{0.035}{\beta^3 + 1} \quad (5)$$

B. Loaded DFIG

Based on the dynamic equivalent circuit of the induction machine shown in Fig. 3, the main DFIG dynamic state-space equations are given by:

$$\frac{d\Psi_{qs}}{dt} = \omega_b[v_{qs} - \frac{\omega_e}{\omega_b}\Psi_{ds} + \frac{R_s}{X_{ls}}(\Psi_{mq} + \Psi_{qs})] \quad (6)$$

$$\frac{d\Psi_{ds}}{dt} = \omega_b[v_{ds} - \frac{\omega_e}{\omega_b}\Psi_{qs} + \frac{R_s}{X_{ls}}(\Psi_{md} + \Psi_{ds})] \quad (7)$$

$$\frac{d\Psi_{qr}}{dt} = \omega_b[v_{qr} - \frac{(\omega_e - \omega_r)}{\omega_b}\Psi_{dr} + \frac{R_r}{X_{lr}}(\Psi_{mq} + \Psi_{qr})] \quad (8)$$

$$\frac{d\Psi_{dr}}{dt} = \omega_b[v_{dr} + \frac{(\omega_e - \omega_r)}{\omega_b}\Psi_{qr} + \frac{R_r}{X_{lr}}(\Psi_{md} + \Psi_{dr})] \quad (9)$$

$$\Psi_{mq} = X_{ml}\left(\frac{\Psi_{qs}}{X_{ls}} + \frac{\Psi_{qr}}{X_{lr}}\right) \quad (10)$$

$$\Psi_{md} = X_{ml}\left(\frac{\Psi_{ds}}{X_{ls}} + \frac{\Psi_{dr}}{X_{lr}}\right) \quad (11)$$

where the stator and rotor current is given by:

$$i_{qs} = {}^1\!/_{X_{ls}}(\Psi_{qs} - \Psi_{mq}) \quad (12)$$

$$i_{ds} = {}^1\!/_{X_{ls}}(\Psi_{ds} - \Psi_{md}) \quad (13)$$

$$i_{qr} = {}^1\!/_{X_{lr}}(\Psi_{qr} - \Psi_{mq}) \quad (14)$$

$$i_{dr} = {}^1\!/_{X_{lr}}(\Psi_{dr} - \Psi_{md}) \quad (15)$$

and the electromagnetic torque in per-unit, active and reactive power of stator and rotor can be calculated as:

$$T_e = (\Psi_{ds}.* i_{qs} - \Psi_{qs}.* i_{ds}) \quad (16)$$

$$P_s = (v_{ds}.* i_{ds} + v_{qs}.* i_{qs}) \quad (17)$$

$$Q_s = (v_{qs}.* i_{ds} - v_{ds}.* i_{qs}) \quad (18)$$

$$P_r = (v_{dr}.* i_{dr} + v_{qr}.* i_{qr}) \quad (19)$$

$$Q_r = (v_{qr}.* i_{dr} - v_{dr}.* i_{qr}) \quad (20)$$

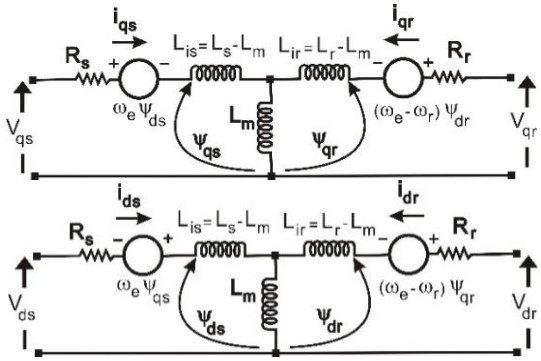

Fig. 3. The equivalent circuit of an induction machine in dq coordinates.

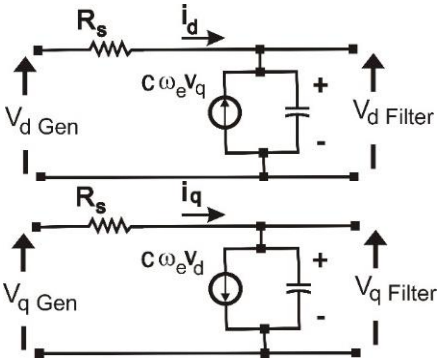

Fig. 4. RC Filter circuit.

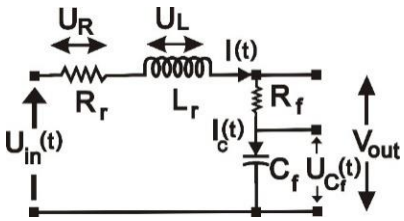

Fig. 5. RLC filter circuit.

C. Unloaded Doubly-Fed Induction Generator model

The most notable point in the unloaded DFIG model is the absence of stator current, which will simplify the model and imply some changes in the equations (6) to (15). The dynamic of the stator winding is described by [34],

$$\frac{d\Psi_{qs}}{dt} = \omega_b[E_{qs} - \frac{\omega_e}{\omega_b}\Psi_{ds}] \quad (21)$$

$$\frac{d\Psi_{ds}}{dt} = \omega_b[E_{ds} - \frac{\omega_e}{\omega_b}\Psi_{qs}] \quad (22)$$

$$\Psi_{ds} = L_m i_{dr} \quad (23)$$

$$\Psi_{qs} = L_m i_{qr} \quad (24)$$

and for rotor windings we have,

$$\frac{d\Psi_{qr}}{dt} = \omega_b[v_{qr} - \frac{(\omega_e - \omega_r)}{\omega_b}\Psi_{dr} - R_r i_{qr}] \quad (25)$$

$$\frac{d\Psi_{dr}}{dt} = \omega_b[v_{dr} + \frac{(\omega_e - \omega_r)}{\omega_b}\Psi_{qr} - R_r i_{dr}] \quad (26)$$

$$\Psi_{dr} = L_r i_{dr} \quad (27)$$

$$\Psi_{qr} = L_r i_{qr} \quad (28)$$

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The stator voltages in the synchronous reference frame (SYRF) (*dq* coordinate) [35] (E_{dq}, E_{qs}) are the variables that need to be calculated. During the synchronization process, these values will be compared with the grid voltage.

D. RC Filter Model (dq)

As shown in Fig. 2(C) an RC filter is used to smooth the stator voltage ripples during synchronization and provide some reactive power after grid connection. Fig. 4 shows the circuit schematic of the filter based on the following equations in SYRF.

$$i_q = c\frac{dv_q}{dt} + c\omega_e v_d \quad (29)$$

$$i_d = c\frac{dv_d}{dt} - c\omega_e v_q \quad (30)$$

As we are interested in the capacitor's voltage, we can re-write (28) and (29) as:

$$dv_{q\,filter}/_{dt} = \frac{1}{RC}[v_{qGen} - RC\omega_e v_d - v_q] \quad (31)$$

$$dv_{d\,filter}/_{dt} = \frac{1}{RC}[v_{dGen} - RC\omega_e v_q - v_d] \quad (32)$$

Then, by solving these equations, the filtered voltage of DFIG in un-loaded mode can be calculated.

E. RLC Filter Model

To protect the rotor's insulation, high *dv/dt* induced on rotor windings due to pulse width modulation (PWM) (step from zero to Direct Current (DC) link voltage, with 3.5 kHz switching frequency), should be reduced. As shown in Fig. 2 (D), an RLC filter is connected to the rotor side converter to smooth the voltage waveform. The filter's schematic is shown in Fig. 5 and its equations are as follows,

$$U_{in}(t) = L_r C_f \frac{d^2U_{cf}(t)}{dt^2} + (R_r + R_f)C_f\frac{dU_{cf}(t)}{dt} + U_{cf}(t) \quad (33)$$

$$\frac{d^2U_{cf}(t)}{dt^2} = \frac{U_{in}(t) - (R_r+R_f)C_f\frac{dU_{cf}(t)}{dt} - U_{cf}(t)}{L_r C_f} \quad (34)$$

$$I(t) = I_c(t) = C_f\frac{dU_{cf}(t)}{dt} \quad (35)$$

$$V_{out} = R_f I_c(t) + U_{cf}(t) \quad (36)$$

F. Grid Side Converter (GSC)

The main circuit topology of the three-phase PWM voltage Source Converter (VSC) [36] is shown in Fig. 6. A three-phase ideal voltage source equipped with an RL filter is used as AC input, which is connected to an IGBT-base three-phase rectifier. Also, each IGBT is protected by a freewheeling diode as an inbuilt protective semiconductor which their presence mandates a pre-charging mechanism, implemented by a three-phase transformer and a half-wave diode base circuit [see Fig. 2(E)]. In this paper, the output load consists of a capacitor, one on-demand chopper resistor (if V_{dc} > 1250V), and a rotor side converter (RSC).

As the IGBT power switches are considered ideal, the model of PWM converter in a three-phase natural reference frame (*abc* coordinate) [35] is as shown in Fig. 7. The concept of switching function (SF) [37] is used as an appropriate tool in comprehending, and simulating the performance of the static power converters. By using the switching function concept, the power conversion circuit's functions are the basis for the modeling instead of the circuit topologies [38].

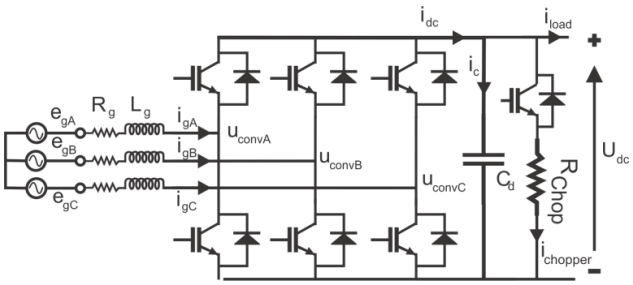

Fig. 6. VSC circuit topology

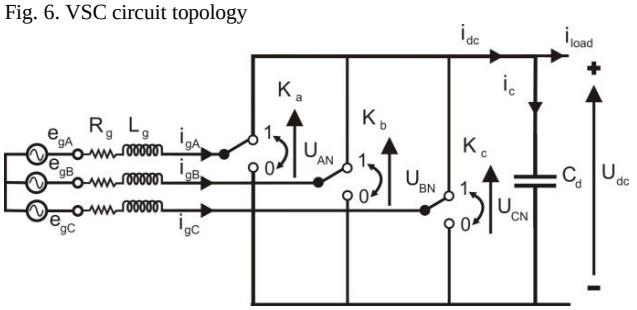

Fig. 7. Simulated model of PWM converter

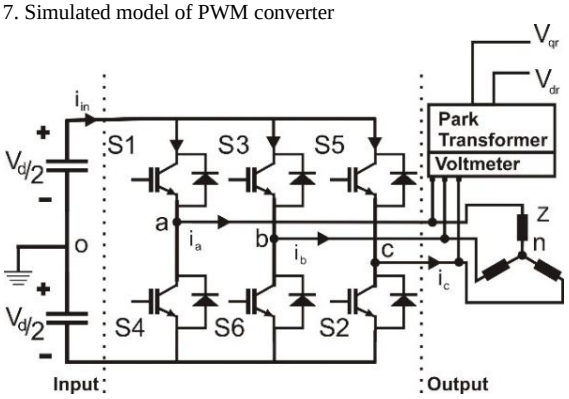

Fig. 8. Circuit configuration of studied VSC

Based on the equivalent circuit for VSC, the following equations are used to calculate the voltage of the DC link, where K_a, K_b, K_c are the switching functions.

$$\frac{di_{gA}}{dt} = \frac{1}{L_g}[e_{gA} - R_g i_{gA} - \frac{U_{dc}}{3}(2K_a - K_b - K_c)] \quad (37)$$

$$\frac{di_{gB}}{dt} = \frac{1}{L_g}[e_{gB} - R_g i_{gB} - \frac{U_{dc}}{3}(2K_a - K_b - K_c)] \quad (38)$$

$$\frac{di_{gC}}{dt} = \frac{1}{L_g}[e_{gC} - R_g i_{gC} - \frac{U_{dc}}{3}(2K_a - K_b - K_c)] \quad (39)$$

$$\frac{dU_{dc}}{dt} = \frac{1}{C_d}[(K_a i_{gA} + K_b i_{gB} + K_c i_{gC} - i_{load} - i_{Chopper}] \quad (40)$$

The implemented DFIG HIL emulator is connected to a control board, and the emulator receives the gate signals from its fiber optic inputs. The processor of the control board sends out each IGBT gate signal according to the switch order of the rectifier. For each arm, both switches should be monitored, and when the up-arm switch is closed, and the down-arm switch is open switch function K_x is equal to one, and it would be zero in the opposite state of switches (where *x*= *a*, *b*, *c*). i_{load} will be calculated in the next part (G) renamed into i_{in}.

G. Rotor Side Converter (RSC)

The detailed schematic of studied VSC is shown in Fig. 8. Using the transfer function (TF) of the system and the dependent

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and independent variables, the relationship between input and output variables are as follows [37],

$$[v_{ab}, v_{bc}, v_{ca}] = TF.V_d \quad (41)$$

$$I_{in} = TF.[I_a, I_b, I_c]^T \quad (42)$$

$$TF = [SF_1, SF_2, \dots] \quad (43)$$

The implemented control philosophy inside the control board's processor defines the switching functions (SF_x) of the HIL system by providing gate signals of the rotor side VSC. V_{ao}, V_{bo}, and V_{co} can be presented as:

$$V_{ao} = \frac{V_d}{2}.SF_{1-a}$$
$$V_{bo} = \frac{V_d}{2}.SF_{1-b} \quad (44)$$
$$V_{co} = \frac{V_d}{2}.SF_{1-c}$$

In this paper, SF_1 and SF_2 are obtained from the digital I/Os (DIO) of the control board. SF_1 expresses V_{ao}, V_{bo}, and V_{co} and is employed to calculate the converter line-to-line and phase voltages. SF_2 designates the voltage across the switch, and the load currents are used to calculate the switch current. The converter line to line voltages are given by

$$V_{ab} = V_{ao} - V_{bo}$$
$$V_{bc} = V_{bo} - V_{co} \quad (45)$$
$$V_{ca} = V_{co} - V_{ao}$$

To calculate the phase voltage of the converter, V_{no} can be derived as

$$V_{no} = \frac{1}{3}(V_{ao} + V_{bo} + V_{co}) \quad (46)$$

The phase voltages are as follows

$$V_{an} = V_{ao} - V_{no}$$
$$V_{bn} = V_{bo} - V_{no} \quad (47)$$
$$V_{cn} = V_{co} - V_{no}$$

Next, for calculating the load current (I_a, I_b, I_c), as the load consists of resistance and inductance of the DFIG's rotor, these currents will be calculated in the model of machine. The switch currents are the product of SF_2 and the load currents.

$$I_{s1} = I_a.SF_{2-a}$$
$$I_{s3} = I_b.SF_{2-b} \quad (48)$$
$$I_{s5} = I_c.SF_{2-c}$$

Finally, the converter input current (i_{in} or i_{load}) can be obtained from the switching currents as follows

$$i_{in} = I_{load} = I_{s1} + I_{s3} + I_{s5}$$
$$i_{in} = I_a.SF_{2-a} + I_b.SF_{2-b} + I_c.SF_{2-c} \quad (49)$$

III. Real-Time System and Modeling

To set up an NI Real-Time HIL system for DFIG studies, a PXIe 1062Q chassis with NI PXIe 8133 CPU and peripheral modules such as NI PXIe 7858R and NI PXI 7833R are employed in this study. NI PXI is a high performance and relatively low-cost platform which is customized for automotive, high-speed measurements, industrial test, and HIL purposes. The architecture of PXI systems is based on ordinary off the shelf standard PCs, and they employ conventional technologies like PXI, PCI, and PXI express. The Real-Time operation system, PharLap ETS, is the turning point in these systems in comparison to ordinary non-Real-Time Windows-based PCs and PXI systems.

LabVIEW is a general-purpose graphical programming language, and it is fully capable of interacting with NI PXI systems. LabVIEW real-time and FPGA modules will do real-time modeling in PXI systems. By either LabVIEW programming or incorporating third-party IP into LabVIEW FPGA, the engineers can use a wide range of algorithms (that are fine-tuned to Xilinx FPGAs to achieve high performance while taking advantage of code reuse).

As shown in Fig. 9 DFIG, filters, protections, back to back

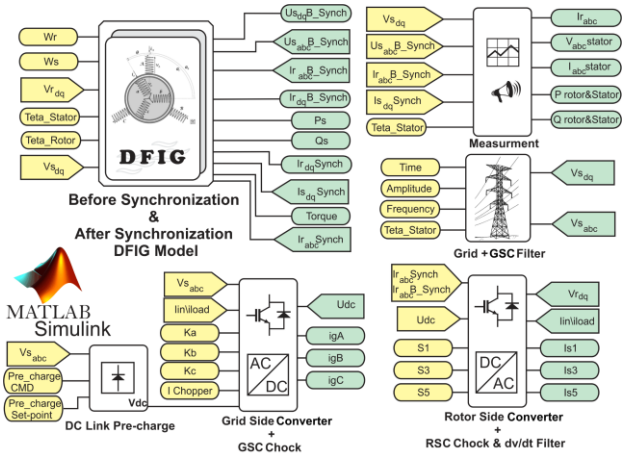

Fig. 9. Block diagram of presented model in MATLAB/Simulink.

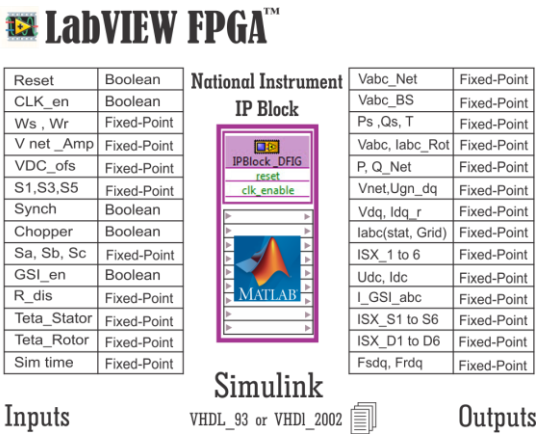

Fig. 10. NI FPGA IP Integration Node and its input - output values inside LabVIEW FPGA.

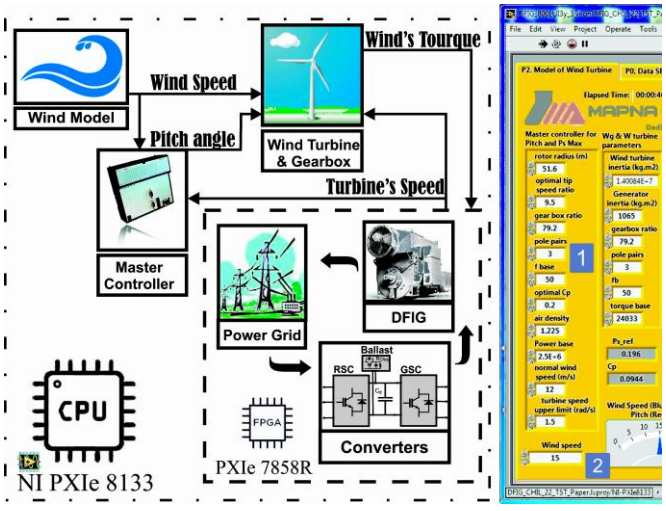

Fig. 11. Turbine, gearbox and wind model implementation in NI PXIe 8133, CPU module in first slot of NI PXIe-1062Q chassis.

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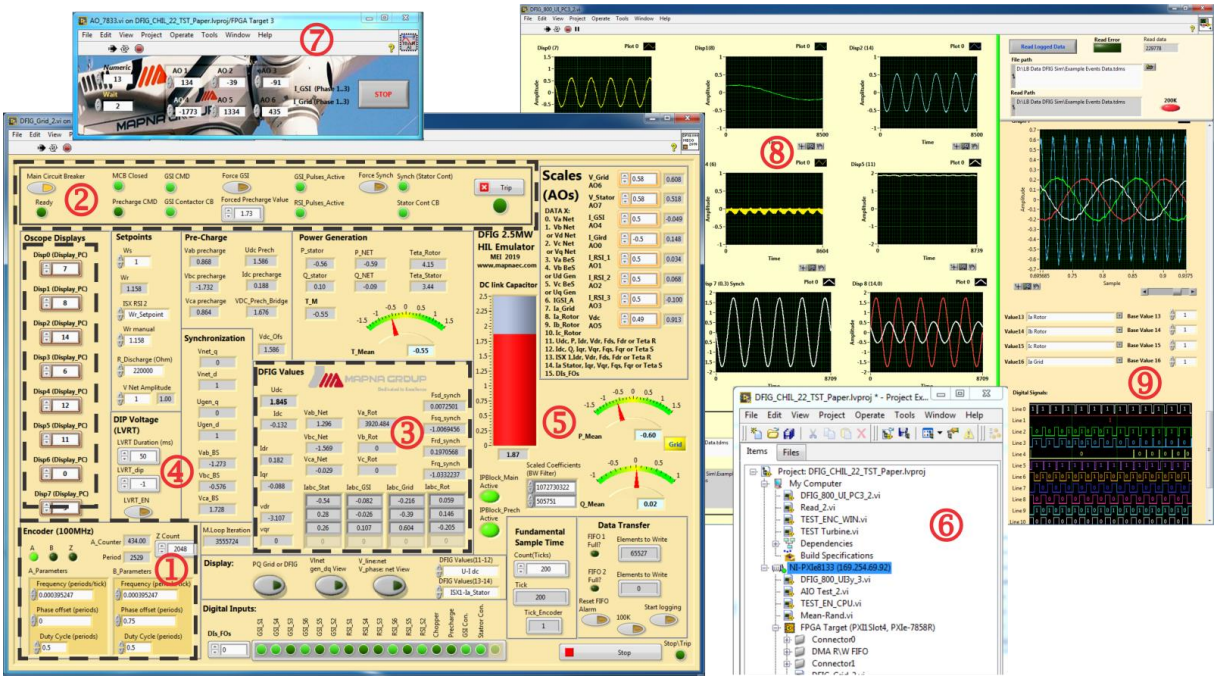

Fig. 12. Overall view of Real-Time DFIG Converter's code.

IGBT-base converter and DC precharge is modeled in the MATLAB/Simulink "HDL coder." Many commercial HIL systems work with MATLAB/Simulink models [26], however, in this study, we used MATLAB/Simulink to develop a model with fixed-point variables consisting of equations mentioned in Section II. MATLAB/Simulink "HDL coder" generates portable, synthesizable VHDL and Verilog codes from the model. Another benefit is providing a workflow adviser that automates the HDL generation of Xilinx and Altera FPGAs. HDL architecture, tuning of critical paths, and hardware resource estimations are also controllable, one of the notable items is critical path estimation. Due to the Simulink "code generation report," the most prolonged path delay in this study is 40.463 nanosecond. Another advantage of using MATLAB/Simulink is its fixed-step solvers that, alongside the model, will be translated into a VHDL code and by LabVIEW FPGA "IP Integration" function; the model will be synthesized for Kintex 7 FPGA of NI PXIe 7858R or other FPGAs. Fig. 10 represents the structure of VHDL code implementation in the LabVIEW FPGA environment and the input-output parameters.

Although the model itself can work in 5 MHz speed, as the emulator's code in FPGA consists of many subsystems including DFIG models in IP Integration Node, incremental encoder simulator, data transmission mechanism for logging chosen variables, display data sending to Host PC and digital-analog I/O interfaces, etc. the fundamental sample time of 5µs (200 kHz) has been chosen for numerical calculation time step in Simulink™ and main FPGA loop by adding such a delay in code. This timing is satisfactory as the control board's sample time is 142.8µs.

In wind energy system modeling, there are some other electrical controllers and mechanical components that do not require microsecond loop time calculations because of their natural response time. In some studies, when the loop time is considerably low, even the Real-Time OS can be substituted with a general-purpose OS [39]. In this study, such components include WT, gearbox, wind model, pitch the angle of the turbine's blades, and their inbuilt controllers. As shown in Fig. 11, such models are not required to be synthesized for FPGA, and they will be modeled by the "LabVIEW Control design and simulation module" and will be deployed into the CPU of the PXI system. The operator shall provide specific model parameter values and other required inputs for the implemented model, and output variables like WT speed or calculated pitch angle will be displayed on the dedicated front panel. [see Fig. 11 (1, 2)]

Besides the main components that form the DFIG and its converter model, there are some other parts that they should also be implemented in FPGA to complete the modeling. As mentioned before, these include online data transmission, Real-Time data logging, and incremental encoder simulator that is running in an independent 100MHz parallel loop alongside the main emulator's while loop. This incremental encoder simulator receives the rotor speed from the turbine model and provides ABZ square pulses for the DFIG control board. The DFIG control board will read these square waves in a high-speed module (50MHz clock), and therefore 100MHz loop in the emulator will maintain the highest possible accuracy. The turbine's angular speed (ω_r) is also accessible via a local variable for DFIG and converter model within the emulator's FPGA. Communication between FPGA, CPU, and Host PC is based on two "targets to host" DMA R\W FIFO function with 65535 and 262143 sixteen bit elements. The first "target to host" function consists of 8 selectable variables with SGL data type for transferring data into CPU and, eventually, online scope data display in Host PC. For sending data to PC first by DMA R\W FIFO, data from PXIe 7858R will be sent to the NI PXIe 8133 CPU through the PXIe buses. In a 1000µs loop, read data will be sorted then stored in different NI's RT FIFO & buffered "network shared variables." Variable numbers of arrays are 1000, and the numbers of elements are 500,000. Having PC connected to the PXI system through a 1 Gigabit Ethernet connection, shared network variables are

accessible, and in a 100ms loop will be read and displayed in the windows-based LabVIEW software [see Fig. 12(8)].

The second "target to host" function consists of 16 selectable variables with SGL data type. This function communicates directly from PXIe 7858R to the windows base target in Host PC. On the operator's demand and with selectable 5µ or 10µs resolution, data will be sent and stored in a Technical Data Management Streaming (TDMS) database and similar to Fig. 12(6 and 9) can be recalled and displayed in the windows software for further investigations.

Code compilation is the last step. Xilinx Vivado compilation tool will synthesize, utilize placement, and routing the logic. As it shows in Table I, the final report contains the number of total employed slices and slice registers, lookup tables (LUTs), amount of used RAMs and digital signal processing (DSP48E) used resources for the model's arithmetic and logic operations. Final timing (routing) will also get measured by the compilation tool, and all the requested frequencies in Megahertz should be met by the logic (including 5MHz loop frequency for the electrical model, 100MHz loop frequency for incremental encoder simulator and 160MHz loop frequency for non-diagram components within the FPGA code).

Final FPGA and PC code are shown in Fig. 12. 100MHz encoder parameters in Fig. 12(1) including features like frequency, offset, and duty cycle. On top of the page, operation sequences from the first step, i.e., main circuit breaker closure to the last one, generator synchronization, and grid connection state, are presented [see Fig. 12 (2)]. DFIG Electrical values are shown in Fig. 12(3) and voltage dip value can be tested according to Fig. 12(4). Active and reactive powers are also available and combined with electrical torque are connected to a Low Pass Filter with a cutoff frequency of 30Hz. The filter will smooth the values and make the turbine model more stable and less vigilant [see Fig. 12(5)]. To extend some analog output signals – converter's grid side and stator current – as shown in Fig. 12(7) these signals will be transferred from NI PXIe 7858R to NI PXI7833R card via the PXI bus. Those analog signals after up-sampling within its Virtex II FPGA of NI PXI 7833R are sent to the interface board and received by the DFIG control board.

IV. The Interface Board

For connecting the Device Under Test (DUT) to the NI PXI system, signal characteristics of both sides should be considered. NI PXI cards have constrained voltage and current range. We utilized both NI PXIe 7858R and NI PXI7833R cards, which yields a ±10v ±2.5mA range for analog outputs and LVTTL & LVCMOS compatibility at digital IOs (ref: NI PXIe 7858R [40] and NI PXI7833R [41] specification). The provided signals from sensors for control unit contain high voltage digital IOs with high source/drive current (e.g., for contactor command and check backs), and analog signals up to several volts with hundreds of milliampere current from sensors. For resembling a real field converter's sensor signals, an interface board is required with level shifters, fiber optic inputs, and precision power amplifiers circuits. The interface board connects to NI PXI via SCSI connectors and performs voltage and current level conversion to the real sensors signal value, and creates an electrical isolation barrier for NI PXI cards. Table II shows the specifications of the interface board. Fig. 13 depict the interface board and its components.

Table I
NI FPGA Used Resources During Compilation

Device utilization	Used	Total	Percent
Total slices	29658	50950	58.2
Slice Registers	34429	407600	8.4
Slice LUTs	91768	203800	45.0
Block RAMs	321	445	72.1
DSP48s	737	840	87.7

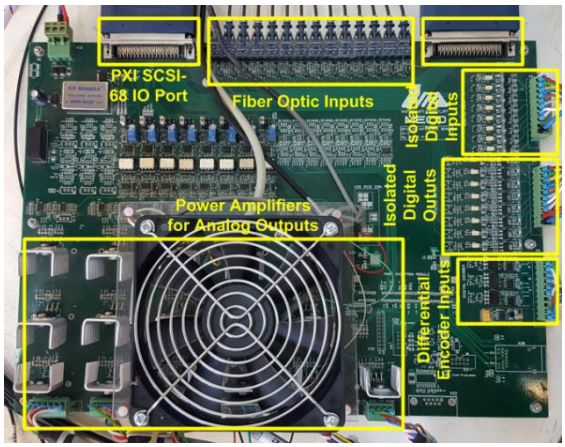

Fig. 13. Interface board

V. DFIG Inverter's Control Board

A. Hardware Specification

For testing and evaluating the DFIG HIL emulator, a commercial controller board of a DFIG converter belonging to a 2.5MW wind turbine generator system (WTGS) has been employed. It receives emulated DFIG converter's real scale signals via the interface board. The controller board uses a Cortex-M4 architecture ARM processor with a core clock of 180MHz and a Xilinx FPGA to perform control actions and digital signal processing. It benefits 12bit resolution analog inputs to read signals of the converter's voltage and current sensors. It also has digital I/Os for relays, encoder, and an RS232 interface to PC is employed for tuning of control coefficients and read/write of system parameters. Fig. 14 shows the structure of the controller board and its peripherals. The developed software performs the related control algorithm in a time cycle of 142.8µs. It generates PWM pulses in 3.5 kHz frequency and resolution of 20ns to control IGBT switches of the converter and send them by fiber optic transmitters to the interface board. The controller board and its interface with the HIL system are shown in Fig. 15.

B. Control Philosophy

The DFIG control board uses a vector control method for regulating output power and DC link voltage. In SYRF, by orienting one axis along with the stator voltage or flux, a decoupled active and reactive power control can be achieved [32]. In this case, the *d* axis is aligned to the stator voltage. Consequently, output active and reactive power can be controlled by the *d* axis and *q* axis component of the rotor current, respectively.

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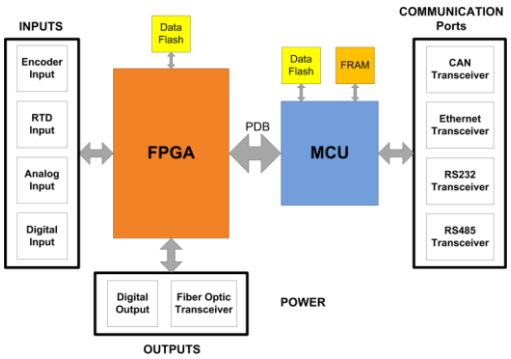

Fig. 14. Structure of controller board.

TABLE II
SPECIFICATIONS OF INTERFACE BOARD

Input/output Ports	Specification
Digital Input	8 × 24v
Digital Output	8 × 24v 1A
Fiber Optic Input	14 × 5Mbd @ 30m
Analog Output	5 × 3phase ±12v 0.7A 1 × 1phase ±12v 0.7A
Encoder Input	3 × 24v Differential Input(A,B,Z,/A,/B,/Z)

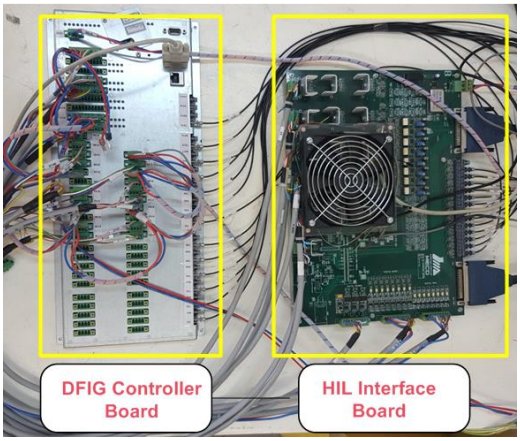

Fig. 15. The controller board and its interface.

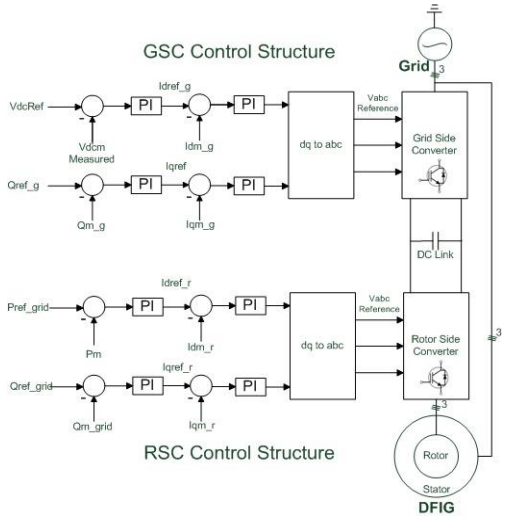

Fig. 16. General control structure of converter.

In the startup process, first, a precharge circuit is activated via the controller by closing a contactor to charge the DC link voltage to an acceptable level for the GSC converter operation. Then, the GSC converter will be activated by the controller, and the DC link voltage will be regulated according to its reference signal using the *d* axis and the *q* axis of GSC current. In this study set-point for the *q* axis is assumed to be zero to have no reactive power injection from the GSC route to the grid. For having a smooth connection of the DFIG stator to the network, a synchronization process is required, in which stator voltage and phase will be adjusted through the regulation of rotor current. After a successful and smooth connection to the grid, DFIG is ready to inject power. The *d* axis current controls output active power or machine output torque, and *q* axis current controls reactive output power. Thanks to the grid voltage orientation and decoupling method, active and reactive power at the output can be controlled independently. The general control structure of the converter is shown in Fig. 16.

VI. EXPERIMENTAL TEST RESULTS

In this CHIL study, a real DFIG converter's control board is connected to the DFIG HIL system, including that represents the remaining mechanical, electrical components, and power system. This model is implemented in MATLAB/Simulink and LabVIEW. National Instrument's PXI system as a platform that guarantees time precision, few deviations, and reasonably low run-time jitter is chosen as the real-time system and presented models are implemented in its FPGAs and CPU. As the main turbine controller and its communications are not in the scope of our study, to start the system, it is required to send start command

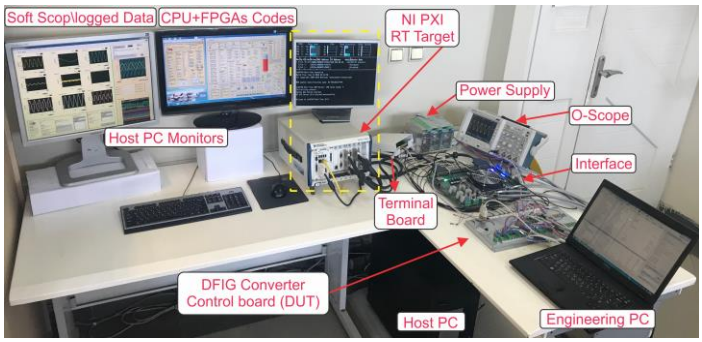

Fig. 17. Overview of the 2.5MW DFIG emulator and the converter control board.

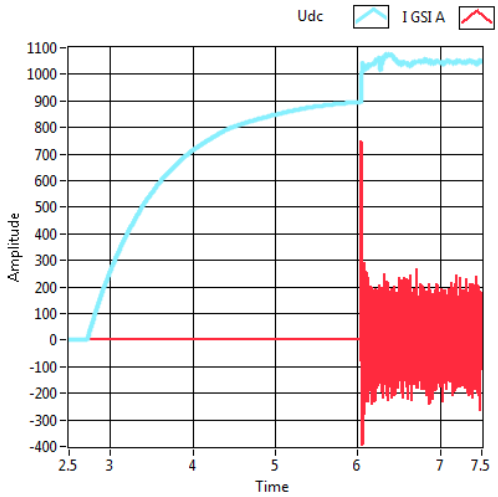

Fig. 18. Pre-charge and DC link boosting.

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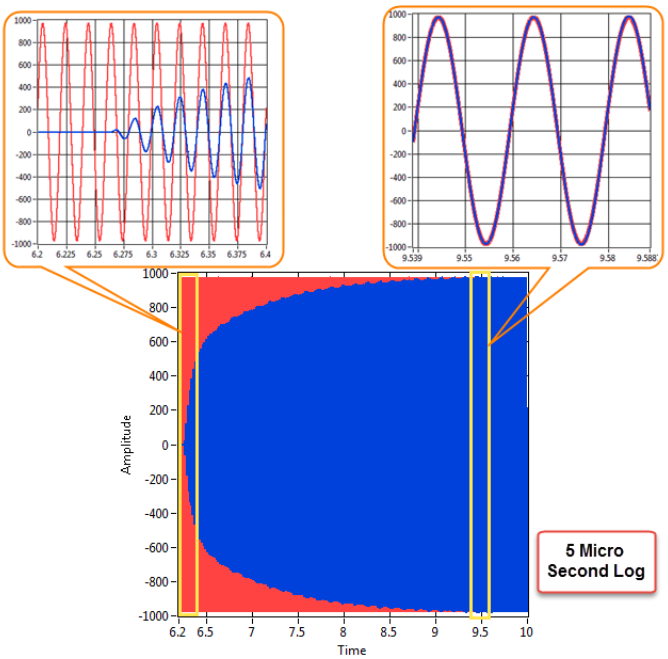

Fig. 19. Stator Synchronization with grid.

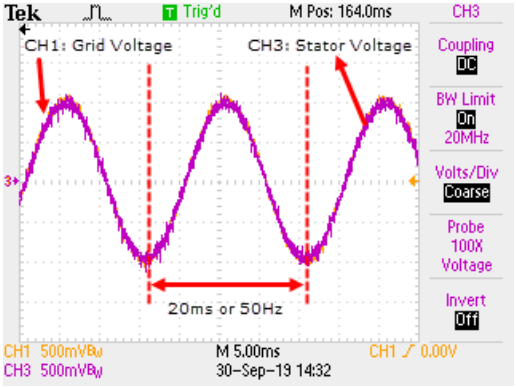

Fig. 20. DFIG Synchronized with the grid [O-Scope, time: 5ms/div, stator and grid voltage: 0.5p.u/div.]

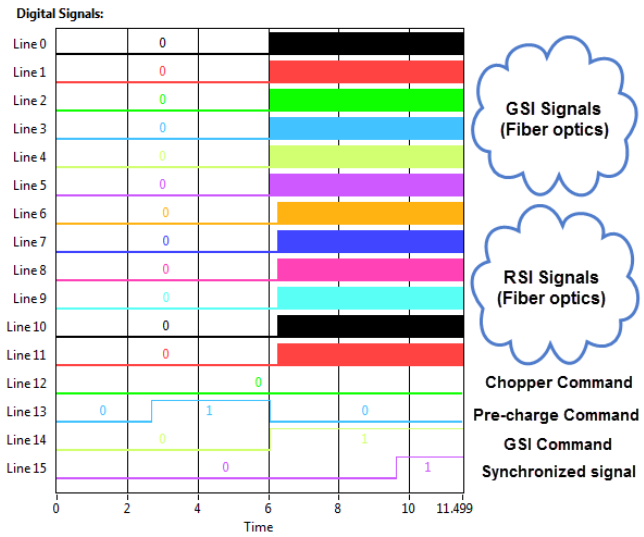

Fig. 21. Startup pulses and signals.

from the engineering PC. Now a live RT electrical loop is constructed between the DFIG converter's control board and the DFIG HIL system.

In this stage, the system will start working from the first controller's inbuilt sequence, DC link pre-charging, to the last operational one, which is power generation. In this HIL emulator, a 2.5MW 690V 50Hz DFIG, which is excited by its back to back converter, is coupled to a 2.5MW WT by a gearbox with a 1:79.2 ratio suitable for 12m/s wind speed. A real DFIG controller board is connected to the CHIL system, as shown in Fig. 17. From the control board, the gird-side and rotor-side IGBT bridges pulses, precharge, breakers, and a maximum 4800 kW/s chopper command are sent to the DFIG emulator. In return encoder pulses, breaker's statuses, actual values of DC link, stator and grid voltages and currents, RSC, and GSC currents will be received by the control board.

Usually, the minimum loop execution time of the hardware under test will dictate the HIL computation speed. The Fastest function in the DFIG converter's controller has a loop time of 142.8µs. This means, in the worst case, the IOs should be updated at least at this rate to provide new data in each control board's loops. In this study empowered by FPGA technology, calculation time was 5µs, which is more than enough for providing required IOs, and the system reported no overrun. Different scenarios have been implemented in this high-speed, safe, and reliable real-time emulator of a complete wind energy generation system, and results are presented as follows.

A. *DFIG Converter's Startup*

Control logic in the DFIG converter controller board has different sequences which after fulfilling one's requirements, the other will be pursued; otherwise, the control board will go into a trip sequence and eventually by blocking gate pulses of IGBTs and opening the circuit breakers, power generation stops. In normal operation, right after reaching to minimum WT speed (700RPM) and after grid breaker closure, the system is ready for DC link pre-charging. In this state, when the control board receives the operation command from WT or farm controller, it will close the DC precharge breaker, and capacitors of DC-link start charging up to 896 V_{dc} when the input AC voltage is 690V. DC link boosting is the next step, in this sequence the control board first close the GSC contactor then sending gate signals by fiber optics to the interface board and eventually to the CHIL emulator activating the grid side (GSC) IGBTs and boosting the DC link up to 1050 V_{dc} (see Fig. 18). This value can be changed via Engineering PC and is highly relevant to the nominal voltage range of IGBTs and the maximum voltage spikes of the designed bridge and its architecture.

When the DC link boosted, rotor side IGBTs (RSC) in the DFIG Emulator will be activated via fiber optics in the same way through the interface and control board. IGBTs switching will eventually lead to a current flow in rotor windings. The frequency of the injected current depends on its angular speed (ω_r) and the electrical angular speed of the grid (ω_s). Rotor side converter's activation will excite the DFIG and induce a three-phase voltage with the grid's frequency on stator winding. Provided feedbacks from the CHIL emulator will help the board's controller to synchronize the stator's voltages with grid voltages by changing the amplitude and phase of stator voltages. Finally, when both phase and amplitude are reasonably alike, the stator contactor will be. Fig. 19 confirm the above explanations. As shown in this

figure V_{as} or the stator voltage is reaching to V_{ag} grid voltage during the synchronizing state. Fig. 20 shows the oscilloscope trace of stator and grid voltages, which are synchronized. O-Scope's probes are connected to the output of the interface board, and as the values are in p.u, the base values of voltages are 563V. Startup sequences, including twelve fiber optics GSC, RSC signals, and circuit breakers digital commands and status signals, are displayed in Fig. 21 beside the chopper's command signal.

B. *Power generation*

After synchronization and grid connection, the DFIG converter regulates the active and reactive power of DFIG. This regulation is by controlling the rotor current and usually at nominal speed (1150RPM). Pitch controller regulates the blade's position to pursue nominal speed on the turbine, which is above synchronous speed for the six pole generator. The converter itself can also provide 800KW or 30% of nominal generated power. The maximum amount of active power generation by DFIG depends on the mechanical input torque, and the set-point is provided by WT control. In this study, as the main focus was on the DFIG controller board, fixed torque on different turbine speed in either under synchronous or above synchronous speed was added as an additional function to the turbine model, and the engineering PC gave active power set-point to the DFIG control board. In this situation, a full range of active power could be generated in a speed range of 700 to 1300 RPM. According to Fig. 22 as an example in 1150RPM or 1.15p.u of rotor nominal speed (Base: 1000RPM), active power set-point increases from zero to 2.5MW (Full Power).

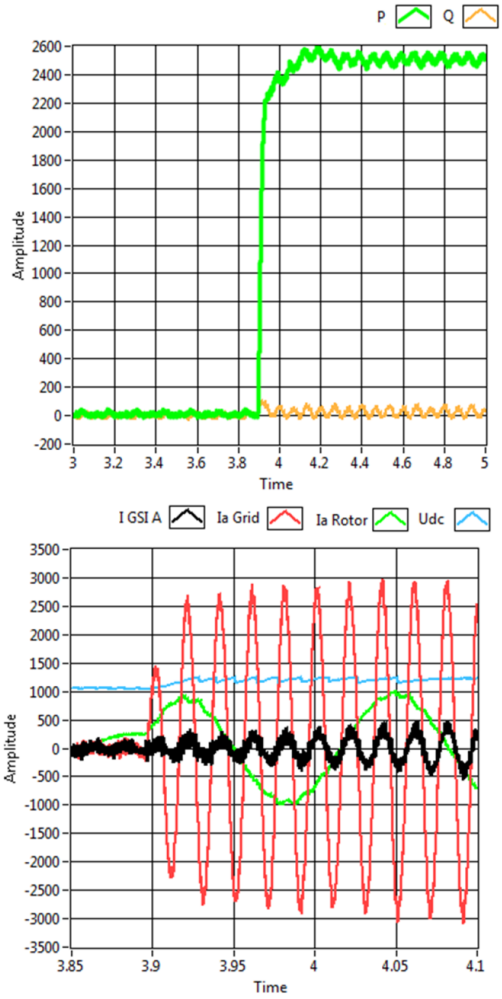

Fig. 22. Active power jump 0 to 2.5MW.

Take this into account that in normal operation often such sudden change in set-point does not occur, and the wind turbine controller after computing maximum power point tracking (MPPT) or maximum reachable power set-point; slowly increases the power set-point. During system tuning or converter's commissioning to adjust the GSC and RSC PIDs, such step response is essential to fine-tune the rotor *dq* currents, DC link voltage PID controllers. Fig. 22 also displays the first phase of GSC current, the grid's current, rotor side current, and DC link voltage. Chopper activation (sudden decline in DC link) is visible in this figure, and retuning of GSC converter's PID should be requested!

C. *Grid Voltage Dip*

Voltage dip is a common phenomenon, especially in weak power networks. Simulation of such a test or three-phase stator voltage fault in a safe environment is an advantage embedded within the emulator. Software and system developers who are aiming to manage low-voltage ride-through (LVRT) or fault ride-through (FRT) functions within the control board, and meeting requirements of grid-code can employ this feature and test their algorithms. Fig. 23 demonstrates a 0.2p.u network voltage dip while the turbine speed is 1.15p.u and P=2.5MW and Q = 0MVar. Base values are 1000RPM for rotor speed, 563 for all voltages, 2953 for stator side currents, and 965.6 for rotor side currents.

VII. Performance Comparison with Typhoon HIL

To evaluate our developed system, in this section, a comparison is made between yielded results from the proposed system and Typhoon HIL 602+, which is a well-known commercial HIL system and is utilized by many research centers and industries. This system has 32 digital I/Os, 32 analog outputs, and 16 analog inputs. It uses four processing cores, which can simulate models with a time step higher than 0.5µs [42]. An electronic interface is required, which has different requirements in comparison to our interface. Complete setup including a computer for visualizing the results using Typhoon HIL Control Center is shown in Fig. 24. One example of results obtained using the Typhoon HIL Control Center is shown in Fig. 25. Two main scenarios are applied to our HIL system and Typhoon HIL 602+. These systems have the same model in their software with negligible differences (e.g., snubbers), and an identical control board with the same software and parameters is connected to both systems.

A. *Power Set-Point Changes*

A step-change in the active power set-point from zero to nominal power is sent to the controller board, and the behavior of both systems is observed. Fig. 26 shows the active power response from both systems to the step-change in active power. As can be seen in that figure, two system's behavior regarding the same change in input is quite similar, and little or no difference can be seen between two graphs. Although same control board and parameters are used to obtain test results from both systems

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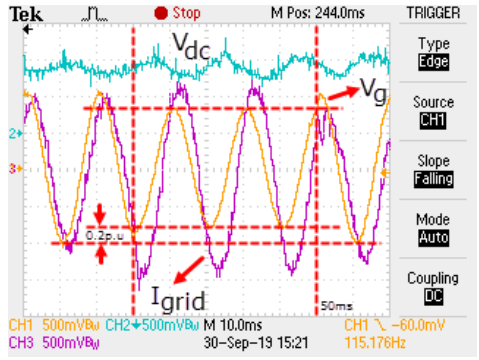

Fig. 23. Oscilloscope trace of 0.2p.u voltage dip of network [time: 10ms/div, Generator voltage (Vg): 0.5p.u/div. Grid Current (Igrid): 0.5p.u\div and link DC voltage (Vdc): 1p.u\div]

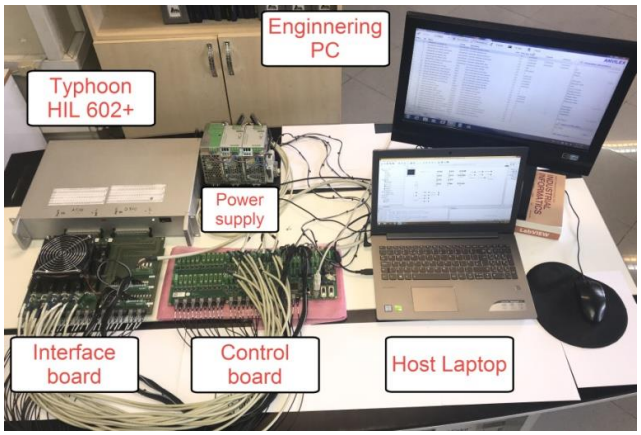

Fig. 24. Typhoon HIL setup.

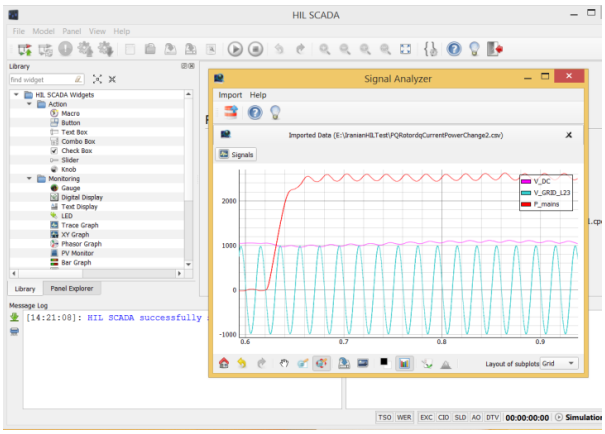

Fig. 25. Typhoon HIL Control Center Results.

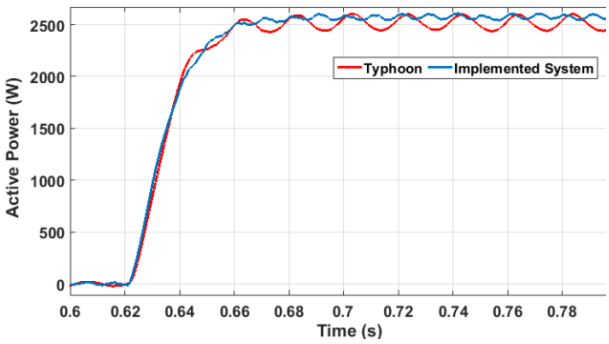

Fig. 26. Active power set-point changes.

but, considering the confidentiality of model implementation, solver selection on Typhoon HIL 602+ and different analog input properties of these systems which mandates designing two different interfaces and calibration error in input voltage and current feedbacks, some minor deviations between results are inevitable.

B. Speed variation

One of the main advantages of DFIG systems is their capability to operate in a speed range approximately 30 percent above or under synchronous speed, which enables them to be a variable speed wind generator with low cost. Due to mechanical mechanisms and the wind blowing patterns, harsh changes in wind speed (severe changes in the time frame of seconds) and, consequently, generator speed usually does not occur. Nevertheless, to show how two models will respond to the same change in generator speed while the same controller board is connected to each system, a fast change in generator speed from 88rad/s to 120rad/s (840 to 1150 RPM) is applied. By changing the generator's speed, the frequency of the rotor currents will be changed, and at the synchronous speed, it will be zero (dc variables). The whole speed range is applied via a ramp. Variations in rotor currents while changing speed (torque reference is kept constant at rated value) are shown in Fig. 27. In both systems, the same behavior in the rotor current is seen. By moving toward synchronous speed frequency of rotor decreases and vice-versa. The shape of rotor currents during these changes is completely dependent on the phase sequence and the instant that change is applied. Due to this issue, results from two systems are drawn in two separate figures, but as it is evident from Fig. 27, two systems exhibit the same performance, and phase sequence will change on synchronous speed.

VIII. Conclusion

In this paper, we presented a Power Electronics oriented Real-Time HIL emulator to test some transient and dynamic behaviors of power electronics converters. A 2.5MW DFIG was modeled, and its controller board tested during this study. Models depend on their fundamental sample time developed for real-time system's CPU or FPGA-based PXI card by LabVIEW FPGA

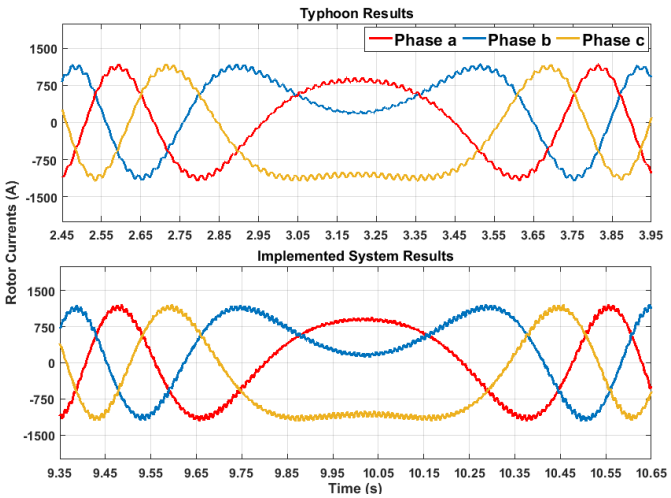

Fig. 27. Speed variation from sub synchronous to over synchronous speed.

Module, LabVIEW Control Design and Simulation Module or MATLAB/Simulink HDL generator. The complete system comprises the DFIG Control board, NI PXIe Chassis, specially designed interface board, and LabVIEW-base software. Proper matching between the implemented HIL emulator and identically developed DFIG 2.5MW model in Typhoon HIL 602+ confirms the accuracy and effectiveness of the proposed DFIG Real-Time HIL emulator. Such systems can be employed to debug the DFIG controller software, improve the inbuilt DFIG control functions, educate new operators, and test new control boards and related devices before installation and commissioning of new DFIG converters.

On the contrary to commercial HIL emulators such as Opal-RT, RT-Box or Typhoon HIL which are often designed for end-users and the calculation recourses needs to be divided among processing cores, proposed NI PXI based HIL Emulator, support integrated and customized modeling in user-friendly graphical software like MATLAB/Simulink and LabVIEW. This versatile emulator allows everyone to expand their model based on required mathematical equations of the system and choose the hardware regarding their number of required I/Os or communication protocols. This capability decreases hardware price by omitting unnecessary equipment and not to be limited only by the provided library, mathematical solver, and even hardware of the commercial HIL Emulators.

Although many custom-made CHIL systems are presented in the literature, these systems have a relatively high step-time. They are not appropriate for power electronic studies with high switching frequencies. The proposed system with fixed-point variables and HDL libraries provides researchers with sufficiently low step-time, which helps them to emulate power switches efficiently. For instance, in this study, besides the mechanical models with 10ms loop time in CPU, a CHIL system with 5us step-time and 40.463ns critical path delay was introduced, which contained the DFIG model, switches and other electrical components connected to a real DFIG Controller. These tools provide a versatile and fast solution for testing critical scenarios and help operators or designers in a plant to perform complex experiments or test modified control algorithms.

ACKNOWLEDGMENT

The Authors would like to express sincere gratitude and appreciation for MECO's funding, support and constant encouragement towards bringing this research into fruition. (http://www.mapnaec.com/en/)

This work was also supported to publish by VILLUM FONDEN under the VILLUM Investigator Grant (no. 25920): Center for Research on Microgrids (CROM). (www.crom.et.aau.dk).

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