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Theoretical Analysis and Experimental Validation of Flying-Capacitor Multilevel Converters under Short-Circuit Fault Conditions

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Abstract—Addressing the increasing demand for high-efficiency and high-power-density converters, the flying-capacitor multilevel converter has shown itself as a promising topology. A key advantage of this topology is the reduced voltage rating of the switches, which also makes it vulnerable to device failure during short-circuit conditions. Despite a large interest in fault-tolerant operation of these converters alongside detailed descriptions of flying capacitor balancing during different conditions, little research has focused on the converter short-circuit fault analysis, which may cause a switch failure if not properly designed for. To address this vulnerability, this work presents a comprehensive model describing the large-signal short-circuit switching behavior of a general N-level flying-capacitor multilevel converter. Based on this, highly simplified models used to predict the evolution of the switch current and voltage stress during the fault are proposed, targeted at practicing engineers for conservative design guidelines. These models are used to determine the time for remedial action of the converter before reaching some predefined maximum tolerable conditions. A 2-to-10-level fully-configurable flying-capacitor multilevel converter and a fault circuit hardware prototype are used to experimentally perform different short-circuit tests, which shows a good match between the predicted and measured behavior.

Index Terms—Flying-capacitor multilevel converter, Voltage-Source Converter, Short-circuit, transient response, Modeling

I. INTRODUCTION

With the continuing growth in renewable power generation and electrical transportation such as electrical on-highway and off-highway traction applications and more electric aircraft, a more demanding request for high-efficiency and high-power-density converters has emerged [1], [2]. To achieve a high power density, multilevel converter topologies [3] are often utilized since they enable a remarkable reduction in the volume of passive components, especially in the output filter inductance [4]. This benefit is achieved through a multilevel output voltage and high effective inductor switching frequency. In particular, the flying-capacitor multi-level converter (FCML) has proven itself as a strong candidate in meeting

such demands, especially for low-to-medium power/voltage applications [5]–[7]. Compared to the modular multilevel converter (MMC), which operate the flying capacitors at the fundamental frequency, the flying capacitors in an FCML converter are switched at the switching frequency [8]. This feature makes it possible to use a smaller capacitance value and thereby improve the power density using high switching-frequency wide band-gap semiconductor devices, such a GaN [9]. However, compared to the MMC, the FCML converter does not have this cell redundancy property, which makes it more vulnerable to device failure. Accordingly, reducing the risk of any device failure is even more important for an FCML converter. Due to the high number of components in multilevel converters, analysis of converter reliability and potential device failure has been studied thoroughly in the past [10]–[16].

These strategies involve fault-tolerant operation with intelligent detection and remedial action as a result of device failure. Nevertheless, prior work does not discuss how such failures may appear from severe critical conditions or present a modeling framework for such transient events. Critical operating conditions, including short-circuit operation of the FCML converter is discussed in [17]. Here, a short-circuit test of an FCML is conducted in simulation, but no analyses on the fault transients are given. Regarding FCML modeling, a great number of publications address the dynamic modeling of voltage balancing of flying capacitors. An often used modeling approach for the nonlinear switched capacitor system is to employ an averaged representation of the switching process. However, since the flying capacitor dynamics happen at the switching frequency, events of interest cannot be captured using an averaged model. Therefore, the switching process is either approximated with a Fourier representation in the frequency domain [3], [18]–[20] or as a state-space representation in the time-domain [21]–[23]. Despite these models' effectiveness in capturing the voltage balancing effects, none of the presented frameworks address short-circuit faults on the FCML. To that end, even though these models are able to describe the flying capacitor dynamics, they still represent an averaged behavior. For fault situations, the deviation around this averaged dynamic response may not be small in value and can therefore not be neglected when evaluating the actual current and voltage switch stress, which may occur during short-circuit conditions.

Previous work addressing fault conditions of FCMLs and multilevel converters focus on fault-tolerant control and how
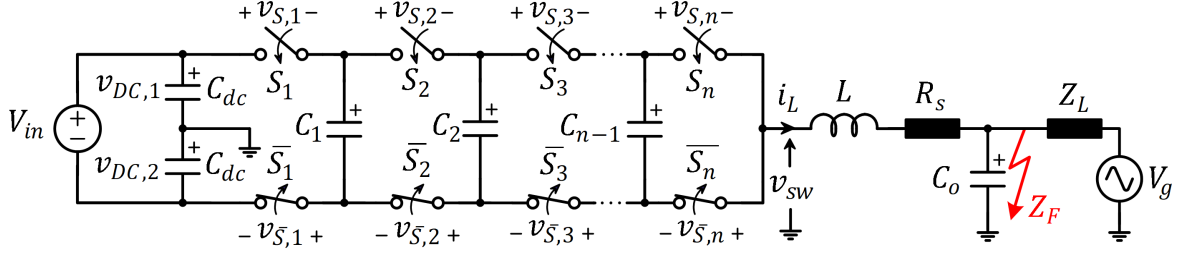
Fig. 1. Single-leg representation of a flying-capacitor multilevel converter. The output filter capacitor is connected back to the dc-link midpoint. A short-circuit occurs with a sudden connected of Z_F.

to deal with a device failure when it already has occurred. Yet, no analysis is performed to study the severe events which may cause such failures, e.g. a short-circuit fault. In this work, we seek to investigate the FCML converters during fault conditions, specifically short-circuit faults, which includes electrically-close grid faults, transformer faults, machine winding faults, and unintended conductive paths as a result of moisture or dust. In either case, robust control must ensure that such events do not evolve into a permanent fault of the converter. Accordingly, a designer should identify the worst-case condition in operation and design the converter and associated control to be able to withstand such conditions without device failure. In this work, a generalized model of an N-level single-leg FCML during a solid short-circuit fault is developed and validated with hardware measurements. Analytical explicit equations are derived based on a simplified nonlinear switching model, enabling the accurate calculation of the available time for remedial action without violating the ratings of the switches. The trends and findings of the presented generalized model are verified through experimental short-circuit tests of a fully configurable 2-10 level FCML. This is to the authors' best knowledge the first publication on actual experimental short-circuit tests of such FCML converters. The findings and expressions in this article serve to educate the reader of the short-circuit behavior of FCMLs and how the converter may be designed to avoid device failure during such severe events.

The remainder of this article is organized as follows: A generalized modeling framework of the N-level FCML is developed and verified in Section II. Based on this model, simplified models describing the current and voltage stress of the converter switches are presented in Section III. The proposed models are experimentally verified in Section IV and compared to other FCML designs. Finally, the article is concluded in Section V.

II. GENERALIZED MODELING OF SINGLE-LEG FCML CONVERTER

If a short-circuit condition occurs, the output current will rapidly increase due to the low resistance and inductance of the conduction path. Following the converter switching operation, different flying capacitors will be inserted in the path of the shorted output, causing a dramatic voltage change in the flying capacitors, which determine the switch voltage stress. In this scenario, two possible causes of failure must be averted:

- The quickly increasing short-circuit current exceeds the device maximum pulsed current rating.
- Voltage imbalances of the flying capacitors cause the voltage on a non-conducting switch to exceed the device blocking voltage.

To capture the pertinent failure mechanisms, the model will include the flying capacitor voltages, the inductor current, and how their evolution during a fault may be predicted.

A circuit representation of the FCML converter is shown in Fig. 1. This is an N-level single-leg converter consisting of $n = N - 1$ complementary operated switch-pairs and $n - 1$ flying capacitors. Each switch can take an on and an off state with the following switching function $S_j(t) \in [0, 1] \ \forall \ j \in [1, \ldots, n]$. The voltage and current of the jth flying capacitor are $v_{c,j}$ and i_j, respectively where $j = 1, \ldots, n-1$ and the capacitor current is defined to flow into its positive terminal following the passive sign convention. The converter output voltage and converter current are filtered by an LC filter, which in turn feeds an impedance and a voltage source, which represents a grid-connected application or motor applications. The filter capacitor C_o is connected to the dc-link midpoint which is directly grounded to earth. For this study, a fault impedance, Z_F, is considered to be abruptly connected across the output capacitor, effectively short-circuiting the output voltage.

The resistor R_s depicted in Fig. 1 represents the parasitic resistance of the output inductor and the on-state resistance of the conducting switches. When analyzing the circuit topology in Fig. 1, one will notice that in any converter state, n transistors will be conducting, hence $R_s = R_L + nR_{DS,on}$ assuming equal and constant on-state resistances of all switches.

a) Model roadmap: The model development is divided into three types of models that are designed for a specific purpose. First, a detailed model capturing the switching dynamics of the system is presented. This model is general which makes it useful when analyzing fault conditions with different number of levels and parameter sweeps. Due to its generality it is well-suited for identifying complicated trends that may not be derived analytically. The second model presents a simple analytical expression for predicting the available time before any switch is overstressed. This is done using a linear and an exponential expression for the switch current and a model for the switch voltage based on a linear inductor current. All

models presented are neglecting the clamping effect of the body diodes of the switches, which happens when the switch voltage reaches around twice its rated voltage. Therefore, being able to predict the switch voltage stress up to twice its nominal operating value is considered more than sufficient for any practical needs.

A. Generalized Equivalent Model

Considering a worst-case condition where $Z_F = 0$, the FCML converter circuit may be represented as a linear charge/discharge circuit of an equivalent capacitor connected across an RL load, as depicted in Fig. 2. It should be noted that such a representation is general since the equivalent capacitance of the inserted flying capacitors C_{eq}, the initial conditions for the equivalent capacitor voltage (V_0), the inductor current (I_0), and the effective input voltage ($V_{in,eff}$) are all functions of the operating switch state. The equivalent circuit diagram shown at the bottom of the figure is constructed from the two above general cases. The top part of the figure represents the cases where $S_1 = 1$ and $S_1 = 0$ as shown in Fig. 2. The dc-link capacitors are considered to have equal capacitance and have the initial voltage conditions $V_{DC1,init}$ and $V_{DC2,init}$. Using these, a generalized representation of the FCML including the dynamics of the dc-link capacitors can be constructed as shown in the bottom part of Fig. 2, where

$$V_{in,eff} = \frac{(2S_1 - 1)V_{in} + V_{DC1,init} - V_{DC2,init}}{2}. \quad (1)$$

The initial conditions for the dc-link capacitors in (1) cannot be reduced since these are only equal prior to the fault condition. C_{eq} may be calculated from the series connection of the inserted flying capacitors as

$$C_{eq} = \left(\sum_{j=1}^{n-1} \frac{|S_j - S_{j+1}|}{C_f} \right)^{-1}, \quad (2)$$

where C_f is the capacitance of each flying capacitor. At the pre-fault condition, the flying capacitors are considered to operate at their nominal voltages defined as

$$V_{c,j,PF} = V_{in} \frac{n-j}{n}, \quad j = 1, \ldots, n-1. \quad (3)$$

Using this, the initial equivalent flying capacitor voltage can be expressed as

$$V_0 = -V_{in} \sum_{j=1}^{n-1} \frac{(S_j - S_{j+1})(n-j)}{n}. \quad (4)$$

Using the generalized circuit from the bottom part of Fig. 2 and the initial conditions for the equivalent flying capacitor voltage (V_0) and the inductor current (I_0), the Laplace domain solution for the inductor current can be found to be

$$i_L(s) = \frac{I_0 s + \frac{V_{tot}}{L}}{s^2 + 2\alpha s + \omega_{0,DC}^2 + \omega_{0,AC}^2} \quad (5)$$

where $\alpha = R_s/(2L)$, $\omega_{0,DC} = 1/\sqrt{2C_{dc}L}$, $\omega_{0,AC} = 1/\sqrt{LC_{eq}}$, and $V_{tot} = V_{in,eff} + V_0$. Here, $\omega_{0,DC}$ is the resonant frequency formed by the paralleled dc-link capacitors and the output inductor, whereas $\omega_{0,AC}$ is the resonant
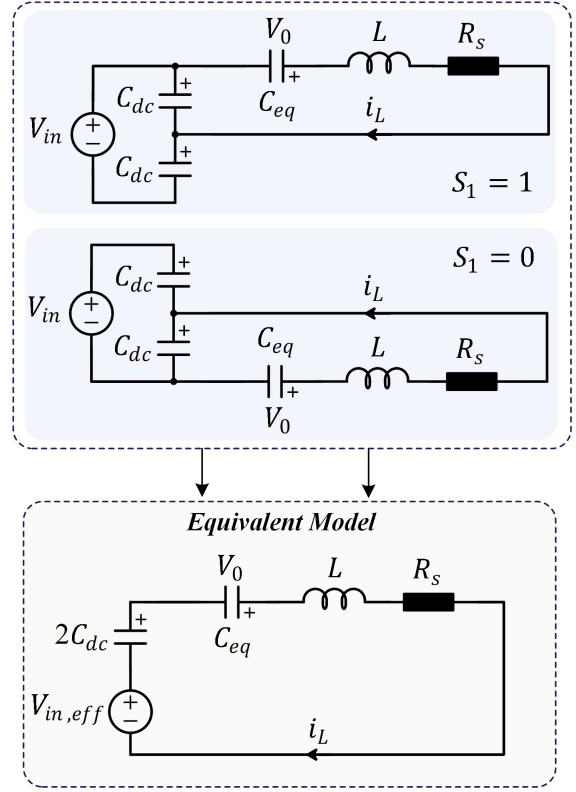

Fig. 2. Equivalent generalized circuit for an N-level FCML converter under a solid short-circuit condition.

frequency formed by the equivalent flying capacitor and the output inductor. Taking the inverse Laplace transformation, the time-domain solution of this second-order differential equation governing the dynamics of the inductor current can be found to be

$$i_L(t) = e^{-\alpha t} \left(I_0 \cosh(\omega_d t) + \frac{(V_{tot} - I_0 L\alpha)}{L\omega_d} \sinh(\omega_d t) \right) \quad (6)$$

where $\omega_d = \sqrt{\alpha^2 - \omega_{0,DC}^2 - \omega_{0,AC}^2}$.

It should be noted that V_0 in the expression for the inductor current is initially calculated from (4). For the next switching state, the flying capacitor connections may have changed, which implies that the initial condition for the equivalent capacitor has changed to

$$V_0 = -\sum_{j=1}^{n-1} (S_j - S_{j+1}) v_{c,j,init}, \quad (7)$$

where $v_{c,j,init}$ is the last entry in the flying capacitor voltage from the previously computed switching state. Similarly, the initial values of the dc-link capacitors, $V_{DC1,init}$, and $V_{DC2,init}$, are initially assumed balanced, i.e. $V_{DC1,init} = V_{DC2,init} = V_{in}/2$, whereas for the next switching state their initial voltages are found from the last value from the previous state. Initial values are likewise updated for the inductor current.

The voltage across a flying capacitor can generally be

expressed as

$$v_{c,j}(t) = \frac{1}{C_f} \int i_{c,j}(t) \, \mathrm{d}t + v_{c,j,init} \quad \text{for} \quad j = 1, \ldots, n-1. \tag{8}$$

where the flying capacitor current is

$$i_{c,j} = i_L(t)(S_j - S_{j+1}) \quad \text{for} \quad j = 1, \ldots, n-1. \tag{9}$$

Now, each flying capacitor voltage can generally be expressed as

$$v_{c,j}(t) = \frac{(S_j - S_{j+1})}{C_f} \int i_L(t) \, \mathrm{d}t, \tag{10}$$

where the initial condition is included in the formulation of i_L. Inserting the expression for the inductor current (6), the jth flying capacitor voltage can be calculated by (11) where $v_{c,j}(\infty)$ is the final value of that capacitor voltage when the considered switching state is left unchanged. The full solution in (11) consists of the natural transient response of the non-forced system, including initial conditions and the particular solution that describes the final value of the system. The final value is found by inspection and is discussed later.

During a fault condition, the dc-link capacitor voltage will also change, and must be calculated. Since the dc-link capacitors are assumed to have equal capacitance, they will share the load current equally. This means that by defining the capacitor current to flow into the defined positive terminal of the capacitor, it is always true that $i_{DC1} = -i_{DC2}$. When $S_1 = 1$, the top capacitor voltage will discharge by injecting current and the bottom one will charge. The opposite is true when $S_1 = 0$. Using this constraint, the currents in the dc-link capacitors can then be found to be

$$i_{DC1} = -\frac{(2S_1 - 1)i_L(t)}{2}, \tag{15}$$

$$i_{DC2} = -i_{DC1} = \frac{(2S_1 - 1)i_L(t)}{2}. \tag{16}$$

Accordingly, the dc-link capacitor voltages can be calculated from the inductor current and the above equations as (12) and

$$v_{DC2}(t) = -(v_{DC1} - v_{DC1}(\infty)) + v_{DC2}(\infty). \tag{17}$$

1) Final Value of Capacitor Voltages: For any circuit state, if left unchanged, the capacitor voltages will eventually settle on final steady-state values. This case is shown in Fig. 3 for a general case. In steady-state it is true that

$$V_{tot} + \Delta v_{DC}(\infty) + \Delta v_{c,eq}(\infty) = 0.$$

Accordingly, the final values for the dc-link capacitors and the flying capacitors can be found from this equation. It should be noted that $\Delta v_{DC}(\infty)$ and $\Delta v_{c,eq}(\infty)$ represent the change from their initial condition, which is contained in the expression for V_{tot}. Hence, this change can be expressed from the voltage divider formula as

$$\Delta v_{DC}(\infty) = V_{tot} \cdot \frac{C_{eq}}{2C_{dc} + C_{eq}}, \tag{18}$$

$$\Delta v_{c,eq}(\infty) = V_{tot} \cdot \frac{2C_{dc}}{2C_{dc} + C_{eq}}. \tag{19}$$

With this, the expression for the final value of each of the

capacitors can be calculated. From the top part of Fig. 2, the final values of the dc-link capacitors should together with the inserted equivalent capacitors satisfy Kirchoff's voltage law as

$$v_{DC1}(\infty) = V_{in}(1 - S_1) + v_{c,eq}(\infty), \tag{20}$$

$$v_{DC2}(\infty) = V_{in}S_1 - v_{c,eq}(\infty). \tag{21}$$

where the final value for the equivalent capacitor is

$$v_{c,eq}(\infty) = \Delta v_{c,eq}(\infty) - V_0. \tag{22}$$

Here, $v_{c,eq}(\infty)$ represents the final voltage of all the inserted series-connected flying capacitors (the equivalent flying capacitor). Using the final value for the voltages on the equivalent capacitor ($v_{c,eq}(\infty)$), we may define the final value of the jth capacitor where it is assumed that it alone will counterbalance the voltage from the dc-link to achieve zero current in steady state. This is denoted as $v_{c,j,max}$ and is expressed as (13). It should be noted that the last term in (13) is included to take into account that when the flying capacitor is not inserted, it remains at its initial voltage. Using (13), the final value of each individual flying capacitor $v_{c,j}(\infty)$, considering that they share the balancing, can be found as

$$v_{c,j}(\infty) = v_{c,j,init} + \frac{(v_{c,j,max} - v_{c,j,init})}{\sum_{j=1}^{n-1} |S_j - S_{j+1}|}. \tag{23}$$

With the expression for the flying capacitor voltage being derived, formulations for the voltages for the top and bottom switches can be expressed as

$$v_{S,j}(t) = (1 - S_j)(v_{c,j-1}(t) - v_{c,j}(t)) + R_{DS,on}i_L(t), \tag{24}$$

$$v_{\bar{S},j}(t) = S_j(v_{c,j-1}(t) - v_{c,j}(t)) - R_{DS,on}i_L(t), \tag{25}$$

for $j = 1, \ldots, n$ and $v_{c,0} = V_{in}, \; v_{c,n} = 0$.

2) Case of no inserted flying capacitors: The equivalent circuit shown in Fig. 2 assumes that at least one flying capacitor will be inserted given any state. However, this is not true when either all transistors are on or off, i.e. $S = 11 \ldots 1$ or $S = 00 \ldots 0$. Considering these two special switch cases, the equation for the inductor current will be valid if $C_{eq} = 0$, $\omega_{0,AC} = 0$. For these cases, the flying capacitors will not be inserted, and hence their voltages will not change, i.e. $v_{c,j}(t) = v_{c,j,init}$. Lastly, the expression for the voltages of the dc-link capacitors reduces to (14) where $\omega_d = \sqrt{\alpha^2 - \omega_{0,DC}^2}$ and the voltage of the second dc-link capacitor is computed from (17). For the switching state $S = 11 \ldots 1$, the final values for the dc-link capacitors and flying capacitors are $v_{DC1}(\infty) = 0, \; v_{DC2}(\infty) = V_{in}, \; v_{c,j}(\infty) = v_{c,j,init}$, where $v_{c,j,init}$ is the initial voltage of the jth flying capacitor when the state $S = 11 \ldots 1$ is entered. Likewise for the switching state $S = 00 \ldots 0$, the final values for the capacitors are $v_{DC1}(\infty) = V_{in}, \; v_{DC2}(\infty) = 0, \; v_{c,j}(\infty) = v_{c,j,init}$.

B. Model Validation

The developed model is compared to a PLECS simulation for a 5-level FCML. The results of the inductor current and flying capacitor voltages can be seen in Fig. 4(a) and Fig. 4(b),

$$v_{c,j}(t) = -\frac{2C_{dc}C_{eq}(S_j - S_{j+1})}{C_f(2C_{dc} + C_{eq})}e^{-\alpha t}\left(V_{tot}\cosh(\omega_d t) + \frac{\left(V_{tot}\alpha - I_0\left(\frac{1}{2C_{dc}} + \frac{1}{C_{eq}}\right)\right)}{\omega_d}\sinh(\omega_d t)\right) + v_{c,j}(\infty), \tag{11}$$

$$v_{DC1}(t) = -\frac{C_{eq}(2S_1 - 1)}{2C_{dc} + C_{eq}}e^{-\alpha t}\left(V_{tot}\cosh(\omega_d t) + \frac{\left(V_{tot}\alpha - I_0\left(\frac{1}{2C_{dc}} + \frac{1}{C_{eq}}\right)\right)}{\omega_d}\sinh(\omega_d t)\right) + v_{DC1}(\infty) \tag{12}$$

$$v_{c,j,max} = (S_j - S_{j+1})\left(v_{c,eq}(\infty) - \sum_{i=1,i\neq j}^{n-1}(S_i - S_{i+1})v_{c,i,init}\right) + v_{c,j,init}(1 - |S_j - S_{j+1}|) \tag{13}$$

$$v_{DC1}(t) = e^{-\alpha t}\left(V_{tot}\cosh(\omega_d t) + \frac{\left(V_{tot}\alpha - \frac{I_0}{2C_{dc}}\right)}{\omega_d}\sinh(\omega_d t)\right) + v_{DC1}(\infty) \tag{14}$$
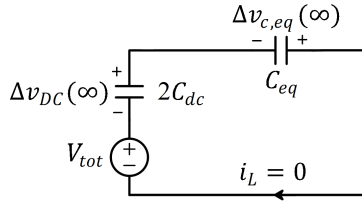

Fig. 3. Equivalent generalized circuit with $t \to \infty$ for any given state.

respectively, which confirms the accuracy of the presented model. Accordingly, the described model fully describes the detailed dynamics of the N-level FCML and will lay the foundation for further analysis regarding design consideration in addition to the expected voltage and current stress on the switches during short-circuit faults.

III. SWITCH STRESS DURING SHORT-CIRCUIT FAULT

To achieve natural balancing of the flying capacitors and considering the popularity of the method [24]–[27], the Phase-Shifted Pulse-Width Modulation (PS-PWM) method is considered for this analysis. Fig. 5 shows the operation of the converter with a sinusoidal duty cycle, $D \in [0, 1]$. As can be seen from the converter switched output voltage, v_{sw}, the sinusoidal duty cycle is synthesized using N distinct voltage levels where the converter will switch between two neighboring voltage levels when the duty cycle is within a certain range. These ranges are $D = [0.75, 1]$, $D = [0.5, 0.75]$, $D = [0.25, 0.5]$, and $D = [0, 0.25]$. To simplify the analysis, and considering the fact that during a short-circuit condition, the state trajectories of interest are within the first tens of inductor switching cycles, the duty cycle is considered constant. Using PS-PWM, the n carriers will be equally distributed within the switching period where the phase shift for each carrier can be calculated as

$$\phi_j = \frac{2\pi(j-1)}{N-1} \quad \text{for } j = 1, \ldots, n. \tag{26}$$

A. Switch Current during Short-circuit Condition

Using the model presented in Section II, the inductor current for a 5-level FCML with the duty cycle swept from 1 to 0 in steps of 0.1 is shown in Fig. 7(a). It is evident from Fig. 7(a) that the previous expression for the inductor current evaluation

for each switch state may be characterized by a significantly simplified model in the early time of the fault. Dependent on the time period of interest and model accuracy, either a linear approximation or an exponential charging function can characterize the inductor current accurately. The intuition behind such an approximation is that for a given duty cycle, the converter aims to output an average voltage of $(2D-1)V_{in}/2$, which will cause the current to rise determined by L and R_s. For a duty cycle of 0 or 1, this average representation would be nearly exact since no flying capacitors are switched. However, for duty cycles in between, the non-ideal operation of the switched capacitors will cause a gradual opposition to the output current, which may be modeled as an added series resistor, which is a function of the duty cycle, D, and the number of levels, N.

As an example, consider the inductor current to be characterized as an exponential charge function, i.e., the solution to a voltage-stepped RL circuit. This can be written as

$$i_{L,e} = \frac{(2D-1)V_{in}}{2R_s}\left(1 - e^{-t\frac{R_s}{L}}\right) + I_0. \tag{27}$$

The response of this is seen to match for $D = 1$ in Fig. 6(b), whereas it has some mismatch for a lower duty cycle. This mismatch can be reduced by increasing the effective resistance. Similarly, considering the inductor current to rise linearly in the region of interest, this may be expressed as

$$i_{L,l} = At + B = \frac{(2D-1)V_{in}}{2L} \cdot t + I_0. \tag{28}$$

The result using this method is seen in Fig. 6(c). As can be seen, the accuracy is not as good as the exponential function, but it gives a much simpler representation and provides a slightly conservative result, i.e., worse estimation than to be experienced in a realistic situation. To that end, the accuracy in a practical range of the switch current has a very low error. In this way, if one designs the FCML to withstand the stress or successfully change its operating state before failure occurs by using the prediction from the linear model, it can be assured to also work for a real-world situation where the switch current will be lower due to the circuit damping resistance.

An identical set of plots is made for numerous levels (4-13) of the FCML as presented in Fig. 7(a). Here it can be

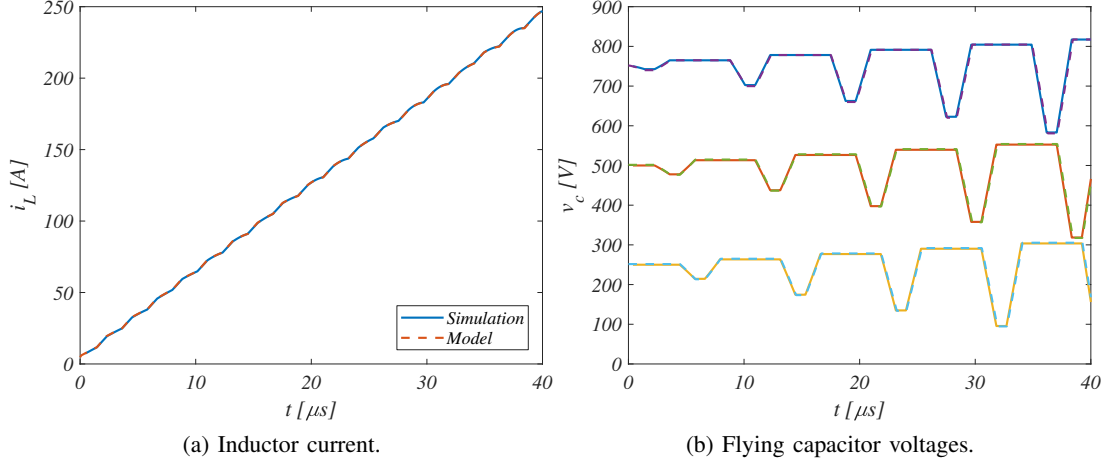(a) Inductor current.

(b) Flying capacitor voltages.

Fig. 4. Validation of the developed model for calculating inductor current and flying capacitor voltages during a short-circuit fault where $D = 0.85$ and $N = 5$. The simulation results are represented using solid lines, whereas the modeled results are shown with dashed lines.
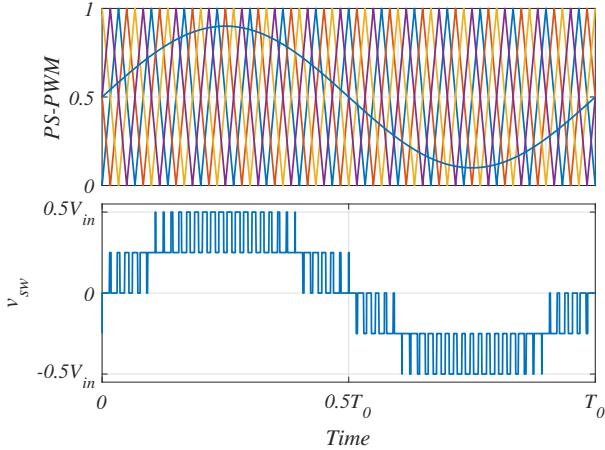

Fig. 5. A 5-level FCML operated with PS-PWM showing the phase-shifted carriers, the reference voltage and the switched output voltage. T_0 is the fundamental period.

appreciated that the inductor currents become more smooth with an increasing number of levels, making the simplified model more accurate. The results are shown for six different duty cycles groups, each consisting of six different number of levels. Since the only parameter being changed is N, the equivalent series resistance of the switches will increase linearly with N, explaining the reduction in inductor current with increasing N. As previously described, the resistance of the exponential function is dependent on the applied duty cycle and N. This is addressed using a compensation factor K which is multiplied with the resistance, which is

$$K = (4.5 - 7 \cdot |D - 0.5|) \cdot (1.3 - 0.05 \cdot N). \quad (29)$$

This function is found on a best fit between the needed resistance to match the modeled results and the applied duty cycle and N. It should be noted that the compensation factor is only valid for the test-data used here and should be reevaluated if data outside this range is needed. Nevertheless, as mentioned previously, for a practical case, it is desired to initiate some fault mitigation strategy in the initial phase of the fault. This

implies that a linear representation or $K = 1$ may be used with sufficient accuracy.

The simplified exponential model with compensated resistance from (29) for $N = 5$ is visualized in Fig. 7(b) showing a good match for all duty cycles. Using the model in (27), and by defining a maximum allowed switch current I_{max}, one can determine the critical time available for remedial action of the FCML as

$$t_F = -\frac{L}{KR_s} \ln\left(\frac{V_{in}(2D-1) + 2KR_s(I_0 - I_{max})}{V_{in}(2D-1)}\right) \quad (30)$$

which is valid for $D > 0.5$. It should be noted that the inductor current is symmetrical around $D = 0.5$ and therefore, the evaluation of t_F on this duty cycle range is fully descriptive.

B. Charging and discharging intervals of flying capacitors

With the inductor current determined during the fault, a simplified representation for the capacitor voltages may be expressed. For this, the charging and discharging intervals of the flying capacitors need to be known. Using PS-PWM and considering the jth flying capacitor, each switching period can be divided into four different regions: an interval where the capacitor is charged (T_C), a subsequent interval after charging where the capacitor is not inserted (T_{AC}), the discharging interval of the capacitor (T_D), and the not inserted period after the discharge (T_{AD}). These periods are defined by the on-interval of the two surrounding switches. Depending on the applied duty cycle, these four regions can be determined as shown in Fig. 8. Here the top switching signal is S_j whereas the bottom is S_{j+1} considering the jth flying capacitor. When the duty cycle is below $1/(N-1)$, the charging and discharging intervals increase proportionally with the duty cycle as evident from Fig. 8(a). In the duty cycle range in Fig. 8(b), the charging and discharging intervals are independent of the duty cycle and fully determined by the phase shift between the two carriers. At last, for the duty cycle range shown in Fig. 8(c), the charging and discharging times are proportional to $1 - D$. Also, for the cases in Fig. 8(a) and Fig. 8(c), T_{AC} and T_{AD} represent the same state, whereas the color difference is merely
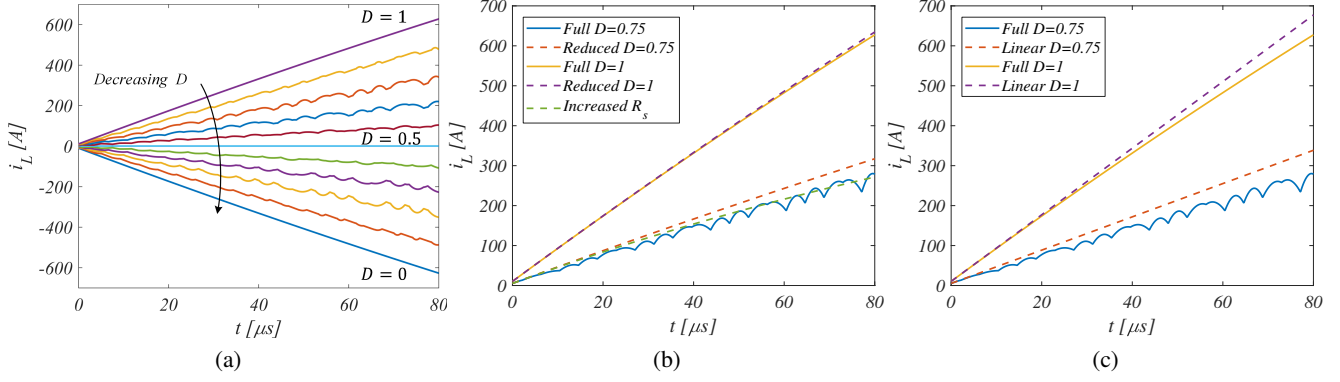
Fig. 6. (a): Short-circuit fault inductor current of 5-level FCML for swept duty cycles between 0 and 1 in steps of 0.1. (b)-(c): Inductor current for $D = 0.75$ and $D = 1$ using developed full model and reduced representation for $N = 5$ (b): Exponential charge functions, (c): Linear model.
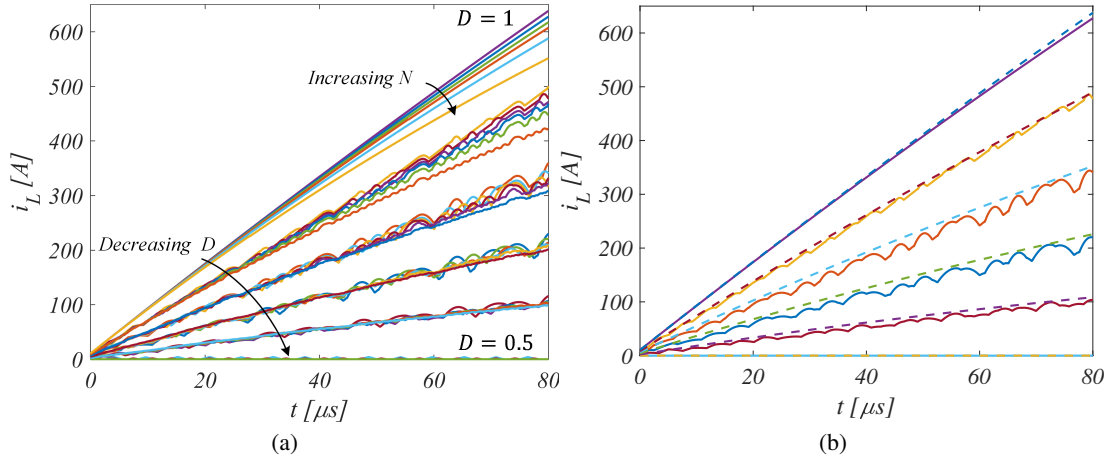

Fig. 7. Inductor current for 4-13 level FCML with duty cycles between 0.5 and 1 in steps of 0.1. (a): Short-circuit fault inductor current for 4-13 level FCML converters, for duty cycles between $D = 0.5$ and 1. (b): Accuracy of the simplified exponential model with compensated resistance for $N = 5$. Dashed line is the simplified model for each duty cycle.

used to distinguish whether they occur after a charging or a discharging interval. Due to the natural balancing principle of the PS-PWM method, the charging and discharging intervals of the flying capacitors are equal for any duty cycle. Using Fig. 8, these can be expressed as

$$T_{C/D} = DT_{sw} \quad \text{for} \quad 0 < D < D_t, \tag{31}$$

$$T_{C/D} = \frac{T_{sw}}{N-1} \quad \text{for} \quad D_t < D < 1 - D_t, \tag{32}$$

$$T_{C/D} = T_{sw}(1-D) \quad \text{for} \quad 1 - D_t < D < 1 \tag{33}$$

where $D_t = 1/(N-1)$. Since in this work it is desired to characterize the largest capacitor voltage swing during a short-circuit condition, one might expect that the largest voltage oscillation on the flying capacitors will occur when the charging/discharging interval is largest, i.e. $D_t \leq D \leq 1 - D_t$. However, besides the length of the charging/discharging interval, the value of the inductor current has a large influence on the voltage swings. As shown previously, the inductor current increases with the duty cycle. Therefore, based on these two factors, the worst-case should exist in the range $D_t < D < 1$, which gives the largest flying capacitor voltage swings.

Besides the charging/discharging interval, the two constant

voltage periods where the flying capacitors are not inserted are

$$T_{AC} = T_{sw}\left(\frac{1}{N-1} - D\right) \quad \text{for} \quad 0 < D < D_t, \tag{34}$$

$$T_{AC} = T_{sw}\left(D - \frac{1}{N-1}\right) \quad \text{for} \quad D_t < D < 1, \tag{35}$$

and

$$T_{AD} = T_{sw}\left(1 - D - \frac{1}{N-1}\right) \quad \text{for} \quad 0 < D < 1 - D_t, \tag{36}$$

$$T_{AD} = T_{sw}\left(D + \frac{1}{N-1} - 1\right) \quad \text{for} \quad 1 - D_t < D < 1 \tag{37}$$

where the subscripts AC and AD denotes after charging and after discharging, respectively. Fig. 8(d) shows a visualization of the time intervals of a flying capacitor voltage waveform during one switching period.
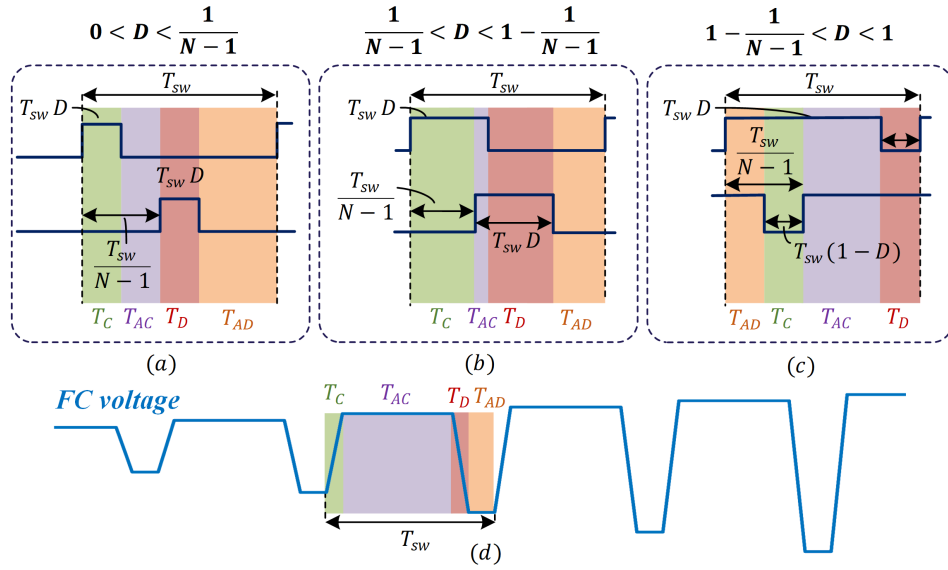
Fig. 8. Time internals of flying capacitor charging (T_C), not inserted after changing (T_{AC}), discharging (T_D), and not inserted after discharging (T_{AD}) divided into three distinct duty cycle ranges (a)-(c). (d): Visualization of time intervals on the flying capacitor voltage waveform.

C. Worst-case duty cycle for Switch Voltage

The developed model from Section II is used to sweep the duty cycle and detect at which D the nominal switch voltage is exceeded with 100% in the shortest time. 3-level to 13-level FCML converters are analyzed and the duty cycle which resulted in the maximum switch voltage stress is recorded and listed as D_{max} in Table I. It is noticed that for all cases, the maximum switch voltage stress occurs for $D > 0.75$ (or $D < 0.25$), whereas the voltage switch stress increases when the duty cycle increases towards 1 for an increasing number of levels. E.g for a 4-level FCML, the duty cycle for max switch voltage stress is 0.77, whereas for a 13-level FCML, the duty cycle is 0.91. For all cases, this is seen to be close to or above $1 - D_t$ defined previously.

D. Switch Voltage during Short-circuit Condition

Based on the previous subsection, the simplified modeling to be developed of the flying capacitor voltages is limited to duty cycles in the range $D > 1 - D_t$, since this is where the maximum stress is found to occur. Using the four charge intervals from Fig. 8(c), the evolution of the jth flying capacitor voltage can be written as (39) where the start time is

$$T_s = \frac{T_{sw}(j-1)}{N-1}. \tag{38}$$

Using the linear expression for the inductor current in (28) and the expressions for the time intervals for $1 - D_t < D < 1$,

TABLE I
DUTY CYCLE RESULTING IN WORST SWITCH VOLTAGE STRESS

Number of Levels	3	4	5	6	7	9	13
D_{max}		0.76	0.77	0.8	0.808	0.84	0.86	0.91

the flying capacitor voltage just after discharging (valley in Fig. 8(d)) evaluated P switching cycles after the short-circuit occurrence can be expressed as (40). Similarly, the flying capacitor voltage after charging evaluated after P switching cycles can be found using the same expression but by evaluating the second summation term to P instead of $P - 1$. These two cases can be simplified and expressed as

$$v_{c,j,AC,P} = V_{in}\frac{n-j}{n} + \frac{AT_{sw}^2(1-D)(P+1)}{C_f(N-1)} \tag{44}$$

and (41) where $A = (2D - 1)V_{in}/(2L)$. By including higher values of P, the flying capacitor charges and discharges to new plateaus where the capacitor is not inserted. This can be seen in Fig. 8(d) and Fig. 9. The peak voltage of a given switch results from the voltage after charging and the voltage after discharging of the two adjacent flying capacitors. During a short-circuit fault, the switch voltage turn-on spike increases with the fault duration time, as shown in Fig. 9. Focusing on this spike and using the expressions in (44) and (41), the increasing switch voltage spike (as seen for $v_{S,j}$ in Fig. 9) of the jth switch evaluated after P switching cycles can be expressed as

$$v_{S,j,P} = v_{c,j-1,AC,P} - v_{c,j,AD,P} + v_{R,j} \tag{45}$$

where

$$v_{c,0,AC,P} = v_{c,0,AD,P} = V_{in}, \tag{46}$$

$$v_{c,n,AC,P} = v_{c,n,AD,P} = 0, \tag{47}$$

$$v_{R,j} = R_{DS,on}(A(PT_{sw} + T_s + T_C) + I_0). \tag{48}$$

Inserting the expressions for $v_{c,j,AC,P}$ and $v_{c,j,AD,P}$, the switch voltage stress after P switching cycles can be formulated as (42). It should be noted that since the first and last switch are directly connected to a clamped voltage, either V_{in} or 0, these will see the lowest voltage stress. Therefore,

$$v_{c,j}(t) = v_{c,j,init} + \frac{1}{C_f}\left(\int_{T_s}^{T_s+T_D} i_L(t)dt + \int_{T_s+T_D+T_{AD}}^{T_s+T_D+T_{AD}+T_C} i_L(t)dt + \int_{T_{sw}+T_s}^{T_{sw}+T_s+T_D} i_L(t)dt + \dots \right) \tag{39}$$

$$v_{c,j,AD,P} = V_{in}\frac{n-j}{n} - \frac{1}{C_f}\sum_{k=0}^{P}\left(\frac{AT_{sw}^2(D-1)(D(N-1)-N(2k+1)+2(k-j)+3)}{2(N-1)} + I_0 T_{sw}(1-D)\right)$$
$$+ \frac{1}{C_f}\sum_{k=0}^{P-1}\left(\frac{AT_{sw}^2(D-1)(D(N-1)-N(2k+1)+2(k-j)+1)}{2(N-1)} + I_0 T_{sw}(1-D)\right) \tag{40}$$

$$v_{c,j,AD,P} = V_{in}\frac{n-j}{n} - \frac{1}{C_f}\left(\frac{AT_{sw}^2(1-D)(D(1-N)+2P(N-2)+2j+N-3)}{2(N-1)} + I_0 T_{sw}(1-D)\right) \tag{41}$$

$$v_{S,j,P} = \frac{V_{in}}{N-1} + \frac{1}{C_f}\left(\frac{AT_{sw}^2(1-D)(D(1-N)+2P(N-1)+2j+N-1)}{2(N-1)} + I_0 T_{sw}(1-D)\right) + v_{R,j} \tag{42}$$

$$t_{crit} = \frac{\frac{T_C}{2} - \frac{I_0}{A} - \frac{T_{sw}}{N-1}}{K} - \frac{C_f(R_{DS,on}I_0 - V_{max} + \frac{V_{in}}{N-1})}{AT_C K}, \quad K = 1 + \frac{R_{DS,on}C_f}{T_C} \tag{43}$$
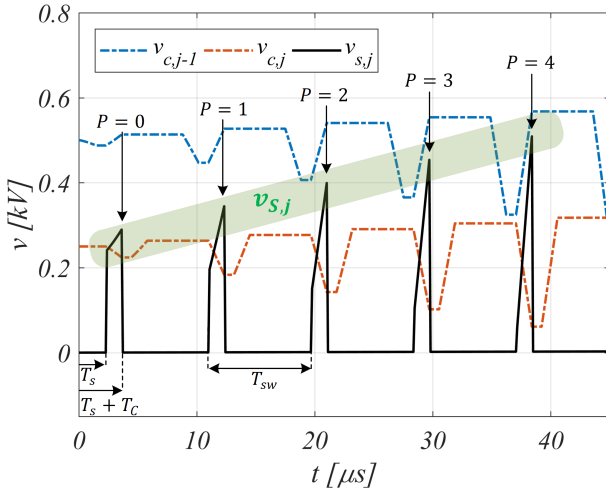

Fig. 9. The voltage across the jth switch formed by the neighboring flying capacitor voltages. The switch voltage spikes are denoted by $v_{S,j}$ evaluated and different P.

one only needs to evaluate the voltage stress of the switches in between as done in (42) valid for $j = 2,\ldots,n-1$. The presented point-wise prediction of the switch voltages presented in (42) is compared to the developed model where the inductor current is assumed linear as in (28). In Fig. 10(a), the point-wise prediction of the switch voltage is shown for S_3 for a 5-level FCML. As can be seen, the prediction matches the modeled results. The same case is shown in Fig. 10(b), but here all switch voltages and point-wise predictions are visualized, where the predictions are highlighted with points and dashed lines. In order to plot the point-wise estimates of the switch voltages as function of time and not P, the following relationship is valid:

$$t = P \cdot T_{sw} + T_s + T_C, \tag{49}$$

where P is a vector going from 0 to k, where k represents the number of switching periods considered for the analysis. Using the relationship between P and time alongside the expression

from (42) and (48), the critical time (t_{crit}) where the maximum allowed switch voltage will be exceeded by $v_{s,j,P}$, can be calculated from (43), where V_{max} is the maximum allowed switch voltage. This approach is valid for any N if the inductor current can be considered linear, i.e., in the initial phase of the short-circuit condition or for systems with a high L/R ratio. Since (43) is derived from the linear equation for $j = 2..n$ from (42), it does not matter how j is selected in (43). This can be understood from Fig. 10(b) where SW2 and SW3 follow the same line but are evaluated at different times based on the switching action. For (43), the time when the straight line reaches some specified V_{max} is computed without taking into account the switching actions. Accordingly, the linear model in (43) cannot distinguish between $SW2, SW3,\ldots SWn-1$. Based on this, the expression for the critical time in (43) is simplified by evaluating $j = 0$.

Using the above method to calculate the critical time where the maximum switch voltage stress is exceeded, the obtained result will be conservative since the estimated current is indeed larger than for a realistic situation. This means that if one designs the control and fault actuation to be sufficiently fast to deal with the above linear formulation, it is assured to also correctly handle a real situation. To that end, since this model assumes ideal switching transitions, overvoltages which will occur during turn-on and turn-off for practical designs are not considered. Therefore, the conservatism of assuming linear inductor currents gives some headroom towards errors associated with unmodeled dynamics and voltage overshoots during switching transitions.

a) Summary of Proposed Models: Three different modeling approaches have been presented. The first is a detailed, high-accuracy model which predicts the switching behavior of the switch voltages and current. Owing to its complexity, this model is less suited for design guidelines but well suited for observing different trends and performing parameters sweeps. Secondly, a simplified exponential expression, which gives a high accuracy approximation of the switch current is proposed.

(a) Results only for the second top switch.

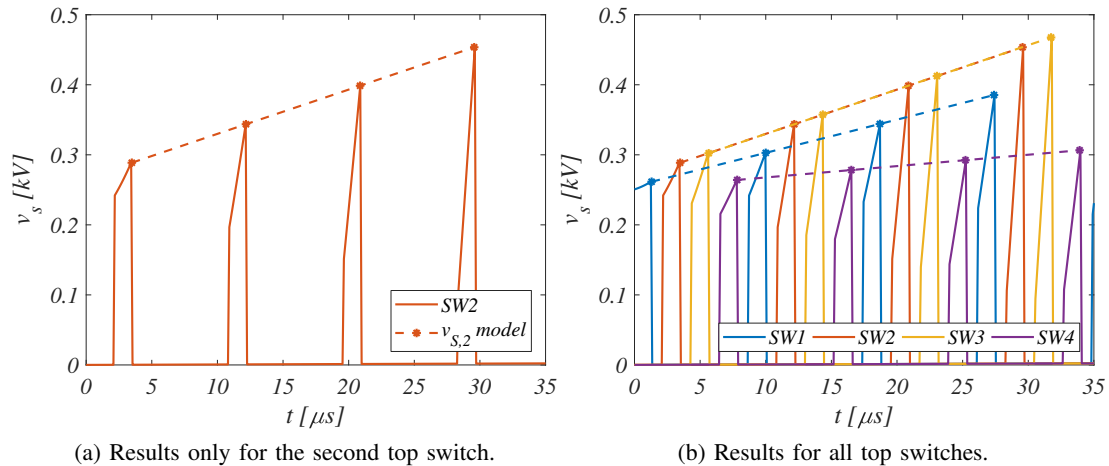
(b) Results for all top switches.

Fig. 10. Voltage stress in top switches of a short-circuited 5-level FCML operated at $D = 0.85$ with a linear inductor current. The actual modeled results and the point-wise prediction using (42) are shown. The dashed line is the point-wise prediction and the solid line is the modeled actual switch voltage.

TABLE II
ACCURACY AND APPLICABILITY OF PROPOSED MODELS

Model type	Short-term	Long-term	Switch voltage	Complexity	Practical value
Detailed	✔	✔	✔	high	low
Exponential	✔	✔	✘	medium	medium
Linear	✔	✘	✔	low	high

TABLE III
COMPONENTS AND PARAMETERS OF EXPERIMENTAL SETUP

Component	Part number	Parameter
GaN switches	EPC2034	200 V, 10 mΩ
GaN gate driver	TI UCC27611	5 V, 6 A
Power isolation	Analog Devices ADuM5010	5 V
Digital isolation	Silicon Labs, Si8610BC	
FPGA controller	Intel Max 10	
Fault switch	Infineon IPT65R033G7	650 V, 33 mΩ
Flying capacitors	MLCC X6S	450 V, 2.2 μF
Inductor	Coilcraft XAL1510-153	25.5 A, 15 μH, soft sat.
Output capacitor	ECW-FD2J395K	630 V, 3.9 μF
-	ECW-FD2J105K	630 V, 1 μF
dc-link capacitor	42 x 450KXW120MEFC18X40	450 V, 4.2 mF, 40 $m\Omega$

Due to its non-algebraic structure, this expression for the inductor current cannot be conveniently applied to derive an expression for the switch voltages. To accomplish this, a third modeling technique that employed simplified models assuming a linear inductor/switch current were developed to describe both the switch voltage and current stress. These models are accurate both for the switch voltage and current a short time period after the fault, which makes it highly useful for practical design guidelines and fault considerations. The accuracy and applicability of the proposed models are summarized in Table II.

IV. EXPERIMENTAL VERIFICATION

The hardware setup built for the experimental verification of the FCML is shown in Fig. 11. The FCML is a 10-level design with two interleaved phases for switching harmonic cancellation [28]. At its nominal design operated at 10 levels, the effective inductor current ripple frequency is above 1 MHz with a power rating of 15 kVA. In this work, only one of the interleaved phases, phase A, is operated, whereas the other phase is bypassed. By shorting different switch-pairs, the converter can be modified to operate at a lower level-count than 10. All tests are operated at a dc-link voltage of 75 V. Owing to the large number of PWM control signals, a field programmable gate array (FPGA) is used to generate gate signals to the transistors. The FPGA is also programmed to activate the fault switch to induce a ground short-circuit fault with a specified duration, duty cycle, and initial switching state of the FCML. To achieve a non-zero initial inductor current, a 12.5 Ω resistive load is connected to the FCML output. Selected components and parameters of the setup are listed

in Table III. The inductors are connected in parallel, which gives a 7.5 μH soft-saturated inductor with a saturation current of 50 A. The flying capacitors utilized for these tests consist of 4 X6S in parallel and 2 in series. This gives a nominal capacitance of 4.4 μF. The fault circuit is measured to have a series resistance of 100 $m\Omega$.

The measurements of voltages and current are taken using a 25-100 MHz differential voltage probe and a 50 MHz current probe, respectively, and visualized on a Keysight MSOX4024A 200 MHz oscilloscope. The inductor output is connected to the drain terminal of the fault switch through a 0.4 m twisted-pair 16 AWG wire. The operation of a 7-level FCML exposed to a fault condition is visualized on the fundamental frequency view, as shown in Fig. 12. Here, the dashed area highlights the fault condition. A zoomed view of a 30 μs short-circuit fault is shown for a 5-level FCML in Fig. 13. As expected, since the inductor current rapidly ramps up, the flying capacitors imbalance and the switch voltage stress increases.

A. Model Validation

The accuracy of the exponential and linear models is analyzed through comparison to the experimental results. Table IV shows the time until the inductor current reaches 20 A, 40 A, and 60 A for the actual experimental measurements and the
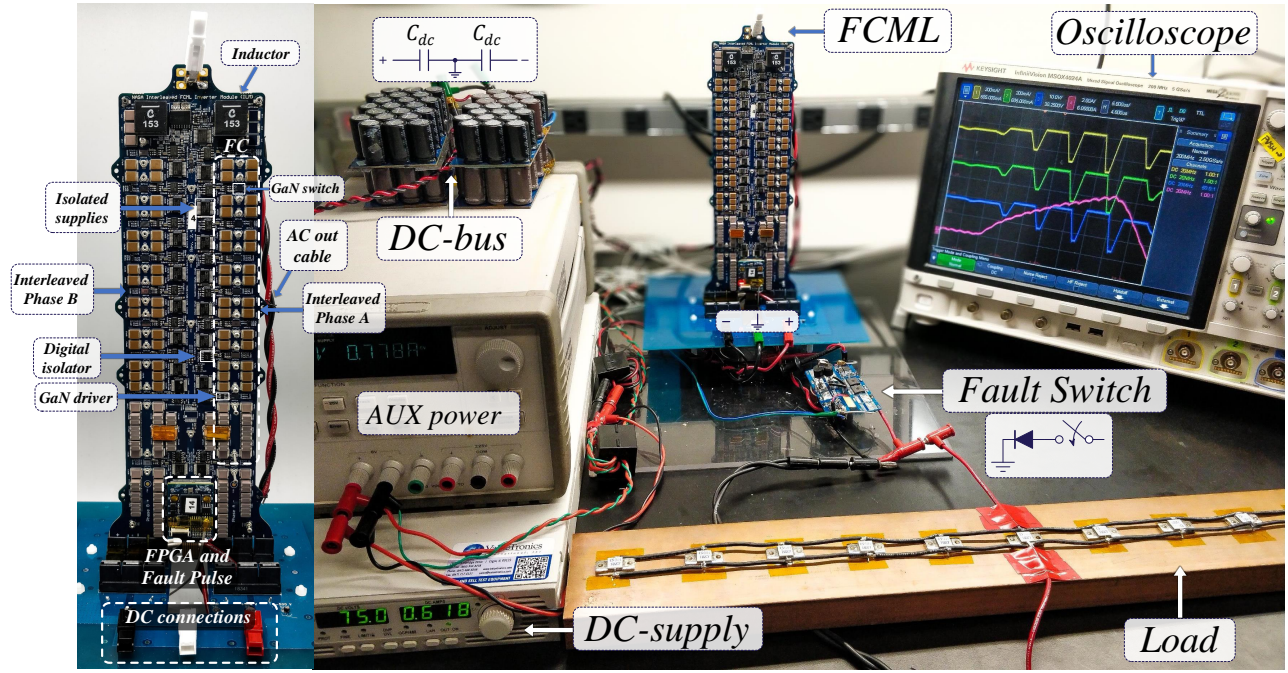
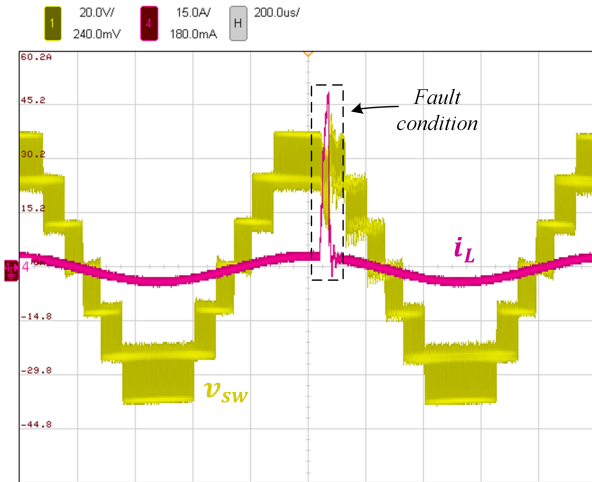Fig. 11. Experimental setup for FCML converter short-circuit tests.

Fig. 12. View of fundamental frequency inductor current (i_L) and converter switch-node voltage (v_{sw}) where the fault condition of interest is highlighted for a 7-level FCML.

two modeling approaches. As expected, the exponential model is more accurate compared to the linear model, which becomes more conservative as time progresses. This is due to the fact that the linearity of the inductor current is only valid in the first few microseconds of the fault.

To validate the conservative model in (42), Fig. 14 shows the predicted and measured maximum switch voltages for different N-level converters. It is evident that the model matches well, especially in the initial part (up to 10-15 μs) of the fault, since this is the linear range of the inductor current. After this point, the linear prediction serves as a conservative estimate of the maximum switch voltage. It is also noticed that in the very early part of the short-circuit fault, the overvoltage during turn-

on of the top-side switches actually goes above the prediction. This is due to ringing effects and switch voltage overshoots, which are not captured in the model.

Due to the non-ideal unmodeled frequency dependency of the dc-link in Fig. 11, the internal inductance and ESR will oppose the release of stored energy when the short-circuit fault occurs. From the ac-side point of view, this looks equivalent to an increased output inductance or decreased dc-link capacitance. The effect of the dc-link rapidly discharging during a short-circuit fault due to its frequency-dependent nature is shown in Fig. 15. The top dc-link capacitor experiences a large discharge during the fault, which is directly reflected to the output voltage. This effect explains why the error associated with the exponential and linear models for predicting the inductor current as shown in Table IV increases with an increasing inductor current. Even with the mismatch in the measured input capacitor behavior to the model, the linear approximation serves as a good and simple representation of the switch voltage stress experienced.

Apart from the simplified models, the detailed model developed in Section 2 is compared with the experimental results. Fig. 16 shows that the detailed model is fully capable of describing the behavior of the experimental system by adjustment of the dc-link capacitance to take into account the observed discharge.

B. Comparison to Other Designs and Recommendations

Having validated the detailed and simplified models, a comparison to two other designs is performed. These include a 5-level FCML with a switching frequency of 60 kHz [29] and a 9-level FCML with a switching frequency of 120 kHz [9]. Both designs have an input voltage of 1000 V. Using the detailed developed model and the parameters of operation for
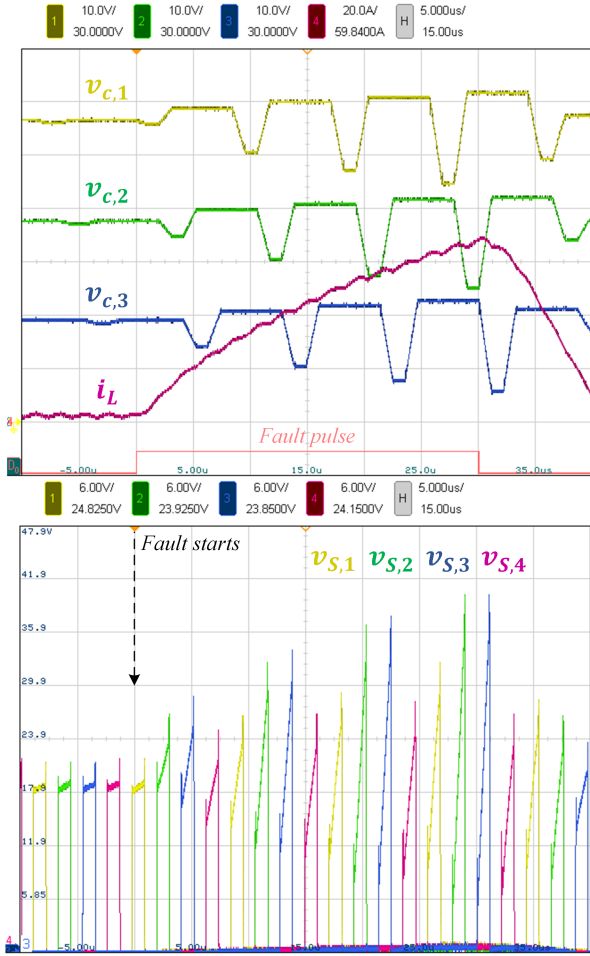
Fig. 13. Zoomed view of fault condition for $N = 5$ and $D = 0.85$. The top scope plot contains the three flying capacitor voltages and the inductor current, whereas the bottom scope plot contains the four top-side switch voltages. The fault pulse has a duration of $30\,\mu s$.

Consequently, for the 9-level converter, the maximum switch current will be violated first, whereas for the 5-level design, the maximum switch voltage will be exceeded first. This indicates that whether overvoltage or overcurrent will be an issue for the FCML, is related to the design and selection of the passive components in the system. E.g., for a converter with a high number of levels and a high switching frequency, both the output inductance and the capacitance of the flying capacitors can be made small which increases the risk of rapid device failure during short-circuit conditions. Lastly, as can be seen for both designs, the maximum values are exceeded well within the first switching period. Accordingly, this indicates that for such conditions, the detection and protection of the fault have to occur at a frequency much higher than the operating switching frequency.

V. CONCLUSION

With the goal of achieving highly efficient power converters with a high power density, the FCML is increasingly utilized for such applications. Even though the steady-state operation and balancing principles of these converter has been thoroughly investigated, its performance towards short-circuit conditions remains unclear. This work has presented a comprehensive generalized model of an N-level FCML subject to a severe ac-side short-circuit fault. Based on this, simplified models describing the switch stress in terms of voltage and current are presented, which can be used to predict the time where the converter operates within safe conditions. A fully-configurable 2-10 level FCML with a designed fault branch circuit is built to test and verify the models. These are also compared to other existing designs of FCMLs, showing a great ability of the simplified models to predict the behavior of the FCML during a short-circuit fault. The presented models and disclosed trends of the FCML serve to be used in the initial FCML design and in the selection of proper short-circuit detection and mitigation hardware/software.

these two designs, the time from short-circuit fault until either the maximum switch voltage or switch current is exceeded is calculated. The maximum switch voltage is considered twice the nominal operating condition, whereas the maximum switch current is set to ten times the peak current at nominal power. As can be seen from the results in Table V, the linear model prediction of the inductor current (28) and switch voltages (43) match well with the results of the detailed model since the violation in the switch current and voltage occurs in the linear range of the inductor current. It is noticeable that for a high N, the inductance can be made very small due to the high effective output frequency. This small inductance leads to a higher power density, but during short-circuit conditions, the opposition to change in current is extremely limited.
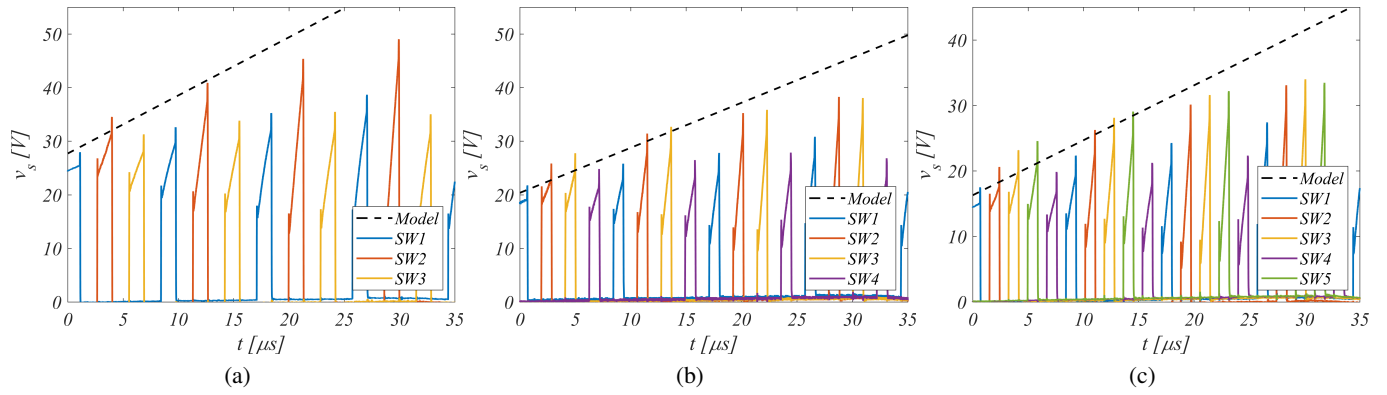
Fig. 14. Comparison of experimental measured switch voltages and the maximum modeled switch voltage from (42) for (a): $N = 4$ and $D = 0.85$, (b): $N = 5$ and $D = 0.9$, and (c): $N = 6$ and $D = 0.9$.
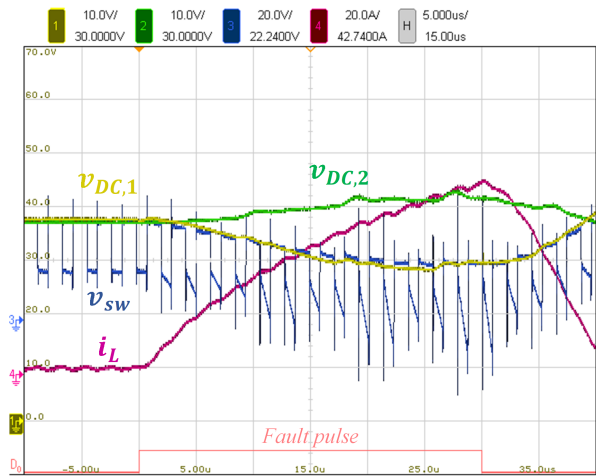

Fig. 15. Short-circuit fault where FCML switch-node output voltage, inductor current, and dc-link voltages are recorded. It is evident that the positive dc-link capacitor experiences a heavy discharge which reduces the output voltage.
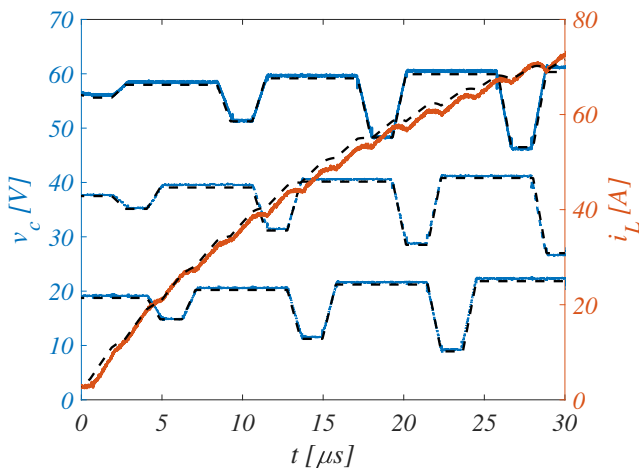

Fig. 16. Comparison of detailed FCML model during short-circuit conditions and the experimental results for $N = 5$ and $D = 0.9$. Dashed lines are the modeled results and solid lines are the experimental results. The effective modeled dc-link capacitance is reduced to $100\,\mu F$.

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