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# SIDO coupled inductor-based high voltage conversion ratio DC–DC converter with three operations

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**Abstract**

Here, a single-input, dual output (SIDO) coupled inductor-based high voltage conversion ratio DC–DC converter is proposed. The proposed converter has the capability of operating as a SIDO converter in a way that the terminal of the input voltage source is exchangeable among the three ports. Therefore, there are three different operation modes for the proposed converter. The voltage conversion ratios of the high voltage ports over the low voltage port can be improved by increasing the turn ratio of the coupled inductors. The main advantage of the proposed converter is achieving high voltage gains with lower number of components for the whole range of duty cycles comparing to the conventional multi-port high voltage gain converters. Moreover, two output voltages of the proposed converter can be simultaneously regulated on different constant levels with a good precision. In this study, the voltage conversion ratios, the inductors' average currents, the voltage and current stress on the switches are calculated theoretically. Finally, an experimental prototype of 30 V input and 410, 260 V outputs with the power 510 W is implemented and the results are verifying the theoretical ones.

## 1 | INTRODUCTION

In recent years, the multi-port converters have been more interested for using in renewable energy systems such as photovoltaics (PV), fuel cells (FC), and also electric vehicles (EV) [1–3]. In the renewable energy systems, it is important to interface different levels of input and output DC voltages. As a result, dual-input, single-output (DISO) converters in [4–7] and single-input, dual-output (SIDO) converters in [8–11, 13–20] and single-input, three-output converter in [12] are presented. Multi-input converters are needed to be used in hybrid energy sources [4–7]. Multi-output converters can be used in off-grid solar home systems and should be able to supply the different electrical consumers with different levels of voltages and powers [12, 14]. Moreover, in the grid connected renewable energy sources, by using a series connected DC–AC inverter to the DC output voltage of DC–DC converter, the AC Bus 220 or 400 V with frequency of 50–60 Hz should be available for delivering power to the grid. On the other hand, considering that the extracted voltages from the renewable energy sources are at low levels, it should be better to increase the output voltage by using high voltage gain DC–DC converters [8, 12–16]. The presented multiport converters in [9–11, 17,18] have low voltage gains and almost equal to the conventional boost or buck converters.

In order to increase the voltage gains in the multi-port converters, there are several approaches. In some converters, by using diode-capacitor cells, the output voltage is extended [8, 12]. In some cases, high voltage conversion ratio is achieved by applying coupled inductors, then the output voltages can be more extended by increasing the turns ratio of the coupled inductors [14–16]. In the case of multi-port DC–DC converters, similar to other DC–DC converters, having the low voltage stress on the semiconductor components leads to have low losses [8, 9, 12–16]. In the multi-output converters, the critical issue is to achieve the suitable precision of the output voltage regulations for all the output ports simultaneously under the variations of the input voltage level or output load. In the interleaved multi-port high voltage gain converters, there are at

least two operating regions based on the duty cycle range. Then, these converters have complicated voltage controlling schemes [4, 6-11]. In [12], three high voltage gains are obtained using the switched-capacitor modules. In this converter, the voltages of the three output terminals cannot be regulated simultaneously. Similarly, the presented converters in [8, 14, 20] cannot be easily controlled, because these converters have just one controlling parameter of the duty cycle, where they have two voltage functions, which should be controlled. The presented SIDO converter in [20] has the capability of operating in a way that the terminal of the input voltage source is exchangeable between each of three ports. This converter suffers from low voltage gains, which is like the conventional boost and buck converters. Among the multi-port converters, some converters have boost and buck operations [21–24], buck and buck-boost operations [25], boost, buck-boost and buck operations [26, 27]. The presented converter in [27] has the reduced number of components but both of the input sources are not able to operate and transfer power at the same time.

In this paper, a new coupled inductor-based single-input, dual output (SIDO) DC–DC converter is presented with the following merits; (i) the proposed converter has high voltage conversion ratio, (ii) the proposed converter has the capability of operating as a SIDO converter in a way that the terminal of the input voltage source is exchangeable among the three ports. This ability has made the converter suitable for versatile applications, (iii) there are three different operation modes for the proposed converter including boost, buck and buck and boost operations that have been explained in details separately, (iv) the voltage conversion ratios of the ports can be improved by increasing the turns ratio of the coupled inductors. As a result, the applied duty cycles to the active switches are not high, even if there is a high voltage gains needed at the load side, (v) comparing to the conventional SIDO converters, the proposed converter can provide high voltage gains with smaller number of components, (vi) the proposed converter has a good dynamic response towards the fluctuations of loads or the input voltage. In this paper, the proposed converter is analysed theoretically. Finally, the obtained analytical results, are reconfirmed by using the experimental results.

## 2 | OPERATING PRINCIPLES OF THE PROPOSED CONVERTER

The proposed converter is shown in Figure 1. Considering that the proposed converter has the three DC-ports, three SIDO operations exist for the proposed converter which can be modelled as Figure 2.

The operations of the proposed converter are categorized in Figure 2(a) and the power circuit of the proposed SIDO converter with the three operation modes are shown in Figure 2(b–d).

Considering Figure 2(b–d), in the proposed converter, each of the three DC ports can be selected as the input voltage source and other two ports can be considered as output ports. In the proposed converter, the voltage $V_l$ is lowest DC voltage and the

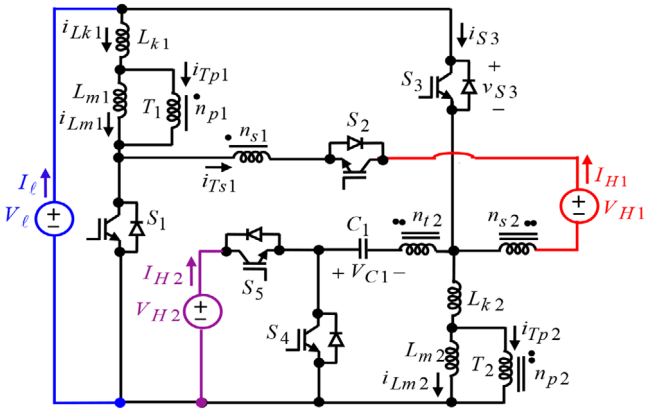


**FIGURE 1** The power circuit of the proposed SIDO converter

voltages $V_{H1}$, $V_{H2}$, are higher voltages $V_l < V_{H2} < V_{H1}$. In the first operation of the proposed converter, the input voltage source is equal to $V_l$ and two output loads are $R_{H1}$ and $R_{H2}$ as shown in 2(b). Considering that the voltages $V_{H1}$ and $V_{H2}$ are higher than the input voltage ($V_l$), therefore, this operation can be defined as stepped-up operation. In the second operation of the proposed converter, the input voltage source is $V_{H1}$ and two output loads are $R_{H2}$ and $R_\ell$ as shown in Figure 2(c).

In this operation mode, the voltages $V_{H2}$ and $V_\ell$ are lower than the input voltage source ($V_{H1}$), therefore, it can be defined as stepped-down operation. The proposed converter in the third operation has the input voltage source equal to $V_{H2}$ and two output loads of and $R_\ell$ as shown in Figure 2(d). Considering that one lower voltage ($V_\ell$) and $R_{H1}$ one higher voltage ($V_{H1}$) than input voltage source ($V_{H1}$) is obtained at the output ports, as a result, this operation is defined as stepped-up and stepped-down operation.

Based on Figure 1, the power circuit of the proposed converter includes switches $S_1$, $S_2$, $S_3$, $S_4$, $S_5$, and capacitor $C_1$. Moreover, it has the first coupling inductor with two-winding transformer of $T_1$, magnetizing inductance of $L_{m1}$, leakage inductance of $L_{k1}$ and second coupling inductor with three-winding transformer of $T_2$, the magnetizing inductance of $L_{m2}$ and leakage inductance of $L_{k2}$. The first and second windings of the transformer $T_1$ have $n_{p1}$ and $n_{s1}$ turns, respectively. As a result, the turn ratio of the transformer $T_1$ is considered as $n_1 = n_{s1}/n_{p1}$. In the same way, the turns ratio of second transformer is considered as $n_2 = n_{s2}/n_{p2} = n_{t2}/n_{p2}$. The capacitor $C_1$ is assumed to be large enough, so, the voltage across capacitor $C_1$ would be constant as $V_{C1}$.

The switching pattern of switches and theoretical voltages' and currents' waveforms of the proposed converter in three operation modes are shown in Figure 3.

The voltages across the components in the three operations are same as each other. Therefore, in Figure 3(b,c) the waveforms of voltages are not shown to avoid showing repetitive waveforms. Considering Figure 3(a–c), it can be seen that only the direction of magnetizing inductors currents is changed in three operations.

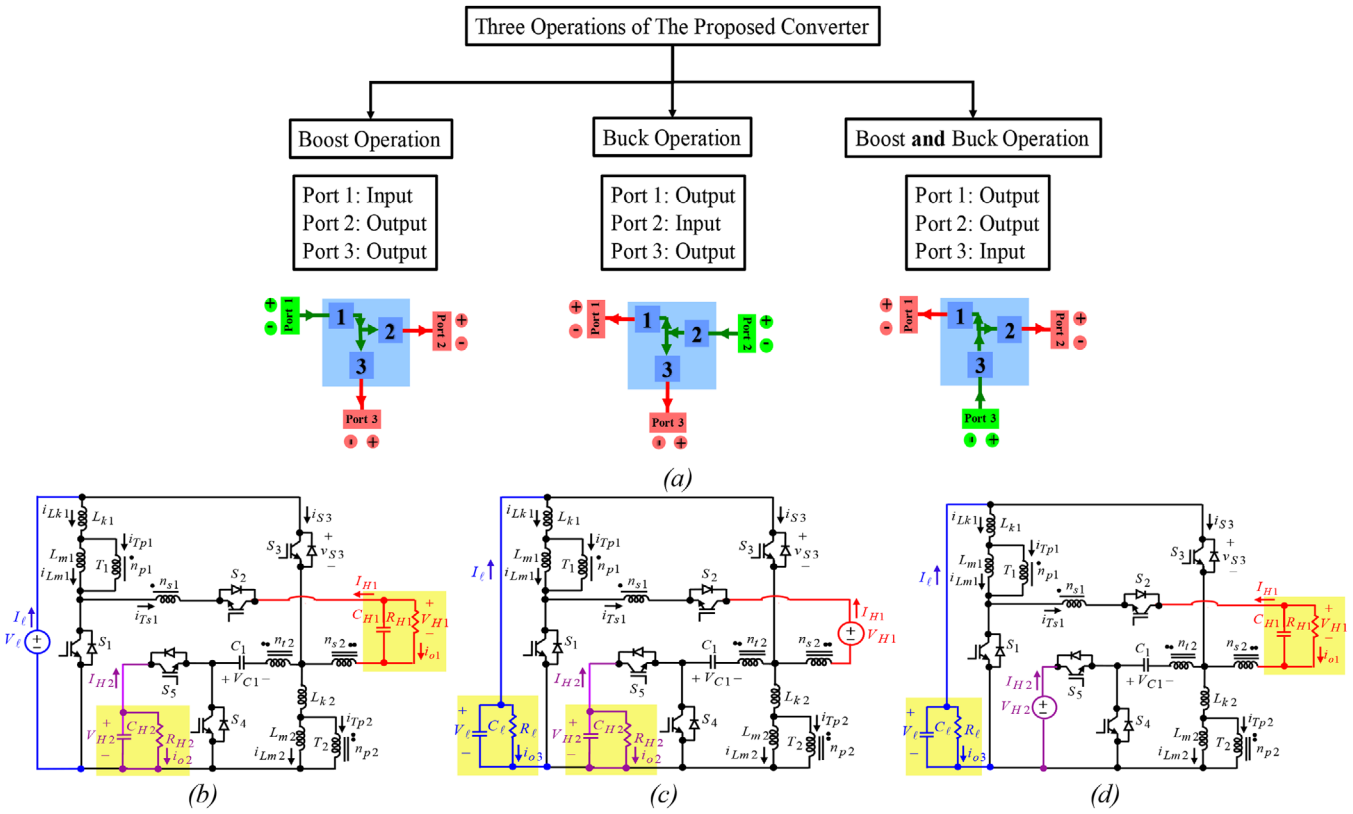


**FIGURE 2** The operations of the proposed converter; (a) flowchart; (b) boost operation; (c) buck operation; (d) boost-and-buck operation

As an example, for the practical application of the experimental prototype of the converter, the input voltage source can be selected as a 30 V FC and the higher output voltages are $V_{H1} = 418.5$ V and $V_{H2} = 262.5$ V. The output voltages can be applied to DC/AC inverters (such as; LS Starvert iS7-750W 400V) to provide 220 V-AC at frequency of 50/60 Hz to supply the grid or off-grid consumers. Furthermore, the experimental prototype of the proposed converter can be utilized for some applications of an electric vehicle or in Green houses.

## 3 | ANALYSIS OF THE PROPOSED CONVERTER DURING A SWITCHING PERIOD

Based on Figure 3(a–c), the conducting interval time for the switch $S_1$ is equal to $D_1 T_s$ and the switch $S_2$ is ON when the switch $S_1$ is OFF. The duty cycle of switches $S_3$, $S_5$ is equal to $D_2$ and the switch $S_4$ is conducting when the switches $S_3$, $S_5$ are OFF. In the analysis of the proposed converter, it is assumed that $D_1 \geq D_2$. Based on Figure 3, the currents of the inductances $L_{m1}$ and $L_{m2}$ have the maximum values ($I_{b1}$ and $I_{b2}$) at $t_2$ and $t_1$ instants, respectively and minimum values ($I_{l1}$ and $I_{l2}$), at $t_0$. Based on Figure 3, the proposed converter has three Modes during a switching period where the equivalent circuits are shown in Figure 4.

Mode 1 [$t_0 \leq t \leq t_1$]: The equivalent power circuit of this Mode is shown in Figure 4(a). During this Mode, the switches, $S_1$, $S_3$ and $S_5$ are conducting, while the switches $S_2$ and $S_4$ are OFF. Therefore, it should be written as $v_{\mathrm{Im1}} = v_{Lk1} = V_\ell$. Considering $i_{Lm1} = I_{Lk1}$, the voltage $v_{Lm1}$ is obtained as $v_{Lm1} = V_\ell/(1 + L_{k1}/L_{m1})$. Moreover, the voltage $v_{Lm2}$ is calculated as $v_{Lm2} = (V_{H2} - V_{C1} - V_\ell)/n_{s2}$. Therefore, the currents of the magnetizing inductances are written as:

$$i_{Lm1} = \left[V_\ell / (1 + L_{k1}/L_{m1})\right](t - t_0)/L_{m1} + I_{l1} \quad (1)$$

$$i_{Lm2} = \left[(V_{H2} - V_{C1} - V_\ell)/n_{s2}\right](t - t_2)/L_{m2} + I_{l2} \quad (2)$$

$S_2$ Mode 2 [$t_1 \leq t \leq t_2$]: Figure 4(b) shows the equivalent power circuit of this Mode. In this Mode, the switches, $S_1$ and $S_4$ are conducting, while the switches $S_2$, $S_3$ and $S_5$ are OFF. Consequently, the voltage $v_{Lm2}$ is calculated as $v_{Lm2} = -V_{C1}/(1 + n_{s2} + k_2)$. Therefore, the current $i_{Lm2}$ should be as follows:

$$i_{Lm2} = -\left[V_{C1} / (1 + n_{s2} + k_2)/L_{m2}\right](t - t_1) + I_{b2} \quad (3)$$

where, $k_2 = L_{k2}/[L_{m2}(1 + n_{s2})]$. The inductor current $i_{Lm1}$ is obtained from Equation (1).

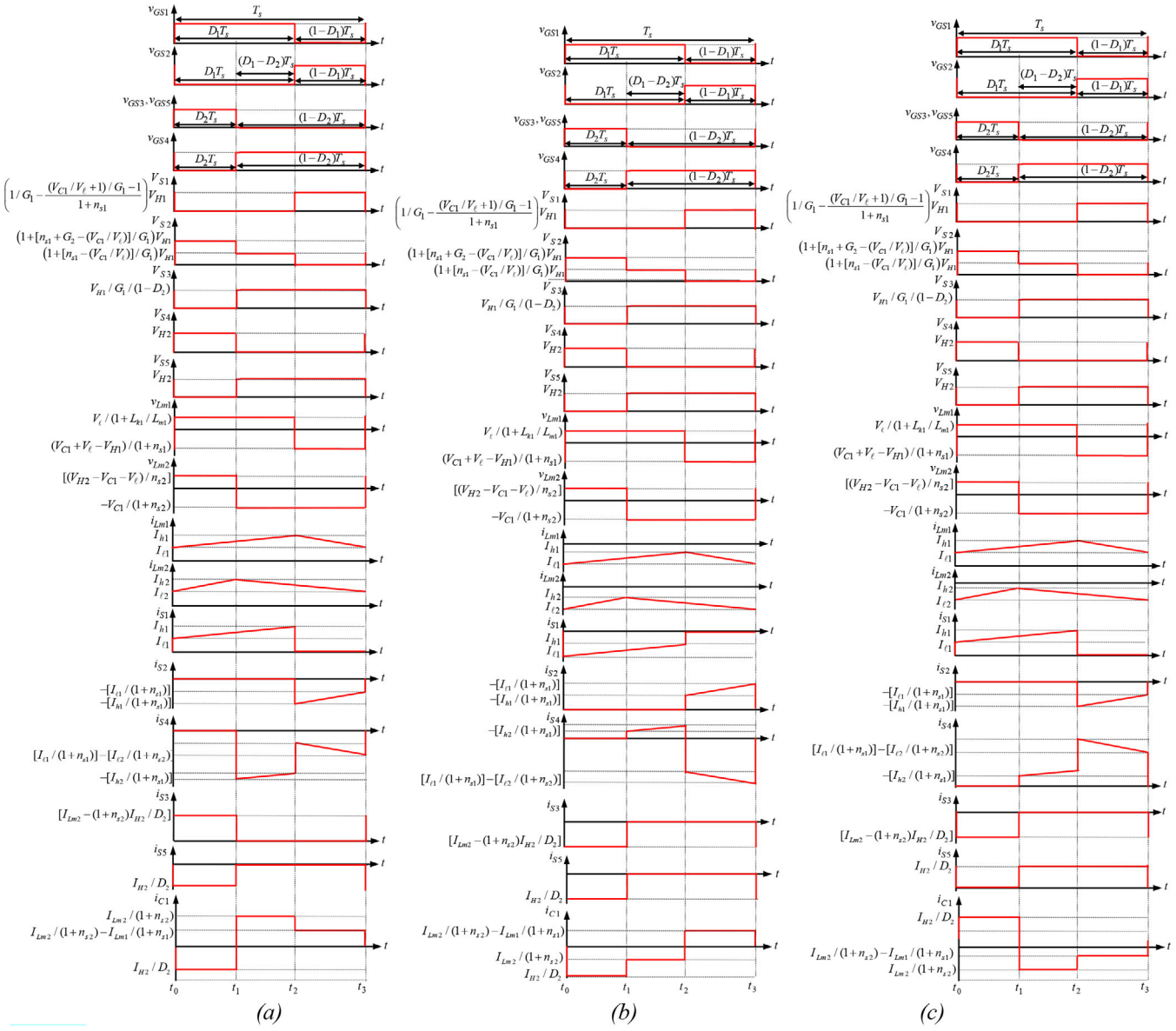


**FIGURE 3** Switching pattern of switches and theoretical waveforms of proposed converter in three operation modes; (a) first operation; (b) second operation; (c) third operation.

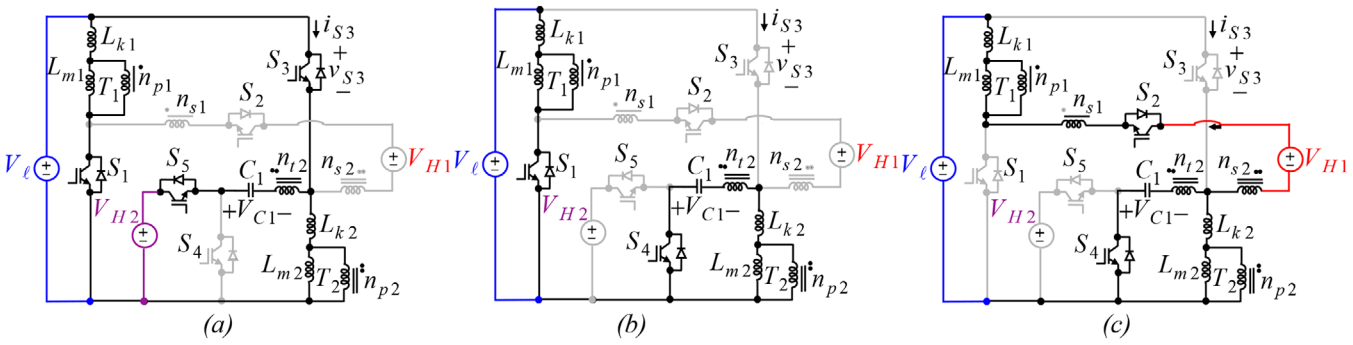


**FIGURE 4** Equivalent circuit of the proposed converter during different modes in a switching period; (a) Mode 1; (b) Mode 2; (c) Mode 3.

Mode 3 [$t_2 \le t < t_3$]: Figure 4(c) shows the equivalent power circuit of this Mode. During this Mode, $S_2$ and $S_4$ are conducting, while the switches $S_1$, $S_3$ and $S_5$ are OFF. Based on Figure 4(c), it can be concluded that $i_{Lk1} = i_{Lm1}/(1 + n_{s1})$. Accordingly, the voltage $v_{Lm1}$ is calculated as $(V_{C1} + V_\ell - V_{H1})/(1 + n_{s1} + k_1)$. As a result, the current $i_{Lm1}$ is calculated as follows:

$$i_{Lm1} = [(V_{C1} + V_\ell - V_{H1})/(1 + n_{s1} + k_1)/L_{m1}](t - t_2) + I_{b1} \quad (4)$$

where, $k_1 = L_{k1}/[L_{m1}(1 + n_{s1})]$. The voltage $v_{Lm2}$ and current $i_{Lm2}$ is calculated with the same equations as in Mode 2.

## 4 | VOLTAGE GAIN AND VOLTAGE ON CAPACITOR

By considering the average voltage balance law of the inductors in steady state, the average voltages of $v_{Lm1}$, $v_{Lm2}$, $v_{Lk1}$ and $v_{Lk2}$ during single switching period should be equal to zero. Therefore, the Equations (5)–(7) are as follows:

$$\tilde{v}_{Lm1} = \frac{D_1 V_\ell}{1 + L_{k1}/L_{m1}} + (1 - D_1)\frac{V_{C1} + V_\ell - V_{H1}}{1 + n_{s1} + k_1} = 0 \quad (5)$$

$$\tilde{v}_{Lm2} = D_2\frac{V_{H2} - V_{C1} - V_\ell}{n_{s2}} + \frac{(1 - D_2)(-V_{C1})}{1 + n_{s2} + k_2} = 0 \quad (6)$$

$$\tilde{v}_{Lm2} + \tilde{v}_{Lk2} = D_2 V_\ell - \frac{(1 - D_2)(1 + k_2) V_{C1}}{1 + n_{s2} + k_2} = 0 \quad (7)$$

By considering Equation (7), $V_{C1}/V_\ell$ can be calculated as follows:

$$V_{C1}/V_\ell = (1 + n_{s2} + k_2) D_2/[(1 + k_2)(1 - D_2)] \quad (8)$$

As a result, the voltage conversion ratio of s is calculated as follows:

$$G_1 = \frac{V_{H1}}{V_\ell} = 1 + \frac{D_1}{1 - D_1}\frac{1 + n_{s1} + k_1}{1 + L_{k1}/L_{m1}} + \frac{D_2}{1 - D_2}\frac{1 + n_{s2} + k_2}{1 + k_2} \quad (9)$$

Based on Equations (6) and (7), the voltage conversion ratio of $G_2$ is calculated as follows:

$$G_2 = \frac{V_{H2}}{V_\ell} = \frac{1 + n_{s2} + k_2}{(1 - D_2)(1 + k_2)} = \frac{V_{C1}}{D_2 V_\ell} \quad (10)$$

By neglecting the leakage inductances of the coupled inductors, the voltage conversion ratio equations can be simplified as $G_2 = (1 + n_{s2})/(1 - D_2)$ and $G_1 = 1 + [D_1/(1 - D_1)](1 + n_{s1}) + [D_2/(1 - D_2)](1 + n_{s2})$.

In Figure 5(a,b), radar chart and 3D plot of the voltage conversion ratio of Port 2 with the calculated voltage gain of $G_1$ considering the number of turn ratio of the coupled inductors along with the duty cycle of the switches is shown to demonstrate the effects of these parameters on the voltage gain of the Port 2. From Figure 5(b), it can be seen that the Port 2 of the proposed converter has the largest operational area (shown in blue) for providing conversion ratios up to 20 times larger than the input voltage. In the same way, Figure 5(c,d) show the voltage conversion ratio of Port 3 which is calculated as $G_2$ considering the number of turn ratio of the coupled inductors with the duty cycle of the switches. From Figure 5(d), Port 3 of the proposed converter has the large operational areas (shown in blue and dark pink) for providing conversion ratios up to 10 times (blue area) and from 10 to 20 times (dark pink) larger voltages than the input voltage.

In Figure 5, the number of turn ratio of the coupled inductors are considered the same values as $n_{s1} = n_{s2} = n_s$ and is considered variable as $n_s = 1, 2, 3, 4, 5, 6, 7, 8, 9$. Considering Equations (9)–(10), for an example in first operation mode, by using controlling parameter of duty cycle $D_1$, the output voltage $V_{H1}$ can be regulated. Moreover, by using the controlling parameter of duty cycle $D_2$, the output voltage of $V_{H2}$ is regulated.

As a result, the output voltages $V_{H1}$ and $V_{H2}$ can be easily regulated at each preselected value. For controlling output voltages PI-controller is used. As shown in Figure 6, the switching controlling pulses of the output voltages would be produced.

## 5 | VOLTAGE STRESS ON SWITCHES

Considering Figure 4(c), the voltage stress on switch $S_1$ during Mode 3 [$(1 - D_1)T_s$] is obtained as follows:

$$V_{S1} = \left[1 + \frac{(1 + k_{1a})[G_1 - G_2 D_2 - 1]}{1 + n_{s1} + k_{1a}}\right]\frac{V_{H1}}{G_1} \; : \; During(1 - D_1)T_s \quad (11)$$

Moreover, the switch $S_2$ is turned off during Modes 1 ($D_2 T_s$) and 2 [$(D_1 - D_2)\, T_s$]. Therefore, the voltage stress on the switch $S_2$ during Modes 1 and 2 is calculated as follows:

$$V_{S2} = \left[1 + \left(G_2 + \frac{n_{s1}}{k_{2a}} - G_2 D_2\right)\frac{1}{G_1}\right] V_{H1} \; : \; During\, D_2 T_s \quad (12)$$

$$V_{S2} = \left[1 + \left(\frac{n_{s1}}{k_{1a}} - G_2 D_2\right)\frac{1}{G_1}\right] V_{H1} \; : \; During\,[(D_1 - D_2)T_s] \quad (13)$$

where, $k_{1a} = 1 + (L_{k1}/L_{m1})$ and $k_{2a} = 1 + (L_{k2}/L_{m2})$.

The switch $S_3$ is turned off during Modes 2 and 3 [$(1 - D_2)T_s$]. Therefore, Considering Figsure 4(b,c), the voltage stress on switch $S_3$ during Modes 2 and 3 [$(1 - D_2)T_s$] is written as follows:

$$V_{S3} = V_{H1}/[(1 - D_2)\, G_1] \; : During\,[(1 - D_2)T_s] \quad (14)$$

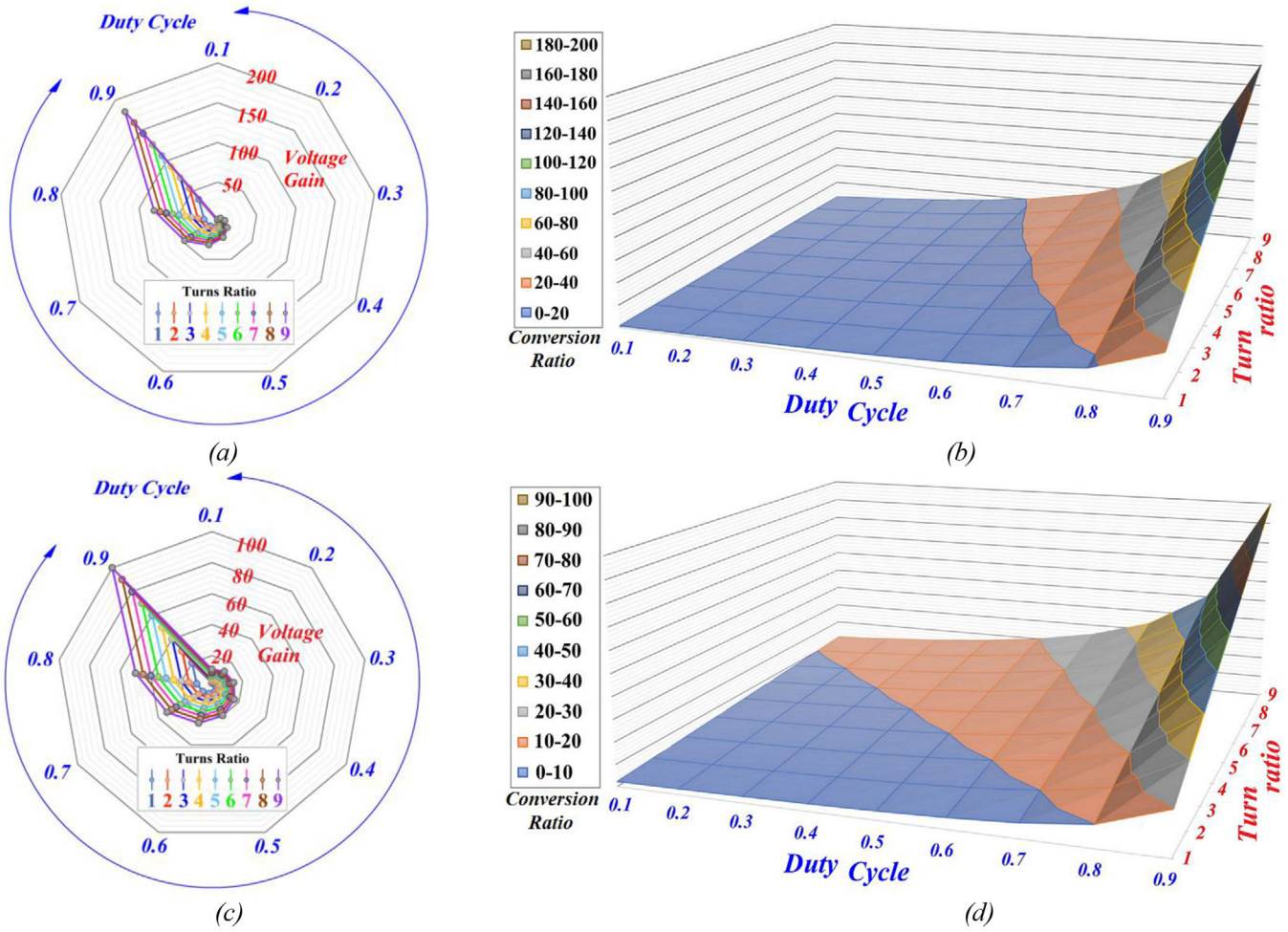


**FIGURE 5** The voltage conversion ratios of the Ports 2 and 3 of the proposed converter ($G_1$, $G_2$) over the number of turn ratio of coupled inductors and duty cycle; (a) Radar chart for $G_1$; (b) 3D plot for $G_1$; (c) Radar chart for $G_2$; (d) 3D plot for $G_2$

The voltage stresses on switch $S_4$ during Mode 1 [$(D_2 T_s)$] and switch $S_5$ during Modes 2 and 3, are obtained as follows:

$$V_{S4} = V_{H2} \quad : During\, D_2 T_s \tag{15}$$

$$V_{S5} = V_{H2} \quad : During\, (1 - D_2)\, T_s \tag{16}$$

## 6 | AVERAGE CURRENTS OF SWITCHES, INDUCTORS AND THE OUTPUT CURRENTS

Referring to Figure 1, the average currents passing through the switches $S_1$, $S_2$, $S_3$, $S_4$ and $S_5$ during a switching period in steady state are calculated as follows:

$$I_{S1} = I_{Lm1} + (1 + n_{s1}) I_{H1} = D_1 I_{Lm1} \tag{17}$$

$$I_{S2} = -(1 - D_1)[I_{Lm1}/(1 + n_{s1})] = I_{H1} \tag{18}$$

$$I_{S3} = I_{Lm2} + (1 + n_{s2}) I_{H1} = [I_{Lm2} - (1 + n_{s2}) I_{H2}/D_2] D_2 \tag{19}$$

$$I_{S4} = I_{S5} = I_{H2} \tag{20}$$

As a result, in the boost operating mode, the normalized current stress on switches based on the input current in the boost operating mode is calculated as follows:

$$I_{S1,n} = \frac{D_1 I_{Lm1}}{I_i} = \frac{D_1 (1 + n_{s1})(P_{o1}/V_{o1})/(1 - D_1)}{G_1 (P_{o1}/V_{o1}) + G_2 (P_{o2}/V_{o2})}$$
$$\frac{D_1 (1 + n_{s1})(P_{o1}/G_1 V_i)/(1 - D_1)}{G_1 (P_{o1}/G_1 V_i) + G_2 (P_{o2}/G_2 V_i)} = \frac{D_1 (1 + n_{s1})/(1 - D_1)}{2G_1} \tag{21}$$

$$I_{S2,n} = -I_{o1}/I_i = 1/(2G_1) \tag{22}$$

$$I_{S3,n} = \frac{1 + n_{s2}}{1 - D_2} \left( \frac{D_2}{2G_1} + \frac{1}{2G_2} \right) \tag{23}$$

$$I_{S4,n} = I_{S5,n} = -I_{o2}/I_i = 1/(2G_2) \tag{24}$$

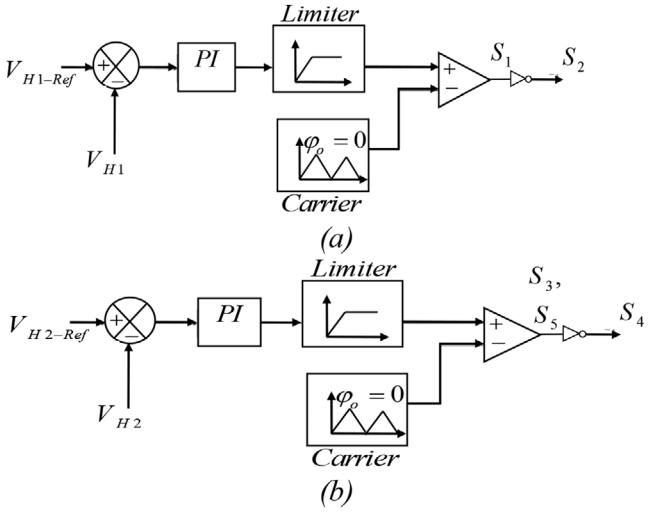


**FIGURE 6** Controlling block diagram of the output voltages of the proposed converter by using the switches; (a) controlling block of the output voltage $V_{o1}$; (b) controlling block of the output voltage $V_{o2}$

To calculate the normalized switches currents based on the input current $I_i = (G_1 I_{o1} + G_2 I_{o2})$ in the above equations, the output powers of the converter $P_{o1}$ and $P_{o2}$ are considered equal to each other ($P_{o1} = P_{o2}$).

Accordingly, the RMS value of switches currents are calculated as follows:

$$I_{S1-RMS,n} = \sqrt{\frac{1}{T_s}\int_0^{D_1 T_s} (I_{S1,n})^2 dt} = I_{S1,n}\sqrt{D_1} = \frac{D_1(1+n_{s1})/(1-D_1)}{2G_1}\sqrt{D_1} \tag{25}$$

$$I_{S2-RMS,n} = I_{S2,n}\sqrt{1-D_1} = \sqrt{1-D_1}/(2G_1) \tag{26}$$

$$I_{S3-RMS,n} = \frac{1+n_{s2}}{1-D_2}\left(\frac{D_2}{2G_1} + \frac{1}{2G_2}\right)\sqrt{D_2} \tag{27}$$

$$I_{S4-RMS,n} = I_{S4,n}\sqrt{1-D_2} = 1/(2G_2)\sqrt{1-D_2} \tag{28}$$

$$I_{S5-RMS,n} = I_{S5,n}\sqrt{D_2} = 1/(2G_2)\sqrt{D_2} \tag{29}$$

Therefore, the average magnetizing inductance current of $i_{Lm1}$ is calculated as follows:

$$I_{Lm1} = (1+n_{s1})(-I_{H1})/(1-D_1) \tag{30}$$

By considering the current balance law for the capacitor $C_1$, the following equation can be written.

$$\tilde{i}_{C1} = D_2(I_{H2}/D_2) + (D_1 - D_2)I_{Lm2}/(1+n_{S2}) + (1-D_1)[I_{Lm2}/(1+n_{S2}) - I_{Lm1}/(1+n_{S1})] = 0 \tag{31}$$

Accordingly, the average value of the inductor current of $i_{Lm2}$ is calculated as follows:

$$I_{Lm2} = -(1+n_{S2})(I_{H1} + I_{H2})/(1-D_2) \tag{32}$$

According to the power balance law in the proposed converter, $I_\ell$ at the low voltage side would be obtained as;

$$I_\ell = -(G_1 I_{H1} + G_2 I_{H2}) \tag{33}$$

The average currents of DC voltages $I_{H1}$, $I_{H2}$, $I_\ell$ in the above equations are obtained based on the operation type.

In the first operation, based on Figure 2(b), the output currents $I_{o1}$ and $I_{o2}$ are equal to $I_{o1} = -I_{H1} = V_{H1}/R_{H1}$ and $I_{o2} = -I_{H2} = V_{H2}/R_{H2}$, respectively. The output powers should be written as $P_{H1} = {V_{H1}}^2/R_{H1}$, $P_{H2} = {V_{H2}}^2/R_{H2}$. The total output power ($P_{oT}$) is equal to $P_{oT} = P_{H1} + P_{H2}$.

In the second operation, based on Figure 2(c), the output currents $I_{o3}$ and $I_{o2}$ are equal to $I_{o3} = -I_\ell = V_\ell/R_\ell$ and $I_{o2} = -I_{H2} = V_{H2}/R_{H2}$, respectively. The output powers would be obtained as $P_\ell = {V_\ell}^2/R_\ell$, $P_{H2} = {V_{H2}}^2/R_{H2}$. The total output power ($P_{oT}$) is written as $P_{oT} = P_\ell + P_{H2}$.

In third operation, considering Figure 2(d), the output currents $I_{o3}$ and $I_{o1}$ are equal to $I_{o3} = -I_\ell = V_\ell/R_\ell$ and $I_{o1} = -I_{H1} = V_{H1}/R_{H1}$, respectively. The output powers would be obtained as $P_\ell = {V_\ell}^2/R_\ell$ and $P_{H1} = {V_{H1}}^2/R_{H1}$. The total output power ($P_{oT}$) is equal to $P_{oT} = P_\ell + P_{H1}$.

The currents' ripple of the magnetizing inductances are $\Delta i_{Lm1} = [V_\ell/(1 + L_{k1}/L_{m1})]D_1 T_s/L_{m1}$ and $\Delta i_{Lm2} = [(V_{H2} - V_{C1} - V_\ell)/n_{s2}]D_2 T_s/L_{m2}$. The maximum and minimum values of the inductor current $i_{Lm1}$ is calculated as $I_{h1} = I_{Lm1} + \Delta i_{Lm1}/2$, $I_{l1} = I_{Lm1} - \Delta i_{Lm1}/2$, respectively. The maximum and minimum values of the inductor current $i_{Lm2}$ is written as $I_{h2} = I_{Lm2} + \Delta i_{Lm2}/2$ and $I_{l2} = I_{Lm2} - \Delta i_{Lm2}/2$, respectively.

## 7 | DESIGN CONSIDERATIONS

In order to achieve continuous conduction mode (CCM) operation of the proposed converter, the average value of the currents passing through the inductances $L_{m1}$ and $L_{m2}$ has to be higher than the half of their current ripples. As a result, the following inequalities has to be verified.

$$L_{m1} > [(1-D_1)D_1 V_\ell]/[2(1+n_{S1})(-I_{H1})f_s] \tag{34}$$

$$L_{m2} > \frac{(V_{H2} - V_{C1} - V_\ell)D_2(1-D_2)}{-2n_{S2}(1+n_{S2})(I_{H2} + I_{H1})f_s} \tag{35}$$

Considering [12], to obtain the more accurate designing of capacitors, then, the peak-to-peak value of the total voltage ripple which is mostly considered as $\Delta V_{CT} = 0.01 V_C$ is equal to sum of the voltage ripple across each capacitor ($\Delta V_C$) and voltage ripple caused by the ESR of capacitor ($\Delta V_{C-ESR} = r_C \Delta I_C$). As a result, the minimum value of capacitors for the maximum

**TABLE 1** Minimum values of capacitors

| | |
|---|---|
| $C_{1\_min}$ | $C_{1\_min} = \frac{[I_{H2}/(D_2)]D_2T_s}{0.01\,V_{C1}-r_C[I_{Lm2}/(1+n_{S2})-I_{H2}/D_2]}$ |
| $C_{H1\_min}$ For boost and buck-boost operations | $C_{H1}\vert_{ESR} = \frac{I_{\ell 1}D_1T_s}{0.01V_{CH1}-r_C\frac{I_{Lm1}}{1+n_{S1}}} = \frac{D_1}{R_{H1}(0.01-\frac{r_C}{R_{H1}}\frac{1}{1-D_1})f_s}$, $C_{H1}\vert_{THT} = (V_{H1}/R_{H1})/[0.01V_{H1}(0.1f_s)] = 1/[0.01R_{H1}(0.1f_s)]$ $[C_{H1-\min} = \max(C_{H1}\vert_{ESR}, C_{H1}\vert_{THT})]$ |
| $C_{H2\_min}$ For boost and buck operations | $C_{H2}\vert_{ESR} = \frac{I_{\ell 2}(1-D_2)T_s}{0.01V_{CH2}-r_C\frac{I_{\ell 2}}{D_2}} = \frac{1-D_2}{R_{H2}(0.01-\frac{r_C}{R_{H2}}\frac{1}{D_2})f_s}$, $C_{H2}\vert_{THT} = 1/[0.01R_{H2}(0.1f_s)]$, $[C_{H2-\min} = \max(C_{H2}\vert_{ESR}, C_{H2}\vert_{THT})]$ |
| $C_{\ell\_min}$ For buck and buck-boost operations | $C_\ell\vert_{\min} = \frac{\{(1-D_2)I_{\ell 3}-I_{Lm1}[D_1-D_2+(1-D_1)/(1+n_{S1})]\}(1-D_2)T_s}{0.01V_{C\ell}-r_C(\frac{(1+n_{S2})I_{H2}}{D_2}-I_{Lm2})}$ $C_\ell\vert_{THT} = 1/[0.01R_\ell(0.1f_s)]$, $[C_{\ell-\min} = \max(C_\ell\vert_{ESR}, C_\ell\vert_{THT})]$ |

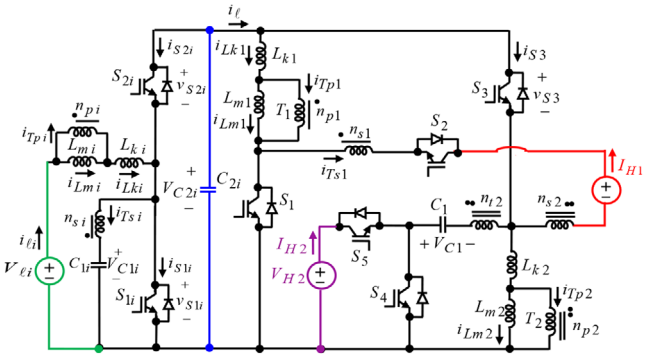


**FIGURE 7** Proposed ripple free single-input two-output converter

voltage ripple of them equal to $\Delta V_C = 0.01\,V_C - r_C\Delta I_C$ are calculated as given in Table 1. About the design of output capacitors, the hold-up time requirement for step-load response is also considered [12].

## 8 | DEVELOPED CONVERTER WITH INPUT CURRENT RIPPLE CANCELLATION

In this part, the developed converter is proposed to eliminate input current ripple of the main proposed converter thoroughly for all ranges of duty cycles considering the method used in [29]. In the developed converter, two extra switches of $S_{1i}$ and $S_{2i}$ which have the duty cycles of $D_0$and $1-D_0$, respectively. The duty cycle of $D_0$ can be selected as the values between zero and one $D_0(0 < D_0 < 1)$ regardless of the duty cycles $D_1$ and $D_2$. Also. It has used two extra capacitors of $C_{1i}$ and $C_{2i}$, respectively. These capacitors are assumed to be large enough, therefore, the voltages across them would be constant as $V_{C1i} = V_{\ell i}$, $V_{C2i} = V_\ell$, respectively. As shown in Figure 7 one coupled inductor with the inductance of $L_P$ for the primary winding, $L_S$ for the secondary winding and $M$ for the coupling inductance are used to eliminate the input current ripple. The analytical results of the proposed converter in Figure 7 are summarized as Table 2.

In this part, the required conditions of achieving zero input current ripple at the low voltage side ($i_\ell$) are obtained during a switching period. According to the Figure 1, the values of inductances $L_{p1}$, $L_{s1}$, $M_{ps1}$, can be replaced based on the used parameters in Figure 1(b) as follows:

$$L_{p1} = L_{m1} + L_{k1},\ L_{s1} = n_{S1}^2L_{m1},\ M_{ps1} = M_{sp1} = n_{s1}L_{m1} \tag{36}$$

The voltages across the windings of the first coupled inductor in Figure 1(a) can be written as follows:

$$v_{Lp1} = L_{p1}(di_{Lp1}/dt) + M_{ps1}(di_{Ls1}/dt) + M_{pf1}(di_{Lf1}/dt) \tag{37}$$

$$v_{Ls1} = M_{ps1}(di_{Lp1}/dt) + L_{s1}(di_{Ls1}/dt) + M_{sf1}(di_{Lf1}/dt) \tag{38}$$

Time Interval of $0 < t < D_0T_s$:

In the proposed developed converter in Figure 7, during mode 1 (switch $S_i$ is on), the following equation can be written:

$$L_P\frac{di_{LP}}{dt} + M\frac{di_{LS}}{dt} = M\frac{di_{LP}}{dt} + L_S\frac{di_{LS}}{dt} = V_i \tag{39}$$

As a result, the voltages $v_{Lp1}$ and $v_{Lf1}$ are equal to $V_\ell$.

Time Interval of $D_1T_s < t < T_s$: In this state, based on Figure 1(a), the switch $S_i$ is off, therefore, it would be written:

$$L_P\frac{di_{LP}}{dt} + M\frac{di_{LS}}{dt} = M\frac{di_{LP}}{dt} + L_S\frac{di_{LS}}{dt} = V_i - V_{Ci2} \tag{40}$$

It can be written that

$$\frac{di_{LP}}{dt} = \begin{cases} \frac{L_S-M}{L_SL_P-M^2}V_i & \text{mode1}\ \ (0 < t < DT_S) \\ \frac{L_S-M}{L_SL_P-M^2}(V_i - V_{Ci2}) & \text{mode2}\ \ (DT_S < t < T_S) \end{cases} \tag{41}$$

Considering Equation (38), the required condition to eliminate input current ripple is resulted as following:

$$L_S = M = K\sqrt{L_SL_P} \Rightarrow K = \sqrt{\frac{L_S}{L_P}} \tag{42}$$

As a result, the required conditions for achieving zero input current ripple at first stage is obtained as follows:

$$L_{si} = M_{psi} \quad or \quad {n_{si}}^2L_{mi} = n_{si}L_{mi} \quad or \quad n_{si} = 1 \tag{43}$$

**TABLE 2** DC characteristics of proposed free ripple converter

| | |
|---|---|
| Average low voltage side current of $I_\ell$ | $I_\ell = -G_{boost}(G_1 I_{H1} + G_2 I_{H2}) = \frac{-(G_1 I_{H1} + G_2 I_{H2})}{1-D_0}$ |
| Average current of inductors | $I_{Lmi} = -(G_1 I_{H1} + G_2 I_{H2})/(1 - D_0)$ |
| | $I_{Lm1} = (1 + n_{s1})(-I_{H1})/(1 - D_1)$ |
| | $I_{Lm2} = -(1 + n_{S2})(I_{H1} + I_{H2})/(1 - D_2)$ |
| Average current of switches | $I_{S1i} = \frac{-D_0}{1-D_0}(G_1 I_{H1} + G_2 I_{H2}), I_{S2i} = -(G_1 I_{H1} + G_2 I_{H2})$ |
| | $I_{S1} = D_1 I_{Lm1}, I_{S4} = I_{S5} = I_{H2}, I_{S2} = I_{H1}$ |
| | $I_{S3} = [I_{Lm2} - (1 + n_{s2}) I_{H2}/D_2] D_2$ |
| The maximum and minimum values of current $i_{Lm1}$ | $I_{h1} = I_{Lm1} + [V_\ell/(1 + L_{k1}/L_{m1})] D_1 T_s/2L_{m1}$ |
| | $I_{l1} = I_{Lm1} - [V_\ell/(1 + L_{k1}/L_{m1})] D_1 T_s/2L_{m1}$ |
| The maximum and minimum values of current $i_{Lm2}$ | $I_{h2} = I_{Lm2} + [(V_{H2} - V_{C1} - V_\ell)/n_{s2}] D_2 T_s/2L_{m2}$ |
| | $I_{l2} = I_{Lm2} - [(V_{H2} - V_{C1} - V_\ell)/n_{s2}] D_2 T_s/2L_{m2}$ |
| The maximum and minimum values of current $i_{Lmi}$ | $I_{hi} = I_{Lmi} + (V_{\ell i} D T_s)/(2L_{mi})$ |
| | $I_{li} = I_{Lmi} - (V_{\ell i} D T_s)/(2L_{mi})$ |
| Voltage conversion ratios | $G_{2i} = \frac{V_{H2}}{V_{\ell i}} = G_{boost} G_2 = \frac{1+n_{s2}}{(1-D_2)(1-D_0)}$ |
| | $G_{1i} = \frac{V_{H1}}{V_{\ell i}} = \frac{1}{1-D_0}(1 + \frac{D_1(1+n_{s1})}{(1-D_1)} + \frac{D_2(1+n_{s2})}{(1-D_2)}) = G_{boost} G_1$ |
| Voltage stress on switches | $V_{S1i} = V_\ell = V_{H1}/G_1$ : $During (1 - D_1) T_s$ |
| | $V_{S2i} = V_\ell = V_{H1}/G_1$ : $During\, D_1 T_s$ |
| | $V_{S1} = [1 + \frac{[G_1 - G_2 D_2 - 1]}{2 + n_{s1}}] \frac{V_{H1}}{G_1}$ : $During (1 - D_1) T_s$ |
| | $V_{S2} = [1 + (G_2 + n_{s1} - G_2 D_2) \frac{1}{G_1}] V_{H1}$ : $During\, D_2 T_s V_{S3} = V_{H1}/[(1 - D_2)\, G_1]$ : $During [(1 - D_2) T_s]$ |
| | $V_{S4} = V_{H2}$ : $During\, D_2 T_s$ |
| | $V_{S5} = V_{H2}$ : $During\, (1 - D_2)\, T_s$ |
| Voltage on capacitors | $\frac{V_{C1}}{V_{\ell i}} = \frac{D_2(1+n_{s2})}{(1-D_2)(1-D_0)}, V_{C1i} = V_{\ell i}, V_{C2i} = V_{\ell i}/(1 - D_0) = V_\ell$ |

$$M_{p1}{}^2 \neq L_{p1} L_{t1} \quad or \quad L_{k1} \neq 0 \tag{44}$$

$$(L_{m1} + L_{k1})\, n_{s1}{}^2 L_{m1} \neq (n_{s1} L_{m1})^2 \quad or \quad L_{k1} \neq 0 \tag{45}$$

Accordingly, the proposed developed converter in Figure 7, not only eliminates input current ripple at the DC port with high current (low voltage port) for whole ranges of duty cycles, but also increase the voltage gains between input voltage and output voltages (the voltage gains of proposed converter multiplied in the voltage gain of conventional boost converter) by using five elements ($S_{1i}$, $S_{2i}$, $C_{1i}$, $C_{2i}$ and one coupled inductor).

## 9 | PERFORMANCE COMPARISON

Table 3 presents comparative results of the proposed converter with other dc-dc single input, two-output converters from different aspects including voltage gains of each port ($G_{port}$), simultaneous control of output voltages (SCOV), maximum normalized voltage stress on switches based on maximum output voltage ($V_{S\,n,\max} = V_{S-\max}/V_{o\_\max}$), normalized current stress for the switch with the maximum voltage stress on it, ($I_{S\,RMS,n}|_{S:VS=VS\max}$), maximum power for switches of converter $(V_{S,n} I_{S\,RMS,n})_{\max}$, maximum normalized current stress on switches based on average input current ripple ($I_{S\,RMS,\,n-\max} = I_{S\,RMS-\max}/I_i$). The total voltage gain $G_T$ in the two-output converters is defined as $G_T = V_{o1}/V_i + V_{o2}/V_i = G_1 + G_2$. Figure 8(a) shows the total voltage gain over duty cycle. Based on Figure 8(a), $G_T$ for the proposed converter is higher than other conventional SIDO converters in Table 3.

On the other hand, the voltage gain of two output ports and total voltage gain $G_T$ of proposed converter and conventional converters for the specified duty cycle of $D = 0.6$ and $n = 1$ are calculated as column 3 of Table 3, which shows that $G_T$ for the proposed converter is obtained equal to $G_T = 12$ which is higher than that for the other conventional dual output converters.

Figure 8(b) shows the maximum normalized voltage stress on switches over duty cycle. Based on Figure 8(b), $V_{S\,n,\max}$ for the proposed converter (which is the voltage stress on switch $S_2$) is the medium value comparing to other conventional SIDO converters in Table 3.

In the other hand, $V_{S\,n,\max}$ in the proposed converter is lower than the presented converters in [9] and is higher than the presented converters in [8, 20, 28]). Figure 8(c) illustrates the normalized RMS current over the duty cycle for the switch which has the maximum voltage stress (switch $S_2$ in the proposed converter). Based on Figure 8(c), $I_{S\,RMS\,n}|_{VS=VS\max}$ for the proposed

**TABLE 3** Comparing results of high voltage gain SIDO converters

| DC-DC converter | $G_{port}$ | $G_{port}$ and $G_T$ for $D_1 = D_2 = D = 0.6$ $n = 1$ | $V_{S\,n,\max} = \frac{V_{S-\max}}{V_{o\_\max}}$ | $S_{\max} = (V_{S,n} I_{S\,RMS,n})_{\max}$ | $\frac{I_{S\,RMS}\mid_{VS = V\,S\max}}{I_{\ell}}$ | $I_{S\,RMS,\,n-\max} = \frac{I_{S\,RMS-\max}}{I_{\ell}}$ | SCOV | $N_{Op}$ |
|---|---|---|---|---|---|---|---|---|
| First converter in [8] ([8]-A) | $G_1 = \frac{1}{1-D}$<br>$G_2 = \frac{-1}{1-D}$ | $G_1 = 2.5$<br>$G_2 = 2.5$<br>$G_T = 5$ | 1 | $\frac{\sqrt{1-D}}{2G_2}$ | $\frac{\sqrt{1-D}}{2G_2}$ | $\frac{\sqrt{1-D}}{2G_2}$ | No | 1 |
| Second converter in [8] ([8]-B) | $G_1 = \frac{1}{1-D}$<br>$G_2 = \frac{2}{1-D}$ | $G_1 = 2.5$<br>$G_2 = 5$<br>$G_T = 7.5$ | 1 | $(1 - \frac{1}{2G_2} - \frac{1}{2G_1})\sqrt{D}$ | $(1 - \frac{1}{2G_2} - \frac{1}{2G_1})\sqrt{D}$ | $(1 - \frac{1}{2G_2} - \frac{1}{2G_1})\sqrt{D}$ | No | 1 |
| Third converter in [8] ([8]-C) | $G_1 = \frac{1}{1-D}$<br>$G_2 = \frac{2-D}{1-D}$ | $G_1 = 2.5$<br>$G_2 = 2.5$<br>$G_T = 5$ | 1 | $(1 - \frac{1}{2G_2} - \frac{1}{2G_1})\sqrt{D}$ | $(1 - \frac{1}{2G_2} - \frac{1}{2G_1})\sqrt{D}$ | $(1 - \frac{1}{2G_2} - \frac{1}{2G_1})\sqrt{D}$ | No | 1 |
| [9] | $G_1 = \frac{D}{1-D}$<br>$G_2 = \frac{2D-1}{1-D}$ | $G_1 = 2.5$<br>$G_2 = 3.5$<br>$G_T = 6$ | $\frac{1}{2D-1}$ | $\frac{\sqrt{D}}{2D-1}$ | $\sqrt{D}$ | $\sqrt{D}$ | Yes | 1 |
| [20] | $G_1 = \frac{1}{1-D}$<br>$G_2 = \frac{D}{1-D}$ | $G_1 = 2.5$<br>$G_2 = 1.5$<br>$G_T = 4$ | 1 | $(\frac{1}{2G_2} + \frac{1}{2G_1})\sqrt{D}$ | $(\frac{1}{2G_2} + \frac{1}{2G_1})\sqrt{D}$ | $(\frac{1}{2G_2} + \frac{1}{2G_1})\sqrt{D}$ | No | 3 |
| [28] | $G_1 = \frac{1}{1-D}$<br>$G_2 = \frac{1}{1-D}$ | $G_1 = 2.5$<br>$G_2 = 2.5$<br>$G_T = 5$ | 1 | $\frac{\sqrt{1-D}}{2G_1}$ | $\frac{\sqrt{1-D}}{2G_1}$ | $\frac{\sqrt{1-D}}{2G_1}$ | Yes | 2 |
| Proposed converter | $G_1 = \frac{1+nD}{1-D} + \frac{D(1+n)}{1-D}$<br>$G_2 = \frac{1+n}{1-D}$ | $G_1 = 7$<br>$G_2 = 5$<br>$G_T = 12$ | $S_2 : 1 + \frac{G_2 + n_{i1} - G_2 D}{G_1}$ | $S_2 : \frac{G_1 + n_{i1} + G_2(1-D)}{G_1} \frac{\sqrt{1-D}}{2G_1}$ | $S_2 : \frac{\sqrt{1-D}}{2G_1}$ | $S_3 : \frac{1+n_{i2}}{1-D}(\frac{D}{2G_1} + \frac{1}{2G_2})\sqrt{D}$ | Yes | 3 |

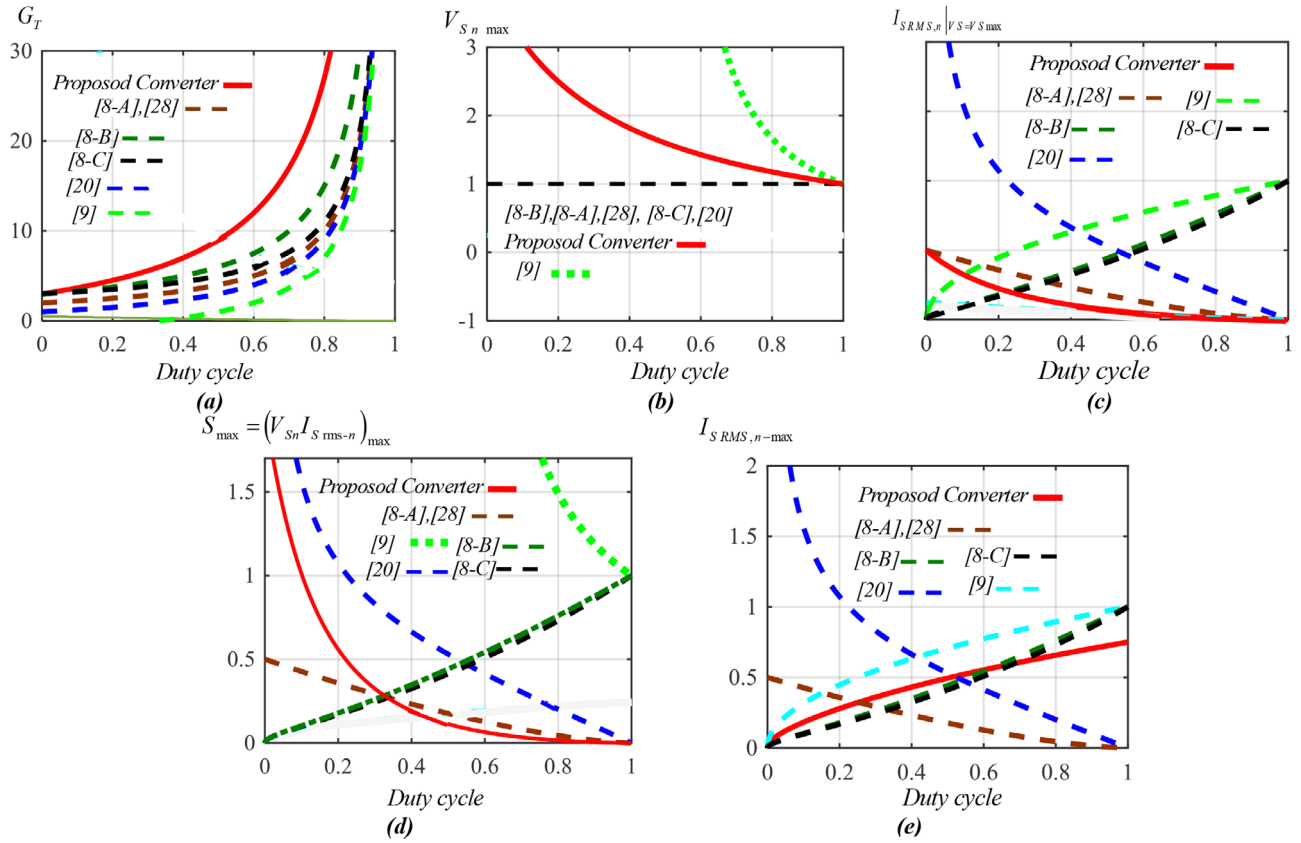


**FIGURE 8** (a) Total voltage gain over duty cycle; (b) maximum normalized voltage stress on switches; (c) normalized current stress for the switch with the maximum voltage stress; (d) maximum power for switches of converter; (e) maximum normalized current stress on switches

converter has the minimum value comparing to other conventional SIDO converters.

The cost of converters can be compared with their voltage and current stress on the semiconductors. If the current and voltage stress on each semiconductor multiply together, an equation will be achieved. By this equation (here called S and defined as power of switch), the cost, voltage and current stress on the semiconductors can be compared. As a result, the maximum value for the equation of power of switch $S_{\max}$ can be written as follows:

$$S_{\max} = (I_{RMS,n}\, V_{S,n})_{\max} = I_{S\,RMS,n}|_{S:VS=VS\,\max}\; V_{S,n\,\max} \quad (46)$$

Figure 8(d) is plotted to show that, the obtained maximum power of switches ($S_{\max}$( in the proposed converter (switch $S_2$ in the proposed converter) has almost the minimum value comparing to other conventional converters of the same type for the duty cycles higher than 0.3 regarding that the proposed converter has the medium value for maximum normalized voltage stress on switch based on Figure 8(b). Also, the maximum normalized current stress on switch ($I_{S\,RMS,n-\max}$) is plotted as Figure 8(e). Figure 8(e) shows that the proposed converter has the medium value of $I_{S\,RMS,n-\max}$ comparing to other conventional converters of the same type.

In order to have a simple comparison in Table 3 and Figure 8, all the duty cycles of the compared converters are considered as a same parameter of the duty cycle $D(0 < D_1 = D_2 = D < 1)$. The turns ratio of coupled inductors is considered as $n_{s1} = n_{s2} = n = 1$ in Figure 8.

Table 3 shows that the proposed converter and the converter in [20] have the maximum number of operation modes ($N_{Op} = 3$) and exchangeable place for the input voltage source among each of three ports. Moreover, the proposed converter and presented converters in [9] and proposed converter have the capability of simultaneous control of output voltages.

## 10 | EXPERIMENTAL RESULTS

In order to reconfirm the analytical results, the experimental results are extracted for first operation (stepped-up mode) of the proposed converter in Figures 8–10. The values of the different elements are summarized in Table 4. According to Equations (8)–(10), the capacitor voltage and output voltages for the parameters in Table 4 are calculated as $V_{C1} = 157.5$ V, $V_{H1} = 418.5$ V and $V_{H2} = V_{C1}/D_2 = 262.5$ V. The output voltages are almost equal to obtained values by experimental results in Figures 8(b) and 9(a). So, considering Table 1, the minimum values of used capacitors are calculated as $C_{1\_\min} = 11.41$ ¯F, $C_{H1\_\min} = 40$ ¯F, $C_{H2\_\min} = 57$ ¯F. Moreover, considering Equations (21) and (22), the inductances $L_{m1}$ and $L_{m2}$ to achieve CCM operation of the proposed converter,

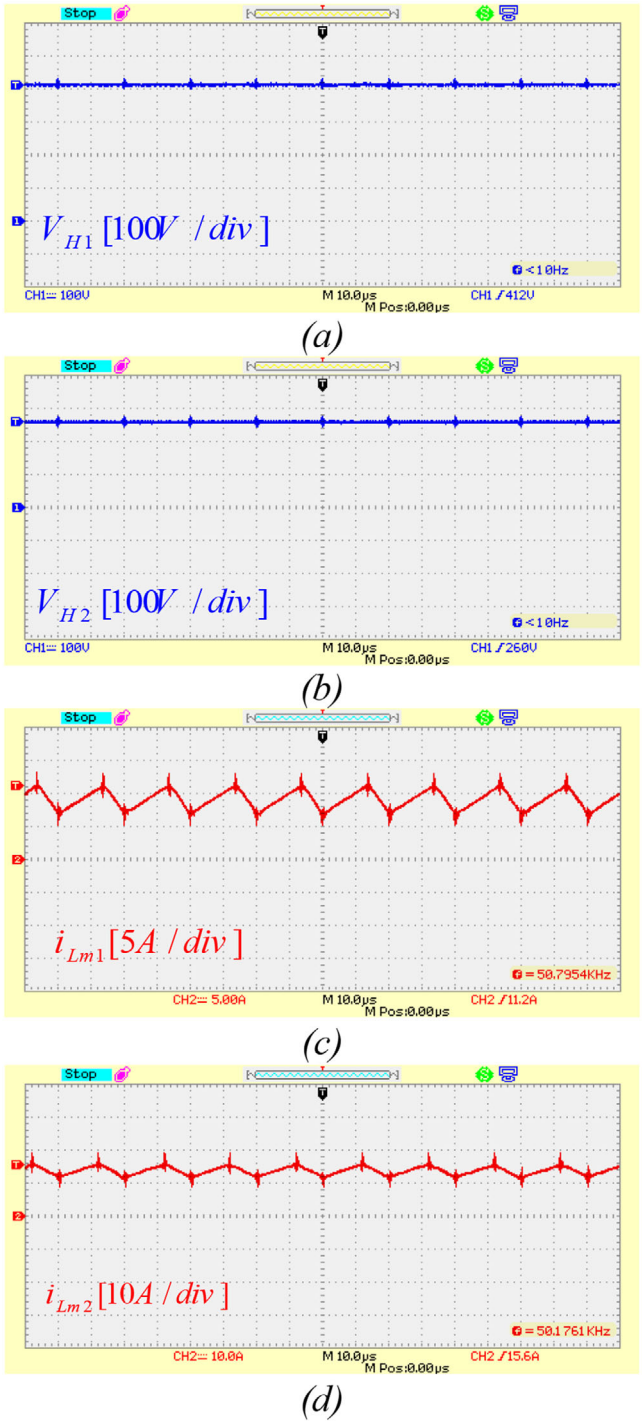


**FIGURE 9** Experimental results of output voltages and currents of inductors; (a) $V_{H1}$; (b) $V_{H2}$; (c) $i_{Lm1}$; (d) $i_{Lm2}$

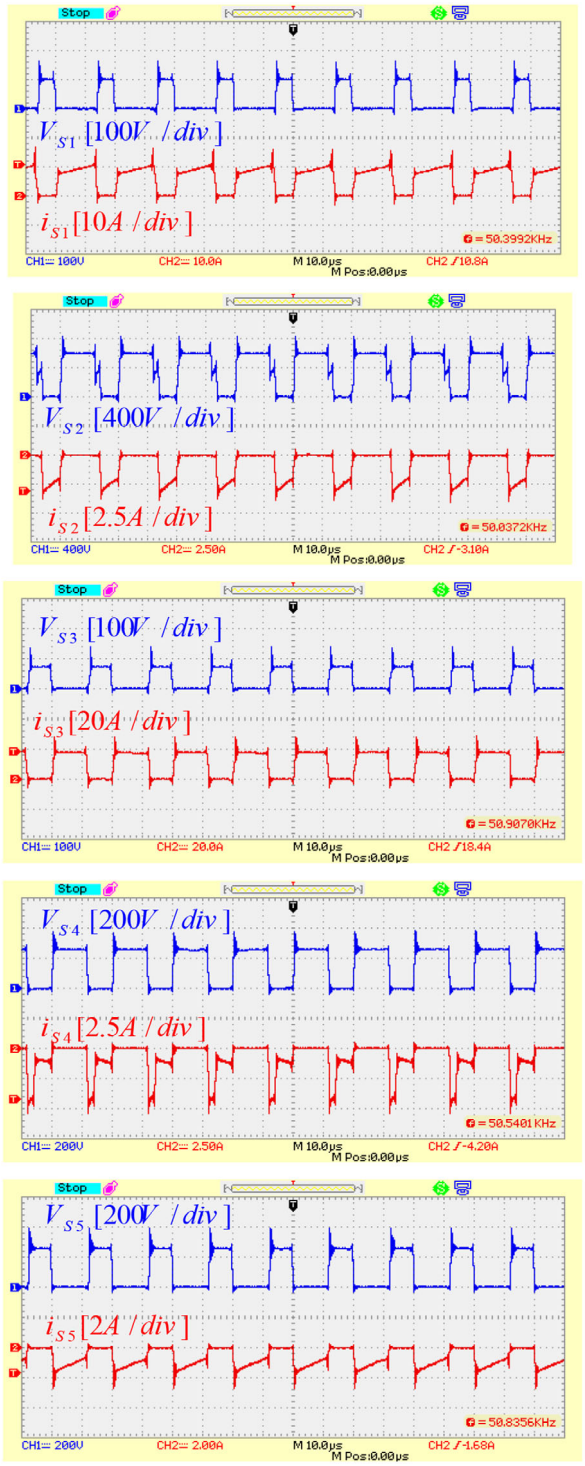


**FIGURE 10** Experimental results of voltages and currents of the switches $S_1$, $S_2$, $S_3$, $S_4$ and $S_5$.

should verify the inequalities $L_{m1} > 22.8$ ¯H and $L_{m2} > 13$ ¯H. Therefore, the capacitors and inductances values are selected as Table 4. In this operation, the output powers are theoretically calculated as $P_{H1} = {V_{H1}}^2/R_{H1} = 350.2$ W and $P_{H2} = {V_{H2}}^2/R_{H2} = 196.8$ W. Therefore, the total output power of converter based on theoretical analysis is equal to $P_{oT} = 547$ W. Referring to Equations (11)–(16), the voltage stress on switches $S_1$, $S_2$, $S_3S_4$, $S_5$ are calculated as follows:

$V_{S1} = 100$ V during the interval time of $(1 - D_1)\,T_S = 0.3\,T_S$,

$$V_{S2} = \begin{cases} 592 \text{ V} & during\ D_2\,T_S = 0.6\,T_S \\ 330 \text{ V} & during\ (D_1 - D_2)\,T_S = 0.1\,T_S \end{cases}$$

$V_{S3} = 75$ V during $(1 - D_2)\,T_S = 0.4\,T_S$

$V_{S5} = 262.5$ V during $(1 - D_2)\,T_S = 0.4\,T_S$

$V_{S4} = 262.5$ V during $D_2 T_S = 0.6 T_S$

**TABLE 4** Experimental parameters

| | |
|---|---|
| $V_\ell/V_{H1}/V_{H2} = 30\ V/410\ V/260\ V$ | DC Voltages |
| $P_{oT} = 510\ W$, $R_{H1} = 500\ \Omega$,$R_{H2} = 350\ \Omega$ | Power/Load |
| $C_1 = C_{H1} = C_{H2} = 100\mu F$ | Capacitors |
| $D_1 = 0.7$, $D_2 = 0.6$, $f_s = 50$ kHz | Duty cycles/Frequency |
| $L_{m1} = L_{m2} = 100\mu H$, $L_{k1} = 3.96\mu H$, $L_{k2} = 3.14\mu H$, $n_{S1} = 2.3$, $n_{S2} = 2.5$, Type: Toroid TDK PC40-T51 | Inductors |
| $S_1$: IRFP4668PbF (200V, 130A), $S_2$: IXFK32N80Q3(800V, 32A), $S_3$: NDPL180N10B (100V, 180A), $S_4$,$S_5$: IXFK150N30X3(300V, 150A) | Switches |

As a result, the calculated values are reconfirmed by the voltages stresses results in the experimental results in Figure 10. The output currents are calculated as $I_{o1} = -I_{H1} = 0.837A$, $I_{o2} = -I_{H2} = 0.75A$. Therefore, considering Equations (17) and (19), the average value of inductors' currents are calculated as $I_{Lm1} = 9.207$A and $I_{Lm2} = 13.88$A. The current ripple of the magnetizing inductances are calculated as $\Delta i_{Lm1} = (V_\ell/k_{1a})D_1T_s/L_{m1} = 4.11$ A and $\Delta i_{Lm2} = [(V_{H2} - V_{C1} - V_\ell)/n_{s2}]D_2T_s/L_{m2} = 3.6$A. Accordingly, the maximum and minimum values of current $i_{Lm1}$ are calculated as $I_{h1} = 11.262$A and $I_{l1} = 7.152$A that are almost equal to the illustrated values by experimental results in Figure 9(c).

The maximum and minimum values of the current $i_{Lm2}$ are calculated as $I_{h2} = 15.68$A and $I_{l2} = 12.08$A that are similar to the obtained result in Figure 9(d). The average currents passing through the switches $S_1$, $S_2$, $S_3$, $S_4$ and $S_5$ during a switching period at the steady state are calculated theoretically as $I_{S1} = D_1I_{Lm1} = 6.44$A, $I_{S2} = -(1 - D_1)[I_{Lm1}/(1 + n_{s1})] = -0.837$A, $I_{S3} = 10.95$A, $I_{S4} = I_{S5} = I_{H2} = -0.75$A. Based on the experimental results of the currents of switches in Figure 10, their average values during a switching period are calculated as $I_{S1} = 6.47$A, $I_{S2} = 0.785A$, $I_{S3} = 10.8A$ and $I_{S5} = -0.735A$ which are verified by theoretical values.

For controlling output voltages PI-controller is used. The output voltage regulations of the proposed converter under the variation of the input voltage $V_\ell$ increasing from 30 [V] to 40 [V] and decreasing to 20 [V] are extracted as shown in Figure 11. According to Figure 11, the voltage regulation of both two output ports are achieved at the same time in an acceptable way and the changes of the output voltages are not considerable by the changes of input voltage. Note that the spikes in Figure 11 happens when a sudden change happens in the input port. The implemented prototype of the proposed converter is shown in Figure 12.

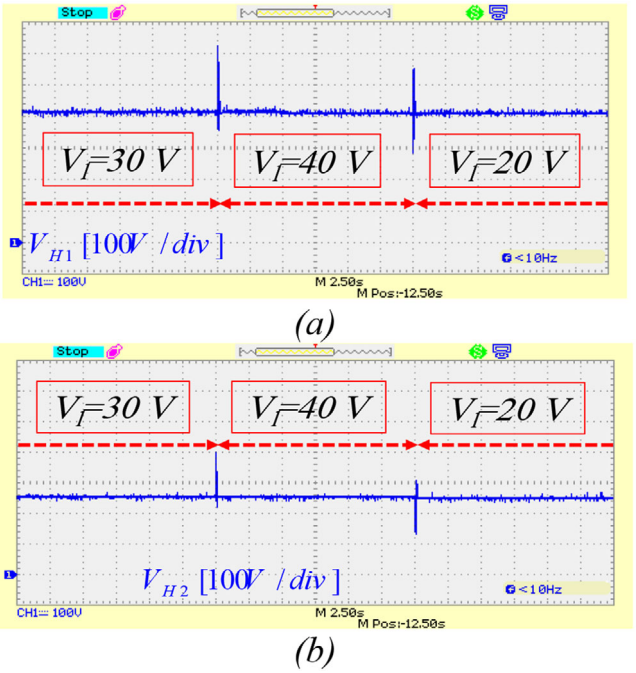


**FIGURE 11** The output voltages regulation under the input voltage $V_\ell$ variation

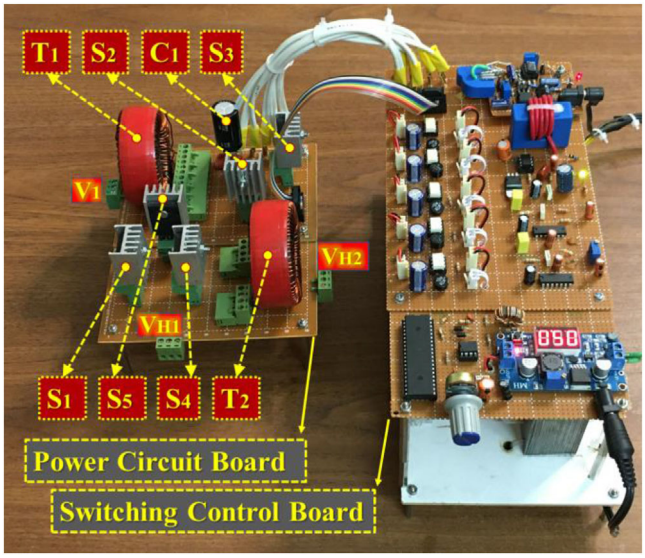


**FIGURE 12** Implemented prototype of the proposed converter

## 11 | POWER LOSS AND EFFICIENCY

In this section, the conduction and switching losses of proposed converter are calculated to obtain the efficiency. As a result, the internal resistors of switches ($r_S$), inductors ($r_L$), capacitors ($r_C$), forward drop voltage of switches ($V_{FS}$), rise time ($t_r$) and fall time ($t_f$) of switches are considered for calculating power losses.

According to [12], conduction losses of switches ($P_{Cond,S}$), switching losses for the switches ($P_{sw,S}$), total power loss of switches ($P_{S,Tot}$), total conduction loss of inductors ($P_{Cond,L}$),

**TABLE 5** Power loss calculation for all components of proposed converter

| | |
|---|---|
| $P_{Cond\_S}$ | $\frac{1}{T_s}\int_0^{T_S}(V_{FS}i_S + r_S{i_S}^2)\,dt = (V_{FS} + r_S I_{S-ON})I_S$ |
| $P_{SW,S}$ | $P_{Sw,S} = \frac{1}{2}f_S V_S i_S\|_{t=ton} t_r + \frac{1}{2}f_S V_S i_S\|_{t=toff} t_f$ |
| $P_{S,Tot}$ | $P_{S,Tot} = P_{Cond,S} + P_{SW,S}$ |
| $P_{Cond,L}$ | $P_{Cond,L} = r_{L1}{I_{Lm1}}^2 + r_{L2}{I_{Lm2}}^2$ |
| $P_{Core}$ | $\Delta B_{Lm1} = [V_\ell D_1 T_s]/N_1 A_c$ so, $P_{C1}$ in [kW/m$^3$] from datasheet<br>$\Delta B_{Lm2} = [(V_{H2} - V_{C1} - V_\ell)/n_{s2}]\,D_2 T_s/N_2 A_c$ so, $P_{C2}$ in [kW/m$^3$] from datasheet,<br>$P_{Core\_total} = (P_{C1} + P_{C2})\,V_e$ |
| $P_{Cond,C}$ | $P_{Cond,C} = \frac{1}{T_S}\int_0^{T_S} r_C {i_C}^2 dt$ |
| $P_{Loss}Efficiency$ | $P_{Loss} = P_{S,Tot} + P_{Cond,C} + P_{Cond,L} + P_{Core}$,<br>$Efficiency = P_o/(P_o + P_{Loss})$ |

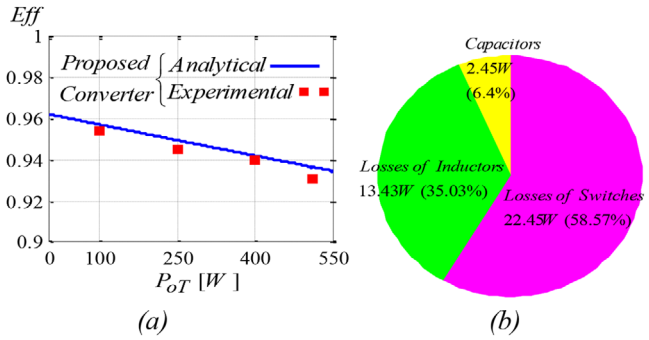


**FIGURE 13** (a) Efficiency of proposed converter versus output power; (b) power loss distribution among switches, inductors and capacitors for the output power equal to $P_{oT} = 510$ W

total core loss of inductors ($P_{Core\_total}$), total conduction loss of capacitors ($P_{Cond,C}$) and total power loss ($P_{Loss}$) are calculated as shown in Table 5. Figure 13(a) shows the efficiency of the proposed converter versus output power. The power loss distribution of the proposed converter among switches, inductors and capacitors for the output power of $P_{oT} = 510$ W is illustrated in Figure 13(b).

The switches are considered as Table 2. Therefore, the parameters of switches are as $V_{FS1} = V_{FS2} = V_{FS5} = V_{FS4} = 0.7$ V, $V_{FS3} = 0.75$ V, $r_{S1} = 8$ m$\Omega$, $r_{S2} = 270$ m$\Omega$, $r_{S3} = 2.5\,m\Omega$, $r_{S4} = r_{S5} = 6.6\,m\Omega$, $t_{rS1} = 105ns$, $t_{fS1} = 74ns$, $t_{rS2} = 13ns$, $t_{fS2} = 10ns$, $t_{rS3} = 320\,ns$, $t_{fS3} = 130ns$, $t_{rS4} = t_{rS5} = 32ns$, $t_{fS4} = t_{fS5} = 14ns$. Moreover, the internal resistors of capacitors and inductors are considered as $r_C = 0.5\,\Omega$ and $r_L = 0.1\,\Omega$, respectively.

## 12 | SIMULATION RESULTS OF THE PROPOSED DEVELOPED CONVERTER

The used simulation parameters of the proposed developed ripple free converter are shown in Table 6. Table 7 illustrates the analytical results of voltages on switches, capacitors, average currents of switches, average input current and output voltages

**TABLE 6** Simulation parameters for the proposed developed converter

| | |
|---|---|
| $L_{mi} = 50\mu H, L_{ki} = 5\mu H, n_{si} = 1\mu H$ | $V_{\ell i} = 12$ V |
| $C_{i1} = C_{i2} = 100\mu F$ | $D_0 = 0.6$ |

**TABLE 7** Theoretical analysis results of the proposed developed converter

| Voltage or current parameters | Calculated theoretical values of parameters |
|---|---|
| $I_{\ell i}, I_{Lmi}$ | $I_{Lmi} = -(G_1 I_{H1} + G_2 I_{H2})/(1 - D_0) = 44.8A$, |
| $I_{Si}$ | $I_{S1i}\|_{0<t<DT_s} = I_{\ell i} = 44.8A$,<br>$I_{S2i}\|_{DT_s<t<T_s} = I_{\ell i} = 44.8A$ |
| $V_{C1i}, V_{C2i}$ | $V_{C1i} = V_{\ell i} = 12\,V$, $V_{C2i} = V_\ell = 30\,V$ |
| $V_{H1}, V_{H2}$ | $V_{H1} = 260V, V_{o2} = 418.5V$ |
| $V_{S1i}, V_{S2i}$ | $V_{S1i} = 30\,V$ during $DT_S < t < T_S$ $V_{S2i} = 30\,V$ during $0 < t < DT_S$ |

of the proposed ripple free converter according to the given parameters in Table 6.

The calculated results of capacitor's voltages and output voltages which are shown in Table 7 can be verified by simulation results in Figure 16.

The voltage stresses on switches which are calculated in Table 7 during first ($0 < t < DT_S$) and second ($DT_S < t < T_S$) modes, respectively, are verified by Figure 15.

Based on Table 7, the analytical results of average currents of switches are shown which are almost equal to the obtained average currents of switches by simulation results in Figure 15. For example, according to Figure 15(a,b), the obtained average current of switches $S_{1i}$ and $S_{2i}$ by simulation results are as $I_{S1i}|_{0<t<DT_s} \simeq 43.6A$, $I_{S2i}|_{0<t<DT_s} \simeq 43.6A$ (verify calculated analytical results from Table 2 equal to $I_{S1i}|_{0<t<DT_s} \simeq 44.8A$, $I_{S2i}|_{DT_s<t<T_s} \simeq 44.8A$). The average value of inductor's currents from Table 7 is verified by Figure 14. The input current waveform is shown in Figure 14(c) which as it can be seen it is almost free ripple DC current with average value of $I_i = 43.53\,A$ from simulation results (verify theoretical analysis which is seen in Table 7 equal to $I_i = 44.8A$).

Figure 14 shows the Simulation results of currents of input side of proposed developed converter to confirm how the developed converter achieve zero input current ripple. By considering the developed converter in Figure 7, the sum of magnetizing inductor current ($i_{Lmi}$) and current of first winding of coupled inductor ($i_{Tpi}$) would be constant DC value equal to input current of $i_i$ as shown in Figure 14. Figure 15 shows the simulation results of voltage stresses on switches. Figure 16 shows the simulation results of voltages of capacitors and output voltages.

## 13 | CONCLUSION

In this paper, a SIDO high voltage gain coupled inductor- based DC–DC converter is proposed. The proposed converter can be

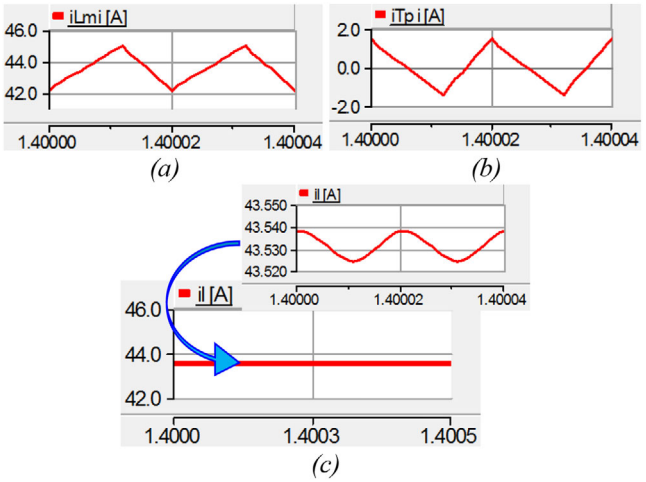


**FIGURE 14** Simulation results of currents of input side of proposed developed converter; (a) magnetizing inductor current ($i_{Lmi}$); (b) current of first winding of coupled inductor ($i_{Tpi}$); (c) input current of $i_i$ and its ac magnitude

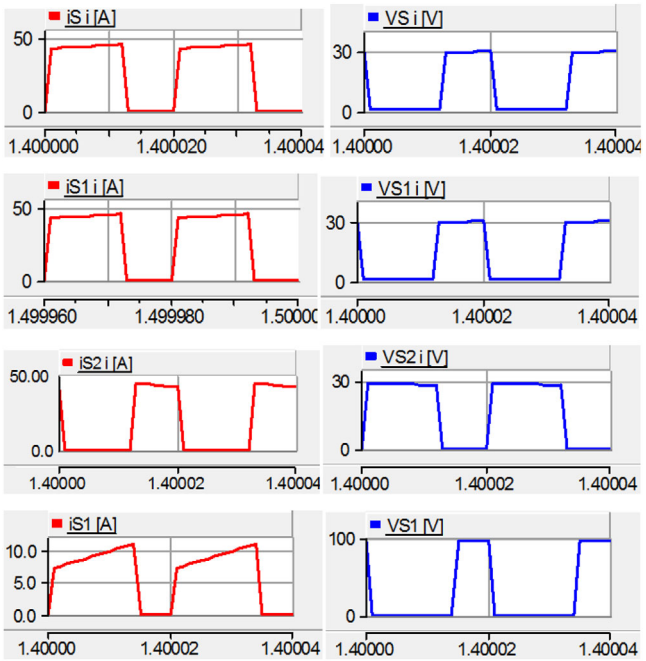


**FIGURE 15** Simulation results of voltage stresses on switches

operated in three different single-input/two-output structures. In this converter, the input voltage source can be replaced by any of each three ports. The voltage conversion ratios can be increased by increasing the turns ratio of the coupled inductors. The proposed converter has achieved high voltage gains with low number of components comparing to the conventional multi-port, high voltage gain converters. Moreover, two output voltages of the proposed converter can simultaneously be regulated on different constant levels. In this study, the voltage conversion ratios and the voltage and current stress on switches of the structure is analysed theoretically. Additionally, to demonstrate the validity of calculation results, a 30 V/410 V/260 V

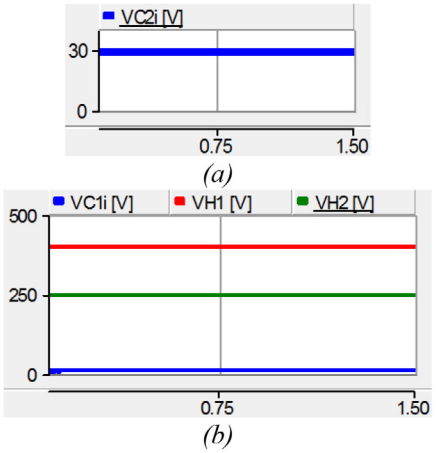


**FIGURE 16** Capacitor's voltages and output voltages; (a) $V_{C2i} = V_{\ell i}$; (b) input voltage $V_{C1i} = V_{\ell i}$, output voltage of $V_{H1}$ and output voltage of $V_{H2}$

with 510 W prototype is implemented in laboratory for stepped-up operation mode.

## NOMENCLATURE

| | |
|---|---|
| $V_l$ | Lowest DC voltage in port 1 |
| $V_{H1}$ | Medium DC voltage in port 2 |
| $V_{H2}$ | Highest DC voltage in port 3 |
| $D_1$ | Duty cycle of Switch $S_1$ |
| $D_2$ | Duty cycle of Switch $S_2$ |
| $D_0$ | Duty cycle of Switch $S_{1i}$ in the developed converter |
| $T_s$ | A complete switching period |
| $f_s$ | Switching frequency |
| $S_1$, $S_2$, $S_3$, $S_4$ and $S_5$ | Switches |
| $C_1$ | Capacitor |
| $T_1$ | Transformer of first coupling inductor |
| $L_{m1}$ | Magnetizing inductance of first coupled inductor |
| $L_{k1}$ | Leakage inductance of first coupled inductor |
| $T_2$ | Transformer of Second coupling inductor |
| $L_{m2}$ | Magnetizing inductance of second coupling inductor |
| $L_{k2}$ | Leakage inductance of second coupled inductor |
| $n_{p1}$ | Number of turns of the first windings of the transformer $T_1$ |
| $n_{s1}$ | Number of turns of the second windings of the transformer $T_1$ |
| $n_{p2}$ | Number of turns of the first windings of the transformer $T_2$ |
| $n_{s2}$ | Number of turns of the second windings of the transformer $T_2$ |
| $n_1$ | Turn ratio of the transformer $T_1$ |
| $n_2$ | Turn ratio of the transformer $T_2$ |
| $V_{C1}$ | Voltage across capacitor $C_1$ |
| $I_{b1}$ | Maximum value of the current of $L_{m1}$ at $t_2$ and $t_1$ |

$I_{b2}$ Maximum value of the current of $L_{m2}$ at $t_2$ and $t_1$s
$I_{l1}$ Minimum value of the current of $L_{m1}$ at $t_0$
$I_{l2}$ Minimum value of the current of $L_{m2}$ at $t_0$
$i_{Lm1}$ Current of the magnetizing inductance of the first coupling inductor
$i_{Lm2}$ Current of the magnetizing inductance of the second coupling inductor
$v_{Lm1}$ Voltage across the magnetizing inductance of the first coupling inductor
$v_{Lm2}$ Voltage across the magnetizing inductance of the second coupling inductor
$v_{Lk1}$ Voltage across the leakage inductance of the first coupling inductor
$v_{Lk2}$ Voltage across the leakage inductance of the second coupling inductor
$\tilde{v}_{Lm1}$ Average voltage across the magnetizing inductance of the first coupling inductor
$\tilde{v}_{Lm2}$ Average voltage across the magnetizing inductance of the second coupling inductor
$\tilde{v}_{Lk1}$ Average voltage across the leakage inductance of the first coupling inductor
$\tilde{v}_{Lk2}$ Average voltage across the leakage inductance of the second coupling inductor
$G_1$ The voltage conversion ratio of port 2 over port 1
$G_2$ The voltage conversion ratio of port 3 over port 1
$G_{port}$ Voltage gains of each port
$V_{S1}$ The voltage stress on switch $S_1$
$V_{S2}$ The voltage stress on switch $S_2$
$V_{S3}$ The voltage stress on switch $S_3$
$V_{S4}$ The voltage stress on switch $S_4$
$V_{S5}$ The voltage stress on switch $S_5$
$i_{S1}, i_{S1}, i_{S1}, i_{S1}$ and $i_{S1}$ Currents passing through the switches at each moment
$I_{S1}$ Average current passing through the switch $S_1$ during a switching period in steady state
$I_{S1,n}$ Normalized average current passing through the switch $S_1$ based on input current for boost operation
$I_{S1-RMS,n}$ Normalized RMS current passing through the switch $S_1$ for boost operation
$I_{S2}$ Average current passing through the switch $S_2$ during a switching period in steady state
$I_{S2,n}$ Normalized average current passing through the switch $S_2$ based on input current for boost operation
$I_{S2-RMS,n}$ Normalized RMS current passing through the switch $S_2$ for boost operation
$I_{S3}$ Average current passing through the switch $S_3$during a switching period in steady state
$I_{S3,n}$ Normalized average current passing through the switch $S_3$ based on input current for boost operation
$I_{S3-RMS,n}$ Normalized RMS current passing through the switch $S_3$ for boost operation
$I_{S4}$ Average currents passing through the switch $S_4$ during a switching period in steady state
$I_{S4,n}$ Normalized average current passing through the switch $S_4$ based on input current for boost operation
$I_{S5}$ Average currents passing through the switch $S_5$ during a switching period in steady state
$I_{S5,n}$ Average currents passing through the switch $S_5$ based on input current for boost operation
$I_{S5-RMS,n}$ Normalized RMS current passing through the switch $S_5$ for boost operation
$I_{Lm1}$ Average magnetizing inductance current of magnetizing inductance of first coupled inductor
$I_{Lm2}$ Average magnetizing inductance current of magnetizing inductance of second coupled inductor
$\tilde{i}_{C1}$ Average current passing through the capacitor $C_1$
$I_l$ Average current passing through DC voltage port 1
$I_{H1}$ Average current passing through DC voltage port 2
$I_{H2}$ Average current passing through DC voltage port 3
$I_{o1}$ Output current of port 1 in boost operation
$I_{o2}$ Output current of port 2 in boost operation
$I_{o3}$ Output current of port 3 in boost operation
$P_\ell$ Input power from port 1
$P_{H1}$ Input Output power from port 2
$P_{H2}$ Input power from port 3
$P_{oT}$ Total output power
$\Delta i_{Lm1}$ Currents' ripple of the magnetizing inductance $L_{m1}$
$\Delta i_{Lm2}$ Currents' ripple of the magnetizing inductance $L_{m2}$
$\Delta V_{CT}$ Peak-to-peak value of the total voltage ripple of the capacitors
$V_C$ Average value of the voltage across the capacitors
$\Delta V_C$ The voltage ripple across the capacitors
$\Delta V_{C-ESR}$ Voltage ripple across the capacitors caused by the ESR of capacitors
$r_C$ Inner resistance of the capacitors
$\Delta I_C$ Current ripple of the capacitors during
$V_{C\ell}$ Average voltage across the output capacitor in port 1
$V_{CH1}$ Average voltage across the output capacitor in port 2
$V_{CH2}$ Average voltage across the output capacitor in port 3
$C_{1\_\min}$ Minimum designed capacitance value for the capacitor $C_1$

| | |
|---|---|
| $C_{l\_\min}$ | Minimum designed capacitance value for the output capacitor at port 1 |
| $C_{\ell}\|_{ESR}$ | Minimum capacitance value for the output capacitor at port 1 considering Equivalent Series Resistance (ESR) |
| $C_{\ell}\|_{THT}$ | Minimum capacitance value for the output capacitor at port 1 considering Total holding Time (THT) |
| $C_{H1\_\min}$ | Minimum designed capacitance value for the output capacitor at port 2 |
| $C_{H1}\|_{ESR}$ | Minimum capacitance value for the output capacitor at port 2 considering Equivalent Series Resistance (ESR) |
| $C_{H1}\|_{THT}$ | Minimum designed capacitance value for the output capacitor at port 2 considering Total Holding Time (THT) |
| $C_{H2\_\min}$ | Minimum designed capacitance value for the output capacitor at port 3 |
| $C_{H2}\|_{ESR}$ | Minimum designed capacitance value for the output capacitor at port 3 considering Equivalent Series Resistance (ESR) |
| $C_{H2}\|_{THT}$ | Minimum designed capacitance value for the output capacitor at port 3 considering Total Holding Time (THT) |
| $R_{\ell}$ | Output load at port 1 |
| $R_{H1}$ | Output load at port 2 |
| $R_{H2}$ | Output load at port 3 |
| $I_S$ | Average current passing through the switches |
| $I_{S-ON}$ | Average current passing through the switches at the turning on moment |
| $r_{S1}$, $r_{S2}$, $r_{S3}$, $r_{S4}$ and $r_{S5}$ | The internal resistors of switches $S_1$, $S_2$, $S_3$, $S_4$ and $S_5$ |
| $r_L$ | The internal resistors of inductors |
| $r_C$ | The internal resistors of capacitors |
| $V_{FS1}$, $V_{FS2}$, $V_{FS3}$, $V_{FS4}$ and $V_{FS5}$ | Forward drop voltage of switches $S_1$, $S_2$, $S_3$, $S_4$ and $S_5$ |
| $t_{rS1}$, $t_{rS2}$, $t_{rS3}$, $t_{rS4}$ and $t_{rS5}$ | Rise time of switches $S_1$, $S_2$, $S_3$, $S_4$ and $S_5$ |
| $t_{fS1}$, $t_{fS2}$, $t_{fS3}$, $t_{fS4}$ and $t_{fS5}$ | Fall time of switches $S_1$, $S_2$, $S_3$, $S_4$ and $S_5$ |
| $t_r$ | Fall time of switch |
| $t_f$ | Rise time of switch |
| $P_{Cond\_S}$ | Conduction losses of switches |
| $P_{SW,S}$ | Switching losses for the switches |
| $P_{S,Tot}$ | Total power loss of switches |
| $P_{Cond,L}$ | Total conduction loss of inductors |
| $P_{Core\_total}$ | Total core loss of inductors |
| $P_{Cond,C}$ | Total conduction loss of capacitors |
| $P_{Loss}$ | Total power loss |
| $P_{Core}$ | Losses of the cores of the inductors |
| $\Delta B_{Lm1}$ and $\Delta B_{Lm2}$ | Flux density of inductors |
| $P_{C1}$ and $P_{C2}$ | Power density of inductors [kW/m$^3$] |

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