A Variable Phase-Shift Control Scheme for Extended-Duty-Ratio Boost Converter with Automatic Current Sharing in High Step-up High Current Application

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A Variable Phase-Shift Control Scheme for Extended-Duty-Ratio Boost Converter with Automatic Current Sharing in High Step-up High Current Application

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***Abstract*—Recently, an extended-duty-ratio (EDR) boost converter has attracted great attention of many scholars. However, the EDR boost converter with fix phase shifts is difficult to achieve phase-to-phase current sharing over a wide range of duty ratio. In this paper, a variable phase-shift control strategy is proposed to further expand its current sharing range for the EDR boost converter. Under the proposed control strategy, the EDR boost converter can operate in wide range of duty ratio varying from 0.5 to 1 with automatic current sharing between phases since two adjacent phase shifts can be adjusted to guarantee that the energy stored in certain inductor is only transferred to the next phase capacitor step by step for generating high step-up output voltage. Next, the steady-state analysis of the EDR boost converter under the proposed control strategy is discussed thoroughly, and the switch voltage stresses and current stresses are also analyzed. Finally, a 300 W, 3.3 V to 38.9 V, four-phase EDR boost hardware prototype has been built. The effectiveness of the proposed control strategy is verified by the experimental results of the built prototype.**

***Index Terms*—Current sharing, duty ratio, extended-duty-ratio (EDR), high step-up, phase shifts.**

I. Introduction

With the increase of traditional energy consumption and the resulting environmental pollution, it is an extremely urgent task for human beings to find renewable and clean energy sources. As alternative energy sources, solar energy and hydrogen energy are effective measures to ensure electricity supply and reduce greenhouse gases. However, due to the relatively low output dc voltage generated by fuel cells and photovoltaic panels, it is necessary to boost the voltage to the specified rating by high-efficiency and high step-up dc-dc converters [1]–[3]. In addition, with the increasing demand for energy storage systems in recent year, high step-up converters have attracted more and more attention, especially in the interface with lithium batteries [4], [5]. For example, a single-cell lithium battery with a large capacity (3.3 V / 100 Ah) as an energy storage battery for electric bicycles requires a high step-up dc-dc converter for power conversion.

From the perspective of electrical isolation, high step-up dc-dc converters can be classified into isolated and non-isolated types. Non-isolated high step-up dc-dc converters are widely used in industrial applications due to their advantages such as high efficiency, high power density, and low cost. And these converters can be further classified into coupled-inductor and uncoupled-inductor types. In the non-isolated coupled-inductor converters, the high voltage gain can be achieved by adjusting turns ratio of the coupled inductor [6]–[10]. However, larger leakage inductor may cause voltage spikes across the switches, which requires the technique to clamp or recycle the energy to suppress oscillation and improve the efficiency [9], [10]. The non-isolated uncoupled inductor converters are usually composed of cascaded boost converters [11]–[13] or quadratic boost [14], [15] or the voltage-lift technology [16]–[18] or voltage multipliers (gain cells) [19]–[24], or switched inductor and/or switched-capacitor cells [25]–[28]. These converters can provide high voltage gain, but due to the large number of components, they are a bit complex and costly. In general, it is difficult for most of these topologies to be directly used in high current applications.

In practical applications, it is challenging to realize both low voltage and high current. Interleaved converters are widely used in high current and high power applications due to their advantages such as current ripple cancellation, fast transient response, and reduced passive component size [29]–[33]. However, classic interleaved boost converters are not suitable for high step-up applications because when the converter is operating at extremely high duty ratios to attain the high step-up voltage gain, high amplitude narrow pulse currents will

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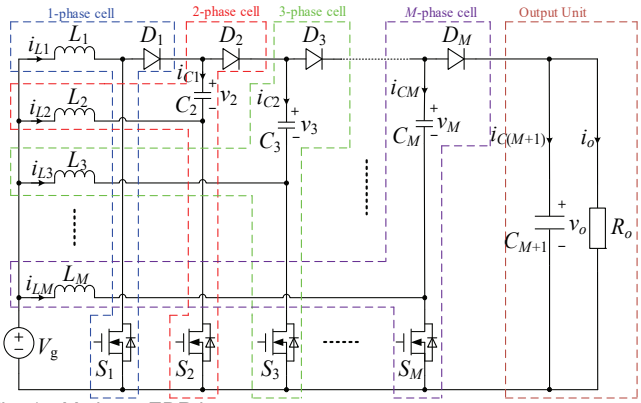


Fig. 1. *M*-phase EDR boost converter.

be generated in the diode, which can cause serious reverse recovery issues.

One effective way to overcome the limitations of convert performance due to extreme duty ratio is to employ extended duty ratio (EDR) boost converters. According to the topologies presented in [34]–[37] and [39], EDR converters are ideal for high current and high step-up applications. A coupled inductor extended duty ratio buck converter was proposed as a solution of voltage regulators for microprocessor application in [35]. Two-phase and four-phase versions of the topology were further examined in [37] and [36], where the two-phase interleaved buck converter with two active switches in series and a coupled capacitor was proposed to achieve step-down conversion ratio, and the four-phase version was developed to achieve a higher step-down conversion ratio and more power without operating at an extremely low duty ratio. In [39], the two-phase converter with high-voltage gain was proposed and the current sharing conditions for the converter were discussed in detail. In addition, the *N*-phase converters were presented, but the range of the duty ratio and the phase shifts with the current sharing were not clarified. Although a fixed phase-shift control method by 180° was proposed to achieve the current sharing for the *N*-phase EDR converter in [40], this control method is only a special case, and the mechanism of how the duty cycle and phase shift affect current sharing was not clearly investigated.

In recent works, a sensor-less current sharing technique for *M*-phase (where *M* is the number of phases) EDR boost converter was developed to ensure input current being shared equally between phases in [38], and a three-phase EDR boost converter was implemented with this control strategy as the first power stage for the PV microinverter system to generate a higher dc voltage in [34]. Unfortunately, the *M*-phase EDR boost converter only had inherent current sharing among the phases in a limited duty ratio range with the fixed phase shift $2\pi/M$ [38]. The inherent current sharing characteristics of the converter would lose when the duty ratio exceeds the limits in wide input voltage applications. Simultaneously, as the number of phases of the converter increases, the duty ratio range of the converter operating with current sharing would become smaller and smaller. Obviously, it was a serious challenge. To solve this problem, the authors in [38] tended to change the duty ratio of each phase individually to ensure the current sharing when the duty ratio was reduced beyond the range, instead of having the same duty ratio for all phases.

In this paper, a variable phase-shift control strategy for *M*-phase EDR boost converter with automatic current sharing is proposed to further extend the operation range of duty ratio. Under the proposed control strategy, all switches in *M*-phase EDR boost converter operate at the same duty ratio. It is only necessary to adjust the phase shifts in *M*-phase EDR boost converter to achieve the current sharing. When the phase shifts satisfy certain conditions, the energy stored in each phase of the EDR boost converter will be transferred to the next, step by step, to generate high step-up output voltage at the end stage. By applying the amp-second balancing to the capacitors, all inductor currents are equal to each other. Besides, since no current sensor is required, the control strategy is simple and flexible, and the range of current sharing is not limited to the number of phases of the converter.

This paper is organized as follows. The following Section II presents the fixed phase-shift control strategy and the proposed phase-shift control strategy for *M*-phase EDR converter. In Section III, the analysis of the steady-state performance is developed under the proposed control strategy. Section IV presents the simulation of input ripple current and dynamic load behavior. The hardware prototype of four-phase EDR boost converter is developed based on the analysis, and detailed experimental results are presented for validation in Section V. Finally, the main contributions of this paper are summarized in Section VI.

II. Proposed Phase-Shift Control Scheme

A. *M*-Phase EDR Boost Converter with Fixed Phase Shift ($2\pi/M$) Control Strategy

The *M*-phase EDR boost converter is composed of input dc voltage source, *M*-phase cell and output unit, as shown in Fig. 1. From Fig. 1, it can be also seen that each of phase cells consists of an active switch, a diode, and a capacitor (except for the first phase). This converter not only inherits the advantages of multiple capacitors and multiple inductors, but also has low losses due to the low voltage stress of most switches. With fixed phase shift ($2\pi/M$), the operation of *M*-phase EDR boost converter has been divided into *M* different zones, and the duty ratio limitation for the *m*th zone given in [38] is shown as follows.

$$\frac{M-m}{M} \le D \le \frac{M-m+1}{M} \quad \text{for all } m \in [1, M]. \tag{1}$$

In different zones, the voltage gain of *M*-phase EDR boost converter couldn't be expressed with a general expression. The current was inherently shared among all inductors only in zone I according to [38]. Thus, as the number of phases increases, the inherent current sharing range related to the duty ratio will be significantly reduced. However, it is impossible to guarantee the converter operating in zone I when the input or output voltage varies over a wide range. Therefore, the currents among all inductors are no longer shared equally. In [38], another method was presented to change the duty ratio of each phase individually to ensure the current sharing in all operating re-

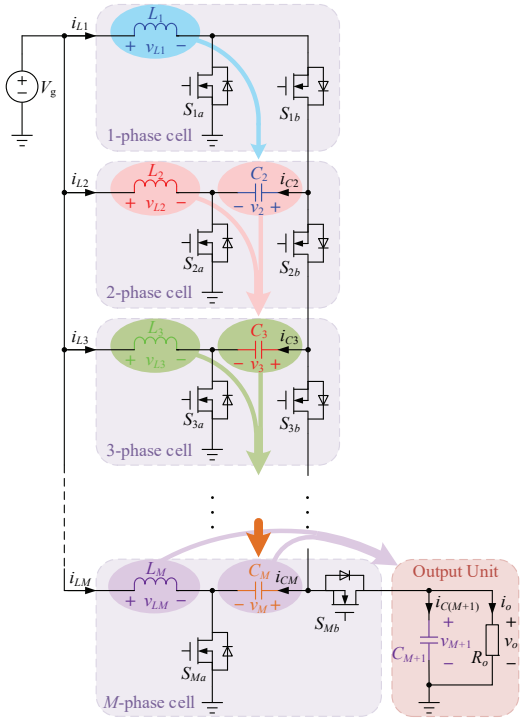


Fig. 2. Energy transferring diagram for *M*-phase EDR boost converter.

gions. However, it is difficult to find a generalized approach for the EDR boost converter with a higher number of phases.

B. Proposal of Phase-Shift Control Strategy

It is assumed that: 1) the *M*-phase EDR converter in Fig. 1 operates at a fixed frequency, 2) each phase has the same duty ratio, and 3) there is a variable phase shift between any two adjacent phases. In addition, to simplify the operational analysis of the converter, the following assumptions are made:

1) All components are considered ideal, ignoring their parasitic parameters; the inductance values of all inductors are equal to each other and are large enough to ensure that their instantaneous currents can be approximated by the average current, respectively.

2) Complementary pulses drive a pair of switches (S_{na} and S_{nb}), ignoring the dead time.

3) The output capacitor C_{M+1} is large enough that its voltage is considered constant during one switching cycle.

In order to obtain a high output voltage, the energy stored in L_n ($n = 1, 2, \ldots, M$) is sequentially transferred to C_{n+1} through a reasonable switching action. Then, the energy stored in C_{n+1} together with L_{n+1} continues to be transferred to C_{n+2}. Finally, the energy of all inductors is transferred to C_{M+1} and powers the load R_o. Replacing all diodes in Fig. 1 with a synchronous MOSFET can further reduces conduction losses and improves converter's efficiency. Therefore, the *M*-phase EDR converter is reconstructed as shown in Fig. 2, where the energy transferring diagram reveals how to deliver energy the load step by step.

Concretely, when S_{1a} is in ON-state, V_g is applied to L_1, thus i_{L1} linearly increases. When S_{1a} is in OFF-state, both S_{1b} and S_{2a} are in ON-state, then C_2 is charged by L_1 and V_g. i_{L1} decreases

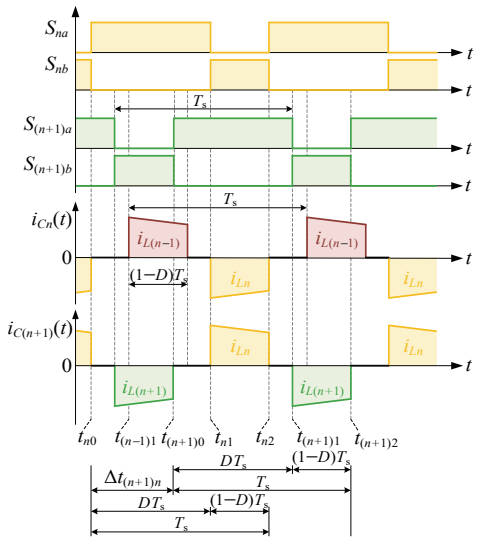


Fig. 3. Waveforms for the switching time sequences of $S_{(n+1)a}$ and S_{na} and currents flowing through C_n and C_{n+1}.

and v_{C2} increases. During this period, the energy stored in L_1 is transferred to C_2. Besides, L_2 is charged by V_g, and i_{L2} linearly increases. When S_{2a} is in OFF-state, both S_{2b} and S_{3a} are in ON-state, then C_3 will be charged by L_2, C_2, and V_g. Subsequently, i_{L2} decreases, v_{C2} decreases, and v_{C3} increases. Therefore, the energy stored in L_2 and C_2 is transmitted to C_3 during this period. In addition, L_3 is charged by V_g, and i_{L3} increases linearly. Finally, when S_{Ma} is in ON-state, L_M is charged by V_g, and i_{LM} linearly increases. When S_{Ma} is in OFF-state and S_{Mb} is in ON-state, the energy stored in L_M and C_M are released to C_{M+1}. The load R_o is supplied by C_{M+1}.

Fig. 3 shows the switching time sequences of any two adjacent lower switches $S_{(n+1)a}$ and S_{na}, where $\Delta t_{(n+1)n}=t_{(n+1)0} - t_{(n)0}$. In Fig. 3, t_{n0} and $t_{(n+1)0}$ are the turn-on times of S_{na} and $S_{(n+1)a}$, respectively. In order to obtain the energy transfer mode mentioned above, it must be satisfied that $S_{(n+1)a}$ is in ON-state when S_{na} is in OFF-state. Hence, the following two inequalities must be true.

$$\begin{cases} \Delta t_{(n+1)n} \le DT_s \\ \Delta t_{(n+1)n} + DT_s \ge T_s. \end{cases} \tag{2}$$

The above formula can be simplified to

$$(1-D)T_s \le \Delta t_{(n+1)n} \le DT_s. \tag{3}$$

From (3), obviously, D must be satisfied with

$$D \ge 0.5. \tag{4}$$

If the phase shift between any adjacent two phase $S_{(n+1)a}$ and S_{na} are signified by $\varphi_{(n+1)n}$, phase shift $\varphi_{(n+1)n}$ is equal to

$$\varphi_{(n+1)n} = 2\pi \frac{\Delta t_{(n+1)n}}{T_s} \quad \text{for } n = 1, 2, 3, \ldots, M-1. \tag{5}$$

Substituting (5) into (3), the phase-shift range can be obtained

$$2\pi(1-D) \le \varphi_{(n+1)n} \le 2\pi D \quad \text{for } n = 1, 2, 3, \ldots, M-1. \tag{6}$$

When $\Delta t_{(n+1)n}$ satisfies inequality (3), $i_{C(n+1)}$ flowing through C_{n+1} is shown in Fig. 3, where only i_{Ln} and $i_{L(n+1)}$ flow through C_{n+1} in a switching period T_s.

By applying the ampere-second balance principle on C_{n+1} during the OFF-state of S_{na} and OFF-state of $S_{(n+1)a}$, the average current ($I_{L(n+1)}$) of L_{n+1} is equal to the average one (I_{Ln}) of L_n. That's to say

$$I_{Ln} = I_{L(n+1)}. \tag{7}$$

A similar argument can be applied to C_{M+1}, and the average current (I_{LM}) can be expressed as follows:

$$I_{LM} = \frac{I_o}{1-D}. \tag{8}$$

By (7) and (8), it can be obtained as:

$$I_{L1} = I_{L2} = \ldots = I_{LM} = \frac{I_o}{1-D}. \tag{9}$$

The current ripple Δi_{Ln} of inductor L_n can be given by

$$\Delta i_{Ln} = \frac{V_g}{2L_n} D T_s. \tag{10}$$

According to (9) and (10), it can be conclude that the proposed control strategy can realize the current sharing without the current sensor when 1) D for each phase is the same and in the range of $0.5 \le D < 1$ and 2) $\varphi_{(n+1)n}$ ($n = 1, 2, 3, \ldots, M-1$) must be satisfied with $2\pi(1-D) \le \varphi_{(n+1)n} \le 2\pi D$. Since no current sensor is required, the proposed control scheme is easy to be implemented in practice.

III. Performance Analysis for Converter With Proposed Control Scheme

A. Capacitor Voltages

The steady-state voltage and current waveforms of the capacitors in the M-phase EDR boost converter are illustrated in Fig. 4. There are four subintervals for the capacitor voltage (v_{n+1}) for C_{n+1} during one switching period T_s.

1) Constant minimum voltage stage [$t_{(n+1)0}$–t_{n1}]: During this subinterval, v_{n+1} remains at the constant minimum voltage, equal to $V_{(n+1)min}$ since no current flows through C_{n+1}.

2) Charging stage [t_{n1}–t_{n2}]: During this subinterval, C_{n+1} is charged by L_n, and v_{n+1} reaches the maximum voltage $V_{(n+1)max}$ from $V_{(n+1)min}$. Therefore, neglecting the current ripple of L_n, v_{n+1} can be expressed as:

$$v_{n+1}(t) = V_{(n+1)min} + \frac{I_{Ln}}{C_{n+1}} t \quad 0 < t \le (1-D)T_s. \tag{11}$$

3) Constant maximum voltage stage [t_{n2}–$t_{(n+1)1}$]: During this subinterval, since no current flows through C_{n+1}, v_{n+1} still remain the constant maximum voltage equal to $V_{(n+1)\,max}$.

4) Discharging stage [$t_{(n+1)1}$–$t_{(n+1)2}$]: During this subinterval, C_{n+1} is discharged by L_{n+1}, and v_{n+1} would decrease from $V_{(n+1)\,max}$ to $V_{(n+1)\,min}$. Similarly, v_{n+1} can be expressed as:

$$v_{n+1}(t) = V_{(n+1)max} - \frac{I_{L(n+1)}}{C_{n+1}} t \quad 0 < t \le (1-D)T_s. \tag{12}$$

The following equation can be obtained from the Fig. 4

$$\int_0^{(1-D)T_s} [V_{(n+1)max} - \frac{I_{L(n+1)}}{C_{n+1}} t]dt = \int_0^{(1-D)T_s} [V_{(n+1)min} + \frac{I_{Ln}}{C_{n+1}} t]dt. \tag{13}$$

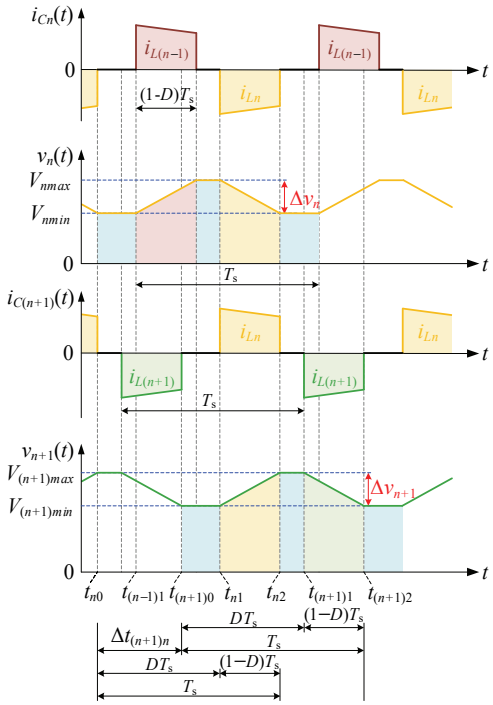


Fig. 4. Waveforms of voltage and current for capacitor C_n and C_{n+1}.

By applying volt-second balance principle to all inductors, the following equations can be obtained.

$$\begin{cases} V_g T_s - \int_0^{(1-D)T_s} (V_{2min} + \frac{I_{L1}}{C_2} t)dt = 0 \\ V_g T_s + \int_0^{(1-D)T_s} (V_{2max} - \frac{I_{L2}}{C_2} t)dt - \int_0^{(1-D)T_s} (V_{3min} + \frac{I_{L2}}{C_3} t)dt = 0 \\ \ldots\ldots \\ V_g T_s + \int_0^{(1-D)T_s} (V_{2max} - \frac{I_{L2}}{C_2} t)dt - \int_0^{(1-D)T_s} (V_{3min} + \frac{I_{L2}}{C_3} t)dt = 0 \\ V_g T_s + \int_0^{(1-D)T_s} (V_{(n+1)max} - \frac{I_{L(n+1)}}{C_{(n+1)}} t)dt \\ \qquad - \int_0^{(1-D)T_s} (V_{(n+2)min} + \frac{I_{L(n+1)}}{C_{n+2}} t)dt = 0 \\ \ldots\ldots \\ V_g T_s + \int_0^{(1-D)T_s} (V_{Mmax} - \frac{I_{LM}}{C_M} t)dt - \int_0^{(1-D)T_s} v_o(t)dt = 0. \end{cases} \tag{14}$$

From (13) and (14), the dc component of output voltage can be derived as

$$V_o = \frac{M V_g}{1-D}. \tag{15}$$

Similarly, the expressions of V_{nmin} and V_{nmax} can be obtained as

$$\begin{cases} V_{nmin} = \frac{(n-1)V_g}{1-D} - \frac{I_{L(n-1)}(1-D)T_s}{2C_n} \\ V_{nmax} = \frac{(n-1)V_g}{1-D} + \frac{I_{L(n-1)}(1-D)T_s}{2C_n} \end{cases}, \quad n = 2, 3, \ldots, M. \tag{16}$$

Substituting (9) into (16) yields

$$\begin{cases} V_{nmin} = \dfrac{(n-1)V_{\mathrm{g}}}{1-D} - \dfrac{I_o T_s}{2C_n} \\ V_{nmax} = \dfrac{(n-1)V_{\mathrm{g}}}{1-D} + \dfrac{I_o T_s}{2C_n} \end{cases}, \ n = 2, 3, ..., M. \tag{17}$$

The voltage variation of C_n is represented by Δv_n, as illustrated in Fig. 4. From (17), Δv_n can be expressed as

$$\Delta v_n = \frac{I_o T_s}{C_n}, \ n = 2, 3, ..., M. \tag{18}$$

Without exception, Δv_{M+1}, equal to the ripple of output voltage, can be expressed as

$$\Delta v_{M+1} = \frac{I_o D T_s}{C_{M+1}}. \tag{19}$$

Equations (18) and (19) can be used to select the capacitor values in a given voltage ripple.

B. Voltage Stress of Power Switches

The drain-source voltages of S_{na} and S_{nb} are represented by v_{DSna} and v_{DSnb}, respectively. According to the previous analysis, $S_{(n+1)a}$ must be in ON-state when S_{na} is in OFF-state. No matter if S_{na} is in OFF-state or in ON-state v_{DSna} is actually equal to $v_{n+1} - v_n$ ($n = 2, 3, \ldots, M$). Therefore, v_{DSna} can be expressed as

$$v_{DSna} = \begin{cases} 0, & S_{na} = 1 \ \& \ n = 1, 2, 3, ..., M \\ v_{n+1}, & S_{na} = 0 \ \& \ n = 1 \\ v_{n+1} - v_n, & S_{na} = 0 \ \& \ n = 2, 3, ..., M. \end{cases} \tag{20}$$

For S_{nb}, the expression of v_{DSnb} can be described by

$$v_{DSnb} = \begin{cases} 0, & S_{nb} = 1 \quad \& \ n = 1, 2, 3, ..., M \\ v_{n+1}, & S_{nb} = 0, S_{(n+1)a} = 1 \ \& \ n = 1 \\ v_{n+1} - v_n, & S_{nb} = 0, S_{(n+1)a} = 1 \ \& \ n = 2, 3, ..., M \\ v_{n+2}, & S_{nb} = 0, S_{(n+1)a} = 0 \ \& \ n = 1 \\ v_{n+2} - v_n, & S_{nb} = 0, S_{(n+1)a} = 0 \ \& \ n = 2, 3, ..., M-1. \end{cases} \tag{21}$$

From (17), v_{DSna_max} and v_{DSnb_max} can be calculated by, respectively,

$$v_{DSna\_max} = \begin{cases} \dfrac{V_{\mathrm{g}}}{1-D} + \dfrac{I_o T_s}{2C_{n+1}}, & n = 1 \\ \dfrac{V_{\mathrm{g}}}{1-D} + \dfrac{I_o T_s}{2} \dfrac{C_n + C_{n+1}}{C_n C_{n+1}}, & n = 2, 3, ..., M. \end{cases} \tag{22}$$

$$v_{DSnb\_max} = \begin{cases} \dfrac{2V_{\mathrm{g}}}{1-D} + \dfrac{I_o T_s}{2C_{n+2}}, & n = 1 \\ \dfrac{2V_{\mathrm{g}}}{1-D} + \dfrac{I_o T_s}{2} \dfrac{C_n + C_{n+2}}{C_n C_{n+2}}, & n = 2, 3, ..., M-1 \\ \dfrac{V_{\mathrm{g}}}{1-D} + \dfrac{I_o T_s}{2} \dfrac{C_n + C_{n+1}}{C_n C_{n+1}}, & n = M. \end{cases} \tag{23}$$

C. Current Stress of Power Switches

The steady-state minimum and maximum currents of L_n are represented by I_{Ln_min} and I_{Ln_max}, respectively. And I_{Ln_min} and I_{Ln_max} can be expressed as

$$\begin{cases} I_{Ln\_min} = I_{Ln} - \dfrac{V_{\mathrm{g}}}{2L_n} DT_s = \dfrac{I_o}{1-D} - \dfrac{V_{\mathrm{g}}}{2L_n} DT_s \\ I_{Ln\_max} = I_{Ln} + \dfrac{V_{\mathrm{g}}}{2L_n} DT_s = \dfrac{I_o}{1-D} + \dfrac{V_{\mathrm{g}}}{2L_n} DT_s \end{cases} \tag{24}$$

where $n = 1, 2, 3, \ldots, M$.

Thus, the maximum value of i_{S1a} can be obtained as

$$i_{S1a\_max} = I_{L1} + \frac{V_{\mathrm{g}}}{2L_1} DT_s = \frac{I_o}{1-D} + \frac{V_{\mathrm{g}}}{2L_1} DT_s. \tag{25}$$

When L_n is equal to L_{n-1}, i_{Sna} can be expressed into (26), and i_{Sna_max} can be obtained:

$$i_{Sna\_max} = \begin{cases} \dfrac{I_o}{1-D} + \dfrac{V_{\mathrm{g}}}{2L_1} DT_s, & n = 1 \\ \dfrac{2I_o}{1-D} + \dfrac{V_{\mathrm{g}}}{L_n} \left(DT_s - \dfrac{\varphi_{n(n-1)} T_s}{2\pi} \right), & n = 2, 3, ..., M. \end{cases} \tag{27}$$

For the power switches S_{nb}, similarly, i_{Snb_max} can be given as

$$i_{Snb\_max} = \frac{I_o}{1-D} + \frac{V_{\mathrm{g}}}{2L_n} DT_s, \quad n=1, 2, 3, ..., M. \tag{28}$$

D. Performance Comparisons

Table I shows the comparison results, including the conversion ratio and normalized voltage and current stresses of both active and passive switches between the proposed control strategy and that in [38] and [40].

For the comparison convenience, the voltage stresses are expressed by their calculation formulas. Although the duty ratio range for the EDR converter under the current sharing in [40] is the same as the proposed control, this fixed phase-shift control strategy with 180° is more suitable for two-phase EDR converters. If the 180° phase-shift one is extended to multi-phase EDR converter, the input ripple will be larger than that of other phase shift angles. As can be seen from Table I, the EDR boost

$$i_{Sna} = \begin{cases} i_{Sna1} = \dfrac{I_o}{1-D} - \dfrac{V_{\mathrm{g}}}{2L_n} DT_s + \dfrac{V_{\mathrm{g}}}{L_n} t, & 0 < t \le DT_s - \dfrac{\varphi_{n(n-1)} T_s}{2\pi} \\ i_{Sna2} = \dfrac{2I_o}{1-D_s} + \dfrac{1-2D}{1-D} \dfrac{V_{\mathrm{g}}}{L_n} t - \dfrac{DV_{\mathrm{g}}}{(1-D)L_n} \left(\dfrac{\varphi_{n(n-1)} T_s}{2\pi} - DT_s \right), & DT_s - \dfrac{\varphi_{n(n-1)} T_s}{2\pi} < t \le T_s - \dfrac{\varphi_{n(n-1)} T_s}{2\pi} \ \& \ n = 2, 3, ..., M. \\ i_{Sna3} = \dfrac{I_o}{1-D} - \dfrac{V_{\mathrm{g}}}{2L_n} DT_s + \dfrac{V_{\mathrm{g}}}{L_n} t, & T_s - \dfrac{\varphi_{n(n-1)} T_s}{2\pi} < t \le DT_s \end{cases} \tag{26}$$

TABLE I
COMPARISONS BETWEEN THE PROPOSED CONTROL STRATEGY AND OTHER PHASE-SHIFT APPROACHES IN [38] AND [40]

Object	Conventional control in [38]			Control in [40]	Proposed control
Duty ratio	0~1/3	1/3~2/3	2/3~1	1/2~1	1/2~1
Phase	3			3	M
Voltage gain	$\frac{1}{(1-D)^3}$	$\frac{2D^2-4D+19/9}{(1-D)^3}$	$\frac{3}{1-D}$	$\frac{3}{1-D}$	$\frac{M}{1-D}$
Voltage stress on switching	$v_{DSna(b)\_max}=\begin{cases}\frac{V_g}{(1-D)^3}, n=1\\ \frac{V_g}{(1-D)^2}, n=2\\ \frac{V_g}{1-D}, n=3.\end{cases}$	$v_{DSna(b)\_max}=\begin{cases}\frac{V_g\left(D^2-2D+10/9\right)}{(1-D)^3}, n=1\\ \frac{V_g\left(D^2-7D/3+4/3\right)}{(1-D)^3}, n=2\\ \frac{V_g\left((D^2-2D+1\right)}{(1-D)^3}, n=3.\end{cases}$	$v_{DSna\_max}=\frac{V_g}{1-D}, n=1,2,3$ $v_{DSnb\_max}=\begin{cases}\frac{2V_g}{1-D}, n=1,2\\ \frac{V_g}{1-D}, n=3.\end{cases}$	$v_{DSna\_max}=\frac{V_g}{1-D}, n=1,2,3$ $v_{DSnb\_max}=\begin{cases}\frac{2V_g}{1-D}, n=1,2\\ \frac{V_g}{1-D}, n=3.\end{cases}$	$v_{DSna\_max}=\begin{cases}\frac{V_g}{1-D}+\frac{I_oT_s}{2C_{n+1}}, & n=1\\ \frac{V_g}{1-D}+\frac{I_oT_s}{2}\frac{C_n+C_{n+1}}{C_nC_{n+1}}, & n=2,3,\ldots,M\end{cases}$ $v_{DSnb\_max}=\begin{cases}\frac{2V_g}{1-D}+\frac{I_oT_s}{2C_{n+2}}, & n=1\\ \frac{2V_g}{1-D}+\frac{I_oT_s}{2}\left(\frac{1}{C_{n+2}}+\frac{1}{C_n}\right), & n=2,3,\ldots,M-1\\ \frac{V_g}{1-D}+\frac{I_oT_s}{2}\left(\frac{1}{C_{n+1}}+\frac{1}{C_n}\right), & n=M.\end{cases}$
Current stress on switching	---		$i_{Sna\_max}=\begin{cases}\frac{I_o}{1-D}, n=1\\ \frac{2I_o}{1-D}, n=2,3,\ldots,M\end{cases}$ $i_{Snb\_max}=\frac{I_o}{1-D}, n=1,2,3,\ldots,M.$	$i_{Sna\_max}=\begin{cases}\frac{I_o}{1-D}, n=1\\ \frac{2I_o}{1-D}, n=2,3,\ldots,M\end{cases}$ $i_{Snb\_max}=\frac{I_o}{1-D}, n=1,2,3,\ldots,M.$	$i_{Sna\_max}=\begin{cases}\frac{I_o}{1-D}+\frac{V_g}{2L_1}DT_s, & n=1\\ \frac{2I_o}{1-D}+\frac{V_g}{L_n}\left(DT_s-\frac{\varphi_{n(n-1)}T_s}{2\pi}\right), & n=2,3,\ldots,M\end{cases}$ $i_{Snb\_max}=\frac{I_o}{1-D}+\frac{V_g}{2L_n}DT_s, n=1,2,3,\ldots,M.$
Input ripple currents	Small			Large	Medium
Operating mode	CCM			CCM	CCM
Current sharing	No		Yes	Yes	Yes
Topology	EDR Boost				

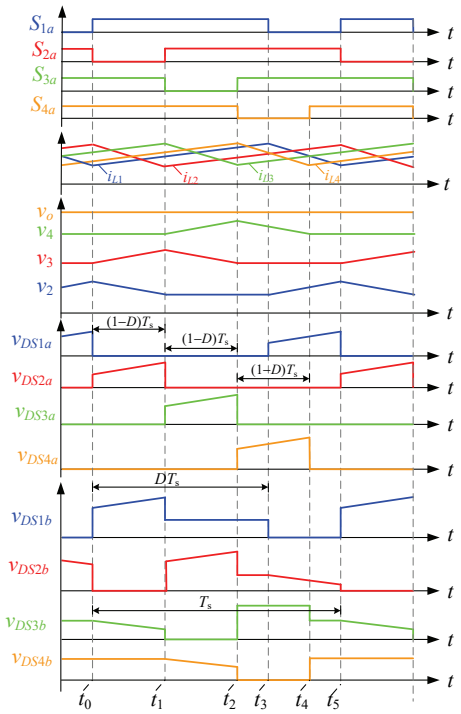


Fig. 5. Key waveforms of the four-phase EDR boost converter

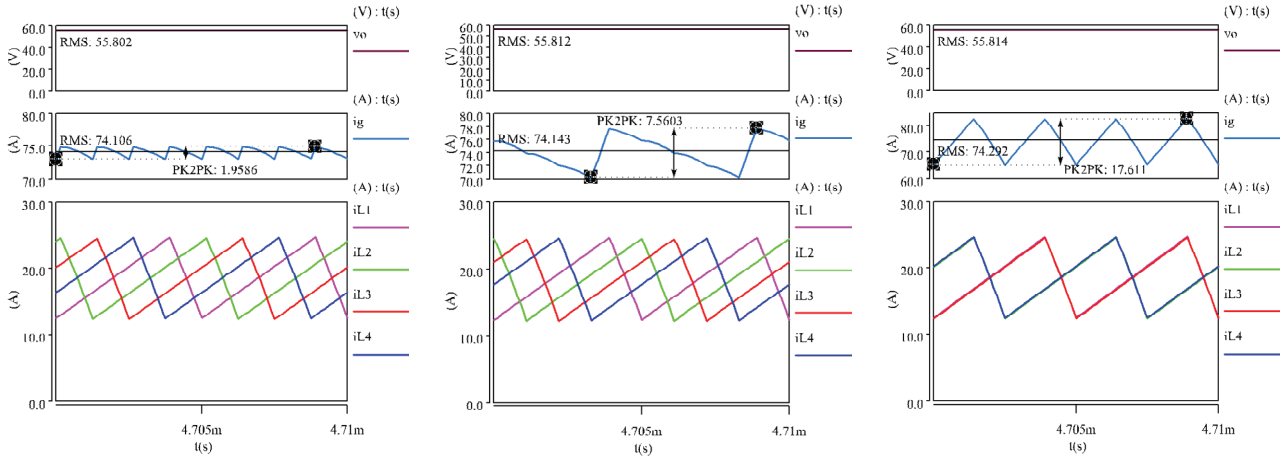
converter with the proposed control strategy can achieve the current sharing in a wider duty ratio range than that of [38]. Therefore, the proposed converter is more suitable for low-voltage and high-current applications with a high step-up conversion ratio. It can be also seen from Table I that voltage stress of power devices with the propose control strategy is different from that in [38]. As the diodes of the converter in [38] are replaced with synchronous rectifiers, it is expected that the proposed synchronous EDR boost converter can achieve a higher conversion efficiency. In addition, the converter can only work in continuous conduction mode (CCM) because all switches are bidirectional conducting devices. Unfortunately, since the proposed converter is not strictly interleaved by the number of phases, its input ripple current will be slightly larger than that of [38].

TABLE II
OPERATING MODES OF THE FOUR-PHASE EDR BOOST CONVERTER

Mode	Time Interval	$S_{1a}S_{2a}S_{3a}S_{4a}$	Charging	Discharging
1	t_0–t_1	1011	L_1, L_3, L_4, C_3	L_2, C_2, C_5
2	t_1–t_2	1101	L_1, L_2, L_4, C_4	L_3, C_3, C_5
3	t_2–t_3	1110	L_1, L_2, L_3, C_5	L_4, C_4
4	t_3–t_4	0110	L_2, L_3, C_2, C_5	L_1, L_4, C_4
5	t_5–t_6	0111	L_2, L_3, L_4, C_2	L_1, C_5

E. Operation Principle of Four-Phase EDR Boost

In order to facilitate the analysis of the operating principle of the converter, a four-phase EDR converter is taken as an example. Key waveforms of the four-phase EDR boost converter, including the gate switching sequence, inductor currents, and switched capacitor voltages, are given in Fig. 5. When D varies in the range of $0.5 \le D < 1$ and $\varphi_{(n+1)n}$ ($n = 1, 2, 3, \ldots, M-1$) is satisfied with $2\pi(1-D) \le \varphi_{(n+1)n} \le 2\pi D$, there are a total of



(a) (b) (c)

Fig. 6. Simulation waveform of the input ripple currents for the four-phase EDR boost converter. (a) the conventional phase shift (b) the proposed control strategy. (c) 180° phase shift.

TABLE III
SIMULATION RESULTS AND COMPARISON FOR THE INPUT RIPPLE CURRENTS

Cases	Phase	D	V_g(V)	I_{rms}(A)	Input current peak-to-peak(A)	I_o(A)	V_o(V)	P_{in}(W)	P_{out}(W)
(A)	0.5π	0.78	3.3	74.106	1.9586	4	55.802	244.55	223.21
(B)	0.44π	0.78	3.3	74.143	7.5603	4	55.812	244.67	223.25
(C)	π	0.78	3.3	74.292	17.611	4	55.814	245.16	223.26

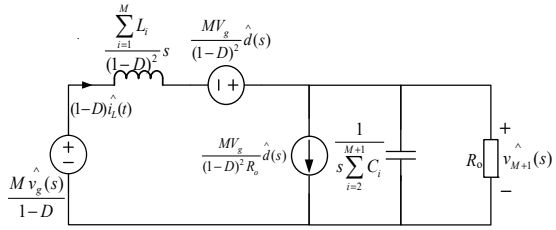


Fig. 7. The small-signal model for the multi-phase EDR-Boost converter.

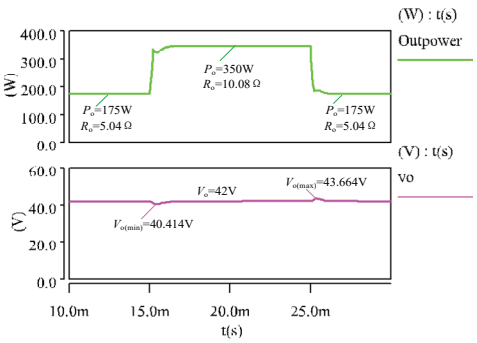


Fig. 8. The closed-loop simulation waveform for output voltage in Saber.

eight following combinations in one switching period T_s. There are only five ones in one switching period T_s when D varies from 2/3 to 3/4 and its phase shift is equal to $2\pi(1-D)$.

Table II shows the operating modes of the four-phase EDR converter. It's defined that the ON-state of the lower switches S_{1a}, S_{2a}, S_{3a}, and S_{4a} are represented by "1". Conversely, "0" is the OFF-state of the lower switches S_{1a}, S_{2a}, S_{3a}, and S_{4a}. Therefore, $S_{1a}S_{2a}S_{3a}S_{4a}$ = 1111 represents that S_{1a}, S_{2a}, S_{3a}, and S_{4a} are all in ON-state, and $S_{1a}S_{2a}S_{3a}S_{4a}$ = 0000 means that S_{1a}, S_{2a}, S_{3a}, and S_{4a} are all in OFF-state. Besides, the pair of switches (S_{na}, S_{nb},) operate in complementary conduction. The operating details for the converter are not described here.

IV. SIMULATION OF INPUT RIPPLE CURRENTS AND DYNAMIC LOAD BEHAVIOR

Different phase-shift control strategies for the multi-phase EDR boost converter will result in different input current ripples. When the average input currents of converters with different phase-shift control strategies are the same, the RMS value I_{rms} of input current for the converter with larger current ripple will be larger. Furthermore, if the input port line resistance R_g is constant, the higher RMS value of the input current will cause the lower converter efficiency. To better illustrate this aspect, taking the four-phase EDR boost converter as an example, simulation verifications among the conventional phase shift (i.e., completely interleaved) (case A), the proposed control strategy (case B) and 180° phase shift (case C) presented in [40] are carried out under the same conditions in Saber. Fig.6 shows the simulation waveforms of the four-phase EDR boost under three different strategies. The simulation parameters and results are listed in the Table III.

From Fig.6, it can be observed that peak-to-peak values of the input current ripples in case A, B and C are respectively about 2 amps, 7.5 amps, and 17.6 amps. Obviously, among these three cases, the input current ripple in case A is the smallest, case B is medium, and case C is the largest. Similar conclusions apply to the RMS values of the input currents in the three cases. Finally, the above simulation results are consistent with the theoretical analysis in the previous Section.

Additionally, in order to show the dynamic performance under the proposed control method, the small signal model for multi-phase EDR-Boost converter has been established as shown in Fig. 7, and, the closed-loop verification of the

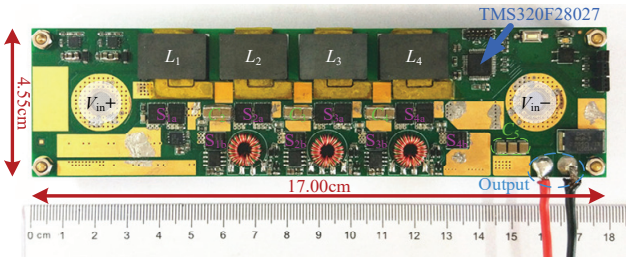


Fig. 9. Hardware of established prototype.

four-phase converter is performed based on the simulation model. The dynamic characteristics with the proposed control method are shown in Fig. 8 under the close-loop control. It can be seen from Fig. 8 that the output voltage is stable when the output power is changed from the half load (P_o=175W) to full load (P_o=350W).

V. Prototype and Experimental Verification

A. Hardware Prototype

A 300 W digital-controlled experimental prototype, as shown in Fig. 9, has been built to validate the above analysis of the proposed control strategy. The parameters and selected component details are summarized in Table IV. For the inductors, the winding is wound inside the PCB, and ER20 is used as the core. TI DSP TMS320F28027 is implemented as a system controller to produce the PWM signals with the switching frequency of 200 *k*Hz. The capacitors C_2, C_3 and C_4 are all made up of nine 2.2 μF ceramic capacitors in parallel. The output capacitor C_5 is composed of eighteen 22 μF electrolytic capacitors in parallel plus three 2.2 μF ceramic capacitors in parallel.

It is worth noting that it is quite difficult to directly measure the phase current of the converter with a current probe because the entire circuit uses a compact PCB integrated design. In addition, it is generally not recommended to measure it by a current probe because the input current value in the experiment is up to nearly 100 A. However, the magnitudes for the phase currents (i_{L1}, i_{L2}, i_{L3} and i_{L4}) can be indirectly reflected by the lengths of charging and discharging time for C_2, C_3 and C_4 during one switching period. According to the principle of capacitor charge balance and (16), it is concluded that the average currents of each phase is all the same (i.e. $I_{L1} = I_{L2} = I_{L3} = I_{L4}$) as long as the lengths of charging time and discharging time for C_2, C_3 and C_4 are all equal.

B. Experimental Verification

In this experiment, the input source is substituted with a lithium battery, whose output voltage (about 3.3 V) is used as the input of the converter. The total output power is set at 300 W. In order to verify the effectiveness of the proposed control scheme, the variable phase-shift experiments are performed on the converter in four cases, where the first and second cases are at D=0.6, and the third and fourth cases are at and D=0.7. Fig. 10 shows the voltage waveforms of the gate switching sequences for S_{1a}, S_{2a}, S_{3a} and S_{4a} in the four cases. Specifically,

TABLE IV
Converter Specification and Component Details

Parameter	Value
Input voltage V_g	3.3 V
Output voltage V_o	24 V to 40 V
Output current I_o	6 A to 8 A
Maximum output power P_o	300 W
Switching frequency f_s	200 kHz
Duty ratio D	0.5 to 0.8
Inductors L_1, L_2, L_3, L_4	Inductance 1.2μH; Core ER20; Air gap 1 mm, turns 3;
Capacitors C_2, C_3, C_4	9 × 2.2-μF/100 V ceramic capacitors
Output capacitor C_5	18 × 22-μF/63 V electrolytic capacitors, 3 × 2.2-μF/100 V ceramic capacitors
Lower switches S_{1a}, S_{2a}, S_{3a}, S_{4a}	SIR182DP 60 V/117 A
Upper switches S_{1b}, S_{2b}, S_{3b}, S_{4b}	BSC040N10NS5 100 V/100 A

Figs. 10(a), (b), (c), and (d) respectively illustrate the waveforms of the converter operating at D=0.6 & $\varphi_{21}=\varphi_{32}=\varphi_{43}=0.8\pi$, D=0.6 & $\varphi_{21}=0.8\pi$ $\varphi_{32}=\varphi_{43}=1.2\pi$, D=0.7 & $\varphi_{21}=\varphi_{32}=\varphi_{43}=0.6\pi$, and D=0.7 & $\varphi_{21}=0.6\pi$ $\varphi_{32}=\varphi_{43}=1.4\pi$, respectively.

Fig. 11 shows the voltages across C_2, C_3, C_4 and C_5 in the four cases. From Fig. 11, it can be seen that no matter the duty ratio is equal to 0.6 or equal to 0.7, the charging times and discharging times for C_2, C_3, and C_4 are almost the same. When the duty ratios are 0.6 and 0.7, respectively, the corresponding time lengths are 2 μs and 1.5 μs, respectively. This indicates the average current for each phase is all equal in the two duty ratios. When the duty ratios are the same, the maximum and minimum voltages across C_2, C_3, and C_4 are almost equal, and the values calculated according to (17) are consistent with the experimental results.

Fig. 12 shows the waveforms of input voltage and output voltage in the four cases. From Fig. 12, it can be seen that the converter has the same voltage gain as long as it operates at the same duty ratio, regardless of the phase shifts. The experimental results are basically consistent with that calculated by equation (15). The drain-source voltages of S_{1a}–S_{4a}, and S_{1b}–S_{4b} have been illustrated in Fig. 13. From Fig. 13(a)–(d), it can be observed that the maximum voltages across power switch S_{1a}–S_{4a} are 13.2 V, 15.5 V, 15.5 V and 13.9 V respectively. Similarly, the maximum voltages across power switch S_{1b}–S_{4b} are 23.4 V, 25.5 V, 22.9 V and 12.7 V from Fig. 13(e)-(h), respectively. The maximum voltage stress of all switches doesn't exceed 30 V, which is less than the output voltage. The experimental results of the voltage stresses of all switches are consistent with the analysis in Section III.

C. Efficiency Analysis

Fig. 14 illustrates the loss breakdown of power devices in the prototype when D is 0.7 and the load is 300 W. From Fig. 14, it can be observed that: 1) the conduction losses are the dominant losses come from, which mainly include the switch conduction loss, DC bus conduction loss, the copper loss of the inductors, and the ESR loss of the capacitors, and 2) the switching loss and the core loss are relatively small, occupying only a small proportion of the total loss. It needs to be mentioned that the losses of the capacitors can't be negligible in low-voltage and high-current applications.

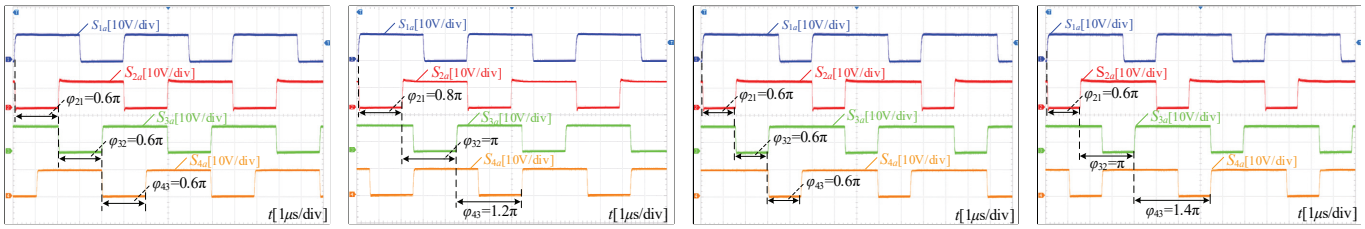


Fig. 10. Experimental waveforms of gate driving voltages for the switches S_{1a}, S_{2a}, S_{3a} and S_{4a}. (a) D = 0.6, φ_{21} = φ_{32} = φ_{43} = 0.8π. (b) D = 0.6, φ_{21} = 0.8π, φ_{32} = π, φ_{43} = 1.2π. (c) D = 0.7, φ_{21} = φ_{32} = φ_{43} = 0.6π. (d) D = 0.7, φ_{21} = 0.6π, φ_{32} = π, φ_{43} = 1.4π.

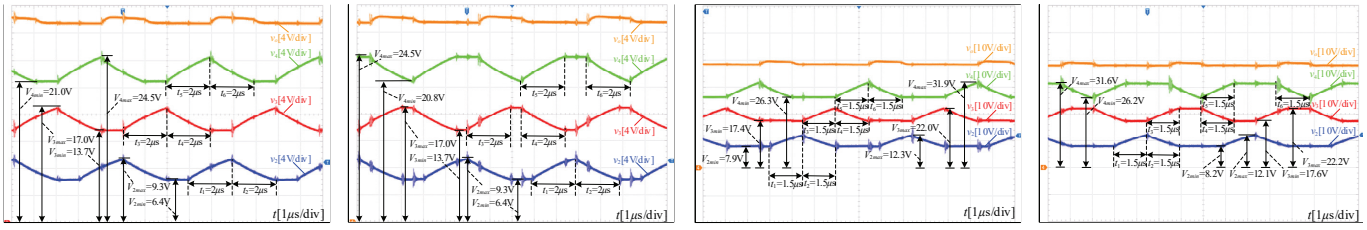


Fig. 11. Experimental waveforms of the capacitor voltages v_2, v_3 and v_4 and output voltage vo. (a) D = 0.6, φ_{21} = φ_{32} = φ_{43} = 0.8π. (b) D = 0.6, φ_{21} = 0.8π, φ_{32} = π, φ_{43} = 1.2π. (c) D = 0.7, φ_{21} = φ_{32} = φ_{43} = 0.6π. (d) D = 0.7, φ_{21} = 0.6π, φ_{32} = π, φ_{43} = 1.4π.

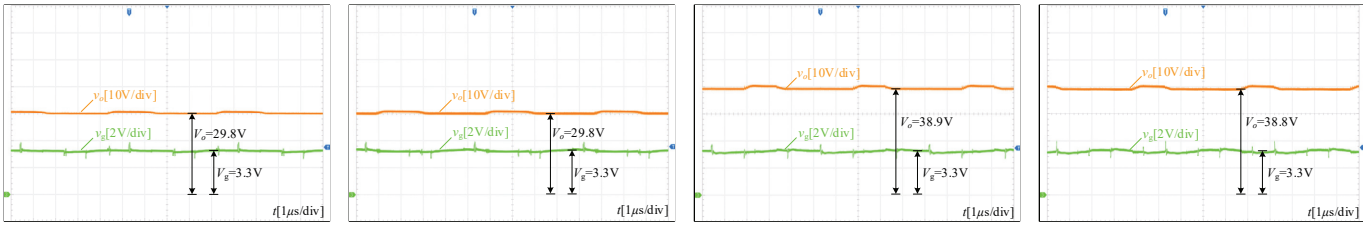


Fig. 12. Experimental waveforms of input voltage v_g and output voltage v_o. (a) D = 0.6, φ_{21} = φ_{32} = φ_{43} = 0.8π. (b) D = 0.6, φ_{21} = 0.8π, φ_{32} = π, φ_{43} = 1.2π. (c) D = 0.7, φ_{21} = φ_{32} = φ_{43} = 0.6π. (d) D = 0.7, φ_{21} = 0.6π, φ_{32} = π, φ_{43} = 1.4π.

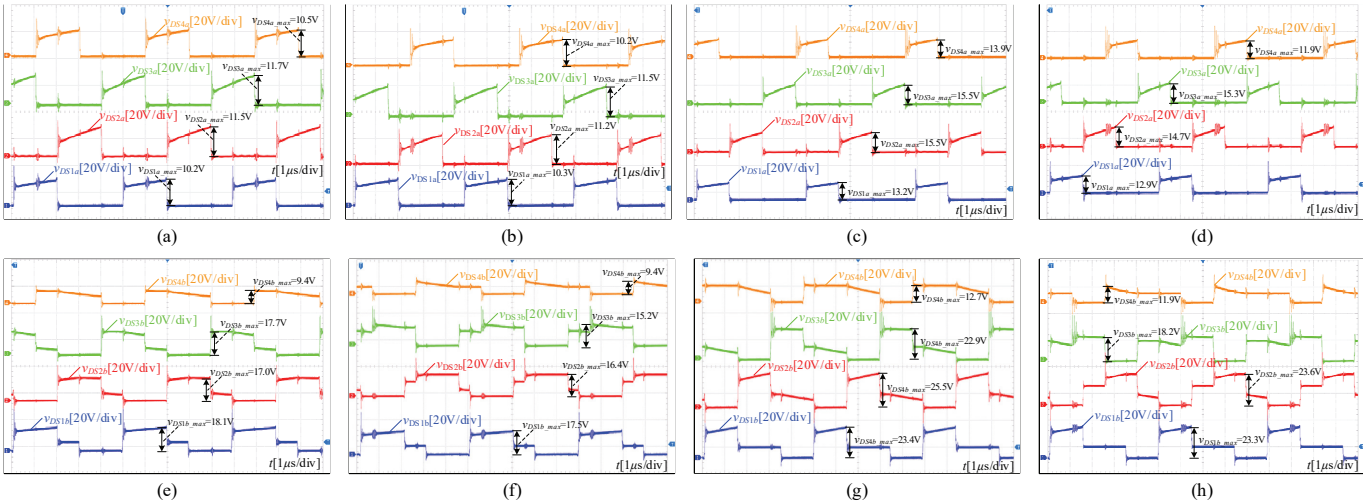


Fig. 13. Experimental waveforms of drain-source voltages for the power switches. (a) D = 0.6, φ_{21} = φ_{32} = φ_{43} = 0.8π. (b) D = 0.6, φ_{21} = 0.8π, φ_{32} = π, φ_{43} = 1.2π. (c) D = 0.7, φ_{21} = φ_{32} = φ_{43} = 0.6π. (d) D = 0.7, φ_{21} = 0.6π, φ_{32} = π, φ_{43} = 1.4π. (e) D = 0.6, φ_{21} = φ_{32} = φ_{43} = 0.8π. (f) D = 0.6, φ_{21} = 0.8π, φ_{32} = π, φ_{43} = 1.2π. (g) D = 0.7, φ_{21} = φ_{32} = φ_{43} = 0.6π. (h) D = 0.7, φ_{21} = 0.6π, φ_{32} = π, φ_{43} = 1.4π.

Fig. 15 shows measured efficiency curves of the prototype for the four-phase EDR boost converter, where Fig. 15(a) and (b) respectively means the experimental efficiencies with various output power and with various duty ratios. From Fig. 15(a), it can be seen that the peak efficiency of the converter is close to 96% when the load power is about 100 W, and the efficiencies are greater than 90% at 300 W. In low-voltage and high-current applications, due to the large conduction losses, the efficiency of the converter decreases rapidly with increasing power. It can be also observed from Fig. 15(b) that the efficiency of the EDR boost converter would become lower with the increasing of the duty cycle under a constant output current (6A). This conclusion is similar to that of the conventional boost converter.

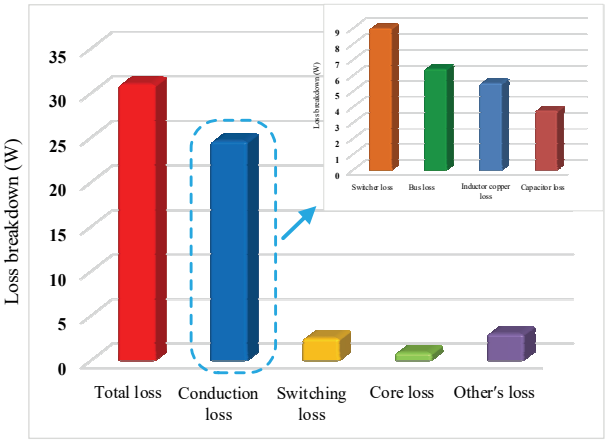


Fig. 14. Loss breakdown of the prototype at 300 W.

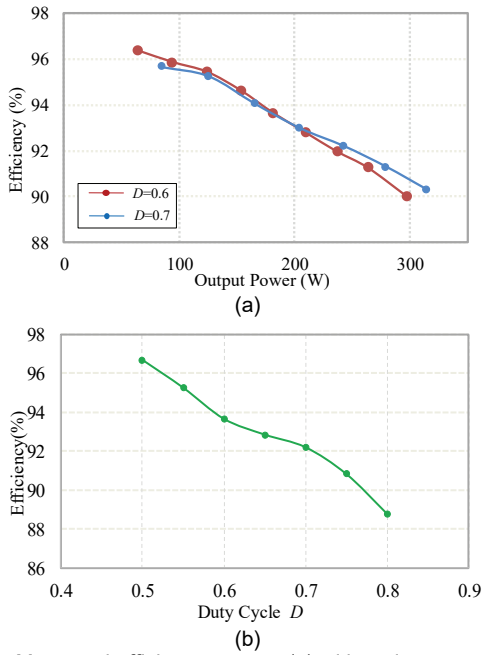


Fig. 15. Measured efficiency curves. (a) with various output power (b) with various duty ratios.

VI. Conclusion

In this paper, a variable phase-shift control strategy is proposed to operate in a wide duty ratio range with current sharing for the multiphase EDR boost converter in high current applications. The control strategy is simple and flexible as the converter is operating with the same duty ratio for each phase and without current sensors. Moreover, the range of the current sharing is not limited to the phase number of the converter. Under the proposed control strategy, the EDR boost converter can operate in wide duty ratio varying from 0.5 to 1 with automatic current sharing among phases, which only requires the phase shift $\varphi_{(n+1)n}$ to satisfy with $2\pi(1-D) \le \varphi_{(n+1)n} \le 2\pi D$. Besides, the output/input voltage gain, the switch device's voltage and current stresses of the converter are analyzed in detail. Finally, a 300 W, low-voltage input/high-voltage output, four-phase interleaved laboratory prototype has been built. The experimental results verify the validity of the proposed control strategy and related analysis for the converter.

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