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Single Phase Step-up Switched-Capacitor Based Multilevel Inverter Topology with SHEPWM

Marif Daula Siddique[1], *Student Member, IEEE,* Saad Mekhilef[2,3,*] *Senior Member, IEEE,* Sanjeevikumar Padmanaban[4], *Senior Member, IEEE*, Mudasir Ahmed Memon[2], and Chandan Kumar[5] , *Senior Member, IEEE*

[1] Department of Electrical Engineering, Qatar University, Doha, Qatar
[2] Power Electronics and Renewable Energy Research Laboratory, Department of Electrical Engineering, University of Malaya, 50603 Kuala Lumpur, Malaysia
[3] School of Software and Electrical Engineering, Swinburne University of Technology, Melbourne, Victoria, Australia
[4] Department of Energy Technology, Aalborg University, Esbjerg, Denmark
[5] Department of Electronics and Electrical Engineering, IIT Guwahati, India
Corresponding Author: Saad Mekhilef (saad@.um.edu.my)

***Abstract* -- Multilevel inverter (MLI) topologies play a crucial role in the dc-ac power conversion due to their high-quality performance and efficiency. This paper aims to propose a new switched-capacitor based boost multilevel inverter topology (SCMLI). The proposed topology consists of nine power semiconductor switches with one dc voltage source and two capacitors, capable of generating a nine-level output voltage waveform with twice voltage gain. With the addition of two switches, the proposed topology can be used for higher voltage gain applications. Other features of the proposed topology include self-voltage balancing of capacitors, parallel operation of capacitors, lower voltage stress across the switches, along with inherent polarity changing capability. To obtain the high-quality output waveform, selective harmonic elimination pulse width modulation (SHEPWM) technique is applied. In this technique, the detrimental low-order harmonics can easily be regulated and eliminated from the output voltage of MLI. The proposed topology is compared with the recently introduced SCMLI topologies considering various parameters to set the benchmark of the proposed topology. The performance of the proposed MLI is investigated through various experimental results using a laboratory prototype setup.**

***Index Terms*—Multilevel inverter, switched-capacitor, SHEPWM, boost topology, reduce switch count.**

I. INTRODUCTION

The importance of multilevel inverters (MLIs) has been on the rise owing to their increased industrial applications demand. MLIs enhance the performance of renewable energy systems, unified power flow controllers, and electric vehicles. MLIs can achieve output voltage waveform in a staircase manner with reduced distortion thus enhancing the power quality. The staircase output voltage is obtained by intelligent switching of dc-link voltages and the semiconductor switches. MLIs have some added advantages over conventional two-level inverters such as reduced total harmonic distortion (THD), lower blocking voltage ratings and *dv/dt* rating of switching devices and reduced output filter size [1]–[3]. In the first place, three classical structures of MLIs have been mentioned in the literature. They can be classified as Diode-Clamped MLIs (DC-MLIs), Flying-Capacitor MLIs (FC-MLIs) and Cascaded H-bridge (CHB-MLIs). Nevertheless, conventional MLIs have a wide range of advantages over the two-level inverters. However, each of the three MLIs suffers from similar as well as different limitations. Some of the limitations include increased switch count, large number of dc-link voltage sources and capacitor banks [4]–[9].

Multilevel inverters can be broadly categorized as symmetrical and asymmetrical, depending on the amplitudes of the dc voltage source. The asymmetrical MLI produces a higher number of levels at the output while using the same number of components and dc voltage sources as compared to its symmetrical counterpart. Nevertheless, asymmetrical MLI topologies require several isolated dc voltage sources with different magnitudes, making them impractical.

The advancement of topologies for the multilevel output has a significant focus on the reduction of the number of components. The availability of dc voltage sources has been a critical concern for these topologies. Therefore, the dc voltage sources have been replaced by capacitors to create different levels of the input supply. Research-based on single dc voltage source multilevel inverter topologies is gaining further popularity due to its practicability. One such category of multilevel inverters has been the switched-capacitor (SC) based topologies with step-up capabilities. The SC-based MLI topologies produce a higher number of levels at the output while reducing the number of dc power supplies. Capacitors along with power semiconductor devices mitigate the concerns on the power supplies. SC-based topology has found to be well suited for various applications due to its simple structure and practical approach. More recently, several novel MLIs have been presented by researchers with reduced component counts, namely, the required number of power switches, dc power supplies, gate drivers, etc [10]–[13].

The staircase output voltage waveform can be generated from the series and parallel combinations of the input dc voltage source and capacitors with self-voltage balancing competences. Several seven-level topologies have been proposed in [14]–[20] with a voltage gain of 1.5. In these topologies except [20], the number of capacitors is three, whereas in [20], four capacitors are used for seven-level output

voltage. These topology fails to attain the peak voltage equal to the sum of all capacitor voltages. Furthermore, the loading stress on the capacitors is of different levels, making the voltage balancing more complex. The higher number of capacitors increases the overall cost and losses of the topology. To increase the utilization of the capacitors, some high gain topologies have been proposed in [21]–[25], however, the higher voltage gain is achieved by using a higher number of components.

A cascaded switched capacitor MLI topology has been proposed in [26]. The topology has been based on the series /parallel units of a switched capacitor. An H-bridge has been used to produce an ac voltage across the load. In the cascade connection, the required number of isolated dc voltage sources is high, making the topology unrealistic. Another topology based on the SC concept has been presented in [27], which generates nine levels at the output while employing 12 power semiconductor switches with a voltage gain of two. Furthermore, the topologies suggested in [28]–[30] requires a higher switch count.

A topology based on the cross-connected module proposed in [31] requires a higher voltage rating of switches, as the cross-connected switches will have to block twice its input voltage. Furthermore, this topology has a peak voltage equal to the addition of capacitor voltages without including the dc input voltage. If the dc voltage source has been included in the output levels, the resulted voltage levels will be smooth. A new step-up switched capacitor has been suggested in [32]. The recommended topology requires a different set of capacitors which has to be used in both positive and negative levels with different voltage ratings. In [33], a new single-phase topology has been presented based on the switched capacitor. The SC section of the topology generates unipolar voltage and an H-bridge is used to convert the unipolar to bipolar. Use of H-bridge increases the voltage stress which limits its application in high voltage. A K-Type MLI topology based on SC has been suggested in [34]. This topology uses two dc voltage sources with two capacitors to generate 13 levels at the output with the help of 14 switches. Out of 13 levels, the discharging of capacitors occurred in three levels whereas the charging takes place only in the zero states of the output voltage. This results in unbalanced capacitor voltages. Furthermore, topologies suggested in [35]–[37] lacks the boosting ability.

This paper proposed a new configuration of the SC-based multilevel inverter topology which can produce nine-level output voltage along with boosting capability of the input dc voltage source and self-voltage balancing. The SHEPWM control technique is applied to obtain a high-quality output waveform. This is an offline technique used to calculate the optimized switching angles for each modulation index and store in memory as a lookup table. This paper has been structured as: Section II explains the proposed topology with the mathematical formulation. Section III describes the SHEPWM used for the proposed topology. Section IV gives the power loss analysis of the proposed topology, and Section V demonstrates the comparative analysis of the proposed topology with other similar topologies. Section VI presented the different experimental results of the proposed topology with different considerations. This paper ends with the conclusion given in Section VII.

II. PROPOSED TOPOLOGY

A. *Circuit Description of the Proposed nine-level (9L) Topology*

The circuit assembly of the proposed single-phase step-up multilevel inverter topology is shown in Fig. 1 and has been named as [P1]. The assembly of the proposed topology consists of one dc voltage source with magnitude V_{dc} along with two series-connected capacitors. Nine unidirectional switches along with two power diodes are used to connected dc voltage source V_{dc}, capacitors C_1 and C_2 have the same magnitude and load in a different arrangement. Out of nine switches, two have a series connected diode, and the remaining have the diodes in anti-parallel configurations. Two capacitors are used to split the dc voltage sources into equal halves to create different voltage levels. Furthermore, the voltage across both capacitors can be connected in additive polarity with the dc voltage source to boost the output voltage across the load. The proposed topology can produce nine levels (four positive levels, four negative levels, and zero) across the load.

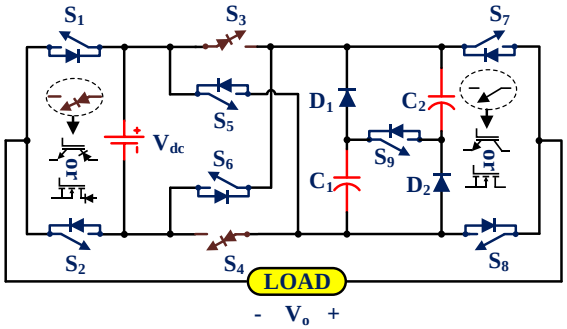

Fig. 1: Proposed switched-capacitor based boost multilevel inverter topology with 9L operation [P1]

B. *Operating Principle*

The different switching states of the proposed topology with the charging and discharging of both capacitors are presented in Table 1.

TABLE I
SWITCHING STATES FOR THE PROPOSED TOPOLOGY WITH 9L OPERATION [P1]

Voltage State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	V_o	C_1	C_2
[+4]	0	1	0	0	1	0	1	0	1	$2V_{dc}$	D	D
[+3]	0	1	0	0	1	0	1	0	0	$1.5V_{dc}$	D	D
[+2]	0	1	1	1	0	0	1	0	1	V_{dc}	C	C
[+1]	1	0	0	0	1	0	1	0	0	$0.5V_{dc}$	D	D
[+0]	1	0	1	1	0	0	1	0	1	zero	C	C
[-0]	0	1	1	1	0	0	0	1	1			
[-1]	0	1	0	0	0	1	0	1	0	$-0.5V_{dc}$	D	D
[-2]	1	0	1	1	0	0	0	1	1	$-V_{dc}$	C	C
[-3]	1	0	0	0	0	1	0	1	0	$-1.5V_{dc}$	D	D
[-4]	1	0	0	0	0	1	0	1	1	$-2V_{dc}$	D	D

Notations: 0/1 = OFF/ON state of the switch, ─ = no change in capacitor voltage, C = charging of capacitor, D = discharging of capacitor

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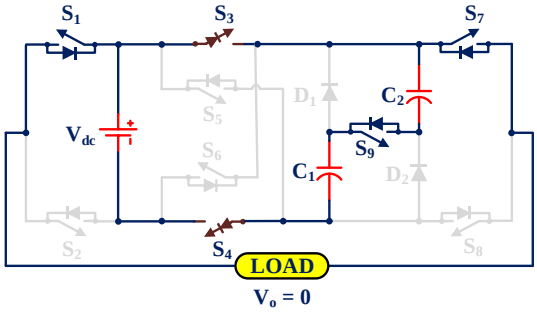
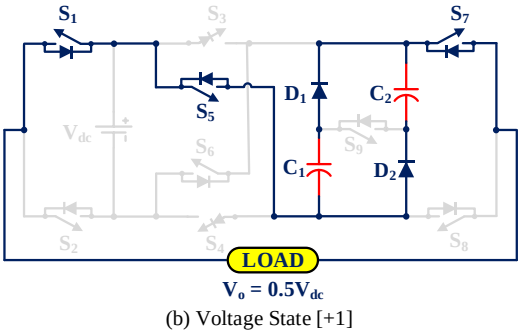
Fig. 2 (a)-(j) shows the different switching combinations of the proposed topology in one fundamental cycle. The explanations of each level in the positive cycle are given below.

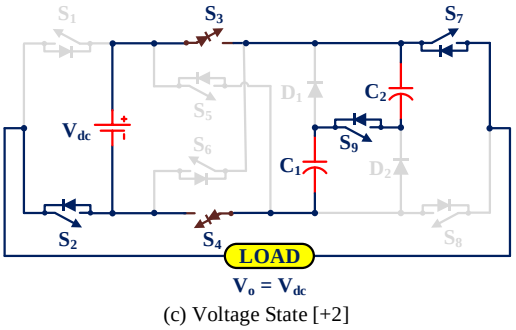
i. *Zero Voltage State [+0]:* Fig. 2 (a) shows the



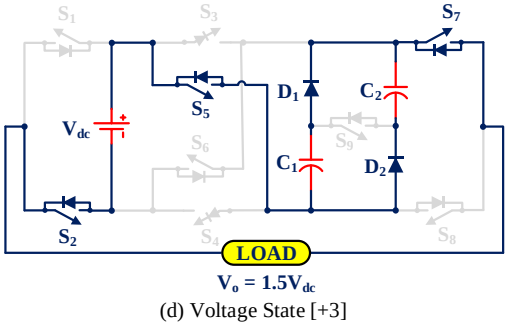
(a) Voltage State [+0]



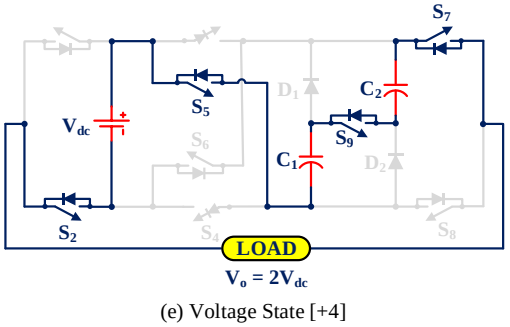
(b) Voltage State [+1]



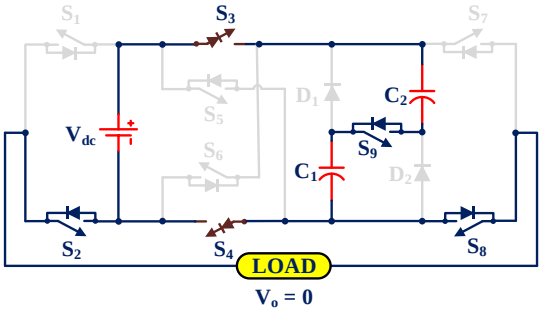
(c) Voltage State [+2]



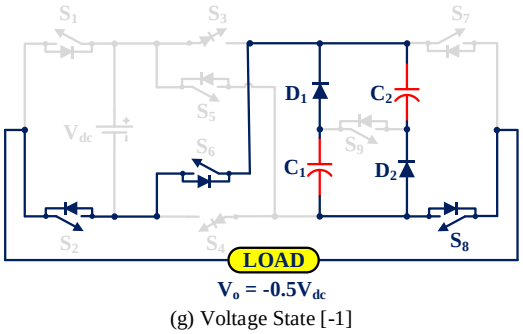
(d) Voltage State [+3]



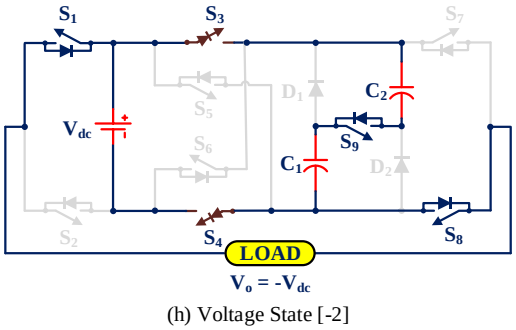
(e) Voltage State [+4]



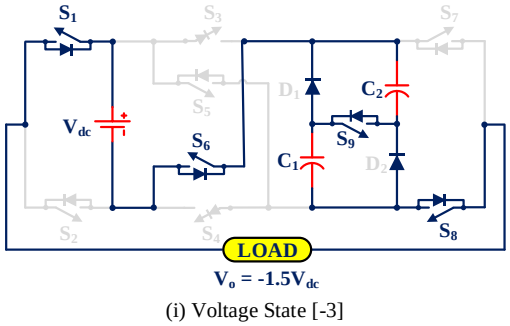
(f) Voltage State [-0]



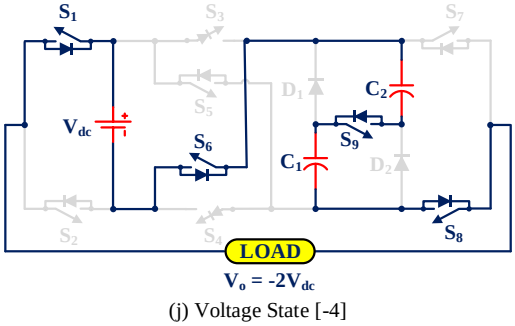
(g) Voltage State [-1]



(h) Voltage State [-2]



(i) Voltage State [-3]



(j) Voltage State [-4]

Fig. 2: Different voltage states of the proposed topology with 9L operation

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switching diagram for the zero voltage across the load. In this state, both capacitors C_1 and C_2 are charged and both capacitors attend a voltage level equal to half of the supply voltage V_{dc} as both capacitors are directly connected to the dc voltage source V_{dc}, i.e. $V_o = 0$, $V_{C1} = 0.5V_{dc}$, and $V_{C2} = 0.5V_{dc}$. V_{C1} and V_{C2} are the capacitor voltages of C_1 and C_2 respectively.

ii. *First Voltage State [+1]:* Fig. 2 (b) shows the switching diagram of the output voltage with a magnitude of $0.5V_{dc}$. This voltage level is generated by connecting both capacitors in parallel to the load and the load current is shared by both capacitors. This voltage level is achieved by turning OFF switches S_3, S_4, and S_9 and turning ON switch S_5.

iii. *Second Voltage State [+2]:* In this voltage state, the dc voltage source is parallel to the load with two capacitors C_1 and C_2, which results in an output voltage of equal to the dc voltage source V_{dc}. The capacitors get charged through dc voltage sources. This state is achieved by turning ON switches S_2-S_4 and turning OFF switches S_1 and S_5. This voltage state has been demonstrated in Fig. 2 (c).

iv. *Third Voltage State [+3]:* From this voltage state as depicted in Fig. 2 (d), the capacitors are used to boost the output voltage across the load. The parallel combination of both capacitors is added with the dc voltage source by turning ON switch S_5 and turning OFF switches S_3, S_4 and S_9 results in $V_o = 1.5V_{dc}$.

v. *Fourth Voltage State [+4]:* As depicted in Fig. 2 (e), in this voltage state, the capacitor voltages V_{C1} and V_{C2} are added with the dc voltage source V_{dc} by releasing the energy stored in both capacitors, results in the boost in the output voltage with $V_o = 2V_{dc}$.

For the negative voltage levels, the mode of operation has been depicted in Fig. 2 (f) – (j). However, the charging and discharging patterns of the capacitors remain the same. Therefore, for one complete cycle, the charging and discharging time for both capacitors become the same. Fig. 3 shows the output voltage with charging and discharging over one complete cycle. and represents the charging and discharging of the capacitors and gives the idea of power flow from dc voltage source V_{dc} to capacitors and load. As

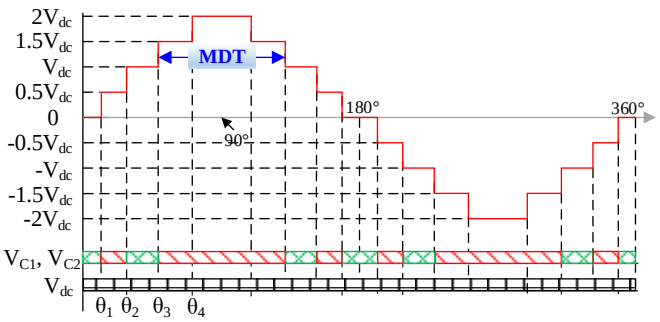

Fig. 3. Capacitors charging and discharging patters in one complete cycle of output voltage.

illustrated in Fig. 3, the pattern of both capacitor voltage is same for a fundamental period of the output voltage. Therefore, the symmetrical operation of both capacitors gives the self-balancing of the capacitor voltage [14].

C. Modifications in the Proposed Topology

One major issue with the proposed topology is the lacking of the inductive load ability. During the voltage levels of $\pm 0.5V_{dc}$ and $\pm 1.5V_{dc}$, the path for the negative current flow is not possible due to the presence of diode in the path. This negative current is due to the highly inductive load connected to the output terminals of the proposed topology. To overcome this problem, either of the diode or both of the didoes, i.e., D_1 or D_2 can be replaced by a unidirectional switch as shown in Fig. 4 and named as [P2]. According to the change in the topology, the modified switching table is given in Table II.

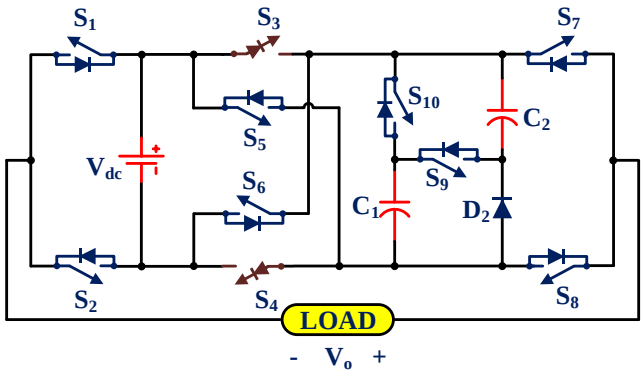

Fig. 4: Modifications in the proposed topology for inductive load ability with 9L operation [P2]

TABLE II
SWITCHING STATE FOR THE PROPOSED TOPOLOGY WITH INDUCTIVE LOAD ABILITY WITH 9L OPERATION [P2]

Voltage State	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	V_o	C_1	C_2
[+4]	0	1	0	0	1	0	1	0	1	0	$2V_{dc}$	D	D
[+3]	0	1	0	0	1	0	1	0	0	1	$1.5V_{dc}$	D	D
[+2]	0	1	1	1	0	0	1	0	1	0	V_{dc}	C	C
[+1]	1	0	0	0	1	0	1	0	0	1	$0.5V_{dc}$	D	D
[+0]	1	0	1	1	0	0	1	0	1	0	zero	C	C
[-0]	0	1	1	1	0	0	0	1	1	0			
[-1]	0	1	0	0	0	1	0	1	0	1	$-0.5V_{dc}$	D	D
[-2]	1	0	1	1	0	0	0	1	1	0	$-V_{dc}$	C	C
[-3]	1	0	0	0	0	1	0	1	0	1	$-1.5V_{dc}$	D	D
[-4]	1	0	0	0	0	1	0	1	1	0	$-2V_{dc}$	D	D

Table III and IV provides the details of voltage and current stresses of different components of the proposed topology, respectively. As the switches S_5 and S_6 are cross-connected switches, the voltage stress is equal to the peak of the output voltage. The remaining switches, i.e., S_1-S_4, S_7, and S_9 are of voltage rating equal to the input voltage. the remaining devices need to block the voltage rating equal to the half of the input voltage. Therefore, the total standing voltage (TSV) which is

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the sum of maximum voltage stress of all the devices becomes $11.5V_{dc}$.

The current rating of the switches is also important. From Table IV, only three switches, i.e., S_3, S_4 and S_9 are in the charging loop of capacitors, thus they need to carry the charging current with the load current. Therefore, these three switches need to be of higher current rating than other switches.

TABLE III
VOLTAGE STRESS ($\times V_{dc}$) OF DIFFERENT DEVICES [P_1, P_2]

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10} / D_1	D_2	V_o
1	0	1	1	0	2	0	1	0	0.5	0.5	$2V_{dc}$
1	0	0.5	1	0	1.5	0	0.5	0.5	0	0	$1.5V_{dc}$
1	0	0	0	1	1	0	1	0	0.5	0.5	V_{dc}
0	1	0.5	1	0	1.5	0	0.5	0.5	0	0	$0.5V_{dc}$
0	1	0	1	1	1	0	1	0	0.5	0.5	Zero
1	0	0	0	1	1	1	0	0	0.5	0.5	
1	0	1	0.5	1.5	0	0.5	0	0.5	0	0	$-0.5V_{dc}$
0	1	0	0	1	1	1	0	0	0.5	0.5	$-V_{dc}$
0	1	1	0.5	1.5	0	0.5	0	0.5	0	0	$-1.5V_{dc}$
0	1	1	1	2	0	1	0	0	0.5	0.5	$-2V_{dc}$

TABLE IV
CURRENT STRESS OF DIFFERENT DEVICES [P_1, P_2]

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10} / D_1	D_2	V_o
0	I_o	0	0	I_o	0	I_o	0	I_o	0	0	$2V_{dc}$
0	I_o	0	0	I_o	0	I_o	0	0	I_o	I_o	$1.5V_{dc}$
0	I_o	I_o+I_c	I_o+I_c	0	0	I_o	0	I_o+I_c	0	0	V_{dc}
I_o	0	0	0	I_o	0	I_o	0	0	I_o	I_o	$0.5V_{dc}$
I_o	0	I_o+I_c	I_o+I_c	0	0	I_o	0	I_o+I_c	0	0	Zero
0	I_o	I_o+I_c	I_o+I_c	0	0	0	I_o	I_o+I_c	0	0	
0	I_o	0	0	0	I_o	0	I_o	0	I_o	I_o	$-0.5V_{dc}$
I_o	0	I_o+I_c	I_o+I_c	0	0	0	I_o	I_o+I_c	0	0	$-V_{dc}$
I_o	0	0	0	0	I_o	0	I_o	0	I_o	I_o	$-1.5V_{dc}$
I_o	0	0	0	0	I_o	0	I_o	I_o	0	0	$-2V_{dc}$

D. Configuration of the Proposed Topology for Higher Voltage Gain

The proposed topology can be operated for higher voltage gain operation. Fig. 5 shows the proposed topology for the seven-level (7L) operation. Both diodes from the proposed 9L topology shown in Fig. 1 has been replaced by the unidirectional switches. The replacement enables the charging of the capacitor up to the voltage equal to the input voltage, i.e., V_{dc}. With the capacitor voltage of V_{dc}, the output voltage levels have a magnitude of zero, $\pm V_{dc}$, $\pm 2V_{dc}$, and $\pm 3V_{dc}$. The peak magnitude of the output voltage is $3V_{dc}$ which reflects has a triple voltage gain of the proposed topology with 7L operation. The switching table for the 7L operation is given in Table V.

Furthermore, for higher voltage gain and number of levels, the topology shown in Fig. 5 can be extended as shown in Fig. 6. In the extension with *N* level output voltage, the number of capacitors is added to the switched capacitor module. The voltage rating of all the capacitors is V_{dc}. The addition of one capacitor is accomplished with the inclusion of three unidirectional switches as shown in Fig. 6. The equations for different parameters for the *N* level topology are as follows:

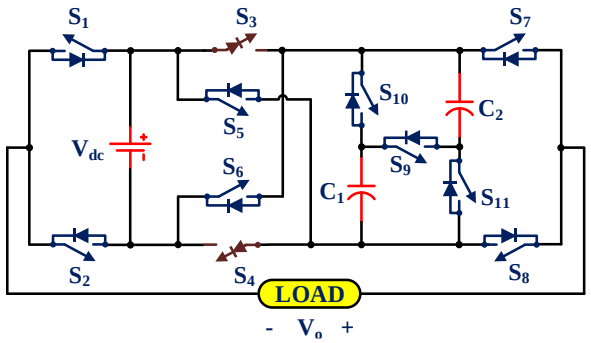

Fig. 5: High gain configuration of the proposed topology with 7L operation

TABLE V
SWITCHING STATES FOR THE PROPOSED 7L TOPOLOGY [P3]

S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	V_o	C_1	C_2
0	1	0	0	1	0	1	0	1	0	0	$3V_{dc}$	D	D
0	1	0	0	1	0	1	0	0	1	1	$2V_{dc}$	D	D
0	1	1	1	0	0	1	0	0	1	1	V_{dc}	C	C
1	0	1	1	0	0	1	0	0	1	1	zero	C	C
0	1	1	1	0	0	0	1	0	1	1			
1	0	1	1	0	0	0	1	0	1	1	$-V_{dc}$	C	C
1	0	0	0	0	1	0	1	0	1	1	$-2V_{dc}$	D	D
1	0	0	0	0	1	0	1	1	0	0	$-3V_{dc}$	D	D

$$\left.\begin{aligned} N_{sw} &= \frac{1}{2}(3N+1) \\ N_C &= \frac{1}{2}(N-3) \\ G &= \frac{1}{2}(N-1) \\ N_{sc} &= N-3 \end{aligned}\right\} \quad (1)$$

where *N*, N_{sw}, N_c, *G*, and N_{sc} signifies the number of levels, number of switches, number of capacitors, voltage gain and number of switches in the charging loop, respectively.

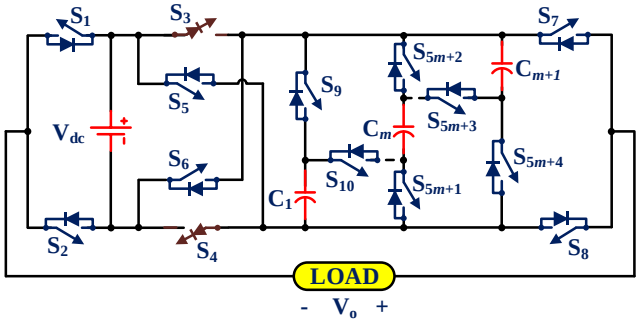

Fig. 6: High gain configuration of the proposed topology with *N* level operation

E. Capacitance Calculation

The proper selection of capacitor value in the SC-MLI is the major challenge in the design of the proposed inverter topology. The optimum selection of capacitor value significantly reduces the ripples in the output voltage. Fig. 3 shows the maximum discharge time (MDT) for the floating capacitor used in the design of the proposed 9L inverter. From the Figure, it is shown that at voltage levels $\pm 1.5V_{dc}$ and $\pm 2V_{in}$, the floating capacitors C_1 and C_2 is discharged. These two voltage levels are centric at 90^0 and 270^0 during the positive and negative half-cycle, respectively. For the discharge angle θ, the capacitor discharges from (90°-0.5θ) to (90°+0.5θ). The capacitance C during the interval of supplied electric change will be calculated using (2).

$$C_1 = C_2 = C = \frac{I_{o,p} \times \cos\left(90^\circ - 0.5\theta\right) \times \cos\phi}{\pi \times f \times \Delta V_C} \tag{2}$$

where $I_{o,p}$, ΔV_c and f denote the peak load current, ripple voltage and output frequency respectively. The ΔV_C and ϕ, denotes the capacitor ripple voltage of the floating capacitor and load power factor angle respectively.

III. MODULATION TECHNIQUE

The output power quality is essential in the design of an MLI. The preferred output voltage is the waveform which is close to sinusoidal, with lower harmonic content. SHEPWM is a fundamental frequency PWM technique that has been widely used for the elimination of lower order harmonics from the output voltage waveform [38], [39]. The Fourier series of the output voltage waveform can be expressed as

$$v_o\left(t\right) = \frac{a_o}{2} + \sum_{i=0}^{n} a_n \cos\left(\frac{2\pi nt}{T}\right) + b_n \sin\left(\frac{2\pi nt}{T}\right) \tag{3}$$

where a_o, a_n, and b_n represents the dc component, even-numbered harmonics, and odd-numbered harmonics component of the output voltage waveform respectively with n being the harmonic order. The output voltage have quarter-wave symmetry, results in a_o, a_n and sine terms of odd harmonics to attain zero value. Therefore, the equation for the output voltage waveform simplifies to:

$$v_o\left(t\right) = \sum_{i=1,3,5,\ldots}^{n} b_n \sin\left(n\alpha_i\right) \tag{4}$$

For a staircase output voltage, b_n can be expressed as

$$b_n = \frac{4V_{dc}}{n\pi} \sum_{\mathrm{i=1,3,5,\ldots}}^{\mathrm{n}} \cos\left(n\alpha_i\right) \tag{5}$$

For the nine-level output voltage waveform as shown in Fig. 3, four switching angles i.e. $\theta_1, \theta_2, \theta_3,$ and θ_4 are required to be calculated. With four switching angles, three harmonic orders can be eliminated from the output voltage waveform. For the proposed topology, 3rd, 5th, and 7th order harmonics are selected for elimination from the output voltage waveform. In SHEPWM technique, firing angles are calculated using (6) by maintaining the relationship $(0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < {}^{\pi}/_{2})$.

$$\left.\begin{aligned} m_a &= \frac{1}{s}\left[\cos\left(\theta_1\right) + \cos\left(\theta_2\right) + \cos\left(\theta_3\right) + \cos\left(\theta_4\right)\right] \\ \cos\left(3\theta_1\right) + \cos\left(3\theta_2\right) + \cos\left(3\theta_3\right) + \cos\left(3\theta_4\right) &= 0 \\ \cos\left(5\theta_1\right) + \cos\left(5\theta_2\right) + \cos\left(5\theta_3\right) + \cos\left(5\theta_4\right) &= 0 \\ \cos\left(7\theta_1\right) + \cos\left(7\theta_2\right) + \cos\left(7\theta_3\right) + \cos\left(7\theta_4\right) &= 0 \end{aligned}\right\} \tag{6}$$

where m_a is given by

$$m_a = \frac{\pi \times V_D}{4 \times S \times V_{dc}} \tag{7}$$

Where, V_D is the required fundamental voltage, S is the number of switching angles and V_{dc} is the nominal dc voltage. In SHEPWM, feasible solutions that eliminate the undesired lower order harmonics are only available for fewer ranges of modulation index. Therefore, the main objective of the SHEPWM technique is to get the fundamental at the desired level for each modulation index with the additional advantage of eliminating the low order harmonics if suitable solutions exist. For the nine-level inverter, 4 optimized switching angles i.e. θ_1, θ_2, θ_3, and θ_4 are calculated using the fitness function given in (8) which satisfies the fundamental at the desired level and eliminates the lower-order harmonics. In this paper, optimized switching angles are calculated using particle swarm optimization (PSO) algorithm discussed in [39].

$$f = min\left[\left|100\frac{V_D - V_1}{V_D}\right|^4 + \sum_{s=2}^{S}\frac{1}{h_s}\left|50\frac{V_{h_s}}{V_1}\right|^2\right] \tag{8}$$

Where h_s is the order of particular harmonic e.g. $h_2 = 3$ and $h_3 = 5$, and V_1 is the fundamental voltage. In PSO, particles are arranged in a ring topology that updates their velocity and position using (9) and (10) respectively.

$$\begin{aligned} v_{i,j}^{t+1} = (v_{i,j}^{t} \times w^{t+1}) &+ \left[c_1 \times r_{1j}^{t} \times (P_{Best,i}^{t} - x_{i,j}^{t})\right] \\ &+ \left[c_2 \times r_{2j}^{t} \times (L_{Best} - x_{i,j}^{t})\right] \end{aligned} \tag{9}$$

$$x_{i,j}^{t+1} = x_{i,j}^{t} + v_{i,j}^{t+1} \tag{10}$$

where L_{Best} is the local best particle among $i+1$, i and $i-1$, $P_{Best,i}^{t}$ is the personal best position of particle and $\mathrm{w}^{\mathrm{t+1}}$ is the inertia weight calculated using (11).

$$\mathrm{w}^{\mathrm{t+1}} = w_{max} - \left(\frac{w_{max} - w_{min}}{Z} \times \text{current iteration}\right) \tag{11}$$

where Z is the total number of iteration.

Table VI contains the values of control parameters selected for the PSO algorithm. Based on the flow chart shown in Fig. 7, the solution for the equations for SHEPWM has been obtained for the modulation index in the range of 0 to 1 at the step size of 0.01. Fig. 8 (a) and (b) shows the variation of optimized switching angles and the magnitude of harmonics concerning the modulation index. From Fig. 8 (b), it is shown that the PSO algorithm calculates the optimized switching angles that eliminate the undesired lower-order harmonics (3rd, 5th, and 7th)

for some regions of modulation index and achieved the fundamental at the desired level for the whole range of modulation index.

TABLE VI
CONTROL PARAMETER VALUE SELECTED FOR PSO

Symbol	Quantity	Values
c_1 , c_2	Acceleration Coefficient	2.0
P	Swarm Size	100
w_{min}	Minimum inertia	0.4
w_{min}	Maximum inertia	0.9
$Iter_{Pmax}$	Maximum number of Iterations	500
β	Initialization of swarm	$0 < \theta_1 < \theta_2 < \theta_3 < \theta_4 < \frac{\pi}{2}$
m_a	Modulation Index	$0 < m_a \leq 1$

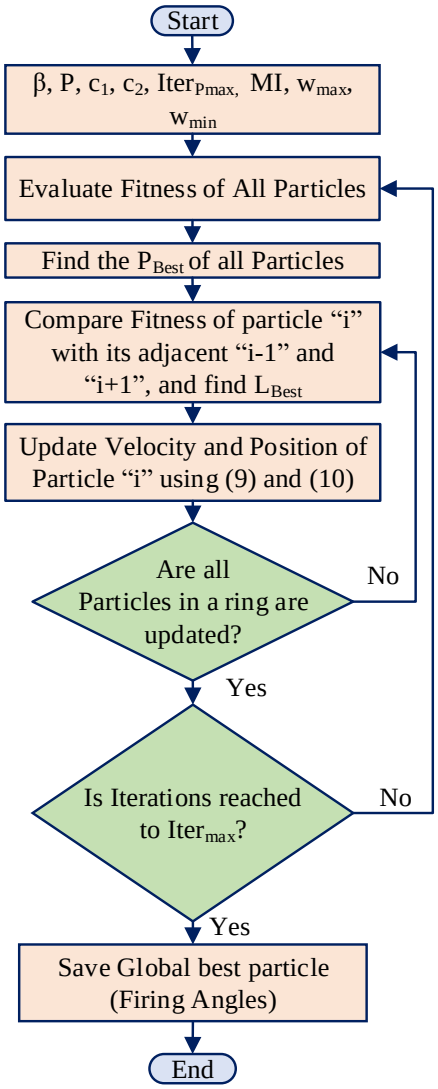

Fig. 7: Flowchart for the solution of SHEPWM

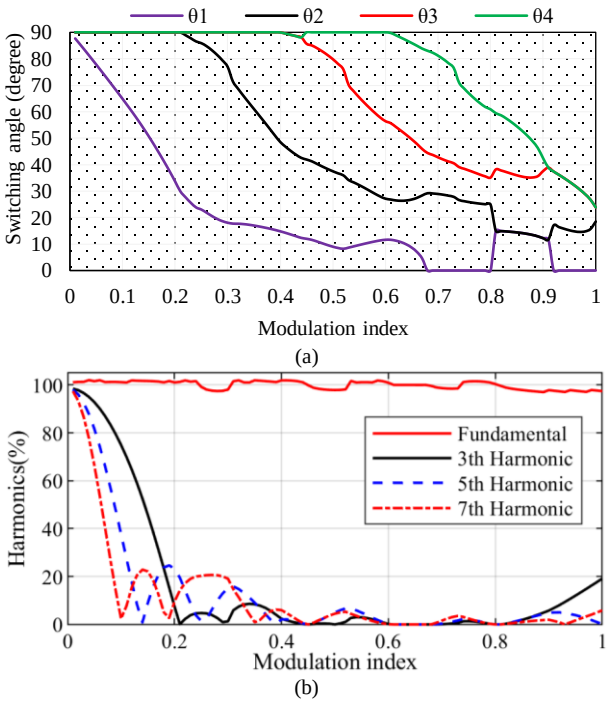

Fig. 8: Variation of (a) switching angles and (b) fundamental and harmonic with respect to m_a

IV. POWER LOSS ANALYSIS

The power loss analysis of the proposed topology has been accomplished in this section. The total power losses of the SC-based MLI is given in (12) as

$$P_{losses} = P_{sw} + P_c + P_{ripple} \tag{12}$$

Where, P_{sw}, P_c and P_{ripple} are switching, conduction, and ripples losses respectively. The P_C and P_{SW} losses are due to power semiconductor devices and P_{ripple} losses occur due to capacitors.

A. Switching losses (P_{sw})

The current and voltage overlap each other during the transition of switching state due to the non-ideal behavior of the power switch and cause switching losses. The P_{sw} losses in the SC-MLI can be calculated using (13).

$$P_{sw} = \left[\sum_{allswitches} \sum_{within\ 1/f_o} \frac{V_{on} I_{on} T_{on}}{6} + \frac{V_{off} I_{off} T_{off}}{6} \right] \times f_o \tag{13}$$

Where, f_o is the output voltage frequency, V_{on}, T_{on}, and I_{on} denote the voltage, time duration and current of a power switch for the ON state period. V_{off}, T_{off}, and I_{off} denote voltage, time duration and current of a power switch for the OFF state period.

B. Conduction Losses (P_c):

The P_c losses of the power switch are calculated using (14)

$$P_c = \sum_{allswitches} I_{o,switch}^2 R_{on} \tag{14}$$

Where R_{on} is the internal resistance of the switch and $I_{o,switch}$ is the current flow through the power devices in an on-state.

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C. Ripple Losses (P_{ripple})

Due to internal resistance of the capacitor that is also known as equivalent series resistance (ESR), the ripple losses or voltage drop (ΔV_c) appears in the output waveform of SC-MLI and calculated using (15).

$$P_{ripple} = \frac{f_{sw}}{2} \times C \times \Delta V_c^2 \quad (15)$$

The PLECS software is used to estimate the total power loss with thermal modeling of the component associated with the proposed topology. The efficiency curve of the proposed topology has been depicted in Fig. 9. It is shown that, at the output load range (100-400) W, the efficiency of the proposed inverter is around 98%. Furthermore, the performance of the proposed inverter is also improved at higher loading conditions. At the output power of 1kW, the efficiency of the proposed inverter is 96.2%.

Furthermore, the power loss distribution of the proposed topology has been illustrated in Fig 10 (a) and (b) for the topologies [P1] and [P2] respectively. The power losses of the switches S_3, S_4 and S_9 have higher power losses compared to other switches and diodes due to the charging current flow of the capacitors.

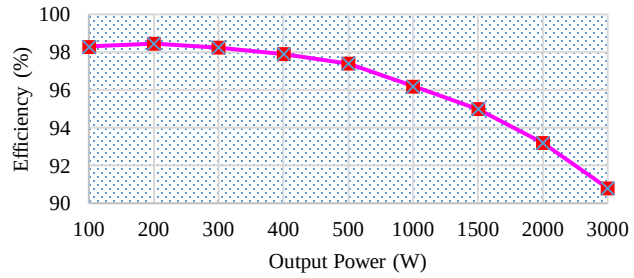
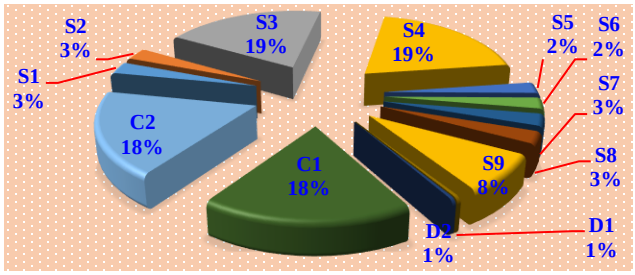
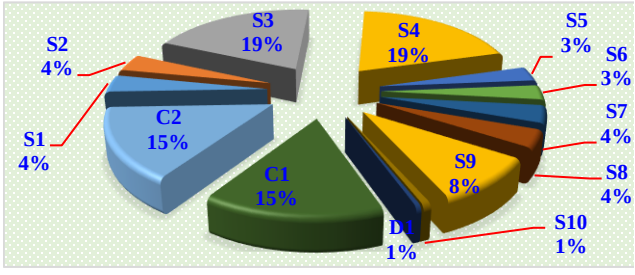


Fig. 9: Efficiency curve of the proposed topology [P1] and [P2]



(a)



(b)

Fig. 10. Power loss distribution with (a) Z = 100Ω [P1] and (b) Z = 100Ω + 200mH [P2]

V. Comparative Study

To judge the usefulness of the proposed topology, a detailed comparison is done with recently proposed similar topologies. For the selection of different topologies used for the comparison, the following criterion has been considered.

(i) Single source configuration
(ii) Boosting ability of the topology
(iii) capacitor voltage equal to or less than the input source voltage

For the comparison, [P1] represents the topology for the resistive load (Fig. 1), [P2] refers to the proposed topology with inductive load capability (Fig. 4) and [P3] represents the proposed topology with the high voltage gain operation. For the comparison, apart from the quantitative comparison, voltage rating of capacitors, the number of switching in the charging loop of the capacitors, N_{sc}, TSV, number of ON-state conducting devices and cost function (CF) is considered.

Table VII shows the comparison of different topologies. The topologies proposed in [14]-[20] generate seven-level output voltage whereas the other topologies provided in Table VII generate nine-level. The topology suggested in [14]-[19] uses three capacitors and topology of [20] uses four capacitors for seven-level generation, whereas the proposed topology uses only two capacitors. Further, in topologies [14]-[20], the voltage rating of the capacitor is of higher rating whereas the proposed topology requires capacitors with a voltage rating of $0.5V_{dc}$. The higher voltage rating of capacitors increases the overall cost of the topology. The topologies with higher voltage gains are proposed in [21]-[23], however, with higher voltage gain, these topologies suffer from a higher number of components with their higher voltage ratings. The higher voltage rating of the components increases the overall cost of the topologies.

The proposed topologies [P1] and [P2] along with the topologies suggested in [25]-[28] gives the nine-level output voltage with twice voltage gain. The topology suggested in [27] requires three capacitors with 11 switches. Out of three capacitors, one has a voltage rating equal to the input voltage. The topology proposed in [28] uses the lowest number of switches for nine-level output voltage, however, the voltage stress of the switches have a higher voltage rating.

The number of devices in the charging path of the capacitors (N_{sc}) also determines the performance of the SC-based topologies. These devices need to be of higher current rating and also contributes to higher power losses due to the charging current. From Table VII, the proposed topologies [P1] and [P2] along with topology suggested in [19] have only three devices in the charging loop which is lower compare to all other topologies given in Table VII.

The proposed topology [P3] gives a voltage gain of three along with topologies suggested in [21]-[25]. In terms of component count, the number of devices in the charging loop, and cost, the proposed topology [P3] shows the improvement over other topologies as given in Table VII.

The switching loss of the SC-based MLI is small due to the lower switching frequency and the voltage stress of the switches. Also with sufficient capacitance, the ripple loss can

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TABLE VII
COMPARISON TABLE OF SC BASED MLI TOPOLOGIES WITH BOOSTING ABILITY

Top	N	N_{sw}	N_{gd}	N_d	N_c	V_{CR}		N_{sc}	G	$TSV_{p.u.}$	TCD					CF (with value of α and β)			
						$0.5V_{dc}$	V_{dc}				$\pm1^{st}$	$\pm2^{nd}$	$\pm3^{rd}$	$\pm4^{th}$	TCD_{avg}	0.5, 0.5	1.0, 1.0	1.5, 0.5	0.5, 1.5
[14]	7	10	8	0	3	2	1	6	1.5	5.3	3	4	3	-	3.33	26.65	34.3	31.95	36.65
[15]	7	9	8	0	3	2	1	4	1.5	5.3	6	5	5	-	5.3	26.65	37.3	31.95	42.65
[16]	7	9	8	0	3	2	1	4	1.5	5.3	5	4	4	-	4.3	25.15	34.3	30.45	38.15
[17]	7	10	9	0	3	2	1	4	1.5	6	5	4	5	-	4.67	27	37	33	41
[18]	7	9	8	0	3	2	1	4	1.5	5.3	5	5	4	-	4.67	25.65	35.3	30.95	39.65
[19]	7	9	8	0	3	2	1	3	1.5	5.67	5	4	4	-	4.3	24.335	33.67	30.005	37.335
[20]	7	10	8	0	4	2	2	4	1.5	7.3	5	4	5	-	4.67	28.65	39.3	35.95	42.65
[21]	7	13	13	4	3	0	3	8	3	5.67	6	6	6	-	6	47.335	53.67	54.005	53.335
	9	17	17	5	4	0	4	12	4	5.5	10	9.5	8	8.5	9	62.25	69.5	67.75	71.25
[22]	7	14	14	0	2	0	2	6	3	4.7	6	6	7	-	6.33	41.516	47.033	46.216	47.85
	9	17	17	0	3	0	3	9	4	5.5	8	8	8	8	8	53.75	60.5	59.25	61.75
[24]	7	12	11	0	2	0	2	8	3	5.3	8	8	6	-	7.33	39.316	45.633	44.616	46.65
[25]	7	16	14	0	2	0	2	8	3	5.3	10	8	8	-	8.67	46.983	53.966	52.283	55.65
[27]	9	12	11	0	2	2	0	4	2	5.5	7	6	5	4	5.5	34.5	40	40	40
[28]	9	11	10	0	2	2	0	4	2	5	7	6	6	5	6	32.5	38	37.5	38.5
[29]	9	11	10	0	3	2	1	4	2	5	5	6	6	5	5.5	33.25	38.5	38.25	38.75
[30]	9	9	9	2	2	2	0	4	2	6.5	5	6	5	4	5	31.75	37.5	38.25	36.75
[P1]	**9**	**9**	**9**	**2**	**2**	**2**	**0**	**3**	**2**	**5.75**	**5**	**5**	**5**	**4**	**4.75**	**30.25**	**35.5**	**36**	**35**
[P2]	**9**	**10**	**10**	**1**	**2**	**2**	**0**	**3**	**2**	**5.75**	**5**	**5**	**5**	**4**	**4.75**	**31.25**	**36.5**	**37**	**36**
[P3]	**7**	**11**	**11**	**0**	**2**	**0**	**2**	**4**	**3**	**5.67**	**6**	**5**	**4**	-	**5**	33.335	38.67	39.005	38.335

N_d/V_{CR} = Number of diodes/voltage rating of capacitors, N_{sc} = Number of devices in charging loop, G = voltage gain, TSV_{pu}=Total standing voltage in pu, TCD = Total conducting devices, TCD_{avg} = Average value of TCD

be reduced. The major portion of overall losses for SC-based MLIs is therefore due to the conducting loss. The nine-level topology has four half cycle output levels which are 1st, 2nd, 3rd, and 4th voltage levels whereas seven-level topology has three voltage levels. The term total conducting devices (TCD) provides the total number of conducting devices at each voltage level. From Table VII, the proposed topology has the least number of conducting devices during each level for nine-level output voltage.

To further evaluate the proposed topology, a CF has been defined as described by [26]:

$$CF = N_{sw} + N_{gd} + N_C + N_d + N_{SC} + \alpha TSV_{pu} + \beta TCD_{avg} \quad (16)$$

The term N_{sc} has been included in the CF as it reflects the number of switches that need to be of the higher current rating. α and β represent the weight coefficients of TSV_{pu} and TCD_{avg}, respectively. The value of α and β is different. If the value of α and β is selected more than one in general, the TSV_{pu} and TCD_{avg} are considered important compare to the component count, while if α and β are selected less than one, the cost of the switch, capacitor and gate driver circuit dominate the value of TSV_{pu} and TCD_{avg}. To show the different scenarios of the CF, four different combinations of α and β are used and the estimated cost is given in Table VII. The CF value for the proposed topology has a lower value compared to all nine-level topologies with all the values of α and β.

An efficiency comparison for different topologies has also been carried out and illustrated in Fig. 11. The proposed topology has better efficiency compare to other topologies as it uses less number of components with lower voltage rating. Further, the efficiency of the proposed topology is improved due to the lower number of conducting devices. From all these points, the proposed topology provides a better topology for the nine-level output voltage.

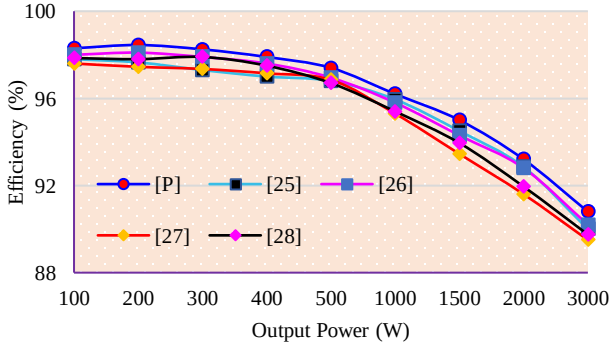

Fig. 11: Efficiency comparison for the 9L configuration

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VI. RESULTS AND DISCUSSION

The proposed SC MLI has been tested experimentally to verify the performance under different operating conditions. TOSHIBA IGBT GT50J325 with an antiparallel diode has been used for the development of the proposed topology. A 2200μF capacitor has been used for splitting the dc voltage sources and boosting the input voltage. The experiment is performed using the dSPACE CP1104 controller for the modulation indexes given in Table VIII. The dSPACE CP1104 controller contains the TMS320F240 slave processor that is responsible for generating the gate pulses for gate drives based on the stored switching angles through digital I/O ports. The control algorithm is made in Simulink/MATLAB and downloaded on a dSPACE CP1104 system which generates the pulses pattern based on the stored firing angles for the gate drive to operate the IGBTs for particular modulation index. The gate drives provide isolation and change the pulse voltages (0 and 5V) into compatible IGBT driving voltages (±15V). Table IX gives the different parameters of the components used in the experimental setup. Fig. 12 shows the prototype of the experimental setup.

TABLE VIII
SWITCHING ANGLE FOR NINE LEVELS (DEGREE)

m_a	θ_1	θ_2	θ_3	θ_4
0.45	12	41.93	85.67	89.99
0.65	8.66	26.82	49.57	85.96
0.8	0.01	24.91	35.13	60.90

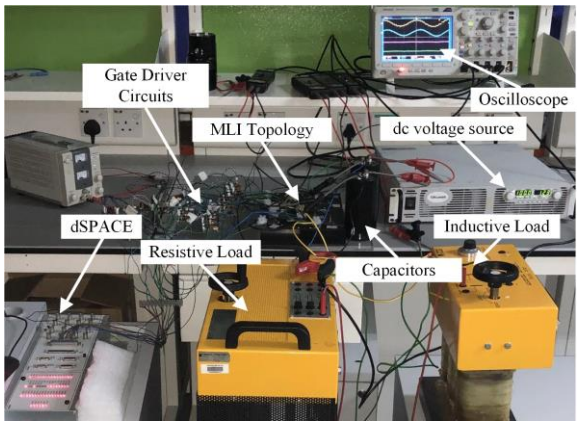
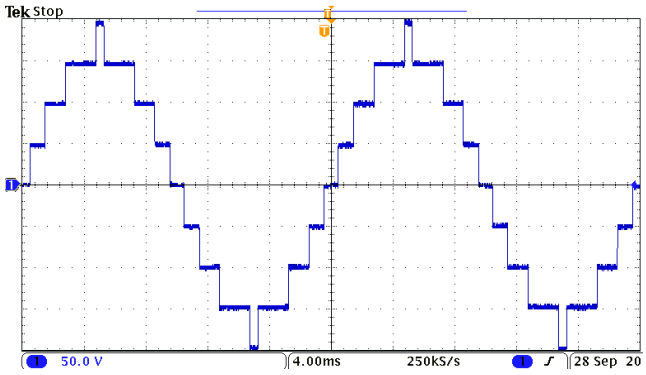


Fig. 12: Experimental Setup

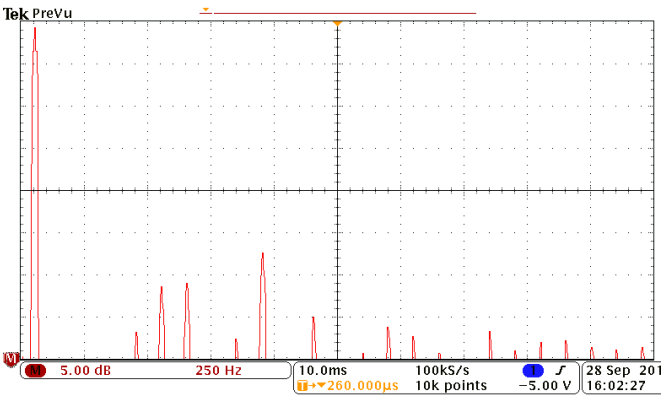
TABLE IX
SPECIFICATIONS OF EXPERIMENTAL SETUP

Input Voltage	100V
Capacitors	2200μF, 450V
IGBT module	GT50J325
Output frequency	50Hz
Controller	dSPACE CP1104
Resistive Load	100Ω
Inductive Load	200mH

Fig. 13 (a) and (b) show the output voltage waveform for the proposed 9 level topology and its FFT respectively at the modulation index of 0.65. The output voltage has a peak magnitude of 200V with a step voltage of 50V. The FFT of the output voltage has an almost zero value for the 3rd, 5th, and 7th order harmonic which has been selected for elimination using SHEPWM.



(a)



(b)

Fig. 13: (a) Output voltage waveform and (b) FFT of the output voltage waveform

The proposed topology has also been tested with different loading conditions. Fig. 14 (a) and (b) depict the output voltage and current waveform with load R and series-connected RL load respectively with a frequency of 50Hz. - In both figures, changes in the modulation index result in changes in the magnitude of the output voltage and current. In Fig. 14 (c), the variation is shown for modulation index 0.80 and 0.65. The voltage across both the capacitors do not show any significant variations when the modulation index is slightly altered. In Fig. 14 (d) the difference in modulation index is made more significant, between 0.8 and 0.45. However, this significant change in modulation index does not affect the capacitor voltages V_{C1} and V_{C2}, and both remain at 50V.

Fig. 15 (a) and (b) shows the different parameter of the output quantity. From Fig. 15 (a) and (b), it is clear that as the output power changes from 134.3 W to 266.9 W, the output voltage magnitude and THD remains the same. The equal

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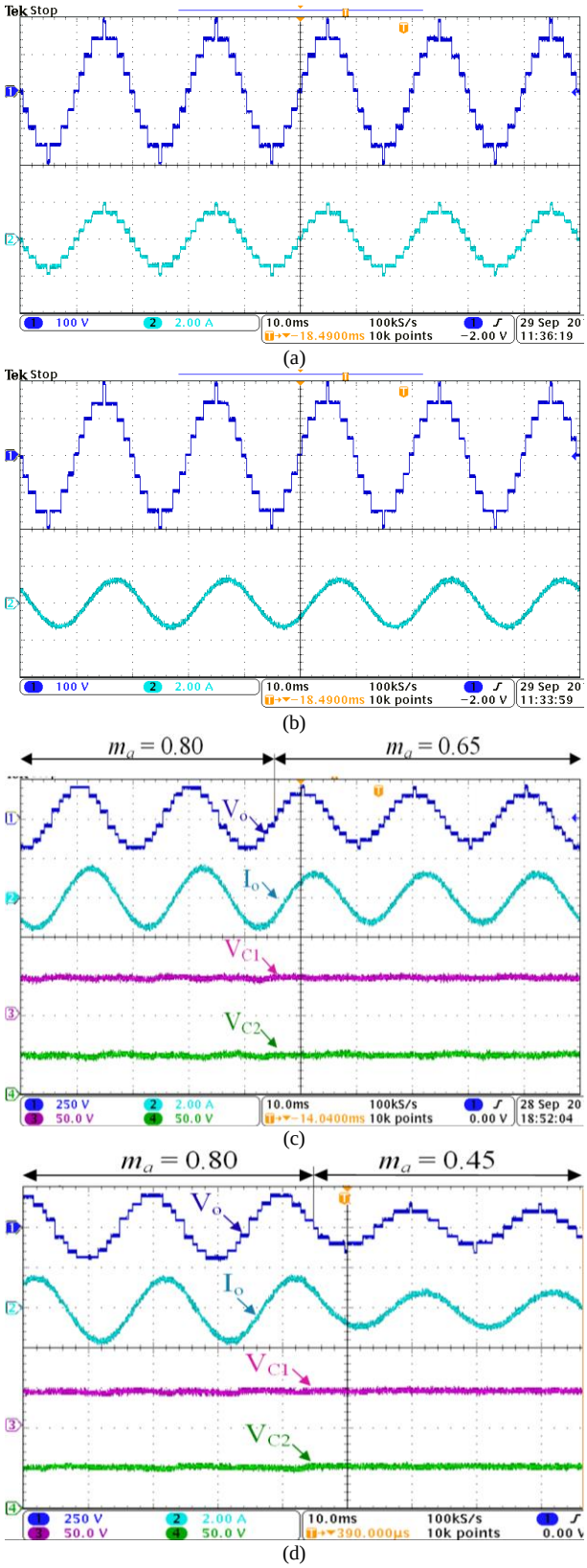

Fig. 14: Output voltage and current waveform with (a) R load and (b) series connected RL load, (c) output voltage and current waveform along with capacitor voltages for change of modulation index from 0.8 to 0.65 and (d) 0.8 to 0.45

amount of voltage THD which is 11.75% with R = 100 Ω and 11.85% with R = 50Ω reflected the capacitor voltage balancing and is unaffected with the change in output power.

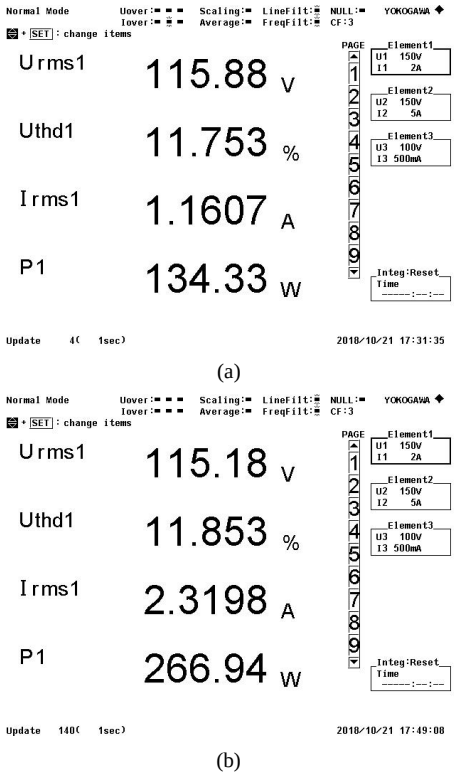

Fig. 15: (a) Different parameters of output with (a) R=100 Ω (b) R=50 Ω [U_{rms1} = rms value of the output voltage, U_{thd1} = THD value of the output voltage, I_{rms1} = rms value of the output current, P_1 = output power]

VII. CONCLUSION

This article introduces a new single-phase switched-capacitor based step-up multilevel inverter topology. The proposed topology achieves nine output voltage levels with a single dc voltage source with a boosting factor of 2. Both polarities are obtainable at the output without using H-bridge, parallel operation of capacitors, lower voltage rating of capacitors, self-voltage balancing of the capacitor voltage with reduced TSV and switch count has been the main feature of the proposed topology. Further, the high gain configuration of the proposed topology has also been discussed. The comparative study with recently proposed SC topologies demonstrates the superiority of the proposed topology. SHEPWM technique has been used for the pulse generation with the removal of dominant lower order harmonics from the output voltage waveform. Lastly, a laboratory prototype was set up to validate the operation of the proposed topology. Various experimental results were obtained to verify the performance of the proposed topology.

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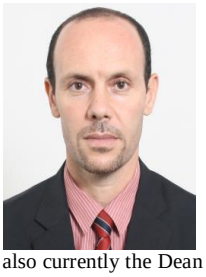
Marif Daula Siddique (S'18) was born in Chhapra, Bihar, India, in 1992. He received the B.Tech and M.Tech degrees in Electrical Engineering from Aligarh Muslim University (AMU) in 2014 and 2016, respectively. He is currently working towards the Ph.D. degree in the Power Electronics and Renewable Energy Research Laboratory (PEARL), Department of Electrical Engineering, University of Malaya, Kuala Lumpur, Malaysia. He is also currently working as Research Assistant with the Department of Electronic Engineering, Qatar University, Doha, Qatar. He has authored or coauthored more than 20 publications in international journals and conference proceedings. His research interest includes step-up power electronics converters (dc/ac, and dc/dc), multilevel inverter topologies and their control. He is serving as a regular reviewer for various journals of IEEE and IET.



Saad Mekhilef (SM'12) received the bachelor's degree in electrical engineering from the University of Setif, Setif, Algeria, in 1995, and the master's degree in engineering science and the Ph.D. degree in electrical engineering from the University of Malaya, Kuala Lumpur, Malaysia, in 1998 and 2003, respectively. He is currently a Professor and the Director of the Power Electronics and Renewable Energy Research Laboratory with the Department of Electrical Engineering, University of Malaya. He is also currently the Dean of the Faculty of Engineering, University of Malaya. He is also a Distinguished Adjunct Professor with the School of Software and Electrical Engineering, Faculty of Science, Engineering and Technology, Swinburne University of Technology, VIC, Australia. He has authored or coauthored more than 500 publications in international journals and conference proceedings. His current research interests include power converter topologies, control of power converters, renewable energy, and energy efficiency. He is serving as an Editor of *Renewable & Sustainable Energy Reviews*, an Associate Editor of *IEEE Transactions on Power Electronics*, *IEEE Open Journal of Industrial Electronics*, and *Journal of Power Electronics*.

Sanjeevikumar Padmanaban (M'12–SM'15) received the bachelor's degree in electrical engineering from the University of Madras, Chennai, India, in 2002, the master's degree (Hons.) in electrical engineering from Pondicherry University, Puducherry, India, in 2006, and the PhD degree in electrical engineering from the University of Bologna, Bologna, Italy, in 2012. He was an Associate Professor with VIT University from 2012 to 2013. In 2013, he joined the National Institute of Technology, India, as a Faculty Member. In 2014, he was invited as a Visiting Researcher at the Department of Electrical Engineering, Qatar University, Doha, Qatar, funded by the Qatar National Research Foundation (Government of Qatar). He continued his research activities with Dublin Institute of Technology, Dublin, Ireland, in 2014.

He was an Associate Professor with the Department of Electrical and Electronics Engineering, University of Johannesburg, Johannesburg, South Africa, from 2016 to 2018. Since 2018, he has been a Faculty Member with the Department of Energy Technology, Aalborg University, Esbjerg, Denmark. He has authored more than 300 scientific papers. S. Padmanaban was the recipient of the Best Paper cum Most Excellence Research Paper Award from IET-SEISCON'13, IET-CEAT'16, IEEE-EECSI'19, IEEE-CENCON'19 and five best paper awards from ETAEERE'16 sponsored Lecture Notes in Electrical Engineering, Springer book. He is a Fellow of the Institution of Engineers, India, the Institution of Electronics and Telecommunication Engineers, India, and the Institution of Engineering and Technology, U.K. He is an Editor/Associate Editor/Editorial Board for refereed journals, in particular the IEEE SYSTEMS JOURNAL, IEEE Transactions on Industry Applications, IEEE ACCESS, *IET Power Electronics*, and *International Transaction on Electrical Energy Systems, Wiley*, and the Subject Editor for the *IET Renewable Power Generation*, *IET Generation, Transmission and Distribution*, and *FACTS* journal (Canada).

Mudasir Ahmed Memon received the B.E. degree in Electronic Engineering and the M.E. degree in electronic systems engineering from the Mehran University of Engineering and Technology, Jamshoro, Pakistan, in 2008 and 2015, respectively and the Ph.D. degree in Power Electronics from the University of Malaya, Kuala Lumpur, Malaysia in 2019.

He is currently working as Assistant Professor with the Department of Electronic Engineering, Faculty of Engineering and Technology, University of Sindh, Jamshoro. His research interests include multilevel inverters, power quality, and control strategies.

Chandan Kumar (S'13-M'15-SM'19) received the B.Sc. degree from Muzaffarpur Institute of Technology, Muzaffarpur, India, in 2009; the M.Tech. degree from the National Institute of Technology, Trichy, India, in 2011; and the Ph.D. degree from the Indian Institute of Technology Madras, Chennai, India, in 2014, all in electrical engineering.Since 2015, he is working as assistant professor in electronics and electrical engineering department at Indian Institute of Technology Guwahati, India. In 2016-17, he worked as Alexander von Humboldt research fellow at Chair of Power Electronics, University of Kiel, Kiel, Germany. He serves as an Associate Editor of the IEEE Access. His research interests include power electronics application in power system, power quality, and renewable energy.