HVDC Grid Fault Current Limiting Method Through Topology Optimization Based on Genetic Algorithm

Tao, Yan ; Li, Baohong; Dragievi, Tomislav; Liu, Tianqi; Blaabjerg, Frede

Published in:
I E E E Journal of Emerging and Selected Topics in Power Electronics

DOI (link to publication from Publisher):
10.1109/JESTPE.2020.3026026

Publication date:
2021

Document Version
Accepted author manuscript, peer reviewed version

HVDC Grid Fault Current Limiting Method through Topology Optimization Based on Genetic Algorithm

Yan Tao, Baohong Li, *Member, IEEE*, Tomislav Dragičević, *Senior Member, IEEE*, Tianqi Liu, *Senior Member, IEEE*, Frede Blaabjerg, *Fellow, IEEE*

***Abstract*—Limiting fault current level of high voltage direct current (HVDC) grid is conducive to reduce the cost of current limiting devices and to relieve the stringent time constraints on protection, but the main concentrations are focused on pole-to-pole fault, while few attentions have been paid to pole-to-ground fault, especially in symmetrical mono-pole DC grid. This paper proposes a pole-to-ground fault current limiting method through topology optimization, which is implemented in three steps. The influence factors of pole-to-ground fault current in symmetrical mono-pole HVDC grid are clarified in the first step, which is based on the detailed state space model of DC grid. And the fact that the topology of DC grid influences fault current a lot is confirmed. In the second step, a simplified index is proposed based on the above theoretical analysis, thus the fault current level of each topology can be estimated in a simple and efficient way. At last, to limit the pole-to-ground fault current level, the genetic algorithm is used to optimize the DC grid topology. The optimization results of studied cases indicate that the mesh structure or ring structure is recommendable for DC grid in term of fault current limiting.**

***Index Terms*—HVDC grid, pole-to-ground fault current, fault current limitation, topology optimization, genetic algorithm**

I. Introduction

THE voltage sourced converter (VSC) based HVDC grids are prospecting and researched a lot in the past years with the advancements in power electronics technology[1], [2]. Especially, the modular multilevel converter (MMC) endows VSC with high voltage and large capacity, and it has become the essential choice in practical VSC-HVDC projects [3].

However, compared with the traditional thyristor-based converters, the IGBT components in the VSC are much more vulnerable and sensitive to fault currents [4], which makes the fault current limitation in modern VSC-HVDC grids of greater importance compared to traditional HVDC, especially for the grid using DC circuit breaker (DCCB) to isolate DC faults [5]. The extremely fast propagation speed of fault current and the poor tolerance of power electronic devices to overcurrent impose more stringent technical requirements on DCCBs [6], [7], as well as on protection system design.

Generally, the fault current of VSC-HVDC can be divided into two types, which are pole-to-ground fault current and pole-to-pole fault current. Because the pole-to-pole fault has higher impact compared to the pole-to-ground fault, much more researches have been done on it. The high-frequency equivalent impedance model proposed in [8] and [9] proves that the pole-to-pole fault current value can only be influenced by the parameters of the fault line and its terminal converters rather than other healthy lines. It makes the characteristic of pole-to-pole fault not complex, and thus, the most effective method to limit a pole-to-pole fault current is adding extra devices [10], and some pole-to-pole fault current limiters are invented in past years [11]-[13].

Compared with the pole-to-pole fault, the pole-to-ground fault in HVDC grid received very little attention, although it appears much more frequently and also need to be limited. The current literatures of the pole-to-ground fault mainly concentrated on the fault location and ride through methods [14]-[16]. The reference [17] studied the characteristic and calculation of pole-to-ground fault in bipolar DC grid, but this type pole-to-ground fault is actually a pole-to-pole fault in symmetrical mono-pole DC grid. Its limiting method still depends on extra devices. The analytical expressions of pole-to-ground fault current proposed in [18] ignores the dynamic process of the submodule capacitance, while only the capacitance of the faulty pole is considered to contribute to the fault current in [19]. The above calculation methods can not accurately describe the law of fault current development, and further analysis on its influence factors is not thorough.

It is suggested that all the terminals in a symmetrical mono-pole DC grid should be grounded by high impedance to effectively limit the pole-to-ground fault current [20] and to mitigate overvoltage [21]. If the current limiting only depends on the grounding devices, larger land occupation and extra considerable expenditure are always needed.

Actually, the characteristic of pole-to-ground fault in symmetrical mono-pole DC grids is much more complex and

This work was supported by the National Key Research and Development Program of China under Grant 2018YFB0904600.

Yan Tao, Baohong Li and Tianqi Liu are with the College of Electrical Engineering, Sichuan University, Chengdu, 610065, and China. (Corresponding author: Baohong Li, e-mail: scu_lbh@163.com;)

Tomislav Dragicevic and Frede Blaabjerg are with the Department of Energy Technology, Aalborg University, Aalborg, 9920, Denmark.

different from that of the pole-to-pole fault. The healthy lines in symmetrical mono-pole DC system will impact the fault current value [22]. It indicates that topologies of DC grid can influence the pole-to-ground fault current. Thus, the fault current in symmetrical mono-pole DC grid can also be limited by optimizing the grid topology rather than simply adding expensive devices, which can be done in the early time of power network planning stage.

However, optimizing the DC grid topology based on detailed MMC models is impossible, especially in multi-terminal HVDC systems. Some researchers proposed state space model based on RLC equivalent circuit to simplify the pole-to-pole fault current calculation [23]. But it is unsuitable for topology optimization, as the order of differential equations is so high that just one-line fault current calculation would take several minutes, not to mention the topology is varying. Thus, some simplified indexes and intelligence algorithms are needed to improve the efficiency of DC topology optimization. But no relative work has been done until now.

To limit the overall fault current level and provide reference for power grid construction, this paper proposes a topology optimization method for symmetrical mono-pole DC grids based on genetic algorithm. The novelty of this paper can be concluded from three aspects.

(1) The characteristic of the pole-to-ground fault current in symmetrical mono-pole DC grid is clarified through state space model.

(2) Based on the characteristic analysis, the simplified index to estimate the pole-to-ground fault current level of different DC grid topologies is proposed.

(3) Through the simplified index, the topology optimization method based on genetic algorithms to limit the pole-to-ground fault current level in symmetrical mono-pole DC grid is also proposed, which can impose less stringent time constraints on protection and DCCBs.

The organization of this paper is as follows. Section II studies the pole-to-ground fault current calculation method in symmetrical mono-pole DC grid based on state space model. Based on the calculation method of section II, Section III investigates the characteristic of pole-to-ground fault current, and then proposes a simplified index to estimate the fault current level of each topology. Through the proposed index, section IV researches the DC grid optimization method based on genetic algorithm to limit the fault current level. Topology optimization of several DC grid cases with different terminals are studied in Section V, and Section VI concludes the paper.

II. Fault Current Calculation and Analysis Methods

In symmetrical mono-pole HVDC grid, the fault characteristic of pole-to-ground fault has close relationship with system's grounding mode. But in this paper, the AC side grounding mode through star-point inductors and resistor is discussed only, as Fig. 1 (a) shows. As for the other two grounding modes, which are the AC side grounding mode through the neutral point of transformer and the DC side grounding mode, are either unsuitable for high voltage transmission or cannot form pole-to-ground fault current in symmetrical mono-pole HVDC grid.

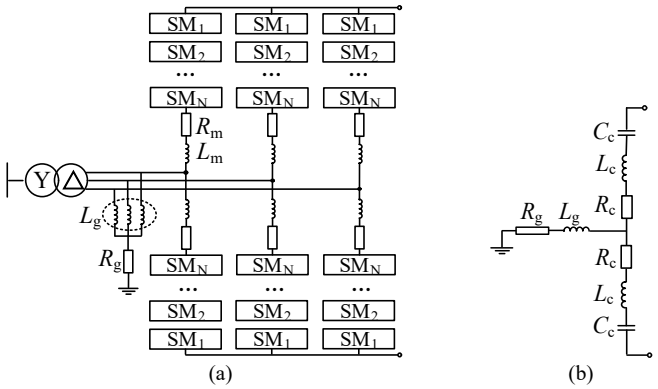


Fig. 1. Simplified circuit of MMC. (a) Circuit diagram of MMC. (b) RLC equivalent circuit for pole-to-ground fault analysis.

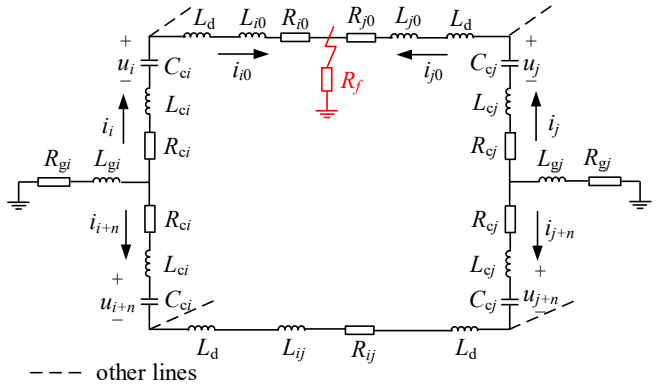


Fig. 2. Model of DC grid for pole-to-ground fault current analysis.

After the confirmation of the grounding mode in DC grid, the influence factors and characteristic of pole-to-ground fault current need to be investigated, so that the topology optimization objective can be obtained. Thus, the detailed calculation and characteristic analysis of fault current are discussed in this section.

A. Equivalent Circuit for Pole-to-Ground Fault Current Analysis

According to the MMC equivalent model, a pole-to-ground equivalent RLC circuit can be obtained in symmetrical mono-pole HVDC grid, as Fig. 2 shows. Here R_m is the sum of the on-state resistance of all the IGBT modules, L_m is the arm inductance, R_g is the grounding resistance, and L_g is the equivalent inductance of the grounding star-point inductors (one third of grounding inductance). The final equivalent RLC model of a converter for fault current calculation is presented in Fig. 1 (b), where the R_c, L_c and C_c are equivalent resistance, equivalent inductance and equivalent capacitance respectively, which can be obtained as [24]

$$R_c = \frac{R_m}{3} \tag{1}$$

$$L_c = \frac{L_m}{3} \tag{2}$$

Assuming capacitor voltages of SMs are balanced, and are equal to the same value U_{SM}, the energy conservation principle can be expressed as [24]

$$E = 3 \times N_{SM} \times \frac{1}{2} C_{SM} U_{SM}^2 = \frac{1}{2} C_c \left(\frac{1}{2} N_{SM} U_{SM} \right)^2 \quad (3)$$

where C_{SM} is the sub-module (SM) capacitance and N_{SM} is the number of SMs per arm. The expression of equivalent capacitor C_c is obtained as

$$C_c = \frac{12 C_{SM}}{N_{SM}} \quad (4)$$

B. Pole-to-Ground Fault Current Calculation Method

Although the topologies of DC grids are varied, the KVL equations of each DC grid can be obtained with the help of converter's equivalent circuits in Fig. 1(b). For convenient theoretical analysis, the main step of pole-to-ground fault current calculation can be described in two steps: firstly the state space equations based on KVL differential equations are obtained, where the grid is with no fault; then the parameters related to fault branch are changed and additional fault equations are added to state space equations when a certain line occurs a pole-to-ground fault. The following part will discuss this in detail.

The dynamic process of the healthy pole when the voltage rises is usually ignored. Hence the differential equations do not reflect the charging or discharging process of the sub-module capacitors in healthy pole. In this section, the dynamic process of both positive and negative poles will be considered to calculate the pole-to-ground fault current.

Assuming that a symmetrical mono-pole DC grid has n converters and l lines, and in converter i, the equivalent arm current in positive pole is i_i and in negative pole is i_{i+n}. The voltage of equivalent capacitor in positive pole is u_i and in negative pole is u_{i+n} correspondingly, as shown in Fig. 2. The DC lines are modelled as series RL circuits, where the resistance and inductance of the line ij (in negative line is $i+n$, $j+n$) are R_{ij} and L_{ij}, and L_d is the smoothing reactor. If a pole-to-ground fault happens at line ij, which is positive line of course, the parameters of line ij need to be changed to R_{i0}, R_{j0} and L_{i0}, L_{j0}, and the line current i_{ij} (the current from node i to node j) should also be adjusted to fault current i_{i0} and i_{j0}, as shown in Fig. 2. Nevertheless, a new fault branch with a grounding resistance R_f should be considered and new equations need to be added also.

Thus, to obtain the state space equations with no fault firstly, the state variables are confirmed as the line currents and the equivalent arm capacitor voltages, which are $\boldsymbol{i}=[i_{12} \dots i_{ij} \dots]^T$ and $\boldsymbol{u}=[u_1 \dots u_n \ u_{n+1} \dots u_{2n}]^T$. The equivalent arm current vector $\boldsymbol{i}_c=[i_1 \dots i_n \ i_{n+1} \dots i_{2n}]^T$ can be obtained with the help of incidence matrix describing the topology relationship between lines and converters, as shown in (5).

$$\boldsymbol{i}_c = \boldsymbol{A}\boldsymbol{i}. \quad (5)$$

The dimension of incidence matrix $\boldsymbol{A}$ is $2n \times l$ and the elements of it are defined as

$$a_{ik} = \begin{cases} 1 & \text{node } i \text{ is the starting point of branch } k \\ -1 & \text{node } i \text{ is the terminating point of branch } k \\ 0 & \text{node } i \text{ is not a point of branch } k. \end{cases} \quad (6)$$

As the current in positive pole has opposite direction with current in negative pole, a $2n \times 2n$ diagonal matrix $\boldsymbol{M}$ is defined to modify the current direction and the elements in $\boldsymbol{M}$ are defined as

$$m_{ii} = \begin{cases} 1 & \text{node } i \text{ is positive node} \\ -1 & \text{node } i \text{ is negative node.} \end{cases} \quad (7)$$

With the help of KVL equations, (8) can be obtained as

$$\boldsymbol{B}\boldsymbol{u} = \boldsymbol{R}\boldsymbol{i} + \boldsymbol{L}\frac{\mathrm{d}\boldsymbol{i}}{\mathrm{d}t} \quad (8)$$

where $\boldsymbol{B}$ is

$$\boldsymbol{B} = \boldsymbol{A}^T \boldsymbol{M}. \quad (9)$$

$\boldsymbol{R}$ is the resistance matrix and $\boldsymbol{L}$ is the inductance matrix in (8), which are both $l \times l$ matrixes and represent the matrix of loop resistance and loop inductance respectively. The writing rules of $\boldsymbol{L}$ and $\boldsymbol{R}$ are of the same. Taking $\boldsymbol{R}$ for an example, the diagonal element of $\boldsymbol{R}$ consists of all the resistances that the loop current flows through, which is $R_{gi}+R_{ci}+R_{ij}+R_{cj}+R_{gj}$. As stated before, the diagonal elements are modified as $R_{gi}+R_{ci}+R_{i0}+R_f$ and $R_{gj}+R_{cj}+R_{j0}+R_f$ when fault happens at line ij, where new current variables i_{i0} and i_{j0} should also be added. As for non-diagonal elements in matrix $\boldsymbol{R}$, they are all grounding resistances and equivalent arm resistances. The grounding resistance only shows up at the positions corresponding to certain line currents, as Table I shows, where the subscripts of p and q are other connected nodes. And the arm equivalent resistance writing rule is basically the same except that the elements corresponding to negative line currents are zero when writing positive line elements, as Table II shows.

TABLE I
DISTRIBUTION OF GROUNDING ELECTRODE RESISTANCE IN NON-DIAGONAL ELEMENTS

branch current	i_{ip} /$i_{i+n,p+n}$	i_{pi} /$i_{p+n,i+n}$	i_{pj} /$i_{p+n,j+n}$	i_{jp} /$i_{j+n,p+n}$	i_{pq} /$i_{p+n,q+n}$	i_{qp} /$i_{q+n,p+n}$
element	R_{gi}	$-R_{gi}$	R_{gj}	$-R_{gj}$	0	0

TABLE II
DISTRIBUTION OF EQUIVALENT POSITIVE-POLE ARM RESISTANCE IN NON-DIAGONAL ELEMENTS

branch current	i_{ip}	i_{pi}	i_{pj}	i_{jp}	i_{pq}	i_{qp}
element	R_{ci}	$-R_{ci}$	R_{cj}	$-R_{cj}$	0	0

On the other side, the arm current $\boldsymbol{i}_c$ can be expressed as

$$\boldsymbol{C}\frac{\mathrm{d}\boldsymbol{u}}{\mathrm{d}t} = -\boldsymbol{M}\boldsymbol{i}_c. \quad (10)$$

Combining (5) and (10) yields

$$\boldsymbol{C}\frac{\mathrm{d}\boldsymbol{u}}{\mathrm{d}t} = -\boldsymbol{M}\boldsymbol{i}_c = -\boldsymbol{M}\boldsymbol{A}\boldsymbol{i} = \boldsymbol{P}\boldsymbol{i}. \quad (11)$$

$\boldsymbol{C}$ is a diagonal matrix composed of the equivalent capacitance of the positive and negative poles of each converter, which is $\boldsymbol{C}=\mathrm{diag}[C_{c1} \dots C_{cn} \ C_{c1} \dots C_{cn}]$.

Thus, the state space equations of DC grid are obtained from (8) and (11), which are shown as

$$\begin{cases} \boldsymbol{L}\dfrac{\mathrm{d}\boldsymbol{i}}{\mathrm{d}t} = -\boldsymbol{R}\boldsymbol{i} + \boldsymbol{B}\boldsymbol{u} \\ \boldsymbol{C}\dfrac{\mathrm{d}\boldsymbol{u}}{\mathrm{d}t} = \boldsymbol{P}\boldsymbol{i}. \end{cases} \tag{12}$$

It should be pointed out that the current calculated in (12) is the fault component of current. Added with the steady-state component $\boldsymbol{i}_{st}$, the total value of the line current after fault can be written as

$$\boldsymbol{i}_f = \boldsymbol{i} + \boldsymbol{i}_{\mathrm{st}}. \tag{13}$$

Noting that (12) are homogeneous equations and can be rewritten as

$$\frac{\mathrm{d}}{\mathrm{d}t}\begin{bmatrix}\boldsymbol{i}\\ \boldsymbol{u}\end{bmatrix} = \begin{bmatrix}-\boldsymbol{L}^{-1}\boldsymbol{R} & \boldsymbol{L}^{-1}\boldsymbol{B}\\ \boldsymbol{C}^{-1}\boldsymbol{P} & \boldsymbol{0}\end{bmatrix}\begin{bmatrix}\boldsymbol{i}\\ \boldsymbol{u}\end{bmatrix} \Leftrightarrow \frac{\mathrm{d}\boldsymbol{x}}{\mathrm{d}t} = \boldsymbol{S}\boldsymbol{x}. \tag{14}$$

It is also known that for a homogeneous equation, its results can be calculated by infinite series by (15), where $\boldsymbol{x}_0$ is the initial vector of variable $\boldsymbol{x}$.

$$\boldsymbol{x}(t) = e^{\boldsymbol{S}t}\boldsymbol{x}_0 = \left(\boldsymbol{I} + \boldsymbol{S}t + \frac{1}{2!}\boldsymbol{S}^2t^2 + \cdots + \frac{1}{k!}\boldsymbol{S}^kt^k + \cdots\right)\boldsymbol{x}_0 \tag{15}$$

Another important fact is that, people usually only concern about the fault current value in the very beginning time in DC grids, namely in 10 milliseconds [17], [23]. Thus, the high order parts of (15) can be ignored as t is very small. Thus, the fault current results now can be obtained without solving the high order differential equations, and the variables can also be retained for analysis.

III. Fault Current Characteristic Analysis and Simplified Index for Optimization

A. *Verification of Fault Current Calculation Methods*

Before the characteristic analysis of pole-to-ground fault current, the simulation verifications are needed to ensure the fault current theoretical calculation is accurate. The simulation model based on PSCAD/EMTDC software is shown in Fig. 3. The parameters of the converter stations and DC lines are listed in Table I, where the positive direction of converter station's power is from AC system to DC system. A positive pole-to-ground fault occurs at line 1-4 when t=1s. The comparison results of the proposed calculation method are illustrated in Fig. 4(a), and that of the method proposed in [19] are shown in Fig. 4(b).

There is obvious discrepancy between the simulation results and the calculation results without considering the dynamic process of healthy poles, as shown in Fig.4 (b), so it is unable to describe the evolution of fault current correctly. By contrast, the numerical calculation matches well with the simulation results with both positive and negative poles considered. As shown in the absolute error stem chart in Fig. 4(a), the maximum miscalculation is only 0.08 kA (the relative error is 2.4 %), which is utterly acceptable in projects. Thus, we can continue the characteristic analysis of pole-to-ground fault current in symmetrical mono-pole HVDC grid based on the highly-accurate theoretical calculation.

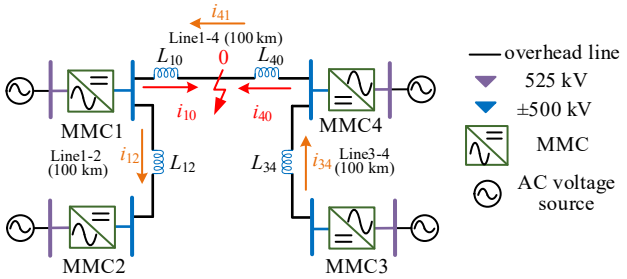


Fig. 3. Topology of HVDC grid.

TABLE III
Parameters of Converter Stations and DC Lines in Fig. 3

Parameter	Value
Rated capacity	3000 MVA
Rated DC voltage	±500 kV
Rated AC voltage	525 kV
Arm inductance	66 mH
Arm resistance	0.67 Ω
Capacitance of one submodule	16.3 mF
Number of submodules per arm	495
DC smoothing reactor	150 mH
Line Resistance	0.0099Ω/km
Line Inductance	0.82 mH/km
Grounding inductance	3 H
Grounding resistance	200 Ω
Control Mode	MMC1: P=1500 MW, Q=0 Mvar MMC2: U_{dc}=1000 kV, Q=0 Mvar MMC3: P=2000 MW, Q=0 Mvar MMC4: P=-1000 MW, Q=0 Mvar

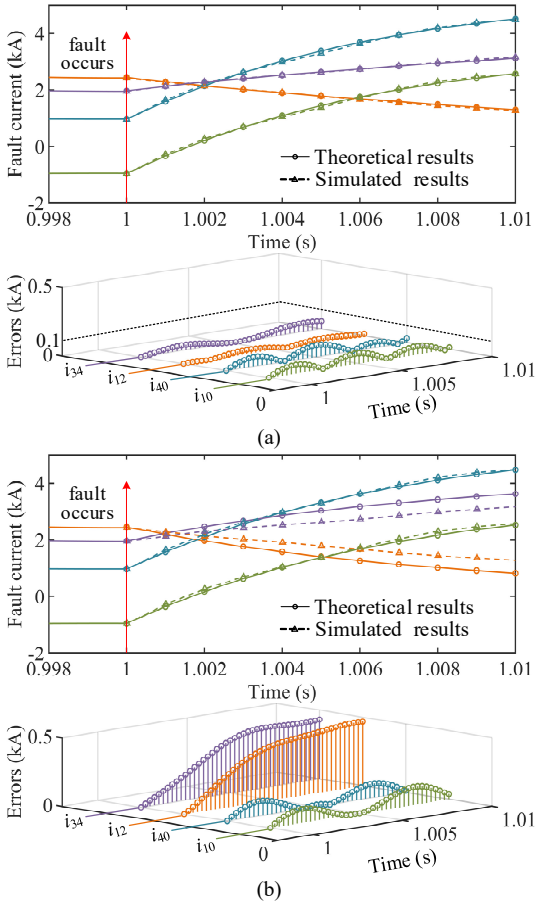


Fig. 4. Comparison of numerical calculation and simulation. (a) Results with healthy pole considered. (b) Results without healthy pole considered.

B. Analysis of Line Parameters' Influence on Fault Current

As calculated in (13), the fault current consists of two independent parts, i.e., fault component and steady-state component. The steady-state component is influenced by the power flow distribution, line impedance, line voltage drop and the topology. Thereinto, the power flow distribution and line voltage drop vary with mutable operation modes. So that the steady-state current is hard to be controlled for the purpose of fault current limiting. However, for a DC grid with determined converter parameters, the fault component is significantly influenced by the topology. Therefore, the fault component is more suitable to be limited by topology optimization. When the fault component decreases, the total fault current will decrease of course. In the subsequent analysis and optimization, the output of each converter is set to zero to eliminate the steady-state component, which can more clearly highlight the influence on the fault component.

As the line resistance mainly affects the steady-state value of fault current [22], the line inductance's influence is mainly discussed here, which can shed the light on the influence of DC grid topology.

The lines' inductance impact on pole-to-ground fault i_{10} in Fig. 3 is analyzed through previous theoretical calculation method, as shown in Fig. 5 (a), (c). The simulation curves of fault current with different inductance values corresponding to 3-dimensional diagrams are also shown in Fig. 5 (b), (d).

It can be seen that the line inductance of L_{10} influence the fault current most, as MMC1 is the nearest converter. And L_{12} influence the fault current less because the fault current injected from MMC2 has a larger distance. It can also be found that for each line, the bigger value of its inductance is, the smaller fault current is obtained.

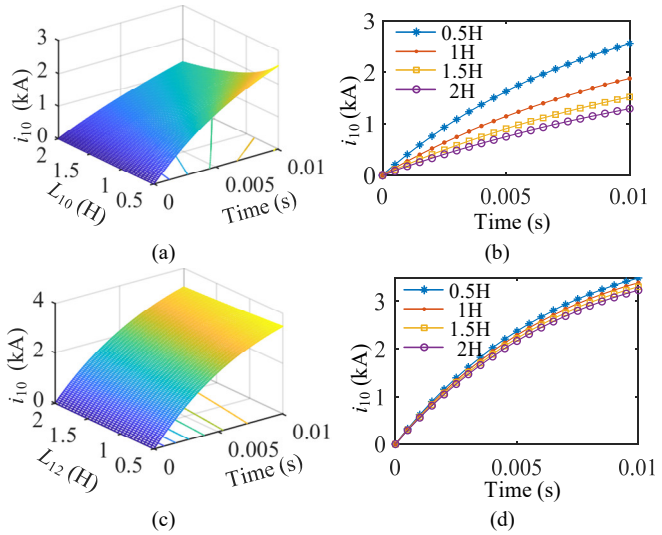


Fig. 5. Influence of different parameters on fault current. (a) Theoretical influence of L_{10}. (b) Simulations of different L_{10}. (c) Theoretical influence of L_{12}. (d) Simulations of different L_{12}.

C. Simplified Index for Topology Optimization

According to the analysis above, the influence of line parameters on pole-to-ground fault current is clarified. But realizing topology optimization based on above detailed model is difficult, thus it is necessary to define a simplified index to evaluate the fault current level in an efficient way.

1) Simplified Index for Single Converter

Based on the obtained characteristic, we can conclude that the pole-to-ground fault current in symmetrical mono-pole HVDC grid is influenced by other converters, and each converter's contribution to the fault current is in an inverse proportion of its distance to the fault location.

Thus, the simplified index for topology optimization can consider the form of reciprocal of distance. And for each single converter n, the simplified index to evaluate its contribution to the pole-to-ground fault current is defined in (16).

$$Index_{\mathrm{PTG}n} = \frac{1000}{Dist_{\mathrm{equivalent}}}. \tag{16}$$

In (16), $Dist_{\mathrm{equivalent}}$ is the equivalent distance from the calculated converter to fault location. The equivalent distance is obtained by converting all the related inductance to equivalent line distance based on the actual DC line parameter, which is 0.082H/100km. For example, the $Dist_{\mathrm{equivalent}}$ of a 0.2H inductance is 243.9km. And the constant 1000 is to prevent the $Index_{\mathrm{PTG}n}$ from being too small for computer calculation.

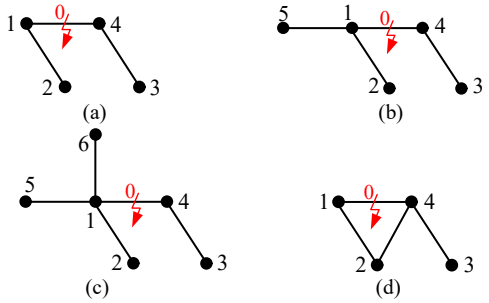


Fig. 6. Four topologies for analysis. (a) Topology 1. (b) Topology 2. (c) Topology 3. (d) Topology 4.

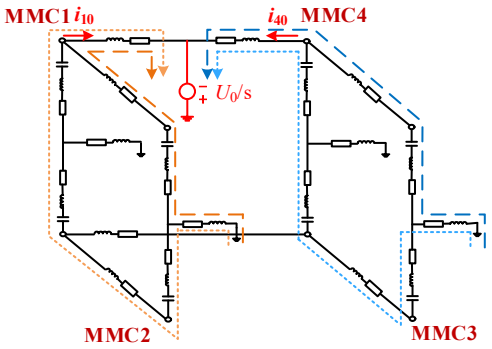


Fig. 7. The fault current paths from other converters to fault point.

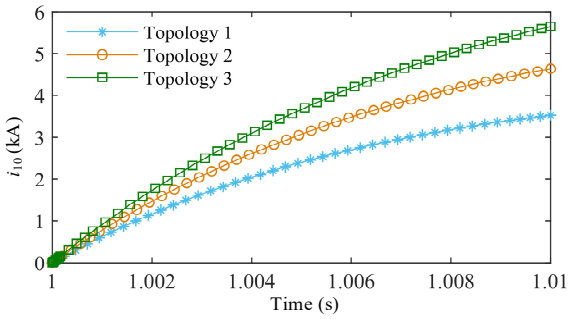


Fig. 8. Curves of i_{10} under three topologies.

2) Simplified Index for DC Grid

The topology of Fig. 3 can be represented by the subfigure (a) of Fig. 6, whose fault current paths are drawn in its detail equivalent model in Fig. 7. Obviously, the impedance on the path through the healthy pole is much greater than that on the path through the faulty pole. Therefore, the contribution from the healthy pole of the converters unconnected to the fault lines to the fault line current in the initial stage can be ignored in the calculation. This is confirmed by the consistency of calculated i_{10} and i_{40} with simulation in Fig. 4(b), where only the dynamic process of the faulty pole is considered. According to the superposition principle proposed in [8], the fault network can be simplified as the combination of impedance and an additional voltage U_0/s at the fault point with step form. The current contributed by the converter i to the fault point can be approximately expressed as

$$i_{\text{con}i}(s)=\frac{U_0}{sZ_{i0}(s)} \tag{16}$$

where Z_{i0} is the impedance on the current path from converter i to fault point in faulty pole. The current of the fault line can be obtained by adding all the feed-in currents of the converters on the same side.

The fault currents' addition rule can be verified as follows, which is through changing the DC grid topology in Fig. 3. After adding the other two lines, namely line 1-5 in subfigure (b) and line 1-6 in subfigure (c), both of which have the same parameter of original line 1-2, the theoretical fault currents of i_{10} corresponding to subfigure (a), (b) and (c) are shown in Fig. 8. Each new added converter increases the fault current with same value, which further proves that the new lines' contribution to the fault current still abide the addition rule all the time. Thus, the simplified index for a whole grid can just add all the related converters' index together.

The simplified index when fault occurs at line i-j is the sum of the related converters' indexes, which can be written as

$$Index_{\text{PTG\_line}ij}=Index_{\text{PTG1}}+Index_{\text{PTG2}}+\cdots+Index_{\text{PTG}n}+\cdots. \tag{17}$$

The $Index_{\text{PTG}n}$ in (17) represents the simplified index of the nth converter, which injects fault current in the direction from i to j. For a fixed topology, when a certain line i-j has a pole-to-ground fault, the larger the $Index_{\text{PTG}ij}$ is, the higher the fault current value of line i-j will be.

3) Two Other Rules for Simplified Index Calculation

There are two other calculating rules should also be considered. Firstly, for each fault line, there are two grounding fault current, which is the left side fault current i_{10} and the right-side fault current i_{40} in the Fig. 3. For each fault current's index calculation, the converter which has no contribution should not be considered.

Taking the MMC3 in Fig.3 for example, which is the black point 3 in subfigure (a) of Fig. 6, the parameter L_{34} basically has no influence on the left side fault current i_{10}. This is because the fault current injected by MMC3 flows into the other right-side fault current i_{40}, thus the index calculation of i_{10} just need to take MMC1 and MMC2 into consideration.

Secondly, some converters contribute the fault current of both sides. As the subfigure (d) of Fig. 6 shows, the converter 2 would inject fault current to the left side and right side simultaneously. In this situation, converter 2 should be taken into consideration in index calculations of both sides. Nevertheless, the equivalent distance of converters 2 needs to be increased to reflect the weaken effect of injecting fault current to both sides.

$$Index_{\text{PTG2}}=\frac{1000}{\dfrac{Dist_{\text{equivalent2-1}}+Dist_{\text{equivalent2-4}}}{Dist_{\text{equivalent2-4}}}Dist_{\text{equivalent2-1}}}. \tag{18}$$

Equation (18) defines the index calculation method in the situation of converter 2 in subfigure (d) of Fig. 6, where the $Dist_{\text{equivalent2-1}}$ denotes the equivalent distance from converter 2 to 1 and $Dist_{\text{equivalent2-4}}$ denotes the equivalent distance from converter 2 to 4 respectively.

IV. Topology Optimization Based on Simplified Index through Genetic Algorithm

Based on the simplified index above, this section will optimize the DC grid topology to limit the pole-to-ground fault current through genetic algorithm. As a widely used intelligence algorithm [25], the genetic algorithm is well known and suitable for topology optimization [26]. Its theory can be found in reference [27], and Fig. 9 presents the optimization procedure.

The optimization procedure in Fig. 9 is basically the same with the classical genetic algorithm except for some steps are adjusted for topology optimizations, which are in orange colour. The following part will explain them in detail.

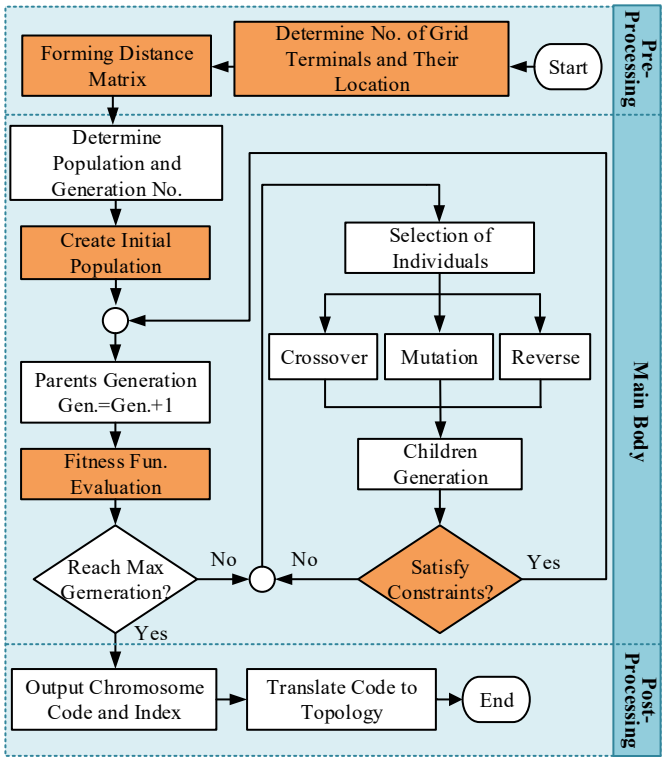


Fig. 9. The procedure of genetic algorithm for topology optimization.

A. The Genetic Coding Rule

Before describing and explaining the adjusted procedures in orange boxes, the genetic coding rule needs to be clarified firstly. In this paper, the binary code is chosen for topology optimization. Assuming a DC grid has five terminals, which are numbered from 1 to 5. For such a fixed topology, its coding rule is shown in Fig. 10.

In Fig. 10, the first two rows are the ordinal permutation of terminal number, which is fixed once the terminal numbers are confirmed. And the third row is the final genetic codes for one topology, namely the chromosome. For one chromosome, the 1 indicates the connection of the two converter stations corresponding to the first two rows, while the 0 indicates disconnection. Thus, the chromosome in Fig. 10 indicates a radical topology, in which the other converters are all directly connected to converter 1.

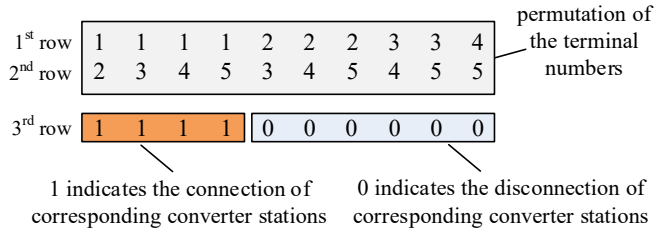


Fig. 10. The binary coding rule of genetic algorithm for topology optimization.

B. Terminals' Location and the Distance Matrix

To calculate the simplified index proposed above, the equivalent distance between each converter needs to be known. Thus, the coordinates of each converter should be confirmed before optimization. In this paper, the reference point is set as the location of converter 1, which means converter 1 is at the origin point.

Based on the coordinate, the distance matrix can be obtained for equivalent distance calculation, as Fig. 11 shows. The D_{ij} in the matrix is the distance between corresponding converters. It is obviously that the distance matrix is a symmetric matrix.

Converter NO.	1	2	3	4	5
1	0	D_{12}	D_{13}	D_{14}	D_{15}
2	D_{21}	0	D_{23}	D_{24}	D_{25}
3	D_{31}	D_{32}	0	D_{34}	D_{35}
4	D_{41}	D_{42}	D_{43}	0	D_{45}
5	D_{51}	D_{52}	D_{53}	D_{54}	0

Fig. 11. The distance matrix.

C. Create Initial Population and the Constraints

To ensure the optimization be efficient and correct, some constraints are needed when creating the initial population and processing iteration.

The first constraint is the connectivity checking. If the output chromosome represents a topology which has disconnected converters, the flag of this chromosome is set to 0 and the previous operation is repeated or recovered until it satisfies this constraint. The second constraint is the restriction of the connectivity degree, which means to prevent too manly connection lines for a topology, because it is uneconomic to design lots of connections in practical project.

D. Fitness Function Evaluation

The fitness function is actually the optimization objective. All the theoretical analysis of last section is to obtain a suitable fitness function.

To represent the fault current level, the fitness function needs to be able to describe the max fault current value of a topology. Thus, for each fixed topology, the fitness function is set as the max simplified index, which is obtained by calculating each line's simplified index when it has a pole-to-ground fault, as (19) shows.

$$f_{\text{fitness}} = \max(Index_{\text{PTG\_line12}}, Index_{\text{PTG\_line21}}, \ldots, Index_{\text{PTG\_line}ij}, Index_{\text{PTG\_line}ji}, \ldots) \tag{19}$$

$Index_{\text{PTG\_line}ij}$ in (19), denotes the simplified index when line ij has a pole-to-ground fault, and the fault current index is calculated from i to j direction. The $Index_{\text{PTG\_line}ji}$ is similar except for the fault current direction is from j to i. And to limit the fault current level of a topology, the optimization direction of the fitness function is minimization.

In one word, the above fitness function is letting each line has a pole-to-ground fault one by one and calculating the simplified index, choosing the max index of them as the fitness function value of this topology, and finally minimizing the fitness function value when topologies vary.

V. Case Study

To validate the proposed simplified index and realize the topology optimization, a symmetrical mono-pole DC system with five terminals is tested in this section. The converters' parameters are the same with the value in Table III except for the outputs are all set to zero for a better comparison. The coordinate of each converter is present in Fig. 12, and the location of converter 1 is set as the origin point as stated before.

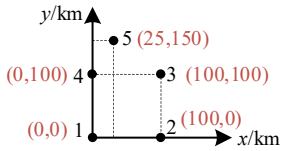


Fig. 12. The coordinates of five converters.

A. Validation of the Simplified Index

Before the topology optimization, the proposed simplified index, namely the $Index_{\text{PTG\_line}ij}$ in (17), should be validated. The topology ④ in Fig. 16 is used for test. Fig. 13 presents the simulation result of the maximum fault current when each single line of this topology has a pole-to-ground fault at 0.5s, which is in detailed view as the curves are very intensive. And Table IV shows the precise current value at 10 ms after fault. It should be noted that the current i_{ij} and i_{ji}, i_{12} and i_{21} for example, are actually fault currents on the either side of fault line ij. The fault is set at the head of the line ij when focusing on i_{ij}, which is the same setting in latter optimization.

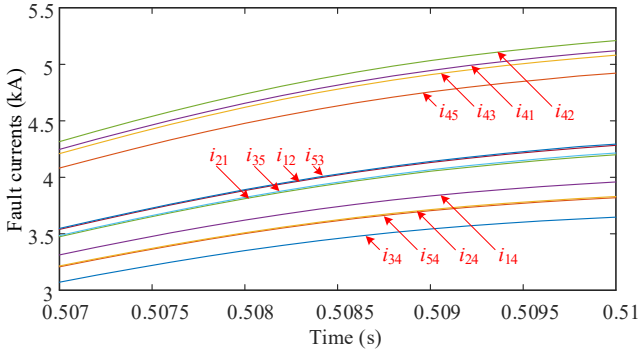


Fig. 13 The simulation results of fault current around 10ms after fault.

TABLE IV
FAULT CURRENTS OF TOPOLOGY ④ IN SEQUENCE

Fault Current No.	i_{42}	i_{41}	i_{43}	i_{45}	i_{53}	i_{12}
Fault current value at 10ms (kA)	5.21	5.12	5.08	4.92	4.29	4.28
$Index_{PTG\_line ij}$ (p.u.)	9.47	9.39	9.34	9.24	7.30	7.24
Fault Current No.	i_{35}	i_{21}	i_{14}	i_{24}	i_{54}	i_{34}
Fault current value at 10ms (kA)	4.22	4.20	3.96	3.82	3.81	3.65
$Index_{PTG\_line ij}$ (p.u.)	7.12	7.08	6.29	6.28	6.27	6.26

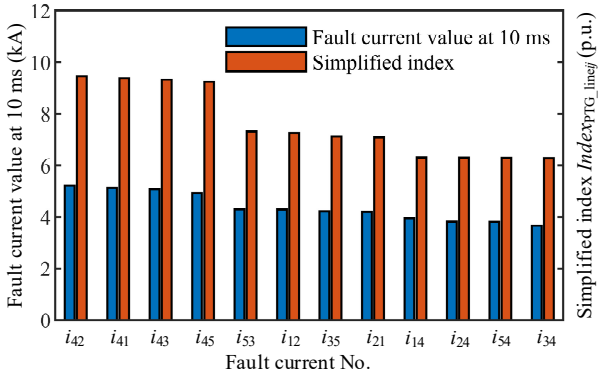


Fig. 14 The bar diagram of TABLE IV.

To compare the actual fault current value and simplified index directly, Fig. 14 also presents the bar diagram for better observation. According to these results, the changing situation of the current values and indexes are the same, hence it can be concluded that the simplified index is suitable to represent the fault current. And of course, the fitness value of this topology, which is the fault current level, is the maximum index 9.47.

B. *Topology Optimization Based on Genetic Algorithm*

Based on the simplified index, this part will optimize the topology through genetic algorithm. The number of the population is set to 200, and the maximum generation number is 50. After the computer calculation, the final output chromosome and the fitness function value are shown in Fig. 15, which is a ring network actually.

Topology ② - topology ⑥ are randomly selected topologies for further comparison, as Fig. 16 shows. The values in the figures are the maximum values of 10 ms' fault current in each topology; and the red arrows marks the location and direction of the maximum fault current in this topology. As reflected by the results, the order of fitness function values corresponds to that of the maximum fault current, which verifies the effectiveness of the proposed optimization algorithm. The maximum fault current is reduced by at least 1 kA compared with topology ⑥, which is about 20% of the original value. It proves that the fault current limitation of DC grid can be reached by topology optimization.

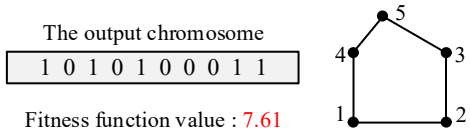


Fig. 15 Optimization results.

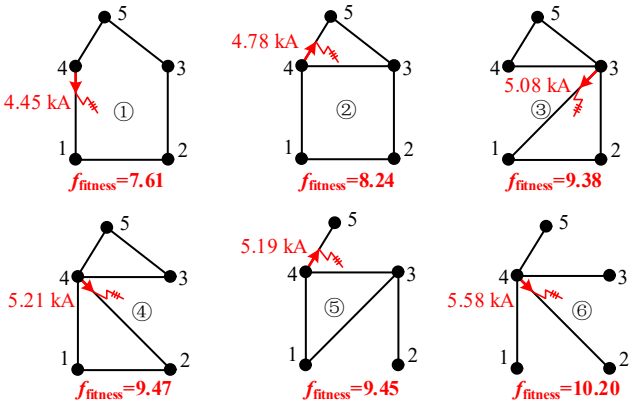


Fig. 16 Comparison of different topologies.

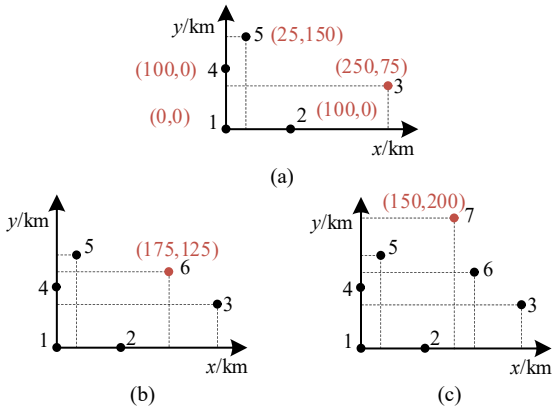


Fig. 17. The coordinates of (a) another five converters, (b) six converters and (c) seven converters.

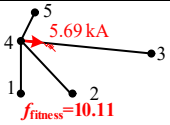
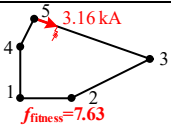
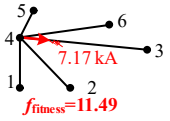
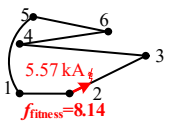
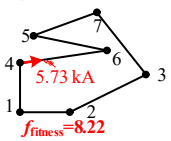
C. *Superiority of Topology Optimization*

For further demonstrating the effectiveness of topology optimization, a new geographical distribution of five converters is visualized in Fig. 17(a). Base on that, the scale of the system is expanded to six-terminal and seven-terminal grids, as shown in Fig. 17(b) and Fig. 17(c). The converters' parameters are still the same as listed in Table III. The optimization results are organized in Table V. The maximum fault current of each topology and its location are labeled therein. From the optimization results, we can draw the following conclusions.

(1) The maximum pole-to-ground fault current can be reduced by 44%, 22% and 30% respectively, which manifests that the current limiting effect of topology optimization is significant.

(2) The structures of the optimal topology are all ring structure, while that of the worst topology all belong to the same type, i.e., radial structure.

TABLE V
OPTIMIZATION RESULTS

Number of terminals	The inferior topology	The optimal topology	Decrease percentage
5			44%
6			22%
7			30%

Based on the above conclusions, two guiding proposals for practical application are given as follows.

i. An optimized topology is beneficial to reduce devices investment and relieve the pressure of protection.

The maximum fault component of pole-to-ground fault current is predictable, which can be suppressed by topology optimization in the stage of design, so that the size and investment of grounding devices can be reduced, and the power loss during operation can also be reduced accordingly [28]. In addition, the time constraints imposed on protection and DCCBs can be less stringent.

ii. The mesh structure or ring structure is recommended in the DC grid.

In a radial DC system, once a pole-to-ground fault occurs at the longest DC line connected to the radiation center, the fault line will bear the feed-in currents of all converters except the opposite one, and the overall impedance of current paths is the minimum. As a result, the fault current will be greater than that of other lines or even the maximum current of other topologies, as i_{43} in the five-terminal and six-terminal grid, and i_{61} in the seven-terminal grid shown in the second column of Table V. Therefore, the radial structure is not recommended for the construction of DC grid from the perspective of fault handling.

The mesh structures exist in the optimal topologies of all cases studied, accurately, the ring structure is likely to be the optimal one upon most occasions. The redundant lines in DC grid contribute to the balanced distribution of fault current, and significantly improve the reliability of power supply of course [29], [30]. The fault-limiting-oriented optimized topologies are consistent with the development direction of DC grid.

D. Cooperation with other topology optimization methods

In terms of technology, reducing the fault current level is beneficial to enhance the effectiveness of DC circuit breakers, which can improve the power supply reliability and reduce the investment of fault current limiters and breakers.

But it is usually difficult to achieve the optimal technical and economic performance with one method. Therefore, it is necessary to propose several topology schemes for different application scenarios. By combining with the factors used in conventional grid planning, the composite topology design method can be considered in different ways as follows.

(1) According to the conventional topology design method (considering application scenarios, economy, reliability, flexibility, etc.), several feasible topology schemes can be selected firstly, and then these topologies can be evaluated through the proposed simplified index and be optimized to limit the fault current level.

(2) By optimizing the topology through the method proposed in this paper, several optimum alternative topology schemes can be obtained with limited fault current level, and then these topologies can be finally evaluated from the other technical and economic aspects to obtain the best topology.

(3) Based on the proposed fault current evaluation index, combined with the indexes used for conventional topology design, the comprehensive index of topology optimization can be designed and the topology can be optimized at once.

VI. CONCLUSION

This paper investigates the characteristic of pole-to-ground fault in symmetrical mono-pole DC grid, and optimizes the DC topology to limit the fault current level. Based on the analysis above, the follow conclusions can be obtained:

(1) The proposed calculation method with both faulty pole and healthy pole considered has high accuracy, and can facilitate the analysis of influence factors on pole-to-ground fault.

(2) Different from the situation of pole-to-pole fault, the fault component of pole-to-ground fault current is influenced by topology of DC grid.

(3) To evaluate the above influence effect and calculate the pole-to-ground fault current value in an efficient way, a simplified index is proposed and is proved to be effective.

(4) Through the proposed index, the topology of symmetrical mono-pole DC grid can be optimized to limit the pole-to-ground fault current level based on genetic algorithm, which is helpful to reduce the investment of grounding devices and the pressure on protection design and DCCB interrupting.

(5) The results of several studied cases show that the mesh structure or ring structure is recommendable for DC grid construction.

REFERENCES

[1] T. An, G. Tang and W. Wang, "Research and application on multi-terminal and DC grids based on VSC-HVDC technology in China," *High Voltage*, vol. 2, no. 1, pp. 1-10, Mar. 2017.

[2] T. An et al., "A DC grid benchmark model for studies of interconnection of power systems," *CSEE J. Energy Syst.,* vol. 1, no. 4, pp. 101-109, Dec. 2015.

[3] A. Lesnicar, and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in Proc. *2003 IEEE Bologna Power Tech. Conf.*, Bologna, Italy, 2003, pp. 1-6.

[4] W. Xiang, S. Yang, L. Xu, J. Zhang, W. Lin and J. Wen, "A transient voltage-based DC fault line protection scheme for MMC-based DC grid embedding DC breakers," *IEEE Trans. Power Del.,* vol. 34, no. 1, pp. 334-345, Feb. 2019.

[5] B. Li, J. He, Y. Li, W. Wen and B. Li, "A novel current-commutation-based FCL for the flexible DC grid," *IEEE Trans. Power Electron.*, vol. 35, no. 1, pp. 591-606, Jan. 2020.

[6] W. Zhou et al., "Development and test of a 200kV full-bridge based hybrid HVDC breaker," *2015 17th European Conference on Power Electronics and Applications*, Geneva, 2015, pp. 1-7.

[7] S. Yang, W. Xiang, X. Lu, W. Zuo and J. Wen, "An adaptive reclosing strategy for MMC-HVDC systems with hybrid DC circuit breakers," *IEEE Trans. Power Del.,* vol. 35, no. 3, pp. 1111-1123, Jun. 2020.

[8] Y. Li et al., "DC fault detection in MTDC systems based on transient high frequency of current," *IEEE Trans. Power Del.,* vol. 34, no. 3, pp. 950-962, Jun. 2019.

[9] J. Li, Y. Li, L. Xiong, K. Jia and G. Song, "DC fault analysis and transient average current based fault detection for radial MTDC system," *IEEE Trans. Power Del.,* vol. 35, no. 3, pp. 1310-1320, Jun. 2020.

[10] J. Mei, G. Fan, R. Ge, B. Wang, P. Zhu and L. Yan, "Research on coordination and optimal configuration of current limiting devices in HVDC grids," *IEEE Access*, vol. 7, pp. 106727-106739, Jul. 2019.

[11] J. Xu, X. Zhao, N. Han, J. Liang and C. Zhao, "A thyristor-based DC fault current limiter with inductor inserting–bypassing capability," *IEEE J. Emerg. Sel. Topics Power Electronics,* vol. 7, no. 3, pp. 1748-1757, Sep. 2019.

[12] T. Ghanbari, E. Farjah and N. Tashakor, "Thyristor based bridge-type fault current limiter for fault current limiting capability enhancement," *IET Gener. Transmiss. Distrib.*, vol. 10, no. 9, pp. 2202-2215, Jun. 2016.

[13] D. Keshavarzi, E. Farjah and T. Ghanbari, "Hybrid DC circuit breaker and fault current limiter with optional interruption capability," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 2330-2338, March 2018.

[14] S. He, G. Zou, C. Sun and S. Liu, "Fault section locating method and recovery strategy of pole-to-ground fault for medium voltage direct current (MVDC) distribution network," *J. Eng.*, vol. 2019, no. 16, pp. 668-673, Mar. 2019.

[15] L. Lin, Z. He, J. Hu, Z. He and K. Xu, "Pole-to-ground fault ride through strategy for half-/full-bridge hybrid MMC-based radial multi-terminal HVDC systems with low-impedance grounded," *IET Gener. Transmiss. Distrib.*, vol. 12, no. 4, pp. 1038-1044, Feb. 2018.

[16] T. Bi, S. Wang and K. Jia, "Single pole-to-ground fault location method for MMC-HVDC system using active pulse," *IET Gener. Transmiss. Distrib.*, vol. 12, no. 2, pp. 272-278, Jan. 2018.

[17] M. Langwasser, G. De Carne, M. Liserre and M. Biskoping, "Fault current estimation in multi-terminal HVdc grids considering MMC control," *IEEE Trans. Power Syst*., vol. 34, no. 3, pp. 2179-2189, May. 2019.

[18] Z. He, J. Hu, L. Lin and Z. He, "Pole-to-Ground Fault Analysis for MMC-HVDC Grid," *2019 10th International Conference on Power Electronics and ECCE Asia (ICPE 2019 - ECCE Asia)*, Busan, Korea (South), 2019, pp. 2984-2989.

[19] S. Xue, J. Lian, J. Qi, et al. "Pole to ground fault analysis and fast protection scheme for HVDC based on overhead transmission line," *Energies*, vol. 1059, no. 10, pp. 1-17, Apr. 2017.

[20] W. Leterme, P. Tielens, S. De Boeck and D. Van Hertem, "Overview of grounding and configuration options for meshed HVDC grids," *IEEE Trans. Power Del.*, vol. 29, no. 6, pp. 2467-2475, Dec 2014.

[21] M. K. Bucher and C. M. Franck, "Comparison of fault currents in multiterminal HVDC grids with different grounding schemes," *2014 IEEE PES General Meeting*, National Harbor, MD, 2014, pp. 1-5.

[22] Yan, Tao, Baohong Li and Tianqi Liu, "The basic theory research of multi-voltage HVDC grid," Sichuan university, Chengdu, China, Tech. Rep. TR-01, Nov. 2019.

[23] C. Li, C. Zhao, J. Xu, Y. Ji, F. Zhang and T. An, "A pole-to-pole short-circuit fault current calculation method for DC grids," *IEEE Trans. Power Syst*., vol. 32, no. 6, pp. 4943-4953, Nov. 2017.

[24] H. Yang, Y. Dong, W. Li and X. He, "Average-value model of modular multilevel converters considering capacitor voltage ripple," *IEEE Trans. Power Del.*, vol. 32, no. 2, pp. 723-732, Apr 2017.

[25] R. Alipour-Sarabi, Z. Nasiri-Gheidari, F. Tootoonchian and H. Oraee, "Improved winding proposal for wound rotor resolver using genetic algorithm and winding function approach," *IEEE Trans. Ind. Elect.*, vol. 66, no. 2, pp. 1325-1334, Feb. 2019

[26] G. Granelli, M. Montagna, F. Zanellini, P. Bresesti et al., "A genetic algorithm-based procedure to optimize system topology against parallel flows," *IEEE Trans. Power Syst*., vol. 21, no. 1, pp. 333-340, Feb. 2006.

[27] Firoz Mahmud and Syed Tauhid Zuhori, *Genetic Algorithm*. Saarbrucken, GER: Lambert Academic Publishing, 2012, pp. 123–135.

[28] J. Hu, K. Xu, L. Lin and R. Zeng, "Analysis and enhanced control of hybrid-MMC-based HVDC systems during asymmetrical DC voltage faults," *IEEE Trans. Power Del.*, vol. 32, no. 3, pp. 1394-1403, Jun 2017.

[29] G. Tang, Z. He, H. Pang, X. Huang and X. Zhang, "Basic topology and key devices of the five-terminal DC grid," *CSEE J. Energy Syst.,* vol. 1, no. 2, pp. 22-35, Jun. 2015

[30] D. van Hertem and M. Ghandhari, "Multi-terminal vsc hvdc for the european supergrid: Obstacles," *Renew. Sustain. Energy Rev.,* vol. 14, no. 9, pp. 3156–3163, 2010.

Yan Tao received the B.S degree in Electrical Engineering from Sichuan University in 2017. Currently, she is pursuing the Ph.D. degree in the College of Electrical Engineering, Sichuan University, Chengdu, China. Her research interests include power system stability analysis and control, and high voltage direct current transmission technology.

Baohong Li (S' 16, M' 19) received the B.S, M.S. and Ph.D. degrees from the college of Electrical Engineering and Information Technology, Sichuan University, Chengdu, China in 2009, 2015 and 2018 respectively. He was with State Grid Corporation of China until 2012. His research interests include power system stability analysis and control, high voltage direct current transmission technologies, and DC grids. He is presently a lecturer in the college of Electrical Engineering, Sichuan University, Chengdu, China.

Tomislav Dragicevic(S'09–M'13–SM'17) received the M.Sc. and Industrial Ph.D. degrees in electrical engineering from the Faculty of Electrical Engineering, Zagreb, Croatia, in 2009 and 2013, respectively. From 2013 to 2016, he was a Postdoctoral Research Associate, and since March 2016, he has been an Associate Professor with Aalborg University, Denmark, where he leads the Advanced Control Lab. He made a guest professor stay at Nottingham University, U.K., in 2018. He has authored or coauthored more than 170 technical articles in his domain of interest, eight book chapters, and a book in the field. His research interests include design and control of micro grids and application of advanced modeling and control concepts to power electronic systems.

Tianqi Liu (SM' 16) received her B.S. and M.S. degrees from Sichuan University in 1982 and 1986, respectively, and Ph.D. degree from Chongqing University in 1996, all are in Electrical Engineering. Currently, she is a professor in College of Electrical Engineering and Information Technology at Sichuan University. Her main research interests are power system stability, HVDC, optimal generation dispatch, dynamic security analysis, dynamic state estimation and load forecast.

Frede Blaabjerg (S'86–M'88–SM'97–F'03) received the Ph.D. degree in electrical engineering from Aalborg University, Aalborg, Denmark, in 1995, and the honoris causa from the University Politehnica Timisoara (UPT), Timi¸soara, Romania, and Tallinn Technical University (TTU), Tallinn, Estonia. He has authored/coauthored more than 600 journal papers in the fields of power electronics and its applications. His current research interests include power electronics and its applications, such as in wind turbines, PV systems, reliability, harmonics, and adjustable speed drives. Prof. Blaabjerg is a recipient of 30 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, and the Villum Kann Rasmussen Research Award 2014. He was the Editor-in-Chief for the IEEE T ON POWER ELECTRONICS from 2006 to 2012. Since 2019, he has been serving as the President of the IEEE Power Electronics Society.