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Symmetrical Bipolar Output Isolated Four-Port Converters Based on Center-Tapped Winding for Bipolar DC Bus Applications

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***Abstract*- Using a multi-port converter to integrate renewable energy and energy storage into the bipolar dc bus is a desirable solution due to its high efficiency and reliability. In this paper, a series of bipolar output active rectifiers with center-tapped winding are proposed to serve as secondary rectification circuits. Then, a family of isolated four-port converters with symmetrical bipolar outputs is further developed to integrate renewable energy and energy storage. The proposed symmetrical bipolar output isolated four-port converters can achieve single-stage power conversion, symmetrical bipolar output voltage, soft switching, and an approximately decoupled control loop. A typical four-port converter, named full-bridge interleaving bidirectional buck/boost + semi-active rectifier with bipolar output converter, is specifically analyzed in detail in terms of operation principles, voltage and power relationship, port current ripples, soft switching performance, and control method. Finally, experimental verifications have been carried out to illustrate the feasibility and effectiveness of the proposed topology.[1]**

***Index Terms*—Renewable energy system, four-port converter, symmetrical bipolar output, bipolar dc bus, phase shift modulation, pulse width modulation, soft switching**

I. INTRODUCTION

The development and utilization of renewable energy sources (RESs), such as solar energy, wind energy, tidal energy, etc., are attracting more and more attention due to their great potential in effectively solving environmental pollution and energy crisis [1]. However, depending on climate and other environmental conditions, the generation power of RES is intermittent. Thus, RESs are generally combined with energy storage systems (ESSs), such as batteries and ultracapacitors, to provide stable and reliable power supply loads, microgrids, or grid-connected inverters [2]-[4]. In general, many RESs and ESSs, such as photovoltaic (PV) panels power generation, Li-ion batteries, light-emitting diode (LED), and electric vehicles (EVs), have dc output characteristics. Therefore, the integration of RESs and ESSs into dc micro-grids is an effective way to clear generation power because of the dc characteristics of many sources and loads [5], [6].

According to the characteristics of bus voltages, the architecture of the dc microgrids can be divided into unipolar dc bus and bipolar dc bus structures, corresponding to the unipolar dc microgrid and the bipolar dc microgrid, respectively. Although unipolar dc bus architecture has been widely used in the past, it is becoming challenging to meet the requirements of many emerging applications in terms of efficiency and reliability, e.g., data centers and fast EV charging stations [7], [8]. Compared with the unipolar dc bus, the following advantages make the bipolar dc structure more attractive.

1) Bipolar dc bus systems are more reliable because one of the dc buses can operate correctly even when the other dc bus is in a faulty condition.

2) Compared with the unipolar dc structure, the efficiency of bipolar dc bus systems is higher under the same load because the bus current is smaller when the power is transmitted through the two dc buses.

3) A bipolar dc bus can provide three alternative voltage levels, including two symmetrical positive and negative polarity voltages, offering paramount flexibility and interface with various voltage-ranged loads.

4) In the bipolar dc bus system, the voltage gain requirement of the interface converter is reduced by half. For example, the conventional 400 V dc bus in the unipolar dc bus corresponds to ±200 V in the bipolar dc bus.

As a result, the bipolar dc bus system can provide higher flexibility, reliability, and efficiency [8]-[10], which has been widely used in intelligent industrial parks, residential buildings, and data centers, e.g., the data center at Intel Corporation and the medium-voltage dc distribution network in Zhuhai, China. In the conventional bipolar dc bus system, the common ground bipolar dc bus is constructed through a voltage balancer. Then, RESs, ESSs, and loads are connected to the bipolar dc bus with a series of independent dc-dc converters, which incurs high cost and low efficiency, and has difficulty achieving centralized control [11], [12]. Alternatively, a multi-port converter (MPC) can be employed to integrate RESs, ESSs, and various loads into the bipolar dc bus, which exhibits many advantages like the single-stage

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power conversion, higher system efficiency, and unified power management, compared to the conventional bipolar dc bus system [13], [14].

In general, the topologies of MPCs can be classified into three categories: non-isolated topologies [15]-[17], partially isolated topologies [18]-[20], and fully isolated topologies [21]. The partially isolated MPC topology is an excellent candidate because it combines the advantages of fully isolated and non-isolated topologies, and is often used in low and medium-power applications that require galvanic isolation between the RES and load. Therefore, a lot of research efforts have been made on this type of MPCs. In [22] and [23], full-bridge MPCs based on a secondary-side phase shift control are presented, with a wide input range, high efficiency, and low voltage stress for RES applications. The MPC based on the secondary active voltage six-folder rectifier is further proposed to achieve a higher voltage gain and extend the soft-switching range in [18]. Other MPC topologies, such as LLC-MPC in [24], half-bridge MPC in [19], and three-level MPC in [20], have also been extensively studied. However, the MPCs described above may fail when they are used to integrate RESs and ESSs into a bipolar dc bus system due to their unipolar output characteristics.

For the application scenario of bipolar dc buses, such as EV charging stations and data centers, a symmetrical and common ground bipolar output voltage is promising to improve power quality and reliability. To realize a symmetrical bipolar output voltage, the neutral point clamped three-level converter is proposed for EV fast-charging stations in [25], providing a bipolar voltage to the loads. A series of voltage balancers derived from basic dc-dc converters is presented in [26], which have the advantages of simple open-loop control and low cost. However, the asymmetry of the positive and negative voltages due to the load asymmetry limits its applications. Various voltage balancing control methods are proposed in [27] to overcome this limitation, which is relatively complexed.

In [28], a four-port dc-dc converter with a bipolar output is proposed for interfacing PV modules and fuel cells to the bipolar dc bus, which lacks the bidirectional power flow port required to connect to ESSs. In [29], a novel four-port converter combining the three-port SEPIC converter and the three-port Cuk converter is presented to integrate the RES and ESS to the bipolar dc bus, which has the inherent characteristics of symmetrical bipolar output voltage, simple structure, and easy to control implement. However, hard switching characteristics and lack of galvanic isolation hinder its applications. In [30] and [31], a dc/dc converter with bipolar output and integrated bus voltage balance capability based on the CLLC bidirectional resonant converter and voltage balancer is presented. The converter has the advantages of isolated bipolar output ports, soft switching, and high efficiency. In [32] and [33], two three-level dual active bridge converters based on diode clamping are presented to achieve single-stage power conversion between RES and bipolar load. However, additional voltage balance control is required under load imbalance conditions, which increases the complexity of the control method.

With the above, this paper proposes a series of novel symmetric bipolar output rectifiers based on center-tapped windings for the secondary side of MPCs, which achieves the bipolar output voltage control through a phase shift modulation method. Moreover, a new family of isolated four-port converters with symmetric bipolar outputs is further developed by combining the proposed rectifiers and specific primary side circuits. The proposed topologies have the following advantages, making them very promising for integrating RESs and ESSs.

1) Single-stage power conversion among RESs, ESSs, and bipolar loads is realized, which helps lower the cost and improve the system's efficiency.

2) Voltages on the positive polarity output (PPO) and negative polarity output (NPO) ports are symmetric irrespective of the operating states. Thus, additional voltage balancing control is not required, reducing the overall control complexity.

3) Power control of RESs and ESSs is optimized on the primary side, and the constant bipolar output voltage control is achieved on the secondary side. More importantly, the two control loops are approximately decoupled.

The rest of this paper is organized as follows. In Section II, the basic principle to develop the proposed novel rectifiers with symmetric bipolar outputs is presented and a new family of isolated four-port converters with symmetric bipolar output is deduced. In Section III, the operation modes and equivalent circuits of an example converter, named full-bridge interleaving bidirectional buck/boost + semi-active rectifier with bipolar output (FB-IB3+SAR-BO), are analyzed in detail. In Section IV, performance characteristics, including voltage and power, soft switching, input current ripple, and control, are analyzed. Experimental results are presented in Section V to illustrate the effectiveness of the proposed converter. Finally, the conclusion is given in Section VI.

II. Topology Derivation of Isolated Four-Port Converters with Symmetric Bipolar Output

A. Structure of the Proposed Converters

The general structure of the proposed symmetric bipolar output isolated four-port converter based on center-tapped windings is shown in Fig. 1, which consists of the primary side circuit, the secondary side circuit, and the high-frequency transformer. The RES port and ESS port are integrated into the primary side of the converter to achieve galvanic isolation of the RES and ESS from the load. The PPO port and NPO port with common ground characteristics are integrated into the secondary side of the converter to obtain symmetrical bipolar output voltages. Furthermore, to provide the necessary galvanic isolation and flexible voltage level for the output port, a high-frequency transformer with a center tap is inserted between the primary and secondary sides, and its center tap is connected to the common ground of the PPO and NPO ports.

In general, there are various implementation possibilities on the primary side with inverter characteristics, such as half-bridge, full-bridge, LLC, etc. On the other hand, the secondary side usually serves as a rectification circuit to achieve symmetric bipolar dc voltage outputs. Therefore, the key is how to construct a secondary side rectifier with symmetrical bipolar output characteristics.

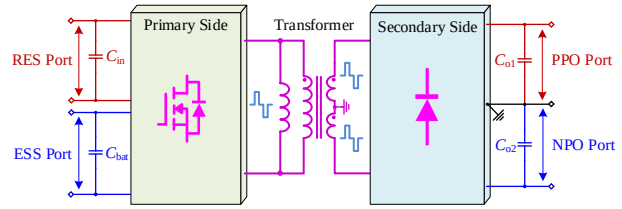


Fig. 1. The general structure of the proposed isolated four-port converter with bipolar outputs, where C_{in} and C_{bat} are filter capacitors for the RES and the ESS ports respectively, and C_{o1} and C_{o2} are filter capacitors for the PPO and NPO ports.

B. Derivation of Secondary Side Rectifiers

The conventional passive rectifiers based on single winding and center tap windings are shown in Figs. 2(a) and (b), respectively, which only include a unipolar output voltage. By combining the rectifier shown in Figs. 2(a) and (b), a novel symmetric bipolar output passive rectifier can be obtained, as shown in Fig. 2(c). The midpoints of the two diode legs are connected to the positive and negative terminals of the secondary side winding, while the center tap of the secondary side winding is connected to the common ground of the PPO and NPO ports to achieve the symmetric bipolar output voltage with common ground.

The bipolar output rectifier shown in Fig. 2(c) cannot be directly used as the secondary side circuit of the four-port converter shown in Fig. 1, as it lacks active switches to achieve bipolar voltage control. In general, the symmetric bipolar output voltage of the four-port converter must be controlled to be constant to meet the load requirements, which can be achieved by the active switches in the secondary side circuit. Meanwhile, the RES input must be controlled to maximize the energy harvesting, while the ESS voltage and current must be managed to ensure its safe operation. ESSs can be controlled through the switches on the primary side for the four-port converter shown in Fig. 1. Consequently, the essential issue is to modify the passive bipolar output rectifier shown in Fig. 2(c), so that it has the capability of symmetrical bipolar output voltage regulation.

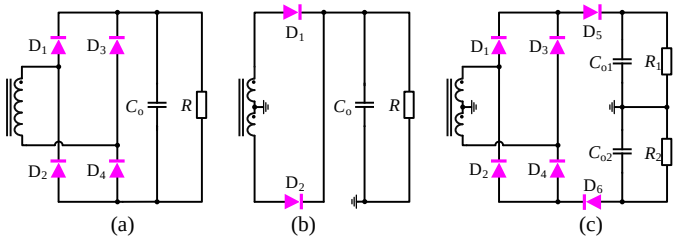


Fig. 2. Passive rectifier on the secondary side: (a) and (b) conventional unipolar output rectifiers, and (c) the proposed bipolar output rectifier.

Inspired by isolated three-port dc-dc converters [23], the output voltage can be regulated by replacing the diodes in the rectifier with active switches, or by inlaying a switching leg with the ability to regulate the output voltage in the rectifier. As a result, two families of rectifiers with symmetrical bipolar output and voltage regulation capabilities can be developed, as presented in Figs. 3 and 4.

The first family of secondary-side rectifier topologies with bipolar output and voltage regulation capability, is called semi-active rectifiers with bipolar output (SAR-BO). As shown in Fig. 3, semi-active rectifiers with bipolar outputs can be developed by replacing the complementary conducting diodes in the passive rectifier shown in Fig. 2(c) with active switches with complementary conducting. There are four possible solutions to do so. In fact, it is also feasible to replace all four diodes D_1 ~ D_4 with active switches, as a full-active rectifier. This structure helps to improve efficiency because of the lower conduction loss compared to the solution of replacing only two diodes. However, more active switches will increase the system cost, so this solution is not shown in Fig. 3.

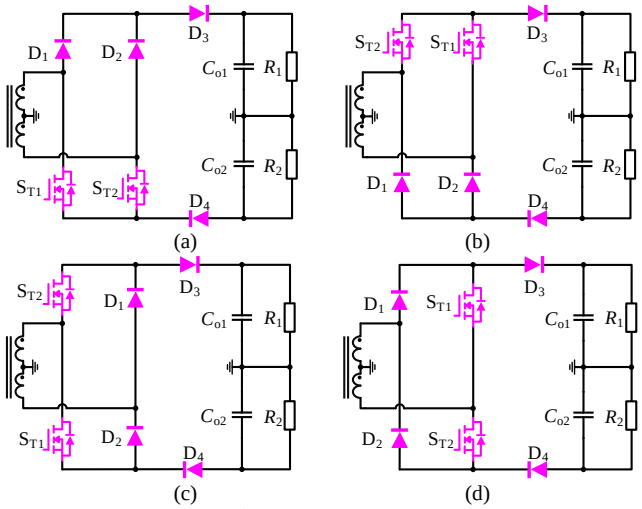


Fig. 3. Four semi-active rectifiers with bipolar outputs.

The second family of secondary-side rectifier topologies with bipolar outputs and voltage regulation capability is named active clamping rectifier with bipolar output (ACR-BO). As shown in Fig. 4, the reverse-connected switches S_{T1} and S_{T2} can be embedded between the diode legs midpoint of the rectifier or between the diode leg and the output port reference ground, as shown in Figs. 4(a) and (b). In addition, the forward series switches S_{T1} and S_{T2} can be inserted in front of or behind the diodes D_5 and D_6, as shown in Figs. 4(c) and (d).

C. Structure of the Primary Side

For the four-port converter with bipolar output, as shown in Fig. 1, the primary side circuit is mainly used to invert the dc input voltage of RESs and ESSs into the high-frequency ac voltage and then supplied to the transformer. Also, the primary side circuit should achieve maximum energy harvesting and safe charging and discharging of energy storage elements. As

a result, the available circuit structure on the primary side is not unique and has many possible forms. Some possible primary side circuit structures are shown in Fig. 5, including forward, half-bridge, full-bridge, full-bridge + interleaving bidirectional buck/boost (FB-IB3), LLC + interleaving bidirectional buck/boost (LLC-IB3), and full-bridge LLC. As shown in Fig. 5, V_{in} corresponds to the RES port in Fig. 1, and V_{bat} corresponds to the ESS port in Fig. 1. The primary side circuit integrates the RES and ESS ports, and the switching element and the primary side winding are shared by two ports, which reduces the cost of the system while improving the overall efficiency.

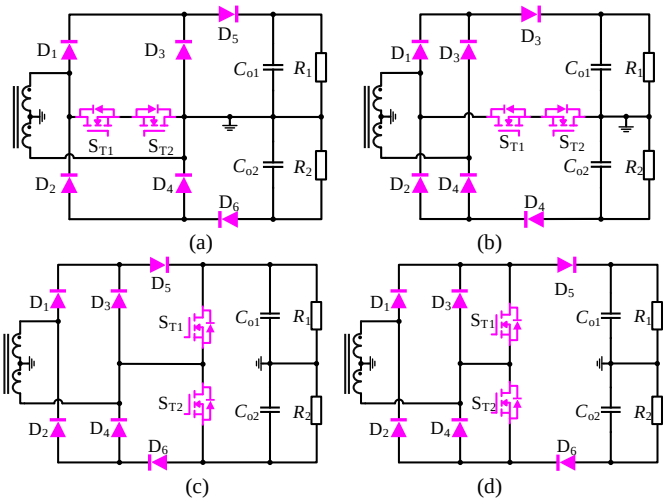


Fig. 4. Four active clamping rectifiers with bipolar outputs.

It is worth noting that all the primary side circuits shown in Fig. 5 can achieve optimal control of RES and ESS, but the corresponding modulation methods are different. For example, the forward, half-bridge, full-bridge, and FB-IB3 all use pulse width modulation (PWM), the LLC-IB3 adopts pulse frequency modulation (PFM), and the full-bridge LLC employs phase-shift modulation (PSM). Detailed control and modulation principles are presented in detail in Section IV.

D. Topology Derivation

The various primary side circuits shown in Fig. 5 can be combined freely with the different secondary side circuits shown in Figs. 3 and 4 to develop a family of isolated four-port converters with symmetric bipolar outputs. Two example topologies, which are derived by connecting LLC-IB3 and SAR-BO [Fig. 3(a)], and combining the forward and ACR-BO [Fig. 4(c)] are illustrated in Fig. 6. Close observation indicates that the proposed family of isolated four-port converters with symmetrical bipolar outputs have the following features:

1) Flexible and various primary and secondary candidate topologies can be used for different applications and facilitate engineering design.

2) Single-stage power conversion among the RES, ESS, and bipolar output ports is achieved, which is helpful to improve the efficiency of the system.

3) Control loops of the primary and secondary sides are entirely independent. The power optimization control of RESs and ESSs is realized on the primary side with PWM or PFM, and the PSM method is used for the secondary side to achieve a constant symmetrical bipolar output voltage.

4) Soft switching, including zero voltage switching (ZVS) for all switches and zero current switching (ZCS) for all diodes, can be achieved in a wide range to reduce the switching losses and further improve efficiency.

In order to enable the designer to select the appropriate circuit configuration for different applications, the performance of the secondary side rectifier, as shown in Figs. 3 and 4, and the primary side circuits, as shown in Fig. 5, are compared, as shown in Table I and Table II, respectively. The number of components, control method, soft switching, output voltage gain, design difficulty, and current stress are listed as important performance and design considerations in Tables I and II. As the comparison results show, both SAR-BO and ACR-BO have inherent soft switching performance on the secondary side. In addition, both control the bipolar output voltage through the PSM of secondary side switches. On the other hand, SAR-BOs have fewer components and lower current stress but lack sufficient output voltage gain capability than ACR-BO. Therefore, the ACR-BO shown in Fig. 4 is more suitable to be selected as a secondary circuit for applications with higher output voltage levels, while the SAR-BO as demonstrated in Fig. 3 is more appropriate for applications with lower voltage levels and low cost.

It can be seen from Table II that although the forward structure shown in Fig. 5(a) has the advantages of simple control and fewer magnetic components, it has the disadvantages of difficulty in soft switching and the maximum duty cycle constraint caused by the demagnetization of the magnetic inductance. The half-bridge and full-bridge circuits shown in Figs. 5(b) and (c) also have the advantages of simple control and compact structure, but port voltage constraints and large current ripple make them uncompetitive for interfacing the RES. Similarly, the properties and characteristics of other primary side structures are shown in Table II and will not be described in detail. Therefore, the designer should reasonably choose the appropriate primary side circuit and secondary side circuit according to the application and requirements, so as to construct a circuit topology that considers various performance compromises.

It is worth noting that the low input current ripple, low current stress, and soft switching performance of the FB-IB3 circuit shown in Fig. 5(d) make it ideal for integrating RES and ESS on the primary side. Moreover, the low current stress, soft switching, and easier ground-side drive characteristics of the SAR-BO shown in Fig. 3(a) make it a better candidate for low output voltage applications. Therefore, the FB-IB3+SAR-BO converter as shown in Fig. 7 is analyzed in detail as an example in the rest of this paper.

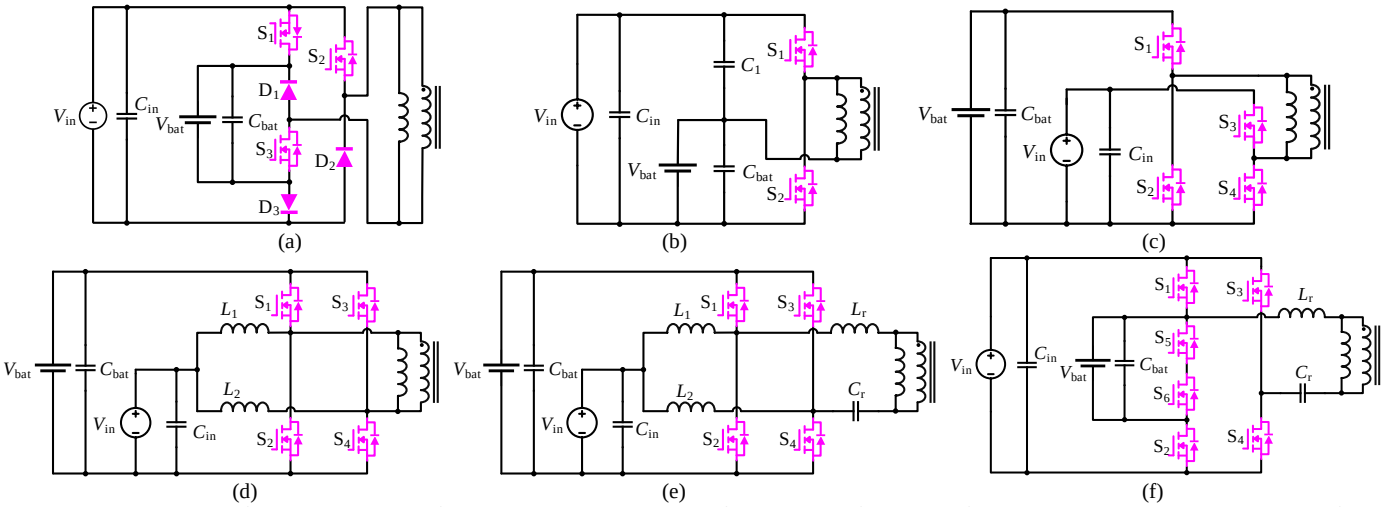


Fig. 5. Example topologies of primary side circuits for integrating RES and ESS: (a) forward, (b) half-bridge, (c) full-bridge, (d) FB-IB3, (e) LLC-IB3, and (f) full-bridge LLC.

TABLE I. PERFORMANCE COMPARISON OF SECONDARY SIDE CIRCUIT STRUCTURES

Secondary side circuit	Number of components (S&D)	Soft switching	Current stress of semiconductor devices	Output voltage gain	Control method
SAR-BO [Fig. 3]	2 + 4	Inherent ZVS and ZCS	Low	Low	PSM
ACR-BO [Fig. 4]	2 + 6	Inherent ZVS and ZCS	Moderate	High	PSM

TABLE II. PERFORMANCE COMPARISON OF PRIMARY SIDE CIRCUIT STRUCTURES

Primary side circuit	Number of components		Control method	Soft switching	Design difficulty	Current stress of semiconductor devices	Other features
	S&D	L					
Fig. 5(a)	6	0	PWM	No	Moderate	High	Existing the maximum duty cycle constraint
Fig. 5(b)	2	0	PWM	ZVS	Low	High	Existing the port voltage range constraint
Fig. 5(c)	4	0	PWM	ZVS	Moderate	Moderate	High port current ripple
Fig. 5(d)	4	2	Interleaved PWM	ZVS	Moderate	Low	Low port current ripple for interfacing RES
Fig. 5(e)	4	3	Interleaved PWM + PFM	ZVS	High	Moderate	Limited output voltage gain; Low port current ripple for interfacing RES
Fig. 5(f)	6	1	PSM	ZVS	High	High	High port current ripple

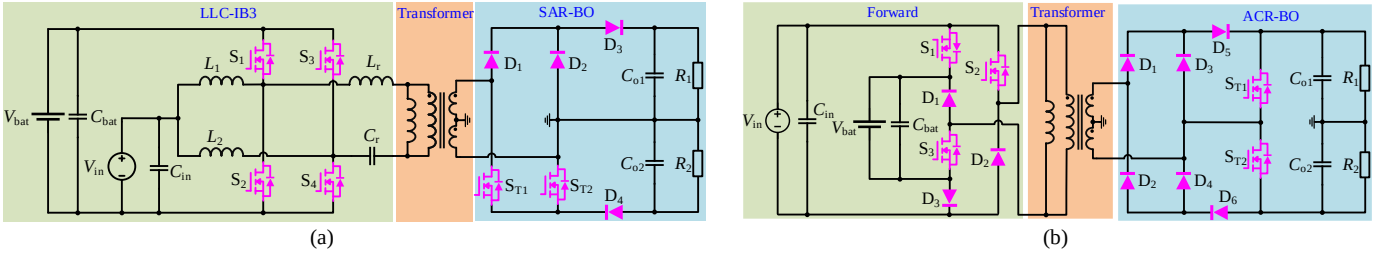


Fig. 6. Example topologies of the proposed isolated four-port converters with symmetrical bipolar output: (a) combination of FB-IB3 and SAR-BO converter, and (b) combination of the forward and ACR-BO.

III. Operating Principle

A. Converter Description and Operation Mode

To have a better understanding of the proposed converters, a symmetrical bipolar output four-port converter as a combination of FB-IB3 and SAR-BO (see Fig. 7) will be exampled in this section. FB-IB3 and SAR-BO are selected as the primary and secondary side circuits due to the wide soft-switching range and the small number of semiconductors and magnetic components. As it can be seen from Fig. 7, the primary side is an interleaving bidirectional buck-boost unit, including two inductors (L_1 and L_2) and four switches S_1 ~ S_4. The driving signals for S_1 and S_2 (S_3 and S_4) are complementary. i_{L1} and i_{L2} are the currents of inductors L_1 and L_2, and I_{in} is the current of the RES. The two switch legs are driven in an interleaved manner with a phase shift angle of 180°, which helps to reduce the input current ripple of the RES port. The duty cycle of S_1 is defined as D, and the range of D is determined by the voltages of the RES port and ESS port. The turn ratio of the primary and secondary sides of the transformer is 1:n:n. On the secondary side of the converter, S_{T1} and S_{T2} are driven complementarily with a fixed duty cycle of 0.5, and the bipolar output port power is regulated by phase-shifting an angle of φ for S_1 and S_{T2}.

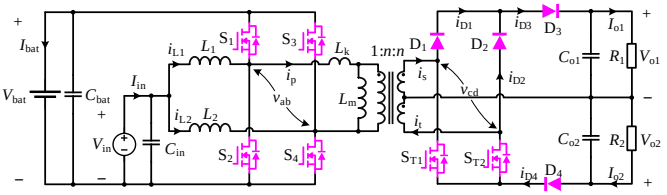


Fig. 7. Circuit diagram of the exemplified FB-IB3 + SAR-BO converter (one of the proposed converters).

When the proposed FB-IB3 + SAR-BO converter is used to integrates RES and ESS units to a bipolar dc bus, three main power flow paths, namely from the RES port to the bipolar load port, the RES port to the ESS port, and the ESS port to the bipolar load port, are identified. Assuming that P_{bat} is positive when the battery is charging and ignoring the power losses in the power conversion, the port power relationship can be obtained as

$$P_{in} = P_{bat} + P_{o1} + P_{o2} \tag{1}$$

where P_{in} and P_{bat} are the power flowing through the RES port and ESS port, respectively, P_{o1} and P_{o2} are the power of the PPO and NPO ports.

The operating modes of the four-port converter can be classified as the battery regulation mode (BRM) and battery independent power supply mode (BISM) according to whether there is power from the RES. In the BRM, the RES provides energy for bipolar loads with its maximum power, and the ESS is used as an energy buffer to regulate the constant bipolar output voltages. In the BISM, the RES is decoupled, and the power is delivered from the ESS to the load.

B. Operational Principle

The proposed FB-IB3 + SAR-BO converter can operate in the continuous current mode (CCM) or the discontinuous current mode (DCM) according to the conditions of the primary side winding current i_p. In this paper, the operation of the converter under the CCM is discussed and analyzed in detail for simplicity. In this case, there are 14 operation stages in one switching period. Considering the circuit symmetry, only seven operation stages in a half switching period are presented. The key waveforms are shown in Fig. 8, and the equivalent circuits in each switching stage are illustrated in Fig. 9. The comprehensive operational analysis of each mode is given as follows.

As shown in Fig. 8, v_{gs1} ~ v_{gs4} are the driving signal of switches S_1 ~ S_4, where S_1 and S_2 (S_3 and S_4) have complementary driving signals, and there is a phase shift of 180° between the driving signals of S_1 and S_3. Moreover, v_{gsT1} ~ v_{gsT2} are the driving signals of switches S_{T1} ~ S_{T2}, where S_{T1} and S_{T2} are switched complementarily with a fixed duty cycle of 0.5, while there is a phase shift of φ between the driving signals of S_1 and S_{T2}. v_{ab} and v_{cd} are the voltages between the midpoints of the primary-side inverter switch legs and secondary-side rectifier switch legs, respectively. i_p, i_s, and i_t are the currents of the primary side winding N_p, and secondary side windings N_s and N_t, respectively. i_{D1} ~ i_{D4} are the currents of diodes D_1 ~ D_4. Referring to the steady-state operation waveform shown in Fig. 8 and the equivalent circuits shown in Fig. 9, the operation of the proposed FB-IB3 + SAR-BO converter is can be analyzed:

Stage I [t_0 ~ t_1] [see Fig. 9(a)]: Before t_0, during the dead time between S_2 and S_1, S_4 and S_{T1} are turned on. The primary side winding current i_p flows through S_4 and the body diode of S_1. The inductor L_1 is linearly de-energized with the voltage $V_{in} - V_{bat}$, and i_{L1} is decreasing linearly. The inductor L_2 is linearly energized with the voltage V_{in}, and i_{L2} is increasing linearly. The secondary side windings N_s and N_t transfer power to NPO and PPO ports through S_{T1} and D_4, D_2, and D_3, respectively. At t_0, S_1 is turned on, and the operating state of the converter is exactly the same as that before t_0. In this stage, the primary side winding current i_p is expressed as

$$i_p(t) = i_p(t_0) + \left(V_{bat} + V_{o1}/n\right)\left(t - t_0\right)/L_k \tag{2}$$

Stage II [t_1 ~ t_2] [see Fig. 9(b)]: Assuming that the load currents of the PPO and NPO ports meet $I_{o1} > I_{o2}$, then, the diode currents meet $i_{D3} > i_{D4}$. At t_1, the diode current i_{D4} and the secondary side winding N_s current i_s decrease to 0. i_{L1} and i_{L2} are the same as in the previous stage. In this interval, only the secondary side winding N_t delivers power to the PPO port. This stage will end at t_2 when i_{D2} and i_{D3} decrease to 0. In this stage, i_p can be expressed as shown in (2).

Stage III [t_2 ~ t_3] [see Fig. 9(c)]: In this stage, the secondary side winding current i_s and i_t freewheel, only through S_{T1} and the body diode of S_{T2}, and no energy is delivered from the secondary side to the bipolar load. In this stage, i_p can be expressed as

$$i_p(t) = i_p(t_2) + V_{bat}\left(t - t_2\right)/L_k \tag{3}$$

And the phase shift angle φ can be given as

$$\varphi = 2\pi f_s\left(t_3 - t_0\right) \tag{4}$$

where $f_s = 1/T_s$ is the switching frequency with T_s being the switching cycle.

Stage IV [$t_3 \sim t_4$] [see Fig. 9(d)]: At t_3, S_{T1} is turned off and S_{T2} is turned on. The secondary side windings N_s and N_t transfer power to PPO and NPO ports through D_1 and D_3, S_{T2} and D_4, respectively. The primary side winding voltage v_{ab} and secondary side winding voltage v_{cd} are V_{bat} and $V_{o1} + V_{o2}$ respectively. In this stage, the primary side winding current i_p is obtained as

$$i_p(t) = i_p(t_3) + \left[V_{bat} - V_{o1}/n\right](t - t_3)/L_k \tag{5}$$

Stage V [$t_4 \sim t_5$] [see Fig. 9(e)]: This stage is the dead time period of S_1 and S_2. At t_4, S_4 is turned off. The inductors L_2 is linearly energized with the voltage V_{in}, and i_{L2} continues to increase linearly. The inductors L_1 starts to be linearly energized with the voltage V_{in}, and i_{L1} starts to increase linearly. The secondary side windings N_s and N_t transfer power to PPO and NPO ports through D_1 and D_3, S_{T2} and D_4, respectively. In this stage, the primary side winding current i_p is expressed as

$$i_p(t) = i_p(t_4) - V_{o1}(t - t_4)/(nL_k) \tag{6}$$

Stage VI [$t_5 \sim t_6$] [see Fig. 9(f)]: At t_5, S_2 is turned on. The converter operates exactly the same as in Stage V.

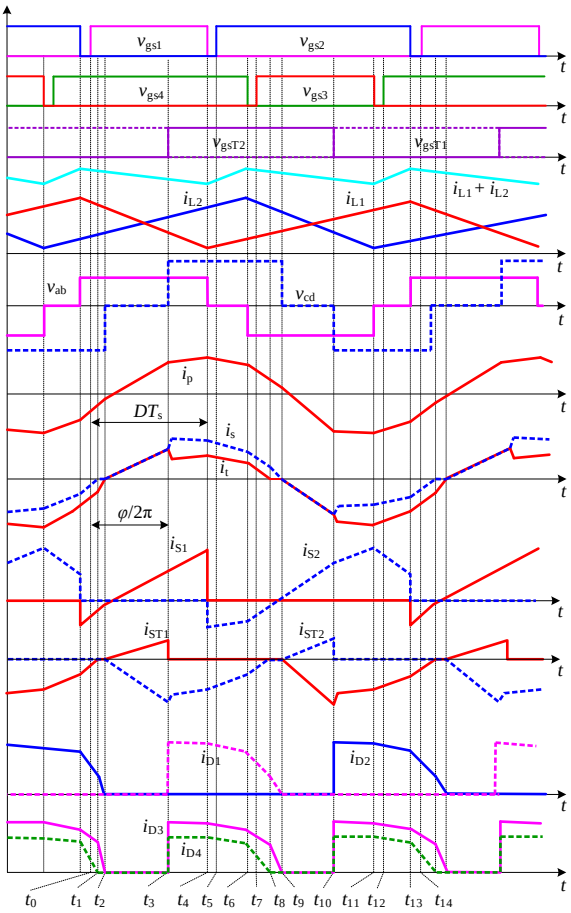


Fig. 8. Steady-state waveforms of the proposed FB-IB3 + SAR-BO converter in the CCM.

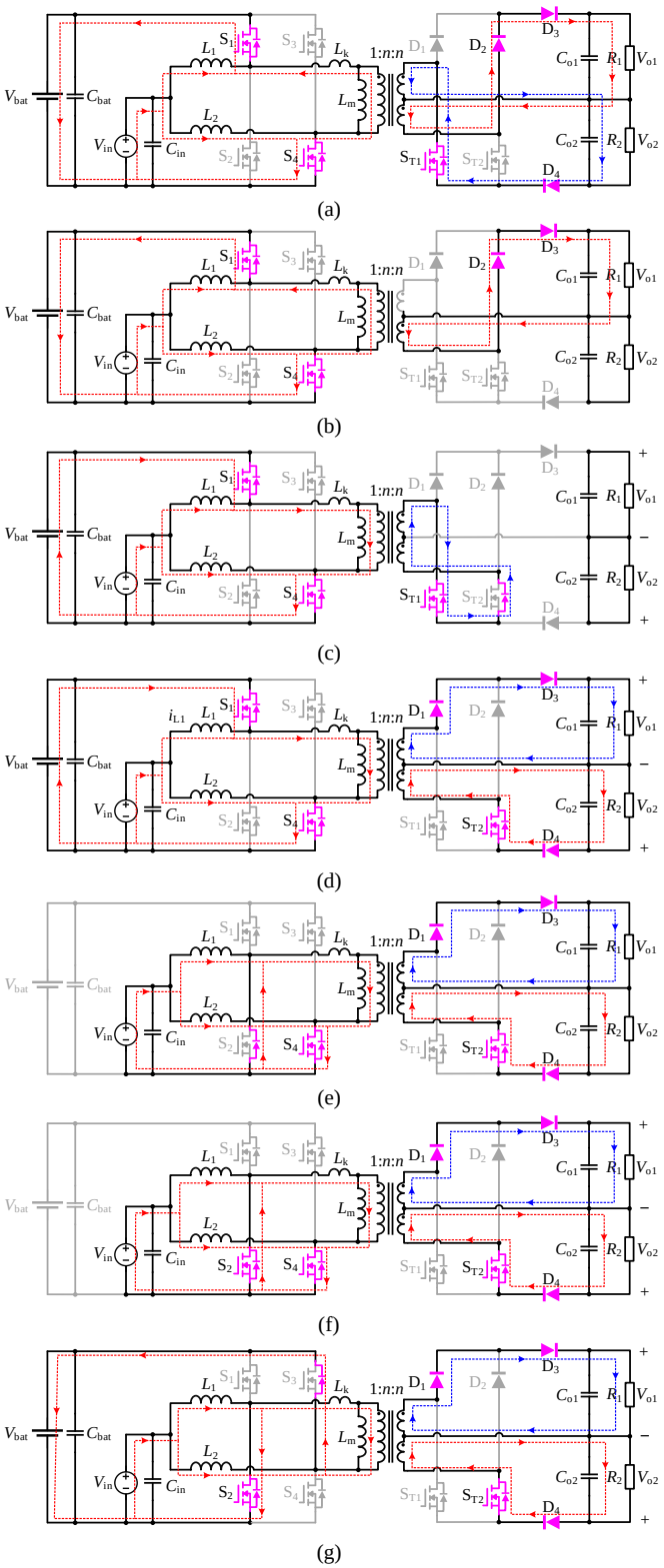


Fig. 9. Equivalent circuits of each stage for the proposed converter. (a) stage I [$t_0 \sim t_1$], (b) stage II [$t_1 \sim t_2$], (c) stage III [$t_2 \sim t_3$], (d) stage IV [$t_3 \sim t_4$], (e) stage V [$t_4 \sim t_5$], (f) stage VI [$t_5 \sim t_6$], and (g) stage VII [$t_6 \sim t_7$].

Stage VII [$t_6 \sim t_7$] [see Fig. 9(g)]: At t_6, S_4 is turned off. This stage is the dead time for S_3 and S_4. The secondary side windings N_s and N_t transfer power to PPO and NPO ports

through D_1 and D_3, D_4 and S_{T2}, respectively. The primary side winding voltage v_{ab} and secondary side winding voltage v_{cd} are $-V_{bat}$ and $V_{o1} + V_{o2}$, respectively. The primary side winding current i_p freewheels through S_1 and the body diode S_3. In this stage, the primary side winding current i_p is given as

$$i_p(t) = i_p(t_6) + \left[-V_{bat} - V_{o1}/n\right](t - t_6)/L_k \quad (7)$$

The proposed FB-IB3+SAR-BO converter may also operate in the DCM when the load power is relatively light. There are also seven operational stages in a half-switching period during the DCM. Using a similar analysis of the CCM operation, the operating principle of the converter in the DCM can also be obtained, which is not given in this paper.

IV. Performance Analysis

A. Output Characteristics

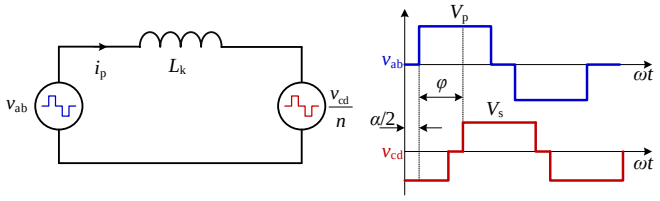
The primary side circuit is essentially an interleaved bidirectional buck/boost converter. According to the operational analysis in the previous section, and ignoring the influence of dead time, the relationship between V_{in} and V_{bat} can be calculated as

$$V_{bat} = V_{in}/D \quad (8)$$

In addition, the following variables are defined to simplify the theoretical analysis.

$$G = (V_{o1} - V_{o2})/nV_{bat}\ ,\ D_p = \varphi/\pi \quad (9)$$

The equivalent circuit of the proposed FB-IB3+SAR-BO converter can be simplified as shown in Fig. 10(a). Typical waveforms of v_{ab} and v_{cd} are demonstrated in Fig. 10(b).



(a) (b)

Fig. 10. (a) Equivalent circuit and (b) typical waveforms, where $V_p = V_{bat}$, and $V_s = V_{o1} - V_{o2}$.

According to the Fourier analysis, v_{ab} and v_{cd} can be expressed as

$$\begin{aligned} v_{ab} &= \sum_{i=1,3,5...} \frac{4V_{bat}}{i\pi}\cos\left(i\frac{\alpha}{2}\right)\sin(2\pi f_s i t) \\ v_{cd} &= \sum_{i=1,3,5...} \frac{4nGV_{bat}}{i\pi}\sin\left[i(2\pi f_s t - \varphi)\right] \end{aligned} \quad (10)$$

Then, ignoring the loss of the converter, the output power can be deduced as

$$P_o = \sum_{i=1,3,5...} \frac{4nGV_{bat}^2}{\pi^3 i^3 f_s L_k}\cos\left[\pi i(0.5 - D)\right]\sin(i\varphi) \quad (11)$$

From (11), the whole output power is equal to the superposition of all the odd harmonic power components. Due to the large amplitude of the fundamental component, only the fundamental component is considered to simplify the analysis. Thus, the relationship between the normalized output power and the phase shift angle φ can be obtained as shown in Fig. 11. It can be seen in Fig. 11 that the output power curve is symmetrical to $\varphi = 0.5\pi$. Therefore, the phase shift angle is limited to between 0 and 0.5π in practical applications.

B. Current Stress

According to the symmetry of the circuit, the primary side winding current $i_p(t_0) = i_p(t_7)$ can be satisfied. Therefore, the primary side winding current i_p can be expressed as.

$$t_2 - t_0 = \frac{(0.5G - 2D + D_p G)T_s}{G} \quad (12)$$

$$i_p(t_0) = -\frac{V_{bat}(1 + 0.5G)(0.5G - 2D + D_p G)T_s}{GL_k} \quad (13)$$

$$i_p(t_3) = \frac{V_{bat}(2D - 0.5G)T_s}{GL_k} \quad (14)$$

$$i_p(t_4) = \frac{\left[(2D - 0.5G) + G(1 - 0.5G)(D - D_p)\right]V_{bat}T_s}{GL_k} \quad (15)$$

$$i_p(t_6) = \frac{\left[2D + G^2(D_p - 0.5D - 0.25) + G(D - D_p - 0.5)\right]V_{bat}T_s}{GL_k} \quad (16)$$

Accordingly, the winding current of the converter can be evaluated and the device can be designed based on the current stress with a certain margin.

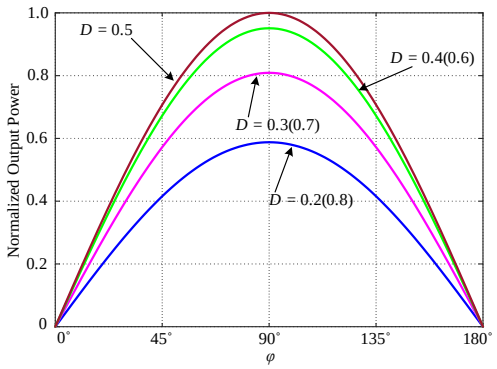


Fig. 11. Normalized output power versus the phase shift angle under different duty cycles.

C. Soft Switching

1) Secondary Side Switches and Diodes: According to the operation principal analysis, the body diodes of the secondary side switches S_{T1} and S_{T2} can conduct before the corresponding gate signals are applied. That indicates the drain-source voltages of S_{T1} and S_{T2} have decreased to zero before applying the gate signals. As a result, the ZVS of the secondary side switches S_{T1} and S_{T2} can be realized naturally without any extra criterion. Meanwhile, the current falling slopes of the secondary side diodes $D_1 \sim D_4$ are limited by the leakage inductance L_k of the high-frequency transformer, and thus, the diode currents $i_{D1} \sim i_{D4}$ can be decreased slowly to zero. Accordingly, the ZCS operation of diodes $D_1 \sim D_4$ can be achieved in the entire operating range, which can

effectively mitigate the reverse recovery issues of the diodes and improve the efficiency of the system.

2) Primary Side Switches: Due to the symmetry between the two switch legs of the primary side circuit, the ZVS condition of S_1 is the same as S_3, while the ZVS condition of S_2 is the same as that of S_4. Therefore, only the ZVS conditions of the switches S_1 and S_2 are analyzed here. According to the operation principle of the proposed converter, the ZVS condition of the primary side switches can be expressed as

$$\begin{cases} S_1: \quad i_{L1}(t_0) - i_p(t_0) > I_{min} \\ S_2: \quad i_{L1}(t_5) - i_p(t_5) < -I_{min} \end{cases} \tag{17}$$

where I_{min} is the minimum current which ensures that S_1 and S_2 can realize the ZVS. Therefore, I_{min} must be large enough to ensure that the voltage of the drain-source capacitance can drop to zero within the dead time. Thus, the following condition should be satisfied:

$$I_{min} \geq 2C_{oss}V_{bat}/t_{dead} \tag{18}$$

where C_{oss} is the drain-source capacitance of switches, and each switch is assumed to have the same drain-source capacitance. For the interleaved bidirectional buck/boost converter of the primary side circuit, $i_{L1}(t_{S1})$ and $i_{L1}(t_{S2})$ are the peak and valley values of the inductor current i_{L1} in a switching cycle, which can be expressed as

$$\begin{cases} i_{L1}(t_{S1}) = (P_o - P_{bat})/2V_{in} + V_{in}(1-D)T_s/2L \\ i_{L1}(t_{S2}) = (P_o - P_{bat})/2V_{in} - V_{in}(1-D)T_s/2L \end{cases} \tag{19}$$

By substituting (17) and (19) into (18), the ZVS conditions of the primary side switches can be obtained as

$$\begin{cases} S_1: \quad P_o + \dfrac{V_{bat}^2 D^2 (1-D)}{Lf_s} - 2DV_{bat}i_p(t_0) - \dfrac{4DC_{oss}V_{bat}^2}{t_{dead}} > P_{bat} \\ S_2: \quad P_o - \dfrac{V_{bat}^2 D^2 (1-D)}{Lf_s} - 2DV_{bat}i_p(t_0) - \dfrac{4DC_{oss}V_{bat}^2}{t_{dead}} < P_{bat} \end{cases} \tag{20}$$

According to (20) and using the parameters given in Section V, the theoretical ZVS range of the primary side switches can be calculated, as presented in Fig. 12. The ZVS boundary of the upper switches (S_1 and S_3) and the lower switches (S_2 and S_4) are shown in the blue curves of Fig. 12 respectively, where the ZVS of the primary side switches can be realized in the region between the two curves. Moreover, considering the unidirectional power flow characteristics of the RES port, $P_{in} > 0$ and $P_o > -P_{bat}$ must be satisfied in the proposed converter. The boundary of ZVS for the upper switches (S_1 and S_3) is higher than the power line ($P_o = -P_{bat}$), which means the ZVS of the upper switches can be achieved regardless of the input/output power. For the lower switches (S_2 and S_4), ZVS can be achieved in a wide range depending on the input/output power. As a result, the ZVS of the primary side switches can be implemented in the shaded region shown in Fig. 12. Moreover, the greater the output power P_o, the easier it is for the proposed converter to achieve soft switching.

D. Input Current Ripple

As aforementioned, the primary side switch legs of the converter are driven in an interleaved manner, which will greatly reduce the input current ripple of the RES port. To analyze the influence of the phase shift angle θ of two switching legs of the primary side on the input current ripple ΔI_{in}, it is assumed that $L_1 = L_2 = L$. The inductance current ripple ΔI_L can be expressed as

$$\Delta I_L = \frac{V_{in}(1-D)}{Lf_s} \tag{21}$$

Then, ΔI_{in}, which is normalized with ΔI_L, can be given by the following:

$$\Delta I_{in} = \begin{cases} 2(D - \theta/2\pi)/D, & D \geq 0.5 \\ 2(1 - D - \theta/2\pi)/(1-D), & D < 0.5 \end{cases} \tag{22}$$

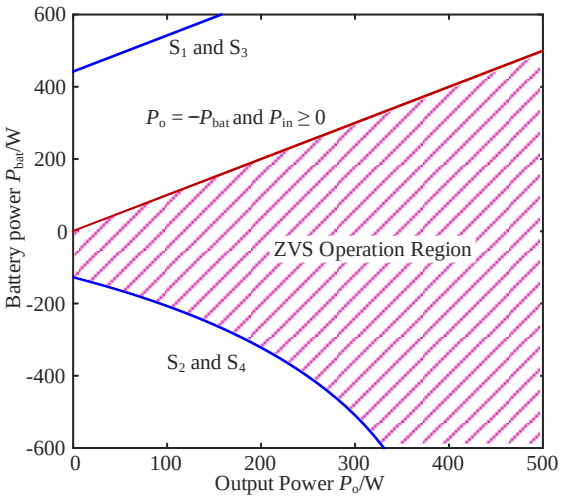


Fig. 12. Theoretical ZVS range of the primary side switches.

Accordingly, the theoretical result of ΔI_{in} with different D and θ can be represented in Fig. 13. As it can be seen from Fig. 13, the minimum input current ripple is achieved when $\theta = 180^o$. As a result, the current ripple of the RES is greatly reduced in the proposed converter, which is very helpful to improve the maximum energy harvesting of the RES and reduce the volume of inductors L_1 and L_2.

E. Control Strategy

The conventional control method for the MPC proposed in [23], namely PWM plus secondary side PSM method, is used in the proposed FB-IB3 + SAR-BO converter. The control block diagram is shown in Fig. 14. As seen in Fig. 14, four regulators are included in the energy management and control system, which include an input voltage regulator (IVR) for the maximum power point tracking (MPPT) control, a battery voltage regulator (BVR), and a battery current regulator (BCR) for battery management, and an output voltage regulator (OVR) for the output voltage control. v_{IVR}, v_{BVR}, v_{BCR}, and v_{OVR} are the outputs of the IVR, BVR, BCR, and OVR, respectively, and I_{B_max}, V_{B_max}, and V_{o_ref} are references of battery current, the battery voltage, and output voltage, respectively. The output v_{OVR} of the OVR is used to regulate

the phase shift angle φ of the secondary side switches, thereby controlling the bipolar output voltage to meet the load demand. The minimum value of v_{IVR}, v_{BVR}, and v_{BCR} is selected to generate the duty cycle D of the primary side switch S_1, in order to realize the power optimization control of RESs and ESSs. As a result, the control loops of the primary side and secondary side are independent and approximately decoupled, which is helpful to the design of the controller.

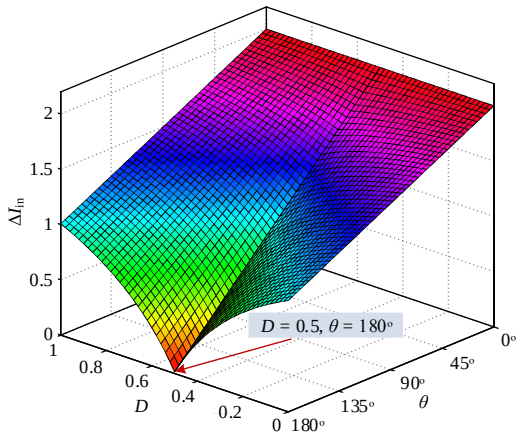


Fig. 13. Relationship among the normalized input current ripple ΔI_{in}, duty cycle D, and phase shift angle θ.

It is worth mentioning that the above control method can also be used to control other isolated four-port converters of the proposed category, where the control of the secondary side rectifier is the same as the above method, and the primary side control can be modified slightly according to topologies. For example, for the topology shown in Fig. 6(a), the primary side can be controlled by a PFM to optimize the power of the RES and ESS ports. For the topology shown in Fig. 6(b), the primary side can be controlled by the PWM plus PSM method, where S_1 and S_3 are controlled by the same PWM driving signal to optimize the power of the RES and ESS ports, and S_2 and S_{T2} are controlled by the same driving signal to achieve constant bipolar output voltage control.

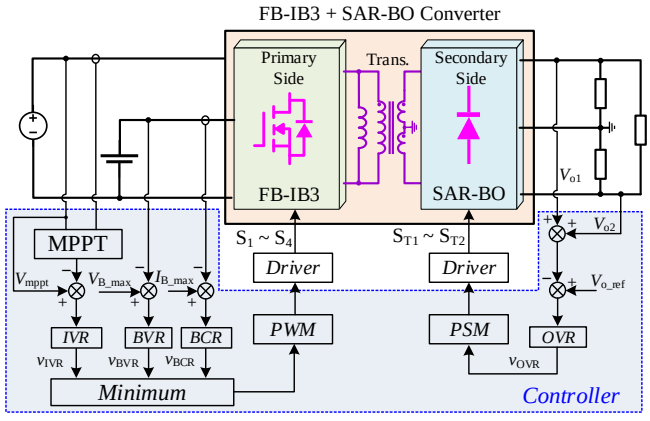


Fig. 14. Control block diagram of the proposed FB-IB3 + SAR-BO converter.

V. Experimental Results

A 500-W experimental prototype is built based on the specifications and parameters in Table III to verify the proposed FB-IB3 + SAR-BO converter and the theoretical analysis. A *Chroma* 62150H PV Simulator is connected to the RES port, and a 96 V lead-acid battery is employed in the prototype as the energy storage element.

TABLE III Parameters Used in the Experimental Prototype

Parameter	Value	Parameter	Value
Output voltage V_o	±60 V	Turn ratio n	0.9
PV voltage V_1	40 V	Magnetic inductor L_m	120 μH
PV current I_1	0 ~ 10 A	Leakage inductor L_k	7 μH
Inductor L_1 and L_2	85 μH	Battery voltage	96 V
Capacitors C_{bat} and C_{in}	220 μF/100 V	Switching frequency	100 kHz
Capacitors C_{o1} and C_{o2}	330 μF/150 V	Diodes D_1 ~ D_4	STPS40120CT
MOSFET	IPP075N15N3G	Controller	TMS320F280049

A. Steady-State and Soft Switching Performances

Fig. 15 shows steady-state waveforms of the proposed FB-IB3 + SAR-BO converter under the CCM. As shown in Fig. 15(a), the total RES port current ripple $i_{L1} + i_{L2}$ is significantly reduced by using the interleaved control with 180° phase shift. The primary side and the secondary side windings voltages v_{ab} and v_{cd}, currents i_p and i_s are shown in Fig. 15(b). It can be seen from Fig. 15 that the experimental waveform is consistent with the theoretical analysis.

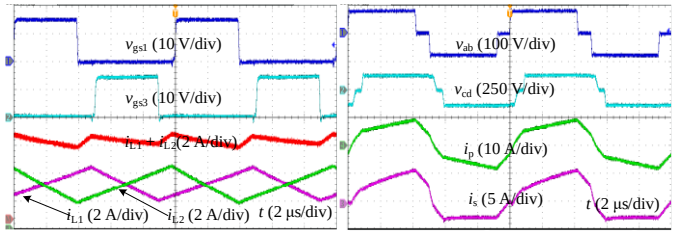


Fig. 15. Steady-state performance of the proposed converter: (a) the driving signals v_{gs1} and v_{gs3} of S_1 and S_3, inductor currents i_{L1}, i_{L2}, and $i_{L1} + i_{L2}$, and (b) windings voltages v_{ab} and v_{cd}, winding currents i_{Lk} and i_s.

The soft switching performance of switches and diodes was tested and the results are shown in Fig. 16. As observed in Figs. 16(a) and (b), ZVS is accomplished for the primary side switches S_1 and S_2. The soft switching waveforms of the secondary side switches S_{T1} and S_{T2} are shown in Figs. 16(c) and (d), which are easier to implement ZVS than primary side switches S_1 ~ S_4. As shown in Figs. 16(e) and (f), the ZCS is achieved for the secondary side diodes D_1 ~ D_4, which helps to eliminate the reverse recovery issue and improve the efficiency.

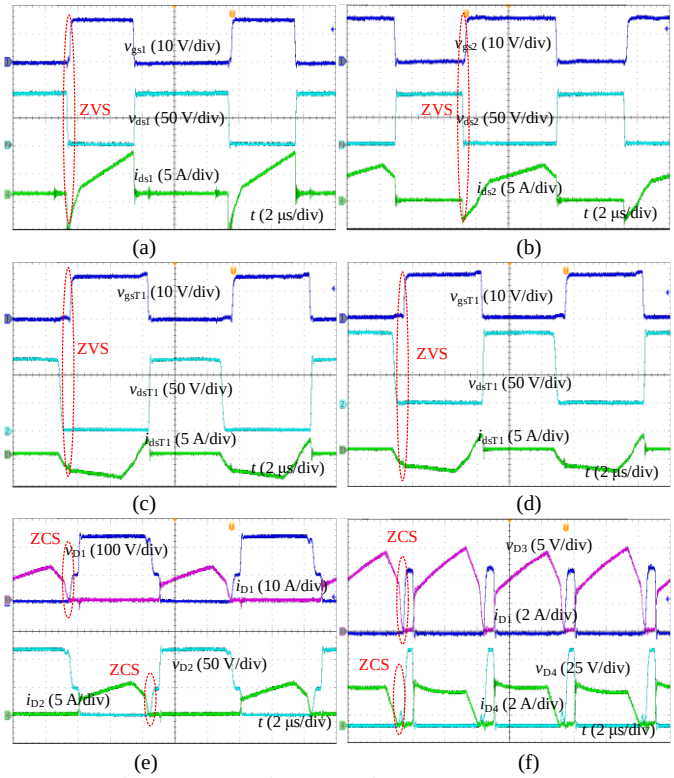


Fig. 16. Soft switching performance of the proposed converter. (a) the primary side switch S_1, (b) the primary side switch S_2, (c) the secondary side switch S_{T1}, (d) the secondary side switch S_{T2}, (e) the diodes D_1 and D_2, and (f) the diodes D_3 and D_4.

B. Dynamic and Mode Transition Performance

The dynamic performance of the proposed converter by stepping the output load and input PV power is shown in Fig. 17. In Figs. 17(a) and (b), the input PV power is kept constant at 300 W. When the total output load power is stepping between 200 W and 400 W, the battery regulates the charging and discharging state to maintain the bipolar output voltage constant. In Fig. 17(c) and (d), the output power is constant 200W, when the input PV power changes between 100W and 300W. The above experimental results show that the output voltages of PPO and NPO ports are symmetrical. Moreover, the positive/negative output voltages are kept at ±60 V constantly during load steps or input variations.

Fig. 18 shows the transient experimental results of the proposed converter under severely unbalanced loads, where the positive polarity load power steps down from 150 W to 0 W suddenly and the negative polarity load power keeps constant at 150 W. It can be seen from the experimental results that the proposed converter can operate under the severely unbalanced load condition of output ports, and the positive/negative output voltages are strictly symmetric and kept at ±60 V.

When the PV input power is suddenly reduced to zero from 200 W, the total output power is maintained at 400 W, it can be seen that the proposed converter can realize mode transition between BRM and BISM, and the experimental results are shown in Fig. 19. It can be seen in Fig. 19 that the converter can achieve seamless mode switching between BRM and BISM when the available PV power drops to zero suddenly (e.g., due to fast passing clouds), while the symmetrical bipolar output voltage can be controlled as a constant at ±60 V.

Fig. 20 shows the experimental waveforms when the positive polarity dc bus fails, where the available PV input power is constant at 250 W, and the power of the load R_2 steps between 300 W and 200 W. It can be seen that the negative bus can still operate normally and maintain -60 V under the condition of positive bus failure. Experimental results show that the bipolar dc bus structure has higher reliability than the unipolar dc bus structure.

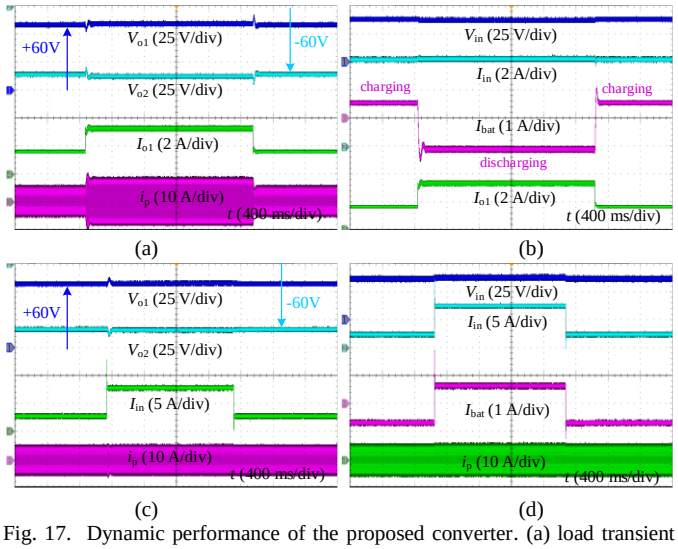


Fig. 17. Dynamic performance of the proposed converter. (a) load transient waveforms: V_{o1}, V_{o2}, I_{o1}, i_p, (b) load transient waveforms: V_{in}, I_{in}, I_{bat}, I_{o1}, (c) input transient waveforms: V_{o1}, V_{o2}, I_{in}, i_p, and (d) input transient waveforms: V_{in}, I_{in}, I_{bat}, i_p.

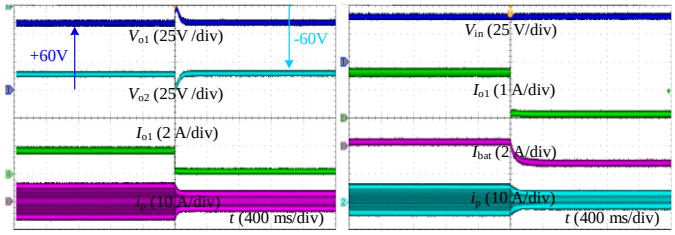


Fig. 18. Experimental waveforms under severely unbalanced loads. (a) V_{o1}, V_{o2}, I_{o1}, i_p, and (b) V_{in}, I_{o1}, I_{bat}, i_p.

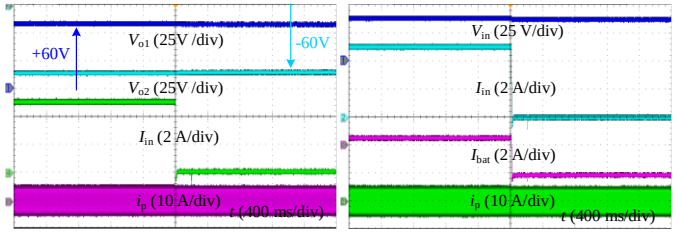
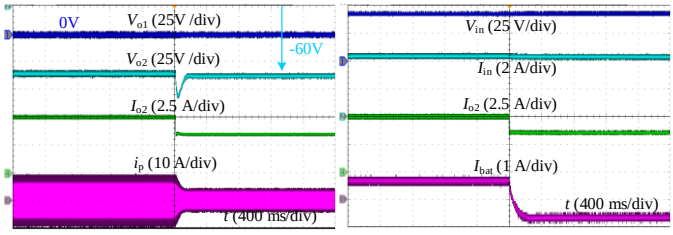


Fig. 19. Mode transition performance of the converter. (a) V_{o1}, V_{o2}, I_{in}, i_p, and (b) V_{in}, I_{in}, I_{bat}, i_p.



(a) (b)

Fig. 20. Experimental waveforms under the condition of positive bus failure. (a) V_{o1}, V_{o2}, I_{o2}, i_p, and (b) V_{in}, I_{in}, I_{o2}, I_{bat}.

C. Efficiency

The conversion efficiency of the proposed FB-IB3 + SAR-BO converter is evaluated in three different power transfer paths (e.g., from the RES port to ESS port, from the ESS port to output ports, and from the RES port to output ports). The measured efficiency curves are shown in Fig. 21. As it can be observed in Fig. 21, the proposed converter has high efficiency in the full load range, and the higher efficiency can be obtained in the power conversion from the RES port to the ESS port because the power path does not include the secondary circuit.

D. Comparison

Table IV provides a comparison of the proposed converter and other similar solutions. Since most existing solutions consist of only one input port and one bipolar output port, the power conversion path from the ESS to the bipolar output is compared with existing solutions to obtain a fairer performance comparison. The number of components, symmetry of bipolar voltages, voltage stress, soft switching, control method, rating power, and efficiency are listed in Table IV. It is observed from the Table IV that the proposed symmetric bipolar output converter offers the following key features:

1) In terms of the number of components, the proposed converter has fewer semiconductor devices and a lower cost than the solutions in [32] and [33]. Furthermore, the proposed converter has fewer magnetic elements than the converter in [30] and [31].

2) Compared with the solutions in [32] and [33], the proposed converter has an inherent symmetrical bipolar output voltage, which is independent of the control method. Therefore, additional voltage balancing controls are not needed and the complexity of the design is simplified.

3) Soft-switching performance, including ZVS for all switches and ZCS for all diodes, can be achieved, thus ensuring that the proposed converter has higher efficiency than other converters.

4) In addition, the proposed converter also has higher voltage stress of switches than the topologies in [32] and [33], so that it is more suitable for applications with low output voltage levels.

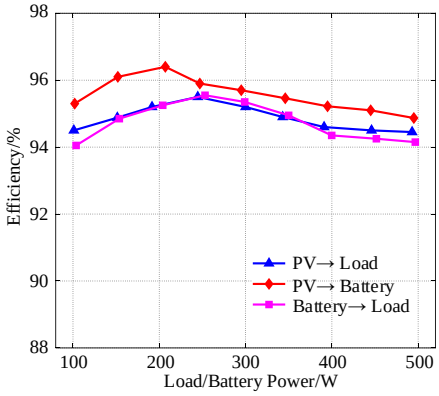


Fig. 21. Measured efficiency versus output power in different power flow paths.

TABLE IV. THE COMPARISON OF THE PROPOSED CONVERTER AND OTHER SIMILAR SOLUTIONS

Solutions		[30]	[31]	[32]	[33]	Proposed
Number of components	MOSFET	8	8	12	12	6
	Diode	0	0	6	4	4
	Magnetic components	Transformer + 2 inductors	Transformer + 2 inductors	Transformer	Transformer	Center tapped transformer
Symmetry of bipolar voltages		Inherently symmetric bipolar output	Inherently symmetric bipolar output	Depends on the balancing control	Depends on the balancing control	Inherently symmetric bipolar output
Voltage stress of switches		$2V_{o1}$	$2V_{o1}$	V_{o1}	V_{o1}	$2V_{o1}$
Control method		Voltage balance control	PSM	Voltage balance control	Dual loop voltage balance control	PSM
Soft switching		ZVS	ZVS	N/A	N/A	ZVS + ZCS
Rating power		500W	3000W	1500W	3000W	500W
Peak Efficiency		N/A	96.7%	95.3%	94.7	95.6%

VI. CONCLUSION

In this paper, a family of symmetrical bipolar output isolated four-port converters based on center-tapped winding are developed to integrate RES and ESS to bipolar dc bus. Various active rectifiers with symmetrical bipolar outputs, including the SAR-BO rectifiers and ACR-BO rectifiers, have

been developed as secondary side circuits of the converter family to achieve symmetrical and controllable bipolar output voltages. Meanwhile, various primary side circuits that can integrate RES and ESS are presented to realize the power optimization control of RES and ESS. Therefore, an approximately decoupled control loop is realized in the proposed symmetrical bipolar output isolated four-port converters. Single-stage power conversion is realized to improve the conversion efficiency of the power system. The proposed FB-IB3 + SAR-BO converter is analyzed in detail as an example, including operating principle, steady-state characteristics, soft switching, port current ripple, and control method. Experimental results of a 500W prototype have verified the feasibility and effectiveness of the proposed topologies and the advantages of the derived isolated four-port converters with symmetric bipolar output topologies.

REFERENCES

[1] Ellabban, H. Abu-Rub, and F. Blaabjerg, "Renewable energy resources: current status, future prospects and their enabling technology," *Renewable Sustain. Energy Rev*., vol. 39, pp. 748-764, Nov. 2014.

[2] J. Wu, X. Xing, X. Liu, J. M. Guerrero, and Z. Chen, "Energy management strategy for grid-tied microgrids considering the energy storage efficiency," *IEEE Trans. Ind. Electron*., vol. 65, no. 12, pp. 9539-9549, Dec. 2018.

[3] M. T. Lawder, B. Suthar, P. W. Northrop, S. De, C. M. Hoff, O. Leitermann, M. L. Crow, S. Santhanagopalan, and V. R. Subramanian, "Battery energy storage system (BESS) and battery management system (BMS) for grid-scale applications," *Proceedings of the IEEE*, vol. 102, no. 6, pp. 1014-1030, Jun. 2014.

[4] G. Zhou, Q. Tian, M. Leng, X. Fan, and Q. Bi, "Energy management and control strategy for DC microgrid based on DMPPT technique," in *IET Power Electron.*, vol. 13, no. 4, pp. 658-668, 18 3 2020.

[5] N. Femia, M. Fortunato, and M. Vitelli, "Light-to-light: PV-fed led lighting systems," *IEEE Trans. Power Electron*., vol. 28, no. 8, pp. 4063-4073, Aug. 2013.

[6] T. Dragičević, X. Lu, J. C. Vasquez, and J. M. Guerrero, "DC microgrids-Part II: A review of power architectures, applications, and standardization issues," *IEEE Trans. Power Electron*., vol. 31, no. 5, pp. 3528-3549, May 2016.

[7] K. Hiroaki, M. Yushi, and I. Toshifumi, "Low-voltage bipolar type dc microgrid for super high quality distribution," *IEEE Trans. Power Electron*., vol. 25, no. 12, pp. 3066-3075, Dec. 2010.

[8] F. Gao and D. Rogers, "Duty-cycle plus phase-shift control for a dual active half bridge based bipolar DC microgrid," in *Proc. IEEE App. Power Electron. Conf.*, San Antonio, TX, USA, 2018, pp. 1479-1485.

[9] Z. Zhang D. Shi, C. Jin, L. H. Koh, F. H. Choo, P. Wang, and Y. Tang, "Droop control of a bipolar dc microgrid for load sharing and voltage balancing," in *Proc. IEEE 3rd Int. Future Energy Electron. Conf*., Kaohsiung, Taiwan, 2017, pp. 795-799.

[10] M. B. Ferrera, S. P. Litrán, E. D. Aranda, and J. M. A. Márquez, "A converter for bipolar dc link based on SEPIC-Cuk combination," *IEEE Trans. Power Electron*., vol. 30, no. 12, pp. 6483-6487, Dec. 2015.

[11] P. N. Vovos, A. E. Kiprakis, A. R. Wallace, and G. P. Harrison, "Centralized and distributed voltage control: impact on distributed generation penetration," *IEEE Trans. Power Syst.*, vol. 22, no. 1, pp. 476-483, Feb. 2007.

[12] G. Chen, F. L. Lewis, E. N. Feng, and Y. Song, "Distributed optimal active power control of multiple generation systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7079-7090, Nov. 2015.

[13] T. Jalilzadeh, N. Rostami, E. Babaei, and S. H. Hosseini, "Multiport DC–DC Converter with step-up capability and reduced voltage stress on switches/diodes," *IEEE Trans. Power Electron*., vol. 35, no. 11, pp. 11902-11915, Nov. 2020.

[14] J. Zhang W. Jiang, T. Jiang, S. Shao, Y. Sun, B. Hu, and J. Zhang, "A three-port LLC resonant dc/dc converter," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 7, no. 4, pp. 2513-2524, Dec. 2019.

[15] Q. Tian, G. Zhou, R. Liu, X. Zhang, and M. Leng, "Topology synthesis of a family of integrated three-port converters for renewable energy system applications," *IEEE Trans. Ind. Electron*., vol. 68, no. 7, pp. 5833- 5846, Jul. 2021.

[16] G. Chen, Y. Liu, X. Qing, and F. Wang, "Synthesis of integrated multiport dc-dc converters with reduced switches," *IEEE Trans. Ind. Electron*., vol. 67, no. 6, pp. 4536-4546, Jun. 2020.

[17] M. Uno and K. Sugiyama, "Switched capacitor converter based multiport converter integrating bidirectional PWM and series-resonant converters for standalone photovoltaic systems," *IEEE Trans. Power Electron*., vol. 34, no. 2, pp. 1394-1406, Feb. 2019.

[18] J. Deng, H. Wang, and M. Shang, "A ZVS three-port dc/dc converter for high-voltage bus-based photovoltaic systems," *IEEE Trans. Power Electron*., vol. 34, no. 11, pp. 10688-10699, Nov. 2019.

[19] H. Wu, R. Chen, J. Zhang, Y. Xing, H. Hu, and H. Ge, "A family of three-port half-bridge converters for a stand-alone renewable power system," *IEEE Trans. Power Electron.*, vol. 26, no. 9, pp. 2697-2706, Sept. 2011.

[20] H. Moradisizkoohi, N. Elsayad, and O. A. Mohammed, "A family of three-port three-level converter based on asymmetrical bidirectional half-bridge topology for fuel cell electric vehicle applications," *IEEE Trans. Power Electron*., vol. 34, no. 12, pp. 11706-11724, Dec. 2019.

[21] B. Farhangi and A. T. Hamid, "Modeling and analyzing multiport isolation transformer capacitive components for onboard vehicular power conditioners," *IEEE Trans. Ind. Electron*., vol. 62, no. 5, pp. 3134-3142, May 2015.

[22] J. Zhang, H. Wu, X. Qin, and Y. Xing, "PWM plus secondary-side phase-shift controlled soft-Switching full-bridge three-port converter for renewable power systems," *IEEE Trans. Ind. Electron.*, vol. 62, no. 11, pp. 7061-7072, Nov. 2015.

[23] H. Wu, J. Zhang, X. Qin, T. Mu, and Y. Xing, "Secondary-side-regulated soft-switching full-bridge three-port converter based on bridgeless boost rectifier and bidirectional converter for multiple energy interface," *IEEE Trans. Power Electron.*, vol. 31, no. 7, pp. 4847-4860, Jul. 2016.

[24] H. Zhu, D. Zhang, H. S. Athab, B. Wu, and Y. Gu, "PV isolated three-port converter and energy-balancing control method for PV-battery power supply applications," *IEEE Trans. Ind. Electron*., vol. 62, no. 6, pp. 3595-3606, Jun. 2015.

[25] S. Rivera, B. Wu, S. Kouro, V. Yaramasu, and J. Wang, "Electric vehicle charging station using a neutral point clamped converter with bipolar dc bus," *IEEE Trans. Ind. Electron*., vol. 62, no. 4, pp. 1999-2009, Apr. 2015.

[26] F. Wang, Z. Lei, X. Xu, and X. Shu, "Topology deduction and analysis of voltage balancers for dc microgrid," *IEEE J. Emerg. Sel. Topics Power Electron*., vol. 5, no. 2, pp. 672-680, Jun. 2017.

[27] P. Prabhakaran and V. Agarwal, "Mitigation of voltage unbalance in a low voltage bipolar DC microgrid using a boost-SEPIC type interleaved dc-dc compensator," in *Proc. IEEE 2nd Annu. Southern Power Electron. Conf*., Auckland, New Zealand, 2016, pp. 1-6.

[28] P. Prabhakaran and V. Agarwal, "Novel boost-SEPIC type interleaved dc-dc converter for mitigation of voltage imbalance in a low-voltage bipolar dc microgrid," *IEEE Trans. Ind. Electron*., vol. 67, no. 8, pp. 6494-6504, Aug. 2020.

[29] Q. Tian, G. Zhou, M. Leng, G. Xu and X. Fan, "A nonisolated symmetric bipolar output four-port converter interfacing PV-battery system," *IEEE Trans. Power Electron*., vol. 35, no. 11, pp. 11731-11744, Nov. 2020.

[30] B. Li, Q. Fu, S. Mao, X. Zhao, D. Xu, "DC/DC converter for bipolar LVDC system with integrated voltage balance capability," *IEEE Trans. Power Electron.*, vol. 36, no. 5, pp. 5415-5424, May 2021.

[31] J. -Y. Lee, H. -S. Kim and J. -H. Jung, "Enhanced dual-active-bridge dc-dc converter for balancing bipolar voltage level of dc distribution system," *IEEE Trans. Ind. Electron*., vol. 67, no. 12, pp. 10399-10409, Dec. 2020.

[32] J. Lee, Y. Cho and J. Jung, "Single-stage voltage balancer with high-frequency isolation for bipolar LVDC distribution system," *IEEE Trans. Ind. Electron.*, vol. 67, no. 5, pp. 3596-3606, May 2020.

[33] P. Kolahian, H. Tarzamni, A. Nikafrooz, M. Hamzeh, “Multi-port dc-dc converter for bipolar medium voltage dc micro-grid applications,” *IET Power Electron*., vol. 12, no. 7, pp. 1841-1849, Jul. 2019.