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A Novel Dual-Mode Switched-Capacitor Five-Level Inverter With Common-Ground Transformerless Concept

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Abstract— **Transformerless (TL) grid-connected photovoltaic (PV) inverters with a common-ground (CG) circuit architecture exhibit some excellent features in removing the leakage current concern and improving the overall efficiency. However, the ability to cope with a wide range of input voltage changes while maintaining the output voltage in a single power conversion stage is a key technological challenge. Considering this, the work at hand proposes a novel dual-mode switched-capacitor five-level (DMSC5L)-TL inverter with a CG feature connected to the grid. The proposed topology is comprised of a single dc source and power diode, three capacitors, four unidirectional and three bi-directional power switches. Based on the series-parallel switching conversion of the involved switches, the proposed DMSC5L-TL inverter can generate five distinctive output voltage levels during both the boost and buck operation modes with a self-voltage balancing operation for the involved capacitors. A simple dead-beat continuous current controller (DB3C) modulation technique is also used to handle both the active and reactive power exchange while ensuring a fixed switching frequency operation. The proposed circuit description with its DB3C details, the design guidelines with a comparative study, and some experimental results are also given to show the feasibility of the proposed solution for the practical applications.**

***Index Terms*—Common grounded transformerless inverters, Grid-connected applications, Switched-capacitor cells, and Model predictive control.**

I. INTRODUCTION

GRID-CONNECTED photovoltaic (PV) string inverters with a transformerless (TL) configuration have gained a lot of attraction in both the commercial utilization and industrial applications. Such TL inverter topologies serve higher efficiency with a reasonable percentage of the power density per cost. However, to properly address the safety standards and grid code requirements in the presence of the PV string panels, a plenty of circuit/control improvements have been put forward in the recent decade [1]-[2].

Mitigating or nullifying the leakage current concern and having a low voltage ride through capability during the voltage sag condition of the grid are counted as two strict IEEE 1547 grid code requirements, e.g., VDE 0126-1-1 [3] and VDE-AR-N-4105 [4], which have to be addressed by the new developed TL-inverters. Apart from this, the peak voltage of the grid in the presence of a low-voltage PV string panel has to be also fulfilled by the TL inverters within a single stage energy conversion platform. Following these observations, the power quality enhancement by increasing the number of output voltage levels has turned into another major task of TL-grid-tied inverters, which can facilitate integration of the output low-pass filters with a smaller size [1]-[4]. In this regard, some derived versions of the full-bridge (FB)-based TL inverters can mitigate the leakage current concern through decoupling the dc and ac side of the inverter in freewheeling modes. H5 [5], Highly Efficient and Reliable Inverter Concept (HERIC) [6], Optimized H5 (OH5) [7], dual-buck [8], and different families of the H6 [9]-[10] topologies are counted as the most recently used PV-TL inverters in this category. Step-down feature of the inverter output voltage alongside intensified value of the leakage current during the reactive power support mode are two main shortcomings of such grid-connected TL inverters. Moreover, all of such structures offer a three-level (3L) inverter output voltage only, which call for a bulky filter at their output for improving the injected grid current THD.

Contemporary, active neutral point clamped (ANPC)-TL inverters associated with the flying capacitor (FC) integrated cell can considerably reduce the leakage current value, while it is possible to generate higher number of output voltage levels with a reactive power flow path. As a practical grid-connected TL inverter, the conventional five-level (5L)-ANPC structures still suffer from step-down features at the output, where the peak voltage of the inverter is half of the PV main string input value [11]. The advanced version of such inverters is named as active boost neutral point clamped (ABNPC) inverter, which somehow address this drawback by integrating the FC cell with the redundant charging flow path [12]; however, the peak of output voltage is still equal to the PV string voltage value. Therefore, additional front-end boost-based converter with extra active and passive elements is needed in case of dealing with the low-voltage paralleled PV string panels.

Grid-connected TL inverters with the common-ground (CG) feature is another notable configuration as it can nullify the leakage current concern with a grounded potential between the negative terminal of the PV main string and the null of the grid [13]-[24]. Supposedly, many recently presented topologies of CG-based TL inverters have utilized the concept of virtual dc-link capacitor or the flying inductor [13]-[14]. Here, such a virtual dc-link capacitor is charged up to the required peak of

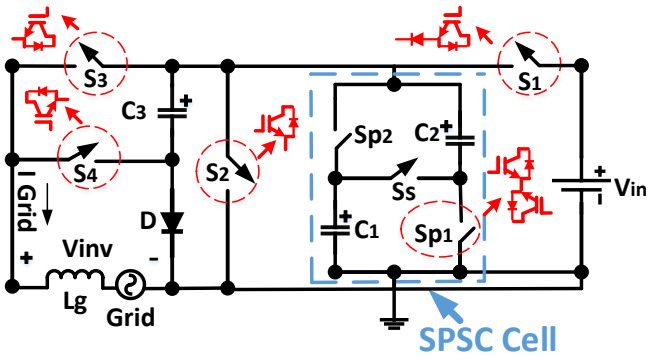


Fig. 1. The proposed DMSC5L-TL inverter topology.

inverter output voltage in one half cycle of the grid and then it is discharged in another half cycle. Consequently, the utilization of single PV source inverter structure with a CG feature would be feasible. Regarding this concept, the 2L [15]-[16], 3L [17]-[18], and 5L [19]-[20] CG-based TL inverters have recently been introduced, whereas they still possess a buck-type feature for the output voltage. Through the contribution of series-parallel switched-capacitor (SPSC) cell with such a mentioned virtual dc-link, some advanced versions of 3L-and 5L-CG-based TL-inverters have also been strived in [21]-[24], which can regulate a two-time voltage boosting feature for the inverter output voltage with a single energy conversion stage. It is obvious that such a boosting feature is necessary whenever a low-scaled PV string panels is available. Since the sun shine irradiation is variable during the day, so when the required voltage level of the PV-TL inverter to inject the power to the grid is fulfilled, the two times voltage boosting feature in these structures may cause some over voltage constraints for the involved active and passive elements.

Conversely, the concept of dual mode (DM)-TL inverters as the recent achievement of the grid-connected PV systems could emerge, which gives the capability of operating under a wide range of input voltage changes to the TL-inverters. Here, a few type of such inverters like the interleaved DM-based TL structure presented in [25] and a 5L-ANPC-based TL topology strived in [26] have been introduced till now. Although they could properly mitigate the leakage current value, the numbers of involved components and their control complexity are still high. Moreover, they lack in offering any CG feature.

The aim of this study is to present a novel topology for the grid-connected TL inverters, which possesses three important aforementioned highlights at the same time e.g. five-level output voltage generation alongside the CG feature with the DM concept. As a result, it can be seen as an efficient topology from the enhancement of the power quality, removing the leakage current concern, and flexible operation within a wide input voltage variation viewpoint. The proposed topology also uses the SPSC cell and is called dual mode switched-capacitor 5L (DMSC5L)-TL inverter. Here, a single dc-source/power diode, three dc-link capacitors, four unidirectional and three bidirectional power switches are required. Through the proposed DMSC5L structure, all five-output voltage levels in both modes of the operation (buck and boost) are generated whilst the voltage-balancing of the involved capacitors is self-controlled without any need of additional voltage sensors. Since the aim of the proposed topology is to inject the power to the grid, a simple but robust dead-beat continuous-current-controller (DB3C) technique is used to control the converter at the fixed switching frequency in both modes of operation. The rest of this paper is organized as follows: The circuit description of the proposed topology in both modes of operation is discussed in Section II. The overall procedure of the employed DB3C strategy to control the proposed TL-inverter in the grid-connected condition is explained in Section III. A design guideline associated with the current stress analysis and a comparative study are presented in Section IV, V, and VI, respectively. And finally, several experimental results are given in Section VII to demonstrate the correctness of the proposed DMSC5L-TL inverter.

II. Operating Principle of the Proposed DMSC5L-TL Inverter

The overall configuration of the proposed DMSC5L grid-connected TL inverter with different switches realization has been depicted in Fig. 1. As it is clear, the proposed topology offers a CG feature and contains a SPSC cell with two bi-directional paralleled power switches ($S_{P1}$and S_{P2}), a single series unidirectional power switch (S_S), and two dc-link capacitors (C_1 and C_2). Such an SPSC cell is essential for the DM operation of the proposed topology under the overall condition of the input dc-source (buck or boost mode). Apart from this cell, the proposed topology needs four other power switches, a single power diode and another dc-link capacitor. Here, three power switches named as S_2, S_3 and S_4 are unidirectional from both the current flowing direction and peak inverse voltage (PIV) viewpoints, while the type of power switch S_1 is the reverse-blocking (RB) one with a unidirectional operation in current flowing direction and bidirectional operation as the PIV aspect. Here also, the C_3 acts as a virtual dc-link like what is used in the other existing TL inverters with a CG concept [16]-[25]. Considering a constant input voltage as V_{dc} and regarding the switching conversion of the proposed topology which will be discussed in the following, the balanced voltage across the involved capacitors in each of the boost and buck modes can be summarized as follows:

$$\begin{cases} V_{C1} = V_{C2} = V_{dc} \\ V_{C3} = 2V_{dc} \end{cases} \rightarrow \text{Boost Mode} \quad (1)$$

$$\begin{cases} V_{C1} = V_{C2} = 0.5V_{dc} \\ V_{C3} = V_{dc} \end{cases} \rightarrow \text{Buck Mode} \quad (2)$$

The details of such a boost and buck mode operation of the proposed DMSC5L-TL inverter connected through a simple L-type filter (L_g) to the grid are discussed in the following subsections.

A. Circuit description during the boost mode operation

Once the input voltage of the inverter is lower than the peak amplitude of the grid, e.g. in case of accessing a lower voltage PV string panel, the proposed inverter must ride through the

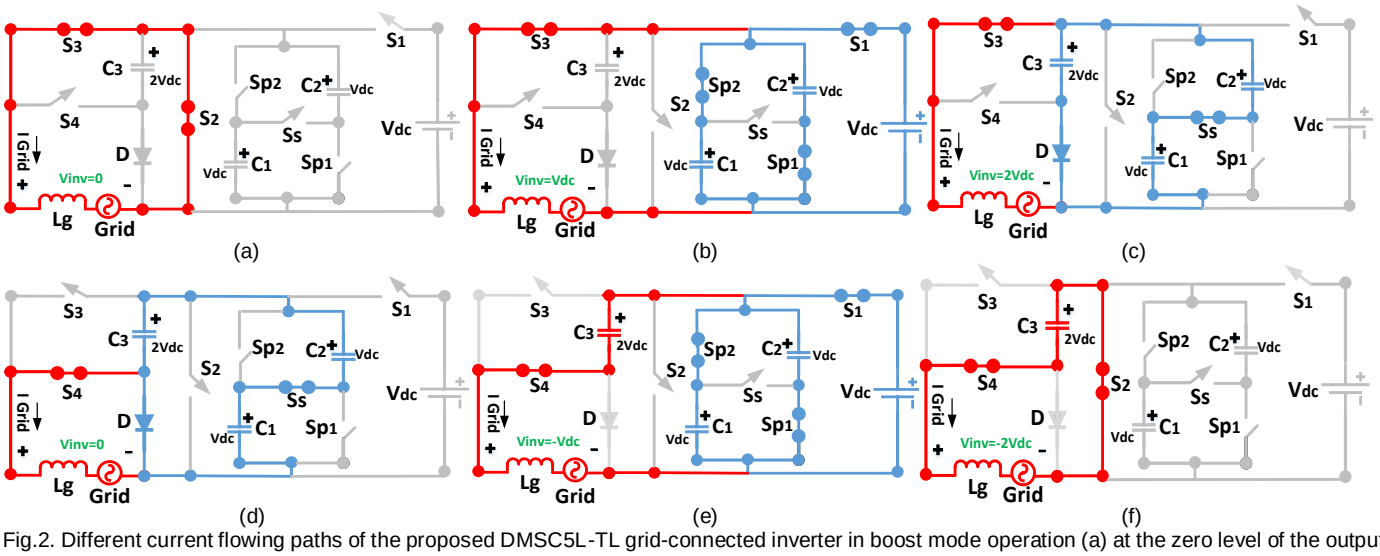


Fig.2. Different current flowing paths of the proposed DMSC5L-TL grid-connected inverter in boost mode operation (a) at the zero level of the output voltage in the positive half cycle (b) at the first positive level of the output voltage (c) at the top positive level of the output voltage (d) at the zero level of the output voltage in negative half cycle (e) at the first negative level of the output voltage (f) at the top negative level of the output voltage.

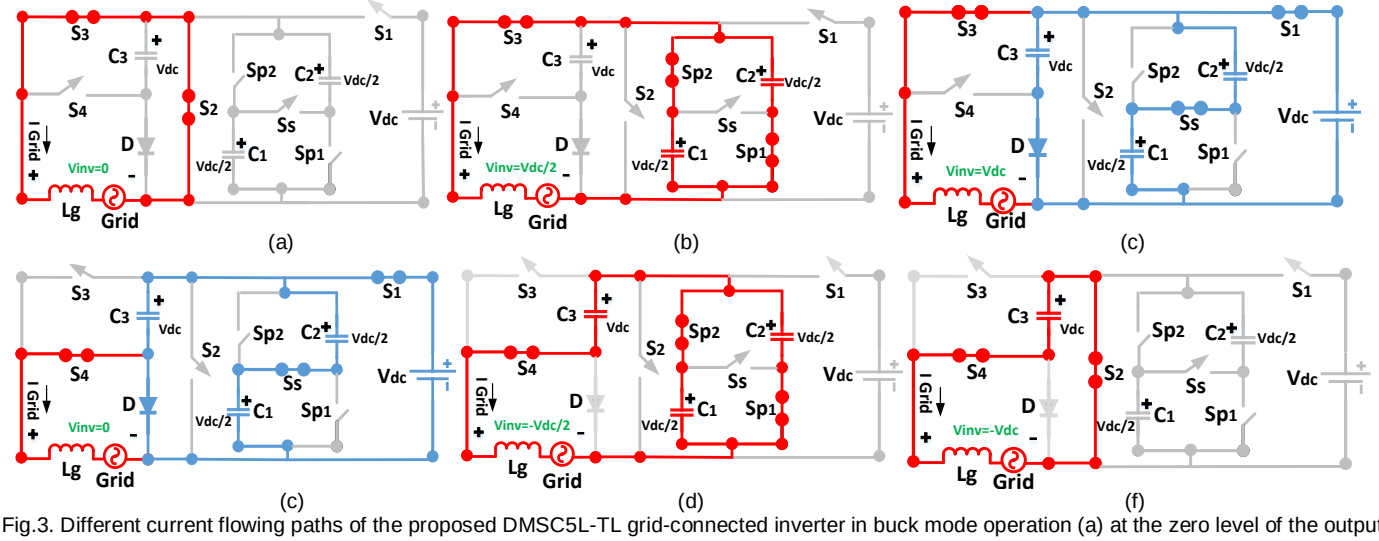


Fig.3. Different current flowing paths of the proposed DMSC5L-TL grid-connected inverter in buck mode operation (a) at the zero level of the output voltage in the positive half cycle (b) at the first positive level of the output voltage (c) at the top positive level of the output voltage (d) at the zero level of the output voltage in negative half cycle (e) at the first negative level of the output voltage (f) at the top negative level of the output voltage.

boost mode operation. Considering V_{dc} as a fixed value of the input dc source voltage that can be a string PV panel with a maximum power point tracking (MPPT) mechanism, the proposed DMSC5L-TL inverter can generate $\pm V_{dc}$, $\pm 2V_{dc}$, and the zero-level of the output voltage. Fig. 2 (a)-(f) illustrate different current flowing paths of the proposed topology within the mentioned five output voltage levels generation. Here, the red and blue lines imply the grid current flowing path and the charging loop of the involved capacitors, respectively. Considering Fig. 2(a), the zero level of the output voltage in positive half cycle of the grid voltage is generated by turning ON contributions of only two power switches (S_3 and S_2) and without involving any of the capacitors in the grid current flowing path. As shown in Fig. 2(b), the first positive output voltage level of the proposed inverter ($+V_{dc}$) can be created by the direct contribution of the input dc source and the power switches S_1 and S_3 . As one can be realized, depending on the grid current direction, both the capacitors of the SPSC cell can be charged to V_{dc} by two ON state parallel switches ($S_{P1}$and S_{P2}). Here, the virtual dc-link capacitor (C_3) is again disconnected from the grid and the input source since the upcoming steady state charged voltage of C_3 makes the diode (D) reverse-biased.

In order to make the top positive output voltage level ($+2V_{dc}$), the series switch of the SPSC cell (S_S) alongside the power switch S_3 must be ON as it can be observed in Fig. 2(c). Here, considering the same direction of the injected grid current and the grid voltage, C_3 is charged to $2V_{dc}$through the charging loop provided by the diode D in forward-biased condition, while both the SPSC cell capacitors will be excluded from the grid current flowing path.

Once the grid voltage is in the negative half cycle, the zero level of the output voltage can be generated again with a different current flowing path. As shown in Fig. 2(d), depending on the positive/negative polarity of the grid current direction, C_3 can be charged/discharged to $2V_{dc}$ once again through the same charging loop as the top positive output voltage level, while by forward biasing the diode D and ON state contribution of S_4, the zero level of the output voltage can be realized. Following this, the first negative output voltage

level ($-V_{dc}$) can be generated by the help of the input dc source voltage and the pre-charged voltage of C_3. Fig. 2(e) shows the current flowing path of this output voltage level, as well. Here, in addition to the ON state power switches S_1 and S_4, both the parallel switches of the SPSC cell must also be ON to provide a charging/discharging loop as for the C_1 and C_2. Therefore, depending on the grid current direction, both such capacitors can be charged/discharged to V_{dc} once again.

Finally, as shown in Fig. 2 (f), the top negative output voltage level ($-2V_{dc}$) in this mode can be produced by the sole contribution of the charged voltage of the C_3 alongwith only two ON state power switches (S_2 and S_4). Here, to avoid the short circuit problem, none of the power switches in the SPSC cell should be ON. Thus both the capacitors C_1 and C_2 will be disconnected from the dc source and the grid.

B. Circuit description of the buck mode operation

When the dc-link voltage or the input voltage is sufficient to produce the grid amplitude requirement, the proposed topology can turn its operation towards the buck mode condition, whilst it is likewise able to generate all the five output voltage levels properly with V_{dc} as the peak value. Similar to the boost mode operation, six different current flowing paths are available to generate five distinctive output voltage levels.

Considering Fig. 3(a), the zero level of the output voltage in positive half cycle of the grid voltage maintains the same switching procedure as provided by the boost mode operation. Hence, again two power switches (S_2 and S_3) must be ON, while all the involved capacitors are disconnected from the grid and the dc source.

Contemporary, to generate the first positive level of the output voltage ($+0.5V_{dc}$), Fig. 3(b) must be considered. Since the upcoming charged voltage of the SPSC cell's capacitors and the virtual dc-link capacitor are on the basis of (2), so this output voltage level is made by the ON state contribution of the S_3, and the pre-charged voltage value of the C_1 and C_2 that are connected in parallel. Hence, depending on the grid current direction, such capacitors can be charged and discharged, whereas regarding the reverse biasing condition of the diode D, C_3 will be disconnected from the supply and the grid.

Consequently, the top positive level of the output voltage ($+V_{dc}$) can be generated by the direct contribution of the input dc source as it can be seen in Fig. 3(c). Herein, through the ON state power switches S_1, S_3, and S_S not only is this voltage level converted to the output, but also with the same polarity of the injected grid current and the grid voltage, all the involved capacitors are charged by the input dc source. As depicted by the blue lines in Fig. 3(c), with the aim of the ON state power switches S_1 and S_S, both SPSC cell's capacitors are in series with the input dc source. Therefore, depending on the grid current direction, they are charged/discharged to $0.5V_{dc}$ magnitude. On the other hand, by forward biasing condition of the diode D, C_3 can also be charged/discharged to V_{dc}.

Similar to the boost mode operation, the zero-output voltage level in the negative half-cycle of the grid voltage can again be made through a different current flowing path as shown in Fig. 3(d). Hereby, the same charging loop of the capacitors as explained for the top positive output voltage level is again used, but the only difference is to changing the state of two power switches S_3 and S_4. Hence, depending on the grid current direction (positive/negative), all the involved capacitors can be directly charged/discharged from the input dc source once again (see the blue lines of Fig. 3(d)).

Taking Fig. 3(e) into account, the first negative level of the output voltage ($-0.5V_{dc}$) is made by disconnecting the input dc source from the grid and using the pre-charged voltage value of the involved capacitors. Here, two paralleled switches of the SPSC cell must be ON, whilst through the reverse biasing the diode D and the ON state contribution of S_4, the voltage level of $-0.5V_{dc}$ can be generated thereby.

Finally, similar to the boost mode operation, the top negative level of the output voltage ($-V_{dc}$) can be generated just by the sole contribution of C_3 and two ON state power switches S_2 and S_4, as shown in Fig. 3(f). Thus, the input dc-source and both the capacitors of the SPSC cell are excluded from the grid and the input dc-source, whereas depending on the grid current direction, C_3 can be charged and discharged.

From the above-mentioned circuit descriptions, it can be revealed that the proposed topology is able to be operated under a wide range of input voltage variations with a provided DM feature. Regarding the self-voltage balancing of the involved capacitors in each mode and considering (1) and (2), the PIV of the involved switches can also be expressed as:

$$V_{S1} = \begin{cases} \pm V_{dc} \rightarrow \text{Boost Mode} \\ V_{dc} \rightarrow \text{Buck Mode} \end{cases} \quad (3)$$

$$V_{Si} = \begin{cases} 2V_{dc} \rightarrow \text{Boost Mode} \\ V_{dc} \rightarrow \text{Buck Mode} \end{cases} \quad i = S, 2, 3, 4 \quad (4)$$

$$V_{SP1} = V_{SP2} = \pm V_{dc} \rightarrow \text{Boost \& Buck Mode} \quad (5)$$

Considering (1)-(2), and (4), it is obvious that without having the buck type feature, four power switches (S_S, S_2, S_3 and S_4) alongside all the involved capacitors should bear a higher stress voltage when the PV string voltage is more than the required peak value of the grid. Apart from such a reasonable value of the PIV, it is worth mentioning that the maximum number of ON state power switches that are involved into the current flowing path at each instant of the proposed topology is only three and four as given by the buck and boost mode operation, respectively. Hence, the proposed topology offers a suitable condition to reduce the conduction losses, as well. Additionally, as can be realized by the different current flowing paths analysis in both modes, two power switches S_3 and S_4 are only being ON during the positive and negative half cycle of the grid, respectively. Hence, they can be switched based on the grid frequency with almost zero switching losses, while other remaining power switches are modulated through high frequency pulse width modulation (PWM) signals.

III. Control Scheme

The overall control block diagram of the proposed grid-connected system is illustrated in Fig. 4. Since the main objective of a grid-tied solar TL inverter is to inject a tightly controlled current to the grid, the desired current reference, i_{ref}, can be generated through the MPPT and the phase-locked loop (PLL) blocks, which is transferred to the proposed DB3C block. Regarding Fig. 4, P_{max},q_{ref}, I_m, and ω denote the maximum active power provided by the MPPT block, desired reactive power, the maximum value of the injected grid current, and the grid angular frequency, respectively.

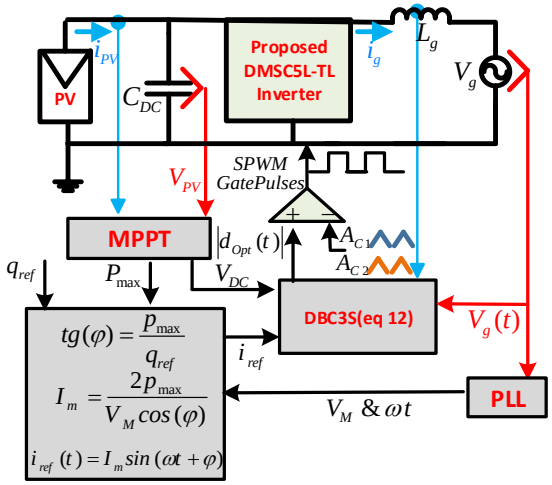


Fig. 4. The overall control block diagram of the proposed topology.

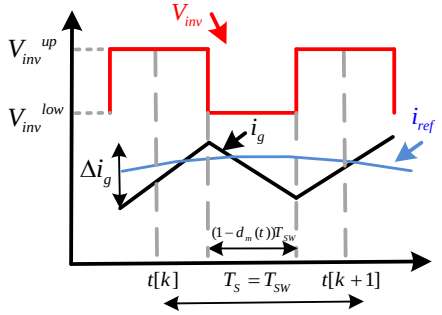


Fig. 5. The typical waveforms of the inverter output voltage and the reference/ injected grid current within a two cycles of the fixed switching frequency.

The proposed DB3C block also requires the measured value of the injected grid/filter inductor current, i_g, within a sampling time, T_S. Considering the instantaneous measured value of i_g, in order to entirely track i_{ref} and generate all the supposed output voltage levels within a fixed switching frequency operation, the injected grid current behavior at the next sampling/switching time can be predicted. Fig 5 shows the detailed operation of the proposed control-block within a sampling/switching time-period, T_{Sw}, between the sampling instant time of "k" and the consecutive future instant "k+1". Since at each switching period, the inverter's output voltage, $V_{inv}(t)$, is switched between two adjacent values, V_{inv}^{up} and V_{inv}^{low} are considered to represent the upper and lower level of $V_{inv}(t)$ at each switching period, respectively. Also, Δi_g is the ripple current across L_g during the switching operation.

Since the inverter voltage, $V_{inv}(t)$, and the grid voltage, $v_g(t)$, are connected via a simple L-type filter, the following continuous-time dynamic relationship can be obtained:

$$V_{inv}(t) = L_g \frac{di_g(t)}{dt} + v_g(t) \quad (6)$$

On the other hand, the initial measured value of the injected grid current at the sampling instant k is denoted by $i_g(k)$, as depicted in Fig. 5. Therefore, the next sampling instant behavior of the injected grid current is denoted by $i_g(k+1)$, which can be predicted by using the following prediction modeling:

$$i_g(k+1) = i_g(k) + f_{inc}(k) d_m(k) T_{Sw} + f_{dec}(k)\big(1 - d_m(k)\big)T_{Sw} \quad (7)$$

TABLE I
SWITCHING STATES OF THE PROPOSED DMSC5L-TL INVERTER OPERATED WITH THE PROPOSED DB3C METHOD

$d_{Opt}(t)$ POLARITY	SPWM CONDITION	ON STATE SWITCHES @BOOST MODE	v_{inv} @ BOOST MODE	ON STATE SWITCHES @BUCK MODE	v_{inv} @BUCK MODE
POSITIVE	$\|d_{Opt}(t)\| \geq A_{C1}$	S_S , S_3	$2V_{dc}$	S_S, S_1, S_3	V_{dc}
	$A_{C2} \leq \|d_{Opt}(t)\| < A_{C1}$	S_{P1}, S_{P2}, S_1, S_3	V_{dc}	S_{P1}, S_{P2}, S_3	$0.5\,V_{dc}$
	$\|d_{Opt}(t)\| < A_{C2}$	S_2 , S_3	0	S_2 , S_3	0
NEGATIVE	$\|d_{Opt}(t)\| \geq A_{C1}$	S_2 , S_4	$-2V_{dc}$	S_2 , S_4	$-V_{dc}$
	$A_{C2} \leq \|d_{Opt}(t)\| < A_{C1}$	S_{P1}, S_{P2}, S_1, S_4	$-V_{dc}$	S_{P1}, S_{P2}, S_4	$-0.5\,V_{dc}$
	$\|d_{Opt}(t)\| < A_{C2}$	S_S , S_4	0	S_S, S_1, S_4	0

where, $f_{inc}(k)$ and $f_{dec}(k)$ denote as the upward (increasing) and the downward (decreasing) slope of i_g during each intersampling. Moreover, $d_m(k)$ represents the switching duty cycle in which its optimal value over a full cycle of the grid-frequency has to be synthesized by a Sinusoidal PWM (SPWM) stage. Considering (6) and Fig. 5, $f_{inc}(k)$ and $f_{dec}(k)$ can be expressed as:

$$f_{inc}(k) = \frac{di_g}{dt} = \frac{V_{inv}^{up} - v_g(k)}{L_g} \quad (8)$$

$$f_{dec}(k) = \frac{di_g}{dt} = \frac{V_{inv}^{low} - v_g(k)}{L_g} \quad (9)$$

where, $v_g(k)$ is the measured value of the grid voltage at the beginning of each sampling period. Having taken into account the fact that the control target of the proposed DB3C method is to reach a zero steady-state error between the injected grid current and its reference, the following expression can be written:

$$e = i_{ref}(k+1) - i_g(k+1) \quad (10)$$

where, $i_{ref}(k+1)$ is the next behavior of the sinusoidal reference current and through a fourth order Lagrange extrapolation, it can be found out by (11) [26].

$$i_{ref}(k+1) = 4\,i_{ref}(k) - 6\,i_{ref}(k-1) + 4\,i_{ref}(k-2) - i_{ref}(k-3) \quad (11)$$

Now, considering (7)-(11), the optimal value of $d_m(k)$ in the discrete-time domain ($d_{Opt}(k)$) is obtained as:

$$d_{Opt}(k) = \frac{L_g\big(i_{ref}(k+1) - i_g(k)\big) + \big(v_g(k) - V_{inv}^{low}\big)T_{Sw}}{\big(V_{inv}^{up} - V_{inv}^{low}\big)T_{Sw}} \quad (12)$$

Now, taking into account the fact that $d_{Opt}(t)$ always varies between -1 and 1 with a sinusoidal behavior over the grid's frequency, to ease the SPWM implementation, an absolute function of $d_{Opt}(t)$ is considered and then compared with two level-shifted high frequency triangular carrier waveforms (A_{C1} and A_{C2}). Besides tracking i_{ref}, another control target of the proposed DB3C method is to keep the switching frequency fixed. Hence, the frequency of both such carriers must be according with the sampling/switching period provided by $d_{Opt}(t)$ ($f_{Sw} = \frac{1}{T_{Sw}}$). Considering such notions and taking into account the operating principles of the proposed topology in both modes, the ON switching states of the power switches with such an SPWM procedure can be deduced from Table I. Here, the optimal duty cycle with two 10 kHz carriers waveforms, the injected grid/reference current, the 5L inverter's output with the grid/dc-link voltage, and all the gate

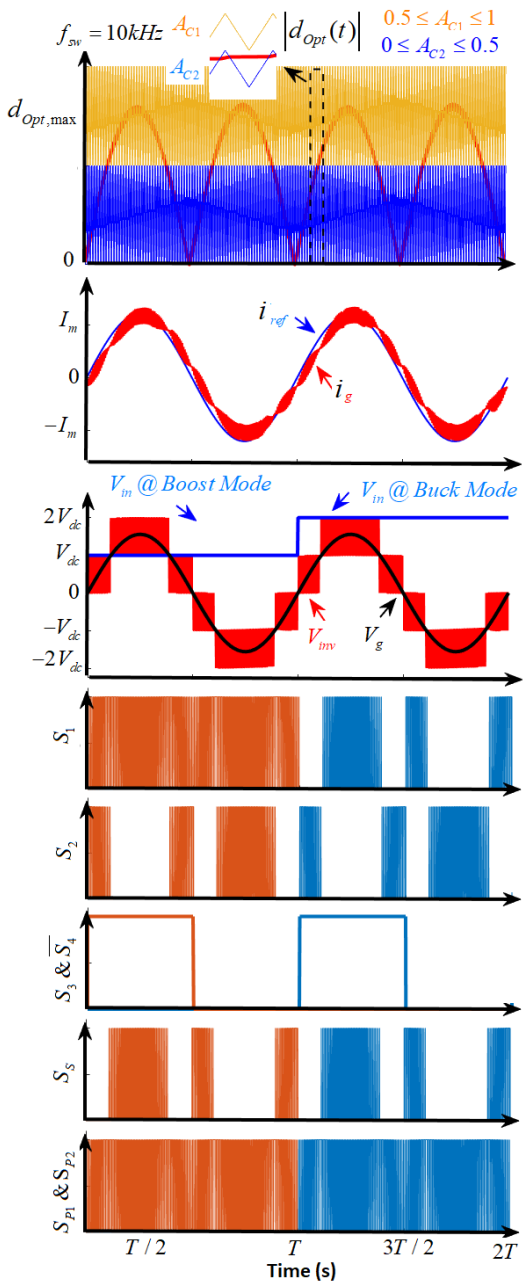


Fig. 6. Typical waveforms of the proposed DB3C with the final gate switching pulses of the switches @ 10 kHz fixed switching frequency.

switching pulses of the involved switches during the operation in boost and buck mode can be observed in Fig. 6. Note that, the small phase difference between i_{ref} and i_g is due to the low value of the switching frequency and the instant capturing time since there is always a leading phase difference between $i_{ref}(k)$ and $i_g(k+1)$ over each sampling time. Such a small phase shift would be more visible when a lower rate of switching frequency is adopted. Also, it is worth emphasizing that similar to any other predictive-based controllers and in case of having a significant mismatching condition between the actual value of L_g and the value used in the calculation, the injected grid current THD is degraded owing to the high frequency ripple [27].

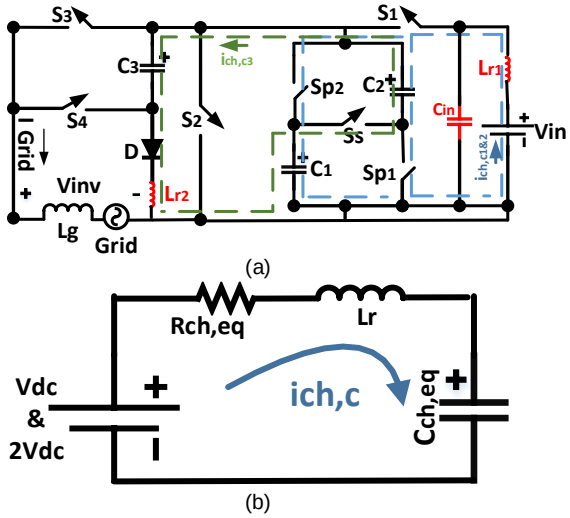


Fig. 7. QSC operation of the proposed DMSC5L-TL inverter (a) main circuit configuration emphasizing the charging flow path of the capacitive charging loop, (b) the equivalent QSC-RLC circuit.

IV. Design Guidelines

Three involved capacitors and a single output L-type filter inductor are the integrated passive elements of the proposed DMSC5L-TL inverter topology. In the following subsections, some descriptions for a correct value design of the passive elements are presented.

A. Filter Inductor Design

Regarding the aforementioned control procedure of the proposed inverter, the average passing current through the inductor can be found out by (13) [23]:

$$i_g(t) = \frac{1}{L_g}\int_0^{d_{Opt}(t)T_{Sw}} v_L(\tau)d\tau + i_g(0) \qquad (13)$$

where, $i_g(0)$ is the initial stored current of the inductor, and $v_L(\tau)$ is the voltage across it. So, with respect to (13) and considering $\Delta i_{g,max}$ as the maximum allowable ripple current across the inductor that is taking place at the peak, the minimum required value of L_g can be taken as:

$$L_{g,min} = \frac{(V_{inv}^{up} - V_M)d_{Opt,max}}{f_{sw}\Delta i_{g,max}} \qquad (14)$$

where, $d_{Opt,max}$ and V_M, respectively, denote as the maximum value of the optimal duty cycle of the switches over the grid frequency and the maximum amplitude of the grid voltage detected by the PLL block.

B. Capacitor's Determination

To determine a suitable value for the capacitance of the virtual dc-link (C_3) and the SPSC cell capacitors (C_1 and C_2), their maximum discharging time interval and the voltage difference across them (ΔV_{C1}&ΔV_{C2}andΔV_{C3}) are of importance. Considering the longest discharging time interval of the capacitors (α, β), the following equation can be expressed:

$$\frac{1}{C_i}\int_\alpha^\beta i_{Ci}(t)dt = \Delta V_{Ci} \quad i = 1,2,3 \qquad (15)$$

where, i_{Ci} is the passing current through the capacitors. Considering (P_{Out}) as the output power injected to the grid and regarding (15), $i_{Ci}(t)$ can be directly relevant to the i_g through finding the discharging duty cycles of the capacitors [23]; so the

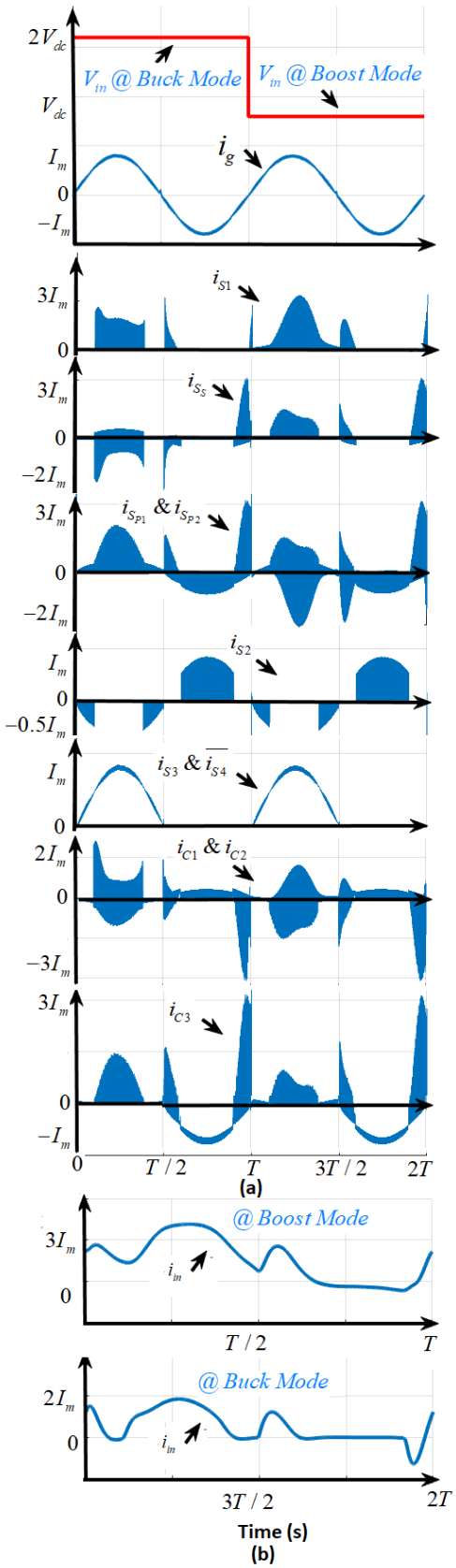


Fig. 8. (a) Typical current stress waveforms of all the involved power switches and the capacitors within the operation of the proposed DMSC5L-TL inverter in both modes, (b) typical input current waveform in both operation modes and in presence of the QSC input inductor.

required capacitance of the involved capacitors can be determined as follows:

$$C_{1\&2} = \frac{P_{Out}}{V_{dc}\Delta V_{C1\&2}}\left(\frac{2T}{3} + \frac{0.5T}{d_{Opt,max}\pi}\sqrt{1-\frac{1}{4d_{Opt,max}^2}}\right) \quad (16)$$

$$C_3 = \frac{P_{Out}}{V_{dc}\Delta V_{C3}}\left(\frac{2T}{3} + \frac{T}{d_{Opt,max}\pi}\sqrt{1-\frac{1}{4d_{Opt,max}^2}}\right) \quad (17)$$

where, T is the grid fundamental period. Taking into account that the C_3 has a crucial role in both the operating modes to inject the power to the grid in negative half cycle of the grid (the first and second negative output voltage levels) and using (16) and (17), it will be obvious that its capacitance has to be larger than that ones as used in the SPSC cell.

V. Quasi-Soft Charging Operation and Current Stress Analysis

Similar to any other SC-based inverter, all power switches that are involved in the charging path of the involved capacitors for the proposed DMSC5L-TL inverter may experience additional losses, which can degrade the performance of the overall system in higher power ratio. To alleviate the concern of the capacitors charging current, two small inductors, L_{r1} and L_{r2}, are integrated into the charging loop of the involved capacitors as shown in Fig. 7 (a). Therefore, by appropriate designing of such integrated inductors, the charging operation of the involved capacitors can possess a quasi-soft charging (QSC) behavior. As depicted in Fig. 7 (b), the equivalent charging loop of the involved capacitors can then be interpreted as a simple RLC circuit, where $R_{ch,eq}$and C_{eq} denote the parasitic ON state resistance of the involved power switches and also the equivalent capacitance of the path, respectively. Hence, to make a QSC operation for the capacitor's charging current ($i_{Ch,Ci}(t)$), the above-mentioned RLC circuit may possess either under-damp or over-damp operations [28]. Considering the damping factor of a typical RLC circuit equals to $\frac{\sqrt{2}}{2}$, the value of L_r for the under-damp operation can be designed as follows:

$$L_r = \frac{C_{eq}(R_{Ch,eq})^2}{4} \quad (18a)$$

Therefore, by solving the differential equation of the RLC circuit, the value of $i_{Ch,Ci}(t)$ can be obtained as follows:

$$i_{Ch,Ci}(t) = \frac{V_{ch,i}-V_{Ci,max}+\Delta V_{Ci}}{L_r\omega_r}e^{-\alpha t}\sin\omega_r t \quad i = 1\&2, and\ 3 \quad (18b)$$

where, $V_{ch,i}$ is the desired balanced voltage of each of the involved capacitors. e. g. V_{dc} and $2V_{dc}$ for $C_1\&C_2$ and C_3, respectively. Also, $V_{Ci,max}$ is the maximum variation of the balanced voltage across each capacitor, whereas ω_r is the resonant frequency that must cover the operating switching frequency of the proposed DMSC5L-TL inverter to make a suitable impedance in the charging loop of the capacitors. In this case, the coefficient of α is constant and is equal to $R_{ch,eq}/2L_r$.

Moreover, as for the over-damp operation of such an equivalent RLC circuit, the value of L_r should be very small, whilst C_{eq} must possess larger values to cancel out the effect of large ripple voltages. Hence, the charging current of $i_{Ch,Ci}(t)$ can offer the following expression:

$$i_{Ch,Ci}(t) = \frac{C_{eq}}{2}\left(\delta_1\rho_1 e^{\delta_1 t} + \delta_2\rho_2 e^{\delta_2 t}\right) \quad (19a)$$

Table II. A Comparison Between the Proposed Topology and Different TL Grid-Connected Converters.

Type of Converter		No. of Components				Max No. of ON-Switches	Minimum V_{in} /Buck&Boost Feature	No. of Levels	Leakage Current	Reactive Power Support	Capacitors Charge Balancing	Reported Rated Efficiency
		S	D	C	L							
H5 [5]		5	-	2	2	3	320 V/Only Buck	3	Low	Yes	Not needed	98.5%@0.5kW
HERIC [6]		6	2	2	2	2	320 V / Only Buck	3	Low	NO	Not needed	97% @1kW
OH5 [7]		6	-	2	2	3	320 V / Only Buck	3	Low	Yes	Not needed	97.2@1kW
Dual Buck [8]		9	-	2	4	3	160 V/ Only Buck	3	Low	Yes	Not needed	98.5%@2kW
H6 [9]-[10]		6	2	2	2	3	320 V / Only Buck	3	Low	Yes	Not needed	97.4%@1kW
ANPC [11]		6	2	2	1	2	640 V/ Only Buck	5	Very Low	Yes	Needed	NA@1kW
ABNPC [12]		8	-	3	1	2	320 V / Only Buck	5	Very Low	Yes	Inherent	97.8%@1.2kW
CG-Type [13]		5	-	2	2	3	320 V / Only Buck	3	Zero	Yes	Inherent	95.5%@500W
CGType[17]	Type I&II	4	1	3	1	2	320 V / Only Buck	3	Zero	Yes	Inherent	99.1%@800W
	Type III	4	-	3	1	2	320 V / Only Buck	3	Zero	Yes	Inherent	96%@800W
CG-Type [18]		4	2	4	2	2	320 V / Only Buck	3	Zero	Yes	Inherent	95.2%@500W
CG-FC-based [19]		6	1	3	1	3	320 V / Only Buck	5	Zero	Yes	Needed	95.8%@1.2kW
CG-FC-based [20]		6	-	3	1	3	320 V / Only Buck	5	Zero	Yes	Needed	97%@1kW
CG-SC-based [21]		6	1	3	1	3	160 V /Only Boost	3	Zero	Yes	Inherent	98.1%@500W
CG-SC-based [22]		6	2	3	1	3	160 V /Only Boost	3	Zero	Yes	Inherent	98.1%@500W
CG-SC-based [23]-[24]		6	2	3	1	3	160 V /Only Boost	5	Zero	Yes	Inherent	98.1%@600W
DM-HERIC-based [25]		10	4	3	4	5	160 V/Buck&Boost	5	Low	Yes	Needed	97.3%@1kW
DM-ANPC-based [26]		10	-	4	1	5	320 V/Buck&Boost	5	Very low	Yes	Needed	NA@1.5kW
Proposed DMSC5L		9	1	4	1	4	160 V/Buck&Boost	5	Zero	Yes	Inherent	96.5%@600W (Boost) 97%@600W (Buck)

$$\begin{cases} \delta_{1,2} = -\frac{R_{ch,eq}}{2L_r} \pm \sqrt{\left(\frac{R_{ch,eq}}{2L_r}\right)^2 - \frac{2}{L_r C_{eq}}} \\ \rho_{1,2} = \frac{\delta_{1,2}}{\delta_1 - \delta_2} \Delta V_{Ci} \end{cases} \quad (19b)$$

Having taken into account the described QSC procedure, the current stress profile of all the involved power switches and capacitors within both the buck and boost modes operation of the proposed DMSC5L-TL inverter have been illustrated in Fig. 8 (a), while I_m is the maximum value of the injected grid current. Concerning the value of $R_{ch,eq}$, and the given design values of the involved capacitors expressed in Section IV, the maximum charging current of the capacitors would be around $3I_m$ and $2I_m$ for the boost and buck mode of the operation, respectively. Regarding this and the current flowing path analysis, it can be revealed that four power switches of S_1, S_S, S_{P1}, and S_{P2} are tolerating the maximum current stress equal to around $3I_m$ and $2I_m$ in the boost and buck mode of the operation, respectively, while the remaining switches are passing a true shape of the grid current waveform. Apparently, without the QSC inductors, the charging current flowing through the capacitors and the switches in the capacitive charging loops is large, which limits the power level of the converter. Moreover, by incorporating the input inductor of the QSC cell, the shape of input current will be different from the discontinuous current stress profile of S_1 as shown in Fig. 8 (b).

VI. Comparative Study

To show the potential capability of the proposed DMSC5L-TL inverter over its other existing counterparts, a comparative study from different aspects is given in this Section. Herein, the comparison is done in Table II, which includes the number of required active/passive elements (including the pre-assumed filter components), the maximum number of ON state power switches, required value of the input dc voltage and the potential mode transition, number of output voltage levels, leakage current value, reactive power support ability, capacitor charge balancing requirement, and the reported measured efficiency. Here, the value of the leakage current is considered low and very low if it is less than 120 mA and 10 mA, respectively [24].

As is clear from Table II, excluding the proposed topology, only two other structures mentioning as [25] and [26] can be operated within both modes of the operation. However, as opposed to the proposed topology, none of them is CG-based; therefore, the leakage current cannot be fully eliminated. Moreover, [25] needs more numbers of active/passive elements

Table III. Parameters used for Analysis and Measurements.

Element	Type	Description
Power Switches	IPW60R099C6	650 V/33 A (Continuous)
Gate Drivers	ACPL-P343	IC Chip
Isolated DC Supply of Gate Drivers	MTU1S0512MC	IC Chip
Power Diode	C5D50065D	650 V/100 A
Current/Voltage Transducer	LA55P	USM3IV
Microcontroller	DSP	TMS320F28379D
Local Grid's Peak Voltage/ Frequency	311 V/50 Hz	-
Switching Frequency	20 kHz	-
C_1&C_2 and C_3	193 PUR-SI	$0.47mF$ & $1mF$
Filter's Inductor	Ferrite Core	2.3 mH

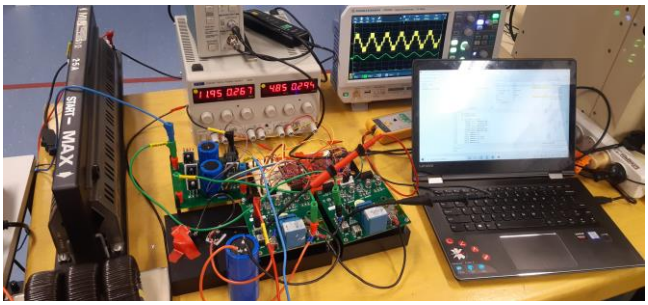
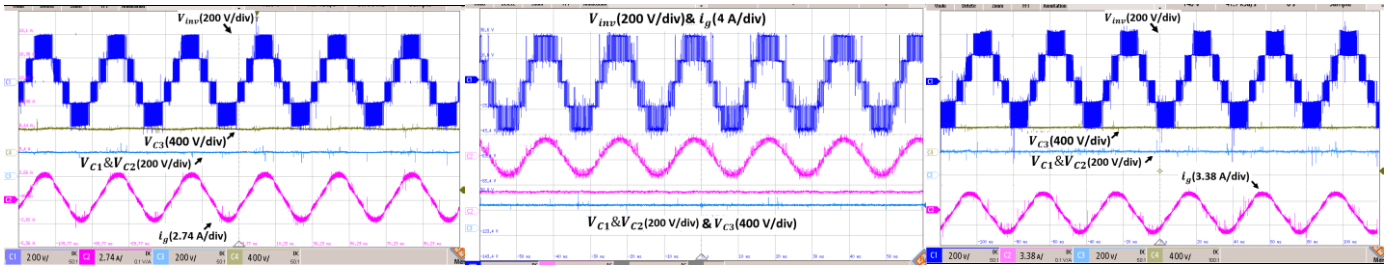
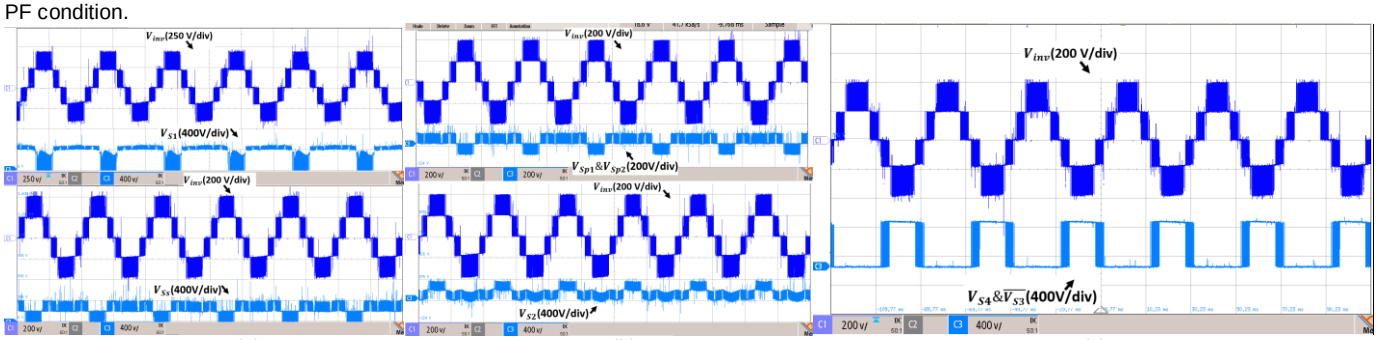


Fig. 9. A picture of the built setup.



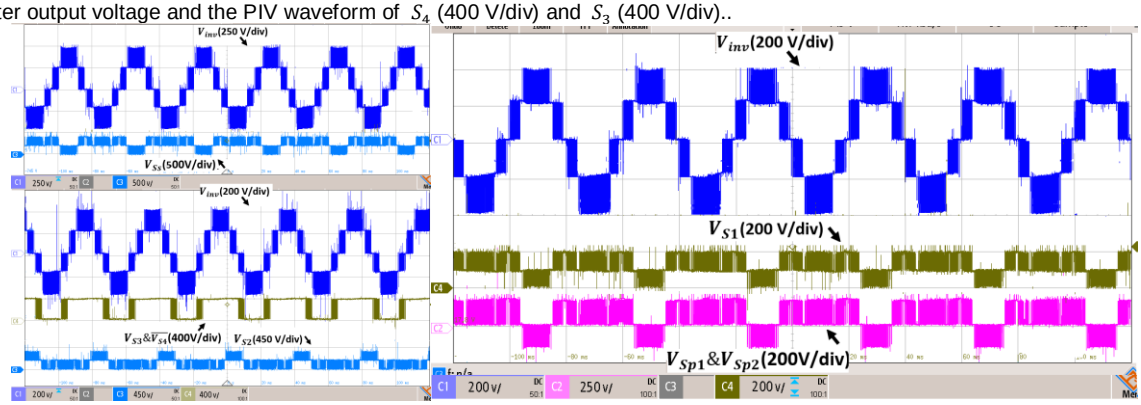
(a) (b) (c)

Fig. 10. Measured waveforms of the proposed DMSC5L-TL-inverter showing: the inverter output voltage (200 V/div), the capacitors voltage (400 and 200 V/div), and the injected current @ (a) buck mode of the operation and once the input voltage is 400 V, at unity PF condition (b) boost mode of operation and once the input voltage is 200 V at unity PF condition. (c) boost mode of operation and once the input voltage is 200 V at non-unity PF condition.



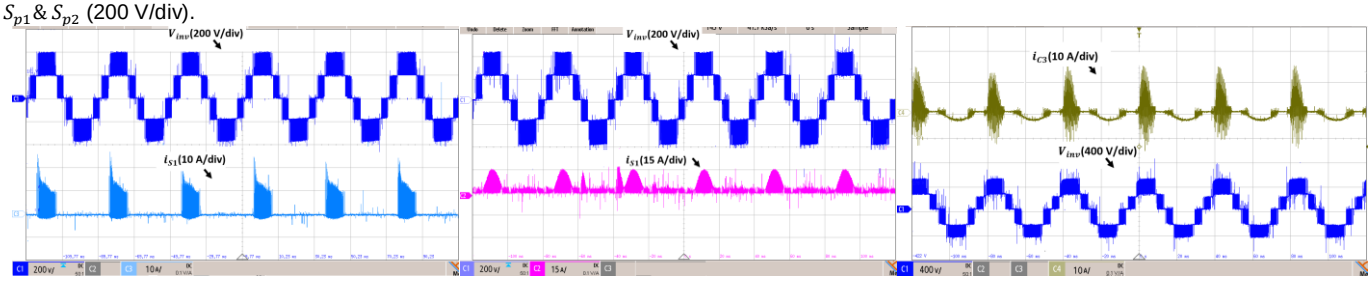
(a) (b) (c)

Fig. 11. Measured waveforms of the proposed DMSC5L-TL-inverter in buck mode of operation showing (a) the inverter output voltage and the PIV waveforms of S_1 (400 V/div) and S_4 (400 V/div) (b) the inverter output voltage and the PIV waveforms of S_{p1}& S_{p2} (200 V/div) and S_2 (400 V/div), (c) the inverter output voltage and the PIV waveform of S_4 (400 V/div) and S_3 (400 V/div)..



(a) (b)

Fig. 12. Measured waveforms of the proposed DMSC5L-TL-inverter in boost mode of operation showing (a) the inverter output voltage and the PIV waveforms of S_s (500 V/div) , S_4 (400 V/div) , and S_2 (450 V/div), (b) the inverter output voltage and the PIV waveforms of S_1 (200 V/div) and S_{p1}& S_{p2} (200 V/div).



(a) (b) (c)

Fig. 13. Measured waveforms of the proposed DMSC5L-TL-inverter (a) the inverter output voltage (200 V/div) and the current passing through S_4(10 A/div) at buck mode of operation (b) the inverter output voltage (200 V/div) and the current passing through S_4(15 A/div) at boost mode of operation (c) the inverter output voltage and the current passing through C_3 (10 A/div) at buck mode of the operation.

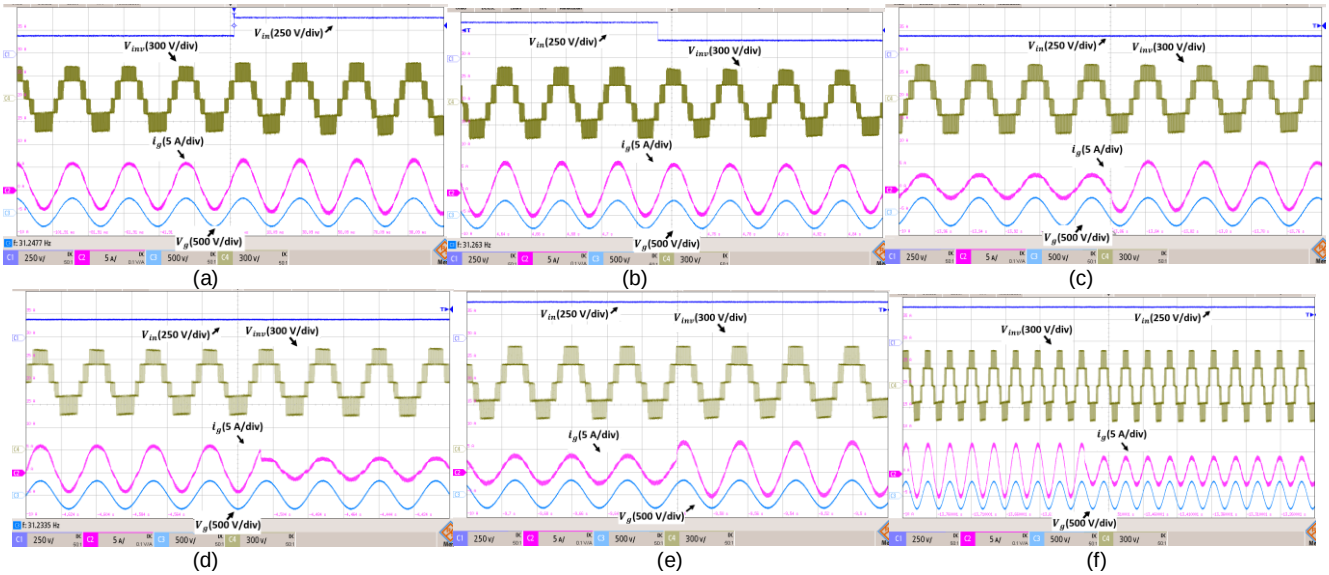


Fig. 14. Measurement dynamic results showing the input voltage (250 V/div), the inverter output voltage (300 V/div), the injected grid current (5 A/div), and the grid voltage (500 V/div) once (a) the input voltage is changed from 200 V to 400 V (from boost to buck mode) (b) once the input voltage is changed from 400 V to 200 V (from buck to boost mode) (c) once the output power is changed from 50 % ratio to 100% in boost mode (d) once the output power is changed from 100 % ratio to 50% in boost mode (e) once the output power is changed from 50 % ratio to 100% in buck mode (f) once the output power is changed from 100 % ratio to 50% in buck mode.

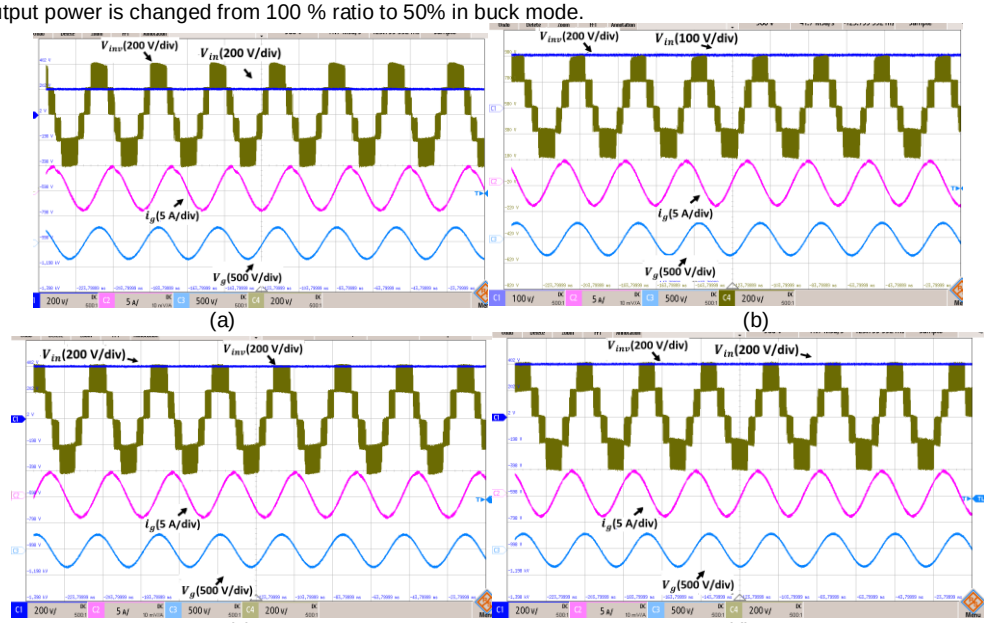


Fig. 15. Measurement results showing the reactive power support capability of the proposed DMSC5L-TL inverter (a) in the boost mode with lagging PF condition (b) in the boost mode with leading PF condition (c) in the buck mode with lagging PF condition, and (d) in the buck mode with leading PF condition.

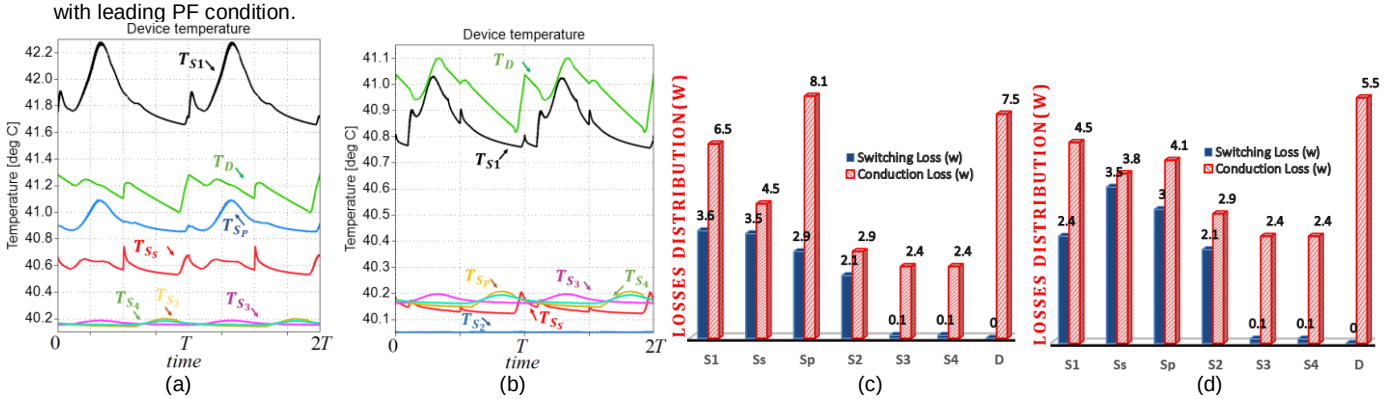


Fig. 16. Semiconductors junction temperature and loss analysis results obtained by the PLECS @1 kW injected active power (a) for the boost mode of the operation (b) for the buck mode of the operation (c) for the boost mode of the operation, (d) for the buck mode of the operation.

with a charge balancing control procedure of the dc-link capacitors that can increase the complexity/losses. Here, [26] has used four bidirectional power switches instead of three ones as used in the proposed topology. Having considered a standard local grid with 310 V as the peak voltage, the DM-ANPC-based topology presented in [26] needs at least 320 V input voltage for the grid-connected applications, whereas because of step-up feature of the proposed DMSC5L-TL inverter in the boost mode, it only needs a 160 V dc supply as the input. Regarding this comparative table, there might be found some topologies with lower number of semiconductor devices; yet, even their maximum number of output voltage levels is only three, or their structures lack in providing an DM ride through capability.

VII. Verification Results

In order to verify the correct performance of the proposed DMSC5L-TL inverter (Fig. 1) with the presented DB3C grid connected control strategy (Fig. 6), some laboratory measurement results are presented in this Section. A picture of the built prototype is depicted in Fig. 9 and the circuit specifications of all the measured waveforms are summarized in Table III. In this case, all the involved passive element values have been selected based on the given design guideline procedure in Section IV. A generation of CoolMOS™ C6 power transistors from Infineon Tech have also been utilized in the experiment owing to their reliable performance for handling the pulsating current of the SC-based circuits. Moreover, the drain-source ON-state resistance of such type of switches is relatively low, which helps the switches to possess less power dissipation when operating at higher output power values.

An Elektro-Automatik (EA) PV emulator (model EA-PSI-9750-12) was used as an adjustable dc laboratory power supply to electrically feed the proposed DMSC5L-TL inverter throughout the experimental tests. A Texas Instrument TMS320F28379D DSP was also employed to generate the required PWM signals of all the involved power switches through the Code Composer Studio Software. Throughout all the experiments, the value of the input dc-power supply is fixed at 200 V and 400 V for the boost and buck mode operations, respectively.

The peak of reference current for the proposed DB3C-SPWM technique in both buck and boost mode cases has been set at 3 A for a RL load with values of 100 Ω and 1.8 mH. Also, according to Fig. 7 (a), a small shielded QSC inductor of 3.6μH (part number SER-1412-362-ME) has been placed in the charging path of the capacitors to alleviate the charging current concern of the proposed DMSC5L-TL inverter during both operation modes. In throughout the experiment, a value of 1mF for C_{in} is chosen to form the QSC input filter.

Regarding such observations, the steady state measured waveforms of the proposed inverter output voltage, the load current and the balanced voltage of all the integrated capacitors operating as buck and boost modes have been shown in Fig. 10 (a)-(c), respectively. Herein, Fig. 10 (a) and (b) are respectively related to the buck and boost operations mode of the proposed topology in the unity power factor (PF) condition of the load current, whilst Fig. 10 (c) is pertained to the non-unity PF condition of the proposed inverter in the boost mode of the operation. As can be seen, all five output voltage levels with a peak value of 400 V in both buck and boost operation modes are properly generated, while the peak of the load current waveform for both the cases is at its desired reference. Additionally, it can be confirmed that the balanced voltage of the SPSC cell capacitors in both modes is 200 V, while the steady-state voltage across the virtual dc-link capacitor, C_3, is 400 V. The measured PIV waveforms of all the integrated switches with the resulting 5L inverter output voltage in both buck and boost operation modes can also be seen in Fig. 11 and 12, respectively. As can be realized, the results are in accordance with the analysis presented in (3)-(5). The measured current passing through S_1 with the 5L output voltage of the proposed inverter for both buck and boost operation modes are also shown in Fig. 13 (a)-(b), while the current passing through the virtual dc-link capacitor for a buck operation mode is shown in Fig. 13 (c). These results confirm the fact that the QSC inductors can alleviate the large inrush current concern of the available SC-based converters.

To evaluate the dynamic performance of the proposed DMSC5L-TL grid-tied inverter modulated based on the proposed DB3C-SPWM technique, some measurement results obtained from the OPAL RT-OP5700 platform are shown in Fig. 14 (a)-(f). To do this, an RT-LAB simulation software is used to implement the closed-loop control and respective modulation strategy in the OPAL system. The grid-connected model of the proposed DMSC5L-TL inverter via an L-type filter is also developed through the incorporated eHS module of the OPAL-RT system. The time-step of the OPAL-RT is also set at 50μS to mimic the 20 kHz fixed switching operation of the proposed DB3C-SPWM technique. Regarding the DM capability of the proposed topology and having considered the peak requirement of the grid voltage, the input dc source voltage is again kept constant at 200 V in boost mode operation, while it is suddenly changed to be 400 V during the buck mode operation. Here, a peak of 5 A as for the reference current of the proposed DB3C strategy in the unity PF operation has been considered, which results in almost 0.8 kW active power injection to the grid. As can be realized in Fig. 14 (a) and (b), the peak of inverter output voltage is fixed at 400 V whilst maintaining all its 5L output voltage waveform irrespective of a step change within a wide input dc voltage changes in both the upward and downward directions. This confirms the acceptable flexibility of the proposed topology to dynamically ride through both modes of operation in respect to the input dc voltage changes. The stable performance of the proposed inverter from injecting active power to the grid viewpoint can also be seen during these step-change conditions of the input dc-voltage.

To evaluate the precise tracking performance of the injected grid current and the fast dynamic capability of the proposed control system, a step change in the current reference (from 100 % to 50 % of the rated power in both directions) is applied. As for the boost operation mode, the input dc source voltage is again kept fixed at 200 V, while for a buck operation mode is set to 400 V. As can be seen by the captured results presented in Fig 14 (c)-(f), a proper closed-loop dynamic response of the injected grid current can be achieved in both operation modes, while generating all five levels in the output voltage.

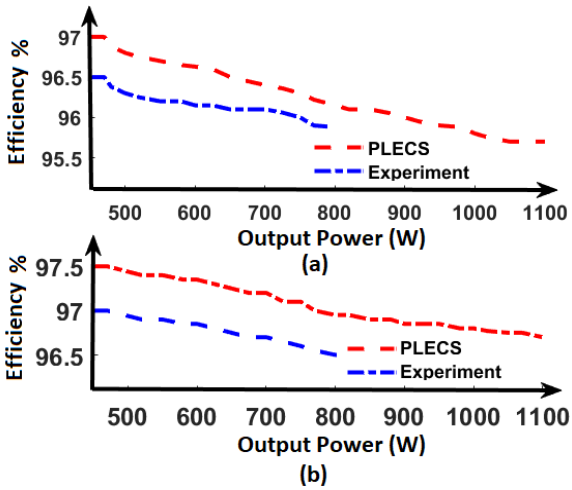


Fig. 17. Efficiency versus output active power curve of the proposed DMSC5L-TL inverter (a) for the boost mode of operation (b) for the buck mode of operation.

The reactive power support feature of the proposed DMSC5L-TL inverter in both operation modes has also been verified by the real-time measurement results obtained from OPAL-RT. The results are shown in Fig. 15 (a)-(d). Here, it can be observed that the converter can inject reactive power to the grid in both cases of lagging and leading PF conditions. Herein, similar to the previous studied case, the input voltage for the boost mode is fixed at 200 V, while for a buck mode is set to 400 V.

Finally, in order to further investigate the performance of different involved semiconductor devices used in the proposed DMSC5L-TL inverter, a thermal and loss analysis at 1 kW injected active power have been conducted by the help of an industry-based standard software PLECS. The results for both the cases in boost and buck operations mode are illustrated in Fig. 16 (a)-(d). Here, the exact model and part number of the involved switching devices listed in Table III have been used in the PLECS for both the operating junction temperature behavior and loss analysis. Also, a constant ambient temperature of $40°C$ with a uniform distributed temperature across the heat sink is considered during all the thermal analysis. Regarding the working principle of the proposed DMSC5L-TL inverter and the importance of QSC inductors placed in the charging loops of the capacitors, a stable average junction temperature of less than $44°C$ is achieved for all the semiconductor devices in both the operating modes as can be confirmed by Fig. 15 (a) and (b). This feature can further highlight the acceptable performance of the proposed topology from a reliability viewpoint of the involved switching devices. Herein, since this power switch S_1, is in the charging loop of both the SPSC cell and the virtual dc-link capacitor, its average operating temperature is higher than other switches in both operation modes. The same logic can also be applied for the single power diode D incorporated into the charging loop of C_3. The resulting switching and conduction losses of all the involved power switches and the diode provided by PLECS is summarized in Figs. 15 (c) and (d). The reported overall loss of the proposed topology at 1 kW injected power is around 46.6 W and 36.8 W for the boost and buck operation modes, respectively. Such obtained values give around 95.6% and 96.7% of the overall efficiency for the proposed DMSC5L-TL inverter. A comparative efficiency curve comparing the output power between the results provided by the PLECS versus the results obtained by experimental measurements has also been shown in Fig. 16 (a) and (b). The experimental efficiency of the proposed DMSC5L-TL inverter in both operation modes have been measured using a Voltech PM3000A Universal Power Analyzer. As can be seen, the results are close to each other, and as expected the buck operation mode of the proposed topology possesses higher efficiency due to the reduced current stress profile of the switches.

VIII. Conclusion

A novel DMSC5L-TL inverter has been introduced in this work. The proposed topology is based on a CG circuit architecture, which provides almost zero leakage current value for the PV grid-connected applications. Through the series-parallel switching conversion of the involved switches in both the buck/boost modes, the voltage across all the involved capacitors is inherently balanced, allowing the converter to generate five distinctive output voltage levels despite the presence of a wide input voltage variations. To control the proposed topology during a grid-connected condition, a simple dead-beat current controller technique with a fixed switching frequency operation has also been employed, which can ride through both the active/reactive power support mode. A comparative study alongside simulation and experimental results have also been presented to verify the feasibility and correctness of the proposed topology.

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