Aalborg Universitet



A Review of Multilevel Converters With Parallel Connectivity

Fang, Jingyang; Blaabjerg, Frede; Liu, Steven; Goetz, Stefan M.

Published in: I E E E Transactions on Power Electronics

DOI (link to publication from Publisher): 10.1109/TPEL.2021.3075211

Publication date: 2021

Document Version Accepted author manuscript, peer reviewed version

Link to publication from Aalborg University

Citation for published version (APA): Fang, J., Blaabjerg, F., Liu, S., & Goetz, S. M. (2021). A Review of Multilevel Converters With Parallel Connectivity. *I E E Transactions on Power Electronics*, *36*(11), 12468-12489. [9415177]. https://doi.org/10.1109/TPEL.2021.3075211

General rights

Copyright and moral rights for the publications made accessible in the public portal are retained by the authors and/or other copyright owners and it is a condition of accessing publications that users recognise and abide by the legal requirements associated with these rights.

- Users may download and print one copy of any publication from the public portal for the purpose of private study or research.
- You may not further distribute the material or use it for any profit-making activity or commercial gain
 You may freely distribute the URL identifying the publication in the public portal -

Take down policy

If you believe that this document breaches copyright please contact us at vbn@aub.aau.dk providing details, and we will remove access to the work immediately and investigate your claim.

A Review of Multilevel Converters with Parallel Connectivity

Jingyang Fang, Member, IEEE, Frede Blaabjerg, Fellow, IEEE, Steven Liu, Member, IEEE, and Stefan M. Goetz, Member, IEEE

Abstract-Cascaded-bridge converters (CBCs) and modular multilevel converters (MMCs) enjoy growing popularity mostly due to modularity and scalability. Conventionally, their submodules allow only serial and bypass operation so that the use of lowvoltage components for high-voltage output becomes possible. Dually, submodule parallelization adds switched-capacitor behavior to CBCs/MMCs and has witnessed an upward trend in recent years. Salient advantages of parallel operation comprise sensorless voltage balancing, capacitance saving, current sharing, and system efficiency optimization. To capture the advancement in the field, this article reviews state-of-the-art multilevel converters with parallel connectivity, covering various submodules, macro-level circuit topologies, implementation challenges and solutions, as well as control and optimization schemes. In particular, this article derives and classifies submodules as well as macro-level topologies according to basic H-bridge, asymmetrical half-bridge, and symmetrical half-bridge submodules. On top of that, this article introduces strategies for the simplification of submodules and creation of novel topologies vet maintaining parallel connectivity. We highlight the role of graph theory on creating new analytic and synthetic methodologies for multilevel converters. In addition, this article discloses the relationship between multilevel converters with parallel connectivity and switched capacitor converters.

Index terms—Capacitance saving, cascaded-bridge converter (CBC), modular multilevel converter (MMC), submodule parallelization, switched-capacitor converter, topology, voltage balance.

I. INTRODUCTION

Multilevel converters have become a preferred technology choice in high-voltage dc/ac transmissions [1–3], motor drives [4–6], renewable energy generation [7–9], energy storage systems [10–12], power quality enhancement equipment [13–15], modular solid-state transformers [16–18], special power supplies [19–21], high-power amplifiers [22–25], electric vehicles [26–28], and high-power chargers [29]. Multilevel converters outweigh their two-level counterparts in terms of semiconductor voltage ratings, power quality, passive filter size, electromagnetic interference noise, and system redundancy.

Manuscript received November 11, 2020; revised February 24, 2021; accepted April 09, 2021. This work was supported by the Alexander von Humboldt Foundation, KSB Foundation, the National Science Foundation under Grant No. 1608929, and the Duke Energy Research Seed Fund.

J. Fang and S. M. Goetz are with Duke University, Durham, NC 27710, USA (e-mails: jf274@duke.edu; stefan.goetz@duke.edu)

F. Blaabjerg is with the Department of Energy Technology, Aalborg University, Aalborg 9220, Denmark (e-mail: fbl@et.aau.dk).

S. Liu is with Technische Universitaet Kaiserslautern, Kaiserslautern, RP 67663. Germanv (e-mail: sliu@eit.uni-kl.de).

Cascaded-bridge (CBC), flying capacitor, and diode-clamped converters are three well-known multilevel converters [30–32]. Among them, CBCs stand out owing to their modularity and scalability and the avoidance of any additional diodes and high-voltage capacitors. Further, we obtain modular multilevel converters (MMCs) by employing CBCs in replacement of individual active switches in two-level converters [33]. To this end, MMCs inherit benefits from CBCs, as MMC arms consist of CBCs. The breadth and speed of technological changes in MMCs in the past two decades are unprecedented [34–39].

Despite with obvious advantages, conventional CBCs or MMCs only exploit a portion of their submodules for desirable voltage synthesis, while the remaining submodules are dynamically bypassed [30], [33]. However, bypassed submodules contribute nothing but conduction power losses [40]. Furthermore, although the serial cascading of submodules breaks the output voltage into smaller portions for all module components, the current does not scale: each module—no matter how many—has to conduct the entire arm current.

In addition, the imbalance of submodule capacitor voltages poses a serious threat to normal operation of CBCs and MMCs [41]. The mechanisms behind voltage imbalance often lie in the mismatch of charges and/or capacitances during certain periods [42]. Balancing is typically performed through circulating currents across the entire arm, which can add substantial losses in large systems [43], [44]. Especially, when supplying low-frequency voltages (e.g., for variable-speed motor drives), MMCs experience voltage drifts and hence significant submodule voltage imbalance [45]. As a straight-forward solution, the use of large module capacitances appears practically viable. However, the module capacitors are bulky and expensive components that often largely determine converter size, weight, and cost [46], [47]. As such, there is a strong motivation of capacitance reduction rather than a further increase [48]. On top of the aforesaid features, system efficiency stays a key aspect of power converters [42]. Therefore, the pursuit of higher efficiency through conduction- and/or switching-loss reduction remains a paramount goal [42], [49-52].

Multilevel converters with parallel connectivity can mitigate the challenges and drawbacks mentioned in the previous paragraph [27], [40]. Flexible and dynamic transitions between series and parallel connection of modules add new features to CBCs and MMCs, known from switched-capacitor converters, while maintaining their own advantages, such as multiple inputs and outputs as well as voltage sharing among submodules [53–55].

IEEE POWER ELECTRONICS REGULAR PAPER

As one way to enable parallelization without losing the advantage of low-voltage module components, a submodule can be tied to each of its neighboring submodules via two terminals. By proper activation of semiconductor switches, the bypassed submodules can now temporarily operate in parallel with active submodules [40], [56]. In many solutions for such parallelization, which will be elaborated further, several submodules can collectively share the arm current and thereby reduce conduction losses [27]. Moreover, dynamic parallelization can equalize submodule capacitor voltages, which is inherited as a feature intensively used in switched-capacitor converters [57-59]. As voltage equalization happens without the need of oversight, multilevel converters with parallel connectivity allow voltage balancing in a sensorless fashion [27], [40], [56], [60]. Hybrids of switched-capacitor and CBCs or MMCs allow compact converters with high reactive power capabilities and multilevel converters that can output ac down to 0 Hz, i.e., dc. The latter improves variable-speed motor drives, self-balancing or sensor consistency checking for safety-relevant systems, or dynamically reconfigurable battery systems, which in conventional CBCs suffer from pulsatile and reactive battery loads [61-69].

The removal of voltage sensors and the associated controllers can translate into significant improvements of system cost and reliability. Importantly, by providing an alternative way of voltage balancing, MMCs with serial and parallel connectivity (sometimes abbreviated as MMSPCs) can effectively mitigate voltage drifts in low-frequency applications, enabling the use of half-bridge MMCs even in dc microgrids [70]. Alternatively, the reduction of capacitor voltage ripple allows saving capacitance, such as in static compensator (STATCOM) applications, which in turn enables a further reduction of system cost and size [71]. Additionally, the added parallel states offer an extra control freedom for converter efficiency optimization [40]. Because of the aforementioned benefits, multilevel converters with various ways to introduce parallel connectivity have received increasing attention in recent years [27], [40], [56], [70–73].

However, the option of parallelization typically increases the number of individual semiconductor switches including their drivers, although in many topologies, the current rating per switch decreases on a similar level. For example, double-H-bridge submodules (namely, the H-bridge submodules that allow parallel connection) double the number of individual switches in multilevel converters [27]. A large quantity of active switches can increase complexity of hardware and control. As not all connectivity modes and degrees of freedom are necessary in each application, submodules can be simplified, and the semiconductor count reduced [45], [56], [72–75]. Despite tremendous growth of options, many submodules are application-specific without obvious relationships.

This article reviews state-of-the-art multilevel converters with parallel connectivity. In particular, we derive submodules and macro-level topologies from three basic submodules, viz. H-bridge, asymmetrical half-bridge, and symmetrical halfbridge submodules. On top of that, novel strategies for circuit simplification while maintaining some forms of parallel connectivity are included. Also, we present strategies for the creation of novel macro-topologies. Besides, the implementation challenges and solutions are covered. The remainder of this article is organized as follows. Section II presents basic submodules of conventional multilevel converters. Section III derives corresponding submodules for multilevel converters with parallel connectivity. Further, Section IV introduces the strategies for submodule simplification, particularly for a reduction of semiconductors. Section V focuses on macro-level converter topologies. Section VI concentrates on implementation issues and solutions. Section VII discusses control and optimization of multilevel converters with parallel connectivity. Finally, Section VIII provides concluding remarks.

II. BASIC SUBMODULES OF CONVENTIONAL MULTILEVEL CONVERTERS

This section introduces three basic submodules of conventional CBCs and MMCs, which serve as the origins of multilevel converters with parallel connectivity.

Fig. 1 illustrates the schematic diagrams of three basic submodules of conventional multilevel converters—H-bridge, asymmetrical half-bridge, and symmetrical half-bridge submodules [30], [33], [56]. As shown, each submodule consists of at least one energy storage element, such as capacitors, batteries, or any mix of them, as well as a plurality of semiconductor switches, including active switches, such as insulatedgate bipolar transistors (IGBTs) or field-effect transistors (FETs), and diodes. Current-source versions with unidirectionally conducting diode–transistor pairs or thyristors are rarer [76–79]. In conventional multilevel converters, submodules are connected in series for voltage sharing, thereby having two output terminals, each tied to one neighboring submodule [80–83].

As for H-bridge submodules [see Fig. 1(a)], the upper (S_{i1} or S_{i3}) and lower switches (S_{i2} or S_{i4}) typically operate complimentarily with dead times to avoid shoot through [70]. When diagonal switches S_{i1} and S_{i4} (or S_{i2} and S_{i3}) turn on/off synchronously, we expect either a positive or a negative voltage (denoted as ±1) from H-bridge submodules. Otherwise, the H-bridge submodule outputs a zero voltage (i.e., 0) given that its upper switches (or lower ones) turn on simultaneously. In consequence, H-bridge submodules allow bipolar voltage outputs and bypass operation. During normal operation, H-bridge submodules use two switches to conduct load currents.

Regarding asymmetrical half-bridge submodules shown in Fig. 1(b), the two switches (S_{i1} and S_{i2}) operate complimentarily [33], [83]. With S_{i1} on and S_{i2} off, asymmetrical half-bridge



(a) H-bridge (b) Asymmetrical half-bridge (c) Symmetrical half-bridgeFig. 1. Basic submodules of conventional multilevel converters.

IEEE POWER ELECTRONICS REGULAR PAPER

TABLE I. METRICS OF BASIC SUBMODULES.

| Metrics | H-bridge | Asym half-bridge | Sym half-bridge | |
|---------------------|------------|------------------|-----------------|--|
| Submodule count | п | n | n | |
| Switch count | 4 <i>n</i> | 2n | 2 <i>n</i> | |
| Cond. switch | 2 <i>n</i> | n | n | |
| Capacitor count | n | n | 2n | |
| Polarity | Bipolar | Unipolar | Bipolar | |
| Bypass operation | Yes | Yes | No | |
| Parallel connection | No | No | No | |
| Voltage levels | $\pm 1, 0$ | +1,0 | ±1 | |

submodules supply a positive voltage (+1). Alternatively, we obtain a zero voltage (0). As such, asymmetrical half-bridge submodules enable bypass operation yet only unipolar voltage outputs. Notably, unipolar voltage outputs prevent MMCs from operating during dc-side faults [81]. Besides, bipolar outputs are necessary for MMCs with certain macro-level topologies, such as H-bridges [82]. Nevertheless, asymmetrical half-bridge submodules save half of the switches compared to H-bridge submodules. Moreover, each asymmetrical half-bridge submodule carries the load current with only one switch, thus featuring lower conduction losses.

The symmetrical half-bridge submodule [see Fig. 1(c)] employs two switches and two energy storage elements [56], [71]. Upon S_{i1} on and S_{i2} off, symmetrical half-bridge submodules yield a positive voltage (+1) contributed by their upper capacitors. Alternatively, with S_{i1} off and S_{i2} on, symmetrical half-bridge submodules inversely output their lower capacitor voltages (-1). As a result, symmetrical half-bridge modules enable bipolar operation, yet without any bypass state. Additionally, the balance of upper and lower capacitor voltages becomes a special problem associated with symmetrical half-bridge submodules and converters [56], [84–87].

Table I summarizes the key metrics of basic submodules, including the numbers or counts of switches, conducting switches, and dc energy storage elements (such as capacitors) as well as polarity, bypass operation, voltage levels, and parallel connectivity. Such metrics disclose important features of submodules. Ideally, submodules should allow bipolar and bypass operation with a large amount of output voltage levels as well as minimized numbers of switches, conducting switches, and energy storage elements.

III. DERIVED SUBMODULES OF MULTILEVEL CONVERTERS WITH PARALLEL CONNECTIVITY

This section presents three major derived submodules of multilevel converters with parallel connectivity, which are modified from basic submodules introduced in the previous section. Submodules with local parallel connectivity are briefly discussed.

A. Submodules Derived from H-Bridge

Ilves et al. introduced a double H-bridge submodule (see Fig. 2) that allows local parallel connectivity between two



Fig. 2. Double H-bridge submodules of multilevel converters with local parallel connectivity.

capacitors, where two H-bridge circuits work collectively as one submodule [80]. As shown in Fig. 2(a), the positive module rail of one H-bridge and the negative module rail of the other act together as output terminals, while their switching nodes are connected. When corresponding diagonal switches S_{i11} , S_{i14} and S_{i21} , S_{i24} (or S_{i12} , S_{i13} and S_{i22} , S_{i23}) turn on synchronously, double H-bridge submodules give a positive voltage (+1) contributed by two parallelized dc capacitors C_{dcil} and C_{dci2} , as exemplified by Fig. 2(b). Additionally, we can bypass the first H-bridge by turning on its upper switches S_{i11} and S_{i13} . On the contrary, turning on the lower switches S_{i22} and S_{i24} bypasses the second H-bridge. Combining these two bypass modes, we bypass the entire submodule (0). Alternatively, double H-bridge submodules yield their highest output voltage-the sum of two serial capacitor voltages (+2)-with S_{i12} , S_{i14} , S_{i21} , and S_{i23} on. However, due to topology asymmetry, double H-bridge submodules cannot output negative voltages, thereby featuring unipolar operation [80]. Moreover, as each double H-bridge submodule ties to an adjacent submodule via only one terminal, parallelization is only possible within, but impossible across submodules. As such, the double H-bridge submodules in Fig. 2 only possess local parallel connectivity.

As a contemporaneously proposed alternative, a double-Hbridge submodule of multilevel converters with parallel connectivity is shown in Fig. 3, which consists of four switch pairs—eight switches, one energy storage element, and two pairs of output terminals (i.e., four terminals) [27]. One such submodule connects to its preceding or following submodule through a pair of (or two) output terminals instead of one as in conventional MMCs and CBCs. The pairwise module interconnection enables parallelization of several submodules such



Fig. 3. Double-H-bridge submodules of multilevel converters with parallel connectivity.

IEEE POWER ELECTRONICS REGULAR PAPER

that the switch utilization is still 50% and the blocking-voltage requirements for the modules' components do not increase.

Fig. 4 visualizes the six major operating states of double-Hbridge submodules, where only two adjacent submodules are shown for simplification [40]. Specifically, Figs. 4(a) and (b)



Fig. 4. Major operating states of double-H-bridge submodules.

demonstrate the positive (+2) and negative (-2) serial states, respectively. Notably, these two serial states are inherited from H-bridge submodules, except for single switches being replaced by two paralleled ones, leading to the reduction of conduction losses. In this case, the equivalent number of conducting switches is one. Additionally, Figs. 4(c) and (d) highlight the two parallel states. Under these conditions, two submodule capacitors are paralleled for voltage balancing and power loss reduction [27], [40]. Note that the maximum number of paralleled capacitors equals the number of double-H-bridge submodules, which is greater than two in general. Dependent on the states of remaining switches, either a positive (+1) or a negative (-1) voltage can be contributed by paralleled submodules. In addition, double-H-bridge submodules feature two bypass states, which give a zero voltage (0), as illustrated by Figs. 4(e) and (f). In short, double-H-bridge submodules allow bipolar, bypass, and parallel operation as well as large operating flexibility. The cost of flexibility is twice the number of individually controllable switches, though the utilization of switches is 50%. As the current can pass through two parallel transistors at each time, the total power rating of all semiconductor switches combined is exactly the same as that in conventional MMCs.

B. Submodules Derived from Asymmetrical Half-Bridge

By transplanting the same concept of parallelization into asymmetrical half-bridge submodules in Fig. 1(b), we obtain asymmetrical double-half-bridge submodules of multilevel converters with parallel connectivity, as shown in Fig. 5 [88], [89]. Here, we present two versions. Fig. 5(a) illustrates the unipolar positive version, which allows the two states of either a positive (+1) or a zero (0) output. In contrast, the negative version in Fig. 5(b) cannot yield positive voltages. Referring to Fig. 5, we notice that each asymmetrical double-half-bridge submodule comprises four switches and one energy storage element. Similar to double-H-bridge submodules, asymmetrical double-half-bridge submodules link neighbors via two terminals. Asymmetrical double half-bridge submodules with local parallel connectivity follow the fundamental principle in Fig. 2, and not detailed here [72].

Taking the positive version in Fig. 5(a) as an example, we present the major operating states of asymmetrical double-half-bridge submodules in Fig. 6 with two adjacent submodules included. Noticeably, the paralleled switches S_{i4} and $S_{(i+1)1}$ should switch together. Otherwise, turning on only one of them translates into increased power losses. As such, we can lump the two switches into one, as will further be discussed



Fig. 5. Asymmetrical double-half-bridge submodules of multilevel converters with parallel connectivity.





Fig. 6. Operating states of asymmetrical double-half-bridge submodules.

later on [70]. Fig. 6(a) illustrates the serial state of submodules with their diagonal switches S_{i1} , S_{i4} , $S_{(i+1)1}$, and $S_{(i+1)4}$ on. In this case, the submodules give their highest output voltage (+2) with 1.25 equivalent conducting switches (i.e., S_{i1} in series with shared S_{i4} // $S_{(i+1)1}$). Alternatively, by turning off the above-mentioned switches and turning on the remaining ones, we derive the only parallel state (+1) in Fig. 6(b). Obviously, at least two module capacitors are parallelized in this manner. Under another condition, Fig. 6(c) shows the bypass state, where S_{i3} and $S_{(i+1)3}$ switch on, leading to a zero output (0). In summary, asymmetrical double-half-bridge submodules enable parallel connectivity yet with unipolar voltage outputs.

C. Submodules Derived from Symmetrical Half-Bridge

Fig. 7 demonstrates symmetrical double-half-bridge submodules of multilevel converters with parallel connectivity [71]. As an extension of the symmetrical half-bridge submodule in Fig. 1(c), the symmetrical double-half-bridge submodule contains four switches, two energy storage elements, and four terminals. The addition of switches and terminals im-



Fig. 7. Symmetrical double-half-bridge submodules of multilevel converters with parallel connectivity.

proves symmetrical half-bridge submodules in terms of flexibility, reliability, and performance.

Fig. 8 illustrates the six major operating states of symmetrical double-half-bridge submodules, where two adjacent



Fig. 8. Operating states of symmetrical double-half-bridge submodules.

IEEE POWER ELECTRONICS REGULAR PAPER

TABLE II. METRICS OF DERIVED SUBMODULES.

| Metrics | H-bridge | Asym half-bridge | Sym half-bridge |
|---------------------|------------|------------------|-----------------|
| Submodule count | п | n | n |
| Switch count | 8 <i>n</i> | 4 <i>n</i> | 4 <i>n</i> |
| Cond. switch count | n | 1.25 <i>n</i> | 0.5 <i>n</i> |
| Capacitor count | n | n | 2 <i>n</i> |
| Polarity | Bipolar | Unipolar | Bipolar |
| Bypass operation | Yes | Yes | Yes |
| Parallel connection | Yes | Yes | Yes |
| Voltage levels | $\pm 1, 0$ | +1,0 | ±1,0 |

submodules are incorporated. It is observed from Figs. 8(a) and (b) that symmetrical double-half-bridge submodules inherit positive (+2) and negative (-2) serial states from conventional symmetrical half-bridge submodules. More importantly, the additional parallel states [see Figs. 8(c) and (d)] allow the parallelization of diagonal capacitors C_{dci2} and $C_{dc(i+1)1}$ (or C_{dci1} and $C_{dc(i+1)2}$), which in turn provides an elegant way of balancing voltages between upper and lower capacitors [71]. It should be emphasized that parallel and serial states may appear simultaneously, where diagonal switches turn on. As a result, parallel connectivity greatly saves on module capacitances in STATCOM applications [71], where multilevel converters compensate reactive power for voltage support [90]. Besides, symmetrical double-half-bridge submodules feature two bypass modes, as shown in Figs. 8(e) and (f). Notably, these bypass modes are excluded from conventional symmetrical half-bridge submodules [56].

Table II summarizes the key metrics of the submodules in Figs. 3, 5, and 7. As compared to Table I, the numbers of individual switches double, correspondingly. However, due to parallelization, the equivalent conduction switch count may even decrease. Parallelization improves the operating flexibility with more output voltage levels. It is possible to balance capacitor voltages and reduce voltage ripple in a sensorless way [27], [40]. Moreover, paralleled submodules share arm currents, resulting in the reduction of conduction power losses.

IV. SIMPLIFIED SUBMODULES OF MULTILEVEL CONVERTERS WITH PARALLEL CONNECTIVITY

This section presents strategies that reduce the number of active switches and simplify submodules of multilevel converters. The introduced strategies provide add-on benefits for the submodules introduced in the previous section.

A. Diodes as Replacement of Active Switches

In cases where unidirectional parallel connectivity is sufficient, we can replace some active switches, in combination with their drivers, by simpler diodes to save system cost and improve robustness.

Fig. 9(a) presents the schematic of double-H-bridge submodules with diodes, where one pair of active switches (i.e., S_{i7} and S_{i8}) is replaced by diodes. Notably, such replacement is not unique. Figs. 9(b) and (c) demonstrate the two parallel



Fig. 9. Double-H-bridge submodules with diodes.



Fig. 10. Asymmetrical modified-half-bridge submodules with reduced switch count and diodes.

states, which correspond to Figs. 4(c) and (d), respectively. However, parallelization occurs in a unidirectional pattern. To be specific, the capacitors C_{dci} and $C_{dc(i+1)}$ will be parallelized only when the voltage of $C_{dc(i+1)}$ is greater than that of C_{dci} , namely, $v_{dc(i+1)} > v_{dci}$. Therefore, the use of additional diodes simplifies the circuits at the expense of operation flexibility.

By generalization of the diode concept, Fig. 10 illustrates the asymmetrical modified-half-bridge submodules with parallel connectivity. As compared to Fig. 6, Fig. 10 first combines the two active switches S_{i4} and $S_{(i+1)1}$ into one single switch

 $S_{i4}/S_{(i+1)1}$ and then replaces the active switch S_{i3} by a diode. As a result, on the basis of the asymmetrical half-bridge topology shown in Fig. 1(b), each submodule uses only one additional diode to achieve parallelization, thereby greatly simplifying circuit hardware and control software [91]. However, the unidirectional property of diodes indicates that parallelization only happens when $v_{dc(i+1)} > v_{dci}$.

Similarly, Fig. 11 provides symmetrical double-half-bridge submodules with diodes, where two active switches (i.e., S_{i3} and S_{i4}) are replaced by diodes [56]. Once again, the parallel operation is unidirectional. Different from Figs. 9 and 10, it is worth noting that Fig. 11 involves different parallel capacitors $(C_{dci2}/C_{dc(i+1)1})$ or $C_{dci1}/C_{dc(i+1)2}$).

B. Removal of Redundant Active Switches

Returning to double-H-bridge submodules in Fig. 4, we note that two parallel states exist. Eliminating one redundant parallel state can reduce the number of active switches. For demonstration, Fig. 12 illustrates one asymmetrical modified-H-bridge submodule of multilevel converters with parallel connectivity [92]. It is clear from Fig. 12(a) that two active switches, along with their drivers and protection circuits, are removed. Fig. 12(b) represents the only remaining parallel state. Instead of positive module rails, the two interlinking active switches forming one bidirectional switch can likewise connect the negative module rails, although not shown here explicitly [92].

Fig. 13 illustrates the schematic of another set of asymmetrical modified-H-bridge submodules with two adjacent submodules [89], [93]. In this case, each submodule contains six



Fig. 11. Symmetrical double-half-bridge submodules with diodes.

active switches, similar to that in Fig. 12. Interestingly, the associated parallel state [see Fig. 14(b)] implies that parallelization is possible across submodules [93]. To be specific, keep the additional switches (i.e., S_{x5} and S_{x6}) on, the submodules that are not adjacent can also be connected in parallel, as long as their diagonal switches (e.g., S_{i1} , S_{i4} and $S_{(i+2)1}$, $S_{(i+2)4}$) remain on. The ability of parallelization across submodules enables a further improvement of system efficiency [89], [94]. However, submodules alternate in this case.

Fig. 14 demonstrates symmetrical modified-H-bridge submodules with reduced numbers of individual semiconductors. Clearly, each submodule comprises six active switches [89],



Fig. 12. Asymmetrical modified-H-bridge submodules with reduced switch count.



Fig. 13. Asymmetrical modified-H-bridge submodules with reduced switch count and parallel connectivity across submodules.

IEEE POWER ELECTRONICS REGULAR PAPER

[93]. As compared to Figs. 12 and 13, Fig. 14 achieves symmetry at the expense of higher conduction losses in serial states, where each symmetrical modified-H-bridge submodule features 2.5 equivalent conducting switches. By comparing Figs. 12(b) and 14(b), we find identical parallel states.

Further, we simplify the two paralleled switches S_{i5} and $S_{(i+1)2}$ into one single switch $S_{(i+1)2}$, resulting in a reduction of the number of switches, as shown in Fig. 15 [89], [93]. In this case, each modified-H-bridge submodule employs only one more active switch on the basis of conventional H-bridge to enable parallel connectivity. However, three switches must



(b) Parallel state

Fig. 14. Symmetrical modified-H-bridge submodules with reduced switch count.



Fig. 15. Simplified symmetrical modified-H-bridge submodules with reduced switch count.

simultaneously conduct in serial states to carry load currents.

C. Submodule Hybridization

An effective means of creating new multilevel converters with parallel connectivity and fewer active switches refers to hybridization. There are two levels of hybridization. First, we can obtain novel submodules through combinations of different parts of existing submodules. Second, we connect different submodules in a string to form novel CBCs or MMCs.

To illustrate the first way of hybridization, Fig. 16 presents a novel hybrid modified-H-bridge submodule that is contributed in part by the simplified symmetrical modified-H-bridge submodule (see Fig. 15) and partially by standard double-Hbridge submodules (see Fig. 3) [93], [95]. As expected, such hybrid submodules possess features of both predecessors. In terms of switch numbers, hybrid submodules reduce two switches as compared to standard double-H-bridge submodules but increase one compared to simplified symmetrical modified-H-bridge submodules. Speaking of conducting switches, two switches conduct load currents, which is a compromise between the two predecessors once again.

Fig. 17 demonstrates the second aspect of hybridization, where two different submodules—standard double-H-bridge and symmetrical double-half-bridge submodules are alternately connected in series, creating a novel hybrid multilevel converter with parallel connectivity, which so far has not been reported by any reference. Clearly, such hybridization reduces the average number of switches at the expense of modularity. In general, we can hybridize all the submodules (in Figs. 3–16) that allow parallel connection mentioned in this article. Table III summarizes the metrics of derived submodules with reduced switch numbers.

D. Modularization

The modularization, i.e., where to split a phase unit and how to group ideally identical units, has often been a relatively arbitrary process. Early CBCs and MMCs were drafted bottom-up by replicating known units, typically half- or Hbridges with capacitors [33], [96]. However, also a top-down



Fig. 16. Hybrid modified-H-bridge submodules



Fig. 17. Hybridization of double-H-bridge and symmetrical double-halfbridge submodules.

TABLE III. METRICS OF DERIVED SUBMODULES WITH REDUCED

 SWITCH NUMBERS.

| Metrics | Fig. 12 | Fig. 13 | Fig. 14 | Fig. 15 | Fig. 16 |
|---------------------|------------|------------|--------------|------------|------------|
| Submodule count | п | п | п | п | п |
| Switch count | 6n | 6n | 6 <i>n</i> | 5 <i>n</i> | 6 <i>n</i> |
| Cond. switch | 2n | 2n | 2.5 <i>n</i> | 3 <i>n</i> | 2n |
| Capacitor count | n | n | n | n | n |
| Polarity | Bipolar | Bipolar | Bipolar | Bipolar | Bipolar |
| Bypass operation | Yes | Yes | Yes | Yes | Yes |
| Parallel connection | Yes | Yes | Yes | Yes | Yes |
| Voltage levels | $\pm 1, 0$ | $\pm 1, 0$ | $\pm 1, 0$ | $\pm 1, 0$ | $\pm 1, 0$ |

modularization starting from the overall circuit is possible and shows that delimiters to form modules can be shifted relatively freely. Although, such redefinition of modules appears topologically and theoretically irrelevant, the modularization has large practical implications.

Most literature defines modules with storage element inside and a switched, practically ac interconnection to the outside [74]. These interconnections typically follow established halfbridge structures and entail the advantage that all low-side transistors of a module share the same source or emitter potential, which in turn allows to drive the gates of about half of the individual semiconductors of a module on the same potential. For topologies with a parallel mode, however, that can introduce timing constraints for switching for adjacent modules and lead to a seemingly high number of module states, e.g., all combinations of bridges left and right of the storage element.

Alternatively, the module state definition can be per interconnection unit between two energy storage elements, which comprises half-bridges from two neighboring modules according to the more conventional definition above [40]. This step uncovers the high redundancy in the state definition per bridge and reduces the number of required (interconnection) states drastically, from *m* to approximately \sqrt{m} [97]. All control operations, including modulation and module scheduling, can be performed in the interconnection space for simplification [88], [98]. If the state definition does not match the module definition, a mapping between both translates the control signals before they are sent to the modules; the first and the last bridges forming the outermost terminals of a module string can, though far apart, indeed be control-wise be united into one interconnection [88], [97].

The logical structure can also be used as the principle for modularization in hardware so that each interconnection between module energy storage elements is entirely inside a module [45]. The module terminals become dc, the module states coincide with the interconnection states, and any timing conditions are simpler within a module.

V. MACRO-LEVEL TOPOLOGIES OF MULTILEVEL CONVERTERS WITH PARALLEL CONNECTIVITY

The selection of the best submodule depends largely on the application and how they are assembled to larger structures as

the topologies of modules, thus the more macro-level topologies.

As an example, the overall structure might limit the load on some or all of its arms, i.e., typically strings of modules, to mere dc voltage, though often still providing bipolar ac output at the converter terminals; in consequence, modules in such macro-level topologies only have to operate on two quadrants and be unipolar. Furthermore, the macro-level topology determines the balancing paths and can allow parallel connectivity across arms.

We start to derive macro-level topologies on the basis of the three submodules mentioned in Section II. Next, we present several special macro-level topologies. In particular, we introduce two approaches of generating novel macro-level topologies. Finally, the role of graph theory on macro-level topologies is pointed out.

A. Macro-Level Topologies Derived from Basic Submodules

Before proceeding to detailed topology derivations, we first present fundamental multilevel converters with parallel connectivity, i.e., CBCs or MMC arms with parallel connectivity, as depicted in Fig. 18, where *n* identical submodules (denoted by $M_1, M_2, ..., M_n$) are connected in series, similar to conventional CBCs [30]. For selection of submodules, it should be remembered that submodules must allow bipolar operation in typical applications of CBCs, such as STATCOMs [99]. The connection point of converter terminals allows several variants detailed in Fig. 18.

Next, we proceed to show macro-level topologies from fundamental submodules in Fig. 1. Recapping Fig. 1(a), we obtain macro-level H-bridge MMCs with parallel connectivity by replacing either switches (with paralleled diodes) or capacitors by CBCs in Fig. 18, as detailed in Fig. 19 [100]. Note that we remove bus capacitors in the left part of Fig. 19 such that the topology becomes totally symmetrical. This follows the concept of conventional macro-level H-bridge MMCs [82]. In contrast, the right-hand-side schematic shows dc multilevel converters.

Fig. 20 presents macro-level asymmetrical half-bridge MMCs with parallel connectivity, which are derived from asymmetrical half-bridge submodules. Again, either switches or capacitors can be replaced by CBCs with parallel connectivity. Typically, macro-level asymmetrical half-bridge MMCs



Fig. 18. CBCs or MMC arms with parallel connectivity.

IEEE POWER ELECTRONICS REGULAR PAPER



Fig. 19. Macro-level H-bridge MMCs with parallel connectivity.

aim at dc-dc power conversion [75].

Fig. 21 illustrates macro-level symmetrical half-bridge MMCs with parallel connectivity. Remarkably, the corresponding MMC topologies without parallel connectivity have been widely used [101], [102]. One salient benefit of symmetrical half-bridge MMCs is that submodules with unipolar voltage outputs are still applicable, as voltage differences between upper and lower arms determine the eventual output.

B. Macro-Level Topologies Derived from Other Submodules

In addition to basic submodules, three-phase two-level converters can also serve as macro-level topologies. As a notable example, Fig. 22 presents macro-level three-phase MMCs with parallel connectivity, where either switches or bus capacitors of conventional three-phase two-level converters are replaced. The corresponding conventional MMCs have been extensively investigated [103–105].

Fig. 23 illustrates multilevel matrix converters with parallel connectivity, where bidirectional switches of matrix converters are replaced by CBCs. As known, matrix converters allow direct ac-ac power conversion without intermediate power stages [106]. Therefore, multilevel matrix converters enable direct high-voltage ac-ac power transfer [103].

Fig. 24 presents another interesting type of macro-level three-phase MMCs (defined as hexagonal MMCs) with paral-



Fig. 20. Macro-level asymmetrical half-bridge MMCs with parallel connectivity.



Fig. 21. Macro-level symmetrical half-bridge MMCs with parallel connectivity.

lel connectivity [103], [107]. Similar to multilevel matrix converters, hexagonal MMCs also enable direct ac–ac power conversion yet with a reduced number of arms and compromised control flexibility [107].

IEEE POWER ELECTRONICS REGULAR PAPER



Fig. 22. Macro-Level three-phase MMCs with parallel connectivity.



Fig. 23. Multilevel matrix converters with parallel connectivity.

Fig. 25 demonstrates a ring–star macro-level MMC with parallel connectivity [108]. Such MMCs are particularly suitable for poly-phase machine drives due to the decreasing phaseto-phase voltage, when phases are equivalently distributed along the ring [108]. Ring–star MMCs feature higher efficiency under light-load conditions due to parallel connectivity and desirable modulation indices. Moreover, the ring provides two mechanisms for flexible voltage balancing, specifically through capacitor parallelization and circulating currents.



Fig. 24. Hexagonal MMCs with parallel connectivity.

TABLE IV. METRICS OF MACRO-LEVEL TOPOLOGIES.

| MMC topologies | Arm count | Input | Output | Comments |
|----------------|-----------|-------|--------|------------|
| CBC | 1 | - | DC/AC | - |
| H-bridge MMC | 4 | DC/AC | DC/AC | - |
| HB (aym) MMC | 2 | DC | DC | +1 cap |
| HB (sym) MMC | 2 | DC | DC/AC | +2 caps |
| 3Φ MMC | 6 | DC | 3ФАС | - |
| Matrix MMC | 9 | 3ФАС | 3ФАС | - |
| Hexagonal MMC | 6 | 3ФАС | 3ΦAC | - |
| Ring-Star MMC | 6 | 3ФАС | 3ФАС | +6 modules |

In short, the majority of existing macro-level topologies of conventional MMCs are applicable to MMCs with parallel connectivity. Through the use of novel CBCs (see Fig. 18) as replacement of conventional CBCs, we achieve parallel connectivity of MMCs. Table IV summarizes the metrices of macro-level MMC topologies, including the arm count, input nature, output nature, and additional comments.

C. Creation of Novel Macro-Level Topologies

We have derived macro-level topologies based on single submodules/converters. In this subsection, we intend to create novel topologies through hybridization and nested structures.

Fig. 26 visualizes an example of macro-level hybridization, which consists of macro-level H-bridge and three-phase MMCs, both with parallel connectivity. Hybrid MMCs are

IEEE POWER ELECTRONICS REGULAR PAPER



Fig. 25. Ring-Star MMCs with parallel connectivity.



Fig. 26. Hybrid MMCs with parallel connectivity.

potential candidates for connecting two ac grids (e.g., a singlephase grid and a three-phase grid). In principle, we can parallel multiple MMCs, CHBs, or hybridize other macro-level topologies as long as their terminals match [142], [143].



Fig. 27. Matryoshka multilevel converters based on symmetrical double-halfbridge.

Another interesting way of creating novel converters lies in the idea of nesting. Nested topologies create converters, also sometimes called Matryoshka converters [100], with more than one layer. Specifically, each layer consists of several submodules, which further comprise more submodules from sub-layers. Fig. 27 provides novel Matryoshka multilevel converters on the basis of symmetrical double-half-bridge, where two top-layer symmetrical double-half-bridge submodules each incorporates a number of nested modules. Obviously, each top-layer submodule can be regarded as a macro-level MMC structure for the submodules in the second layer (represented as M_x), which may further be divided into more submodules [100]. Alternatively, nested modules can form the energy storage element of a nesting module while keeping discrete nesting-module transistors. Through nesting, macrolevel (or micro-level) topologies become relative concepts. Other examples of Matryoshka multilevel converters can be found in [100].

D. The Role of Graph Theory on Macro-Level Topologies

Graph theory is a valuable tool for the analysis and synthesis of macro-level topologies. For illustration, we provide an example to disclose the requirement of macro-level topologies on submodule voltage balancing via graph theory.

We begin the illustration with two simple ring MMCs shown in Fig. 28, where each MMC contains three submodules that allow parallel connectivity. In Fig. 28(a), the ring incorporates standard double-H-bridge submodules, thus allowing bidirectional voltage balancing. In contrast, the diodes in Fig. 28(b) only conduct in a unidirectional manner.



(b) Double-H-bridge submodules with diodes

Fig. 28. Two simple ring MMCs for voltage balance study.

Next, we simplify each submodule to a node and every pair of connection lines into an edge, leading to the graphs depicted in Fig. 29, where all the nodes and edges are sequentially numbered. Notably, Fig. 29(a) represents an undirected graph, where the edges without any arrow notation can be regarded as bidirectional edges. In contrast, Fig. 29(b) shows a directed graph with clearly marked arrows.

We define the graphs in Fig. 29 as the following triplets:

$$\mathbf{G}_{1} \triangleq \left(\mathbf{N}_{1}, \mathbf{E}_{1}, \mathbf{A}_{1}\right) \text{ and } \tag{1}$$

$$\mathbf{G}_2 \triangleq \left(\mathbf{N}_2, \mathbf{E}_2, \mathbf{A}_2 \right), \tag{2}$$

where N_1 and N_2 , E_1 and E_2 , A_1 and A_2 stand for the sets of nodes, sets of edges, and adjacency matrices, respectively [109]. According to Fig. 29, they are expressed as



(a) Standard double-H-bridge submodules



(b) Double-H-bridge submodules with diodes

Fig. 29. Graph representations of two ring MMCs for voltage balance study.

$$\mathbf{N}_1 = \mathbf{N}_2 = \{1, 2, 3\} . \tag{3}$$

$$\mathbf{E}_{1} = \{(1,2), (1,3), (2,1), (2,3), (3,1), (3,2)\}$$
(4)

 $\mathbf{E_2} = \{(1,2), (1,3), (2,3)\}$

$$\mathbf{A}_{1} = \begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{bmatrix} = \mathbf{A}_{1}^{\mathrm{T}}, \mathbf{A}_{2} = \begin{bmatrix} 0 & 1 & 1 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} \neq \mathbf{A}_{2}^{\mathrm{T}}.$$
 (5)

Notably, the elements of the edge sets E_1 and E_2 have two indices, which correspond to source and sink nodes, respectively. In addition, the adjacency matrices A_1 and A_2 have a one-to-one mapping to the edge sets E_1 and E_2 .

The prerequisite of random submodule voltage balance is that a (directed) path exists between every two nodes. Here, the path is defined as an ordered sequence of edges that links two nodes. For example, there are two paths from Node 1 to Node 3 in Fig. 29(b)—specifically {(1,3)} and {(1,2), (2,3)}. The existence of paths between every two nodes is equivalent to the (strong) connectivity of graphs, which can be judged by the irreducibility of adjacency matrices [110]. By definition, **A** is an irreducible matrix if and only if the sum matrix of \mathbf{A}^k (k = 0, 1, 2, ..., n-1) features all positive entries [110]. Specifically, \mathbf{A}_1 is irreducible, as

$$\sum_{k=0}^{2} \mathbf{A}_{1}^{k} = \begin{bmatrix} 3 & 2 & 2 \\ 2 & 3 & 2 \\ 2 & 2 & 3 \end{bmatrix}.$$
 (6)

Alternatively, A_2 is found to be reducible since it contains zero entries, as proved by

$$\sum_{k=0}^{2} \mathbf{A_{2}}^{k} = \begin{bmatrix} 1 & 1 & 2 \\ 0 & 1 & 1 \\ 0 & 0 & 1 \end{bmatrix}.$$
 (7)

Referring to Fig. 29(a), we observe that random voltage balance is possible. However, voltage balance from Node 2 (or 3) to Node 1 is impossible in Fig. 29(b).

The above example briefly demonstrates the role of graph theory on the analysis of MMC macro-level topologies for submodule voltage balance. In general, MMC macro-level topology analysis and synthesis through graph theory is a promising area.

VI. IMPLEMENTATION CHALLENGES AND SOLUTIONS

This section focuses on implementation challenges and solutions of multilevel converters with parallel connectivity. The section first points out similarities and differences between multilevel and switched-capacitor converters. Next, it analyzes parallelization dynamics and discloses challenges due to capacitor parallelization. Further, we analyze balancing energy losses. Finally, this section ends with strategies for current ripple suppression.

A. Switched-Capacitor Converters

As the name suggests, switched-capacitor converters refer to power converters mainly consisting of semiconductor

IEEE POWER ELECTRONICS REGULAR PAPER

switches and capacitors, typically without magnetic components, such as inductors. As compared to inductors, capacitors can allow higher power and energy densities, thereby enabling lower-power switched-capacitor converters to be implemented as integrated circuits (ICs) [69]. Similar to multilevel converters with parallel connectivity, switched-capacitor converters balance capacitor voltages and transfer energy through parallelization [53–55]. By alternation between serial and parallel states, switched-capacitor converters can achieve very steep step-up or step-down ratios [111], [112].

Notably, multilevel converters with parallel connectivity and switched-capacitor converters can share very similar topologies. For example, Fig. 30(a) shows a typical topology of switched-capacitor converters, where the converter submodule is essentially the asymmetrical modified-half-bridge submodule with a reduced switch count (see Figs. 5 and 10) [57]. As shown in Fig. 19(b), the parallel state equalizes several selected capacitor voltages (i.e., $v_{in} = v_{dci} = v_{dc(i+1)}$). On top of that, the serial state [see Fig. 19(c)] of switched-capacitor converters determines the remaining capacitor voltage(s) (i.e., $v_{out} =$ $v_{in} + v_{dci} + v_{dc(i+1)} = 3v_{in}$) [57].

Since the inputs and outputs of switched-capacitor converters are often capacitor voltages, whose relationships are fixed by serial and parallel states, switched-capacitor converters generally feature discrete (and sometimes unique) step-up or step-down ratios (e.g., 3 or 1/3). To achieve flexible voltage regulation, pulse-width modulation (PWM) can be transplanted into switched-capacitor converters [113]. However, the usability of PWM greatly depends on parasitic resistors and equivalent series resistances (ESRs) of capacitors. Another methodology uses additional components, such as inductors,



Fig. 30. Typical schematic and operation of switched-capacitor converters.

in switched-capacitor converters for voltage regulation [114]. In this case, switched-capacitor and conventional PWM converters overlap [115]. Along this direction, the combined operation of both modes is still under research [116], [117].

In contrast, multilevel converters with parallel connectivity typically select certain switching nodes (instead of capacitors), together with passive filters to smoothen current ripple, as inputs and outputs. As a result, flexible voltage regulation of multiple input/output ports can be expected, similar to conventional MMCs [81]. Various modulation schemes for flexible voltage regulation will be introduced in the next section.

As mentioned, both switched-capacitor and multilevel converters with parallel connectivity can achieve voltage balance via capacitor parallelization. They encounter common challenges, as voltage sources (such as ideal capacitors) with very different voltages should not be directly connected in parallel [118]. We will elaborate on this point through detailed analysis of parallelization dynamics.

B. Analysis of Parallelization Dynamics

In addition to paralleled capacitors, parasitic inductances, forward voltage drops, and equivalent resistances of semiconductors, capacitors, and cables determine parallelization dynamics [119]. For example, consider the case of two capacitors C_1 and C_2 for parallel connection in Fig. 31. As shown, v_{c1} and v_{c2} stand for the respective capacitor voltages. Elements v_{d12} , R_{12} , and L_{12} model the lumped voltage drop, resistance, and inductance, respectively; i_{12} denotes the current due to parallelization.

Parallelization dynamics are governed by the following differential equations of the serial *RLC* circuit

$$v_{c1}(t) = v_{c2}(t) + v_{d12} + R_{12}i_{12}(t) + L_{12}\frac{di_{12}(t)}{dt}$$
 and (8)

$$i_{12}(t) = -C_1 \frac{\mathrm{d}v_{c1}(t)}{\mathrm{d}t} = C_2 \frac{\mathrm{d}v_{c2}(t)}{\mathrm{d}t}, \qquad (9)$$

whose theoretical bases are Kirchhoff voltage and current laws, respectively [118].

Before parallelization, assume that

$$v_{c1}(0) = v_{c10}, v_{c2}(0) = v_{c20}.$$
 (10)

$$C_1 v_{c1}(t) + C_2 v_{c2}(t) = C_1 v_{c10} + C_2 v_{c20}.$$
(11)

In the steady state, the two capacitors share an identical voltage, namely,

$$v_{c1\infty} = v_{c2\infty} = \frac{C_1 v_{c10} + C_2 v_{c20}}{C_1 + C_2} \,. \tag{12}$$

Taking the derivative of (8), we obtain



Fig. 31. Equivalent circuit for analysis of parallelization dynamics.

IEEE POWER ELECTRONICS REGULAR PAPER

$$\frac{d^2 i_{12}(t)}{dt^2} + \frac{R_{12}}{L_{12}} \cdot \frac{d i_{12}(t)}{dt} + \frac{(C_1 + C_2)i_{12}(t)}{L_{12}C_1C_2} = 0.$$
(13)

The corresponding characteristic equation is

$$x^{2} + 2\zeta \omega_{0} x + \omega_{0}^{2} = 0, \qquad (14)$$

where

$$\omega_0 = \sqrt{\frac{(C_1 + C_2)}{L_{12}C_1C_2}} \text{ and } \zeta = \frac{R_{12}}{2} \sqrt{\frac{C_1C_2}{L_{12}(C_1 + C_2)}}$$
(15)

represent the natural angular frequency and damping factor, respectively. Alternatively, the damping factor can be quantified through

$$\alpha = \zeta \omega_0 = \frac{R_{12}}{2L_{12}} \,. \tag{16}$$

According to (14), we derive the two roots as

$$x_{1,2} = -\omega_0(\zeta \pm \sqrt{\zeta^2 - 1}) = -\alpha \pm \sqrt{\alpha^2 - \omega_0^2}.$$
 (17)

The nature of roots and parallelization dynamics depend on the damping factor [120]. Specifically, as known from other oscillators, three cases exist.

1) Overdamped Case ($\zeta > 1$)

In this case, the two roots are both real numbers. The current due to parallelization is

$$i_{12}(t) = A_1 e^{x_1 t} + A_2 e^{x_2 t}, \qquad (18)$$

where the coefficients are determined by the following initial conditions:

$$i_{12}(0) = 0, (19)$$

$$L_{12} \left. \frac{\mathrm{d}i_{12}(t)}{\mathrm{d}t} \right|_{t=0} = v_{c10} - v_{c20} - v_{d12} \,. \tag{20}$$

Substitution of (19) and (20) into (18) entails

$$i_{12}(t) = \frac{v_{c10} - v_{c20} - v_{d12}}{L_{12}(x_1 - x_2)} (e^{x_1 t} - e^{x_2 t}), \qquad (21)$$

which varies monotonically.

2) Critically Damped Case ($\zeta = 1$)

We expect two identical roots under this condition. Correspondingly, the current takes the form of

$$i_{12}(t) = B_1 t e^{-\alpha t} + B_2 e^{-\alpha t} .$$
(22)

Considering (19) and (20), we can rewrite the current as

$$\dot{t}_{12}(t) = \frac{v_{c10} - v_{c20} - v_{d12}}{L_{12}} t e^{-\alpha t} .$$
(23)

3) Underdamped Case ($\zeta < 1$)

In the underdamped case, the two roots are essentially one pair of conjugate roots, i.e.,

$$x_{1,2} = -\alpha \pm j\omega_{\rm d} \,, \tag{24}$$

where ω_d stands for the damped resonance frequency. Comparing (17) and (24), we can express ω_d as

$$\omega_{\rm d} = \sqrt{\omega_0^2 - \alpha^2} = \omega_0 \sqrt{1 - \zeta^2} , \qquad (25)$$

Accordingly, the current becomes

$$i_{12}(t) = I_0 e^{-\alpha t} \sin(\omega_d t + \theta) , \qquad (26)$$

where the unknown parameters can be derived from (19) and (20), leading to

$$i_{12}(t) = \frac{v_{c10} - v_{c20} - v_{d12}}{L_{12}\omega_{d}} e^{-\alpha t} \sin(\omega_{d} t) .$$
 (27)

So far, we have introduced the expressions of currents [see (21), (23), and (27)] due to parallelization. According to (9) and (27), we can derive capacitor voltages (in the underdamped case) through integration as [121]

$$v_{c1}(t) = v_{c10} - \frac{(v_{c10} - v_{c20})C_2}{C_1 + C_2} \left[1 - e^{-\alpha t} \left(\cos(\omega_d t) + \frac{\alpha}{\omega_d} \sin(\omega_d t) \right) \right], (28)$$
$$v_{c1}(t) = v_{c10} + \frac{(v_{c10} - v_{c20})C_1}{C_1 + C_2} \left[1 - e^{-\alpha t} \left(\cos(\omega_d t) + \frac{\alpha}{\omega_d} \sin(\omega_d t) \right) \right]. (29)$$

In addition, it is of significance to know the maximum current during parallelization. Let the derivative of (27) equal zero, it gives

$$\frac{\mathrm{d}i_{12}(t)}{\mathrm{d}t}\Big|_{t=t_{\mathrm{r}}} = 0 \Longrightarrow \theta_{\mathrm{r}} = \omega_{\mathrm{d}}t_{\mathrm{r}} = \arctan\left(\frac{1}{\alpha}\right) = \arctan\left(\frac{2L_{12}}{R_{12}}\right). (30)$$

Considering (30) and setting $t = t_r$ in (27), we obtain the current peak as

$$i_{12_{max}} = \frac{v_{c10} - v_{c20} - v_{d12}}{L_{12}\omega_{d}} e^{-\alpha\theta_{r}/\omega_{d}} \sin(\theta_{r}) .$$
(31)

Clearly, we can reduce the maximum current by reduction of the capacitor voltage difference ($v_{c10}-v_{c20}$) and/or increment of the voltage drop v_{d12} . Alternatively, increasing inductors helps significantly in ripple suppression, as visualized in Fig. 32 and analyzed in [119]. Analyses of currents in other cases are similar and hence excluded. Strategies for current mitigation will be introduced in the following subsections.

C. Analysis of Balancing Losses

As currents flow through resistors owing to parallelization, there will be energy losses associated with capacitor parallelization. Recapping (10), we express the initial energy that is stored in two capacitors as

$$E_0 = \frac{C_1 v_{c10}^2 + C_2 v_{c20}^2}{2}.$$
 (32)

In steady state, two capacitor voltages equalize as in (12). Their energies amount to

$$E_{\infty} = \frac{(C_1 v_{c10} + C_2 v_{c20})^2}{2(C_1 + C_2)}.$$
(33)



Fig. 32. The effect of inductors in suppression of currents due to parallelization.

IEEE POWER ELECTRONICS REGULAR PAPER

Subtracting (33) from (32), we derive the expression of energy losses as

$$E_{\rm loss} = E_0 - E_{\infty} = \frac{C_1 C_2 (v_{\rm c10} - v_{\rm c20})^2}{2(C_1 + C_2)}.$$
 (34)

Under the assumption of identical capacitances, (34) reduces to

$$E_{\rm loss} = \frac{C_{\rm l} \Delta v_{\rm c12}^{2}}{2} \,, \tag{35}$$

where $\Delta v_{c12} = v_{c10} - v_{c20}$.

Obviously, the energy loss due to parallelization E_{loss} increases quadratically with the increment of the voltage difference Δv_{c12} or linearly the capacitance C_1 . Furthermore, Δv_{c12} is a function of C_1 and the accumulated charge difference ΔQ_{c12} in a cycle of parallelization (e.g., a switching period) per

$$\Delta v_{c12} = \frac{\Delta Q_{c12}}{C_1} \le \frac{\Delta I_{c12_max} T_s}{C_1} , \qquad (36)$$

where $\Delta I_{c12_{max}}$ and T_s denote the maximum current difference and switching period, respectively. Substitution of (36) into (35) derives an upper limit of energy losses as

$$E_{\rm loss} \le \frac{\Delta I_{\rm c12_max}^2 T_{\rm s}^2}{2C_{\rm 1}} \,. \tag{37}$$

Interestingly, this first approximation is independent of the absolute module voltage. Equation (37) implies that fast switching (or reduced T_s) is key in reduction of parallelization energy losses [27]. Alternatively, we can reduce the maximum current difference (i.e., ΔI_{c12_max}) and energy losses through well-organized charging and discharging fashions [40].

In general, energy losses owing to parallelization are notably lower than those caused by conducting and switching of semiconductor switches. As an example, with $\Delta I_{c12_max} =$ 1000 A, $T_s = 10 \ \mu$ s, and $C_1 = 10 \ m$ F, the balancing loss of each submodule is calculated to be $E_{loss}/2 = 2.5 \ m$ J [27]. Assuming a moderate IGBT voltage drop of 1.5 V, the conduction loss per double-H-bridge submodule is found to be 60 mJ, which dwarfs the balancing loss by a factor of 24 [27]. Detailed loss analysis can be found in the literature [27] and [40].

D. Interlinking Inductors

As shown in Fig. 32, the increment of inductances reduces balancing currents. Therefore, inserting small filtering inductors between submodules, as demonstrated in Fig. 33(a), can effectively suppress surge currents [122–124]. For this purpose, a converter can split the large, concentrated, arm inductor of conventional MMCs into smaller portions and distribute those across the module interconnections [45], [88]. The overall arm inductance would largely stay the same [88], [122].

In the case of two interlinking inductors, they can further be coupled for different applications [88]. When two inductors are negatively coupled [see Fig. 33(b)], they strongly attenuate the balancing current i_{12} via an equivalent total inductance of [125]

$$L_{\rm mp} = L_{\rm m1} + L_{\rm m2} + k_{\rm m12} \sqrt{L_{\rm m1} L_{\rm m2}} , \qquad (38)$$

where k_{m12} represents the coupling coefficient. Meanwhile, the coupled inductors pose no threat to arm currents and normal



(b) Equivalent circuit of negatively-coupled inductors

*i*arm



(c) Equivalent circuit of positively-coupled inductors

Fig. 33. Double-H-bridge submodules with interlinking inductors. operation of MMCs [124]. In contrast, the positively-coupled inductors in Fig. 33(c) mainly attenuate the arm current i_{arm} .

Another benefit of employing inductors refers to the independent control of submodule voltages, which can differ from each other [122]. Referring to Fig. 33(a), a bidirectional dc–dc converter (i.e., a buck-cascaded-boost converter) emerges provided that S_{i6} and $S_{(i+1)4}$ (or S_{i5} and $S_{(i+1)3}$) turn on. In this case, we can regulate the voltages of C_{dci} and $C_{dc(i+1)}$ following the existing control methods of buck-boost converters [42]. With different submodule voltages, multilevel converters can yield more voltage levels with fewer submodules [122], [126].

Already with moderate switching, the inductors can be in the low microhenry range. Parasitic inductances of the module interconnections enhanced with ferrite cores have been demonstrated as effective [94].

VII. CONTROL AND OPTIMIZATION OF MULTILEVEL CONVERT-ERS WITH PARALLEL CONNECTIVITY

This section focuses on control and optimization of multilevel converters with parallel connectivity. The added parallel states not only greatly simply control architectures but also allow further system efficiency optimization.

A. Control and Modulation

Previous sections introduced various topologies of multilevel converters that allow parallel connectivity. Although

IEEE POWER ELECTRONICS REGULAR PAPER

fundamental for multilevel converters, topologies and related hardware cannot successfully operate unless with the help of dedicated controllers. As such, this section concentrates on software implementations, including control and modulation as well as efficiency optimization.

For multilevel converters (and also those with parallel connectivity), control is closely related to modulation. To differentiate them, we refer to control as the generation of total output voltage and current references, while modulators and sometimes separate schedulers quantize those continuous reference commands and determine the activation of individual switches. In general, we classify control and modulation schemes into two groups—PWM control of individual submodules at high-switching frequencies or at fundamental frequency, ideally with selective harmonic elimination [127].

Thanks to parallel charge exchange, PWM control is greatly simplified when applied to multilevel converters with parallel connectivity. This simplification is a result of dc voltage balancing that is achieved in a sensorless manner. Thus, once we regulate the dc voltage of a single submodule, all submodule dc voltages are successfully controlled.

Recapping Figs. 7 and 8, we take the multilevel converters based on symmetrical double-half-bridge submodules as an example to illustrate the control concept. Fig. 34 presents a controller for STATCOM applications, where the input reference signals $v_{dc ref}$ and $i_{q ref}$ are concerned with dc capacitor voltages and reactive current, respectively [71]. The grid voltage v_{grid} is measured and then passes through a phase-lockedloop (PLL), yielding the phase angle information $\sin \theta$ and $\cos \theta$. Moreover, $G_{PI}(s)$, $G_{PR}(s)$, $G_{Fil 1}(s)$, and $G_{Fil 2}(s)$ stand for the complex frequency domain transfer functions of proportional integral (PI) controllers, proportional resonant (PR) controllers, notch filters tuned to the 2nd harmonic, and those at the fundamental frequency, respectively. With parallel connectivity, Fig. 34 implies that controllers of multilevel converters become identical to those of conventional two-level converters, e.g., half-bridge controllers in [85-87], [128].

In Fig. 34, the output signals m_i (i = 1, 2, ..., n) are sent to PWM drivers. For illustration, Fig. 35 demonstrates a simple way of modulation, where the individual m_i are compared to carrier waveforms to generate the gate signals g_{Si}



Fig. 34. Controllers of multilevel converters based on symmetrical doublehalf-bridge submodules operating as STATCOMs [71].

(*i* = 1, 2, ..., *n*); the carriers can be phase-shifted for harmonic suppression [129]. Subsequently, g_{Si} produces g_{Si1} and g_{Si2} , which further drive the corresponding upper switch S_{i1} and lower switch S_{i2} in Fig. 7, respectively [71]. The gate signals g_{Si3} and g_{Si4} deserve attention, as they come from $g_{S(i+1)}$ of an adjacent submodule. As a result, diagonal switches turn on and off simultaneously given that dead times are ignored, leading to the parallel states shown in Figs. 8(c) and (d). The relevant simulation and experimental results can be found in [71].

Regarding fundamental frequency controllers, the only necessary adaptation for multilevel converters with parallel connectivity is in principle the replacement of some or all bypass states by parallel states [27]. However, the organization of parallel states can affect system efficiency, which will be discussed in the next subsection.

General concepts of existing control and modulation schemes of conventional multilevel converters remain valid in multilevel converters with parallel connectivity. Notable examples include but are not limited to space-vector PWM [130], direct torque control [131], model predictive control [132], reduced switching frequency modulation [133], circulating current control [103], fault-tolerant control [134], and virtual synchronous machine control [135–137]. In addition, multilevel converters with parallel connectivity also allow the delivery of grid-supportive services [138–141].

B. Efficiency Optimization

The sequence of parallel operation affects system efficiency of multilevel converters. Detailed optimization methodologies can be found in [27], [40]. In this subsection, we briefly introduce the fundamental idea behind efficiency optimization through reduction of parallel energy losses. For demonstration, Fig. 36 shows a multilevel converter with three exemplified submodules that can clear their voltage differences through parallelization. As revealed by (35), energy losses due to parallelization are quadratic functions of voltage differences. Referring to Fig. 36, we choose to parallelize the upper two submodules. This leads to equalized dc voltages and a total energy loss of 0.005 C₁ $v_{dc_ref}^2$ according to (35). Instead, if we first parallelize the lower two submodules and then parallelize them together with the first submodule, the resultant power



Fig. 35. Modulators of multilevel converters based on symmetrical modifiedhalf-bridge submodules [71].

IEEE POWER ELECTRONICS REGULAR PAPER



Fig. 36. Multilevel converters with three submodules illustrating efficiency optimization.

loss amounts to 0.0125 $C_1 v_{dc_ref}^2$, which exceeds that of the first case by a factor of 2.5. This example demonstrates the importance of balancing sequences.

VIII. CONCLUSIONS

This article provides a comprehensive review of multilevel converters with parallel connectivity. It begins with the introduction of three basic submodules-H-bridge, asymmetrical half-bridge, and symmetrical half-bridge submodules. Subsequently, we derive corresponding submodules for multilevel converters that allow parallel operation. Furthermore, we simplify such submodules via systematic techniques, including replacement of active switches by diodes, removal of active switches, and hybridization. These submodules can furthermore form various macro-level topologies of multilevel converters as reviewed. Novel macro-level topologies can emerge through hybridization and nested structures. In addition, the role of graph theory on macro-level topologies is pointed out. Further, implementation challenges and solutions related to parallel operation are detailed. Finally, we briefly review control and optimization strategies for multilevel converters with parallel connectivity. In general, the advance of power electronics promises parallelization an enabling technology for future multilevel converters.

REFERENCES

- N. Flourentzou, V. G. Agelidis, and G. D. Demetriades, "VSC-based HVDC power transmission systems: an overview," *IEEE Trans. Power Electron.*, vol. 24, no. 3, pp. 592–602, Mar. 2009.
- [2] S. Allebrod, R. Hamerski, and R. Marquardt, "New transformerless, scalable modular multilevel converters for HVDC-transmission," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 174-179.
- [3] B. Jacobson, P. Karlsson, G. Asplund, L. Harnefors, and T. Jonsson, "VSC-HVDC transmission with cascaded two-level converters," in *Proc. CIGRE*, Paris, France, 2010, paper B4-110.
- [4] J. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.
- [5] E. Cengelci, S. U. Sulistijo, B. O. Woom, P. Enjeti, R. Teodorescu, and F. Blaabjerg, "A new medium voltage PWM inverter topology for adjustable speed drives," in *Conf. Rec. IEEE-IAS Annu. Meeting*, St. Louis, MO, Oct. 1998, pp. 1416–1423.
- [6] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Applicat.*, vol. 37, pp. 611–618, Mar./Apr. 2001.

- [7] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a singlephase cascaded H-bridge multilevel inverter for grid-connected photovoltaic systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.
- [8] S. Daher, J. Schmid, and F. Antunes, "Multilevel inverter topologies for stand-alone PV systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 7, pp. 2703–2712, Jul. 2008.
- [9] H. Ertl, J. Kolar, and F. Zach, "A novel multicell DC–AC converter for applications in renewable energy systems," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1048–1057, Oct. 2002.
- [10] L. Zhang, Y. Tang, S. Yang, and F. Gao, "Decoupled power control for a modular-multilevel-converter-based hybrid AC–DC grid integrated with hybrid energy storage," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 2926-2934, Apr. 2019.
- [11] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "State-of-charge (SOC) balancing control of a battery energy storage system based on a cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628– 1636, Jun. 2009.
- [12] L. Maharjan, T. Yamagishi, and H. Akagi, "Active-power control of individual converter cells for a battery energy storage system based on a multilevel cascade PWM converter," *IEEE Trans. Power Electron.*, vol. 27, no. 3, pp. 1099–1107, Mar. 2012.
- [13] F. Z. Peng and J. Lai, "Dynamic performance and control of a static var generator using cascade multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.
- [14] F. Z. Peng, J. Lai, J. W. McKeever, and J. VanCoevering "A multilevel voltage–source inverter with separate dc sources for static var generation," *IEEE Trans. Ind. Appl.*, vol. 32, no. 5, pp. 1130–1138, Sep./Oct. 1996.
- [15] F. Z. Peng, Y. Liu, S. Yang, S. Zhang, D. Gunasekaran, and U. Karki, "Transformer-less unified power-flow controller using the cascade multilevel inverter," *IEEE Trans. Power Electron.*, vol. 31, no. 8, pp. 5461– 5472, Aug. 2016.
- [16] J. Shi, W. Gou, H. Yuan, T. Zhao, and A. Huang, "Research on voltage and power balance control for cascaded modular solid-state transformer," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1154–1166, Apr. 2011.
- [17] S. Falcones, X. Mao, and R. Ayyanar, "Topology comparison for solid state transformer implementation," in *Proc. PESGM*, Providence, RI, USA, 25–29 Jul. 2010.
- [18] M. A. Awal el al., "Modular medium voltage AC to low voltage DC converter for extreme fast charging applications." [Online]. Available: https://arxiv.org/abs/2007.04369
- [19] S. M. Goetz, M. Pfaeffl, J. Huber, M. Singer, R. Marquardt, and T. Weyh, "Circuit topology and control principle for a first magnetic stimulator with fully controllable waveform," in *Proc. IEEE Ann. Int. Conf. Eng. Med. Biol. Soc.*, 2012, pp. 4700–4703.
- [20] J. Won et al., "Auxiliary power supply for medium-voltage power converters: topology and control," *IEEE Trans. Ind. Appl.*, vol. 55, no. 4, pp. 4145–4156, Jul./Aug. 2019.
- [21] L. Yue, I. Lee, and X. Yao, "Tokamak vertical stability coil power supply based on modular multilevel converter," in *Proc. IPMHVC*, San Francisco, CA, USA, 6–9 Jul. 2016.
- [22] M. Vasic, et al., "Multilevel power supply for high-efficiency RF amplifiers," *IEEE Trans. Power Electron.*, vol. 25, no. 4, pp. 1078–1089, Apr. 2010.
- [23] G. S. Silva, R. C. Beltrame, L. Schuch, and C. Rech "Hybrid AC power source based on modular multilevel converter and linear amplifier," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 216–226, Jan. 2015.
- [24] E. Ledezma et al., "Development of a modular configurable multimegawatt power amplifier," in *Proc. IECON*, Vienna, Austria, 10–13 Nov. 2013.
- [25] C. Wang, P. Xing, L. Zhang, K. Wang, and Y. Li "A modular cascaded multilevel buck converter based on GaN devices designed for high power envelop elimination and restoration applications," in *Proc. ECCE*, Portland, OR, USA, 23–27 Sep. 2018.
- [26] A. Choudhury, P. Pillay, and S. S. Williamson, "Modified DC-bus voltage-balancing algorithm based three-level neutral-point-clamped IPMSM drive for electric vehicle applications," *IEEE Trans. Ind. Electron.*, vol. 63, no. 2, pp. 761–772, Feb. 2016.
- [27] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular multilevel converter with series and parallel submodule connectivity: topology and control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 203–215, Jan. 2015.

- [28] M. Quraan, T. Yeo, and P. Tricoli, "Design and control of modular multilevel converters for battery electric vehicles," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 507–517, Jan. 2016.
- [29] S. Rivera, B. Wu, S. Kouro, V. Yaramasu, and J. Wang, "Electric vehicle charging station using a neutral point clamped converter with bipolar DC bus," *IEEE Trans. Ind. Electron.*, vol. 62, no. 4, pp. 1999–2009, Apr. 2015.
- [30] R. H. Baker and L. H. Bannister, "Electric power converter," U.S. Patent 3 867 643, 1975.
- [31] T. A. Meynard and H. Foch, "Multi-level conversion: high voltage choppers and voltage-source inverters," in *Proc. IEEE Power Electron. Spec. Conf.*, 1992, pp. 397–403.
- [32] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518–523, Sep./Oct. 1981.
- [33] R. Marquardt and A. Lesnicar, "A new modular voltage source inverter topology," in *Conf. Rec. Eur. Conf. Power Electron. Appl.*, 2003, pp. 1– 10. [CD-ROM].
- [34] R. Marquardt, "Modular multilevel converters: state of the art and future progress," *IEEE Power Electron. Mag.*, vol. 5, no. 4, pp. 24–31, Dec. 2018.
- [35] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.
- [36] S. Kouro et al., "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.
- [37] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786–1817, Nov. 2009.
- [38] B. K. Bose, "Power electronics and motor drives recent progress and perspective," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 581–588, Feb. 2009.
- [39] B. Wu, *High-Power Converters and AC Drives*. Piscataway, NJ: IEEE Press, 2006.
- [40] S. M. Goetz, Z. Li, X. Liang, C. Zhang, S. M. Lukic, and A. V. Peterchev, "Control of modular multilevel converter with parallel connectivity application to battery systems," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8381–8392, Nov. 2017.
- [41] J. A. Barrena, L. Marroyo, M. A. R. Vidal, and J. R. T. Apraiz, "Individual voltage balancing strategy for PWM cascaded H-bridge converter-based STATCOM," *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 21–29, Jan. 2008.
- [42] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. New York, NY, USA: Springer, 2001.
- [43] R. Picas, J. Pou, S. Ceballos, V. G. Agelidis, and M. Saeedifard, "Minimization of the capacitor voltage fluctuations of a modular multilevel converter by circulating current control," in *Proc. IECON*, Montreal, QC, Canada, 25–28 Oct. 2012.
- [44] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 777–788, Feb. 2015.
- [45] Z. Li, R. Lizana, Z. Yu, S. Sha, A. V. Peterchev, and S. M. Goetz, "A modular multilevel series/parallel converter for a wide frequency range operation," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9854–9865, Oct. 2019.
- [46] Y. Tang, F. Blaabjerg, P. C. Loh, C. Jin, and P. Wang, "Decoupling of fluctuating power in single-phase systems through a symmetrical halfbridge circuit," *IEEE Trans. Power Electron.*, vol. 30, no. 4, pp. 1855– 1865, Apr. 2015.
- [47] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 29, no. 1, pp. 77–88, Jan. 2014.
- [48] G. Farivar, B. Hredzak, and V. G. Agelidis, "Reduced-capacitance thinfilm H-bridge multilevel STATCOM control utilizing an analytic filtering scheme," *IEEE Trans. Power Electron.*, vol. 62, no. 10, pp. 6457–6468, Oct. 2015.
- [49] J. W. Kolar, H. Ertl, and F. C. Zach "Influence of the modulation method on the conduction and switching losses of a PWM converter system," *IEEE Trans. Ind. Appl.*, vol. 27, no. 6, pp. 1063–1075, Nov./Dec. 1991.

- [50] H. Li, J. Fang, S. Chen, K. Wang, and Y. Tang, "Pulse density modulation for maximum efficiency point tracking of wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5492–5501, Jun. 2018.
- [51] E. Koutroulis, K. Kalaitzakis, N.C. Voulgaris, "Development of a microcontroller-based, photovoltaic maximum power point tracking control system," *IEEE Trans. Power Electron.*, vol. 16, no. 1, pp. 46–54, Jan. 2001.
- [52] Q. Zhao and F. C. Lee, "High-efficiency, high step-up dc-dc converters," *IEEE Trans. Power Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.
- [53] T. Umeno, K. Takahashi, I. Oota, F. Ueno, and T. Inoue, "New switchedcapacitor DC-DC converter with low input current ripple and its hybridization", in *Proceedings 33rd IEEE Midwest Symposium on Circuits and Systems*, Calgary, Canada, pp. 1091–1094, August 1990.
- [54] M. D. Seeman, V. W. Ng, H.-P. Le, M. John, E. Alon. and S. R. Sanders, "A comparative analysis of switched-capacitor and inductor-based DC-DC conversion technologies", in *Proc. IEEE COMPEL*, Boulder, CO, USA, 28–30 Jun. 2010.
- [55] S. R. Sanders, E. Alon, H.-P. Le, M. D. Seeman, M. John. and V. W. Ng, "The road to fully integrated DC–DC conversion via the switchedcapacitor approach," *IEEE Trans. Power Electron.*, vol. 28, no. 9, pp. 4146–4155, Sep. 2013.
- [56] J. Fang, Z. Li, and S. M. Goetz, "Multilevel converters with symmetrical half-bridge submodules and sensorless voltage balance," *IEEE Trans. Power Electron.*, vol. 36, no. 1, pp. 447–458, Jan. 2021.
- [57] M. S. Makowski and D. Maksimovic, "Performance limits of switchedcapacitor DC–DC converters," in *Proc. 26th Annu. IEEE Power Electron. Spec. Conf.*, Jun. 1995, vol. 2, pp. 1215–1221.
- [58] A. Ioinovici, "Switched-capacitor power electronics circuits," *IEEE Circuits Syst. Mag.*, vol. 1, no. 1, pp. 37–42, Jan. 2001.
- [59] F. Ueno, T. Inuoe, 1. Oota, and I. Harada, "Emergency power supply for small computer systems," *IEEE ISCAS*, 1991, pp. 1065–1068.
- [60] J. Xu, J. Li, J. Zhang, Lu Shi, X. Jia. and C. Zhao, "Open-loop voltage balancing algorithm for two-port full-bridge MMC-HVDC system," *International Journal of Electrical Power & Energy Systems*, vol. 109, pp. 259–268, Jul. 2019.
- [61] J. Xu, M. Feng, H. Liu, S. Li, X. Xiong, and C. Zhao, "The diodeclamped half-bridge MMC structure with internal spontaneous capacitor voltage parallel-balancing behaviors," *International Journal of Electrical Power & Energy Systems*, vol. 100, pp. 139–151, Sep. 2018.
- [62] N. Tashakor, M. Kilictas, E. Bagheri, and S. Goetz, "Modular multilevel converter with sensorless diode-clamped balancing through level-adjusted phase-shifted modulation," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7725–7735, Jul. 2021.
- [63] N. Tashakor, M. Kilictas, J. Fang, and S. M. Goetz, "Switch-clamped modular multilevel converters with sensorless voltage balancing control," *IEEE Trans. Ind. Electron.*, in press.
- [64] C. Terbrack, J. Stöttner, and C. Endisch, "Operation of an externally excited synchronous machine with a hybrid multilevel inverter," in *Proc. EPE*, Lyon, France, 7–11 Sept. 2020.
- [65] M. Vasiladiotis and A. Rufer, "Modular multilevel converters with integrated split battery energy storage," Lausanne, EPFL, Nov. 2014.
- [66] O. Theliander, A. Kersten, M. Kuder, W. Han, E. A. Grunditz, and T. Thiringer, "Battery modeling and parameter extraction for drive cycle loss evaluation of a modular battery system for vehicles based on a cascaded H-bridge multilevel inverter," *IEEE Trans. Ind. Appl.*, vol. 56, no. 6, pp. 6968–6977, Nov./Dec. 2020.
- [67] M. Vasiladiotis and A. Rufer, "Balancing control actions for cascaded Hbridge converters with integrated battery energy storage," in *Proc. EPE*, Lille, France, 2–6 Sept. 2013.
- [68] Z. Li, R. Lizana, S. M. Lukic, A. V. Peterchev, and S. M. Goetz, "Current injection methods for ripple-current suppression in delta-configured splitbattery energy storage," *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7411–7421, Aug. 2019.
- [69] Z. Li, R. Lizana, Z. Yu, S. Sha, A. V. Peterchev, and S. M. Goetz, "Modulation and control of series/parallel module for ripple-current reduction in star-configured split-battery applications," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 12977–12987, Dec. 2020.
- [70] R. Lizana et al., "Modular multilevel series/parallel converter for bipolar DC distribution and transmission," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 9, no. 2, pp. 1765–1779, Apr. 2021.

- [71] J. Fang, S. Yang, H. Wnag, N. Tashakor, and S. M. Goetz, "Reduction of MMC capacitances through parallelization of symmetrical half-bridge submodules," *IEEE Trans. Power Electron.*, in press.
- [72] K. Ilves, L. Bessegato, L. Harnefors, S. Norrga, and H.-P. Nee, "Semi-full bridge submodule for modular multilevel converters," in *Proc. 9th Int. Conf. Power Electronics and ECCE Asia*, 2015, pp. 1067–1074.
- [73] D. Gunasekaran, S. Yang, and F. Z. Peng, "A cascaded two port bridge multilevel converter with automatic voltage balancing capability," in *Proc. IEEE ECCE*, Montreal, QC, 2015, pp.3564-3569.
- [74] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18– 36, Jan. 2015.
- [75] K. K. Gupta, A. Ranjan, P. Bhatnagar, L. K. Sahu, and S. Jain, "Multilevel inverter topologies with reduced device count: a review," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 135–151, Jan. 2016.
- [76] M. A. Perez, R. Lizana, C. Azocar, J. Rodriguez, and B. Wu, "Modular multilevel cascaded converter based on current source H-bridges cells," in *Proc. IECON*, Montreal, QC, Canada, 25–28 Dec. 2012.
- [77] M. M. Bhesaniya and A. Shukla, "Current source modular multilevel converter: detailed analysis and STATCOM application," *IEEE Trans. Power Del.*, vol. 31, no. 1, pp. 323–333, Feb. 2016.
- [78] J. Liang, A. Nami, F. Dijkhuizen, P. Tenca, and J. Sastry, "Current source modular multilevel converter for HVDC and FACTS," in *Proc. EPE*, Lille, France, 2–6 Sep. 2013.
- [79] K. Gnanasambandam, A. K. Rathore, A. Edpuganti, D. Srinivasan, and J. Rodriguez, "Current-fed multilevel converters: an overview of circuit topologies, modulation techniques, and applications," *IEEE Trans. Power Electron.*, vol. 32, no. 5, pp. 3382–3401, Jun. 2017.
- [80] K. Ilves, F. Taffner, S. Norrga, A. Antonopoulos, L. Harnefors, and H. Nee, "A submodule implementation for parallel connection of capacitors in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3518–3527, Jul. 2015.
- [81] R. Marquardt, "Modular multilevel converter: an universal concept for HVDC-networks and extended DC-bus-applications," in *Proc. IEEE Int. Power Electronics Conf. (IPEC), Sapporo*, Japan, 2010, pp. 502–507.
- [82] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.
- [83] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (MMCC)," *IEEE Trans. Power Electron.*, vol. 26, no. 11, pp. 3119 – 3130, Nov. 2011.
- [84] J. Fang, G. Xiao, X. Yang, and Y. Tang, "Parameter design of a novel series-parallel-resonant *LCL* filter for single-phase half-bridge active power filters," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 200–217, Jan. 2017.
- [85] V. S. Cheung, R. S. Yeung, H. S. Chung, A. W. Lo, and W. Wu, "A transformer-less unified power quality conditioner with fast dynamic control," *IEEE Trans. Power Electron.*, vol. 33, no. 5, pp. 3926–3937, May 2018.
- [86] Y. Lo, C. Ho, and J. Wang, "Elimination of the output voltage imbalance in a half-bridge boost rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 4, pp. 1352–1360, Jul. 2007.
- [87] Y. Tang and F. Blaabjerg, "A component-minimized single-phase active power decoupling circuit with reduced current stress to semiconductor switches," *IEEE Trans. Power Electron.*, vol. 30, no. 6, pp. 2905–2910, Jun. 2015.
- [88] Z. Li, R. Lizana, S. Sha, Z. Yu, A. V. Peterchev, and S. M. Goetz, "Module implementation and modulation strategy for sensorless balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8405–8416, Sep. 2019.
- [89] T. Weyh and S. M. Goetz, "Multi-level converter topology with the possibility of dynamically connecting individual modules in series and in parallel," U.S. Patent 9 502 960, 2016.
- [90] R. C. Dugan, M. F. McGranaghan, S. Santoso, and H. W. Beaty, *Electrical Power Systems Quality*. McGraw-Hill, 2004, pp. 295–325.
- [91] X. Liu, J. Lv, C. Gao, Z. Chen, and S. Chen, "A novel STATCOM based on diode-clamped modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 32, no. 8, pp. 5964–5977, Aug. 2017.
- [92] S. M. Goetz, "Device and method for integrating an electrical element into an electrical circuit under load," U.S. Patent 10 014 611, 2018.
- [93] S. M. Goetz and T. Weyh, "Electrical converter system," U.S. Patent 9 496 799, 2016.

- [94] Z. Li, J. Motwani, Z. Zeng, S. M. Lukic, A. V. Peterchev, and S. M. Goetz, "A reduced series/parallel module for cascade multilevel static compensators supporting sensorless balancing," *IEEE Trans. Ind. Electron.*, vol. 68, no. 1, pp. 15–24, Jan. 2021.
- [95] S. M. Goetz, "Apparatus and method for an electric power supply with changeable electric connectivity between battery modules," U.S. Patent 10 442 309, 2019.
- [96] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A nonconventional power converter for plasma stabilization," *IEEE Trans. Power Electron.*, vol. 5, no. 2, pp. 212–219, Apr. 1990.
- [97] Z. Li, R. Lizana, A. V. Peterchev, and S. M. Goetz, "Distributed balancing control for modular multilevel series/parallel converter with capability of sensorless operation," in *Proc. ECCE*, Cincinnati, OH, USA, 1–5 Oct. 2017.
- [98] C. Wang, A. V. Peterchev, and S. M. Goetz, "Closed-loop predictively optimizing control for modular multilevel converter with parallel connectivity," in *Proc. EPE*, Genova, Italy, Italy, 3–5 Sep. 2019.
- [99] F. Z. Peng and J. Lai, "Dynamic performance and control of a static var generator using cascade multilevel inverters," *IEEE Trans. Ind. Appl.*, vol. 33, no. 3, pp. 748–755, May/Jun. 1997.
- [100] S. M. Goetz, "Matryoshka converter," U.S. Patent 10 439 506, 2019.
- [101] S. Yang, P. Wang, and Y. Tang, "Feedback linearization based current control strategy for modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 161–174, Jan. 2018.
- [102] S. Yang, J. Fang, Y. Tang, H. Qiu, C. Dong, and P. Wang, "Modular multilevel converter synthetic inertia-based frequency support for mediumvoltage microgrids," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8992–9002, Nov. 2019.
- [103] M. A. Perez, S. Bernet, J. Rodriguez, S. Koura, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.
- [104] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Trans. Power Electron.*, vol. 28, no. 8, pp. 3702–3713, Aug. 2013.
- [105] J. Qin and M. Saeedifard, "Reduced switching-frequency voltagebalancing strategies for modular multilevel HVDC converters," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2403–2410, Oct. 2013.
- [106] P. W. Wheeler, J. Rodríguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: a technology review," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 276–288, Apr. 2002.
- [107] L. Baruschka and A. Mertens, "A new three-phase AC/AC modular multilevel converter with six branches in hexagonal configuration," *IEEE Trans. Ind. Appl.*, vol. 49, no. 3, pp. 1400–1410, May/Jun. 2013.
- [108] S. M. Goetz, "Converter, electrical polyphase system and method for efficient power exchange," U.S. Patent 01 158 49, 2019.
- [109] F. Dorfler, J. W. Simpson-Porco, and F. Bullo, "Breaking the hierarchy: Distributed control & economic optimality in microgrids," *IEEE Transactions on Control of Network Systems*, vol.3, no. 3, pp. 241–253, 2016
- [110] F. Dorfler, J. W. Simpson-Porco, and F. Bullo, "Electrical networks and algebraic graphtheory: Models, properties, and applications," *Proceedings of the IEEE*, vol. 106, no. 5, pp. 977–1005, 2018.
- [111] Abutbul, A. Gherlitz, Y. Berkovich, and A. Ioinovici, "Step-up switchingmode converter with high voltage gain using a switched-capacitor circuit," *IEEE Trans. Syst. I, Fundam. Theory Appl.*, vol. 50, no. 8, pp. 1098–1102, Aug. 2003.
- [112] R. D. Middlebrook, "Transformerless dc-to-dc converters with large conversion ratios," *IEEE Trans. Power Electron.*, vol. 3, no. 4, pp. 484– 488, Oct. 1988.
- [113] S. V. Cheong, S. H. Chung, and A. Ioinovici, "Development of power electronics converters based on switched-capacitor circuits," in *Proc. IEEE Int. Symp. Circuits Systs.*(ISCAS'92), San Diego, pp. 1907-1910, May 1992.
- [114] T. Umeno, K. Takahashi, F. Ueno, T. Inoue, and I. Oota, "A new approach to low ripple-noise switching converters on the basis of switched- capacitor converters," in *Proc. IEEE Int. Symp. Circuits Systems*, Jun. 1991, pp. 1077–1080.
- [115] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched-capacitor/ switched-inductor structures for getting transformerless hybrid DC-DC PWM converters," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 55, no. 2, pp. 687–696, Mar. 2008.

IEEE POWER ELECTRONICS REGULAR PAPER

- [116] T. Liang, S. Chen, L. Yang, J. Chen, and A. Ioinovici, "Ultra-large gain step-up switched-capacitor DC-DC converter with coupled inductor for alternative sources of energy," *IEEE Trans. Circuits Syst. I, Regular Papers*, vol. 59, no. 4, pp. 864–874, Apr. 2012.
- [117] H. Chung and Y. K. Mok, "Development of a switched-capacitor DC-DC boost converter with continuous input current waveform," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 46, no. 6, pp. 756–759, Jun. 1999.
- [118] J. W. Nilsson and S. A. Riedel, *Electric circuits (10th edition)*. New Jersey, NJ, USA: Prentice Hall, 2015.
- [119] S. Heinig et al., "Implications of capacitor voltage imbalance on the operation of the semi-full-bridge submodule," *IEEE Trans. Power Electron.*, vol. 34, no. 10, pp. 9520–9535, Oct. 2019.
- [120] I. Oota, N. Hara, and F. Ueno, "Influence of parasitic inductance on serial fixed type switched-capacitor transformer," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 5, 1999, pp. 214–217.
- [121] S. Heinig, K. Jacobs, K. Ilves, S. Norrga, and H.-P. Nee, "Implications of capacitor voltage imbalance on the operation of the semi-full-bridge submodule," in *Proc. 19th Eur. Conf. Power Electron. Appl.*, Warsaw, Poland, Sep. 2017, pp. 1–10.
- [122] R. Lizana, S. Rivera, Z. Li, J. Luo, A. V. Peterchev, and S. M. Goetz, "Modular multilevel series/parallel converter with switched-inductor energy transfer between modules," *IEEE Trans. Power Electron.*, vol. 34, no. 5, pp. 4844–4852, May 2019.
- [123] J. Xu, J. Zhang, J. Li, L. Shi, X. Jia, and C. Zhao, "Series-parallel HBSM and two-port FBSM based hybrid MMC with local capacitor voltage selfbalancing capability," *International Journal of Electrical Power & Ener*gy Systems., vol. 103, pp. 203–211, Dec. 2018.
- [124] K. Ilves, Y. Okazaki, N. Chen, M. Nawaz, and A. Antonopoulos, "Capacitor voltage balancing in semi-full-bridge submodule with differentialmode choke," in *Proc. IPEC-Niigata 2018*, 2018, pp. 2335–2342.
- [125] J. Fang, H. Li, and Y. Tang, "A magnetic integrated *LLCL* filter for gridconnected voltage-source converters," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1725–1730, Mar. 2017.
- [126] M. D. Manjrekar, P. K. Steimer, and T. A. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 17, no. 5, pp. 518–523, Sep./Oct. 1981.
- [127] J. Rodriguez, J. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [128] J. Park, J. Kim, S. Park, and K. Kang, "DC voltage balancing control of half-bridge PWM inverter for linear compressor," in *Proc. IEEE Power Electronics for Distributed Generation Systems (PEDG)*, 2012, pp. 598– 602.
- [129] D. G. Holmes and T. A. Lipo, Pulse width modulation for power converters: principles and practive. Hoboken, NJ: Wiley, 2003.
- [130] N. Celanovic and D. Boroyevich, "A comprehensive study of neutralpoint voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Power Electron.*, vol. 15, no. 2, pp. 242–249, Mar. 2000.
- [131] E. Specht, C. Aschauer, C. Korte, and S. Goetz, "Direct torque control with variable level discretization for automotive drives," in *Proc. PCIM*, Nuremberg, Germany, 16–18 May 2017.
- [132] J. Rodriguez et al., "Predictive current control of a voltage source inverter," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 495–503, Feb. 2007.
- [133] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE Trans. Power Del.*, vol. 28, no. 4, pp. 2403–2410, Oct. 2013.
- [134] S. Shao, P. Wheeler, J. Clare, and A. Watson, "Fault detection for modular multilevel converters based on sliding mode observer," *IEEE Trans. Power Electron.*, vol. 28, no. 11, pp. 4867–4872, Nov. 2013.
- [135] H.-P. Beck and R. Hesse, "Virtual synchronous machine," in *Proc. 9th Int. Conf. Elect. Power Quality Utilisation*, Barcelona, Spain, Oct. 2007, pp. 1–6.
- [136] M. Guan, W. Pan, J. Zhang, Q. Hao, J. Cheng, and X. Zheng, "Synchronous generator emulation control strategy for voltage source converter (VSC) stations," *IEEE Trans. Power Syst.*, vol. 30, no. 6, pp. 3093–3101, Nov. 2015.
- [137] J. Fang, Y. Tang, H. Li, and X. Li, "A battery/ultracapacitor hybrid energy storage system for implementing the power management of virtual synchronous generators," *IEEE Trans. Power Electron.*, vol. 33, no. 4, pp. 2820–2824, Apr. 2018.

- [138] S. Yang, J. Fang, Y. Tang, and P. Wang, "Synthetic-inertia-based modular multilevel converter frequency control for improved micro-grid frequency regulation," in *Proc. IEEE ECCE*, Portland, Oregon, USA, 23–27 Sep. 2018.
- [139] J. Fang, H. Li, Y. Tang, and F. Blaabjerg, "On the inertia of future moreelectronics power systems," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 7, no. 4, pp. 2130–2146, Dec. 2019.
- [140] H. Deng, J. Fang, Jiale Yu, V. Debusschere, and Y. Tang, "Small-signal modeling, stability analysis, and controller design of grid-friendly power converters with virtual inertia and grid-forming capability," in *Proc. IEEE ECCE*, Baltimore, MD, USA, 29 Sep.–3 Oct. 2019.
- [141] J. Fang, H. Li, Y. Tang, and F. Blaabjerg, "Distributed power system virtual inertia implemented by grid-connected power converters," *IEEE Trans. Power Electron.*, vol. 33, no. 10, pp. 8488–8499, Oct. 2018.
- [142] S. Milovanovic and D. Dujic, "On facilitating the modular multilevel converter power scalability through branch paralleling," in *Proc. IEEE ECCE*, 2019, pp. 6875–6882.
- [143] S. Milovanovic and D. Dujic, "On power scalability of modular multilevel converters: increasing current ratings through branch paralleling," *IEEE Power Electron. Mag.*, vol. 7, no. 2, pp. 53–63, Jun. 2020.



Jingyang Fang (S'15–M'19) received the B.Sc. and M.Sc. degrees in electrical engineering from Xi'an Jiaotong University, Xi'an, China, in 2013 and 2015, respectively, and the Ph.D. degree from School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, in 2019.

From May 2018 to August 2018, he was a Visiting Scholar with the Institute of Energy Technology, Aalborg University, Aalborg, Denmark. From August 2018 to August 2019, he was a Research Fel-

low with the School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore. Since August 2019, he joined Duke University and TU Kaiserslautern as a postdoctoral fellow. His research interests include power quality control, stability analysis and improvement, renewable energy integration, and digital control in more-electronics power systems.

Dr. Fang is a recipient of the Humboldt Research Fellowship, two IEEE Prize Paper Awards, and one Best Presenter Award. He received the Chinese Government Award for Outstanding Self-Financed Students Abroad in 2018 and the Best Thesis Award from NTU in 2019.



Frede Blaabjerg (S'86–M'88–SM'97–F'03) was with ABB-Scandia, Randers, Denmark, from 1987 to 1988. From 1988 to 1992, he got the PhD degree in Electrical Engineering at Aalborg University in 1995. He became an Assistant Professor in 1992, an Associate Professor in 1996, and a Full Professor of power electronics and drives in 1998. From 2017 he became a Villum Investigator. He is honoris causa at University Politehnica Timisoara (UPT), Romania and Tallinn Technical University (TTU) in Estonia.

His current research interests include power electronics and its applications such as in wind turbines, PV systems, reliability, harmonics and adjustable speed drives. He has published more than 600 journal papers in the fields of power electronics and its applications. He is the co-author of four monographs and editor of ten books in power electronics and its applications.

He has received 33 IEEE Prize Paper Awards, the IEEE PELS Distinguished Service Award in 2009, the EPE-PEMC Council Award in 2010, the IEEE William E. Newell Power Electronics Award 2014, the Villum Kann Rasmussen Research Award 2014, the Global Energy Prize in 2019 and the 2020 IEEE Edison Medal. He was the Editor-in-Chief of the IEEE TRANS-ACTIONS ON POWER ELECTRONICS from 2006 to 2012. He has been Distinguished Lecturer for the IEEE Power Electronics Society from 2005 to 2007 and for the IEEE Industry Applications Society from 2010 to 2011 as well as 2017 to 2018. In 2019-2020 he served as a President of IEEE Power

IEEE POWER ELECTRONICS REGULAR PAPER

Electronics Society. He has been Vice-President of the Danish Academy of Technical Sciences.

He is nominated in 2014-2020 by Thomson Reuters to be between the 250 most cited researchers in Engineering in the world.



Steven Liu (M'03) received the Dipl.-Ing. and Dr.-Ing. degrees from Technische Universität Berlin, Berlin, Germany, in 1986 and 1992, respectively.

He worked with AEG, Berlin, Germany, DaimlerBenz Research, Berlin, Germany, and Harz University of Applied Studies and Research before joining the Technische Universität Kaiserslautern, Kaiserslautern, Germany, as a Full Professor in 2004. His current research interests include control of mechatronic and power systems, robotics, networked

control, and model-based fault diagnosis.



Stefan M. Goetz (M'14) received his undergraduate and graduate degrees from TU Muenchen, Germany. He obtained doctoral training at TU Muenchen as well as Columbia University and received the PhD degree in 2012 with a thesis on medical applications of power electronics for which he was awarded a PhD thesis prize from TU Muenchen. His research interests include multilevel converters, high-quality power electronics, precise high-power pulse synthesizers for magnetic neurostimulation and noninvasive

brain stimulation as well as integrative power electronics solutions for microgrids and electric vehicle applications.