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A Novel Full Soft-Switching High Gain DC/DC Converter Based on Three-Winding Coupled-Inductor

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***Abstract*—In this paper, a new non-isolated full soft-switching step-up DC/DC converter is introduced with a continuous input current for renewable energy applications. The use of a Three-Winding Coupled-Inductor (TWCI) along with a Voltage Multiplier (VM), enables the proposed converter to enhance the voltage gain with lower turns ratios and duty cycles. Also, a lossless regenerative passive clamp circuit is employed to limit the voltage stress across the power switch. In addition to Zero Current Switching (ZCS) performance at the turn-on instant of the power switch, the turn-off current value is also alleviated by adopting a Quasi-Resonance (QR) operation between the leakage inductor of the TWCI and middle capacitors. Moreover, the current of all diodes reaches zero with a slow slew rate, which leads to the elimination of the reverse recovery problem in the converter. Soft-switching of the power switch and all the diodes in the proposed converter significantly reduces the switching power dissipations. Therefore, the presented converter can provide a high voltage gain ratio with high efficiency. Steady-state analysis, comprehensive comparisons with other related converters, and design considerations are discussed in detail. Finally, a 160 W prototype with 200 V output voltage is demonstrated to justify the theoretical analysis.**

I. INTRODUCTION

In recent years, the use of step-up DC/DC converters with a high voltage gain ratio has been increased dramatically. The main applications of these converters are in Renewable Energy Sources (RES) such as Fuel Cells (FCs), Photovoltaic (PV) cells, and wind turbines. Moreover, step-up converters also play an essential role in many industrial applications such as automobiles, electric traction, robotics, satellite, data centers, street lighting, and some medical equipment. In such applications, step-up converters as an interfacing circuit convert the input low-level input (typically <50 V) to the desired regulated high output voltage (e.g. to a 400 V DC-bus). There are some critical requirements such as application, including high voltage gain, low voltage stress, high efficiency, and continuous input current [1]. For low power applications where electrical isolation is not mandatory for the power processing stage, the non-isolated structure of such converters with small volumes and low cost is much more desirable than the isolated ones [2].

Theoretically, the conventional step-up converters, such as boost converter with a simple structure, can provide a high voltage gain at extremely large duty cycles. However, in practice, high voltage stress across the main power switch along with considerable diode reverse recovery loss force the voltage gain to be limited to lower than 5 [3]. Due to the mentioned drawbacks, modifying the configuration of conventional step-up converters to improve the performance key indicators is imperative. For this purpose, to achieve higher voltage gain with reasonable duty cycles, some voltage boosting strategies such as voltage lift, Voltage Multipliers (VMs), Switched Capacitors (SCs), Switched Inductors (SIs), and also Cascading Techniques (CTs) are used in the classical step-up converters [2, 3]. Although most of these modified converters can offer a high voltage gain, operating in a hard-switching condition and using a large number of passive components limit their performance [3, 4].

In recent years, magnetic components in the form of Coupled-Inductors (CI) are broadly employed in different configurations of step-up converters. A wide range of voltage gain can be achieved in these converters by adjusting the winding turn's ratio of the CI [3]. However, many CI-based converters suffer from the effect of leakage inductance that causes voltage spikes over the switching devices, which leads to reduced efficiency. To recover this drawback, active or passive clamp networks can be used [5]. Additionally, to further enhance the voltage gain along with maintaining high efficiency the use of other mentioned voltage boosting strategies (VM, SC/SI, and CT) in CI-based DC-DC converters is becoming more popular [6, 7]. It is noteworthy that high voltage stresses, hard-switching performance, and the diode reverse recovery problem compromise the conversion efficiency in high step-up converters. To overcome these drawbacks, employing the resonant tank in step-up converters is more profitable [8-11].

In recent years, some non-isolated modified DC-DC structures of step-up converters based on CI with proper performance have been presented. In the CI-based step-up converters presented in [12-14], VMs are used in the form of voltage rectifier, and hence the voltage conversion is increased significantly. Even though an ultra-high voltage gain under soft-switching operation is obtained, these converters suffer from a high input current ripple. Moreover, new types of single-switch step-up converters with regenerative passive clamp circuits are presented in [15-19]. In these converters, the main power switch is driven under ZCS condition and low voltage stress. Besides, the CI's leakage inductor helps to alleviate the reverse recovery problem of the diodes. However,

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the mentioned converters cannot offer a wide range of voltage gain. Also, several types of SEPIC-based converters with continuous input current and high efficiency are presented in [8], [9], [20-21]. In these converters, a quasi-resonant (QR) performance along with soft-switching operation is obtained without any additional auxiliary components, which leads to a significant loss reduction related to the switching devices (i.e. MOSFETs and diodes). However, limitation in voltage gain ratio is the most important limitation of these converters. Furthermore, a semi-quadratic step-up DC-DC converter with a high voltage gain is presented in [22]. In this converter, an ultra-high voltage gain is obtained based on a cascaded connection of boost and buck-boost converters. Using two active switches along with the lack of soft-switching performance are two main drawbacks of this converter. Using a Three Winding CI (TWCI), an ultra-voltage gain is achieved in [23-27] as a function of three degrees of freedom, including duty cycle, secondary and tertiary windings turn ratios. Thus, the capability of voltage gain adjustment in a wider range is increased significantly. Nevertheless, in these converters, the use of TWCI at the input in series with DC voltage source creates a large input current ripple, which limits their performance in the RES applications. To solve this problem, three TWCI-based step-up converters with high voltage gain and continuous input current are suggested in [28-30]. In these converters, using a simple passive clamp circuit (consisting of a diode and a capacitor), the leakage energy of the TWCI is recycled. Moreover, the leakage inductor help to alleviate the reverse recovery loss of the converters. However, the limitation in obtaining high voltage gain at low turn ratios is the most important drawback of these converters.

In this paper, a new structure of a quasi-resonant high gain DC-DC converter based on TWCI with high efficiency is proposed with a simple structure and low implementation cost. The outstanding features of the presented single switch topology are high voltage gain without using high turn ratios on the TWCI, low input current ripple, low voltage stress along with soft-switching performance for all switching components. Using the VM cells and TWCI allows the proposed converter to reach an ultra-high voltage gain ratio at a low range of turns ratios and duty cycles. In the proposed converter, the power switch turns on under the ZCS condition. Also, employing a QR performance using a resonant tank created by the leakage inductance an auxiliary capacitor helps to decrease the switch turn-off current value, thereby minimize the turn-off power dissipation. Moreover, the leakage inductor of the TWCI is used to cause a ZCS condition at the turn-off instant for all diodes, which alleviates the reverse recovery problem.

The remainder of this paper is organized as follows. The operating modes and steady-state analysis of the proposed converter are described in Sections *II* and *III*. A performance comparison is given in Section *IV*. Section *V* provides the design procedure of the key elements. Experimental results from laboratory prototype and discussions are done in section *VII*. Finally, the conclusions are presented in Section *VIII*.

II. Circuit Description of the Proposed Converter

The equivalent circuit of the proposed converter is shown in Fig. 1. This converter is composed of a TWCI, a single power switch (*S*), an input inductor (L_{in}), four diodes, and five capacitors. The turns of the primary, secondary, and third windings of the TWCI are N_1, N_2, and N_3, respectively. Also, L_k is the total leakage inductance of the TWCI reflected on the primary side. Combining the three sides of the TWCI and capacitors C_1, C_2, C_3, and C_c, along with diodes D_1 and D_2, in form VMs increases the voltage gain by adjusting the turns ratios of the TWCI. Moreover, the switch voltage spike is restrained by a regenerative passive clamp circuit, including C_c and D_c. In the proposed circuit, due to applying a QR operation among L_k, C_2, and C_c, the switch's current shapes and the diodes D_1 and D_o change in a sinusoidal form, which alleviates the switch turn-off loss and eliminates the diodes reverse recovery problem. To simplify the circuit analysis in Continous Conduction Mode (CCM) condition, the following assumptions are made:

1) All switching devices of the circuit are seen as ideal, and the parasitic components are neglected.
2) All capacitors are large enough so that their voltages are considered to be constant.
3) The TWCI is regarded as an ideal transformer with a parallel magnetizing inductor (L_M) and a series leakage inductor (L_{k1}) seen from the primary side with the turns ratios of $n_{21}=N_2/N_1$ and $n_{31}=N_3/N_1$.

The theoretical waveforms of the proposed converter for a switching period are shown in Fig. 2. These key waveforms are divided into six operational modes. The corresponding equivalent circuits for each operating mode are also shown in Fig. 4.

Mode 1 [t_0 - t_1]: At the beginning of the first mode, at $t = t_0$, the single power switch S starts to conduct at ZCS condition. The leakage inductances of the TWCI remove *di/dt* in the MOSFET power at the turn-on instant. Diode D_2 is conducting, and other diodes are reverse-biased in this time duration. The current flow path is shown in Fig. 4(a). In this mode, the input inductor (L_{in}) starts to be charged by the input voltage V_{in}. The capacitors C_c and C_3 received energy from the secondary winding current of the TWCI. Also in this mode, due to the positive value of i_{Lk1}, and i_{N3}, the capacitors C_1 and C_2 are discharging their energy. During this short time transition, the currents of L_K and L_M decrease linearly. The leakage inductor on the primary side of the TWCI leads to a decreased current slope through D_2. Consequently, at the end of this mode ($t = t_1$), the current of the diode D_2 reaches zero at ZCS condition with minimum reverse recovery loss.

Mode 2 [t_1 - t_2]: In the second time interval, the power switch *S* remains on, and diodes D_1 and D_o began to turn-on

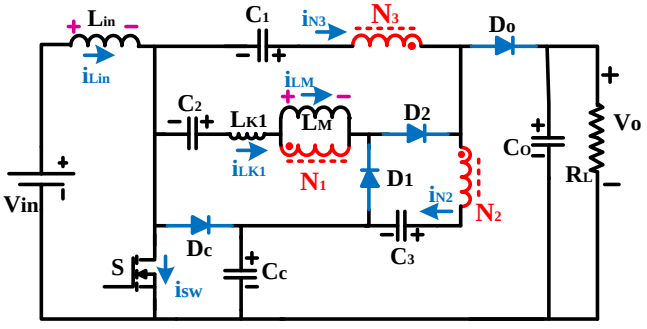


Fig. 1. Equivalent circuit of the proposed step-up converter.

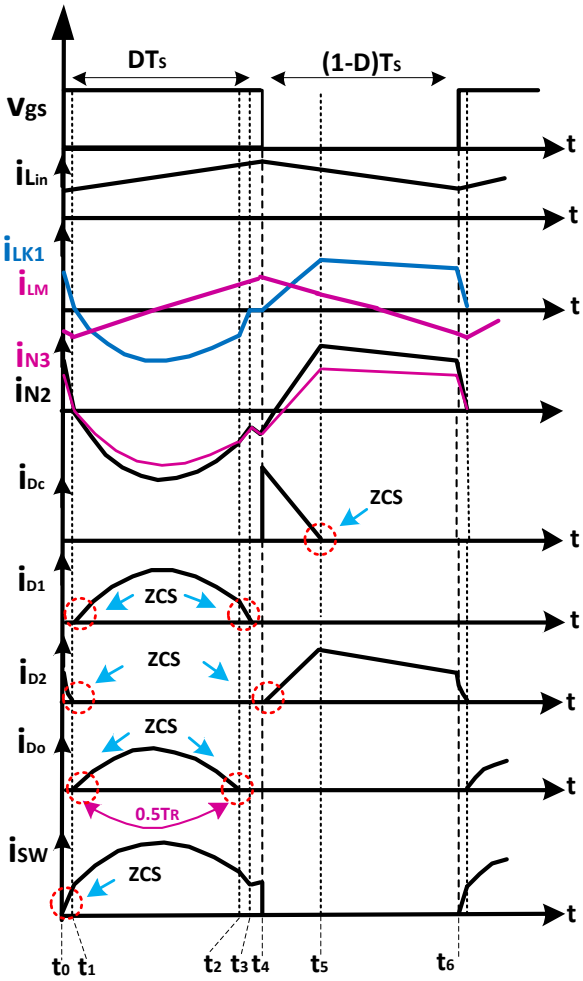


Fig. 2. Typical waveforms in the CCM operation of the converter.

under ZCS condition. The input inductor receives energy from the input voltage, thus its current increase linearly. Also, Due to the positive voltage applied to the magnetic inductor (VC2-VCc), its current starts to increase with a positive slope. Also, the output capacitor C_o received energy from the capacitors C_c and C_3 along with the secondary side of the CI. During this mode, a resonant tank consisting of the leakage inductor L_k and the capacitors C_c and C_2 is created in the form of QR, which discharges the energy of the capacitor C_c. This QR performance changes the current shape of the switch, diodes D_1 and D_o as well as the leakage inductor into a quasi sinusoidal current. As shown in Fig. 2, the current value of the power switch at the end of this mode is decreased significantly, which reduces its turn-off loss. Furthermore, the QR operation causes the current of the output diode to reach zero naturally under the ZCS condition at the end of this mode. Therefore, it is expected that the switching moment spikes at the output DC voltage will be significantly reduced. The resonant frequency (f_R) is obtained by applying Kirchhoff's Voltage Law (KVL) on the circuit and assuming a constant voltage over the magnetizing inductor (L_M) as follows:

$$f_R = \frac{1}{T_R} = \frac{1}{2\pi\sqrt{L_{k1}\left[C_2 \| \frac{C_c}{2+\frac{1+n_{21}}{n_{31}-n_{21}}}\right]}} \quad (1)$$

The resonant operation in the proposed converter can occur in two ways, including Below-Resonant (BR) ($T_R/2 < DT_S$) and Above-Resonant (AR) ($T_R/2 > DT_S$). Under BR, as shown in Fig. 3, The current passing through the switch and the output diode has the highest stress level. As the resonant frequency decreases, the current stress of these components decreases. However, the switch current increases slightly at turn off instant. In the AR operation ($T_R/2 > DT_S$), the output diode has lost the ZCS condition, and the diode current no longer reaches zero with a gentle sine slope. To further reducing the switch and the output diode losses as well as

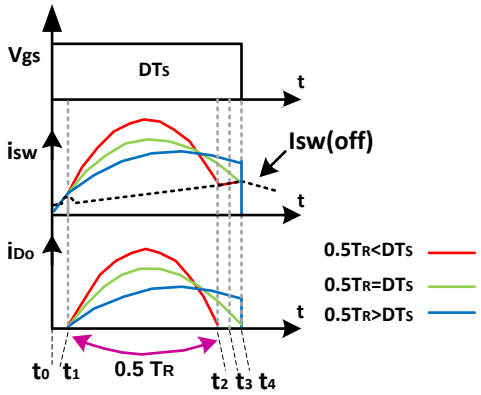


Fig. 3. The current waveforms of the switch and output diode in QRO modes.

reducing their current stress, half of the resonance interval should be adjusted close to the converter switching time interval ($T_R/2 \approx DT_S$). It should be noted that the current waveform changes of the diode D_1 are almost similar to the output diode D_o.

In this mode, the following equations can be written:

$$v_{Lin} = V_{in} \quad (2)$$

$$v_{LM} = v_{C2} - v_{Cc} \quad (3)$$

$$v_{LM} = \frac{v_{C3}+v_{C2}-v_{C1}}{1-n_{21}+n_{31}} \quad (4)$$

$$v_{LM} = \frac{v_o-v_{C1}}{n_{31}} \quad (5)$$

$$v_o = v_{Cc} + v_{C3} + n_{21}v_{LM} \quad (6)$$

$$v_o = v_{C1} + n_{31}v_{LM} \quad (7)$$

Here, $n_{21}=N_2/N_1$ and $n_{31}=N_3/N_1$. Also, the current passed through the single power switch (i_{SW}) is obtained as:

$$i_{sw} = i_{in} - i_{LK1} - i_{N3} \quad (8)$$

where i_{N3} represents the current of the tertiary side of the CI.

Mode 3 [t_2 - t_3]: This mode begins when the QR operation of Mode 2 is finished, and the current of the diode D_o reaches zero naturally in sinusoidal form without reverse recovery problem, as it is shown in Fig. 4(c). During this time, the current value of the second and third sides of the TWCI are identical. The Capacitor C_2 and C_1 are charged by the primary and tertiary sides current of the coupled inductor. The energy stored in capacitor C_c and C_3 are discharged to the coupled inductor. Moreover, in this state, the input inductor is magnetized by the input voltage source. Due to the positive voltage applied to the magnetizing inductor (V_{C2}-V_{Cc}), its

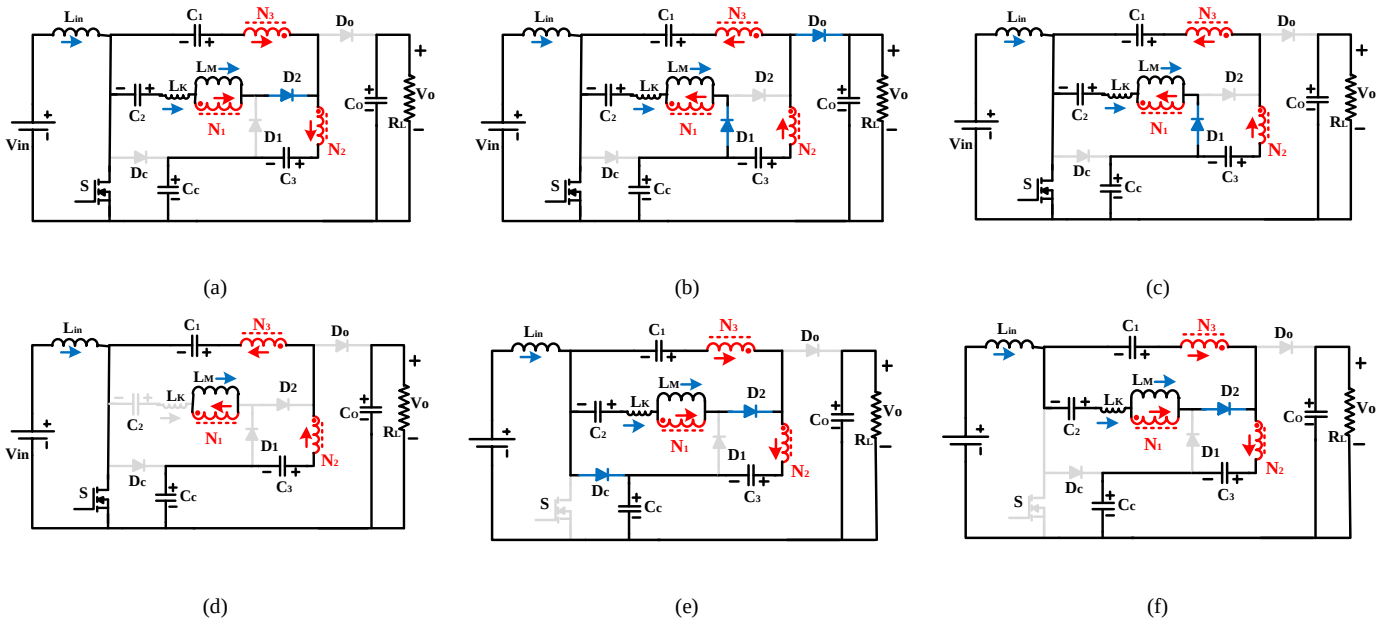


Fig. 4. The operation modes of the proposed converter, (*a*) Mode *1*, (*b*) Mode *2*, (*c*) Mode *3*, (*d*) Mode *4*, (*e*) Mode *5*, and *(f)* Mode *6*.

current starts to increase with a positive slope. The inductors L_{in} and L_M are also charged the same as the operating mode 2. This mode ends, when the current passed through diode D_1 decreases to zero at the ZCS condition. In this time interval, the following equations can be written:

$$v_{LM} = v_{C2} - v_{Cc} \tag{9}$$

$$v_{Lin} = V_{in} \tag{10}$$

$$i_{SW} = i_{in} - i_{LK1} - i_{N3} \tag{11}$$

Mode 4 [t_3 - t_4]: In this transient mode, the power switch remains on, and all diodes are reversed biased. Referring to Fig. 4 (d), the currents of the primary side (i_{N1}) and the magnetizing inductor of the TWCI are identical. Thus, the current of the leakage inductor remains zero. In this mode, the capacitor C_1 received energy from the capacitors C_c and C_3. The current of the single power switch can be expressed as:

$$i_{SW} = i_{in} + \frac{i_{LM}}{n_{31}-n_{21}} \tag{12}$$

Mode 5 [t_4 - t_5]: At $t = t_4$, the power switch S is turned off, and the clamp diode D_c is forward biased, simultaneously. Also, owing to the existence of the leakage inductor, the current of the diode D_2 starts to turn-on under ZCS condition as shown in Fig. 4(e). Therefore, the voltage stress across the single power switch is restricted by the clamp capacitor C_c. Furthermore, the capacitor C_3 begins to charge from the energy stored in the magnetizing inductor and capacitors C_1 and C_2. Moreover, the capacitor C_c receives energy from the input inductor current. Consequently, i_{Lin} and i_{LM} decrease linearly. The following equations can be expressed in this mode:

$$v_{Lin} = V_{in} - V_{Cc} \tag{13}$$

$$v_{LM} = \frac{V_{C2}-V_{C3}}{1+n_{21}} \tag{14}$$

$$v_{LM} = \frac{V_{C2}-V_{C1}}{1+n_{31}} \tag{15}$$

Mode 6 [t_5 - t_6]: This time interval is started when the current passing through the clamp diode D_c reaches zero at the ZCS condition with low reverse recovery loss. In this mode, the energy stored in the input inductor is transferred to the capacitors C_c and C_3. During this time, the current of the third side of the TWCI and the input inductor are identical. The following equations can be obtained in this time duration:

$$v_{LM} = \frac{V_{C2}-V_{C1}}{1+n_{31}} \tag{16}$$

III. Steady-State Performance Analysis of the Proposed Converter

A. Voltage Gain

To find the voltage of the capacitor C_c, the volt-second balance law is applied to the input inductor. Thus, the average value of capacitor C_c can be found as follows:

$$V_{Cc} = \frac{V_{in}}{1-D} \tag{17}$$

where D is the duty cycle of switch S. By employing the volt-second balance across the magnetizing inductor, the following equation between the voltage capacitors C_1 and C_2 is obtained as:

$$(1-D)n_{31}V_{C2} - V_{C1}(\mathrm{D} + n_{31}) = -V_o\mathrm{D}(1+n_{31}) \tag{18}$$

By substituting (3) into (18) and the use of (5), the voltage of the capacitor C_1 is calculated as:

$$V_{C1} = \frac{V_o(1+\mathrm{D}n_{31})+n_{31}(1-D).V_{Cc}}{1+n_{31}} \tag{19}$$

Substituting V_{C1} from (19) into (18), one can obtain the V_{C2} as follows:

$$V_{C2} = \frac{-DV_o(1+n_{31})+V_{C1}(D+n_{31})}{n_{31}(1-D)} \tag{20}$$

In respect to operating Mode *II* and using (3) and (6), the voltage of the capacitor C_3 is derived as:

$$V_{C3} = V_o + V_{Cc}.(n_{21}-1) - n_{21}.V_{C2} \tag{21}$$

Finally, substituting (3) into (4), (14) into (15), and (7) into (6), the overall voltage gain of the proposed converter in CCM

is obtained as:

$$M = \frac{V_o}{V_{in}} = G.\frac{1}{(1-D)} \quad (22)$$

Where the parameter G is defined as:

$$G = \frac{1+n_{31}+X}{X} \quad (23)$$

and the parameter X is defined as:

$$\mathbf{X} = n_{31} - n_{21} \quad (24)$$

From (22), the voltage gain ratio can be regulated in a wide range and increased by adjusting three parameters including n_{31}, X, and D. The voltage gain ratio of the proposed converter as a function of duty cycle and different values of n_{31} and X is depicted in Fig. 5. It can be seen that the voltage gain ratio can be increased by increasing D, n_{31}, and also decreasing the parameter X. Moreover, according to this figure, the voltage gain is more sensitive to the parameter X changes against n_{31}. Thus, a higher voltage gain can be achieved by properly adjusting X at a fewer winding turns ratio (n_{21}+n_{31}). Fig. 6 and Table *I* show the effect of reducing parameter X on the voltage gain under a constant G. It is clear that by reducing X, the specified voltage gain can also be obtained under fewer turns of the TWCI, which leads to less ohmic losses. In the following section, the effect of parameter X on the stress of the elements is analyzed.

B. Voltage and Current Stresses

Regarding the aforementioned analysis and using (17) and (22), drain-source voltage stress (V_{DS}) across the switch (S) is obtained as follows:

$$V_{DS} = \frac{V_{in}}{1-D} = \frac{X}{1+n_{31}+X}V_o = \frac{1}{G}V_o \quad (25)$$

Besides, the maximum repetitive peak reverse voltage across the proposed converter diodes D_c, D_1, and D_2 at their off-state is given as:

$$V_{Dc} = V_{DS} = \frac{X}{1+n_{31}+X}V_o = \frac{1}{G}V_o \quad (26)$$

$$V_{D1} = \frac{1+n_{31}+n_{21}X}{(1+n_{21})(1+n_{31}+X)}V_o \quad (27)$$

$$V_{D2} = \frac{1+n_{31}}{1+n_{31}+X}V_o \quad (28)$$

Moreover, the maximum voltage stress on the output diode D_o, which is happened in the short time transient Mode 1 (see Fig. 3(a)), can be given as:

$$V_{Do} = \frac{n_{31}}{1+n_{31}+X}V_o \quad (29)$$

According to equations (25)-(29), the voltage stress across the semiconductor components can be decreased by increasing n_{31} or decreasing parameter X. Fig. 7 (a) and (b) indicates the effect of parameter X and turns n_{31} across the diodes D_c, D_1, D_2, and D_o as a function of duty cycle under different cases that mentioned in Table *I*. According to this figure, by decreasing the parameter X, the voltage stress on the output diode (V_{Do}) is decreased, and while V_{D2} remains constant. On the other hand, increasing X leads to increasing V_{D2}. However, the level of V_{D2} is far less than the output voltage of the proposed converter.

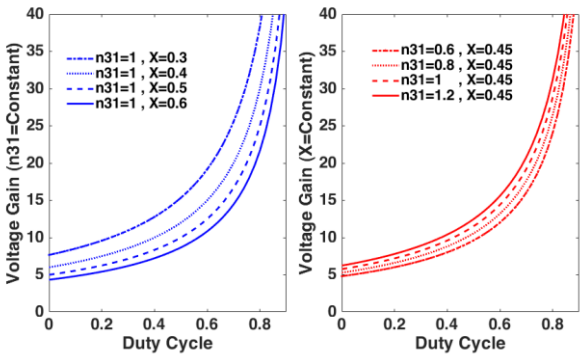


Fig. 5. Voltage gain as a function of the duty cycle for different n_{31} and X.

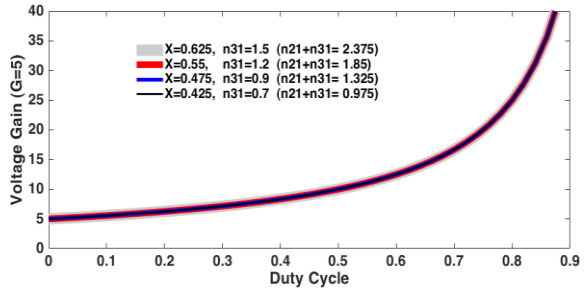


Fig. 6. The effect of reducing parameter X while adjusting n_{31} due to the variation in the duty cycle to achieve s fixed voltage gain (G=5).

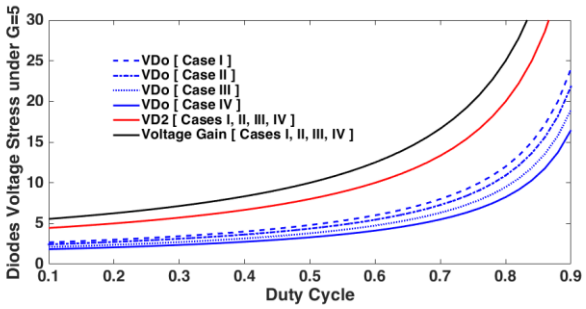
TABLE I. FOUR DIFFERENT MODES OF n_{31} AND PARAMETER X UNDER CONSTANT VALUE OF **G=5.**

Case No.	X	n_{31}	n_{21}	$n_{21}+n_{31}$
I	0.625	1.5	0.875	2.375
II	0.55	1.2	0.65	1.85
III	0.475	0.9	0.425	1.325
IV	0.425	0.7	0.275	0.975

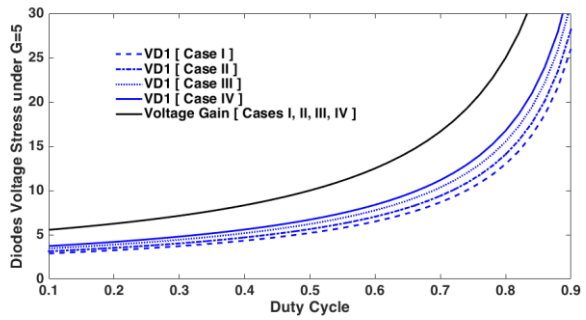
From (22), the average value of the input inductor current is obtained as:

$$< i_{in} >= MI_o \quad (30)$$

Where I_o represents the output load current. Also, applying



(a)



(b)

Fig. 7. The normalized maximum voltage stress across the proposed converter diodes as a function of duty cycle compare the voltage gain under different cases given in Table *I*, (a) the diodes D_2, and D_o, (b) the diode D_1.

ampere-second balance law for capacitors, the average current values passing through D_c, D_1, D_2, and D_o and also the magnetic and the leakage inductors are calculated as:

$$< i_{Dc} >=< i_{D1} >=< i_{D2} >=< i_{DO} >= I_o \quad (31)$$

$$< i_{LM} >=< i_{LK1} >= 0 \quad (32)$$

Assuming the critical mode operation in QR performance, which is taking place in Mode *II* ($0.5T_R \approx D.T_S$), and regarding the sinusoidal form of the current waveform of the diodes D_1 and D_o, the peak current of these diodes are estimated as:

$$i_{D1\_peak} \approx i_{Do_{peak}} = \frac{\pi}{2D} I_o \quad (33)$$

Furthermore, the maximum current value passing through the diode D_2 is given as:

$$i_{D2\_peak} \approx \frac{I_o}{1-D} \quad (34)$$

Using (8), (30), and (33), the peak and Root Mean Square (RMS) values of the single power switch current are computed as follows:

$$i_{SW}(\mathrm{t}) \approx MI_o + \frac{\pi}{2D}\left(\frac{1+n_{31}}{X}\right) I_o \sin(w_R t) \quad (35)$$

$$i_{SW\_peak} = \left(M + \frac{\pi}{2D}\left(\frac{1+n_{31}}{X}\right)\right) I_o \quad (36)$$

$$I_{SW(RMS)} = I_o \sqrt{DM^2 + \frac{4DMH}{\pi} + \frac{DH^2}{2}} \quad (37)$$

Where M is the ideal voltage gain of the proposed converter, and H is defined as:

$$H = \frac{\pi}{2D}\left(\frac{1+n_{31}}{X}\right) \quad (38)$$

As mentioned, due to the QR operation, the switch turn-off current value is decreased in the proposed circuit. Using (12), the switch current value in the turn-off instant is obtained as:

$$i_{SW}^{t=off} = MI_o + \frac{\Delta i_{Lin}}{2} + \frac{\Delta i_{LM}}{2X} \quad (39)$$

Besides, the maximum stress current passing through D_c at the beginning of Mode 5 is given using (39) as:

$$i_{Dc\_peak} = i_{SW}^{t=off} \quad (40)$$

Fig. 8 (a) and (b) illustrate the maximum and the RMS values of the switch current along with the voltage gain at different turns ratio n_{31} under a constant value of parameter X (X is considered 0.45). It can be seen that the minimum rate of the switch current stress has occurred at the duty cycle range $0.4<D<0.65$. Besides, increasing n_{31} leads to a proportional increase in current stress (peak and RMS values).

Moreover, the comparison among the peak, the RMS, and the turn-off values of the switch current for the cases in Table *I* are plotted in Fig. 9. It can be seen that selecting smaller values of parameter X does not affect increasing the peak and RMS current values. However, it can lead to a slight increase in the amount of switch turn-off current. It should be noted that, according to Fig. 7 and Fig. 9, choosing very small values of parameter X is not recommended as it can increase V_{D1} and the current of the switch at turn-off.

C. Analysis of Power Dissipations

In this section, the power loss analysis of the circuit components of the proposed converter is discussed.

Switch Losses: The switch power losses are including turn-on, turn-off, and conduction losses. In the proposed topology, due to ZCS performance for the power switch, the switch turn-on loss is neglected. Thus, the switch power loss is given as:

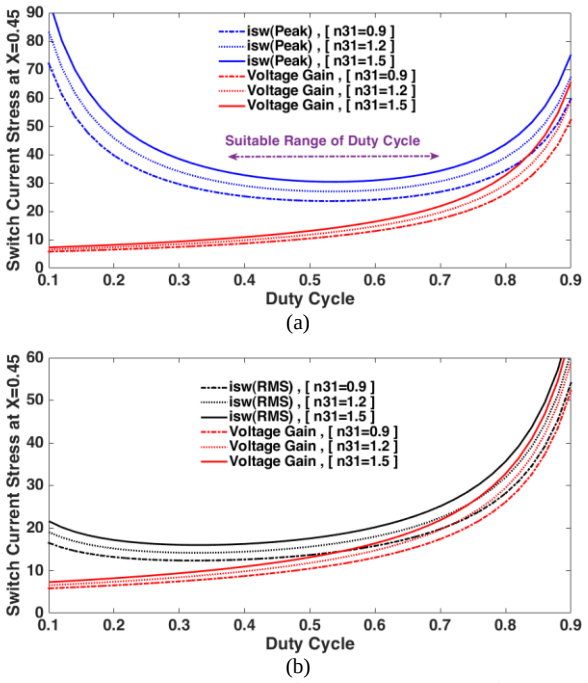


Fig. 8. The normalized current stress of the power switch as a function of the duty cycle compares the voltage gain at different turns ratio n_{31} under X=0.45. *(a) the maximum values of the switch current, (b) the RMS values of the switch current.*

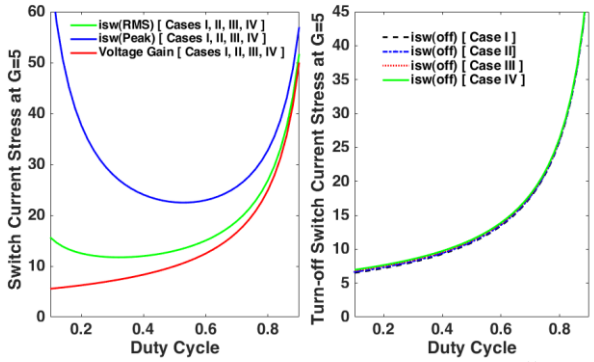


Fig. 9. A comparison among the peak, the RMS, and the turn-off values of the switch currents for the Table I case conditions at G = 5.

$$P_{SW}^{loss} = \frac{1}{2T_s}.V_{DS}\left(i_{SW}^{\mathrm{t=off}}.t_{off}\right) + I_{SW(RMS)}^2.R_{DS(on)} \quad (41)$$

Where t_{off} denotes the switch turn-off time. In the proposed circuit, due to the QR performance takes place during Mode II, the switch turn-off loss is alleviated.

Diode Losses: The diode power losses are divided into the forward voltage drop, conduction resistive losses, and reverse recovery dissipations. In the presented circuit, the ZCS performance for all diodes leads to the reverse recovery alleviation. Consequently, diode losses of the proposed converter are given as:

$$P_{D_{1,2,c,o}}^{loss} = V_F.I_{D(AVG)} + I_{D(RMS)}^2.r_D \quad (42)$$

Where V_F and r_D are the forward voltage drops and the conduction resistance, respectively.

Capacitors Losses: The capacitor losses are calculated using the equivalent series resistance (ESR) as:

$$P_{Cap.}^{loss} = I_{C(rms)}^2.ESR \quad (43)$$

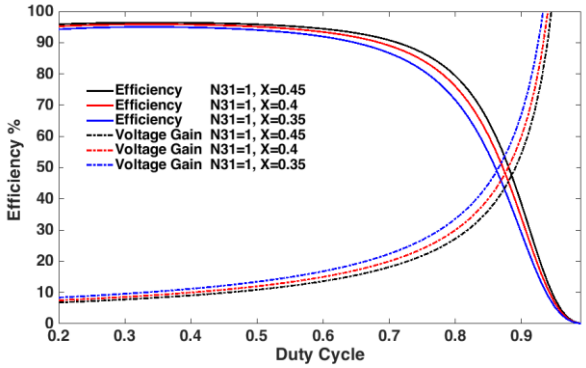
Magnetic component Losses: The magnetic losses of the input

inductor and TWCI, which consist of the copper and core losses, can be expressed as:

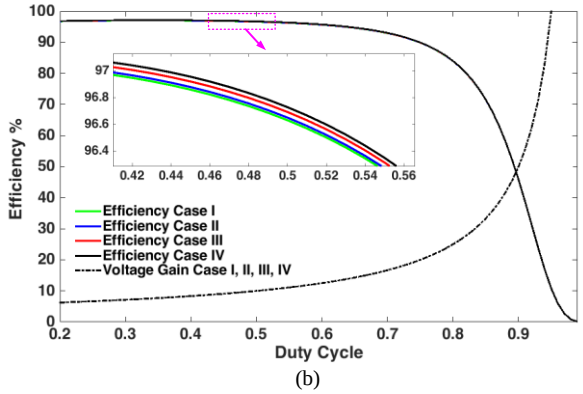
$$P_{mag.}^{loss} = I_{L_{in}(RMS)}^2 . r_{L_{in}} + I_{lk1(RMS)}^2 . r_{eq1} + P_{Core_{Lin}/TWCI} \quad (44)$$

Where r_{Lin} and r_{eq} represent the DC resistances of L_{in} and TWCI, respectively.

The effect of the parameter *X* on the estimated efficiency is demonstrated in Fig. 10 (a) and (b). The converter parameters are considered as follows: V_{in} = 20 V, R_L = 250 Ω, r_{Lin} = 43 mΩ, $r_{LM\text{-}Case\ I}$ = 200 mΩ, $r_{LM\text{-}Case\ II}$ = 150 mΩ, $r_{LM\text{-}Case\ III}$ = 100 mΩ, $r_{LM\text{-}Case\ IV}$ = 48 mΩ, f_s = 50 kHz, $t_{d(off)}$ = 50 ns, $t_{d(on)}$ = 26 ns, $r_{ds(ON)}$ = 5.6 mΩ, $r_{D1} = r_{D2} = r_{Dc} = r_{Do}$ = 7 mΩ, r_{esrC1} = 25 mΩ, $r_{esrCc} = r_{esrC2}$ =30mΩ, $r_{esrC3} = r_{esrCo}$ =100 mΩ, VF_{D2} = 0.52, VF_{Dc} =0.45 , $VF_{D1\text{-}Case\ I}$ =0.5, $VF_{D1\text{-}Case\ II}$ =0.53, $VF_{D1\text{-}Case\ III}$ =0.56, $VF_{D1\text{-}Case\ IV}$ =0.58, $VF_{Do\text{-}Case\ I}$ =0.5, $VF_{Do\text{-}Case\ II}$ =0.47, $VF_{Do\text{-}Case\ III}$ =0.44, and $VF_{Do\text{-}Case\ IV}$ =0.42. From Fig. 10 (a), by increasing the duty cycles and decreasing the parameter *X*, the converter efficiency is decreased. In fact, because of the high voltage and current rates in higher duty cycles, the maximum power-handling capability is limited. This sudden drop in the efficiency curve happens in all high voltage gain topologies. However, the full soft-switching performance, which reduced the power dissipition, led to high power-handling capacity. Also, according to Fig. 10 (b), selecting smaller values of the parameter *X* at a constant voltage conversion ratio (conditions of Table *I* cases) does not lead to a significant effect on the estimated efficiency of the converter.



(a)



(b)

Fig. 10. The estimated efficiencies and voltage gains versus the duty cycle, *(a) under different values of the parameter X, (b) for the conditions of Table I cases.*

IV. Performance Comparison

To clarify the merits of the proposed converter, an analytical comparison is done with its recently published counterparts, which are summarized in Table *II*.

Fig. 11 shows a line chart of the voltage gain comparison of the converters mentioned in Table *II* under the same conditions (case *IV* from Table *I*. As can be seen, only the proposed converter can provide a higher voltage gain than the other converters while maintaining performance features such as continuous input current, soft-switching performance for the power switch, and minimum reverse recovery loss for the diodes. It is noteworthy that the quadratic topology in [22] has a higher voltage gain than the proposed converter only at D>0.5. However, the lack of ZCS condition for its power switches and considerable reverse recovery losses are the main disadvantages of the mentioned converter.

Furthermore, the normalized maximum voltage across the main power switch and the output diode of the converters of Table *II* are compared in Case *IV* and illustrated in Fig. 12 and Fig. 13. As depicted in these figures, the presented converter has the lowest voltage stress level compared to the other converters. This makes it possible to use switching devices (MOSFET and diodes) with lower parasitic components, which decreases the power dissipations. Moreover, because of soft-switching operation for all switching components of the proposed converter, the switching losses are significantly alleviated leading to improved efficiency. For this purpose, a comparison of the theoretical efficiency under the same specific conditions (20 V/200 V, 100 W, 50 kHz, and Case *IV*) is carried out and presented in Table *II*. The parasitic components ($R_{DS(on)}$, ESR, V_F, …) are chosen based on related

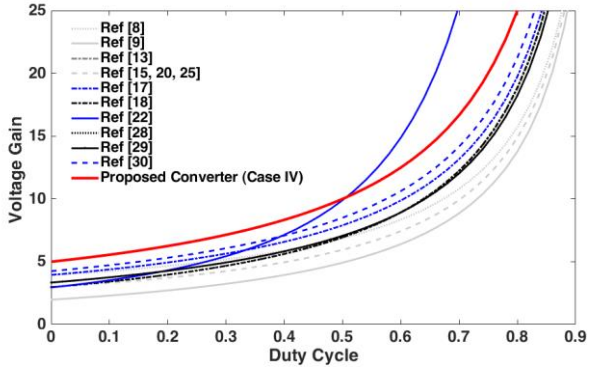


Fig. 11. The voltage gain comparison of converters given in Table *II* under Case *IV*.

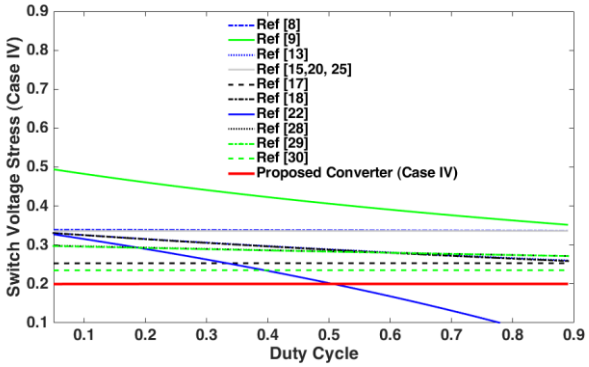


Fig. 12. Comparison of normalized voltage stress across the main power switch of the converters given in Table *II* under Case *IV*.

TABLE II. PERFORMANCE COMPARISON OF THE PROPOSED CONVERTER WITH OTHER RELATED CONVERTERS.

Converter Topology	No. of Components S/D/C/CI+L/T	Voltage Gain	L.I.C.R	Voltage Stress on Main Switch	Voltage Stress on Output Diodes	Soft-Switching (Main Switch)	Reverse Recovery Loss	Eff. 100 W (50 kHz)
[8]	1/4/5/1^{2w} +1/12	$\frac{(1+n)D+1}{(1-D)}+2n$	Yes	$\frac{V_o}{1+D+n(2-D)}$	$\frac{(1+n)V_o}{1+D+n(2-D)}$	ZCS+QR	Very Low	96.4%
[9]	1/4/5/1^{2w} +1/12	$\frac{1+n(1+D)}{(1-D)}$	Yes	$\frac{V_o}{1+n(1+D)}$	$\frac{(1+n)V_o}{1+n(1+D)}$	ZCS+QR	Very Low	96.1%
[13]	1/4/4/1^{2w} +0/10	$\frac{2+n+nD}{(1-D)}$	No	$\frac{V_o}{2+n+nD}$	$\frac{(1+n)V_o}{2+n+nD}$	ZCS	Low	96.8%
[15]	1/3/4/1^{2w} +1/10	$\frac{n+2}{(1-D)}$	Yes	$\frac{V_o}{n+2}$	$\frac{(1+n)V_o}{n+2}$	ZCS	Medium	96.0%
[17]	1/5/6/1^{2w} +1/14	$\frac{2(1+n)}{(1-D)}$	Yes	$\frac{V_o}{2(1+n)}$	$3\times\frac{1+2n(1-D)V_o}{2(1+n)}$	ZCS	Low	95.1%
[18]	1/4/5/1^{2w} +1/12	$\frac{2+n+D}{(1-D)}$	Yes	$\frac{V_o}{2+n+D}$	$\frac{(1+n)V_o}{2+n+D}$	ZCS	Low	95.9%
[20]	1/3/4/1^{2w} +1/10	$\frac{n+2}{(1-D)}$	Yes	$\frac{V_o}{n+2}$	$\frac{(1+n)V_o}{n+2}$	ZCS+QR	Very Low	96.5%
[22]	2/4/4/1^{2w}+1/12	$\frac{1+D+2n(1-D)}{(1-D)^2}$	Yes	$\frac{V_o(1-D)}{1+D+2n(1-D)}$	$\frac{2V_o}{1+D+2n(1-D)}$	QR	Medium	95.8%
[25]	1/4/4/1^{3W}+0/10	$\frac{2+n_{21}+n_{31}}{(1-D)}$	No	$\frac{V_o}{2+n_{21}+n_{31}}$	$\frac{(1+n_{21})V_o}{2+n_{21}+n_{31}}$	-	Low	95.8%
[28]	1/3/4/1^{3W} +1/10	$\frac{2+n_{21}-n_{31}(1-D)}{(1-n_{31})(1-D)}$	Yes	$\frac{(1-n_{31})V_o}{2+n_{21}-n_{31}(1-D)}$	$\frac{(1+n_{21})V_o}{(1-n_{31})(2+n_{21}-n_{31}(1-D))}$	ZCS	Medium	96.2%
[29]	1/3/4/1^{3W} +1/10	$\frac{2+n_{31}-n_{21}}{(1-n_{21})(1-D)}$	Yes	$\frac{(1-n_{21})V_o}{2+n_{31}-n_{21}}$	$\frac{(1+n_{31})V_o}{2+n_{31}-n_{21}}$	ZCS	Low	96.6%
[30]	1/5/6/1^{3W}+1/14	$\frac{3+2n_{21}+n_{31}}{(1-D)}$	Yes	$\frac{V_o}{3+2n_{21}+n_{31}}$	$\frac{(1+n_{31}+n_{21})V_o}{3+2n_{21}+n_{31}}$	ZCS	Low	95.3%
Proposed Converter	1/4/5/1^{3W} +1/12	$\frac{1+2n_{31}-n_{21}}{(n_{31}-n_{21})(1-D)}$	Yes	$\frac{(n_{31}-n_{21})V_o}{1+2n_{31}-n_{21}}$	$\frac{n_{31}V_o}{1+2n_{31}-n_{21}}$	ZCS+QR	Very Low	96.9%

S=Switch, **D**=Diode, **C**=Capacitor, **CI** =Coupled-Inductor, **L**=inductor, **T**=Total Device Count, **L.I.C.R**= Low Input Current Ripple, **Eff**=Efficiency

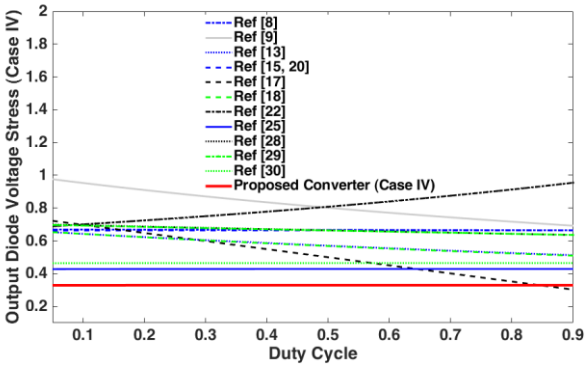


Fig. 13. Comparison of normalized voltage stress across the output diode of the converters given in Table *II* under Case *IV*.

datasheets. Because of full soft-switching performance along with very low reverse recovery loss, the proposed topology demonstrates the highest efficiency against others.

To compare the costs of the converters in the comparison Table *II*, the device price that is used in the circuits should be obtained. Semiconductor elements in different current and voltage stresses are chosen from the same brand, including the IRFP, STL, BUK, and TK series for MOSFETS, BYV series for diodes, ECA series for capacitors, and toroid and ferrite cores from Micrometals for magnetic components. The estimated prices of devices are taken from Mouser or Digikey websites, which are summarized in Table *III*. the total cost of the converters in [13] and [25] much less than the rest due to the use of only one magnetic core. However, the input current with a high ripple is the most important drawback of these two converters, which limits their applications for renewable energy sources. Also, as it can be seen, the cost of the presented converter same as the converters in [15], [18], [20], and [29] is at a low level.

Finally, based on the discussions mentioned above, the proposed topology that has the best utilization of its components can offer relatively good performance for the RES applications.

TABLE. III. SUMMARIZED OF COST COMPARISON OF THE STEP-UP DC-DC CONVERTERS.

Conv.	Cost of				
	Cores	Switches	Capacitors	Diodes	Total
[8]	4.17$	1.48$	3.77$	2.34$	11.76$
[9]	4.17$	1.61$	3.87$	2.32$	11.97$
[13]	1.94$	0.92$	3.70$	2.36$	8.92$
[15]	4.17$	1.48$	3.22$	1.78$	10.65$
[17]	3.76$	0.83$	4.66$	2.74$	11.99$
[18]	4.17$	0.92$	3.22$	2.36$	10.67$
[20]	4.17$	1.48$	3.22$	1.78$	10.65$
[22]	4.84$	4.78$	2.88$	2.18$	14.68$
[25]	1.94$	1.48$	3.46$	2.20$	9.08$
[28]	4.84$	0.92$	3.68$	3.64$	16.08$
[29]	4.17$	1.48$	3.0$	1.78$	10.43$
[30]	3.76$	0.83$	4.78$	2.74$	12.11$
Proposed converter	3.76$	0.5$	4.47$	2.22$	10.95$

V. STABILITY ANALYSIS

The bode plot diagram of input-to-output voltages (V_o/V_{in}) and control-to-output voltage (V_o/d) of the proposed topology obtained using *frest.Sinestream* function in Simulink/ Matlab are illustrated in Fig. 14 (a) and (b). From these curves, the converter is stable with non-minimum phase behaviors. It should be noted that the non-minimum phase behavior is one of the most prominent features of the step-up converters, which is due to the presence to the right half-plane (RHP) zero in the control to output transfer function. The RHP zeros impose an extra phase shift to the loop gain of the transfer function and limit bandwidth.

VI. DESIGN PROCEDURE OF THE KEY ELEMENTS

A. Turn Ratios of the TWCI

The key parameters of the proposed converter are the function of three main parameters *D*, n_{31}, and *X*. As discussed in Section *III*, the value of these parameters affects the performance of the proposed converter. Regarding Fig. 8, the minimum values of the switch current stress happen at 0.4 <D< 0.7. As discussed in Section *III* (see Fig. 6), selecting smaller values for *X* leads to achieving a high voltage gain at fewer turns ratios. However, only a small increment of *X* increases the voltage stress of D_1.

B. Input and Magnetizing Inductors Design

The input inductor L_{in} is designed to limit the input current ripple (at CCM condition) in the desired value as:

$$L_{in} = \frac{V_{in}.D}{\Delta I_{in}.f_s} \tag{45}$$

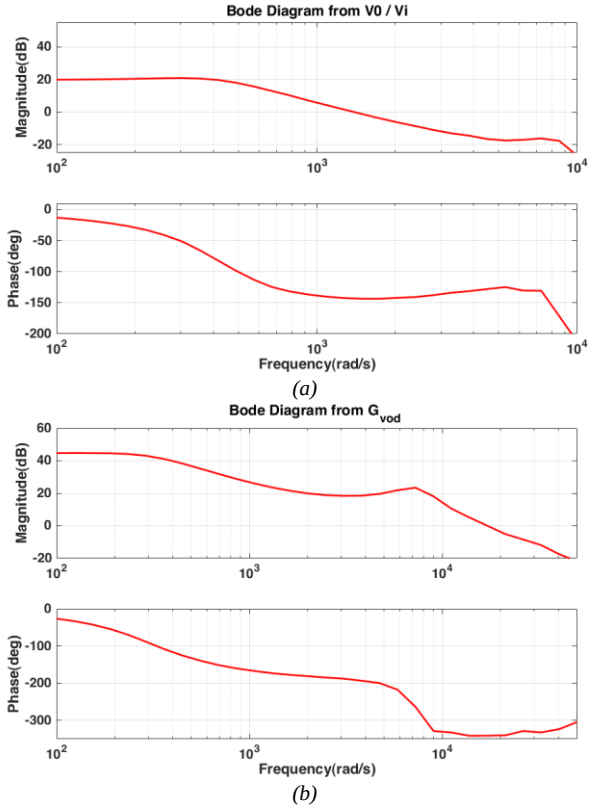


Fig. 14. Bode plot diagrams of the proposed converter, *(a) Input-to-output, (b) Control-to-output.*

Where ΔI_{in} and f_s are the permitted current ripple and switching frequency, respectively. Also, the magnetizing inductor of the TWCI can be designed by:

$$L_M > \frac{V_{Lm}.D}{\Delta I_{LM}.f_s} \tag{46}$$

where ΔI_{LM} is the allowable current ripple. It should be noted that selecting a very small value of the current ripple will increase the amount of L_m, which increases wire consumption as consequently increases the conduction loss.

C. Capacitors Selection

To suppress the voltage ripple on the output load, the output capacitance can be found using the following equation:

$$C_o = \frac{DV_{out}}{R_L.\Delta V_{Co}.f_s} \tag{47}$$

ΔV_{Co} is the maximum tolerant voltage ripple usually set by 1% of the output DC voltage. The suitable values of the capacitors C_1 and C_3 can be determined as:

$$C_1 = \frac{i_{N3}.(1-D)}{\Delta V_{C1}.f_s} > \frac{(1+n_3)V_{out}}{\Delta V_{C1}.R_L.X f_s} \tag{48}$$

$$C_2 = \frac{i_{D2}(1-D)}{\Delta V_{c2}.f_s} > \frac{V_{out}}{\Delta V_{c2}.f_s} \tag{49}$$

$$C_3 = \frac{i_{in}(1-D)}{\Delta V_{c3}.f_s} > \frac{(1-D).M.V_{out}}{\Delta V_{C3}.R_L.f_s} \tag{50}$$

$$C_c = \frac{i_{in}(1-D)}{\Delta V_{Cc}.f_s} > \frac{(1-D).M.V_{out}}{\Delta V_{Cc}.R_L.f_s} \tag{51}$$

Where ΔV_{c1} and ΔV_{c3} represent the allowable voltage ripple. Moreover, based on operation Mode *II*, the QR duration is a function of the capacitors C_2 and C_c. Thus, the values of these capacitors are also obtained as:

$$\pi \sqrt{L_{k1}\left[C_2 \| \frac{C_c}{2+\frac{1+n_{21}}{X}}\right]} = DT_S \tag{52}$$

It is noteworthy that because capacitors C_2 and C_c are not performing any filtering effect, their design can be done under larger allowable voltage ripples. Therefore, selecting small values for these capacitors will not affect the output voltage fluctuation. This will give the designer more freedom in choosing these capacitors. Thus, the simplest and most effective way for adjusting the converter resonant frequency is by properly selecting the values of the capacitors C_2 and C_c.

VII. EXPERIMENTAL RESULTS

To validate the theoretical analysis of the proposed topology, a sample prototype with input voltage from 20 V to 200 V and 160 W output power is built in the laboratory. The experimental setup under full load is shown in Fig. 15. The parameters of the prototype circuit are listed in Table *IV*. Regarding the design procedure, n_{31}=0.827, n_{21}=0.38, and *X*=0.448 are selected (for *G*=5 and *D*=0.53). Thanks to the low voltage stress on the single power switch, a MOSFET with a very low $R_{DS(on)}$ (i.e. IRFP4310) is used in the sample prototype. The sample prototype is built with open-loop control to verify the steady-state performance of the proposed converter. For this purpose, a low-cost PWM driver (TL494) along with an IC Photocoupler TLP 250 have been used to generate the gate pulses. The current and voltage waveforms

were obtained using a high-frequency current probe *PA-667 1MHZ* and a differential probe *GDP-025*, respectively. Moreover, LCR meter *Hantek 1833 /100 kHz* has been used to measure the magnetizing inductor (L_M) and the leakage Inductances of the primary, secondary and tertiary windings of the TWCI. It is noteworthy that, due to the three-winding structure of the coupled-inductor, it is necessary to make three short-circuit tests to obtain the series leakage inductances for the equivalent circuit. The measurement results are presented in Table *IV*.

In Fig. 16 (a), the input inductor current in the steady-state is presented, which is continuous with optimal current ripple ($\Delta I_{in} = 20\% I_{in}$). Regarding Fig. 16 (b), the main power switch turns on at ZCS condition with low voltage stress ($V_{DS} \approx 42$ V). Also, due to QR performance, the switch current is reduced at turn-off time, leading to decreased switching dissipation. From Fig. 17 and Fig.18, the ZCS condition at the turn-off time can be realized in the current of all converter diodes (i_{D1}, i_{D2}, i_{Dc}, and i_{Do}), which eliminates the diode reverse recovery problem. Moreover, the peak reverse voltage across the diodes D_1, D_2, D_c, and D_o are 120 V, 150 V, 40 V, and 60 V, respectively, which are much lower than the output voltage.

The leakage inductor current of the primary side of the TWCI along with the output voltage waveforms are also depicted in Fig. 19 (a).

Table *IV*: PARAMETERS OF PROTOTYPE SETUP.

Parameter	Values
Output Power (P_{out})	160 W
Input Voltage (V_{in})	20 V
Output Voltage (V_{out})	200 V
Switching Frequency (f_s)	50 kHz
Capacitors C_1 and C_3	47 µF / 250 V
Capacitors C_2	6.6 µF / 250 V
Capacitor C_c	8.2 µF / 250 V
Capacitor C_o	100 µF / 250 V
Power Switch	IRFB4310 / $R_{DS(on)}$=5.6 mΩ
Input Inductors L_{in}	130 µH / T184-52
Magnetizing Inductor of the CL (L_m)	220 µH
Turns Ratios of the TWCI *(N1:N2:N3)*	(29:11:24) / EE42/21/20
Leakage Inductances L_{K1}, L_{K2}, L_{K3}	3.96, 0.65, 0.68 µH
Diodes D_1 and D_2	MUR420 ($V_{F\,(Max)}$=0.88 V)
Diodes D_c and D_0	SR360 ($V_{F\,(Max)}$=0.7 V)

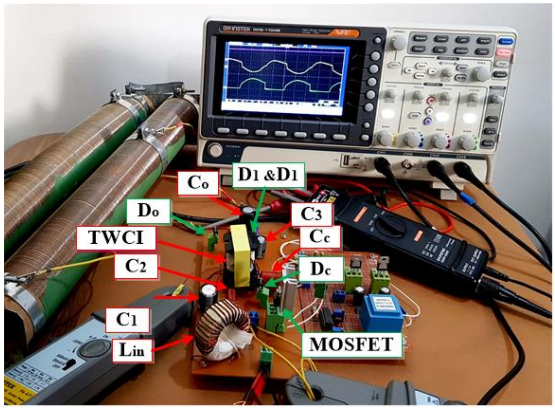
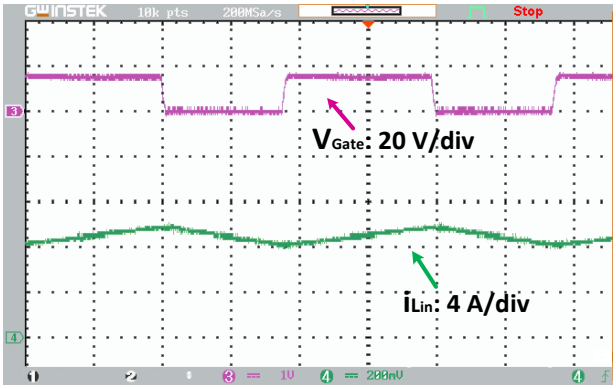
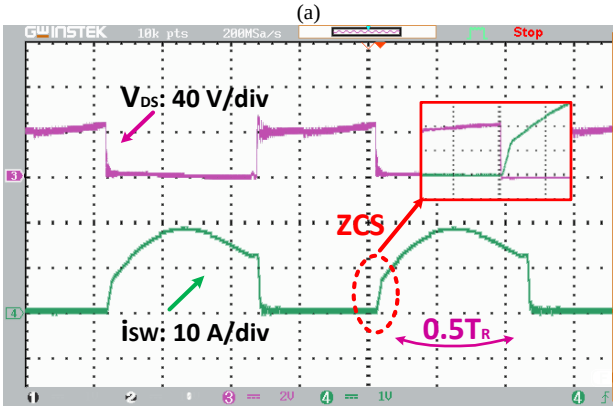


Fig. 15. Picture of the test setup and the experimental prototype under load.

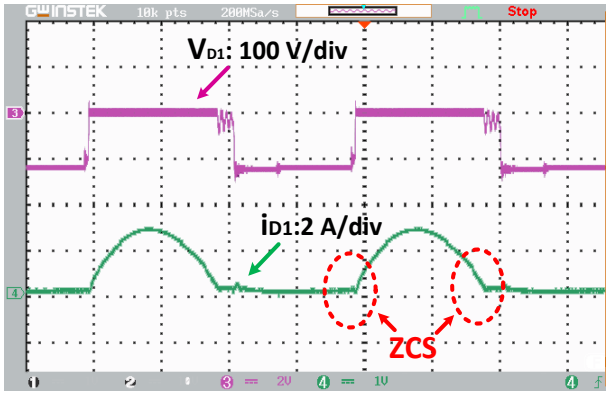


(a)

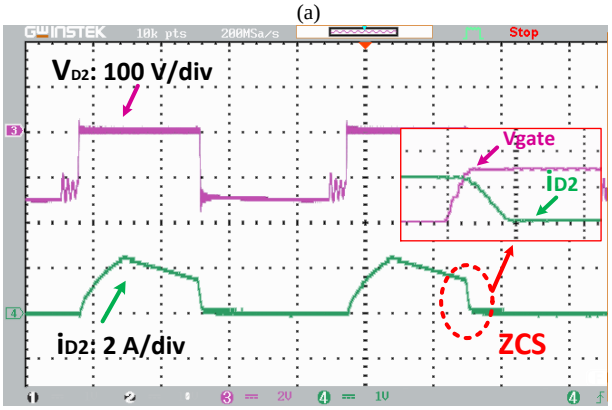


(b)

Fig. 16. Experimental results of the proposed topology, (a) input inductor current (b) MOSFET S.

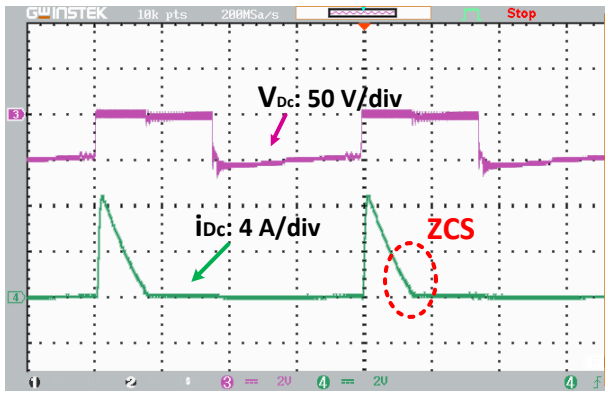


(a)

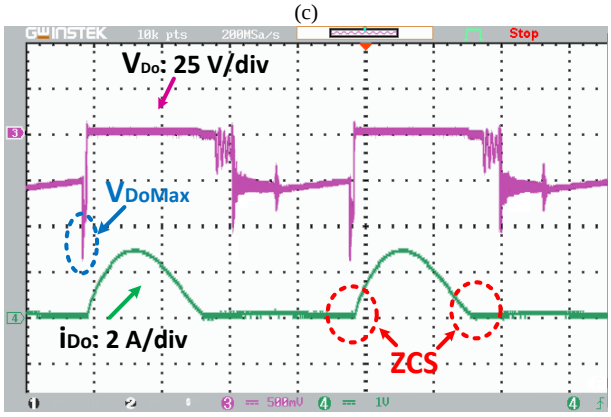


(b)

Fig. 17. Experimental results of the proposed topology, *(a) diode D_1, (b) diode D_2,*

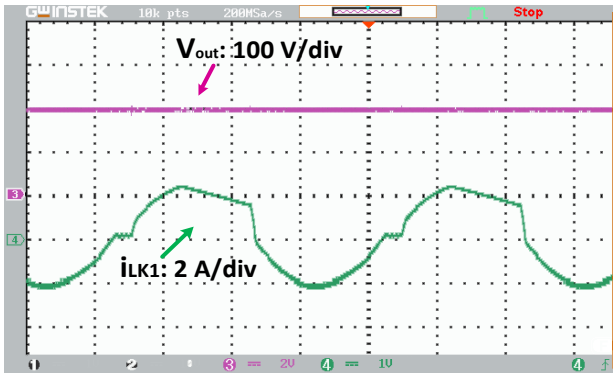


(c)

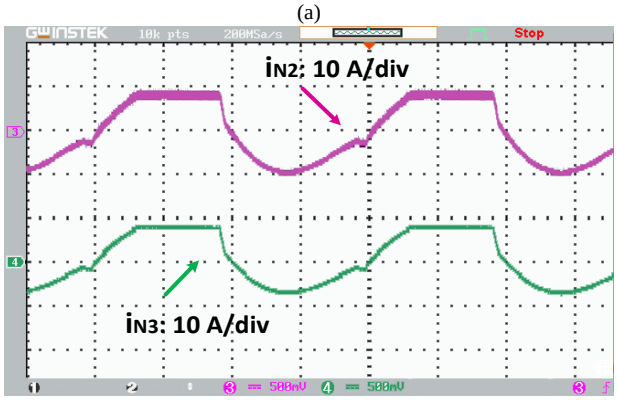


(d)

Fig. 18. Experimental results of the proposed topology, *(a) diode D_c, (b) diode D_o.*



(a)



(b)

Fig. 19. Experimental results of the proposed topology, *(a) i_{LK} and V_{out}, (b) i_{N2}, and i_{N3}.*

Because of the QR performance of the output diode current, the DC output voltage is constant without any voltage spike and noise at the switching instants, which is the other advantage of the proposed converter. Moreover, the experimental results of the secondary and tertiary sides of the TWCI (i_{N2}, and i_{N3}) are shown in Fig. 19 (b).

The measured efficiency of the proposed converter versus output power variations at V_o= 200 V is shown in Fig. 20. The efficiency is measured for two different values of the input voltages, V_{in}=20 V and V_{in}=25 V. The overall efficiency of the proposed converter at full load condition (20 V / 200 V and 160 W) is about 96.6%. From this figure, it can be observed that by decreasing the voltage gain from 10 to 8 at V_{in} = 25 V, the efficiency can be improved. Besides, Fig. 21 represents the pie graph of loss breakdown at full load. This curve is calculated under the theoretical analysis in Section *III* by considering the parasitic elements in real conditions. Despite the high input current level, due to low voltage stress and soft-switching performance (i.e. ZCS and QR), the power dissipation share of the power switch is lower than other losses. Finally, the experimental result of the dynamic response of the output voltage for a step change of 50% in the output load from R_L=250 Ω to R_L=375 Ω is provided and shown in Fig. 22, which proves the inherent stability of the proposed converter. To obtain the experimental result, a 10X voltage probe is used. This voltage change will be eliminated if the closed-loop controller structure is used with the proper bandwidth.

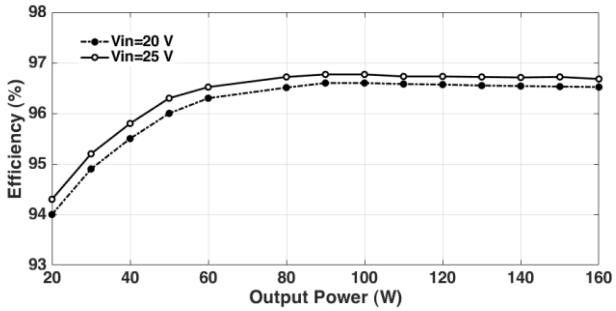


Fig. 20. Measured efficiency versus output powers.

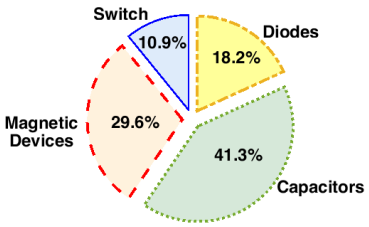


Fig. 21. Break-down of power losses at full load (V_{in} = 20 V, V_o = 200 V, and P_{out} = 160 W).

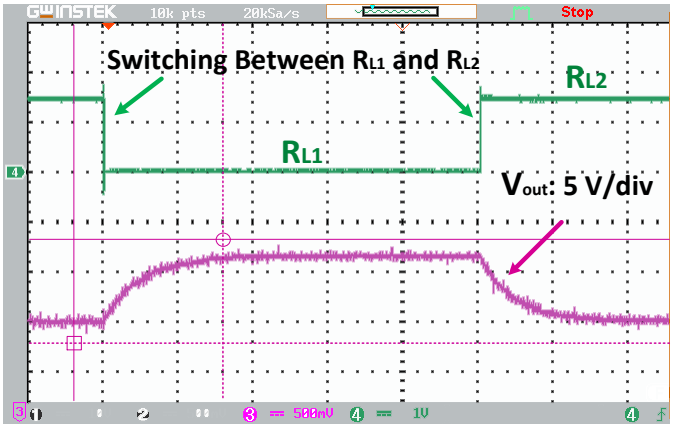


Fig. 22. Hardware measurement of the dynamic response of the output voltage for a 50 % step change in the output load from R_{L1}=250Ω to R_{L2}=375Ω.

VIII. Conclusion

This paper has proposed a new non-isolated single-switch high step-up DC-DC converter for applications like photovoltaic arrays and fuel cells. A three winding coupled inductor along with a voltage multiplier is employed to enhance the voltage gain. A regenerative passive clamp capacitor is also used to limit the main power switch voltage stress and recycle the energy stored in the leakage inductor of the TWCI. High efficiency, high voltage gain, continuous input current with low ripple, low voltage spikes across the single power switch along with ZCS operation for all switching components are the main advantages of the suggested topology. The steady-state analysis and design procedure in the CCM condition have been presented. The major key indicators of the proposed converter have been compared in detail with some other similar converters to justify its merits. Experimental results from a 20 V-200 V /160 W laboratory prototype verified the feasibility of the design. All soft-switching transitions of the switching components are observed in the experimental waveforms, which resulted in high conversion efficiency. The presented results are promising for potential applications for small scale RES applications.

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