Binary-Quintuple Progression Based 12-Switch 25-Level Converter With Nearest Level Modulation Technique for Grid-Tied and Standalone Applications

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Binary-Quintuple Progression Based Twelve Switch Twenty-Five Level Converter with Nearest Level Modulation Technique for Grid-Tied and Standalone Applications

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***Abstract*—This paper introduces a cascaded packed U cell (CPUC) multilevel converter (MLC) to achieve a higher-level count in converter voltage with a minimum number of switches. Here, two five-level PUC topologies are connected in a cascaded manner to obtain twenty-five levels in its output converter voltage. The switch count in CPUC is reduced to 12, as compared to the number of semiconductor devices used for obtaining 25 levels in converter output. A binary-quintuple progression is used for selection of voltage ratios between DC voltage sources, and capacitors. CPUC is operated at low-frequency switching, using the nearest level modulation technique (NLMT). The fundamental switching frequency ensures reduced switching losses as compared to pulse-width modulation (PWM) schemes. The converter performance is analyzed for grid-tied and standalone applications. The performance parameters such as total harmonic distortion (THD) of converter voltage and THD of grid/load current are examined. The CPUC configuration is modeled and simulated in MATLAB/Simulink, and test results are taken using OPAL-RT test bench. The acquired simulation and test results confirm viability, practicability, acceptability, and cost-effectiveness of CPUC-MLI converter over existing MLC topologies for efficient power conversion.**

***Index Terms*— Cascaded Packed U cell, Nearest Level Modulation, Photovoltaic Array, Power Quality,**

NOMENCLATURE

V_{dc1}	DC voltage source of converter I
V_{dc2}	DC voltage source of converter II
S_w	Switch function for ON and OFF state
S_n	Switch n^{th} in the converter
S_{nc}	Complementary of switch S_n
P_1-P_{12}	Twelve positive levels
N_1-N_{12}	Twelve negative levels
i_g	Grid current
v_g	Grid voltage
v_L	Load voltage
i_L	Load current
i_{gref}	Reference grid current
I_{gdc}	Reference peak of the grid
i_n	Current in n^{th} switch
v_{ab}	The voltage across node *ab*
v_{bc}	The voltage across node *bc*
v_{cd}	The voltage across node *cd*
v_{ef}	The voltage across node *ef*
v_{fg}	The voltage across node *fg*
v_{qh}	The voltage across node *gh*
T_L	Total number of levels
L	Level obtained from each cell
N	Number of PUC cells
V_{mli}	Output Converter Voltage of CPUC
C_1	The capacitor of converter I
C_2	The capacitor of converter II
V_{c1}	The voltage across capacitor I
V_{c2}	The voltage across capacitor II
i_{c1}	Current across capacitor I
i_{c2}	Current across capacitor II
R_p	Parasitic resistance
L_f	Interfacing inductance
I_{d1}	Compensating component for the balance of V_{c1}
I_{d2}	Compensating component for the balance of V_{c2}
I_{dT}	The resultant total peak of the grid current
v_{ref}	Modulating Signal
N	Number of PUC Cells
M	Number of positive or negative levels
e_r	The error between reference and actual signal
k_p	Proportional gain
k_i	Integral gain

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I. Introduction

Multilevel converters (MLCs) have created a boom in the electrical sector due to a rise in demand for high power energy conversion [1]. These MLCs are introduced due to limitations of larger filter size and losses in a two-level converter. Furthermore, an extension to a higher power level is not possible without a series connection of semiconductor devices. These MLCs enhance level count in converter voltage and make it near to sinusoidal. In MLCs, switching stress becomes less, and the converter lifetime is increased. The wide known topologies of MLCs are cascaded H bridge (CHB), diode clamped MLC and capacitor clamped MLC [2]. CHB has become popular due to modular structure, but for higher levels isolated DC supply and switch count increase rapidly [3]. Moreover, for more isolated DC supplies, it requires phase-shifting transformers and an extra stage of rectification. The system becomes bulkier, which needs proper space and handling. The diode clamped MLC has a single DC source but possesses neutral point balancing issues [4]. Moreover, device count and additional capacitor balancing

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remain a challenging issue. Similarly, capacitor clamped has balancing issues and flying capacitors (FCs) increase for higher-level MLCs [5]. The main objective is to optimize the converter configuration to reduce the number of devices. The maximum number of levels with minimum component count remains a potential research area in the field of MLCs. Apart from basic configurations, various new topologies have appeared in reduced device count. Packed U cell (PUC) topology is introduced for achieving reduced switch count. The modified PUC converter with the boost mode is proposed in [6]. The five-level and seven-level PUCs are analyzed using six switches, capacitor and DC source. The extension of PUC in terms of CPUC is required to achieve better MLC configurations [7]. The transformer-based multilevel converters with AC side isolation have a single DC source. The work on the configuration with minimum cost is required in grid-connected and standalone MLC systems. The asymmetric MLCs with the ternary sequence are implemented using unipolar PWM. MLCs have been used for single-phase, and three-phase photovoltaic (PV) fed grid-connected applications. The hybrid cascaded MLC with 1:7 asymmetries is discussed in [8]. A nine-level reduced device count active neutral point clamped (ANPC) is proposed in [9]. This configuration has balancing issues and higher device count and extra floating capacitor with higher levels. Nested multilevel topologies have also come but could not give promising solutions [10]. The novel K type multilevel converter is proposed in with self-balancing approach [11]. The level doubling network with capacitor fed H bridge modules is implemented in the literature. Such configuration employs extra capacitors to achieve levels in the converter output voltage. A symmetric switched diode MLC topology with minimized switch count is proposed in [12]. The circuit employs six switches, two DC sources and a diode for obtaining seven level output voltage. A 25 level MLC itself requires 48 switches in CHB configuration. The same level generation with diode clamped MLC and flying capacitor MLC, is practically unfeasible due to a large number of switches, clamped diodes, and capacitors. Moreover, using transformer-based MLIs for 25 levels requires a transformer and measures to tackle saturation issues. The asymmetric MLCs use binary, ternary progressions in isolated DC voltages to obtain higher levels. The selection of ratio plays an important role in the level formation. Modular multilevel converters (MMCs) are also used, but these converters have circulating current issues, and each capacitor requires sorting based complex algorithms [13]. The MLC configurations are operated using several control techniques such as synchronous reference frame (SRF) control for grid-connected and standalone systems. A multifunctional control is implemented for CHB multilevel topology in [14]. The current reference control is implemented for standalone and grid-connected systems [15]. The active and reactive power (PQ) control is implemented for MLCs. Within control schemes, modulation techniques based on level shift and phase shift of carrier are employed. The optimization techniques are implemented for optimal switching angles for selective harmonic elimination (SHE) [16]. The fundamental frequency approach is implemented in MLCs for higher levels [17]. Moreover, hybrid carrier PWM techniques for improving power quality are being proposed. The PWM techniques are used in [18] for balanced power distribution in MLCs. The PWM modulator, controller and optimized configuration are main parts of MLCs. In this paper, two PUCs are cascaded to attain 25 levels in output voltage using six switches in each PUC. The modes of operations and switching states are presented. The converter is tested in standalone and grid-connected mode with current reference unit template control for single-phase applications. The CPUC based MLC is presented with reduced switch count for twenty-five level MLC. This topology is compared with conventional MLCs and makes it a better contender for practical applications. The maximum 25 levels are attained at low switching frequency with a binary-quintuple based approach for selection of voltages. The cascaded converter is tested, and results are validated using OPAL-RT [19-20]. Moreover, a comparison with other topologies is presented with relevant parameters [21]-[27].

II. Cascaded Packed U Cell Converter

The CPUC converter consists of two five-level PUC cells connected in a cascaded manner, as shown in Fig. 1. Each cell contains six switches, one DC voltage source, and a capacitor. The converter switches states are formed with twelve positive levels, one zero level and negative levels are shown in Table I. CPUC forms twenty-five level in output voltage by the addition of converter I and converter II voltages. The sign convention of converter voltages depends on the direction of grid current, which is assumed going into the grid voltage source. CPUC is divided into six sections connected appropriately for level generating modes. Each section has two switches in an antiparallel configuration. The interfacing inductance is designed according to permissible harmonic current injection in the grid. The switches S_{1c}- S_{6c} are complementary for S_1- S_6.

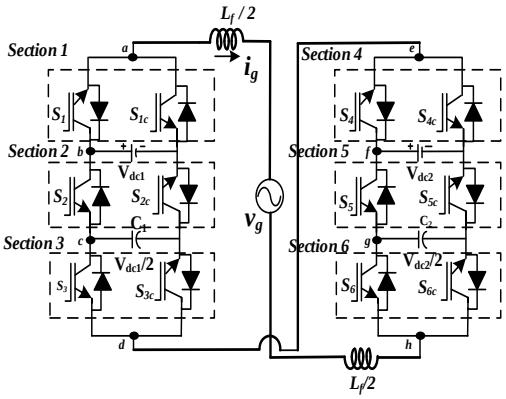

Fig.1 System Configuration of CPUC

A. Modes of Operation

The modes of operation are formed based on the combination of switches of Converter I and Converter II. The nine modes of operation out of 25 states are divided into three parts, as shown in Figs. 2-4. Fig. 2 (a) shows state zero voltage source and capacitor are not part of the circuit, and zero levels are attained. Fig. 2 (b) shows state N_1 where current flows through the capacitor and DC voltage source of first PUC converter with converter voltage of $-V_{dc1}+V_{dc1/2}$. Similarly, Fig. 2(c) discuses mode of operation for state N_4, where S_{1c}, S_2, S_{3c}, S_4, S_{5c}, and S_6 are turned ON.

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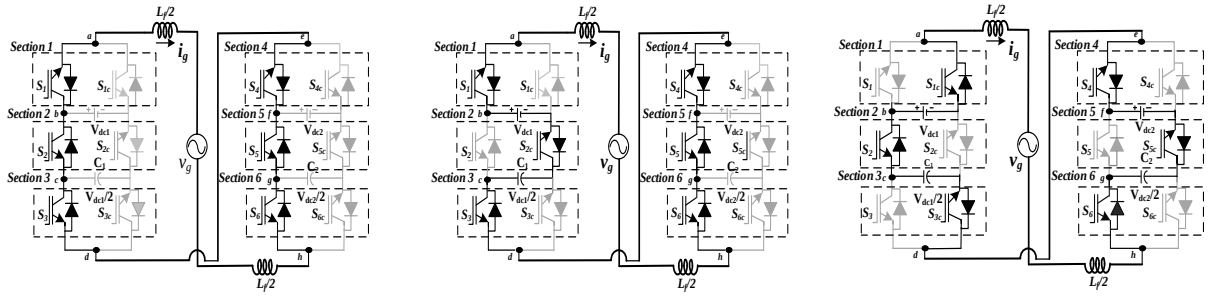
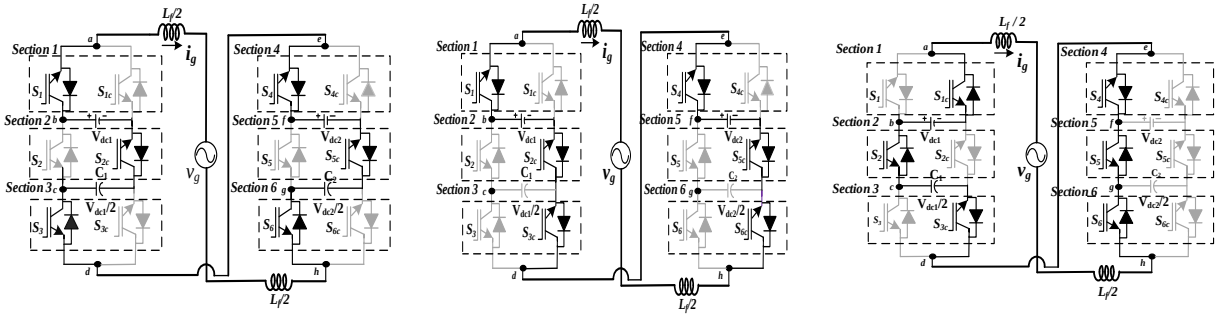


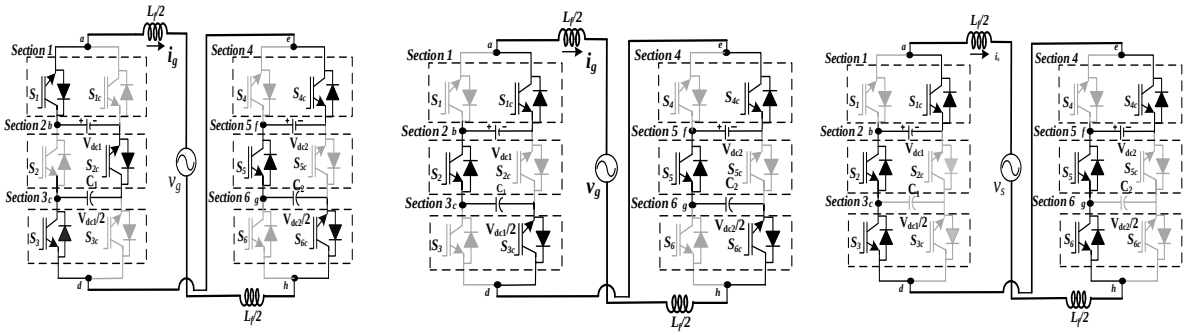
(a) (b) (c)

Fig.2 Operating modes of CPUC Part I (a) State Z Mode (b) State N_1 Mode (c) State N_4 Mode



(a) (b) (c)

Fig.3 Operating modes of CPUC Part II (a) State N_6 Mode (b) State N_{12} Mode (c) State P_1 Mode



(a) (b) (c)

Fig.4 Operating Modes of CPUC Part III (a) State P_4 Mode (b) State P_6 Mode (c) State P_{12} Mode

Figs. 3 (a)-(b) show operating modes for middle negative state N_6 and highest negative level N_{12}. Fig. 3 (c) shows the first positive level P_1 where the current forms path through capacitor C_1 moving up through the first DC voltage source. The part III of operating mode discusses state P_4, P_6 and P_{12} as shown in Figs. 4 (a)-(c). The positive middle level is shown in Fig. 4(b) and the highest positive level is in state P_{12}. The modes of operation validate function and development of states.

The selection of CPUC voltage sources is such that the grid voltage of 325 $V_{p\text{-}p}$ is achieved. The interfacing inductor reduces the instantaneous error between each level of converter voltage and improves grid current harmonics.

B. Mathematical Model

The switching function of CPUC is defined as,

$$S_w = \begin{cases} 0, \text{ when } S_n \text{ is OFF} \\ 1, \text{ when } S_n \text{ is ON} \end{cases} \tag{1}$$

where n=12 for this converter. The complementary equation for each section switches in CPUC is given as,

$$S_n + S_{nc} = 1 \tag{2}$$

Each section works in complementary mode, and the current of each section contributes to the total current fed to load/grid. The load/grid current is related to each section current. The grid current having relation with non-complementary switches is given as,

$$i_g = \frac{i_n}{S_n} \tag{3}$$

The DC link voltages with switching functions are related as,

$$\begin{cases} v_{ab} = (S_1 - 1)/V_{dc1} \\ v_{bc} = (1 - S_2)/(V_{dc1} - V_{dc1}/2) \\ v_{cd} = (1 - S_3)(V_{dc1}/2) \\ v_{ef} = (S_4 - 1)(V_{dc2}) \\ v_{fg} = (1 - S_5)/(V_{dc2} - V_{dc2}/2) \\ v_{gh} = (1 - S_6)(V_{dc2}/2) \end{cases} \tag{4}$$

The total output voltage of the converter becomes,

$$V_{mli} = v_{ab} + v_{bc} + v_{cd} + v_{ef} + v_{fg} + v_{gh} \tag{5}$$

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TABLE I
MODES OF OPERATION

Levels	S_1, S_2, S_3, S_4, S_5, S_6	Converter I	Converter II
P_{12}	011011	V_{dc1}	V_{dc2}
P_{11}	010011	V_{dc1}-$V_{dc1}/2$	V_{dc2}
P_{10}	111011	0	V_{dc2}
P_9	101011	-V_{dc1}+$V_{dc1}/2$	V_{dc2}
P_8	100011	-V_{dc1}	V_{dc2}
P_7	011010	V_{dc1}	V_{dc2}-$V_{dc2}/2$
P_6	010010	V_{dc1}-$V_{dc1}/2$	V_{dc2}-$V_{dc2}/2$
P_5	111010	0	V_{dc2}-$V_{dc2}/2$
P_4	101010	-V_{dc1}+$V_{dc1}/2$	V_{dc2}-$V_{dc2}/2$
P_3	100010	-V_{dc1}	V_{dc2}-$V_{dc2}/2$
P_2	100111	V_{dc1}	0
P_1	010111	V_{dc1}-$V_{dc1}/2$	0
Z	111111	0	0
N_1	101111	-V_{dc1}+$V_{dc1}/2$	0
N_2	100111	-V_{dc1}	0
N_3	011101	V_{dc1}	-V_{dc2}+$V_{dc2}/2$
N_4	010101	V_{dc1}-$V_{dc1}/2$	-V_{dc2}+$V_{dc2}/2$
N_5	111101	0	-V_{dc2}+$V_{dc2}/2$
N_6	101101	-V_{dc1}+$V_{dc1}/2$	-V_{dc2}+$V_{dc2}/2$
N_7	100101	-V_{dc1}	-V_{dc2}+$V_{dc2}/2$
N_8	011100	V_{dc1}	-V_{dc2}
N_9	010100	V_{dc1}-$V_{dc1}/2$	-V_{dc2}
N_{10}	111100	0	-V_{dc2}
N_{11}	101100	-V_{dc1}+$V_{dc1}/2$	-V_{dc2}
N_{12}	100100	-V_{dc1}	-V_{dc2}

In this configuration, total output levels are the multiplication of level obtained from each cell. The generalized expression of the total number of levels is as,

$$T_L = L^N \tag{6}$$

In this configuration, L is taken as 5 and N is selected as 2 to generate twenty-five levels. For example, 125 levels are to be obtained using 5 level PUC cells. The value of N is 3 from (6), which shows that only 3 PUC cells are enough to attain 125 levels in the output voltage. It is possible due to the asymmetric selection of voltages within and among the cascaded cells. The voltage equations for capacitors are given as,

$$\begin{cases} V_{c1} = \frac{1}{C_1}\int [S_3 - S_2] i_g \\ V_{c2} = \frac{1}{C_2}\int [S_6 - S_5] i_g \end{cases} \tag{7}$$

From (7), capacitor currents are given as,

$$\begin{cases} i_{c1} = [S_3 - S_2] i_g \\ i_{c2} = [S_6 - S_5] i_g \end{cases} \tag{8}$$

Similarly, load current equations can be formulated in terms of switching function and capacitors. Kirchhoff's voltage law gives the equation for both grid-connected and standalone mode as,

$$\begin{aligned} -V_{mli} + \left\{ R_p i_g + \left(\frac{L_f}{2}\right)\frac{di_g}{dt} \right\} + v_g + \left\{ R_p i_g + \left(\frac{L_f}{2}\right)\frac{di_g}{dt} \right\} = 0 \\ -V_{mli} + \left\{ R_p i_L + \left(\frac{L_f}{2}\right)\frac{di_L}{dt} \right\} + v_L + \left\{ R_p i_g + \left(\frac{L_f}{2}\right)\frac{di_L}{dt} \right\} = 0 \end{aligned} \tag{9}$$

Rearranging terms of (9) one has,

$$\begin{aligned} V_{mli} - v_g = \left\{ 2R_p i_g + \left(L_f\right)\frac{di_g}{dt} \right\} \\ V_{mli} - v_L = \left\{ 2R_p i_L + \left(L_f\right)\frac{di_L}{dt} \right\} \end{aligned} \tag{10}$$

The parasitic resistance is neglected, and (10) is made simpler for further analysis.

C. Binary-Quintuple Progression Scheme

The level formation solely depends on the selection of voltage sources. The binary and quintuple progressions are integrated together in the proposed scheme to obtain 25 levels in output voltage, as shown in Fig. 5. The cell of CPUC has different ratios within the cell and between one another. The base 2 system is considered as binary and used to select the magnitude of voltage inside each cell of PUC. The ratio of binary is selected between DC voltage source, and capacitor voltage of first PUC cell. Similarly, DC voltage source is twice of capacitor voltage of the second PUC cell. Moreover, the base 5 system has been taken between the first and second PUC being cascaded. The base 5 system is termed as quintuple, where the DC voltage source of converter II is five times of Converter I. Furthermore, the ration between capacitor voltage of converter I and converter II are selected as 1:5. The appropriate selection of voltages has led to the generation of twenty-five level converter output voltage. PUC cell I and PUC cell 2 are converters that aids in level formation from cascaded topology.

III. CONTROL METHODOLOGY

The grid-connected current reference controller for CPUC is shown in Fig. 6. The same controller with modification is implemented for standalone operation. The controller is designed for feeding the desired current reference in the AC grid. The parameters for CPUC are shown in Table II, and comparative analysis of device count is given in Table III.

A. Standalone Operation

The standalone mode of operation is analyzed with the help of an *R-L* load. The DC source feeds *R-L* Load, and such a system has a vast potential in uninterrupted power supplies. The same controller is designated, but PLL is not sensed from the load voltage. A unit sine wave block is used for the generation of the unit template to avoid the effect of load disturbances on the controller. The load current is drawn from the DC side as per load demand.

B. Grid-Connected Operation

The grid-connected controller senses the grid voltage, and the signal is fed to PLL. The active and reactive power transfers are ensured with the help of the addition of phase delay in θ. In the

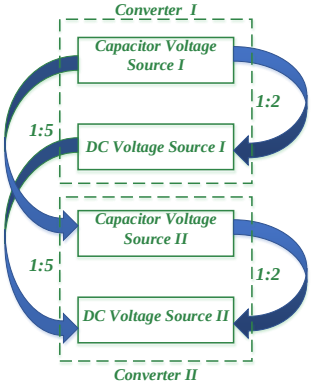

Fig.5 Representation of Binary-Quintuple scheme

TABLE II
SYSTEM PARAMETERS

Parameters	Values
Grid Voltage (v_s)	325 V_{p-p}
Grid Frequency (f_s)	50 Hz
Grid Inductor (L_f)	4 mH
DC Voltage Source I (V_{dc1})	54 V
Capacitor I Voltage (V_{c1})	27 V
DC Voltage Source II (V_{dc2})	270 V
Capacitor II Voltage (V_{c2})	135 V
R-L Load	60 Ω, 80 mH

absence of PV source, the reference DC component is injected in a grid-connected system. The first DC voltage source is halved and used as a reference signal for a capacitor of converter I. The voltage of the capacitor is sensed and balanced using proportional-integral (PI) controller. The balancing control for the converter I capacitor is given as,

$$I_{d1} = I_{d1}(g-1) + k_{p1}\{e_{r1}(g) - e_{r1}(g-1)\} + k_{i1}e_{r1}(g) \quad (11)$$

where,

$$e_{r1} = V^{*}_{c1} - V_{c1} \quad (12)$$

The PI controller minimizes the error e_{r1} between desired and sensed capacitor voltages. Similarly, the output of the PI controller for capacitor voltage balance of converter II is as,

$$I_{d2} = I_{d2}(g-1) + k_{p2}\{e_{r2}(g) - e_{r2}(g-1)\} + k_{i2}e_{r2}(g) \quad (13)$$

where,

$$e_{r2} = V^{*}_{c2} - V_{c2} \quad (14)$$

The modulating signal is generated, and control output for the same is given as,

$$v_{ref} = v_{ref}(g-1) + k_{p3}\{e_{ref}(g) - e_{ref}(g-1)\} + k_{i3}e_{ref}(g) \quad (15)$$

where,

$$e_{ref} = i_{gref} - i_g \quad (16)$$

Nearest level modulation technique (NLMT) is implemented, and its flow chart is shown in Fig. 7. This technique switches IGBTs at fundamental switching and is more efficient. CPUC operation depends on the switching of devices, and the modulation scheme decides the efficiency of the system on a large scale. Therefore, the approach taken is a fundamental switching frequency to avoid higher losses in high frequency-based switching. The switching losses are expressed as the sum of IGBTs turn ON and turn OFF losses. In this modulation strategy, the round function is used to find the nearest voltage level. A new convention is added that round "3.5" is taken as "4" to avoid ambiguity for half integers. The PUC cells are calculated by taking log on both sides of (6) as,

$$N = \log_L(T_L) \quad (17)$$

Moreover,

$$M = 0.5 * (T_L - 1) \quad (18)$$

The total number of positive levels are obtained using (18). The calculated value 12 is used to obtain the predefined level. The quotient k is calculated using the modulated signal and P_L. The L_n function is compared with integer values for switching the CPUC cells. The obtained gate pulses are given to switches of converters I and II.

IV. OBSERVED RESULTS AND DISCUSSION

The CPUC is modeled in MATLAB/Simulink, and results are tested through OPAL-RT test bench. The test bench uses a plant and controller in OPAL-RT stacks. The rapid prototyping function of real-time simulators enables fast hardware synchronization. The OPAL-RT test bench with two stacks OP5700/OP5607 and host PCs are used. The digital and analog signals are processed in a loop using digital out (DO), digital in (DI), analog out (AO) and analog in (AI) ports.

A. Simulation Results

Fig. 8 (a) shows results of standalone mode when R-L Load is connected at converter output terminals. The load voltage and load current is in the same phase. A lagging nature is load current is observed due to load inductance. The converter voltage remains constant and has 25 levels. The cell voltages of converter I and II are shown. Both cell voltages of each PUC cells add up to form 25 level MLC. Fig. 8 (b) shows a grid-connected mode where the grid-current reference is injected in control to feed current into the grid. The DC voltage source acts as a battery feeding power to the grid. The grid current and grid voltage are in phase opposition, which signifies that power is fed into the grid. Moreover, the grid-current reference is changed from 10 A to 15 A for dynamic performance. The increase in grid current and a decrease in grid current reference, as shown in Figs. 9 (a)-(b). The capacitor voltages remain balanced at the dynamic state. The 25-level output voltage remains unaffected under sudden variation of grid current reference.

B. Test Results

Figs. 10-14 show test results of CPUC for standalone and grid-connected operations. Fig. 10 shows are switching pulses, for the converter I and II. The switching pulses of switches in sections I and II of the first PUC cell are shown in Fig. 10 (a). Section III and Section IV pulses are shown in Fig. 10 (b). The pulses of Section V and VI are shown in Fig. 10 (c). The switching pulses in test results are complementary to its non-complementary switch. The standalone operation at a fixed R-L load is shown in Fig. 11(a). Moreover, the converter voltage having 25 levels is obtained at the steady-state condition. The load current lags behind the load voltage and capacitor voltages are also balanced for the standalone mode of operation. Figs. 11 (b)-(c) measure load voltage and load current THD, which is under 5% limit of the IEEE 519 standard.

Figs. 12 (a)-(c) depict performance in the grid-connected mode for steady-state and dynamic conditions. The capacitor voltages remain constant in steady-state. The grid voltage remains constant at the peak value of 325 V. Moreover, Fig. 12 (a) shows reference DC value as injected, which results in a constant grid current of 10 A. The grid current is in phase opposition, which ensures power is being fed into the grid. The unity power factor is maintained for both dynamic and steady-state conditions. In Figs. 12 (b-c) dynamic operation, the grid-current reference is increased from 10 A to 15 A. Furthermore, it is decreased to 10 A for the testing system at sudden changes in the grid- current reference. The controller tuning is as per minimum steady-state error between actual and reference modulating signals.

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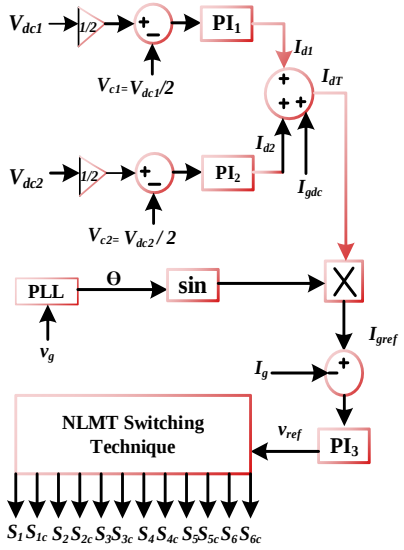


Fig.6 Current reference control for Grid-tied CPUC

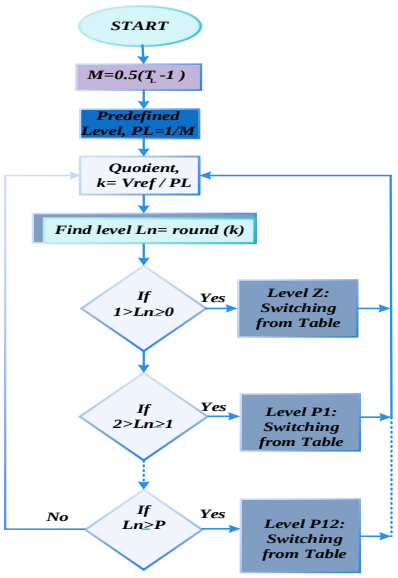
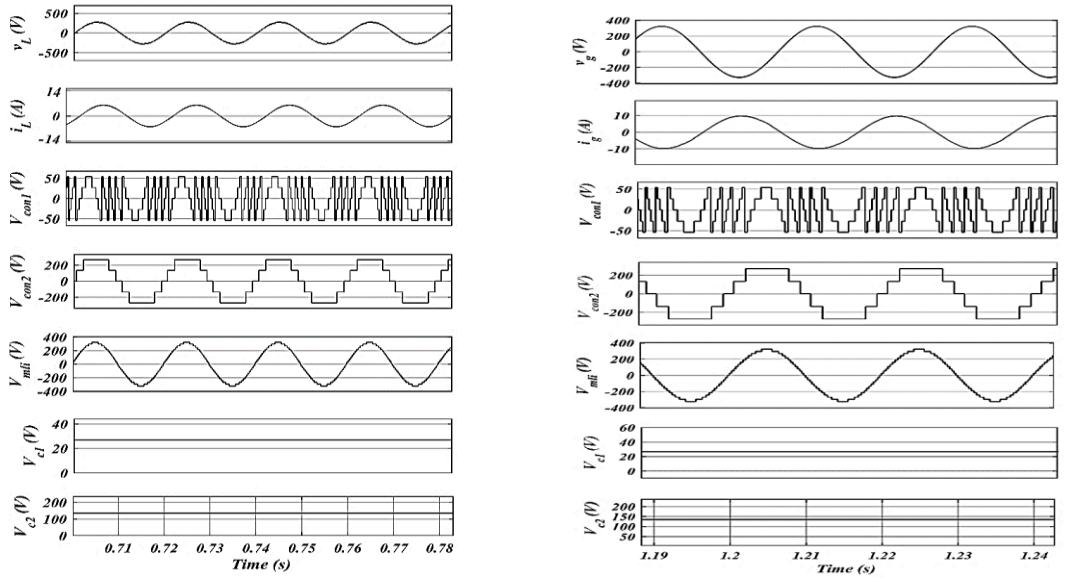
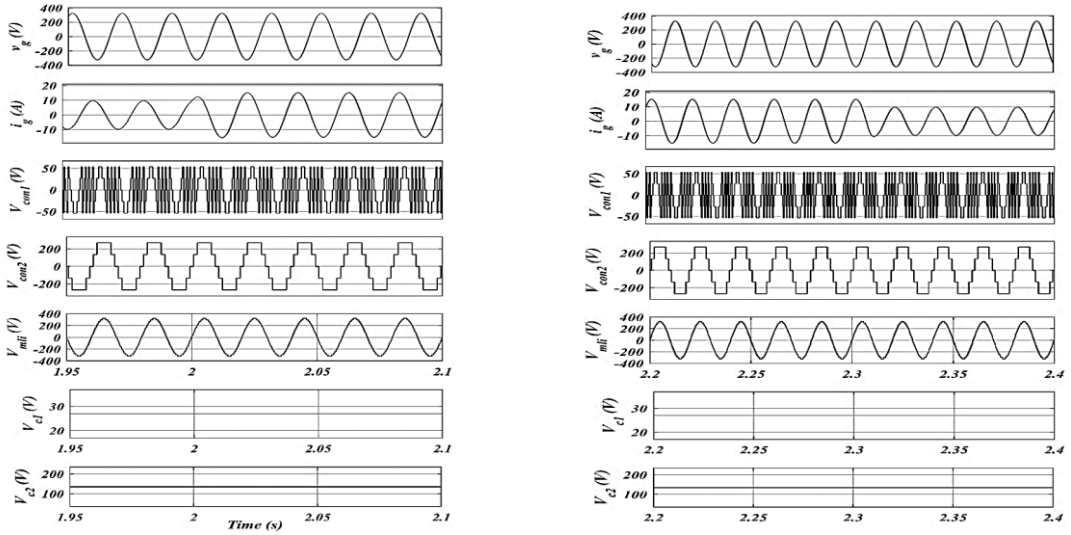


Fig.7 Nearest Level Modulation Strategy for CPUC



(a) (b)

Fig.8 Steady-state simulation results (a) Standalone Mode at fixed R-L Load (b) Grid-connected mode

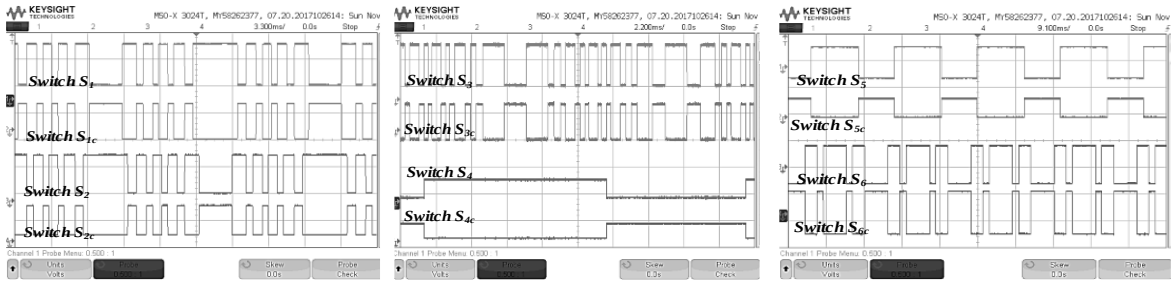


(a) (b)

Fig.9 Dynamic state simulation results (a) Increase in grid current reference (b) Decrease in grid current reference

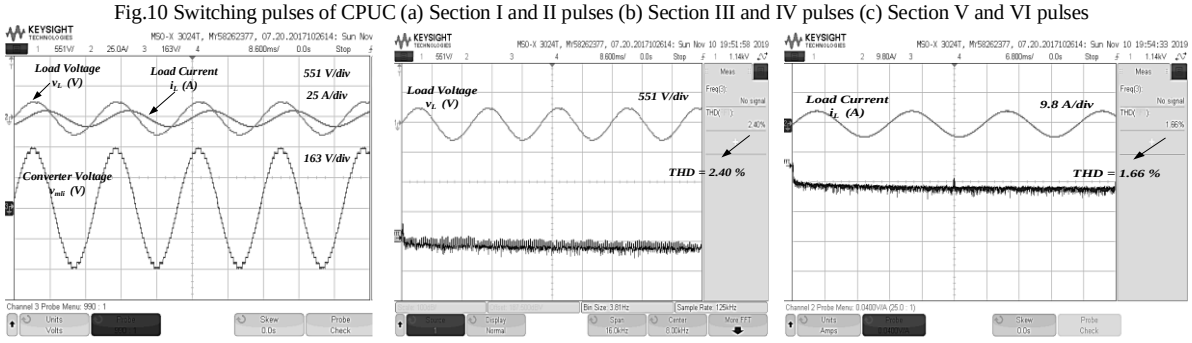
TABLE III
COMPARATIVE ANALYSIS FOR THE PROPOSED WORK

Parameters	**[20]**	**[21]**	**[22]**	**[23]**	**[24]**	**[25]**	**[26]**	**[27]**	**[7]**	**Proposed**
Number of Levels	25	25	25	25	25	25	25	27	49	25
Voltage Ratio	1:5	1:5	1:5	-	-	1:1	1:2:3:6	1:3:9	1:7	1:5
DC Sources	2	2	2	1	22	6	3	3	2	2
Switches	10	10	16	41	15	26	12	12	12	12
Diodes	8	16	0	0	11	0	0	0	0	0
Capacitors	2	4	0	12	0	12	2	0	2	2
Total Count	22	32	18	54	48	44	17	15	16	16
Modulation Technique	PWM	PWM	PWM	SHE	SHE	NLMT	PWM	PWM	PWM	NLMT
Switching Losses	Medium	High	Medium	Low	Low	Low	High	High	High	**Low**
Efficiency	Good	Poor	Good	Good	Good	Good	Good	Good	Good	Very Good
Capacitor Balancing	Natural	Natural	-	Natural	-	Auxiliary Devices	PWM	-	PI Control	PI Control
Control Complexity	Medium	Medium	Low	Medium	Medium	High	Low	Low	Simple	Simple
Unequal Power Distribution	Medium	Medium	Medium	-	-	-	High	High	High	Medium
Thermal Stress	Low	Medium	Medium	Low	Low	Low	High	High	High	Low
Harmonic Performance	Good	Good	Good	Good	Good	Good	Good	Good	Very Good	Good
Thermal Design Cost	Low	Medium	Medium	Low	Low	Low	High	High	High	Low
Drivers and Component Cost	Medium	High	Low	High	High	High	Low	Low	Low	Low



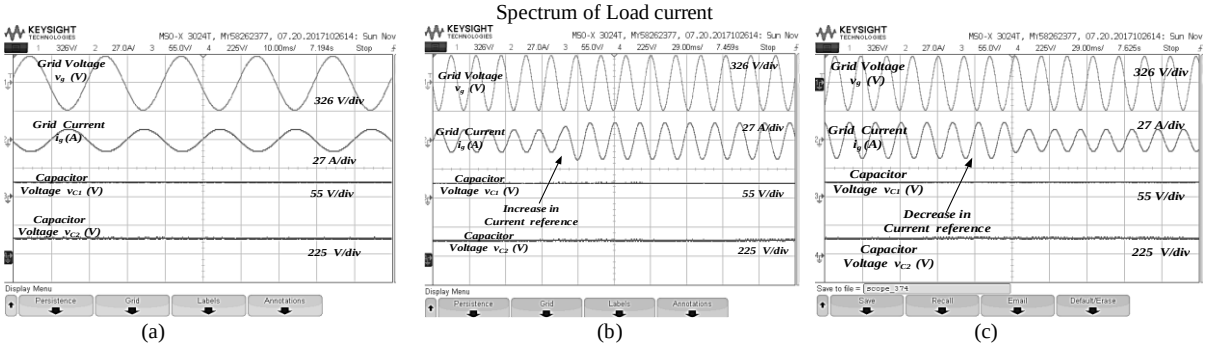
(a) (b) (c)

Fig.10 Switching pulses of CPUC (a) Section I and II pulses (b) Section III and IV pulses (c) Section V and VI pulses



(a) (b) (c)

Fig.11 Standalone Mode of Operation at fixed R-L Load (a) Load voltage, load current and MLC voltage (b) Harmonics Spectrum of Load voltage, (c) Harmonics Spectrum of Load current



(a) (b) (c)

Fig.12 Grid Connected Mode of Operation (a) Steady-state Operation at fixed grid current reference (**b)** Dynamic state with an increase in grid current reference **(c**) Dynamic state with the decrease in grid current reference.

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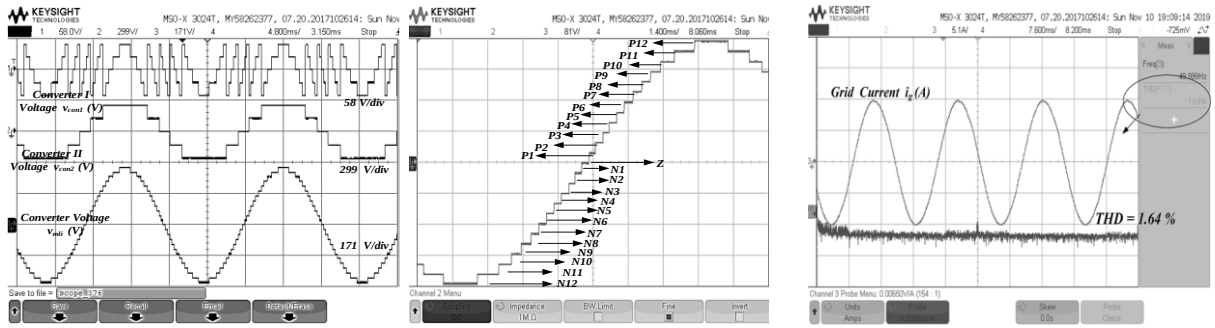

(a) (b) (c)

Fig.13 Converter cell voltages and Harmonic performance (a) Converter I, Converter II and MLI Voltage (**b)** Zoomed View of Converter Voltage, **(c**) Harmonic performance of grid current

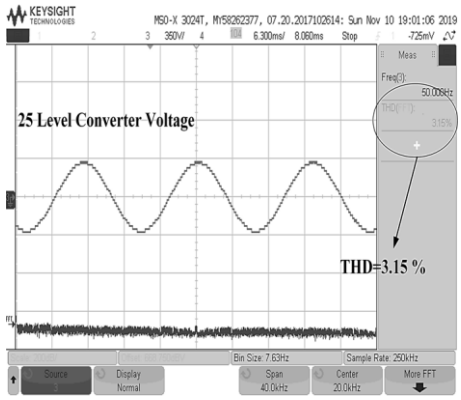

Fig.14 Harmonic performance of converter voltage

Fig. 13 (a) shows the stepped voltage waveform of each PUC cell. Both cell voltages add up to form a 25 level synthesized waveform. Figs. 13 (b)-(c) show a zoomed view of the converter voltage and harmonics analysis of the grid current THD, which is 1.64%. Fig. 14 shows the converter output AC voltage, which has a THD of 3.15% and it meets the IEEE 519 standard. Test results validate cascaded packed U cell-based multilevel converter for grid-tied and standalone applications.

V. CONCLUSIONS

A reduced switch count CPUC is implemented in this work for 25-levels output voltage. The binary quintuple progression scheme is used for the selection of voltages. The capacitor balancing is achieved under standalone as well as the grid-connected operation. The active power is fed into the grid seamlessly, and converter is switched at fundamental frequency using the NLM strategy. The comparative analysis shows that the proposed progression scheme provide a cost effective multilevel converter in terms of cost, reliability, power quality and system efficiency. The detailed comparison has shown the effectiveness of CPUC multilevel converter over other available topologies. The number of levels attained in CPUC is significantly increased. Furthermore, the power quality is improved as THD remains under permissible limits. OPAL-RT test results show the feasibility of this system for standalone and grid-connected applications.

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