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Integrating 10kV SiC MOSFET into Battery Energy Storage System with A Scalable Converter-based Self-powered Gate Driver

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***Abstract*- In the hardware design of Battery Energy Storage System (BESS) interface, in order to meet the high voltage requirement of grid side, integrating 10 kV Silicon-Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) into the interface could simplify the topology by reducing the component count. However, the conventional gate driver design is challenging and inextensible in BESS, since the high voltage rating and high *dv/dt* bring the requirements of high voltage isolation and low common-mode capacitance. Therefore, in this paper, a scalable converter-based self-powered (SCS) gate driver is further proposed. A 5 kV-input power extracting converter based on a voltage-balanced SiC MOSFET stack is constructed to self-power the gate driver, which exhibits simplification of basic topology and sufficient gate driver power handling capability regardless of the switching requirement of main loop power device. Besides this, the power extracting converter is designed to act as a clamping Resistor-Capacitor-Diode (RCD) snubber circuit, which makes the SCS gate driver scalable to the series connection of power devices. Analysis and design consideration are given in detail, followed by the experimental verification using 10 kV/10 A SiC MOSFETs.**

Keywords— SiC MOSFET; Battery Energy Storage System (BESS); self-powered gate driver; series connected

I. Introduction

The increasing penetration of renewable energy sources and associated power electronics interfaces contributes to fabricating a decarbonized distribution grid. However, in the meantime, they also bring instability due to the feature of intermittence. Consequently, as an effective way to compensate, Battery Energy Storage Systems (BESSs) come along [1].

Taking the configuration of Solid State Transformer (SST) with BESS as an example, which was preserved in [2], SST is applied as the interconnection of two Medium-Voltage (MV) DC grids, and in order to increase the stability, BESS is integrated into SST due to its superior energy management capability. In this BESS, the voltage rating of its DC grid side is high, and thus multiple series connected Insulated Gate Bipolar Transistors (IGBTs) are generally adopted as a single switch for meeting the voltage rating requirement. In this way, two challenges are encountered in the hardware design: (1) the difficulty of voltage balancing will increase as the number of series connected power devices increases; (2) the high voltage

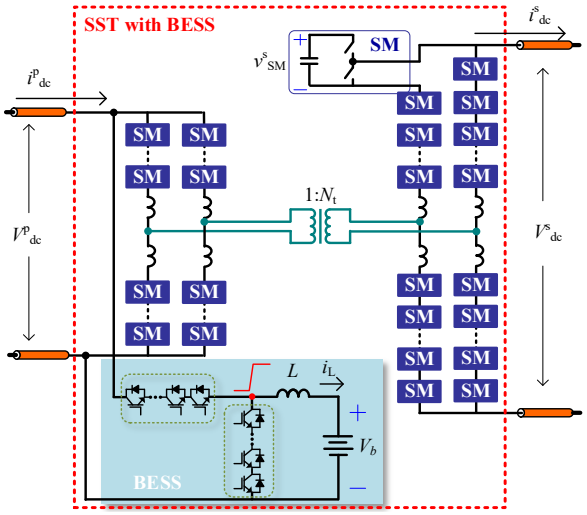

Fig. 1. Configuration of SST with BESS [2]

and the high *dv/dt* of switching node will import the challenges to the gate driver design of power device.

Nowadays, as the development of high voltage Silicon-Carbide (SiC) power devices, 10 kV SiC Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) has drawn extensive research attention due to its superior conduction and switching characteristics [3 - 6], and has become the most promising power device to replace the dominance of IGBT in MV applications. Owing to the high blocking voltage of 10 kV SiC MOSFET, the requirement of the number of series connected power devices will be greatly reduced if it is applied in BESS. Despite of this, the challenges of the high voltage and high *dv/dt* to the gate driver design still exist. In the conventional way, the "external-powered" gate driver is equipped with each 10 kV SiC MOSFET, where the gate driver is powered by a grounded external power supply. Therefore, many papers focus on improving the transformer design of isolated power supply on the gate driver [7 - 15], based on two requirements: (1) high voltage isolation from DC grid voltage to ground; (2) low parasitic capacitance to attenuate the Common Mode (CM) current induced by high *dv/dt*. Those designs result in increased difficulty in terms of designing and manufacturing, besides, they are not suitable for an extension of more levels or more series connected devices to obtain a higher blocking voltage.

Comparatively, it would be advantageous if 10 kV SiC

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MOSFET, its gate driver and corresponding power supply are combined in one single unit, which requires the power supply to extract the power from the main loop directly. In this way, the isolation burden of gate driver design can be eased significantly, and the CM current path to the ground is disabled. Besides, since the external power source is avoided, it is suitable for the extended design. Such a concept is called "self-powered", and has only yet been realized in several ways for thyristors, lower voltage MOSFETs and IGBTs. In [16, 17], a modified snubber circuit provides the power for the gate driver, which behaves like a linear regulator, but low-efficiency is the biggest drawback. In [18 - 20], in order to improve the efficiency, resonant circuits are additionally equipped to accumulate more power for the gate driver. It takes the advantages of the dynamic switching characteristic of power device, but also increases the loss of power device meanwhile. In [21, 22], auxiliary circuits using additional transistors are designed for the same purpose. However, if a higher quiescent power is required in advanced gate drivers nowadays, they are not suitable since they could only provide limited quiescent power. In [23], a two-stage converter is connected in series with the RC snubber circuit of the gate-commutated thyristor (GCT) to power its gate driver. Although there are also no dynamic current pulses to charge the supply during the quiescent state of GCT, the static snubber current with fundamental frequency and low magnitude will charge the supply since it is specifically developed for current source rectifiers. In [24], a promising floating supply system is proposed. By placing a commercial DC/DC converter together with a clamping snubber circuit across each IGBT, it can provide sufficient driving power. However, the constant-power-load characteristic could cause the static voltage unbalancing in series connection applications, which means the scalability is limited and requires additional auxiliary circuits together with the modulation algorithm to compensate it.

As for 10 kV SiC MOSFET, its "self-powered" gate driver design remains unsolved since the 10 kV SiC MOSFET gate drivers in previous publications are all based on the "external-powered" concept. In addition, the existing "self-powered" schemes for lower voltage MOSFETs or IGBTs are no longer suitable for 10 kV SiC MOSFET, since the higher input voltage makes the auxiliary circuit design more difficult. Consequently, the contribution of this paper is the design and consideration of a scalable converter-based self-powered (SCS) gate driver for 10 kV SiC MOSFET in BESS, which mainly involves the necessary improved design of power extracting converter and the scalability optimization for series connection:

- A 5 kV-input power extracting converter is required considering an operating margin of 10 kV SiC MOSFET, making commercial DC/DC converters that can satisfy the design requirement hardly available. Hence, a voltage-balanced SiC MOSFET stack-based modified Flyback topology is proposed to construct such a high-voltage step-down converter.
- The power extracting converter is designed to behave as a clamping Resistor-Capacitor-Diode (RCD) snubber, which makes the modulation control and additional static voltage balancing circuits in [24] unnecessary.

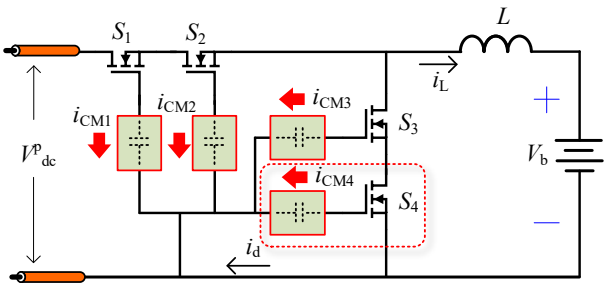

Fig. 2. Bidirectional dc/dc converter in BESS

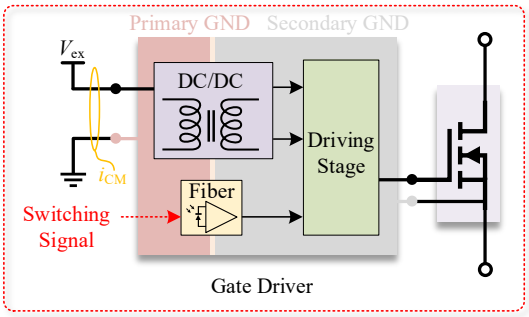

Fig. 3. The gate driver design in a conventional way

Remaining sections of this paper is organized as follows. In Section II, the CM noise is analyzed in running BESS to illustrate the benefit of self-powered gate driver. In Section III, the BESS configuration using 10 kV SiC MOSFETs with proposed SCS gate drivers is presented. In Section IV, the detailed design and consideration regarding of the parasitic capacitance and insulation are analyzed, followed by the experimental verification using a double pulse testing platform in Section V. Finally, the conclusion is given in Section VI.

II. CM Noise Analysis of Running BESS

In this configured bidirectional DC/DC converter in BESS, as shown in Fig. 2, with a targeted DC bus voltage rating V^{P}_{dc} of 10 kV on the MV side, two series-connected 10 kV/10 A SiC MOSFETs S_1 and S_2 are chosen and treated as one single switch of high side considering the design margin. Correspondingly, another two series-connected ones S_3 and S_4 are configured as the single switch of low side. A large inductor L is connected in the power loop, which is then interfaced to the battery V_b.

As for the key gate driver part, as mentioned, the gate drivers of S_i (i=1 - 4) are powered by a common external power supply V_{ex} in the conventional way, and the architecture is drawn in Fig. 3. In this case, when S_1 and S_2 are turned on, the voltage difference between the primary and secondary sides of gate driver reaches V^{P}_{dc}. Therefore, the power and signal stages of the gate driver unit need to

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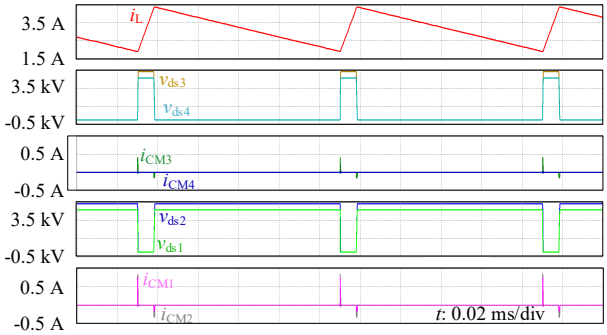

Fig. 4. Simulated waveforms of running BESS

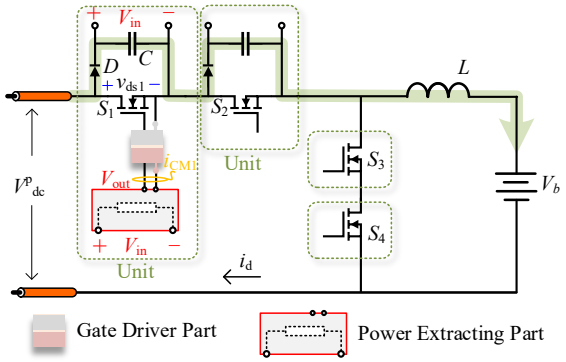

Fig. 5. 10 kV SiC MOSFET based BESS with proposed SCS gate drivers

be isolated to separate the primary ground and the secondary ground referred as the switching node potential, with desired voltage rating. In addition, both of them still contribute to CM noise due to the presence of parasitic capacitances between the primary side and the secondary side. The parasitic capacitance for signal isolation stage could be ignored in case the fiber connector is applied, and thus the major concern is the parasitic capacitance of isolated power supply.

When BESS is running, taking the charging process from DC bus to battery as an example, the bidirectional dc/dc converter behaves as a buck converter. During the switching transients of S_1 and S_2, the voltage potentials at switching nodes experience a high *dv/dt*, which can be considered as noise sources, and that is the origin of emerging CM currents. In order to illustrate the phenomenon clearly, a simulation in LTspice is implemented to help understand the CM noise.

The parameters V^{P}_{dc} = 10 kV, V_b = 800 V and L = 30 mH are chosen. In addition, the LTspice model of 10 kV SiC MOSFET is adopted, which was developed and validated in [25], and the parasitic capacitance of gate driver is 15pF as referencing to the advanced commercial isolation power supply in [26]. It is noticed that, although such an isolated power supply is just recommended for low voltage SiC MOSFET, it becomes applicable for 10 kV SiC MOSFET with the proposed "self-powered" gate driver design, which will be illustrated in the next section. However, in the present case, it is configured in the "external-powered" way as a basis for analysis.

Based on this, the simulation is performed in Fig. 4. It is observed that, as the load current i_L rises and falls, the CM current i_{CMi} (i = 1 - 4) flows through the corresponding gate driver of S_i (i = 1 - 4) during the switching transient. i_{CM2} is largest since the highest *dv/dt* stress appears at the middle point, followed by i_{CM1} and i_{CM3}, while i_{CM4} is always zero. Such CM currents need to be attenuated since they will disturb the control signals on the gate drivers. In severe case, they could cause the break-down of gate drivers and the driven power devices. In addition, in order to observe the influence of i_{CMi} to voltage balancing, the difference of S_i is ignored in this simulation by using the same model and same driving parameters. Therefore, it is also shown that the voltage sharing of the drain-source voltages v_{dsi} of S_i. Obviously, the difference of i_{CM1} and i_{CM2} (i_{CM3} and i_{CM4}) cause the voltage unbalancing of v_{ds1} and v_{ds2} (v_{ds3} and v_{ds4}).

In order to alleviate the negative influences caused by CM noises, the optimization of gate driver design is very important. Comparatively, using a self-powered gate driver could directly eliminate the CM noises since no external power supply is required. Besides, in this way, it is suitable for integrating 10 kV SiC MOSFET into BESS, which will be illustrated next together with the proposed SCS gate driver.

III. BESS Configuration Using 10kV SiC MOSFETs With Proposed SCS Gate Drivers

The diagram of BESS configuration using 10 kV SiC MOSFETs with proposed SCS gate drivers is shown in Fig. 5, where the clamping RCD snubber circuits are suitable to be equipped here for one existing prerequisite and one advantage, which are respectively described as follows:

(1) Due to the existence of a large inductor L in BESS, the current flowing through the diode D indicated by the green line in Fig. 5 is limited. Therefore, D would not be destroyed due to potential surge currents, for example, during the startup process [27].

(2) The snubber clamps the overvoltage of S_1 (S_2) with the aid of the clamping capacitor C, while the original switching speed is not influenced. Therefore, it helps to reduce the dynamic voltage unbalancing of S_1 and S_2, and also the transient voltage overshoot caused by the leakage inductance of the main loop. In the meantime, the resistor R together with D can achieve the goal of static voltage balancing of S_1 and S_2.

Generally, with an adopted clamping RCD snubber, the energy is primarily dissipated on the resistor. Since the snubber circuit is at the same voltage potential as the power device, the energy dissipated in the snubber resistor could be utilized to power the gate driver. Here in the proposed SCS gate driver design, the resistor R is replaced by a power extracting part, which transfers the energy from the capacitor into the gate driver regardless of the switching of power device. Therefore, sufficient quiescent and dynamic powers are provided for the gate driver without any external power supply, and the high voltage isolation design between the primary side and the

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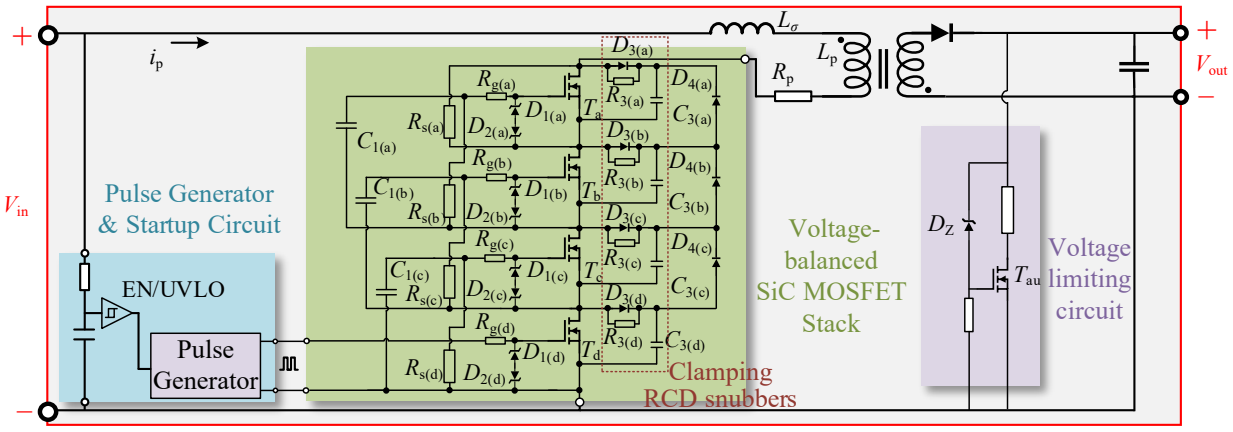

Fig. 6 Power extracting part of the SCS gate driver

secondary side of gate driver is simplified drastically, from V^{p}_{dc} to the voltage of one single unit. Besides, the CM current to the ground through gate driver is eliminated as well. Once a unit is designed, it is conductive to series connection, rather than considering a new design based on a new voltage rating.

In this SCS gate driver, the gate driver part is relatively simple to design as mentioned. Instead, such a power extracting part is rather important, since the challenges will be encountered in the designing: (1) the voltage V_{out} of gate driver power side is around 20 V while the voltage V_{in} across the capacitor could reach 5 kV for the considered target application, resulting in significantly higher voltage step-down ratio, and how to choose the appropriate topology and switching device? (2) What should be the startup sequence for this converter? (3) If this converter can operate reliably like a commercial DC/DC converter, in series connection occasions, how to solve the static voltage unbalancing problem caused by the constant-power-load characteristic?

Based on the above considerations, the power extracting part is designed as shown in Fig. 6, and the corresponding solutions are as follows:

(1) A Flyback converter is chosen as the basic topology due to its simple structure, while it is not appropriate to use a corresponding high voltage power device directly in the SCS gate driver design due to its high cost. Therefore, considering economies of scale, four series connected low-voltage/current SiC MOSFETs are applied as the main switch. Such a voltage-balanced SiC MOSFET topology combines the advantages of single gate driver and the automatic voltage balancing snubber circuit in [28], which is quite suitable in this high-voltage low-power Flyback converter design. Simple structure and low cost are the greatest features.

(2) A resistor-capacitor branch with a large resistance is applied to accumulate energy into the capacitor. With the hysteresis function of enabling and disabling, the energy in the capacitor is enough to provide the startup power of the Flyback converter. And the detail will be given in Section IV.

(3) Instead of using closed-loop control for the Flyback converter, an open-loop control is designed. Using a fixed pulse generator to control the switching of SiC MOSFET stack, the output voltage is regulated by a voltage limiting circuit. In this way, it will not have a constant-load-power characteristic, and behave just like a pure resistor. Therefore, it will not cause the static voltage unbalancing.

In order to make it clear that the power extracting converter act like a clamping RCD snubber, the analysis is given as follows, accompanied with the working principle of the voltage-balanced SiC MOSFET stack.

A. Working principle of the voltage-balanced SiC MOSFET stack

Four series connected SiC MOSFETs in this power extracting part are named from T_a to T_d. Only the bottom one requires a gate driver, and the upper ones are driven by coupling capacitor $C_{1(i)}$ (i = a~ c). $R_{s(i)}$ (i = a~ d) is static voltage-balancing resistor. $R_{g(i)}$ (I = a~ d) is gate resistor. Zener diodes $D_{1(i)}$, $D_{2(i)}$ (i = a~ d) are for gate protection. The transient voltage balancing of series connected SiC MOSFETs is achieved by clamping RCD snubbers $R_{3(i)}$, $C_{3(i)}$, $D_{3(i)}$ (i = a~ d), as shown in the dashed part in Fig. 6. In order to obtain a better voltage balancing effect, diodes $D_{4(i)}$ (i = a~ c) between snubber capacitors for automatic balancing in [28] could be applied directly, which benefits from the single gate driver design and will be explained later.

The working principle begins with turn-on transient, followed by on state, turn-off transient, and off state. The corresponding simplified circuits with key components are shown in Fig. 7, and summarized below:

(a) Turn-on transient: since the power extracting part provides small power, discontinuous current mode (DCM) is the basic working mode, which means that the current i_s flowing through the secondary windings of the transformer will drop to zero before turn-on of the primary side switch. It is a natural zero-current turn-on condition, and provides a good basis for the application of single gate driver.

The pulse generator outputs negative voltage V_{ee}, and T_d together with T_a, T_b and T_c is in off state. As a turn-on signal received, the gate current loop of T_d is formed, and

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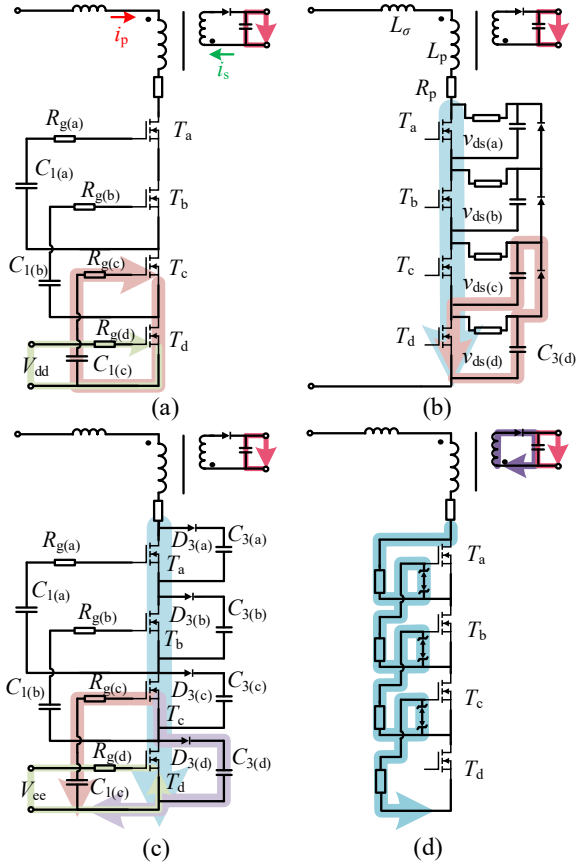

Fig. 7. States of power extracting part: (a) turn-on transient, (b) on state, (c) turn-off transient, (d) off state

its gate-source voltage starts to rise from V_{ee} to positive voltage V_{dd}, followed by the drain-source voltage $v_{ds(d)}$ of T_d to decrease, when T_d enters its miller plateau region. As $v_{ds(d)}$ decreases, the gate current loop of T_c is formed as: $C_{1(c)}$→$R_{g(c)}$→$C_{g(c)}$ (the parasitic gate capacitance of T_c) →T_d. This results in the gate-source voltage $v_{gs(c)}$ of T_c to rise, followed by decrease of its drain-source voltage $v_{ds(c)}$. After that, the turn-on switching sequences of $T_{(b)}$ and $T_{(a)}$ are similar to $T_{(c)}$. When the gate-source voltages for all series connected MOSFETs have reached expected positive values, the turn-on transient of SiC MOSFET stack is completed. It is worth noticing that, since both i_s and the primary side current i_p of Flyback transform under DCM are equal to zero during the turn-on transient, no current would flow through SiC MOSFET stack (ignoring capacitive discharging current during the turn-on transient). Consequently, severe turn-on voltage unbalancing is avoided without the need of limiting circuit.

(b) On state: Due to the design of the single gate driver, T_d is always the first one to turn on as mentioned. Similarly, T_d will be the first one to turn off as well (explained in the subsequent state (c)), consequently, $C_{3(d)}$ as the snubber capacitor stores the most energy, followed by $C_{3(c)}$, $C_{2(b)}$ and $C_{1(a)}$ in succession. During the on state of T_d, the current loop is formed: $C_{3(d)}$→$D_{4(c)}$→$C_{3(c)}$→T_d, which helps to balance the voltages of $C_{3(d)}$ and $C_{3(c)}$. Besides this, another current loop is formed: $C_{3(d)}$→$R_{3(d)}$→T_d, which helps to dissipate accumulated energy during turn-off transient. In the same manner, the voltages of $C_{3(i)}$ (i = a ~ d) are balanced and drop a small degree to be the clamping voltages at the end of the on state.

(c) Turn-off transient: Similar to turn-on transient, when the turn-off signal is received, $v_{gs(d)}$ starts to fall from V_{ee}, followed by the increasing of $v_{ds(d)}$. As $v_{ds(d)}$ increases, the voltage of $C_{1(c)}$ increases as well, which forms a current path: $C_{g(c)}$→$R_{g(c)}$→$C_{1(c)}$. Therefore, $v_{gs(c)}$ begins to fall, and then $v_{ds(c)}$ starts to increase, followed by the similar turn-off switching sequences of T_b and T_a. Finally, the turn-off transient of SiC MOSFET stack is completed. It is noticed that, without RCD snubbers, the asynchrony of $v_{ds(i)}$ (i = a ~ d) will increase, which can result in severe voltage unbalancing. Instead, with this design, $v_{ds(d)}$ is limited by $C_{3(d)}$ only when it reaches the clamping voltage of $C_{3(d)}$ and a current path is formed: T_c→$D_{3(d)}$→$C_{3(d)}$. Therefore, the voltage overshoot is absorbed by $C_{3(d)}$. $C_{3(i)}$ (i= a ~ c) plays the same role when $v_{ds(i)}$ (i= a ~ c) reaches the clamping voltage later. In this way, severe turn-off voltage unbalancing is avoided.

(d) Off state：When SiC MOSFET stack is in off state, the static voltage balancing is achieved by $R_{s(i)}$, and the current path is formed as: $R_{s(a)}$→$D_{2(a)}$→ $D_{1(a)}$→$R_{s(b)}$→$D_{2(b)}$ →$D_{1(b)}$→$R_{s(c)}$→$D_{2(c)}$→$D_{1(c)}$→$R_{s(d)}$. Therefore, the gate side voltage of T_i (i = a ~ c) is negative to ensure the reliable off of T_i, which is determined by Zener voltage of $D_{2(i)}$ (i =a ~ c) plus forward voltage of $D_{1(i)}$ (i =a ~ c).

B. RCD behavior of the power extracting part

In this modified Flyback topology, the grounds of primary and secondary windings of the transformer are connected since the power extracting part and the subsequent gate driver part share the same ground as presented in Fig. 5. In this way, the power isolation of the gate driver part is no longer needed, which makes more commercial gate driver units applicable in the proposed configuration of SCS gate driver. By defining the primary magnetic inductance, resistance and leakage inductance of the transformer respectively as L_p, R_p and L_σ, the equivalent circuit of the primary side is a LR loop, and such a relation exists:

$$V_{in} = (L_p + L_\sigma) di_p / dt + i_p R_p . \quad (1)$$

Based on (1), i_p can be calculated as:

$$i_p = \frac{V_{in}}{R_p} - \frac{V_{in}}{R_p} e^{-\frac{t}{(L_p+L_\sigma)/R_p}} . \quad (2)$$

Once the on time Δt_{on} during one switching cycle is known, the energy E_p accumulated by the transformer and the actual extracting energy E_{in} from V_{in} can be obtained as:

$$\begin{cases} E_p = 0.5 L_p i_p^{\,2} = 0.5 L_p \left(\frac{V_{in}}{R_p} - \frac{V_{in}}{R_p} e^{-\frac{\Delta t_{on}}{L_p/R_p}}\right)^2 \\ E_{in} = \frac{\Delta t_{on} V_{in}^{\,2}}{R_p} - \frac{(L_p+L_\sigma) V_{in}^{\,2}}{R_p^{\,2}} + \frac{(L_p+L_\sigma) V_{in}^{\,2}}{R_p^{\,2}} e^{-\frac{\Delta t_{on}}{(L_p+L_\sigma)/R_p}} \end{cases} . \quad (3)$$

When the SiC MOSFET stack is in reliable off state, as shown in Fig. 7(d), the stored energy E_p is released to the secondary side, so as to power the gate driver part. When

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V_{out} is larger than the setting voltage of the voltage limiting circuit, T_{au} will be turned on, which is determined by the Zener voltage V_Z of Zener diode D_Z and the threshold voltage V_{th} of the auxiliary transistor T_{au}. And thus, the extra energy will be dissipated in the voltage limiting circuit to keep V_{out} nearly unchanged.

If the switching frequency f of SiC MOSFET stack is also known, combining with (3), the power P_{out} that can be provided for the gate driver and the extracting power P_{in} from V_{in} can be expressed as:

$$\begin{cases} P_{out} = 0.5 f L_p \left(\frac{V_{in}}{R_p} - \frac{V_{in}}{R_p} e^{\frac{\Delta t_{on}}{L_p/R_p}}\right)^2 \\ P_{in} = \frac{f \Delta t_{on} V_{in}^2}{R_p} - \frac{f(L_p + L_\sigma) V_{in}^2}{R_p^2} + \frac{f(L_p + L_\sigma) V_{in}^2}{R_p^2} e^{\frac{\Delta t_{on}}{(L_p + L_\sigma)/R_p}} \end{cases} . \quad (4)$$

Therefore, according to (4), if both f and Δt_{on} are fixed, and with known values of L_p, L_σ and R_p once the transformer design is frozen, P_{in} is the same as the loss power of a pure resistor R_{eq}, which can be solved as:

$$\frac{1}{R_{eq}} = \frac{f \Delta t_{on}}{R_p} - \frac{f(L_p + L_\sigma)}{R_p^2} + \frac{f(L_p + L_\sigma)}{R_p^2} e^{\frac{\Delta t_{on}}{(L_p + L_\sigma)/R_p}} . \quad (5)$$

Consequently, the power extracting part together with the diode D and capacitor C at the front of primary stage makes the power extracting converter behave like an RCD snubber.

A conversion efficiency $\eta = P_{out}/P_{in}$ can be considered here as:

$$\eta = \frac{0.5 L_p \left(1 - e^{\frac{\Delta t_{on}}{L_p/R_p}}\right)^2}{\Delta t_{on} R_p - (L_p + L_\sigma)\left(1 - e^{\frac{\Delta t_{on}}{(L_p + L_\sigma)/R_p}}\right)} . \quad (6)$$

η represents how much of the power dissipation on the "RCD snubber" can be recycled to power the gate driver. According to the gate driver power requirement, η could be adjusted according to (6).

In summary, the proposed SCS gate driver can be combined with the power device (10 kV SiC MOSFET) as a unit. It absorbs the energy from power loop directly, then converts to power the gate driver continuously regardless of the switching of power device. Since the open-loop control design eliminates the characteristic of constant-power-load, it is scalable to the series connection of power devices.

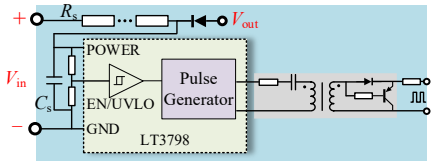

Fig. 8. Pulse generator and its startup circuit

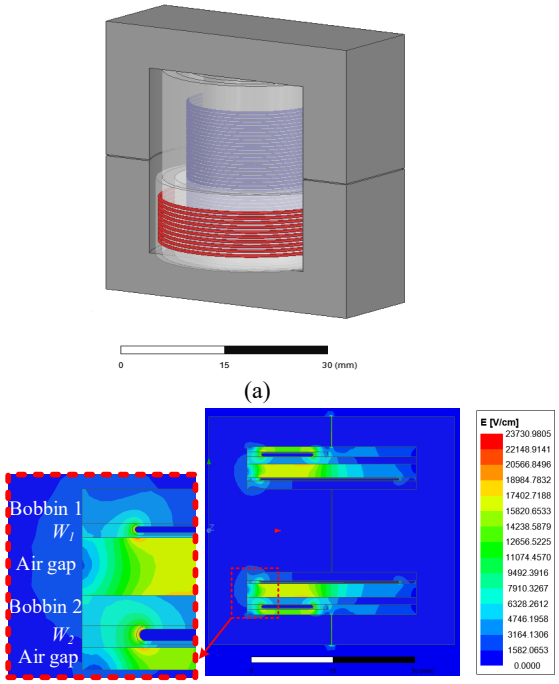

Fig. 9. (a) 3D-CAD model of custom designed transformer and (b) simulated electric field distribution within transformer using ANASYS Maxwell

TABLE I
MATERIAL PROPERTIES SETTINGS

Items	Material	Relative permittivity	Conductivity (S/m)
winding	copper	1.0	5.8×10^7
winding coat	polyamide	4.3	0
Kapton tape	polyimide	3.1	0
core	ferrite	12	0.2
bobbin		4.3	0
gap	air	1.0006	0

IV. Detailed Design and Consideration

In this Section, some important details involved in the design are considered, together with the relevant parameter selection. As mentioned in Section III, the power for startup process is provided by the capacitor in a resistor-capacitor R_sC_s branch, with the aid of hysteresis function. Defining the enabling/disabling level of hysteresis is V_p/V_n, when the voltage across C_s exceeds V_p, pulses are generated to start the power extracting part, and the provided energy E_s for startup is calculated as:

$$E_s = 0.5 C_s (V_p^2 - V_n^2) . \quad (6)$$

As the power extracting converter is started, the output voltage V_{out} feeds back to power the pulse generator, therefore, the converter enters the normal working state.

In proposed design, the pulse generator and the hysteresis function are assembled in an off-line controller, LT3798, as shown in Fig. 8. By removing its feedback circuits, LT3798 can output pulses with a fixed on-time 600 ns and a fixed frequency of 3.5 kHz. Besides, since the output high-level of the controller is just +10 V, a pulse transformer with 1:2 turns ratio is applied to shift the

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voltage level to +20 V which is recommended for SiC devices. Further, according to the known f = 3.5 kHz and Δt_{on} = 600 ns, L_p = 950 μH and R_p = 1.6 kΩ are chosen by (4) since the startup voltage $V_{in(s)}$ and required gate driver power are determined in this case.

Thanks to the voltage-balanced SiC MOSFET stack design, the induced loss by its inside components is small, as the parameters are chosen as follows: $C_{3(i)}$ (i = a ~ d) and $R_{3(i)}$ in clamping RCD snubbers are respectively 50 nF and 50 kΩ, $C_{1(i)}$ is 47 pF, and $R_{s(i)}$ is 500 kΩ.

Based on above, the voltage drop ΔV across C in Fig. 5 during the on duration of one switching cycle could be obtained by:

$$E_{in} \approx 0.5C[(V_{in(s)} + \Delta V)^2 - V_{in(s)}{}^2]. \quad (7)$$

According to (7), there is a tradeoff between C and ΔV since E_{in} is known, and 200 nF (two capacitors in parallel: FKP1Y031007J00JSC9) is chosen here to reduce the voltage ripple.

Another design aspect worth of attention is the Flyback transformer design in the power extracting converter, focusing on (1) the insulation between the primary side winding to the secondary side winding could sustain 5 kV; (2) the interwinding capacitance should be small, a few pF in most cases, since it would result in CM current to increase the current stress of the stack during switching transient.

In order to make the transformer compact, two ferrite E cores are utilized to construct it, as shown in Fig. 9(a). Since the primary voltage of the transformer could reach 5 kV, insulating materials and air gaps are adopted between primary and secondary windings. In this way, the leakage inductance L_σ is inevitably increased, and thus the efficiency η becomes lower according to (6). Based on this, in order to avoid partial discharges at high voltage, the electrical field distribution is analyzed by a 2-D electrostatic finite element analysis (FEM) simulation in ANSYS Maxwell, as shown in Fig. 9(b). Two hollow cylinders are printed using a 3D printer as the primary and secondary bobbins respectively, and the primary winding W_1 with the wire coat is surrounded by a Kapton tape layer, so as the secondary winding W_2. The material properties settings are listed in Table I. In the simulation, 5 kV is applied to W_1 and 0V is applied to W_2, it is seen that, the maximum electrical field is around 19 kV/cm in the air. Such a high value is due to the compact transformer design, which could be lower if a larger transformer core is utilized. Since the break down value is 30 kV/cm of air, it is acceptable in this transformer design of SCS gate driver. In the meantime, the interwinding capacitance of transformer is just 4.2 pF in the simulation, further verified to be 4.8 pF by experiments using an impedance analyzer, Keysight E4990A, which means it is also qualified.

V. Experimental Setup And Results

A. Experimental setup

From the above analysis, the experimental verification is given in this Section. Considering that energy flows from the grid to the battery in Fig. 5, in the established experimental setup, S_1 (S_2) is a custom packaged 10 kV/10 A SiC MOSFET module, which is combined with the proposed SCS gate driver as a single unit, while S_3 (S_4) is substituted with a 10 kV/10 A SiC Schottky diode for freewheeling. A power supply together with a 100 μF DC link capacitor is used as V^p_{dc}. L is a 30 mH MV inductor. V_b is not included (short-circuited) since other parts are sufficient to validate the design. The experimental schematic and its picture are shown in Fig. 10. Inside the unit, as shown at the right side of Fig. 10, 1.7 kV SiC MOSFETs (C2M1000170J) make up the stack in the power extracting part, and the commercial DC/DC power supply (MGJ6D242005LMC) which outputs -5 V/+20 V is applied in the gate driver part. In addition, the measuring equipment list is given in Table II.

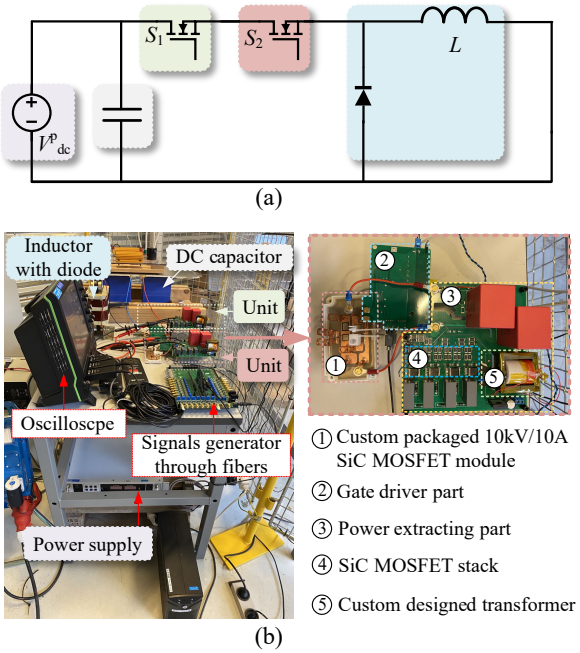

Fig. 10. (a) Schematic and (b) picture of the experimental setup

TABLE II
THE MEASUREMENT EQUIPMENT AND PARAMETERS

Name	Description	Parameter
Oscilloscope	Recording data	HDO6104
Current probe	Measuring i_d	CP030
Pearson probe	Measuring i_{CMi} (i = 1, 2)	Model 2877
Differential voltage probe	Measuring v_{dsi} (i = 1, 2), v_{gsi}(i = 1, 2)	HVD3605A
Passive voltage probe	Measuring v_{dsi} (i = a ~ d)	PPE 4kV
	Measuring V_{out}	PP018

B. Startup process and feasibility of SCS gate driver

In this part, one unit is applied to validate the feasibility of proposed SCS gate driver. Its startup process is shown in Fig. 11, and it is seen that, as the dc bus voltage increases to the startup voltage 2 kV, the SiC MOSFET stack in the power extracting converter starts to switch, and thus the power is extracted from the capacitor C to the gate driver. After a period, the output voltage V_{out} of the converter is

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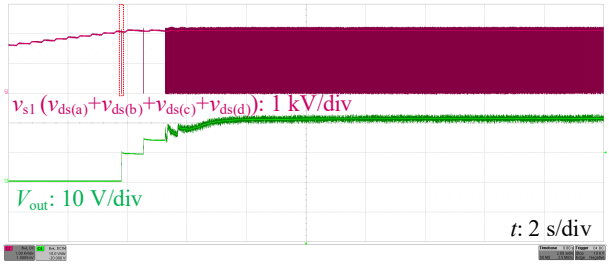

Fig. 11. Startup process using SCS gate driver

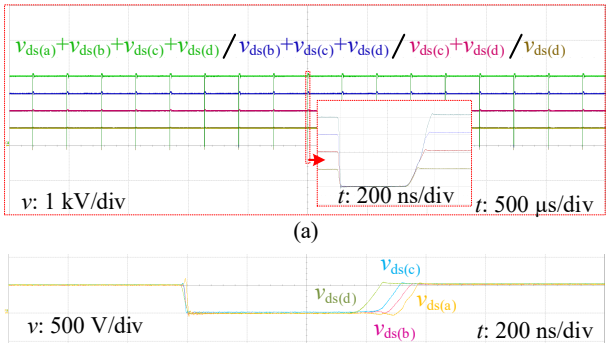

Fig. 12. (a) Zoomed view of Fig. 11 (b) voltage balancing of SiC MOSFET stack

increased to the clamping value 20 V and fed back to LT3798. Therefore, the converter is continuously powered and enters the normal working state. The voltage v_{s1} ($v_{ds(a)}$+$v_{ds(b)}$+$v_{ds(c)}$+$v_{ds(d)}$) across the SiC MOSFET stack falls and rises at the frequency f of 3.5 kHz and the on time Δt_{on} is 600ns, which is controlled by LT3798.

The waveforms are enlarged in Fig. 12(a), which shows good static voltage balancing of $v_{ds(i)}$(i= a ~ d) for four series connected SiC MOSFETs. During the switching transient, $v_{ds(i)}$(i = a ~ d) is shown in Fig. 12(b), which validates the good dynamic voltage balancing performance as well.

Further, the unit performs well for the tests from 2 kV to 5 kV. Considering the target application of 10kV SiC MOSFET (S_1) operating under 5 kV, the switching waveforms using SCS gate driver at V^{P}_{dc} of 5 kV and the current i_d of 3.5 A are shown in Fig. 13. It is seen that SCS gate driver works stable which outputs -5 V/+20 V. Due to the existence of the parasitic inductance in the gate-source switching loop, when the gate current increases from zero to the peak value, a voltage drop in the gate loop is induced and a high frequency oscillation of the gate-source voltage v_{gs1} occurs. In addition, the drain-source voltage v_{ds1} is clamped when it reaches the clamping value of C as the dash line in Fig. 13 (it also indicates the voltage waveform across C), and dv_{ds1}/dt of S_1 during turn-on and turn-off transients are measured to be -17 kV/µs and 10 kV/µs respectively.

C. *CM current comparison with conventional gate driver and scalability for series connection*

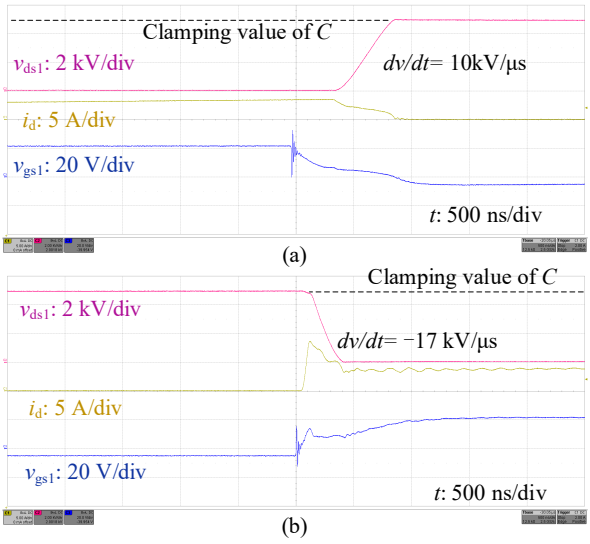

Fig. 13. Measured (a) turn-off (b) turn-on switching waveforms for a 10kV SiC MOSFET using SCS gate driver at 5 kV, 3.5 A

In order to further verify the advantages of proposed SCS gate driver, two units are in series in this part. By removing the connections between the power extracting part and the gate driver part, together with using an external power supply to power the gate driver, the topology is changed to the conventional topology with RCD snubber circuits as shown in Fig. 5. Therefore, the CM current i_{CM} comparison between the conventional gate driver and proposed SCS gate driver is given, and the measuring points are indicated in Fig. 3 and Fig. 5.

As shown in Fig. 14, S_1 and S_2 are tested with two conventional gate drivers. Since the commercial DC/DC converter is not suitable for 10 kV SiC MOSFET in this way, as it is limited by its isolation rating, only double-pulse experiments are conducted and V^{P}_{dc} is limited below 4.5 kV. It is seen that, the falling of drain-source voltage v_{ds1} and v_{ds2} of S_1 and S_2 corresponds to the rising of v_{ds3} and v_{ds4} of S_3 and S_4, and i_d rises from zero to 5 A after two pulses. During the switching process, i_{CM2} is measured to be 600mA and i_{CM1} is smaller due to the lower dv/dt stress. Such a large CM current flowing through the gate driver is a big potential hazard if V^{P}_{dc} goes higher.

In contrast, as shown in Fig. 15, S_1 and S_2 are tested with designed SCS gate drivers. Although no CM current should exist theoretically, some non-ideal factors in the designed SCS gate driver still cause the small CM noise during the switching transient, the reason is given here:

Due to the reverse recovery of the diode D and the parasitic inductance of the capacitor C in the "clamping RCD snubber" circuit, during the turn-on and turn-off transients of 10kV SiC MOSFET in the power loop, a small current can flow through it from the power extracting part. It induces a voltage difference of the primary side inductance of the transformer, resulting in dv/dt between the parasitic capacitor between the primary side and secondary side of the transformer. Therefore, a small

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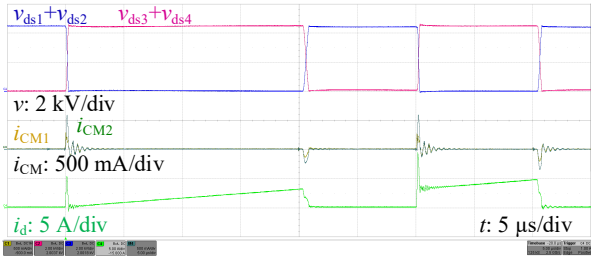

Fig. 14. Measured CM currents for S_1 and S_2 using conventional gate drivers

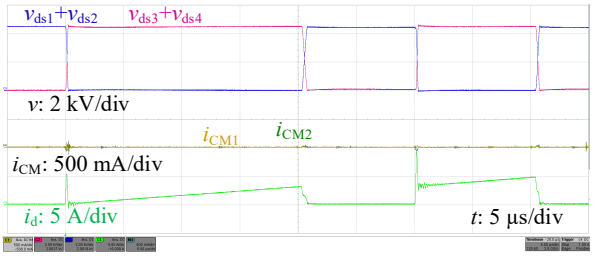

Fig. 15. CM currents of S_1 and S_2 using SCS gate drivers

current can flow through the gate driver unit, which is the cause of the small CM current.

In addition, the corresponding static and dynamic voltage balancing of S_1 and S_2 are also observed. During the static state, due to the open loop design of the power extracting converter, the characteristic of constant-power-load is not present. As shown in v_{s1} and v_{s2} in Fig. 16, the SiC MOSFET stacks in the power extracting parts of two units are both continuously switching at f = 3.5 kHz and Δt_{on} = 600 ns. Since their power loss is similar, the static voltage balancing of v_{ds1} and v_{ds2} is good. Also, as verified in a double pulse test shown in Fig. 17, the dynamic voltage unbalancing of v_{ds1} and v_{ds2} is acceptable since the proposed SCS gate drivers acts as clamping RCD snubber circuits, which proves that the proposed SCS gate driver is scalable to the series connection.

VI. Conclusion

The hardware design challenges of BESS are firstly discussed in this paper. After analyzing the CM noise issues of using the conventional gate driver in a running BESS, a SCS gate driver is further proposed to integrate 10kV SiC MOSFET into BESS, which could ease the design burden significantly. And then the detailed configuration and theoretical analysis are given. Finally, the experiments are conducted to validate the effectiveness. It is concluded that, compared with using conventional gate drivers, the CM currents using SCS gate drivers can be drastically reduced. Besides, as an improved self-powered gate driver design, it can provide sufficient gate driver power regardless of the switching requirement of 10 kV SiC MOSFET. Also, by combining the SCS gate driver with the 10 kV SiC MOSFET as a BESS building unit, it is scalable to the series connection design since it behaves as a clamping RCD snubber circuit.

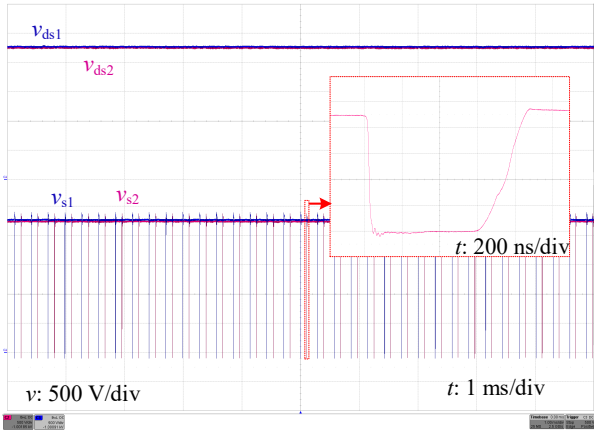

Fig. 16. Measurement showing static voltage balancing of S_1 and S_2 using SCS gate drivers

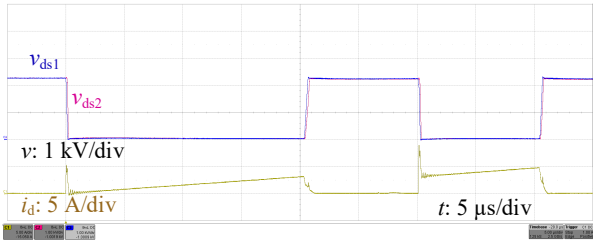

Fig. 17. Dynamic voltage balancing of S_1 and S_2 using SCS gate drivers in a double pulse test

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