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Thin-film VCSEL and Optical Interconnection Layer Fabrications for Fully Embedded Board Level Optical Interconnects

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Thin-film VCSEL and Optical Interconnection Layer Fabrications for Fully Embedded Board Level Optical Interconnects

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Dedication

Dedicated to my father and mother for their unconditional love and support

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Thin-film VCSEL and Optical Interconnection Layer Fabrications for Fully Embedded Board Level Optical Interconnects

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Semiconductor technology has been splendid evolved. As a consequence of, massive data traffic is required in system level. However copper based interconnection reached the upper limit of data transfer rate and can not provide enough bandwidth for high performance system. Copper based interconnection in long haul application was replaced to optical fiber. Optical interconnection in system level is generally considered as an alternative to provide high bandwidth. However, unlike long haul application, optical interconnection in system level encountered many problems such as compatibility, robustness and packaging difficulty. The compatibility to current electrical board system and packaging difficulty must be solved.

This dissertation describes a fully embedded board level optical interconnection, which can solve many problems, components fabrication and hybrid integration with electrical layers. Thin-film VCSEL array and flexible optical waveguide are demonstrated. The optical interconnection layer integrated with thin-film VCSEL and photo-detector arrays is demonstrated.

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Chapter 1: Introduction

1.1 MOTIVATION

The speed and complexity of integrated circuits are increasing rapidly as integrated circuit technology advances from very large scale integrated (VLSI) circuits to ultra large scale integrated (ULSI) circuits. As the number of devices per chip, the number of chips per board, the modulation speed, and the degree of integration continue to increase, electrical interconnects are facing their fundamental bottle-necks, such as speed, packaging, fan-out, and power dissipation. In the quest for high density packaging of electronic circuits, the construction of multi chip modules (MCM), which decrease the surface area by removing package walls between chips, improved signal integrity by shortening interconnection distances and removing impedance problems and capacitances [1,2].

The employment of copper and materials with lower dielectric constant materials can release the bottleneck in a chip level for next several years. The ITRS expects on chip local clock speed will constantly increase to 10GHz by year 2011. On the other hand, chip to board clock speed is expecting slow increasing rate after year 2002 [Figure 1.1][3].

The interconnection speed of copper line on printed circuit board can not run over a few GHz. As an example, the Figure 1.2 shows the simulation results of transmission gains for 7mils wide 42inches long copper trace on FR-4 board[4]. The frequency dependent dielectric loss and the skin effect loss dominate the transmission loss. On the

other hand, channel noise, resulted from connectors and crosstalk between lines, is increasing with the rate of 20dB/dec.

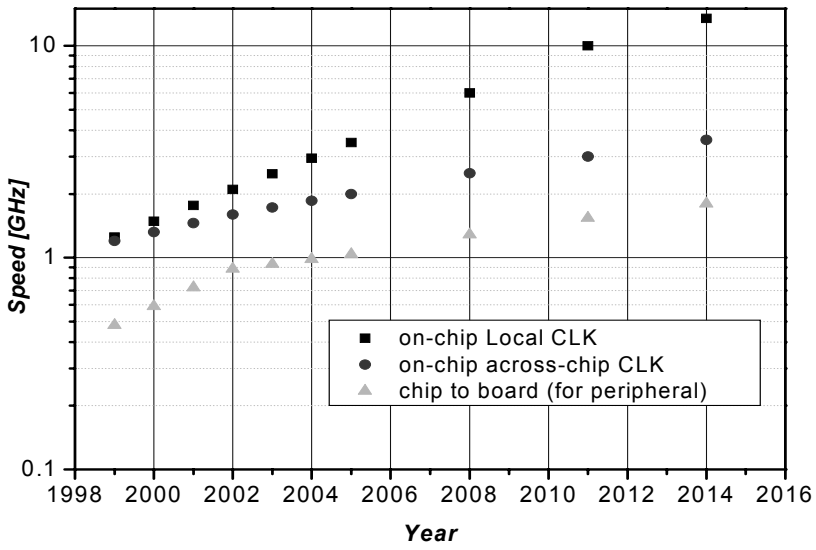


Figure 1.1 Interconnection speed roadmap (from ITRS).

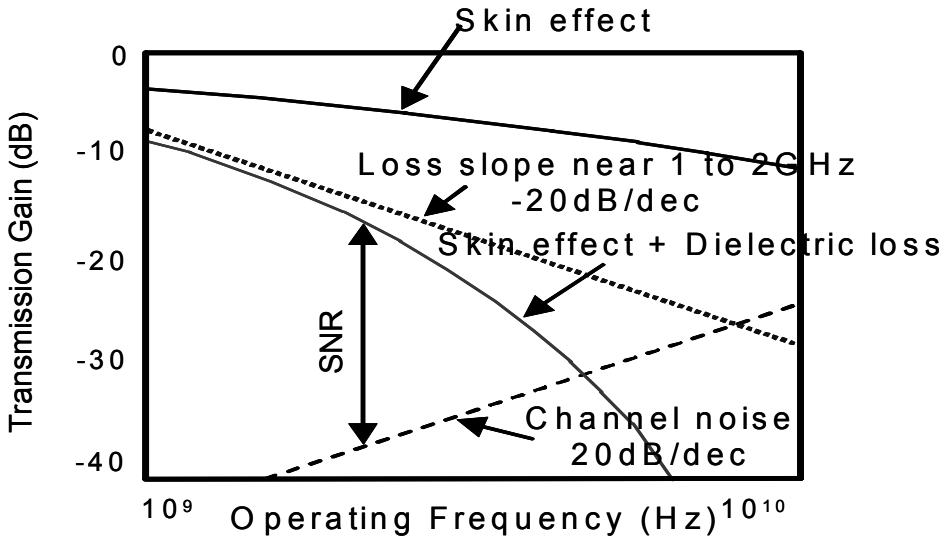


Figure 1.2 Transmission gain of 7mils X48in long Cu traces on FR-4 substrate as a function of operating frequency [Courtesy of Accelerant Networks].

For high fidelity operation, system should secure an adequate signal to noise ratio. As a consequence, FR-4 can not operate beyond a few GHz. High performance materials and advanced layout technology such as IMPS(Interconnected Mesh Power system) are introduced[5]. Especially, IMPS is focused on the signal integrity such as controlled impedance signal transmission with very low cross talk. The electrical interconnection described by Walker *et, al*. provides a 10Gb/s link over a distance less than 20m using coaxial cable[6]. However, coaxial cabling is bulky; therefore, it is not suitable for high density interconnection application.

Current high performance systems such as parallel computer, ATM machine, switching system, and SAN (Storage Area Network) consist of a number of smaller components and require high I/O bandwidth density. The high I/O bandwidth operating at high frequency tends to dissipate more power and be bulky [7]. Electrical interconnects operating at high frequency region have many problems to be solved such as crosstalk, impedance matching, power dissipation, skew, and packing density. However, there is a little hope to solve all of the problems. Power consumption was significantly reduced by adopting low voltage differential signal (LVDS) instead of TTL signal. Typical LVDS has 0.5V amplitude; hence, power consumption due to the 50ohm terminal resistor is reduced by 1/50. As frequency increases, power consumption due to the terminal resistor becomes trivial because the resistance of transmission line and the tangential loss of interlayer dielectric are increased. Additionally driver IC should charge and discharge the charge stored in the parasitic capacitor of the transmission line. The high density interconnect means narrow line width and spacing. It increases crosstalk and parasitic

capacitance. Therefore, longer electrical interconnection lines with high density consume much more power.

However, optical interconnection has several advantages such as immunity to the electro-magnetic interference, independency to impedance mismatch, less power consumption, and high speed operation. Although the optical interconnects have great advantages compared to the copper interconnection, they still have some difficulties regarding packaging, multi-layer technology, signal tapping, and re-workability.

Major performance improvement of a system, so far, comes from the improvements of devices by scaling transistors. The performance improvements of the system will come from new architectures and new technologies, not by relying on incremental reduction of the size of transistors. At present, metal based electrical interconnects dominate inter and intra-chip interconnections. The reason for this is simple. There is no viable cost effective alternative. If optical interconnects can provide cost effective solutions, where conventional electrical interconnects fail to function, optical interconnection in a system will be the most promising technology.

1.2 OVERVIEW OF OPTICAL INTERCONNECTS

The history of an optical interconnection is started from an ancient time. At that time, people communicated by blocking fire or smoke from line of sight. By the beginning of electrical communication, telegram and/or telephone drove out light communication due to the convenience of use. Radio wave communication was started after Guglielmo Marconi had succeed transmitting radio signals and is populated in these

days. Increasing data traffic (including voice) and need for low cost communication resurrect the optical communication. Long haul communication was dominated by means of optical fiber.

Several optical interconnect techniques such as free space, guided wave, board level, and fiber array interconnections were introduced for system level applications. Figure 1.3 depicts an example of free space interconnects [8]. A space between two circuit boards or a circuit board and optical interface board is purely empty; so, it is called free space. Light signals coming out from the sources propagate to designated location on the other substrate. The architecture is simple; however, realization is very difficult. All optical components should be mounted at precise location. Moreover, two substrates should be mounted on the designated place, exactly. If reflective optical components are used, mounting accuracy should be doubled by nature. Another disadvantage of the free space interconnects is that the system is vulnerability to external environment such as vibration, and dust. Maintenance of the system is extremely difficult, also.

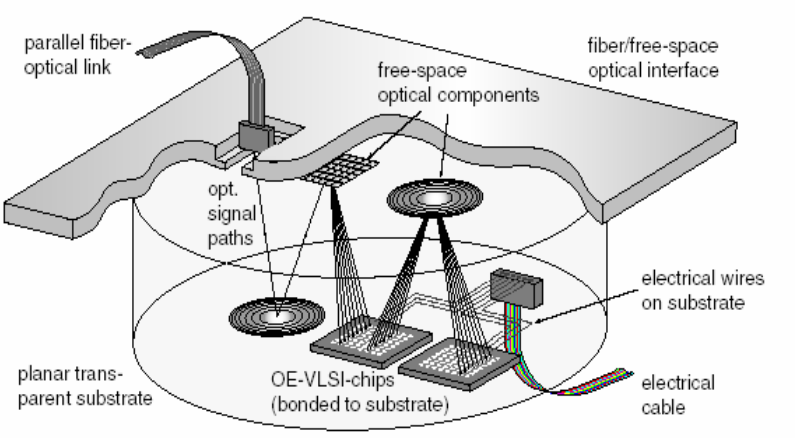


Figure 1.3 Illustration of free space optical interconnect [from M. Gruber [8]].

G. Kim *et al.* demonstrated bidirectional guided substrate mode optical backplane as illustrated in Figure 1.4 [9]. Each daughter board has optical transmitters and receivers (TX/RX). The basic architecture of the backplane is a bus structure. All daughter cards share bus lines. Signal coming out of the daughter card is sent to the transparent thick substrate through multiplexed volume hologram. The hologram splits beam into two directions at angle of 45°. The beam travels along the substrate by total internal reflection at the interfaces of a substrate. When the beam hits the hologram, some of the light coupled out normally and the rest of the light continues propagation. This kind of approach provides bidirectional function unlike any other approaches. However, a number of daughter cards and interconnection density are limited by the divergence of the light. Other issues to be considered are the reliability of the hologram and alignment. The performance of the hologram tends to be degraded by time elapse and sensitive to wavelength.

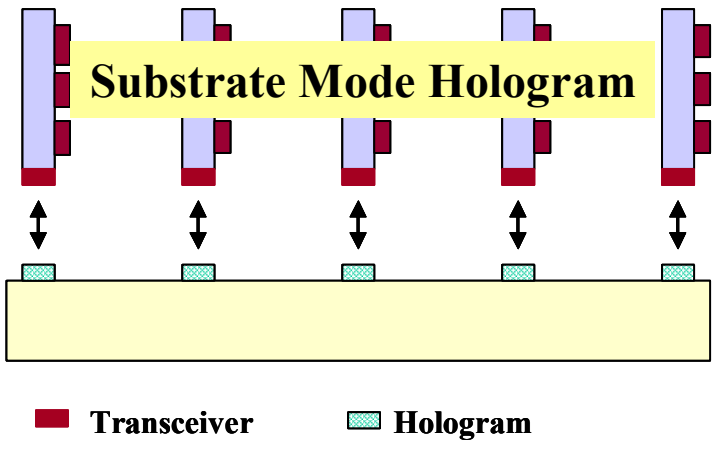


Figure 1.4 Illustration of guided substrate mode backplane [from G. Kim and *et.al*, [9]].

Optical interconnects are still bulky, less reliable, and have packaging difficulties. Many ideas were introduced to overcome aforementioned problems. They are mainly focused on reducing packaging volume and vulnerability to external environment. Scientists use matured semiconductor technology to build optical components. The first effort was fabricating planar lightwave circuits (PLC) on a solid or flexible substrate. Next, PLC was inserted between electrical circuit layers, i.e. hybrid print circuit board (PCB). Examples of the hybrid integrated PCB are illustrated in Figure 1.5, 1.6 and 1.7 [10,11,12]. The waveguide layer and electrical layers are fabricated separately and then laminated together. Optoelectronic devices like VCSELs and PIN-PD are mounted on the top of the hybrid PCB. The optical devices are directly coupled to the waveguide via 45º turning mirror. By doing so, vulnerability can be reduced. However, there is still an alignment problem. After laminating the boards, optoelectronic components should be aligned precisely at designated locations. This procedure is the most difficult part. The end of the waveguide was blocked from the line of sight by device itself. This alignment difficulty can be eased a little by increasing the size of the waveguide. Another shortcoming of these approaches is that optoelectronic devices occupy real estate of board. The only difference between electro-optic circuit board (EOCB) shown in Figure 1.7 and architectures shown in Figure 1.5 and 2.6 is that optoelectronic devices mounted on the heat sink are inserted in PCB. Devices are directly coupled to waveguide without using 45º turning mirror or collimation optics.

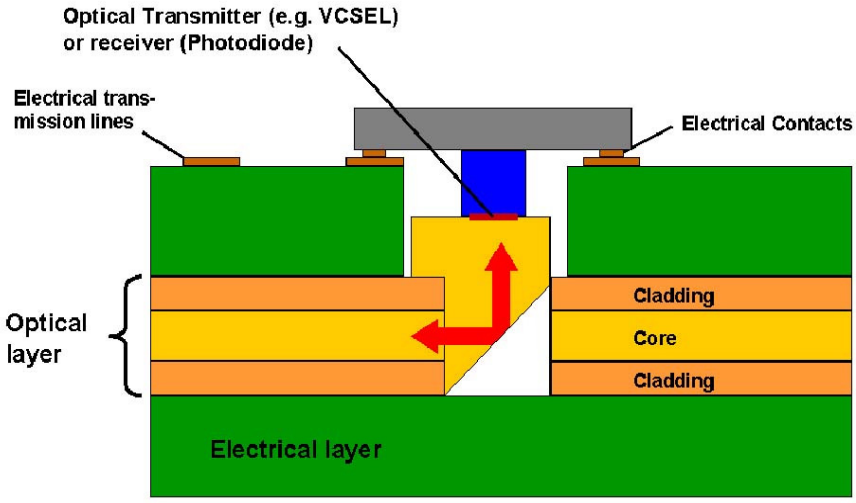


Figure 1.5 Illustration of hybrid PCB and coupling from on-board optical device [from Elmar Griese [10]].

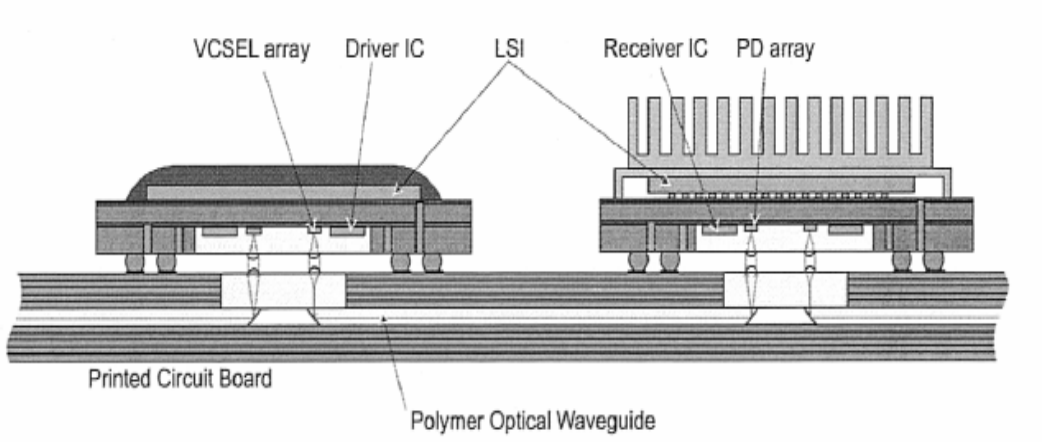


Figure 1.6 Illustration of optical-I/O chip packaging concept [from Yuzo Ishii and *et.al.* [11]].

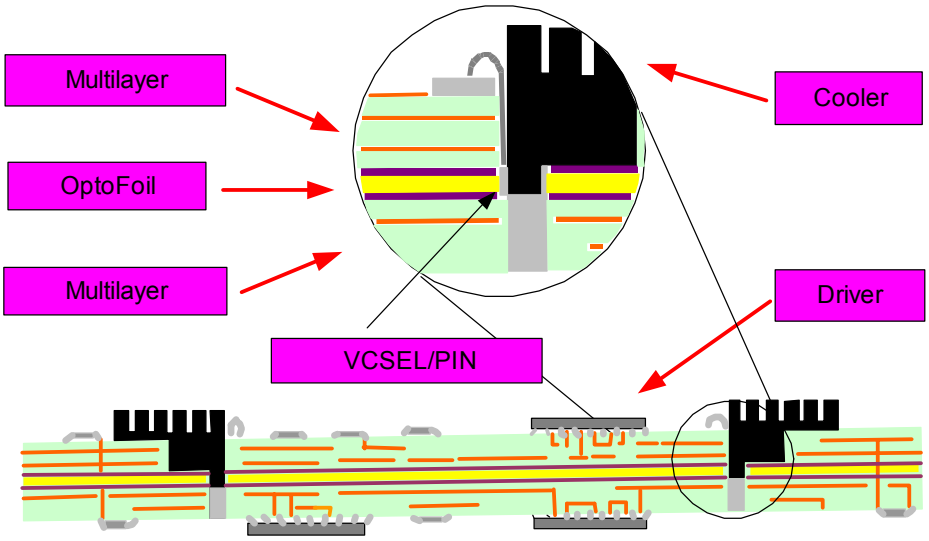


Figure 1.7 Concept of electro-optic circuit board (EOCB) [from Detlef Krabe and *et.al.*[12]].

1.3 FULLY EMBEDDED BOARD LEVEL OPTICAL INTERCONNECTS

The optical waveguides on or within PCB provides a robust system but occupies real estates of the board. Densely packed PCB is used in a high performance system. Therefore, occupying the footprints of the PCB is not a good choice. Securing the real estate of the PCB, robust packaging, and relief from alignment difficulty are major concerns for a board level optical interconnects.

A fully embedded board-level guided-wave optical interconnection is presented in Figure 1.8, where all elements, involved in providing high speed optical communications within a board, are shown. These include a vertical cavity surface emitting laser

(VCSEL), surface-normal waveguide couplers, and a polymer-based channel waveguide functioning as the physical layer of optical interconnection. The driving electrical signals to modulate the VCSEL and the demodulated signals received at the photo-receiver flow through electrical vias connecting to the surface of the PC board. The fully embedded structure makes the insertion of optoelectronic components into microelectronic systems much more realistic when considering the fact that the major stumbling block for implementing optical interconnection onto high performance microelectronics is the packaging incompatibility. All the real estate of the PCB surface is occupied by electronics not by optoelectronic components. The performance enhancement due to the employment of the optical interconnection is observed. There is no interface problem between electronic and optoelectronic components as conventional approaches do.

To realize fully embedded board level optical interconnects, many stumbling blocks are to be solved such as thin film transmitter and detector, thermal management, process compatibility, reliability, cost effective fabrication process, and easy integration.

The research work presented herein eventually will relieve such concerns and make the integration of optical interconnection highly feasible.

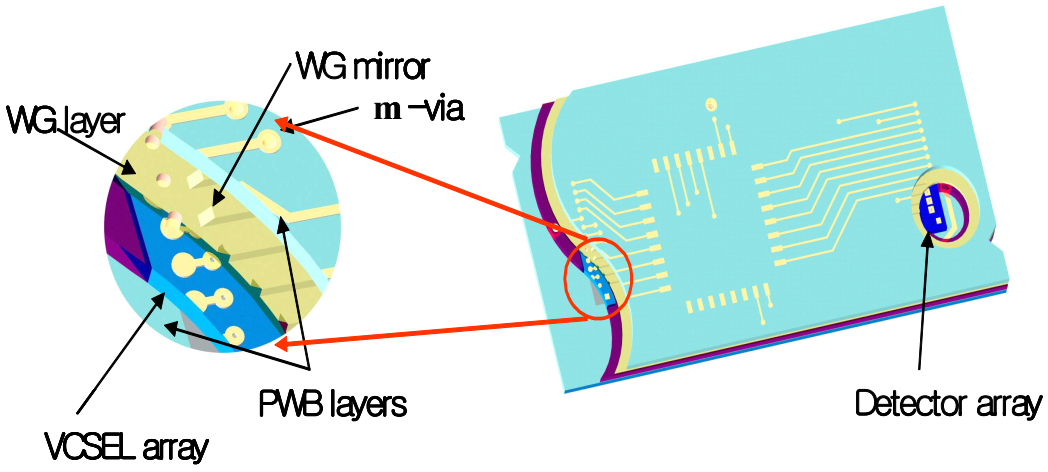


Figure 1.8 Illustration of a fully embedded board level optical interconnects.

1.4 CHAPTER ORGANIZATION

Chapter 2 describes the fabrication process of a linear array of the thin film vertical cavity surface emitting laser (VCSEL). Distributed Brag Reflector (DBR) design theory is addressed. Isolation technique for each device in an array, selective wet oxidation for current confinement, ohmic contacts formation and finally substrate removal technique are explained.

In Chapter 3, characterization of the VCSEL is described. Characterization includes electro-optical, modulation, and thermal property.

Chapter 4 describes the thermal management of a fully embedded VCSEL. The performance of the VCSEL is significantly affected by temperature. Innovative simple

thermal management strategy is established. The results of 2D finite element analysis results are delivered.

In Chapter 5, the fabrication and calculation of the optical interconnection layer (OIL) are described. In the first part of this chapter, the calculation of coupling efficiency for a 45° waveguide mirror is described. Next, 45° micro mirror fabrication process is described. In the last part, the OIL fabrication process using soft molding technique and deformation compensation technique of the soft mold are explained.

Chapter 5 describes optical layer embodiment including the integration of optoelectronic devices. Integration strategy with printed circuit board is explained also.

Finally a summary of this research is provided in Chapter 7. Here, our achievement is described.

Chapter 2: Thinned Vertical Cavity Surface Emitting Laser Fabrication.

2.1 INTRODUCTION

Semiconductor lasers are widely used in optical communications and optical storage devices. Semiconductor lasers can be categorized into two types by device structure. One is edge cleaved laser, and the other is surface emitting laser. The edge cleaved laser has excellent characteristics. However, the realization of 2D array is nearly impossible. Furthermore, initial probe test is impossible before separation into a chip. K. Iga suggested a vertical cavity surface emitting laser in 1977 for the purpose of overcoming aforementioned problems. Fundamental idea was placing a semiconductor gain medium in a Fabry-Perot cavity [13].

Major components of the vertical cavity surface emitting laser (VCSEL) are two mirrors and a gain medium in between. The mirrors are separated by a specific distance for resonance. The mirror is composed of quarter wave thick stack which has different refractive index. The gain medium and mirrors were deposited on semiconductor wafer by epitaxy.

For a long haul interconnection, long wavelength (1.3 or 1.5μm) laser is more suitable due to the low absorption of glass optical fiber. Absorption of the waveguide is not that critical in a short range interconnection. Therefore, there is no need to use a glass fiber. The electrical to optical conversion efficiency and coupling efficiency are more important to reduce power consumption. The VCSEL emitting 850nm wavelength light is

the most suitable source among any other wavelength VCSELs because manufacturing technology of 850nm VCSEL is matured and relatively cheap. Furthermore, polymeric waveguide can be used with VCSEL. A very thin VCSEL is needed in a fully embedded board level optical interconnects because the VCSEL is buried between the optical layer and the electrical layers. Thin-film VCSEL design and fabrication process are described in this chapter.

2.2 DESIGN OF EPITAXIAL LAYER STRUCTURE

A VCSEL has two distributed Bragg reflectors (DBR) and a cavity. Before designing a DBR, first we have to consider materials. The materials should have low electrical resistance and low absorption at lasing wavelength. Generally 850nm emitting laser use $Al_xGa_{1-x}As$ ternary semiconductor.

VSCEL has a small volume of gain medium. To overcome the loss of system, we have to increase feed back by high reflective mirrors. DBR is composed of many alternative quarter-wave thick stacks. The reflectance of the DBR can be calculated from characteristic matrix of a thin film stack [14]. If the DBR is composed of q layers, characteristic matrix of the assembly is simply the product of the individual matrices.

$$\begin{bmatrix} B \\ C \end{bmatrix} = \left(\prod_{r=1}^{q} \begin{pmatrix} \cos\delta_r & i\sin\delta_r/\eta_r \\ i\eta_r \sin\delta_r & \cos\delta_r \end{pmatrix} \right) \begin{bmatrix} 1 \\ \eta_m \end{bmatrix} \qquad \text{Equation 2.1}$$

$$\delta_r = \frac{2\pi N_r d_r \cos\theta_r}{\lambda}$$

$$\eta_r = yN_r \cos\theta_r \quad \text{for TE wave}$$

$$\eta_r = yN_r / \cos\theta_r \quad \text{for TM wave}$$

$$\eta_m = yN_m \cos\theta_m \quad \text{for TE wave}$$

$$\eta_m = yN_m / \cos\theta_m \quad \text{for TM wave}$$

η is the optical admittance of film or medium, δ is the phase difference, N_r is the refractive index of medium, d_r is the physical thickness of film, λ is the wavelength of light and θ is incident angle at medium. The modified admittance (Y) of film assembly is the ratio of tangential component of magnetic field to the tangential component of electric field.

$$Y = \frac{C}{B} \qquad \text{Equation 2.2}$$

The reflectance (R) of the thin film assembly is calculated by Equation 2.3.

$$R = \left(\frac{\eta_0 - Y}{\eta_0 + Y}\right)\left(\frac{\eta_0 - Y}{\eta_0 + Y}\right)^* \qquad \text{Equation 2.3}$$

Designed VCSEL epi-layer structure is shown in Figure 2.1. Bottom DBR consisted of 40.5 pairs of $Al_{0.16}Ga_{0.84}As$ and $Al_{0.92}Ga_{0.08}As$. Between $Al_{0.16}Ga_{0.84}As$ and $Al_{0.92}Ga_{0.08}As$ layer, linearly graded index layer was inserted to reduce resistance. Top DBR consisted of 23 pairs of layers and had same structure as in the bottom DBR.

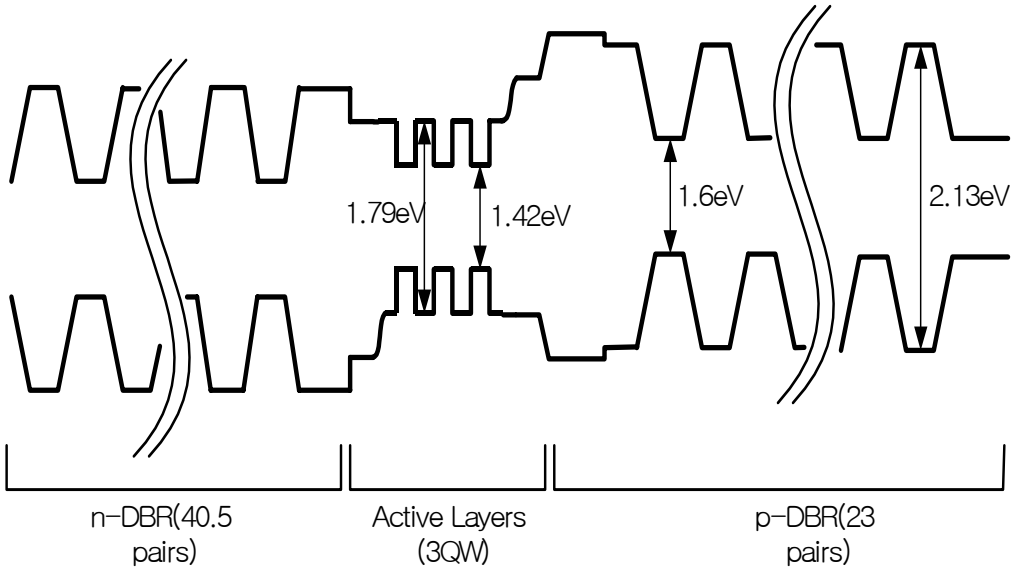


Figure 2.1 Energy band diagram of 850nm emitting VCSEL.

Refractive indices of materials used in DBR are summarized in Table 2.1.

Table 2.1 Refractive indices of $Al_xGa_{1-x}As$ materials at 850nm [15].

Composition $Al_xGa_{x-1}As$	Refractive Index @850nm	Composition $Al_xGa_{x-1}As$	Refractive Index @850nm
x=0	3.675	x=0.6	3.212
x=0.16	3.505	x=0.92	3.031
x=0.3	3.401	x=0.98	3.000

Table 2.2 Epitaxial layer structure of 850nm VCSEL [from Optowell Co., Ltd].

Layer	Material	Composition	Thickness	Doping(cm^3)	Actual Doping	Dopant
26	GaAs		5	3.00E+19	~4.0E+19	C
25	AlxGaAs	0.16	5	2.00E+19	~2.0E+19	C
24 X 23	AlxGaAs	0.16	41.1	2-3E+18	~2.0E+18	C
23 X 23	AlxGaAs	0.92 -> 0.16	20	2-3E+18		C
22 X 23	AlxGaAs	0.92	49.3	2-3E+18	~3.0E+18	C
21 X 23	AlxGaAs	0.16 -> 0.92	20	2-3E+18		C
20	AlxGaAs	0.16	19.5	2-3E+18		C
19	AlxGaAs	0.98 -> 0.16	20	2-3E+18		C
18	AlxGaAs	0.98	30	2-3E+18		C
17	AlxGaAs	0.92	55.1	2-3E+18		C
16	AlxGaAs	0.6	95.3	N		
15	AlxGaAs	0.3	11	N		
14	GaAs		7	N		
13 X 2	AlxGaAs	0.3	10	N		
12 X 2	AlxGaAs		7	N		
11	AlxGaAs	0.3	11	N		
10	AlxGaAs	0.6	95.3	N		
9	AlxGaAs	0.92	59.6	1-2E+18		Si
8	AlxGaAs	0.16 -> 0.92	20	1-2E+18		Si
7X40	AlxGaAs	0.16	41.1	1-2E+18	~1.5E+18	Si
6X40	AlxGaAs	0.92 -> 0.16	20	1-2E+18		Si
5 X 40	AlxGaAs	0.92	49.3	1-2E+18	~2.0E+19	Si
4 X 40	AlxGaAs	0.16 -> 0.92	20	1-2E+18		Si
3	AlxGaAs	0.16	10	1-2E+18		Si
2	GaAs		500	1-3E+18	~3.0E+18	Si
1	AlxGaAs	0.98	100	1-3E+18		
0	GaAs	Substrate				

The bottom DBR (n-DBR) and the top DBR (p-DBR) were doped with silicon and carbon at the doping level of 10^{18} and 10^{19}, respectively. The calculated reflectances of the DBRs is shown in Figure 2.2. The reflectance of n-DBR and p-DBR are 99.98% and 99.68% at 850nm, respectively.

An active layer between DBRs was composed of three GaAs quantum wells. The undoped GaAs epi-layer of 7nm thickness was surrounded by 10nm thick $Al_{0.3}Ga_{0.7}As$ layers to form a quantum well. Fabry-Perot cavity should have the optical thickness of

wavelength. To make one wavelength thick cavity, the rest of space was filled with $Al_{0.6}Ga_{0.3}As$ spacer layer.

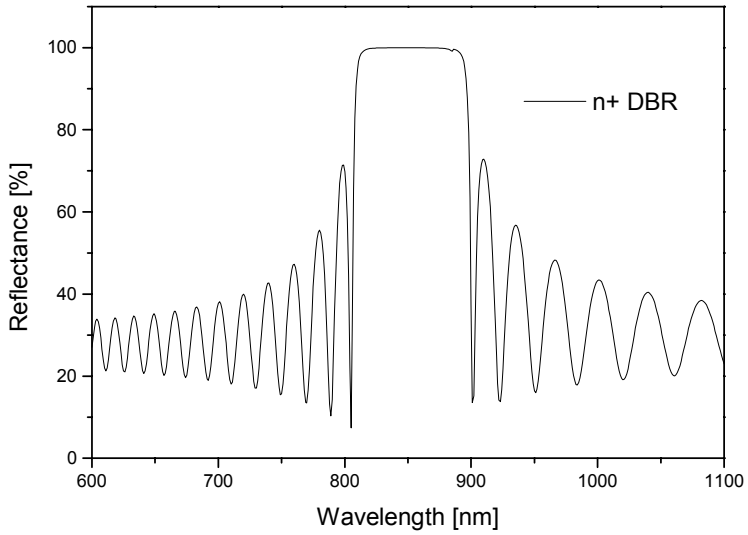
$Al_{0.98}Ga_{0.02}As$ layer of 30nm thickness was inserted between active and top DBR layer for selective oxidation to form current aperture. An etch stop layer was also inserted between GaAs substrate and GaAs buffer layer.

The calculated resonance spectrum of VCSEL is shown in Figure 2.3. In this calculation, material absorption was neglected. Full width at the half maximum (FWHM) of resonance was 0.3nm.

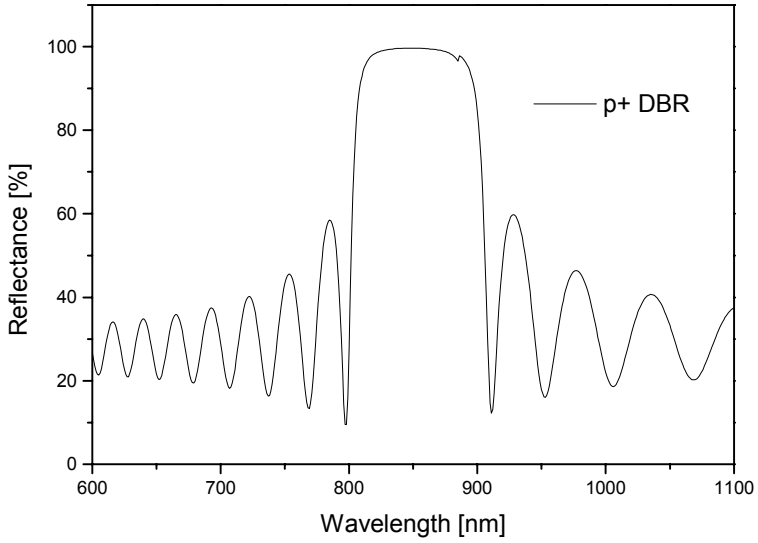
2.3 FABRICATION OF VERTICAL CAVITY SURFACE EMITTING LASER

The epitaxial layers of VCSEL were grown on n-type GaAs wafer using MOCVD at Optowell Co. Ltd. There are two kinds of current confinement method. One is proton implantation. The other is lateral oxide confinement. Proton bombardment forms an insulating region. Therefore, current can not flow through this region. For the annular shape proton bombardment region, a funnel shaped current path is established; therefore, a high current density region is formed at gain medium. The selective lateral oxidation confinement is based on the difference of oxidation rates according to material composition. Selective oxidized current confinement method was chosen in our research because of low threshold current characteristics and ease of fabrication at our facility.

General thin film VCSEL process flow is shown in Figure 2.4. Detailed description will be addressed in the following section.



(a)



(b)

Figure 2.2. Calculated reflectance graphs of n-DBR (a) and p-DBR (b).

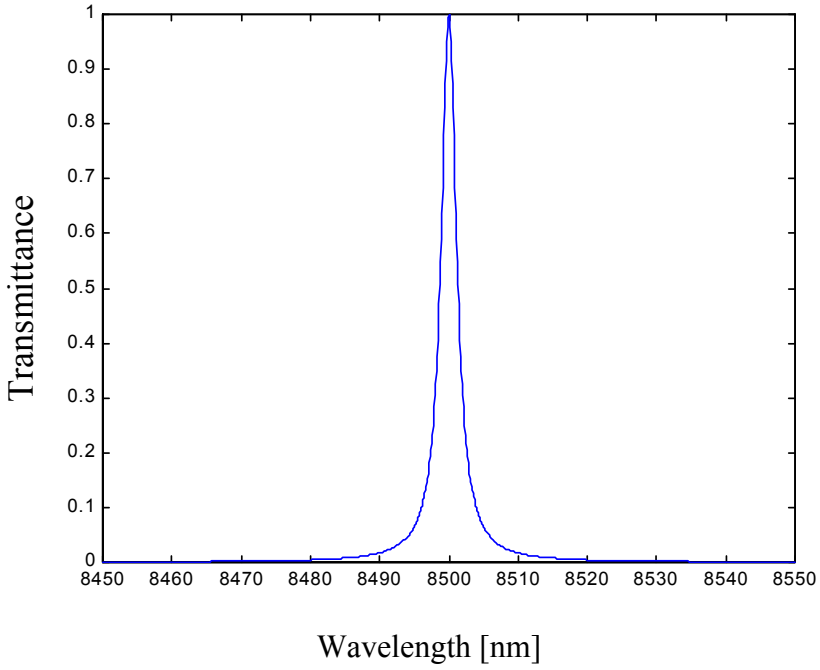


Figure 2.3 Calculated resonance curve of designed VCSEL, (neglects material absorption).

2.3.1 Device isolation

GaAs epi-wafer is electrically conductive; therefore, each device in an array must be isolated. Generally, mesa structure is used for isolation. Annular shaped trench, which has the inner diameter of 42μm, the outer diameter of 80μm, and the depth of 3.2μm, were formed as shown in Figure 2.4a. The depth of the trench was determined to be 3.2μm by the epi-layer structure because of high aluminum composition layer for lateral oxidation is located 3.1μm from the top surface.

First, photoresist AZ5214 was spin coated on the wafer, and annular shape patterns were exposed. After developing the patterns, hard bake was carried out at 100°C

on a hot plate for 15 minutes. Epitaxial layers were composed of high and low aluminum composition AlGaAs. To etch these layers, non-selective etch solution is required for mesa etching. The sulfuric acid (H_2SO_4) of 96%, hydrogen peroxide (H_2O_2) of 30% and water (H_2O) were mixed at the volume ratio of 3:30:150. The etch rate for these epitaxial layers was 1.5μm per minute.

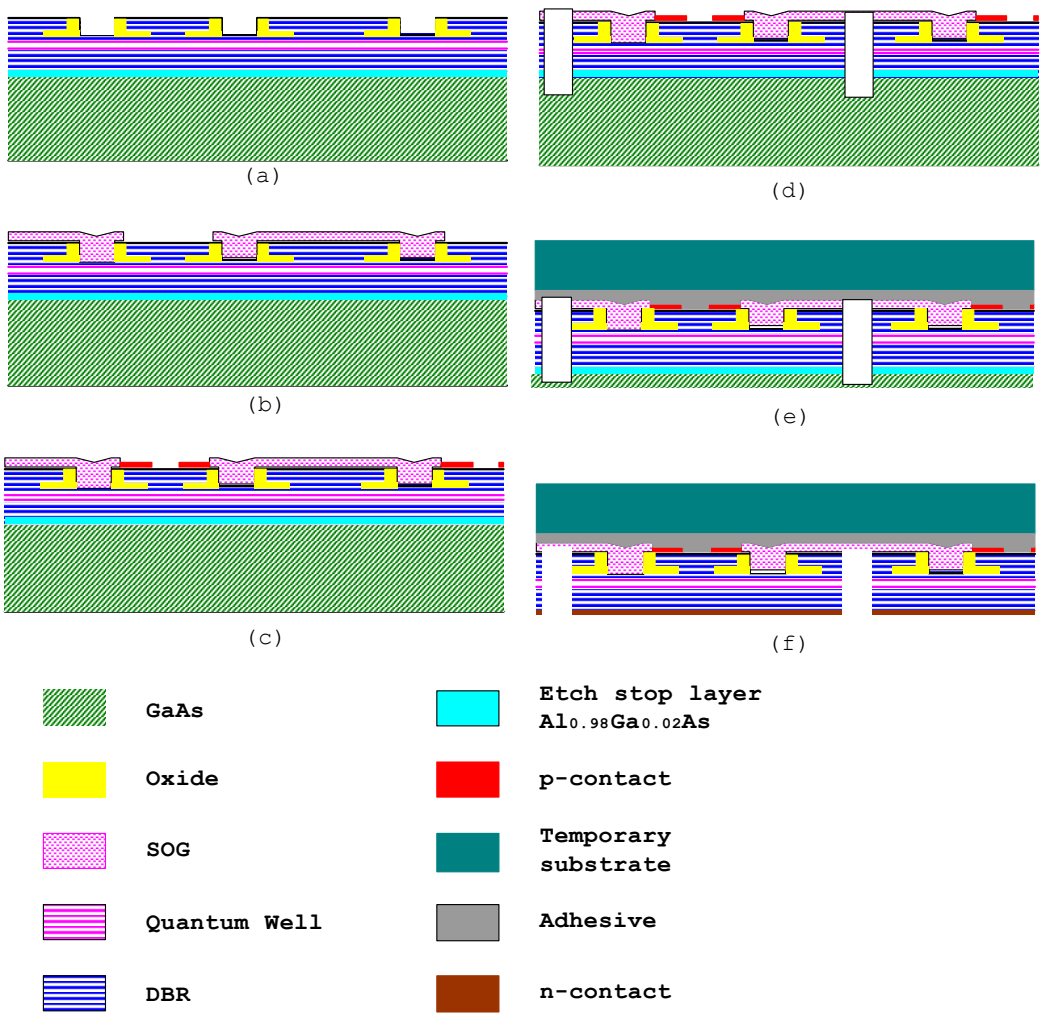
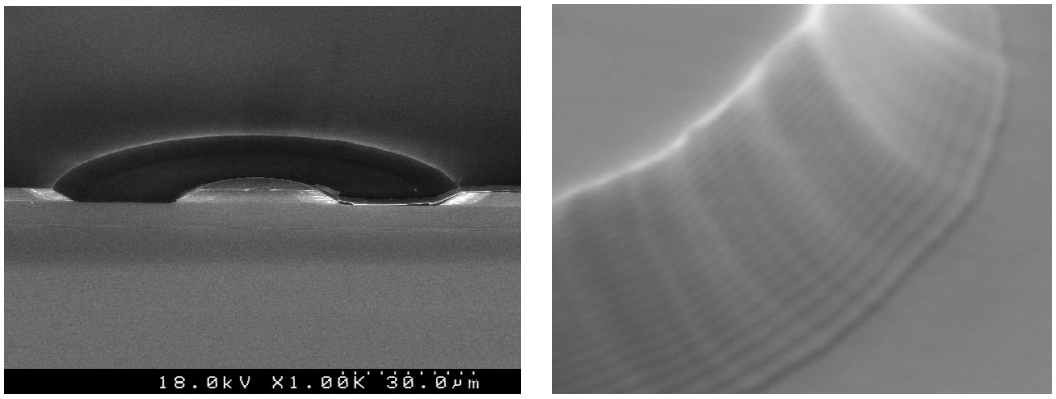


Figure 2.4 Thin film oxide confined VCSEL fabrication flow chart.

The cross sectional view of the annular shape etched trench is shown in Figure 2.5. The mesa at the center of the annular shape trench will be the VCSEL area. The etchant has an isotropic etch characteristic; therefore, undercut was formed just below the photoresist etch mask. The resultant diameter of the mesa was about 36μm, reduced from 42μm. Figure 2.5b shows the sidewall profile of etched region. Due to the isotropic etch property of etchant, sidewall has curved shape.



(a) (b)

Figure 2.5 Cross sectional view of the annular shape trench (a) and sidewall profile (b).

2.3.2 Selective wet oxidation for current aperture

The wet oxidation of AlAs was reported in 1979 [16]. Researchers at the University of Illinois discovered the atmospheric degradation of Al containing compound semiconductors [17]. The wet oxidation of aluminum containing semiconductor at high temperature produces robust oxide, which has lower refractive index than original

material. The thickness of converted semiconductor is reduced a little during oxidation. $Al_{0.98}Ga_{0.02}As$ shows the least shrinkage in thickness during oxidation.

The wet oxidation was performed in a furnace. Figure 2.6 illustrates oxidation apparatus. Nitrogen gas at the flow rate of 2 liters per minute was introduced into a bubbler, which is filled with 90°C water. Water vapor and nitrogen gas were flown into the furnace at 460°C. The water vapor reacts with AlGaAs and converts AlGaAs to oxide. The mesa etched wafer was placed at tilted angle to form an uniform oxidation over the wafer. The measured lateral oxidation extent of AlAs and $Al_{0.975}Ga_{0.025}As$ at different temperature are shown in Figure 2.7. The oxidation rates of AlAs were 0.3μm/min and 0.73μm/min at 420°C and 440°C, respectively. The lateral oxidation rate of the $Al_{0.975}Ga_{0.025}As$ was 1.0μm/min at 460°C. As increasing the aluminum content or oxidation temperature, oxidation rate is increased. For all cases, oxidation rate was constant within given period.

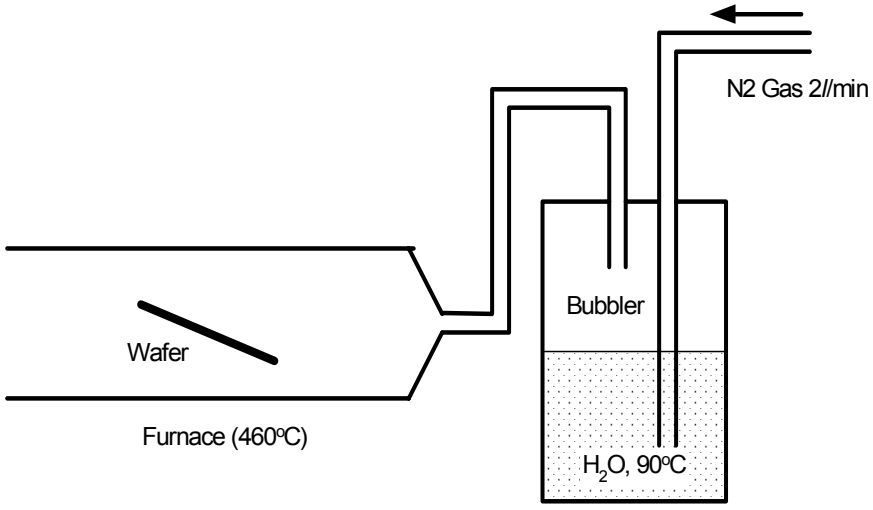


Figure 2.6 Schematic diagram of wet oxidation apparatus.

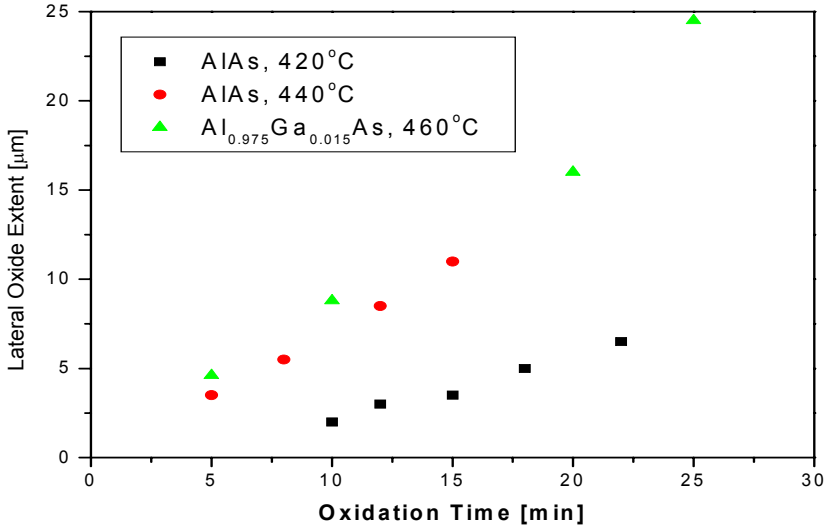
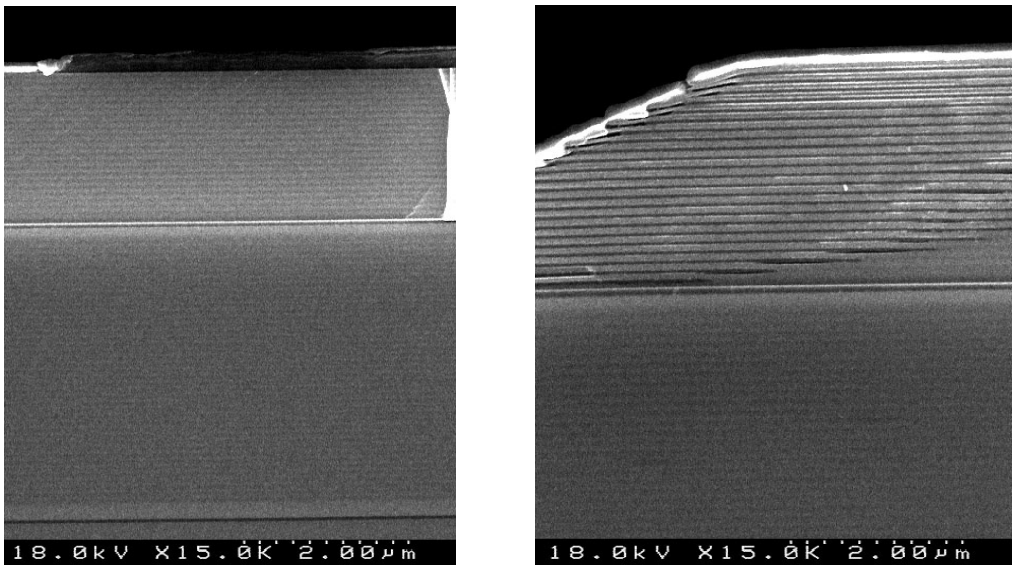


Figure 2.7 Lateral oxidation extents as a function of time for AlAs and $Al_{0.975}Ga_{0.025}As$ at different oxidation temperatures.



(a) (b)

Figure 2.8 SEM pictures of VCSEL epitaxial layers (a) and cross sectional view of the oxidized region near the edge of the trench (b).

Selective oxidation to form current aperture is based on the different oxidation rates of different aluminum composition $Al_xGa_{1-x}As$ semiconductors. Oxidation layer was composed of 30nm thick $Al_{0.975}Ga_{0.025}As$. On the other hand, low index layer was composed of $Al_{0.92}Ga_{0.08}As$. The oxidation rate of $Al_{0.975}Ga_{0.025}As$ is 4 times higher than that of $Al_{0.92}Ga_{0.08}As$ [17]. Therefore, oxide aperture was formed at just above the active layer.

Epitaxial layer structure is shown in Figure 2.8a. White horizontal line in the picture is the active layer of the VCSEL. Figure 2.8b shows the oxidized portion of the annular shape trench.

2.3.3 Metallization and thinning

After the wet oxidation of current aperture layer, annular shaped trench must be filled with dielectric material to protect further oxidation caused from external environment and to provide isolation from other electrical pads because top surface is highly conductive.

There are many gap filling dielectric materials such as polyimide, spin on glass (SOG), and etc. Photo-imagible polyimide is widely used for isolation purpose. Oxide confined VCSEL shows less long-term reliability than ion implanted VCSEL. It may be caused from the further oxidation of current confinement layer due to prolonged exposure to oxygen and humidity. Polyimide permeates more moisture than SOG. In this research, we chose SOG as a gap filling material. Therefore we can expect better long-term reliability.

SOG was spin coated over the wafer at 3000RPM, and then cured in the furnace at 300°C for 30 minutes. The thickness of the SOG was 3000Å after curing. The patterning of the SOG was followed to remove the SOG on the mesa to provide metal contact area. After developing photoresist pattern, the SOG was removed by wet etch using buffered oxide etchant (BOE).

Next process is the metallization of p-contact. Lift-off method was used to define metal contacts. Before depositing metal on the wafer, photoresist (AZ5214) was spin coated, exposed and developed. The thickness of the photoresist was 1.1μm on flat surface. However, the thickness of the photoresist on the top of the mesa was only 0.6μm. It is difficult to lift off metal deposited on a thin photoresist layer. Just before metallization, native oxide formed on the wafer surface was removed by wet etching using high selective etchant (HCl [1] : H_2O [1]). G. Stareev reported extremely low resistance Ti/Pt/Au ohmic contact to p-type GaAs [18]. The titanium of 20nm thick, the platinum of 10nm thick, and the gold of 100nm thick were deposited in sequence in a vacuum chamber. To form a low resistance ohmic contact, the metals need to be annealed at a high temperature with short time interval. However, rapid thermal annealing (RTA) process is carried out later just after the deposition of n-contact.

Before thinning wafer, we should consider how to cut extremely thin individual device from the wafer. If a wafer is thick, it provides enough mechanical strength to withstand dicing process. However, if a wafer is thin, it can not survive the mechanical dicing. Another issue is resulted from reliability after dicing. Mechanical dicing produces lots of damages to cutting edges. They cause small crack and then finally break device

after integration [19]. To avoid this, a deep chemical etch groove technique, so called "Dicing-by-Thinning", was introduced [20]. Before thinning the wafer, the outline of device was deep etched at front side of the wafer using chemical etchant. The depth of the etched groove is larger than final device thickness. Therefore, individual device is separated automatically when thinning was completed.

The fabrication process carried out so far is for a typical thick VCSEL, except for the n-contact formation. However, thin film VCSEL process needs additional fabrication steps. The original thickness of GaAs epitaxial wafer is 650μm. To make very thin VCSEL, we can use either epitaxial liftoff or substrate back etching method.

The epitaxial liftoff (ELO) technique was first developed by E.Yablovitch [21]; after then, many researchers succeed using the technique in various areas such as light emitting diode (LED), VCSEL, MSM photodiode and double barrier resonant tunneling diode (DBRTD) [22,23,24,25]. ELO is based on the high selective etch of different materials. Hydrofluoric acid has a virtually infinite selectivity to GaAs/AlAs system. Substrates can be removed by dissolving AlAs layer between substrate and device layer.

Another approach to make thin film device is back etch. Epitaxial layer structure is the same as in ELO technique, but substrate is removed by etching from the back side. The substrate separated by ELO can be reused, but the back side etch dissolves the substrate. III-V semiconductor wafer is still expensive compared to a silicon wafer. However the performance of a device is much important if we consider the possible degradation of performance caused from not so excellent surface of a reused wafer. Thus

ELO is interesting but not widely used in these days. Therefore we used substrate removal method by back side etching.

Removing 650μm thick substrate using chemical wet etchant is not realistic. Wet etching can dissolve thick GaAs substrate; however, it produces harmful byproducts. Etch stop layer is about 100nm~ 1μm which is very thin. If the thickness of substrate is 650μm and the etch stop layer is 100nm thick, then etchant must have a selectivity of 6500 or better. However, there is no etchant with such a high selectivity. Before lapping, the wafer is bonded to a thick glass substrate using the Crystal Bond 509™. The bonded wafer is strong enough to survive the harsh lapping environment. Then wafer is mechanically lapped down to 70μm by lapping machine, and then chemically etched using medium-selectivity, high-speed etchant and very high selectivity etchant, sequentially. The thickness of mechanically thinned VCSEL wafer was 70μm including an etch stop layer of 100nm and 60μm thick GaAs substrate. It means that the selectivity of an etchant must exceed 600. There is a limitation for using ammonium hydroxide and hydrogen peroxide system to remove the whole substrate without damaging VCSEL structure. The etch selectivity is not enough; hence, thin etch stop layer and some of VCSEL layer will be dissolved unless etching is precisely stopped. Initial etch was carried out using PA etchant. The PA etchant is composed of hydrogen peroxide (H_2O_2) and ammonium hydroxide (NH_4OH) mixed at the volume ratio of 12 to 1. The PA etchant has a selectivity of 35 to $Al_{0.16}Ga_{0.84}As$. The etch rate at ambient temperature was 3μm/min. Etch was stopped when it reaches 30μm because of uneven thickness during the lapping.

Next slow etching was followed by using high selectivity etchant to remove the rest of GaAs. Generally, citric acid hydrogen peroxide system has high selectivity of ~95 [26]. In our application, this is not enough because of thin etch stop layer (100nm) and relatively thick substrate (60μm). Therefore, modified citric acid hydrogen peroxide etchant having high selectivity of more than 1000 was used [27].

The etchant is composed of citric acid monohydrate, potassium citrate and hydrogen peroxide. One mole concentration of citric acid monohydrate in water and the same concentration of potassium citrate were prepared. Just before the etch, both solutions were mixed at the same volume ratio. And then, this mixed solution of seven and half part was mixed with fresh one part of hydrogen peroxide. The etch rate of this solution was 240nm per minute for GaAs, and the selectivity is over 1000 to $Al_{0.9}Ga_{0.1}As$ and GaAs structure. The etching was stopped when etch stop layer is revealed. The remaining epitaxial layers were VCSEL epitaxial layers (top and bottom DBR and active layer), GaAs buffer layer of 50nm and etch stop layer of 100nm thick. The etch stop layer must be removed before deposit metal on the GaAs buffer layer. The etch stop layer was completely removed in HF solution. In this process, etching time is not that important because of the nearly infinite selectivity of HF.

Metallization process for n-contact was followed. A gold germanium (AuGe) of 20nm thick, Nickel (Ni) of 20nm thick and gold (Au) of 120nm thick were deposited in sequence. After metal deposition, thin wafer was removed from the glass substrate by raising temperature. Elevated temperature melts bond material and releases thin VCSEL devices from glass substrate. Cleaning process was followed to remove any residual on

devices. After cleaning, rapid thermal process (RTP) was carried out at 420°C for 20 seconds. A fabricated 10μm thick 1X12 linear VCSEL array is shown in Figure 2.9.

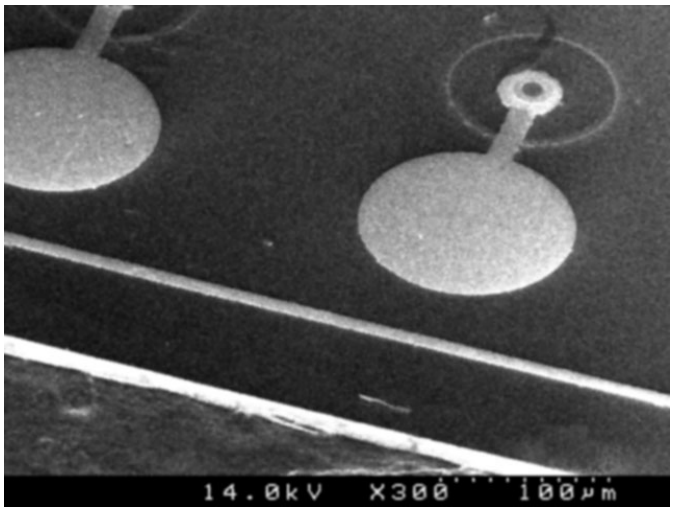


Figure 2.9 SEM photograph of a 10μm thick 1X12 linear VCSEL array.

Chapter 3: VCSEL Characterization

3.1 ELECTRICAL AND OPTICAL CHARACTERISTICS

Epitaxial layers were grown on 2° off n-GaAs wafer at Optowell Co., Ltd. All data regarding to reflectance, photoluminescence and uniformity were measured at the Optowell. The reflectance of the DBR at different areas is shown in Figure 3.1. Fabry-Perot dip is located at 852nm. The variation of the Fabry-Perot dip which indicates uniformity of epitaxial layer was ± 4nm over 3 inche wafer [Figure 3.2].

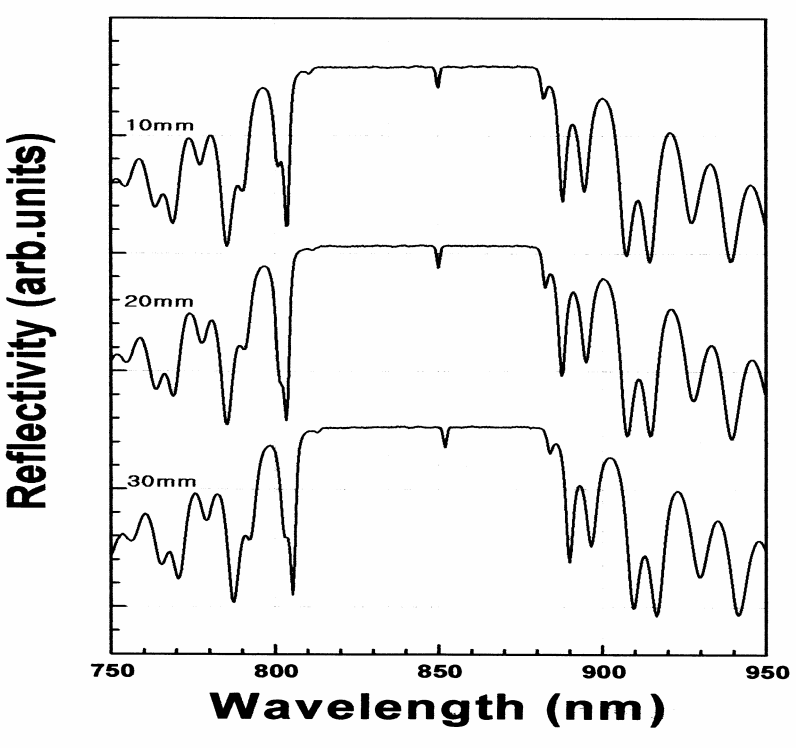


Figure 3.1 Measured DBR reflectance graph of various areas on 850nm VCSEL wafer. [Measured at Optowell Co., Ltd.]

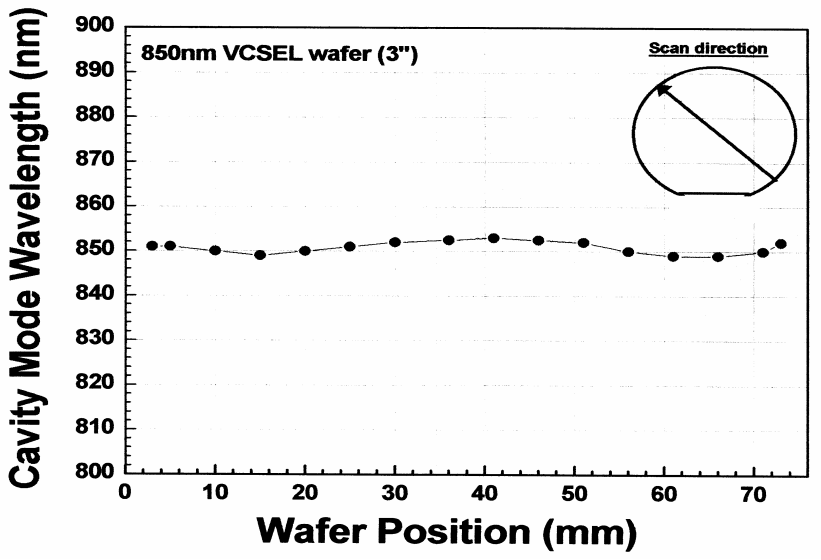


Figure 3.2 Epitaxial layer uniformity across the wafer. [Measured at Optowell Co., Ltd.]

The lasing wavelength of the VCSEL at 6mA was 852nm and had spectral width (FWHM) of 0.3nm as shown in Figure 3.3.

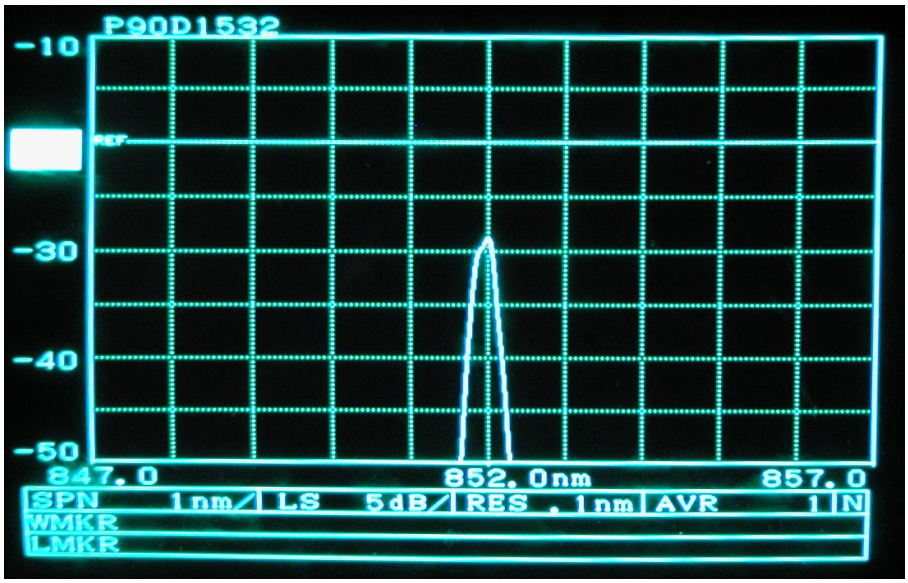


Figure 3.3 Emitting spectrum of an 850nm VCSEL.

The current voltage (I-V) characteristic of the VCSEL was measured using Agilent 4155 semiconductor parameter analyzer. Figure 3.4 shows the I-V characteristics of individual VCSEL in the 15μm aperture VCSEL array. The threshold current was 1.6V. The deviation of I-V curves resulted in non-uniform oxidized current apertures.

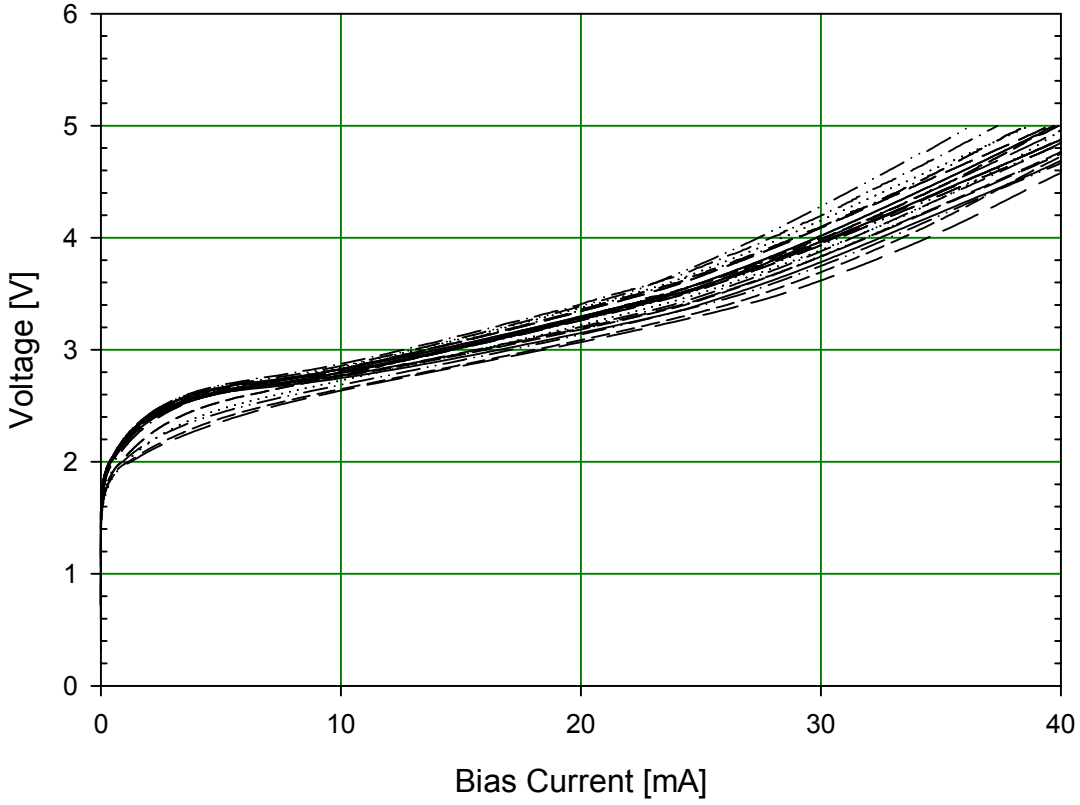


Figure 3.4 Current –Voltage characteristics of a 15μm diameter 1X12 linear VCSEL array.

The light to current (L-I) characteristics of thick VCSEL were also measured. The threshold current was 1mA for VCSEL with 15μm aperture. Average slope efficiency was 31%. Threshold current density was 566A/cm^2. The deviation of the L-I

characteristic mainly resulted in non uniform current aperture. Each curve on the graph corresponds to individual VCSEL in an array. Some of them show a thermal roll over at injection current above 5mA. Uniform oxidation current aperture over the wafer is the most important fact.

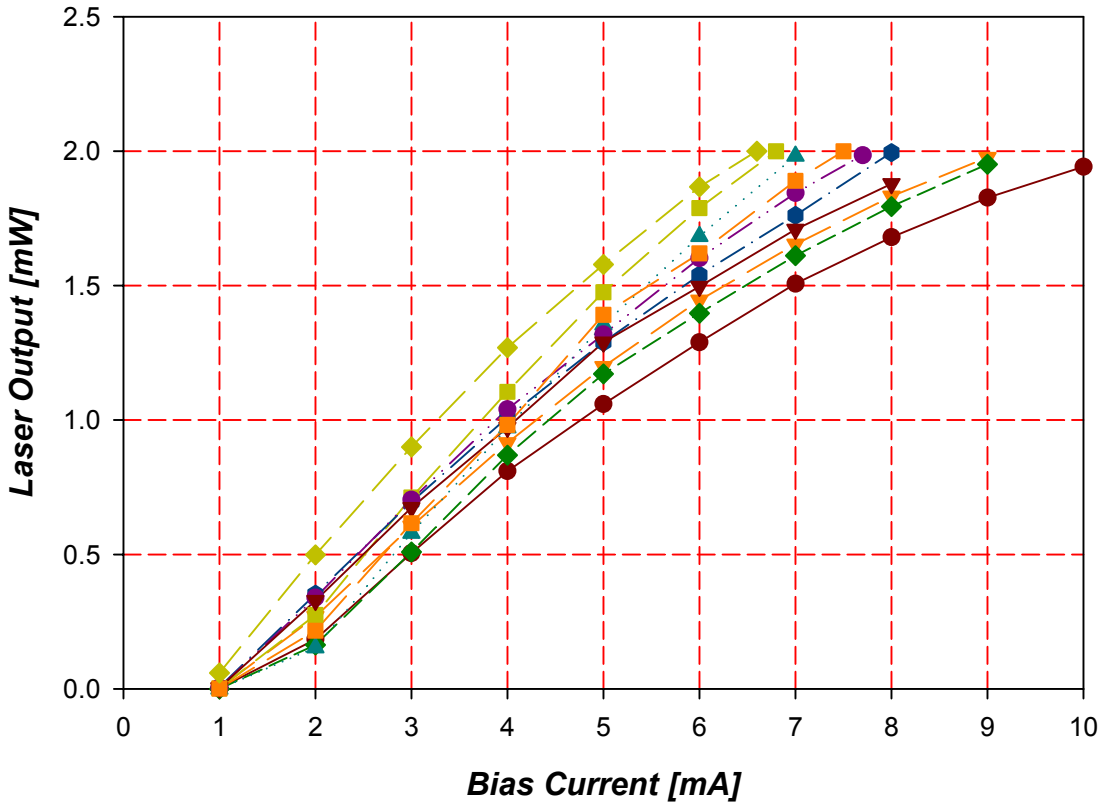


Figure 3.5 Light-Current (L-I) characteristics of a 15µm diameter 1X12 linear VCSEL array.

The I-V characteristics of the various thick VCSEL is shown in Figure 3.6. VCSEL was thinned down to 250µm, and then its I-V characteristic is measured. Next this VCSEL is thinned down to 200µm again and measured. Thinning and measuring

steps were repeated untill whole substrate is completely removed. The diameter of the current aperture was 18μm. Thinner VCSEL shows low serial resistance than thick device at the same current level. This is caused from reducing thickness of resistive GaAs substrate and better heat dissipation.

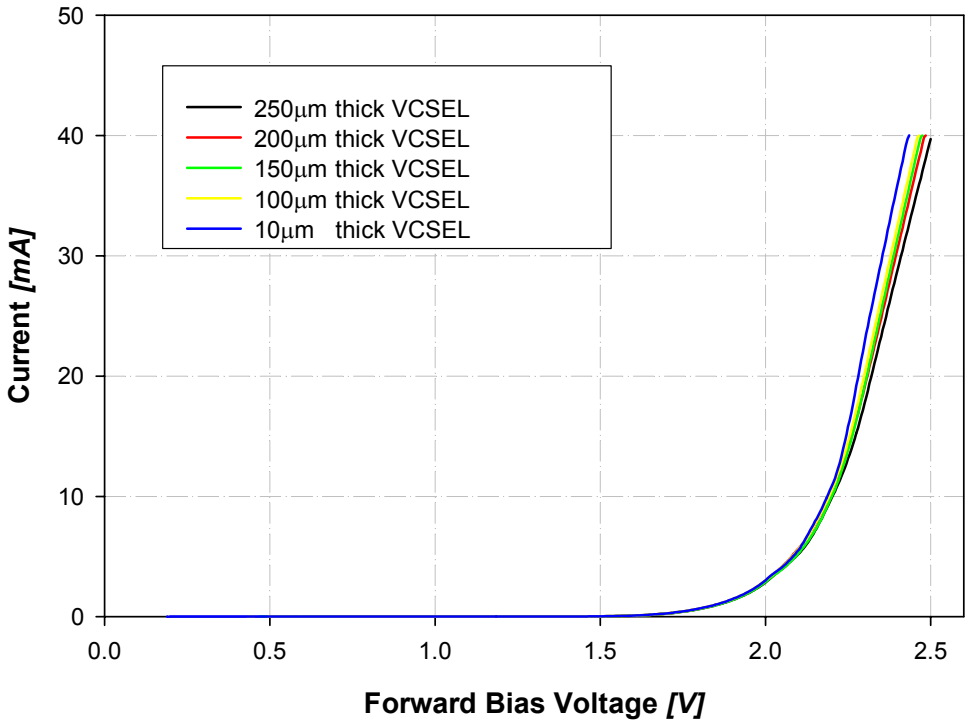


Figure 3.6 Current –Voltage characteristics of different thickness 18μm diameter VCSELs.

The difference of characteristic for VCSELs with various thicknesses is clearly appeared in light to current characteristic. L-I characteristics of 250,200,250,100 and 10μm thick VCSELs are shown in Figure 3.7. Threshold current density was 393A/cm^2 corresponding to 3mA threshold current and 18μm aperture diameter. The quantum efficiency of the 10μm thick VCSEL is increased by ~50% when the driving current is

above 9mA. The reduced temperature of the active region due to higher thermal conductance increases optical gain in quantum well [28,29]. When substrate is removed, the VCSEL (10μm thick) shows linear dependency even at a high injection current.

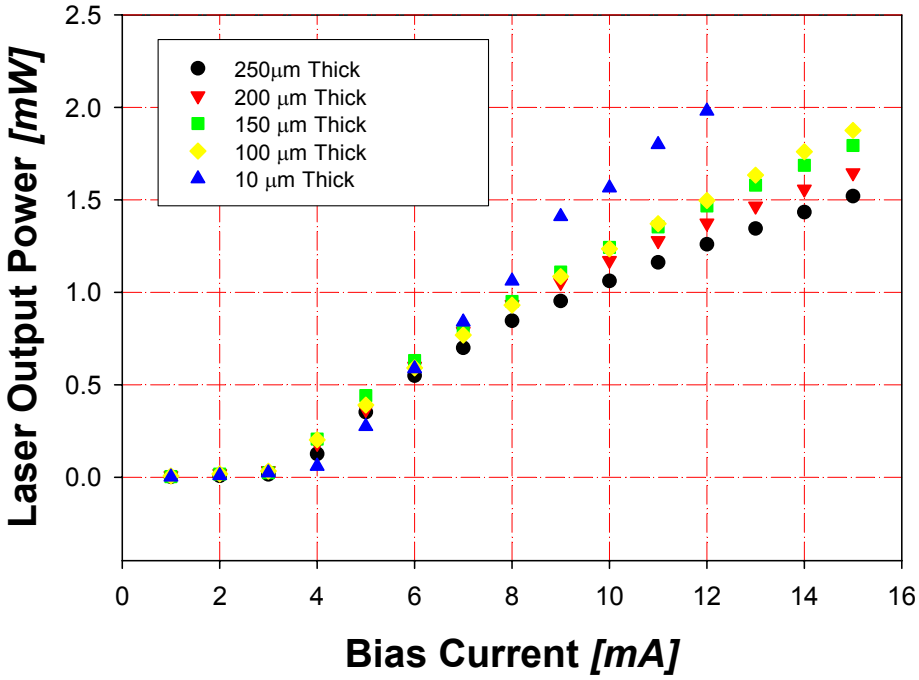


Figure 3.7 Light-Current (L-I) characteristics of different thickness 18μm diameter VCSELs.

3.2 HIGH SPEED MODULATION CHARACTERISTICS

The modulation characteristics of VCSEL can be predicted by relaxation resonance. If bias current is far above threshold, the frequency of relaxation resonance is given by Equation 3.1.

$$f_R = \frac{1}{2\pi}\left[\eta_i \frac{\Gamma \upsilon_g}{qV}\frac{\delta g}{\delta N}(I - I_{th})\right]^{1/2} \qquad \text{Equation 3.1}$$

η_i is internal quantum efficiency, g is gain, N is carrier density at given bias, V is the volume of active region, Γ is confinement factor. From Equation 3.1, VCSEL can be modulated with very high speed because of small active volume. If damping and parasitic are not large, 3dB modulation bandwidth is about 1.55 f_R [30]. The next most important factors limiting modulation bandwidth are parasitic capacitance and heat. For high speed modulation, lower pad capacitance is required.

The measurement of modulation property is little cumbersome because electrical pads are not co-planar. 4GHz bandwidth probe (Cascade) which has three fingers (GSG) was used to feed drive signal. To test high speed modulation property, we have to provide path with low impedance. The problem is the ground contact pad is not on the top surface. Therefore special biasing is required. Biasing schematic is shown in Figure 3.8. A VCSEL to be measured is fed by modulated signal. And neighboring VCSELs are tied to ground. The bottom electrode is biased with negative voltage through an inductor. Two neighboring VCSELs with reverse bias are in conducting state, i.e. low resistance. Modulated signal drives VCSEL to be measured and flows to lower potential. However, even if bottom electrode is biased with negative potential, modulated current can not flow through the inductor because the inductor acts like a giant resistor at high frequency. As a result, the current flows through neighboring VCSELs. Low impedance path is established.

To measure eye diagram, nonreturn to zero (NRZ) pulse was directly applied to VCSEL, and DC -2V is applied to the inductor. Single mode optical fiber was placed close to the VCSEL to tap a light signal. The tapped light was fed to digital oscilloscope through single mode optical fiber. Eye diagram operating at 1GHz and 2.25GHz are shown in Figure 3.9. There was a 100ps jitter in the eye diagram due to the turn on delay of VCSEL. If high quality signal and increasing bias voltage are feed to the device, jitter will be decreased.

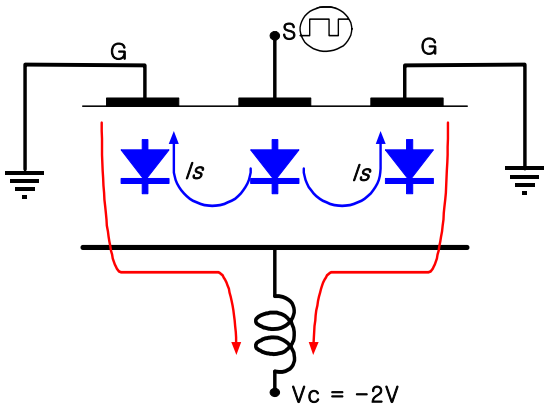
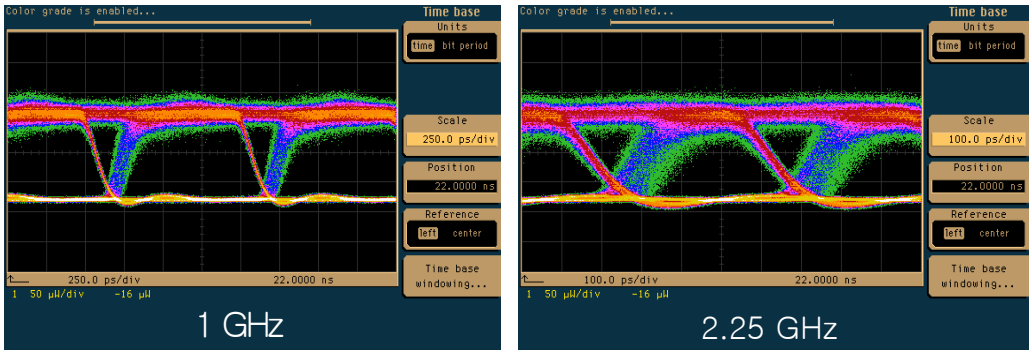


Figure 3.8 Biasing schematic for high speed measurement.



(a) (b)

Figure 3.9 Eye diagrams of modulated VCSEL at 1GHz (a) and 2.25GHz (b).

3.3 THERMAL RESISTANCE

The thermal resistance can be calculated from the shift of measured wavelength as a function of substrate temperature and power dissipation. The thermal resistance is given by $R_{th} = \Delta T / \Delta P = (\Delta\lambda / \Delta P)/(\Delta\lambda / \Delta T)$, where ΔT is the change of junction temperature, ΔP is the change of injected power and $\Delta\lambda$ is wavelength shift. The junction temperature can not be measured directly, however, shift of lasing wavelength is related with the junction temperature. Both $\Delta\lambda / \Delta P$ and $\Delta\lambda / \Delta T$ are experimentally confirmed.

The device under test (DUT) was laid on the top of the gallium indium eutectic metal which is used to make an electrical contact. The substrate temperature was controlled by a thermo-electric cooler (TEC).

The measured wavelength shift as a function of temperature ($\Delta\lambda / \Delta T$) for all devices was 0.75 Å/^{o}C at constant power dissipation. The wavelength shifts as a function of net dissipated power ($\Delta\lambda / \Delta P$) were 0.59, 0.54, 0.5, 0.43, 0.36 Å/mW, respectively, corresponding to 250, 200, 150, 100, and 10μm thick VCSELs as indicated in Figure 3.10. The thermal resistances for 250, 200, 150, 100, and 10μm thick VCSELs were measured to be 772, 710, 657, 572, and 478^{o}C/W, respectively. Note that the thickness of the 10-μm thick VCSEL has an exclusive advantage of heat management due to the reduction of the thermal resistance shown herein.

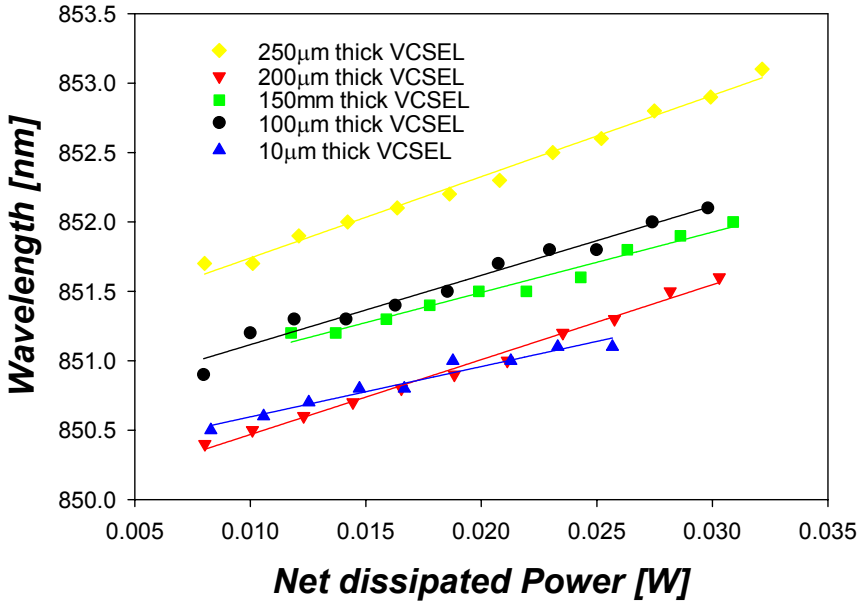


Figure 3.10 Wavelength shifts as a function of dissipated power ($\Delta\lambda/\Delta P$) for different thick VCSEL.

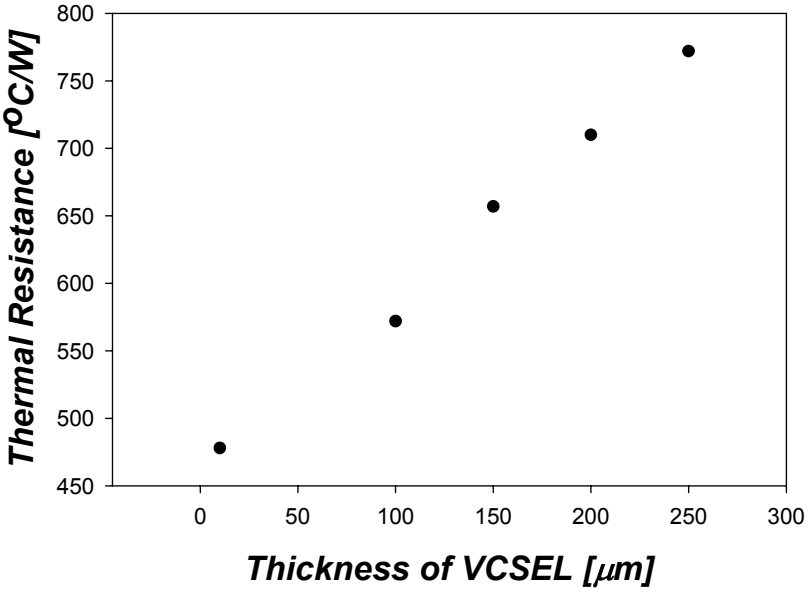


Figure 3.11 Measured thermal resistances of various thick VCSELs.

Chapter 4: Thermal management of Embedded VCSEL

4.1 INTRODUCTION

All optical components such as light sources, channel waveguides, waveguide couplers and detectors are inserted within electrical layers in a fully embedded board level optical interconnection as indicated in Figure 1.8. However, in this configuration, The VCSEL array raises thermal management concerns because it is encapsulated with thermal insulators such as polymer waveguides and bonding film (pre-preg). Only the common bottom metal contact of the VCSEL array can be used as a thermal interface. The improper heat dissipation can lead to thermal runaway. The increasing temperature leads wavelength shift, increasing a threshold current, reducing quantum efficiency, shorten device life time, and dissipating more power. Therefore, the heat management of the driving VCSEL array is a critical issue in the fully embedded structure. Yung-Chen Lee *et al.* reported the thermal management of a VCSEL based optical module [31] and Rui Pu *et al.* reported the thermal resistance of a VCSEL bonded to an IC [32]. Both papers presented valuable results but not applicable to our architecture.

Following section describes the simulated results of the thermal resistance of the VCSEL, fully embedded in PCB, as a function of the VCSEL's thickness and determines the effective heat sink structure.

4.2 TWO DIMENSIONAL FINITE ELEMENT ANALYSIS

The VCSEL is a major heat source in a fully embedded guided-wave optical interconnects. The embedded VCSEL arrays are thermally isolated by surrounding insulators; therefore, heat builds up and the operating temperature increases. The high operating temperature may reduce life time of the device and the laser output power. The reliable operation of the VCSEL is accomplished through proper heat management. Effective heat removal is a challenging task in the embedded structure because we have to consider packaging compatibility to the PCB manufacturing process while providing an effective and simple cooling mechanism.

The innovated heat management system for the fully embedded approach is introduced. The key idea is using an n-contact metal affiliated with the bottom DBR mirror of the VCSEL die as a heat spreader, and a part of the heat sink by directly electroplating with copper during the integration process. In general, thermally conductive paste (usually contains fine metal flakes) was used for low power laser diode packaging. In a high power laser diode packaging, the gold-tin (Au-Sn) eutectic alloy was used to bond LD on heat sink. The thermally conductive paste has a ten times smaller thermal conductivity than that of copper. Therefore, thermally conductive paste can not be used because it has a lower thermal conductivity than copper.

Usually several tens of micrometer thick copper was deposited in copper contained acid chemical solution during PCB process. It can be used as a very good electrical and thermal passage, simultaneously.

The thermal resistance of a buried VCSEL depends on the device structure and the packaging structure. Once the device was designed there is no other ways to change thermal resistance of the device. The direct bonding of the device using Cu electroplating reduces thermal resistance of the device due to the absence of the lower thermal conductivity bonding epoxy.

Thermal resistance can be calculated by solving thermal diffusion equation [Equation 4.1].

$$\frac{\partial T}{\partial t} = \frac{k}{\rho C_p}\nabla^2 T + \dot{q}\frac{1}{\rho C_p} \qquad \text{Equation 4.1}$$

here, T is the temperature, k is the thermal conductivity, ρ is the material density, C_p is the specific heat, and $\dot{q}$ is the heat generation rate. For steady state and constant heat generation case, the Equation 4.1 turns into simple Poisson's equation [Equation 4.2].

$$k\nabla^2 T + \dot{q} = 0 \qquad \text{Equation 4.2}$$

Once temperature difference (ΔT) between device and heat sink was known, thermal resistance (R_{th}) of the embedded VCSEL can be calculated by Equation 4.3.

$$R_{th} = \Delta T / \Delta P \qquad \text{Equation 4.3}$$

Here, ΔP is the dissipated power.

ANSYS software was used to perform a 2-D finite element thermal distribution analysis. The thermal conductivities of GaAs, DBR mirror and copper are 4.6 X 10^{-5} W/μm·K, 2.3 X 10^{-5} W/μm·K, and 4 X 10^{-4} W/μm·K, respectively [33], [34]. As VCSEL parameters, active diameter of 18μm and the thickness of 0.3μm were used.

Heat is generated due to the Bragg reflector's resistance and imperfect conversion efficiency in active region. However, the heat generated due to the DBR is relatively small compared with the active region, therefore we ignored this term in our simulation [32]. The heat generation rate in active region (circular shape, diameter of 18μm) is based on measured value which is 20mW per VCSEL.

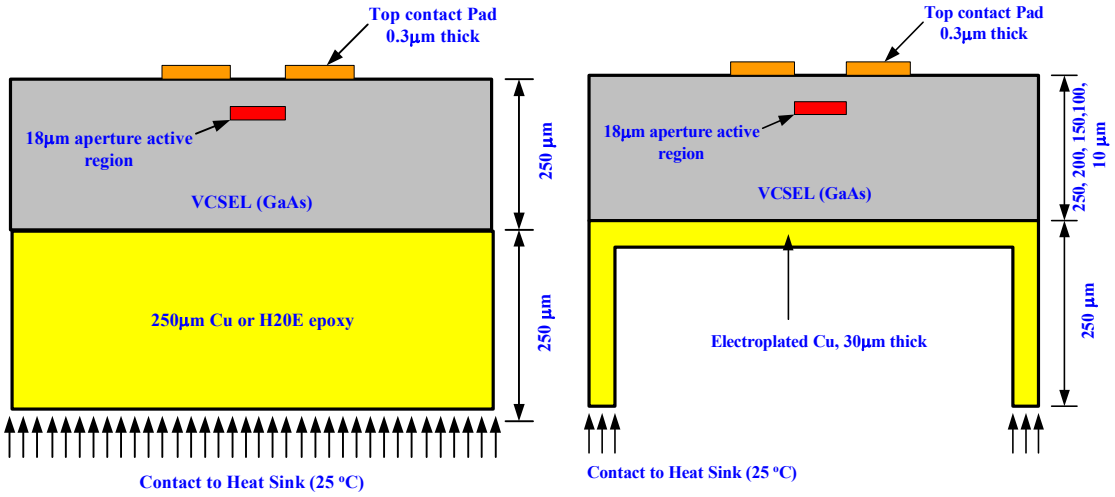
Table 4.1 Thermal conductivities of materials.

Material	Thermal Conductivity [W/μm K]	Material	Thermal Conductivity [W/μm K]
GaAs	4.6 X 10^{-5}	Au	3.2 X 10^{-4}
AlGaAs DBR	2.3 X 10^{-5}	Au/Sn(80:20)	6.8 X 10^{-5}
H20E (Thermal paste)	2.9 X 10^{-5}	Si	1.5 X 10^{-4}
Copper	4 X 10^{-4}	FR-4	1.7 X 10^{-7}

We compared two different cooling structures as depicted in Figure 4.1. One is 250μm thick bulk copper as a conductive material (Figure 4.1a) and one is a 30μm thick electrodeposited copper film (Figure 4.1b). Producing 250μm thick copper in real packaging is nearly impossible. To overcome realization of thick heat sink, the

electroplated copper foil on the back side of VCSEL was introduced. We chose the 30µm thick copper film as a heat sink because this is the thickness of the copper trace in the electrical layer of the PCB. The copper film can be directly electro-deposited on the n-contact metal pad (Au-Ge/Ni/Au) of the VCSEL array during the electroplating step. The shape of the copper foil heat sink looks like rectangular shape cap. During the simulation the bottom surface of the copper block or thermal conductive paste or copper foil is maintained at 25°C.

Figure 4.2 is the automatically generated triangular mesh profile for 10µm thick VCSEL on the copper foil. The simulation results are shown in Figure 4.3~4.6. Note that the bottom portion of the drawing was truncated in Figure 4.2.



(a) (b)

Figure 4.1 Two types of embedded heat sink structure. (a) 250µm thick electroplated copper or thermal conductive paste (H20E™, Epotek), (b) 30µm thick electroplated copper film.

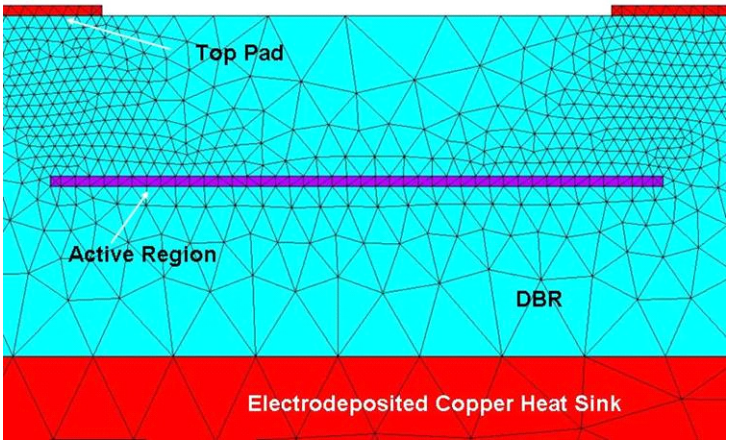


Figure 4.2 Generated 2D mesh structure for 10μm thick VCSEL and 30μm thick electroplated copper film

To validate the simulation results, typical measuring setup with various thick VCSELs were also simulated and then the results were compared to measured results. Figure 4.3 shows temperature distribution of various thick (250μm, 200μm, 100μm, and 10μm) VCSELs attached on gold coated silicon wafer using Indium-Gallium eutectic metal. Temperatures at the active region were reached 39.5, 37.9, 36.9, and 34.9°C for 250μm, 200μm, 100μm, and 10μm VCSEL, respectively. Corresponding thermal resistance were 725, 645, 595, and 495 K/W. The measured and calculated thermal resistances of the devices are summarized in Figure 4.4. As shown in Figure 4.3, the calculated thermal resistances of the devices are well matched with the measured results. According to this result, the simulation model and process were properly carried out.

For the 250μm thick copper heat sink block, the temperature at the active region reached 39.4°C corresponding to a thermal resistance of 722K/W (Figure 4.5a). Despite

of lower thermal resistance of the 250μm thick copper heat sink block, this structure is not realistic in a fully embedded structure due to difficulty in producing this thickness by electroplating.

For 250μm thick thermal conductive paste of instead of copper block, junction temperature reaches at 45.9°C corresponding to a thermal resistance of 1045K/W which is 44% higher than that of copper block. Due to the high thermal resistance of integrated VCSEL thermal conductive paste can not be used for a fully embedded application.

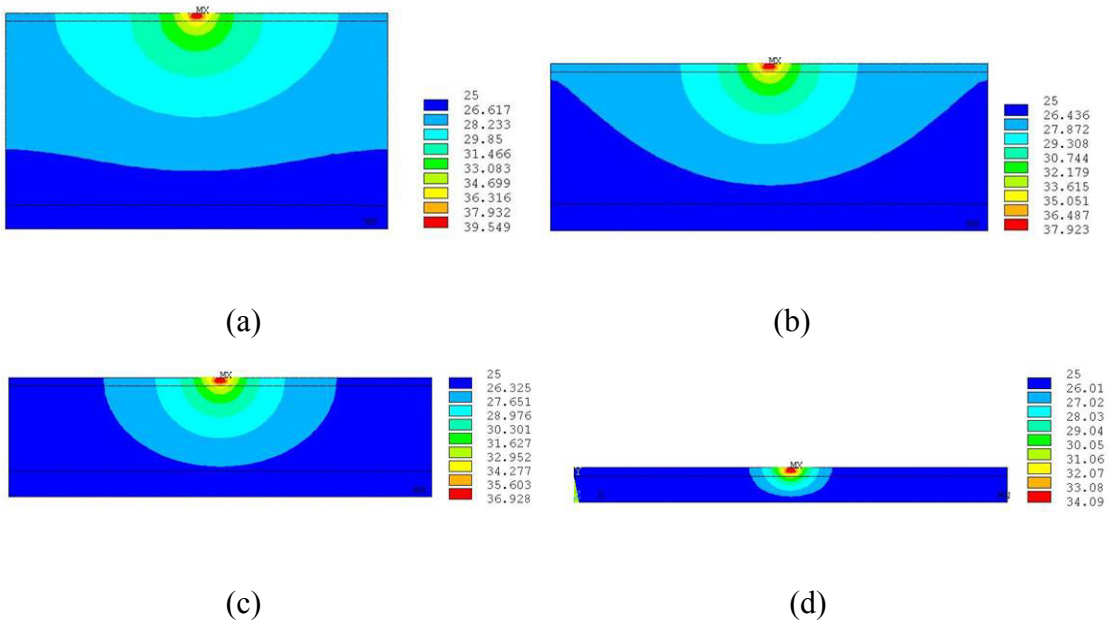


Figure 4.3 Temperature distributions of various thick VCSELs with In-Ga eutectic metal interface between VCSEL and gold plated Si wafer. (a)250μm , (b)200μm, (C)100μm, (d)10μm thick VCSEL

For the case of a 30μm thick electrodeposited copper film heat sink with 10μm thick VCSEL, the junction temperature reached 34.58°C as in Figure 4.6(d) corresponding to thermal resistance of 455K/W. The higher junction temperature reduces the quantum efficiency and finally causes catastrophic failure of the device. Figure 4.7 shows theoretically determined thermal resistances for VCSELs with various thicknesses. For a 30μm thick electroplated copper film, the junction temperatures were theoretically determined to be 43.8, 43, 42.2, 41.5, 40.2 and 34.6°C for 250, 200, 150, 100, 50 and 10μm thick VCSEL, respectively. The substrate removed VCSEL having a total thickness of 10μm shows superior optical and thermal characteristics.

Although the substrate removed VCSEL has superior properties, fabrication and handling are very difficult. If we assume that thermal resistance of the normal thickness VCSEL (250μm thick) packaged on bulk copper heat sink is a reference for reliable operation, maximum thickness of an embedded VCSEL will be 70μm according to simulation results. Several tens micrometer thick device can be easily fabricated and handling of the device is much easier.

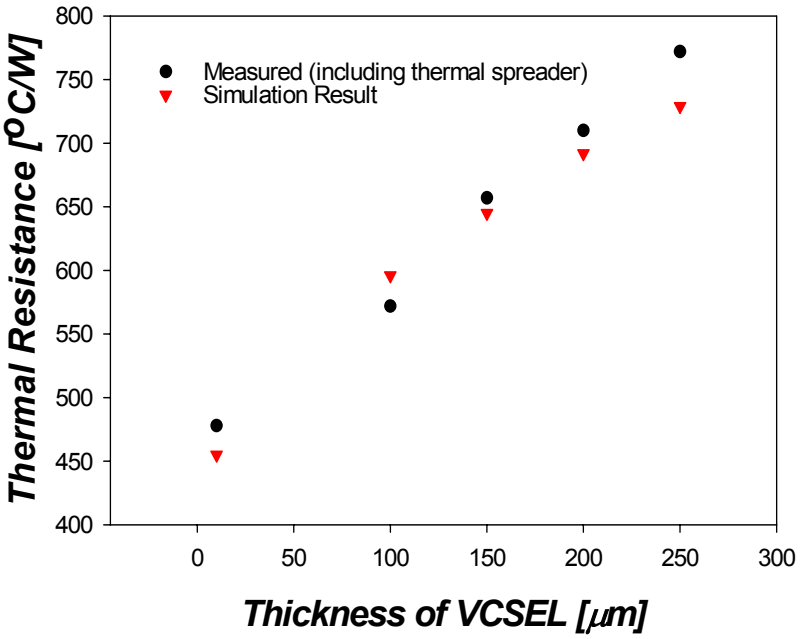
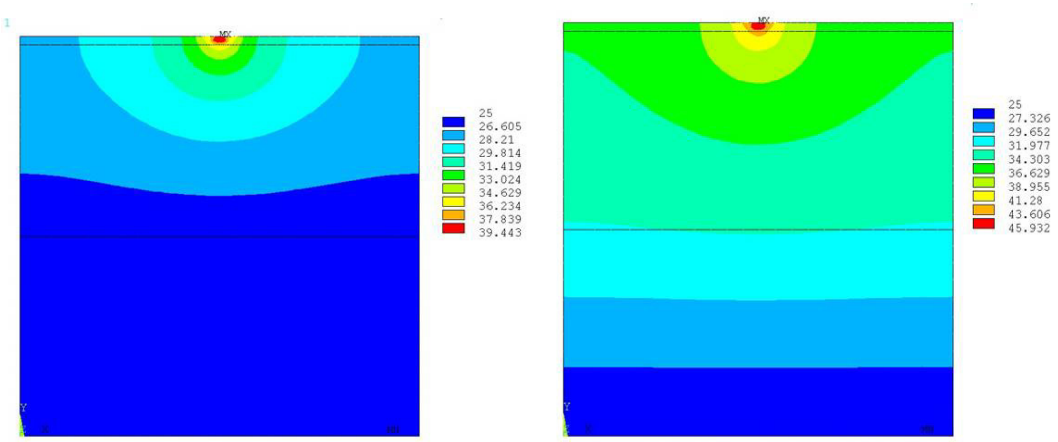
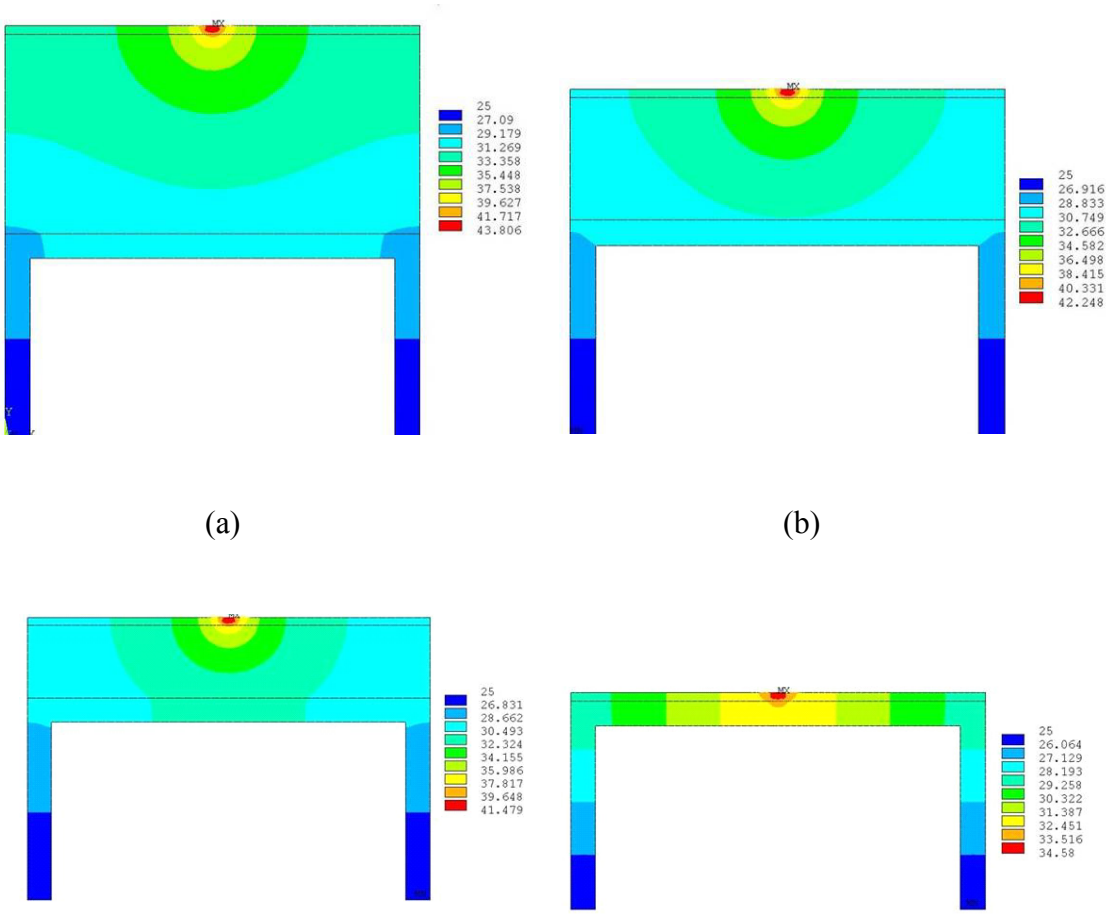


Figure 4.4 Comparison of measured and calculated thermal resistances for various thick VCSELs [Active area : diameter of18μm, height of 0.3μm]



(a) (b)

Figure 4.5 Temperature distribution of 250μm thick VCSEL. (a) 250μm thick electroplated copper heat sink, (b) 250μm thick thermal conductive paste heat sink (H20E, Epotek)



(a) (b)

(c) (d)

Figure 4.6 Temperature distributions of various thick VCSELs with 30μm electroplated copper film heat sink. (a) 250μm, (b) 150μm, (C) 100μm, (d) 10μm thick VCSEL

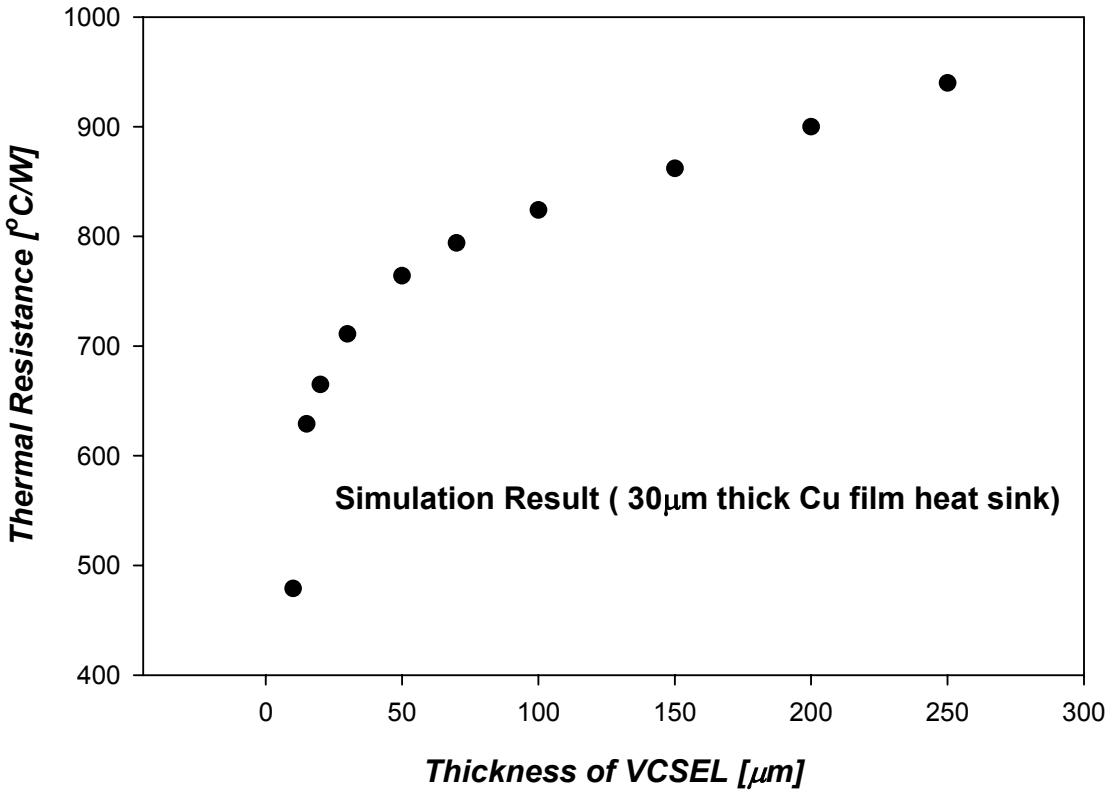


Figure 4.7 Calculated thermal resistances of various thick embedded VCSELs

Chapter 5: Optical Interconnection Layer

5.1 INTRODUCTION

The optical interconnection layer (OIL) is a key component in fully embedded board level optical interconnects. Due to the fully embedded structure in PCB, optical waveguide film must be thin and flexible. Furthermore light source (VCSEL), and photo-detector also should be thin enough. There are many problems to be solved.

1. Compatibility with industrial standard PCB process
2. Low cost material and process
3. Manufacturability
4. Reliability

The compatibility with PCB process means that the OIL should be treated like a traditional electrical layer and survive under harsh PCB lamination environments. Molding process or imprinting is the most suitable method for low cost approach and manufacturability. The materials of the OIL should have well matched thermal expansion coefficients to prevent delamination. The integration of the VCSEL and the photo-detector onto the waveguide film should be easy and robust. And the integrated OIL must provide good heat sink or spreader for reliable operation of the VCSEL.

In this chapter, micro-mirror coupler and the fabrication technique of flexible waveguide will be explained.

5.2 WAVEGUIDE MICRO-MIRROR COUPLER

To efficiently couple optical signals from vertical cavity surface emitting lasers (VCSELs) to polymer waveguides and then from waveguides to photo-detectors, two types of waveguide couplers are investigated. They are tilted grating couplers and 45^{o} waveguide mirrors. There are a large number of publications in grating design [35, 36, 37, 38, 39]. However, the surface-normal coupling scenario in optical waveguides has not been carefully investigated so far. The profile of tilted grating greatly enhances the coupling efficiency in the desired direction. The phenomenon of grating-coupled radiation is widely used in guided-wave optical interconnects. Very often, coupling in a specific direction is required. To achieve this unidirectional coupling, the tilted grating profile is selected as a high-efficiency coupler. A very important aspect of manufacturing of such coupler is the tolerance interval of the profile parameters, such as the tooth height, the width and the tilt-angle. However the tilted grating coupler has inherent wavelength sensitivity and is not applicable for planarized waveguide.

The 45° waveguide mirror coupler is a very critical component in optical interconnection applications especially in planarized lightwave circuits (PLC). The mirror can be incorporated with a vertical optical via to enable 3D optical interconnects and couples light to the waveguide. The 45^{o} waveguide mirror is insensitive to the wavelength of light and has high coupling efficiency. There are various techniques to fabricate 45^{o} mirror such as laser ablation [40], oblique reactive ion etching (RIE) [41], temperature controlled RIE [42], re-flow [43] and machining [44]. The laser ablation method is subjected to lower throughput and surface damage. The oblique RIE method is

limited by directional freedom. The temperature controlled RIE method is free from directional freedom but the quality of the mirror depends on process and materials. The re-flow method is also subjected to lower throughput. The machining provides good surface profile; however, it is difficult to cut individual waveguide on a substrate due to the physical size of the machining tool. We developed a new fabrication method using a microtome blade.

5.2.1 Coupling efficiency calculation

The coupling efficiency is one of the most critical issues in the fully embedded optical interconnects because of the concerns about thermal management and crosstalk. Higher coupling efficiency between waveguide and VCSEL or detector enables the lower power operation of VCSEL. Furthermore, when small aperture VCSEL is used to operate at a high speed, for example, 3μm aperture for 10GHz operation, the coupling efficiency is paramount concern because of the large spatial divergence of VCSEL's light. A large aperture selectively oxidized VCSEL operates in multiple transverse modes due to the strong index confinement created by oxide layer with low refractive index [45]. Various techniques were introduced to operate in single transverse mode [46,47,48]. Real spatial distribution of the VCSEL is not the same as Gaussian profile; however, we can consider it as Gaussian profile by ignoring small discrepancies. This assumption result in a simple calculation. Another assumption is that lights within acceptance angle of waveguide are totally coupled into the waveguide. There are about 10 supporting modes in the 50μm

square waveguide with Δn=0.01. For an exact calculation, we have to consider all the modes, but the number of mode is quite large. It can be treated as geometrical optics.

To calculate coupling efficiency, we need to know intensity distribution and propagation angle at 45° mirror facet. Figure 5.1(a) illustrates waveguide with 45° mirror coupler and transparent substrate. The VCSEL is bonded to the substrate; hence, laser light travels through the substrate and bends at right angle at the mirror facet. The transparent substrate is optically isotropic. Figure 5.1(b) illustrates Gaussian beam propagation in homogeneous medium.

Propagation angle at mirror surface ***θ (r,z)*** can be calculated from the radius of curvature of wavefront ***R(z)*** and distance from center ***r*** [49]**.**

$$\theta(r,z) = \tan^{-1}\left(\frac{R(z)}{r}\right) \qquad \text{Equation 5.1}$$

The radius of curvature ***R*** at any ***z*** of the wave-front is given by equation

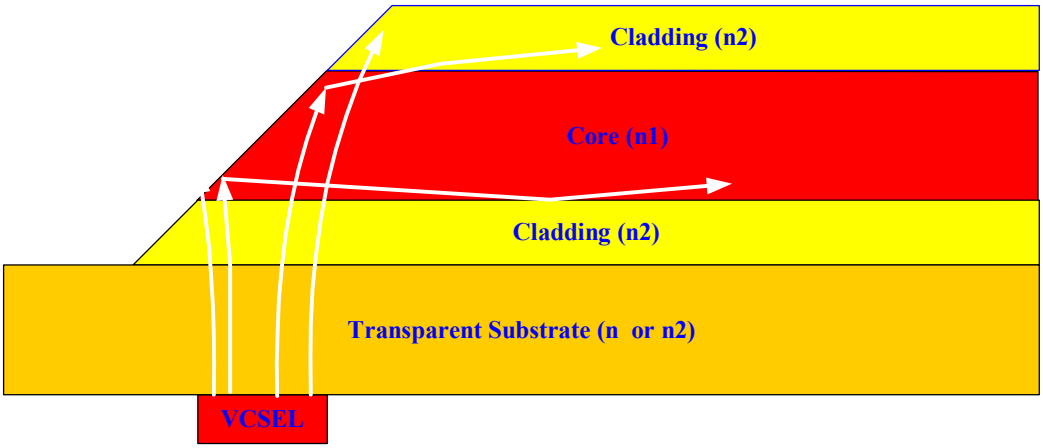
$$R(z) = z\left(1 + \frac{\pi\omega_0{}^2 n}{\lambda z}\right) \quad , \quad z_0 = \frac{\pi\omega^2{}_0 n}{\lambda}, \quad \omega(z) = \omega_0\sqrt{1+\left(z/z_0\right)^2} \qquad \text{Equation 5.2}$$

where, ***λ*** is wavelength, ***ω_0*** is the beam waist at VCSEL surface and ***ω(z)*** is the beam width at ***z***. The electric field distribution ***E(r,z)*** of Gaussian beam in homogeneous medium is given by

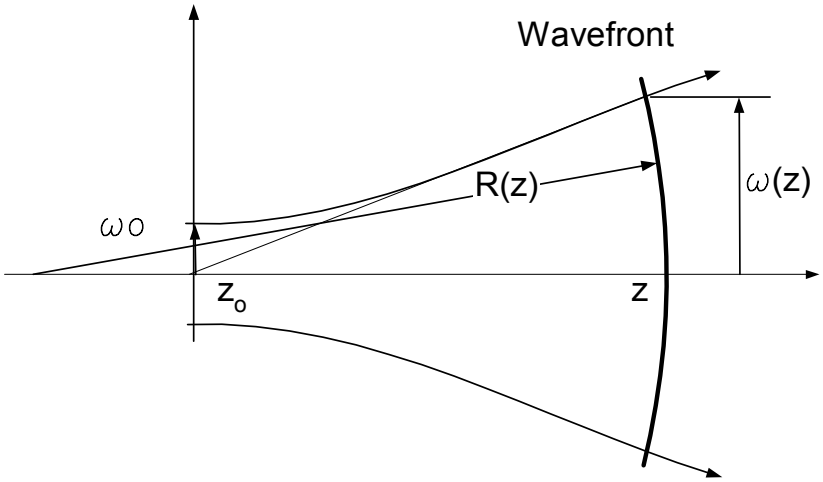
$$E(\mathrm{r},\mathrm{z}) = E_0\frac{\omega_0}{\omega(z)}e^{\left\{-i[kz-\delta(z)]-(r^2)[\frac{1}{\omega^2(z)}-\frac{ik}{2R(z)}]\right\}} \qquad \text{Equation 5.3}$$

and the intensity distribution of the Gaussian beam is

$$I(r,z) = |E(r,z)|^2 = E_0 \left\{ \frac{\omega_0}{\omega(z)} \right\}^2 e^{\left(-2(r^2) \frac{1}{\omega^2(z)} \right)}$$ Equation 5.4



(a)



(b)

Figure 5.1 Coupling Mechanism (a) Diagram of the coupling mechanism (b) Gaussian beam propagation in a homogeneous medium.

Therefore, the coupling efficiency, η, can be calculated by

$$\eta = \frac{\int_{-r_c}^{r_c} |E(r,z)|^2 \, dr}{\int_0^{\infty} |E(r,0)|^2 \, dr} = \left(\frac{\omega_0}{\omega(z)} \right)^2 \int_{-r_c}^{r_c} |E(r,z)|^2 \, dr \qquad \text{Equation 5.5}$$

where, r_c is the maximum radius at the mirror facet which correspond to the acceptance angle of the waveguide.

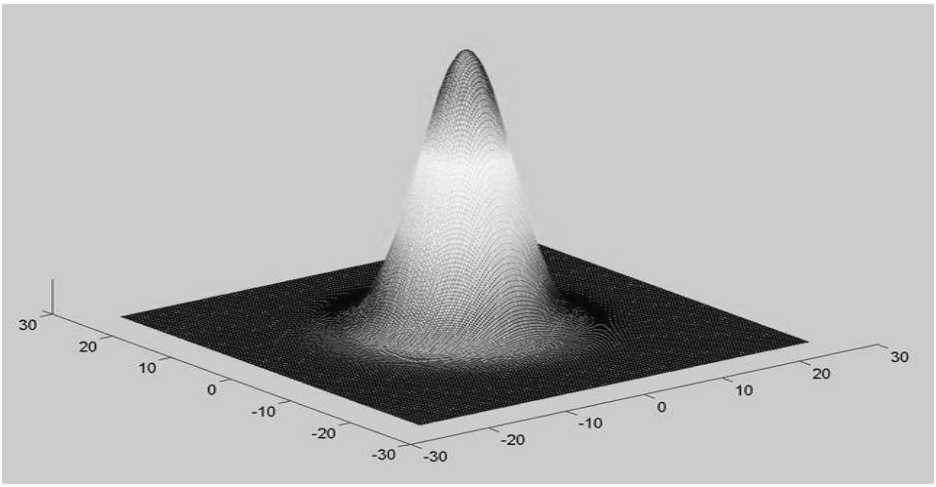
The coupling efficiencies between VCSEL and square (50μmX50μm) waveguide with Δn=0.01(refractive index difference between core and cladding) were calculated as a function of angular deviation from 45°. The substrate thickness (bottom cladding) and the aperture of the VCSEL are 127μm and 12μm, respectively.

Figure 5.2(a) shows the intensity distributions of laser light at the mirror surface, and the coupling efficiencies as a function of angular deviation from 45° for 127μm thick substrate, 50 X 50μm waveguide, and VCSEL with 12μm aperture. The facet of 45° mirror was coated with the aluminum to ensure the reflection because TIR(total internal reflection) does not occur due to the top cladding layer. The reflectance of the aluminum is about 92%. In this scheme all laser lights fall within the mirror. The coupling efficiency is 92% which means nearly 100% of the light is coupled into the waveguide excluding the reflectance due to aluminium. Figure 5.2(b) shows the coupling efficiency as a function of angular deviation from 45°. The coupling efficiency maintains constant values within 45° ± 1.5° mirror angle. Therefore the mirror angle should be kept within 45° ± 1.5°.The coupling efficiency is drops dramatically when the mirror angle is out of the tolerance range (±1.5°).

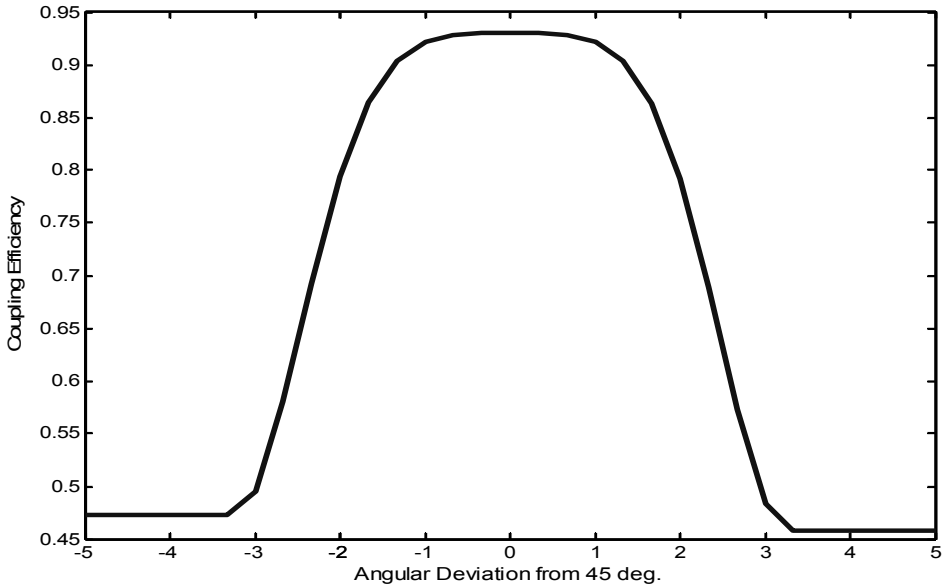
Figure 5.3 illustrates intensity distribution (a) and coupling efficiencies (b) for 3μm aperture VCSEL with substrate thickness of 37μm. Due to the large spatial divergence of the beam, the diameter of the beam spot increases more rapidly as it travels farther; hence, the distance between VCSEL and the mirror is kept short. As a result, the spot size of the beam at the mirror surface is smaller than the mirror. However, large divergence can reduce coupling efficiency. In Figure 5.3(a), the position of the peak intensity is placed at off-center of the mirror. Global intensity distribution of the beam is skewed as the Gaussian distribution for a reason to combine results of the intensity distribution of the beam and distance between the VCSEL and the mirror. The intensity of the light is inversely proportional to the square of the distance. Transverse intensity distribution is reduced by a Gaussian profile. Although all lights hit the mirror surface, some of these lights only coupled into the waveguide. Resultant coupling efficiency is 34% at 45°. However, for 40° tilted angle, the coupling efficiency is increased to 45.4% due to the offset of the intensity distribution at the mirror. Interesting point is that the minimum of coupling efficiency is at the 45° tilt mirror. By increasing or decreasing the angle of mirror from 45°, the coupling efficiency will be increased.

If the distance between the 45° waveguide mirror and the VCSEL increases, some of the laser light hits the out of mirror surface; therefore, coupling efficiency will be dropped. This kind of situation occurs when light source is mounted on the top of PCB. For a small aperture VCSEL, the 45° mirror is not a good coupler as shown in Figure 5.3. To enhance the coupling efficiency, a collimator, different types of coupler

such as curved surface 45° tilted mirror, or a vertical optical via incorporated with 45° mirror will be required.

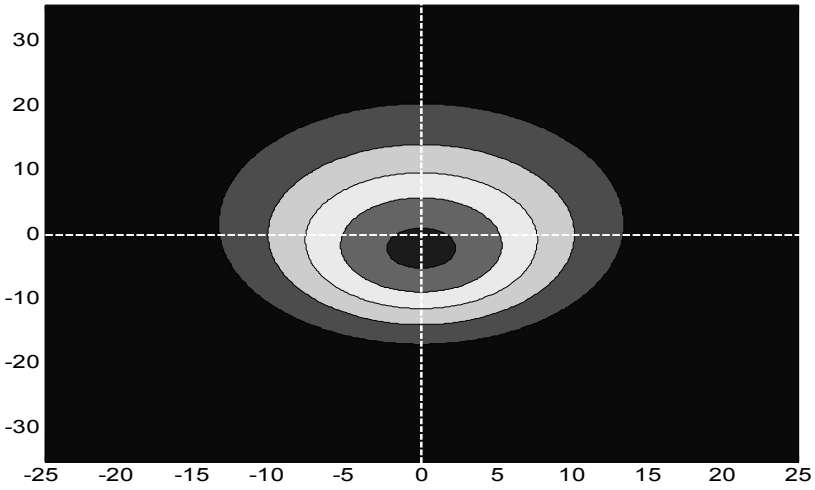


(a)

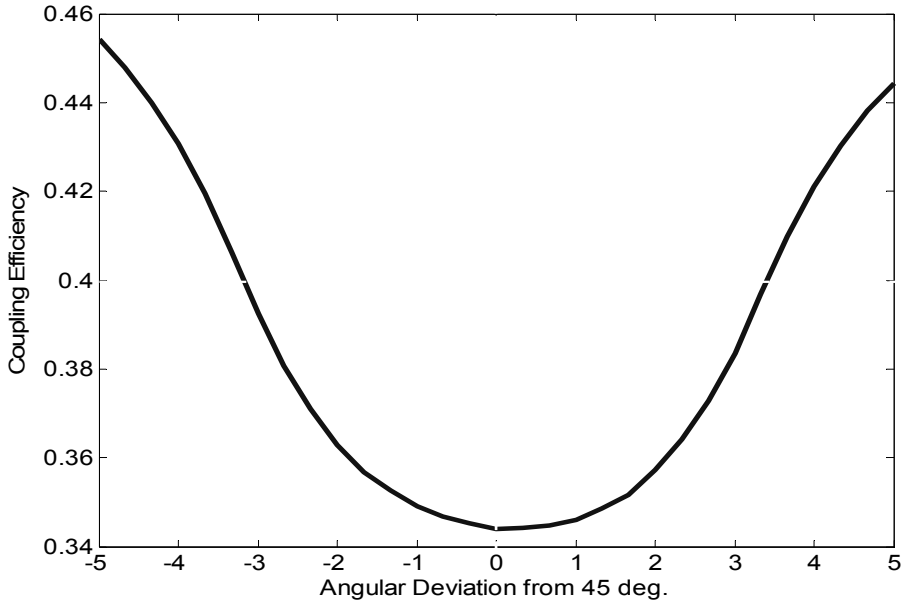


(b)

Figure 5.2 Intensity distributions at the mirror surface for 127μm thick cladding (a), Coupling efficiencies as a function of angular deviation from 45° (b).



(a)



(b)

Figure 5.3 Intensity profile at the mirror surface (a) and coupling efficiencies (b), [VCSEL aperture: 3μm, Cladding thickness: 37μm].

5.2.2 Fabrication of the 45° micro-mirror coupler

Polymers can be cut with a very sharp blade. Based on this fact, a simple fabricating technique was developed. A blade sliding down to the waveguide substrate at 45° slope cuts the waveguides at 45°. It is like a guillotine sliding on a slope. The difference is that the blade of the guillotine falls at the right angle, on the other hand, the blade falls at 45°.

Two kinds of blades were tested. One is the typical razor blade, and the other is micro-machined silicon blade. Because the typical blade is very sharp, it can make a very smooth surface; however, dual edged blade makes it difficult to cut at an exact angle of 45°.

The micro-machined Si-blade also has an extremely sharp edge. Major fabrication process is the anisotropic chemical wet etch of a silicon wafer (Figure 5.4). Silicon nitride film with 1000Å thickness is deposited on a double side polished Si-wafer with <100> orientation in a low pressure chemical vapor deposition (LPCVD) chamber. Then, photoresist coating and patterning steps are followed. The next step is patterning Si_3N_4 film. As a reactive gas, tetrachlorocarbon (CF_4) and oxygen (O_2) mixture was introduced in a RIE chamber. The operating conditions of the RIE were 100W RF power with the flow rate of 65sccm and 38sccm for CF_4 and O_2, respectively.

The following process is the anisotropic wet etching. A basic feature of anisotropic etchants is that their etch rates are strongly dependent on crystallographic orientation. Anisotropic etching is a function of areal density of atoms, the energy needed

to remove an atom from the surface and geometrical screening effect [50]. The <111> planes have an inclination of 54.74º. When the Si-wafer is exposed to anisotropic etchant, etching stops at <111> planes. The potassium hydroxide (KOH) solution of 40% was used as the anisotropic etchant. The chemical reaction equations are [51]

$$Si + 2OH^- \rightarrow Si(OH)_2^{++} + 4e^- \qquad \text{Equation 5.6}$$

$$4H_2O + 4e^- \rightarrow 4OH^- + 2H_2 \qquad \text{Equation 5.7}$$

$$Si(OH)_2^{++} + 4OH^- \rightarrow SiO_2(OH)_2^{--} + 2H_2O \qquad \text{Equation 5.8}$$

The overall reaction is summarized as

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{--} + 2H_2 \qquad \text{Equation 5.9}$$

Final fabrication step is removing Si_3N_4 on the bottom side of the Si-wafer and dicing each blade.

The silicone blade has an apex angle of 54.74°. When the blade tilted at 45°, an angle between the waveguide substrate and the cutting plane of the blade exceeds 90°. [Figure 5.5] The shear strain results from the obtuse angle. As a result of large shear strain, it is more like tearing than cutting. It caused a poor quality cutting plane. Microtome blade has an acute angle and sharp cutting edge; however, it is dual edged. The photograph of two blades is shown in Figure 5.6. The apex angle of microtome blade and micro-machined Si blade are 18.3° and 54.7 °, respectively.

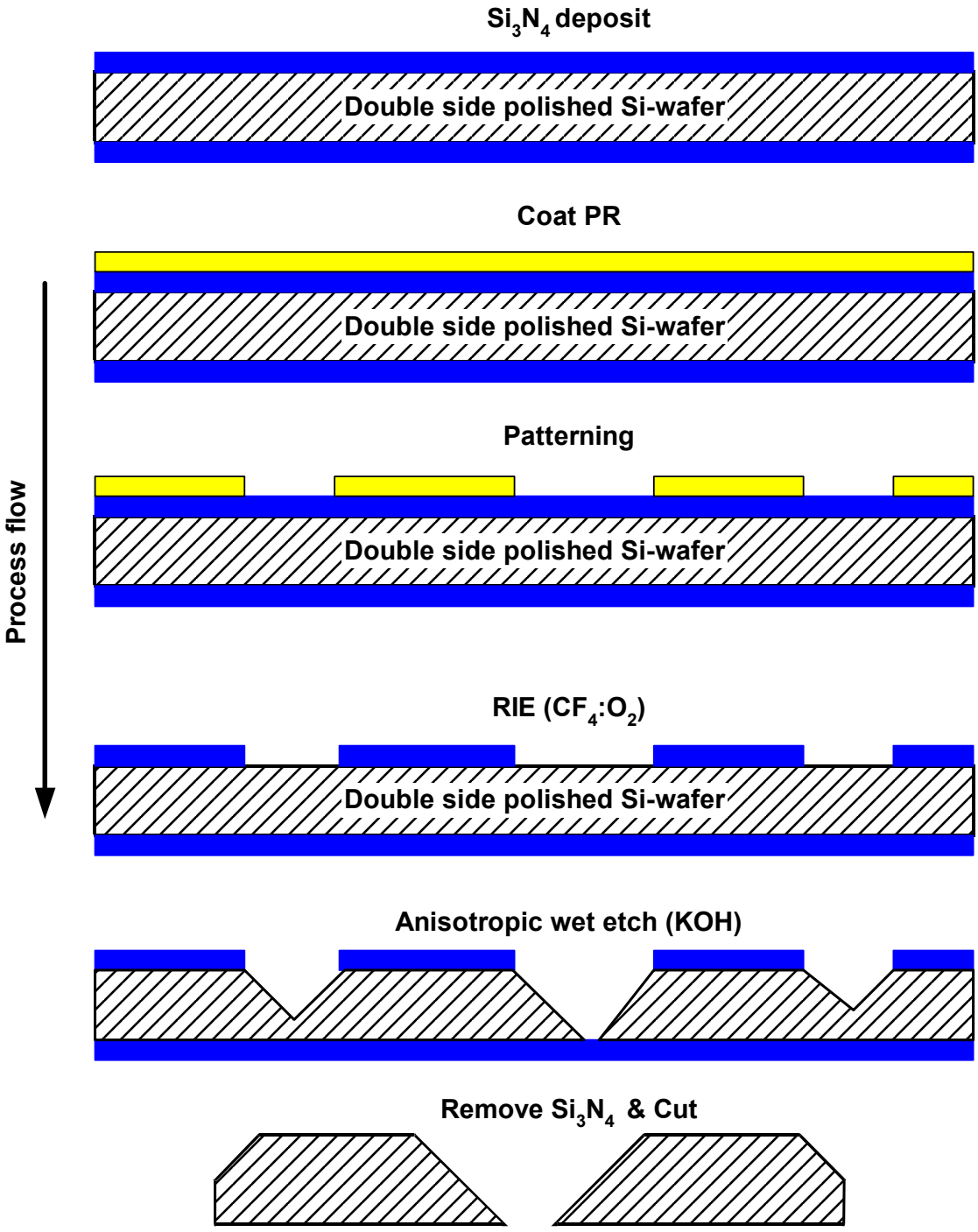


Figure 5.4 Micro-machined Si-blade fabrication process.

The material of master waveguide structure is SU-8 ™ (MicroChem) photoresist. The photoresist (SU-8) was spun on silicon wafer and then developed. Detailed process will be explained in the following section. The fabrication of 45° waveguide mirror was fabricated by tilted microtome setup (Figure 5.7). The master waveguide structure was kept at 120°C on a hot plate. In general, elevated temperature soften polymer. The softness ends up with smoother cutting surface. The blade was sliding down on substrate at 45° slope. The top-off view and surface of the mirror is shown in the Figure 5.8. All waveguides were cut simultaneously by the microtome blade.

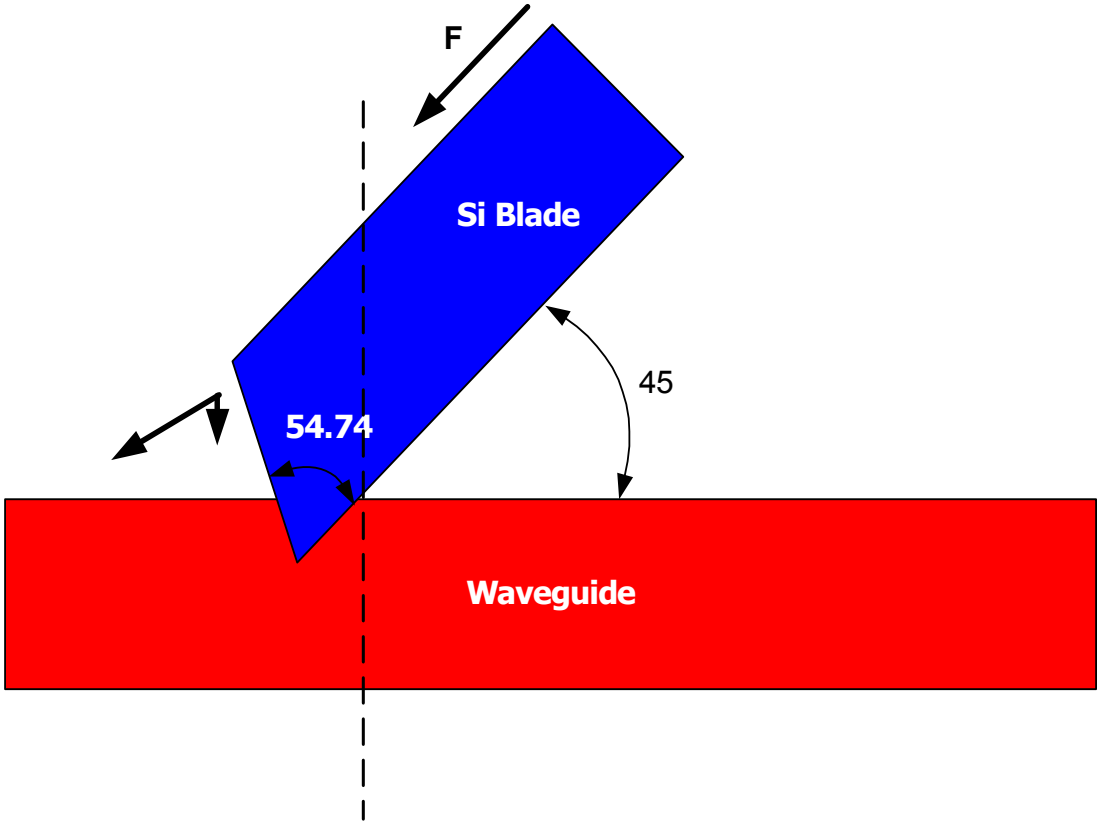
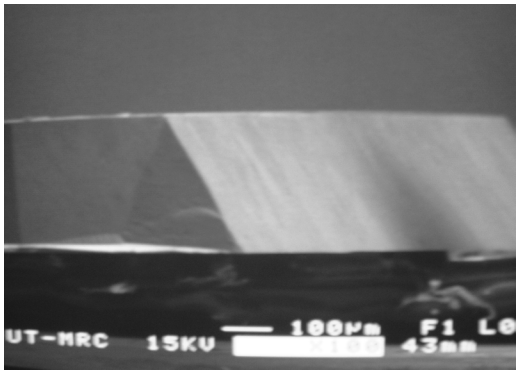


Figure 5.5 Shearing effect by micro-machined Si-blade during cutting.



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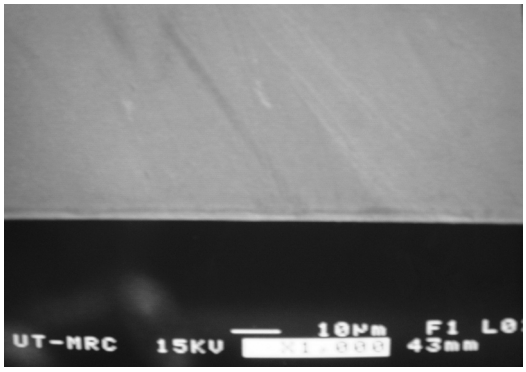

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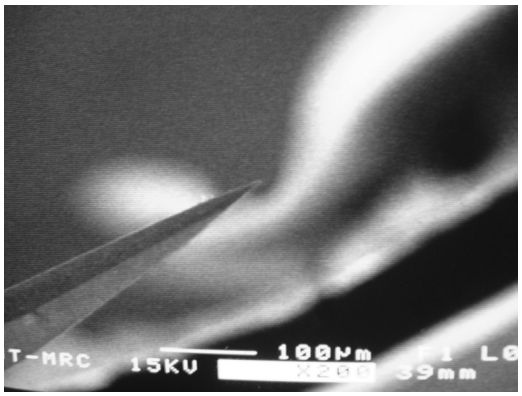
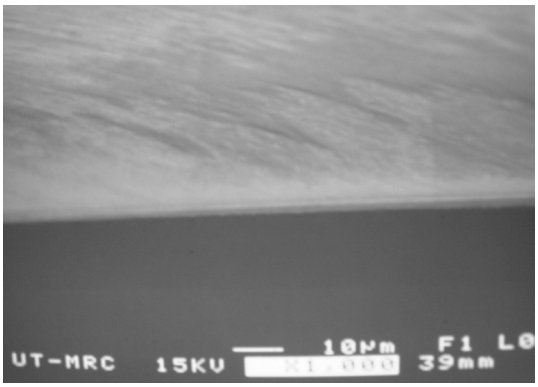


(c)



(d)

Figure 5.6 SEM pictures of (a) micro-machined silicon blade and enlarged view of the blade edge (b), (c) steel microtome blade and enlarged view of the blade edge (d).

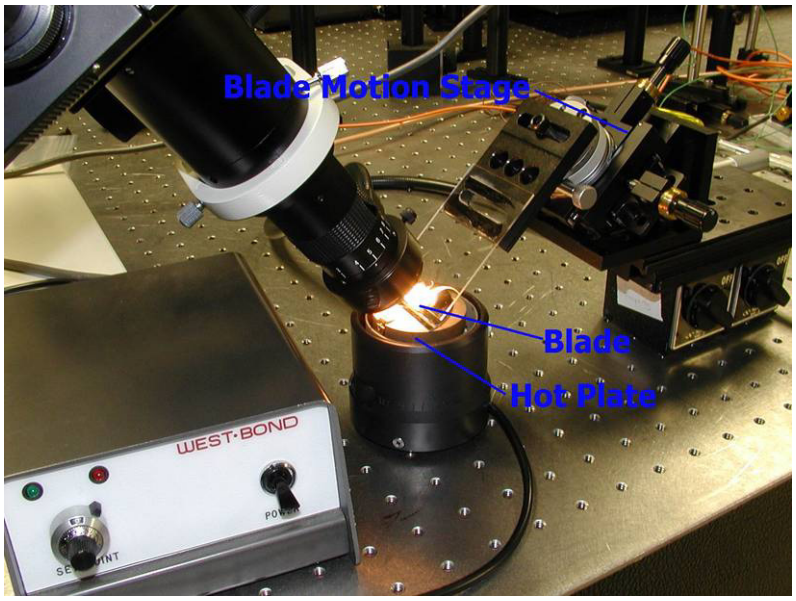
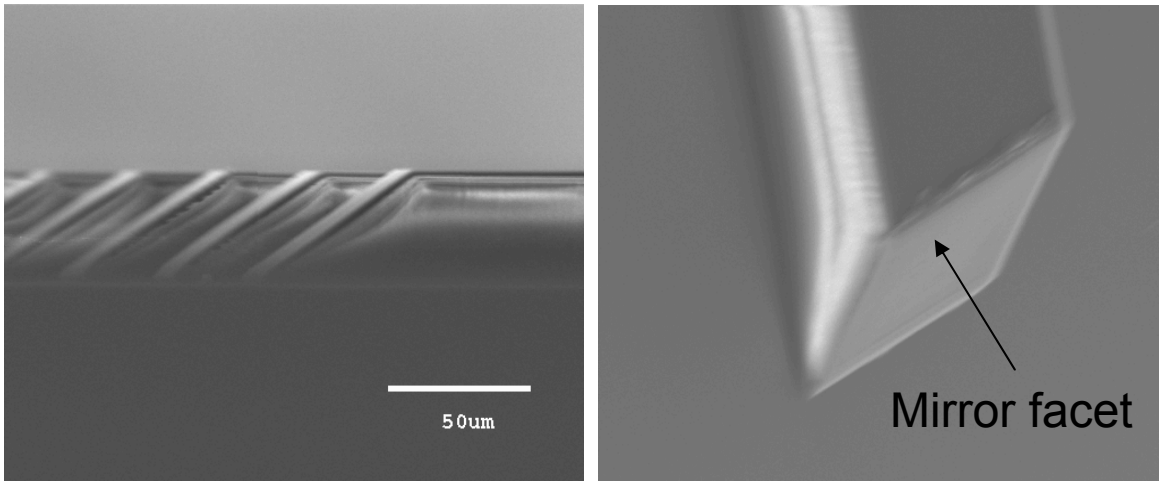


Figure 5.7 45° tilted microtome apparatus setup.



(a) (b)

Figure 5.8 (a) SEM photograph of the waveguide structures with 45^{o} waveguide mirrors (b) Enlarged view of the mirror surface.

5.3 SOFT MOLDING

5.3.1 Introduction

There are various fabricating techniques to define optical waveguide on myriads of substrates. The reactive ion etch (RIE) uses ionized gas to remove material where it is not protected by a mask material in a vacuum chamber. The size of the substrate purely depends on the vacuum chamber. It is relatively free from material selection because RIE is a physical removing process. The lithography uses optically transparent and photosensitive materials. Exposed or unexposed area by UV light makes the material insoluble to solvent due to the cross linking of molecule. However, there is a limitation for choosing material due to the lack of materials which have optical transparency in the interested region and photosensitivity. Hot embossing and molding are indirect fabrication techniques by means of transfering waveguide structure on the substrate. Embossing plate or cast is first fabricated using the master waveguide pattern. Once the plate or the cast was fabricated, the rest of processes are purely replication steps. Therefore, these fabrication techniques are suitable for mass production like stamping of compact disk. Laser ablation technique is similar to carving without a using chisel. Highly intensive UV laser beam removes the material of unwanted region. The motion stage which holds waveguide substrate is moved along the predefined paths. Therefore, processing time is quite long. It is a quite versatile tool for small quantities in fabrication and does not require a mask pattern.

The molding method was chosen in this experiment because of its dependable process and suitability for large volume production even though only a small quantity is

needed in research stage. Solid mold is generally used in various applications such as embossing, optical disk stamping, and Fresnel lens fabrication. The solid mold is made of nickel alloy by electroplating. The fabrication of the solid mold has higher cost and takes a long time. These reasons make us to seek alternative mold materials. Curable resins such as silicone and urethane can be used as an alternative to reduce the fabrication cost and time. The soft mold has been used in various applications such as rubber stamp, small quantity manufacturing, replication, and micromachining. Specially, when the soft mold is used in micro-printing and micromachining, the whole process is usually called as soft lithography.

5.3.2 Master and Mold fabrication

The mold is a negative copy of the master structure. Once the master is fabricated, making the mold is simply pouring a mold material over the master and curing. A silicone elastomer, especially poly(dimethylsiloxane) (PDMS) was chosen to fabricate the mold. The PDMS has several unique characteristics. It has a low glass transition temperature, stable for wide range of temperature (-50 ~200°C), resistance to most chemicals, low interfacial free energy (21.6 dyne/cm), and good thermal stability [52,53].

Master waveguide structure and mold fabrication process is shown in Figure 5.9. The master for the mold was fabricated on a Si-wafer. Multimode waveguide is required for board level interconnection because of the requirement of the lower packaging cost.

Alignment of the devices (laser and detector) and the waveguide is easer when the core size of the waveguide is large.

Designed size of the multimode waveguide is 50μm X 50μm. The process is the same as standard photo-lithography. The Piranha bath consists of 2 parts of sulfuric acid (H_2SO_4) and 1 part of hydrogen peroxide (H_2O_2). A Si-wafer was cleaned in the Piranha bath. After the cleaning, the wafer was bake at 150°C to remove adsorbed water just before spin coating. This baking step improves adhesion and removes bubbles in pre-baking step. After baking, photoresist (SU8- 2000, MicroChem™) was poured on the wafer and then spin coated at 400 RPM for 5 seconds and then ramped to 1500 RPM for 40 seconds. The wafer stayed on a leveled surface for 5 minutes to improve uniformity. And then, the wafer was moved to leveled hot-plate for a pre-bake. The pre-bake was carried out at 65°C for 5 minutes and 90°C for 40 minutes.

The patterning is the trickiest part during the whole fabrication process. The SU-8 is chemically enhanced photopolymer; hence, post exposure bake is necessary. The photoresist is negative type i.e. unexposed area will be removed during developing process. Exposure, to pattern the photoresist, was carried out using Carl-Suss aligner. The Figure 5.10 shows cross sections of SU-8 photoresist pattern for various exposure conditions. The Cross-linking of the SU-8 proceeds in two steps. The first step is the formation of acid during exposure. The second step is acid initiated thermally driven epoxy cross-linking. The photoresist tends to have negative sloped sidewall, which is not good for mold application. The side wall should have positive slope or at least be vertical for mold application. Exaggerated negative wall is often called as T-topping. The T-

topping results from the lateral diffusion of the acid near the surface. UV lights shorter than 350nm is absorbed strongly at the top surface of the photoresist; hence, acid is generated by UV, which diffuses laterally on the top surface.

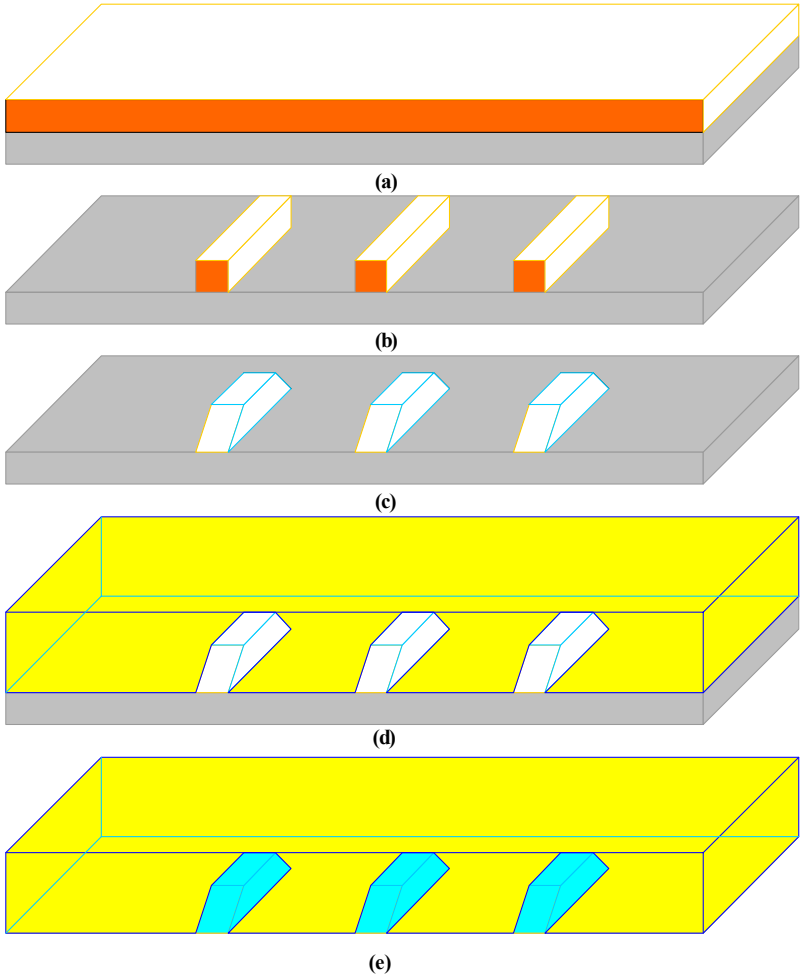


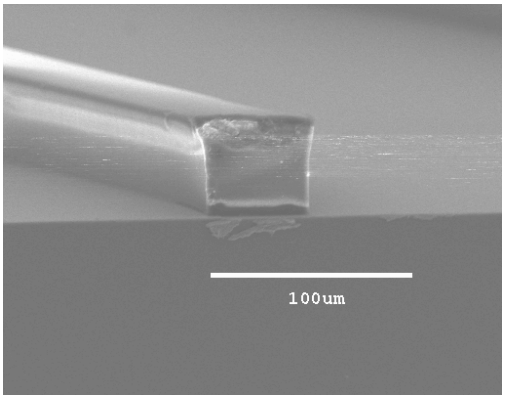
Figure 5.9 Master waveguide and mold fabrication process. (a) Spin coat photoresist (Su-8) at 400RPM for 5sec. + 1500RPM for 40sec. (b) Patterning (exposure, post exposure bake and develop) (c) 45º cut by microtome (d) Pouring PDMS over the master (e) Curing PDMS and remove the master.

After the UV exposure, post exposure bake (PEB) process was carried out under the same conditions as described in the pre-bake step. If the PEB time is short, the pattern does not have enough adhesion; hence, the pattern is peeled off from the substrate during developing process.

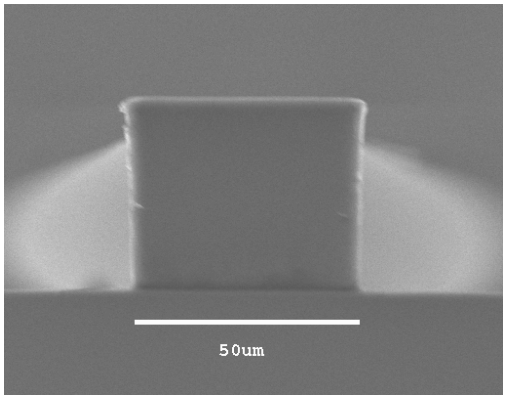
The T-toping can be removed by filtering out short wavelength below 350nm [54]. The T-topping of the pattern is shown in Figure 5.10(a). Nearly vertical side wall (Figure 5.10b) was made using short wavelength cut filter (UV-34, Hoya). However, there is still a beaked shaped feature between side walls and top surface. A beaked shape results from the diffraction at the interface between the mask and the photoresist, and it can be eliminated by filling index matching oil (glycerol) into the gap [55]. The ethylene glycol was used to fill the air gap in this experiment instead of using glycerol.

The beak was completely removed (Figure 5.10c). The portion of the 1X12 linear array of waveguide pattern is shown in Figure 5.10d. The final step in the master fabrication process is cutting waveguide ends at 45°. The cutting was completed by using the microtome setup as described in the section 5.5.2.

The mold material is PDMS (Sylgard 184, Dow Corning). Prepolymer and curing agent were mixed at 1:10 ratio. Air bubbles trapped in PDMS were removed in a vacuum chamber. After removing air bubbles, the PDMS was poured on the master and cured at 90°C in vacuum chamber for 10 hours. Surface relief structures were transferred from master to the mold. The PDMS mold is shown in Figure 5.11.



(a)



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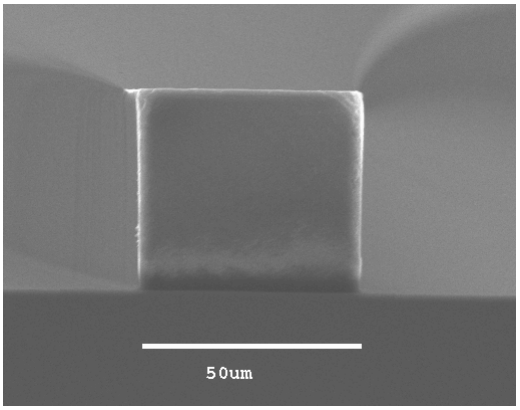

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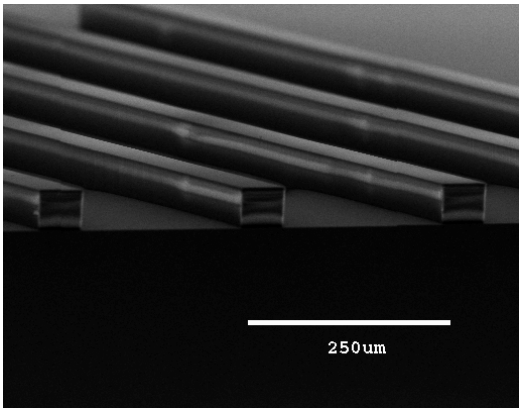


(d)

Figure 5.10 Cross sectional views of SU-8 photoresist pattern for various exposure conditions (Exposure: 300mJ/cm^2) (a) Without UV-34 filter (b) With UV-34 filter (c) With UV-34 filter and Index matching oil (d) Linear waveguide array pattern of photoresist.

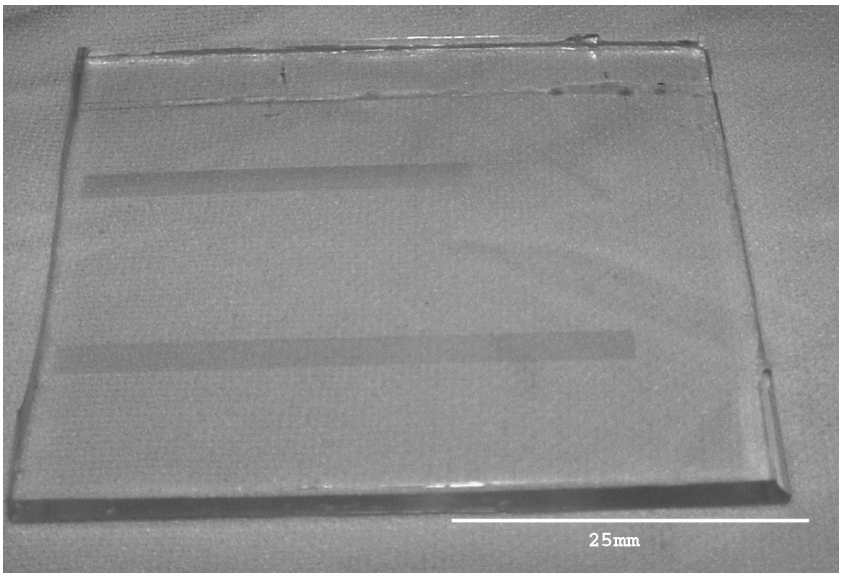


Figure 5.11 PDMS mold.

5.3.3 Deformation compensation

Materials used in the waveguide fabrication process have different coefficients of thermal expansion (CTE). For example, the COC (cycloolefin copolymer, Topas 5013™ from Ticona) as a cladding material has the CTE of 60 ppm/°K. The CTEs are 2.3, 52, 30 ppm/°K for silicon, SU-8, and PDMS, respectively. The dimension of the cast is not the same as the master waveguide due to the shrinkage of PDMS cast after cooling down to ambient temperature. There are two approaches to compensate dimensional change. One is making compensated mold after trial and error and/or accurate

calculation. The other is compensation technique during molding process by adjusting mold pressure. This approach is only valid for soft cast. The first approach is suitable for fixed materials and well defined process conditions. If a material or process is changed, the cast must be changed. The compensation technique during mold process was chosen because the cast material is soft, and it is easy to adjust process in research stage.

Table 5.1 Physical properties of materials used in molding process.

Material	Coefficient of Thermal Expansion, α [ppm/°K]	Young's Modulus ,E [MPa]	Poisson's Ratio, υ
Silicon	2.33	202,000	0.27
SU-8	52	4020	0.22
PDMS	30	0.75	0.5
Topas5013^{TM}	60	-	-

Dimensional change occurs at the beginning of process. The first step to make the flexible waveguide film starts with the fabrication of the soft cast. To make a cast, curing procedure at certain temperature is followed after pouring liquid silicone elastomer on to the master structure. During this process, dimensional change occurs in both the master and the mold. The dimensional change of the master at elevated temperature is given by Equation 5.10

$$L = Lo(1 + \alpha_{Si} \bullet \Delta T) \qquad \text{Equation 5.10}$$

L_O is original length at reference temperature, $\boldsymbol{\Delta T}$ is temperature difference, $\boldsymbol{\alpha_{Si}}$ is the linear expansion coefficient of silicon. The length of the mold at curing temperature is equal to that of the master structure. After cooling down the mold to ambient temperature, the mold is shrunken. The length after cooling ($\boldsymbol{L_{cast}}$) can be calculated from the linear expansion equation (Equation 5.11).

$$\begin{aligned} L_{cast} &= Lo(1+\alpha_{Si}\bullet\Delta T)(1-\alpha_{PDMS}\bullet\Delta T) \\ &= L_O(1-\alpha_{PDMS}\bullet\Delta T+\alpha_{Si}\bullet\Delta T-\alpha_{Si}\bullet\alpha_{PDMS}\bullet\Delta T^2) \\ &\cong L_O(1-(\alpha_{PDMS}-\alpha_{Si})\Delta T) \end{aligned} \qquad \text{Equation 5.11}$$

The dimensional change of the final waveguide film occurs during the molding process. The mold is made of elastic rubber; hence, the applied pressure can deform the mold. In addition, molding process accompanies pressure and heat. The waveguide substrate and the mold expand due to the thermal expansion. The length of the waveguide substrate (Topas film) ($\boldsymbol{L_{Topas}}$) and the length of the mold, due to the thermal expansion are,

$$L_{Topas} = Lo(1+\alpha_{Topas}\bullet\Delta T_M) \qquad \text{Equation 5.12}$$

$$L_{cast,M,therm} = L_O(1-(\alpha_{PDMS}-\alpha_{si})\Delta T)(1+\alpha_{PDMS}\bullet\Delta T_M) \qquad \text{Equation 5.13}$$

If mold curing temperature ($\boldsymbol{\Delta T}$) is the same to molding temperature ($\boldsymbol{\Delta T_M}$) then the equation 5.13 is simply,

$$L_{cast,M,therm} = L_O(1+\alpha_{Si}\bullet\Delta T)$$ Equation 5.14

The dimension of the cast is also affected by the applied pressure (***F***) during mold process.

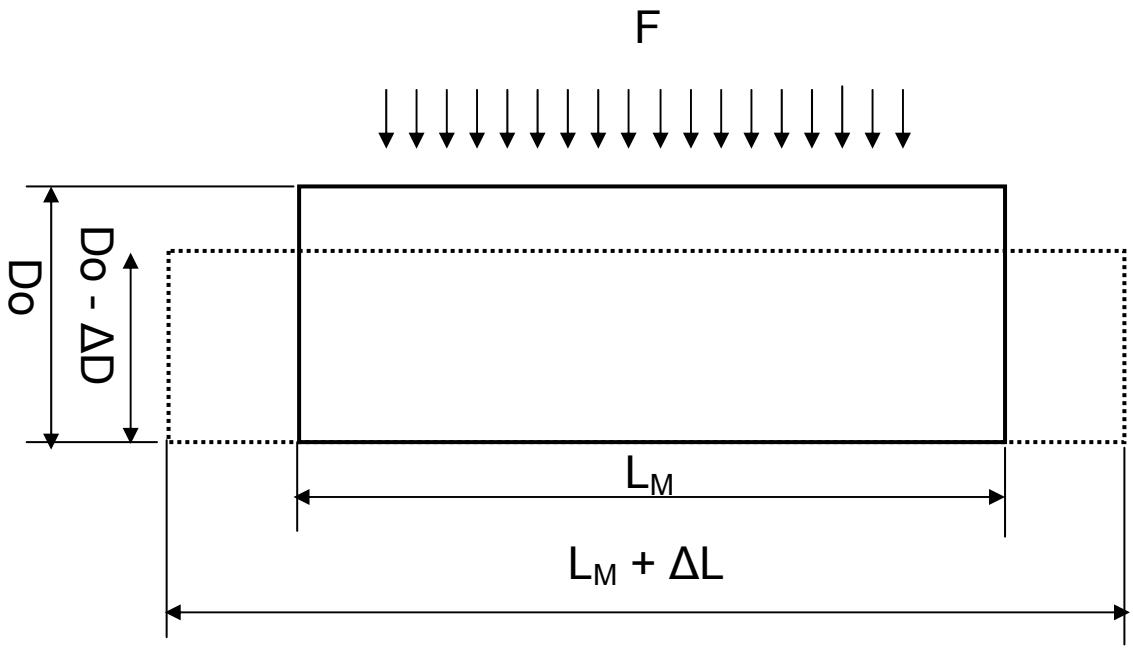


Figure 5.12 Mold deformation during compression molding.

When the cast is subjected to a load, it deforms not only in the direction of the load but also in the direction of perpendicular to the load. In molding process, the load is compressive. The length in the direction of the pressure will decrease, and transverse length will increase.

There are two strains in the molding process, one is axial (ε_a), and the other is transverse (ε_t) [56].

$$\varepsilon_a = \frac{\Delta D}{D_O} \quad \text{and} \quad \varepsilon_t = \frac{\Delta L}{L_M} \qquad \text{Equation 5.15}$$

The Poisson's ratio (υ) is the ratio of transverse strain to the axial strain. If pressure is applied on the cast, the axial strain is compressive so that the sign of strain is negative. On the other hand the transverse strain is tensile. The Poisson's ratio is always a positive value.

$$\upsilon = -\frac{\varepsilon_t}{\varepsilon_a} = -\frac{\Delta L / L_M}{\Delta D / D_O} \qquad \text{Equation 5.16}$$

The length change of the cast due to the pressure can be calculated by introducing Young's modulus ($\boldsymbol{E}$).

$$E = \sigma \frac{D_O}{\Delta D} \qquad \text{Equation 5.17}$$

here, σ is applied load [N/m^2].

The final length change of the cast accounting thermal expansion and deformation (Equation 5.18) can be calculated by plugging Young's modulus term into the Poisson's equation.

$$\Delta L = -L_{cast,M,therm} \frac{\upsilon \sigma}{E} \qquad \text{Equation 5.18}$$

The displacement ($\boldsymbol{\Delta L}$) of the mold should be equal to the displacement of the waveguide film.

$$-L_M \frac{\upsilon\sigma}{E} = L_O \alpha_{Topas} \Delta T \qquad \text{Equation 5.19}$$

Therefore, optimized pressure (σ) to compensate deformation is given by Equation 5.20

$$\sigma = -\frac{E\alpha_{Topas}\Delta T}{(1+\alpha_{Si}\Delta T)\upsilon} \qquad \text{Equation 5.20}$$

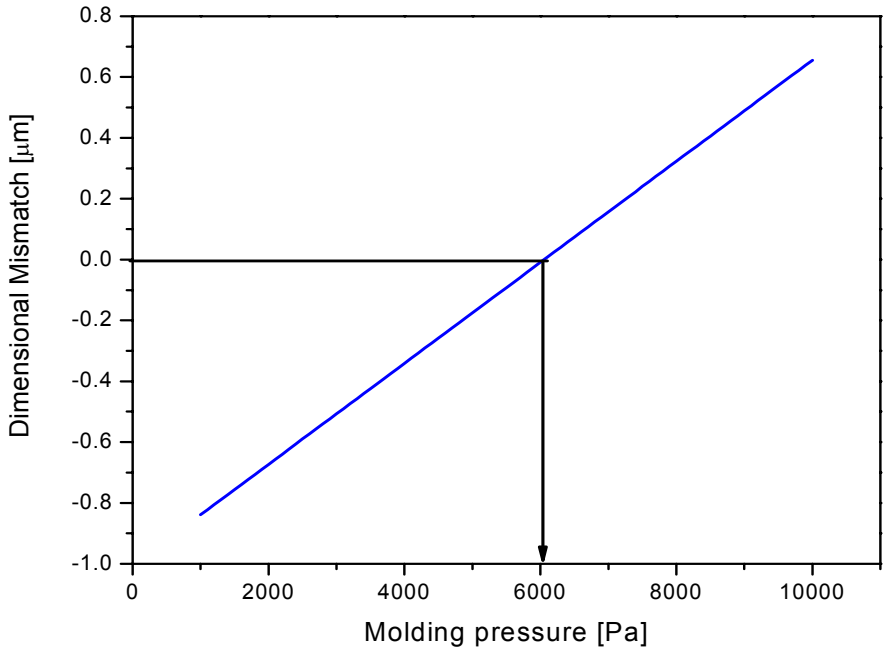


Figure 5.13 Dimensional change as a function of molding pressure. [Dimensional change is based on 250μm structure, i.e. amount of deformation will be accumulated if the size of a feature or mold increased].

Data in the Table 5.1 were used during the calculation. The optimized molding pressure was 6000Pa. If the molding pressure is less than 6000 Pa, the distance between two waveguides will be shorter than the designed distance. For pressure greater than

6000Pa, the distance will be larger. Total displacement will be accumulated by increasing mold or feature dimension.

5.3.4 Optical interconnection layer fabrication

The fully embedded board level optical interconnection requires a thin flexible optical layer. Current electroplating technology can plate easily a through-hole or a via having an aspect ratio of 1 in production line and can plate a hole having an aspect ratio of 3 in laboratory. The size of a typical electrical pad on the device is about 100μm. These are main reasons for the thickness limit of substrate film. The thin and flexible optical waveguide layer was fabricated by compression molding technique using soft mold. A 127μm thick optically transparent film (Topas™ 5013) was used as a substrate of the waveguide circuit.

The fabrication step is straightforward. First, core material (SU-8) was poured on the heated PDMS, which is kept at 50°C (Figure 5.13a). The heated PDMS mold suppresses bubble generation during molding process. And then, excess SU-8 was scraped out using squeegee (Figure 5.13b). The squeegee was made of PDMS, also. The Topas film was applied on the top of the PDMS mold filled with SU-8. In the next step, the mold and the Topas film were inserted into the press machine and then was applied with the pressure of 6000Pa for 30 minutes while plunge plate was held at 90°C (Figure 5.13c). The cooling down procedure was followed. In this procedure, the mold pressure decreased gradually due to the thermal contraction. The core material (SU-8)

was transferred to the substrate film (Figure5.13d). In the next step, the substrate film without the top cladding was exposed to UV to cross-link the SU-8. Once the film was exposed, it becomes chemically and thermally stable. Aluminum was deposited on the mirror facets in a vacuum chamber to make the mirror. Finally, top cladding material (Topas) was coated on the film. Fabricated optical interconnection layer is shown in the Figure 5.14. It has micro-mirror couplers and 12 channel waveguides of 50mm in length.

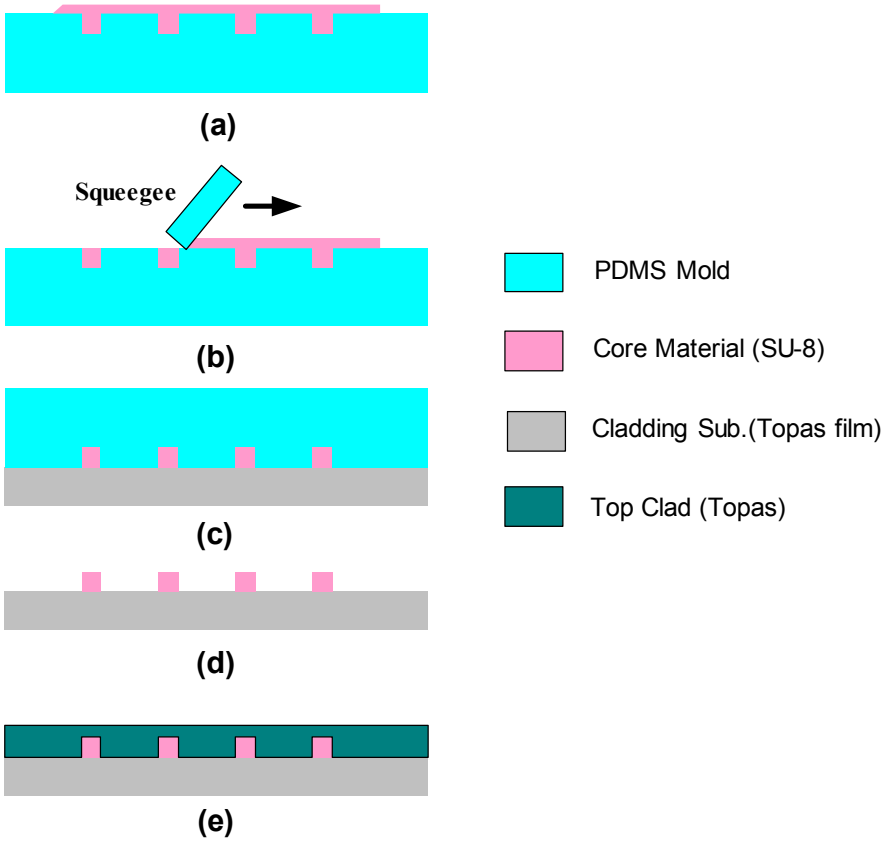


Figure 5.14 Optical interconnection layer fabrication process flow (a) Apply core material (SU-8) (b) Remove excess material (c) Apply heat and pressure on the mold and cladding substrate (d) Cool down and release plunger (e) Apply top cladding materials (either spin coat or lamination).

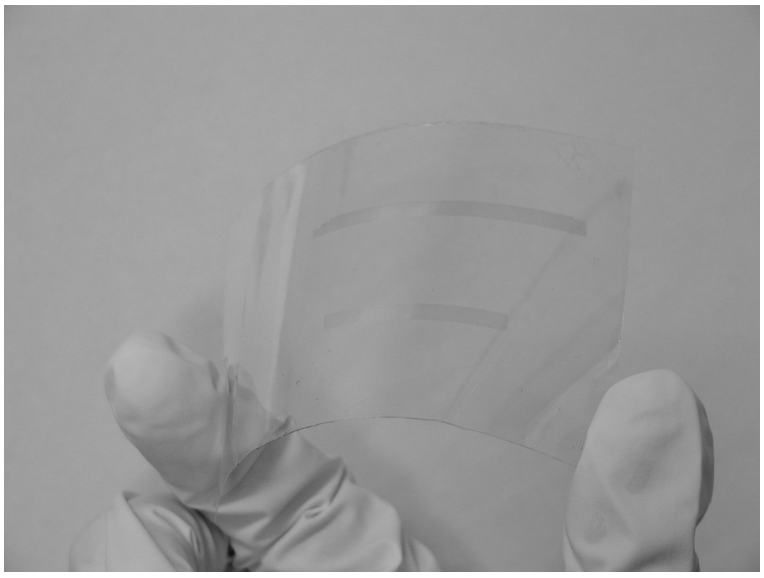


Figure 5.15 Fabricated flexible optical interconnection layer.

5.4 PROPAGATION LOSS MEASUREMENT

The absorption loss of the Topas film was determined by the transmittance of material using spectrometer. Measured transmittance values according to wavelengths were compared to theoretical values.

The transmittance of medium is the ratio of the sum of all transmitted lights to incident power. α is the absorption coefficient of material, L is the thickness of the medium, and R is reflectance between interfaces.

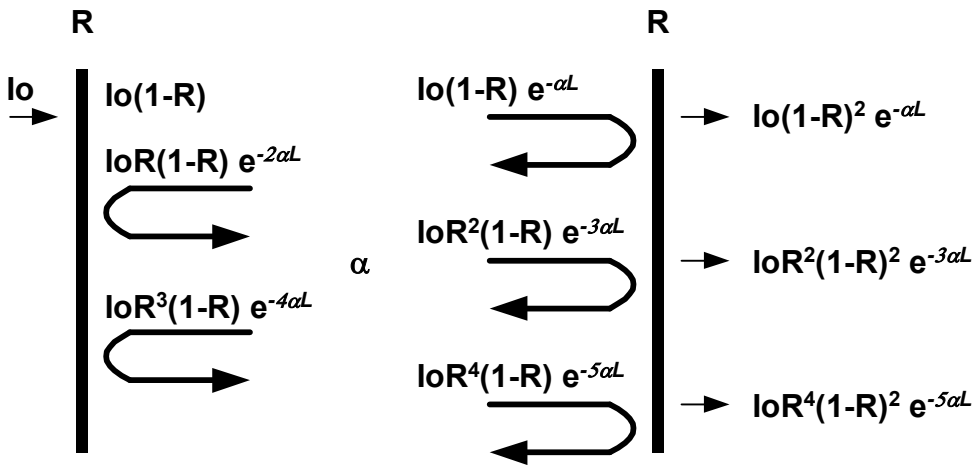


Figure 5.16 Reflectance and transmittance of thick medium.

For normal incident case and air to medium interface, the reflectance at the interface is given by Equation 5.21 [14].

$$R = \left(\frac{n-1}{n+1} \right)^2 \qquad \text{Equation 5.21}$$

Here, n is the refractive index of medium.

The refractive index of Topas^{TM} 5013 is calculated from Cauchy equation (Equation 5.22).

$$n = A + \frac{B}{\lambda^2} + \frac{C}{\lambda^4} \qquad \text{Equation 5.22}$$

For Topas 5013 medium, the coefficients are A=1.519808, B=440569.2, and C=7.755498 X 10^{11}[from Ticona]. The transmitted intensity is the sum of all transmitted lights by multiple reflections at two interfaces.

$$T = (1-R)^2 e^{-\alpha L}\left[1 + R^2 e^{-2\alpha L} + R^4 e^{-4\alpha L} + R^6 e^{-6\alpha L} + \cdots\right]$$
$$= (1-R)^2 e^{-\alpha L}\left[\frac{1}{1-R^2 e^{-2\alpha L}}\right] = \frac{(1-R)^2 e^{-\alpha L}}{1-R^2 e^{-2\alpha L}} \qquad \text{Equation 5.23}$$

$$e^{-\alpha L} = \frac{-I_0(1-R)^2 \pm \sqrt{(1-R)^4 + 4T^2R^2}}{2TR^2} \qquad \text{Equation 5.24}$$

Absorption coefficient α of the medium is

$$\alpha = -\frac{\ln\left(\frac{-I_0(1-R)^2 \pm \sqrt{(1-R)^4 + 4T^2R^2}}{2TR^2}\right)}{L} \qquad \text{Equation 5.25}$$

Absorption loss α_a of the medium per unit length is defined by Equation 5.26.

$$\alpha_a = \frac{10}{l} Log_{10} \frac{P_{in}}{P_{out}} \qquad \text{Equation 5.26}$$

Here, P_{in}/P_{out} is the ratio of the input power to the output power after propagating medium and equals to $e^{\alpha L}$, then

$$\alpha_a = \frac{10}{L} Log_{10} e^{\alpha L} \qquad \text{Equation 5.27}$$

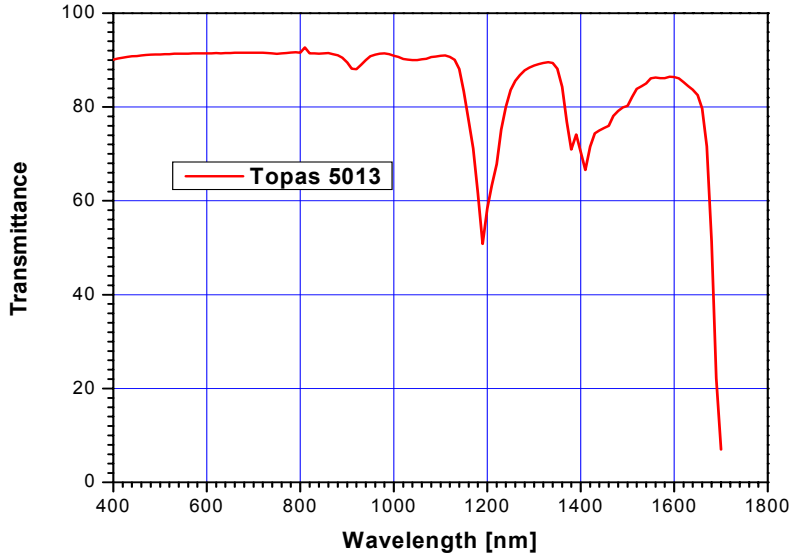


Figure 5.17 Transmittance of 3mm thick Topas™ 5013 [from Ticona].

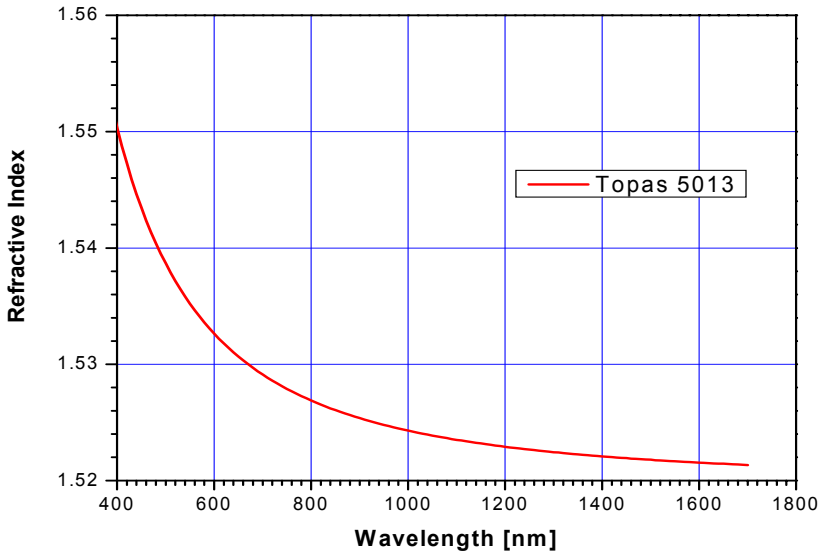


Figure 5.18 Refractive index of Topas™5013 as a function of wavelength. [from Ticona].

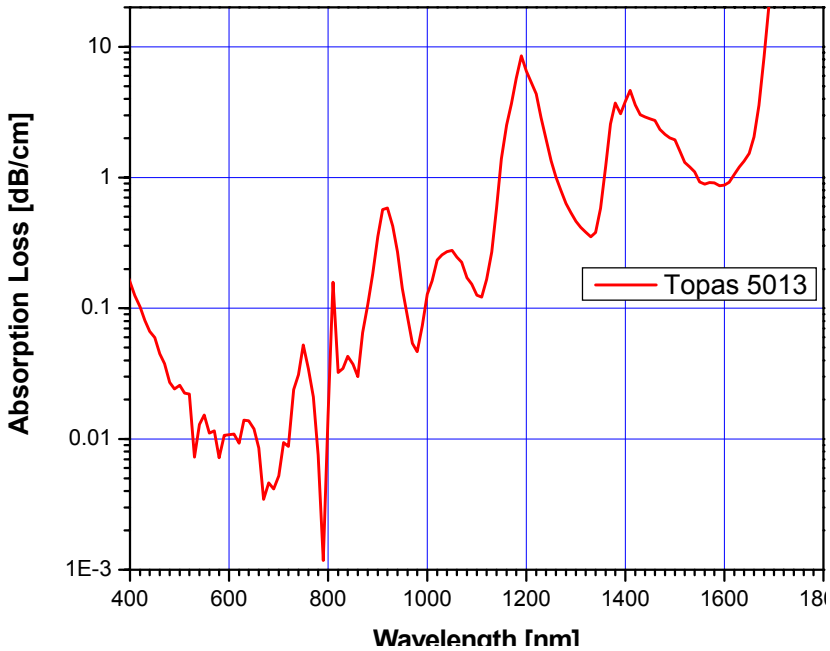


Figure 5.19 Extracted absorption loss of the Topas™ 5013 as a function of wavelength.

The refractive index of UV exposed SU-8 as a function of wavelength was measured using transmittance curve. The oscillating curve beyond 650nm wavelength did not represent real refractive index. There was some interference due to the thin sample. Refractive index is shown in Figure 5.19. The refractive index was 1.584 at 850nm wavelength.

The absorption loss of the Topas is 0.01 dB/cm and 0.03dB/cm at 630nm and 850nm, respectively. The minimum absorption loss at 790nm does not represent an exact value because there is a change of grating during wavelength scan.

Philip D. Curtis reported 6dB/cm propagation loss at 850nm for a multi-mode waveguide [57]. W. H. Wong etc. reported low propagation loss of 0.22 and 0.48dB/cm at 1330 and 1550nm, respectively, using electron beam direct writing [58].

Waveguide propagation loss was measured by cut back method. The core dimension was 50X50μm. The bottom cladding of the waveguide is 3μm thick SiO_2. Fiber pig-tailed 850nm laser was used to couple the laser to waveguide. The diameter of fiber is 10μm, which is similar to VCSEL aperture. Coupled out powers according to the length is shown in Figure 5.20. Measured propagation loss was 0.6dB/cm at 850nm wavelength.

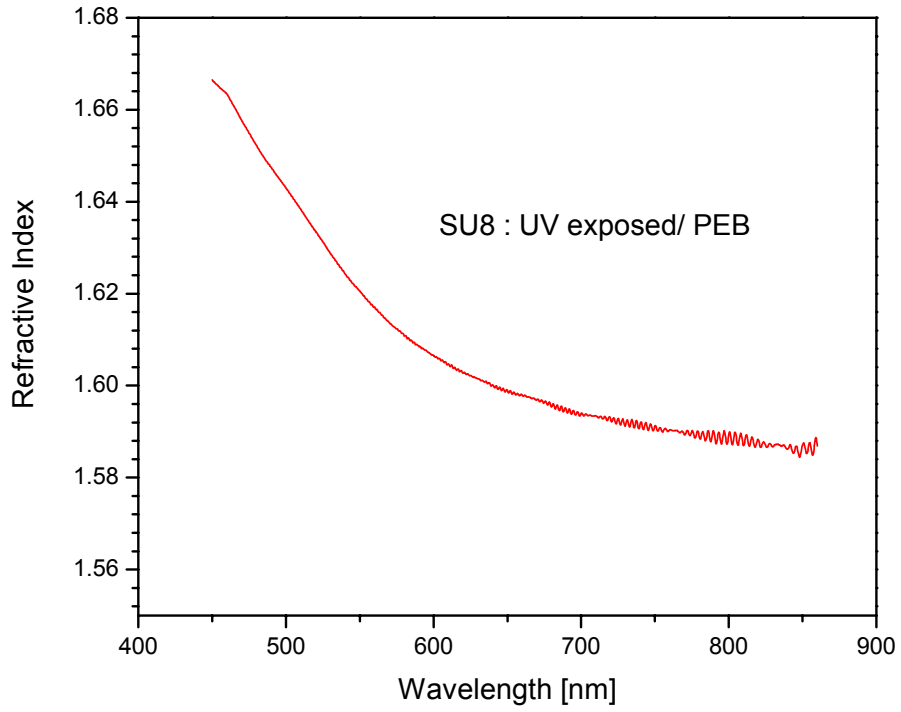


Figure 5.20 Measured refractive index as a function of wavelength.

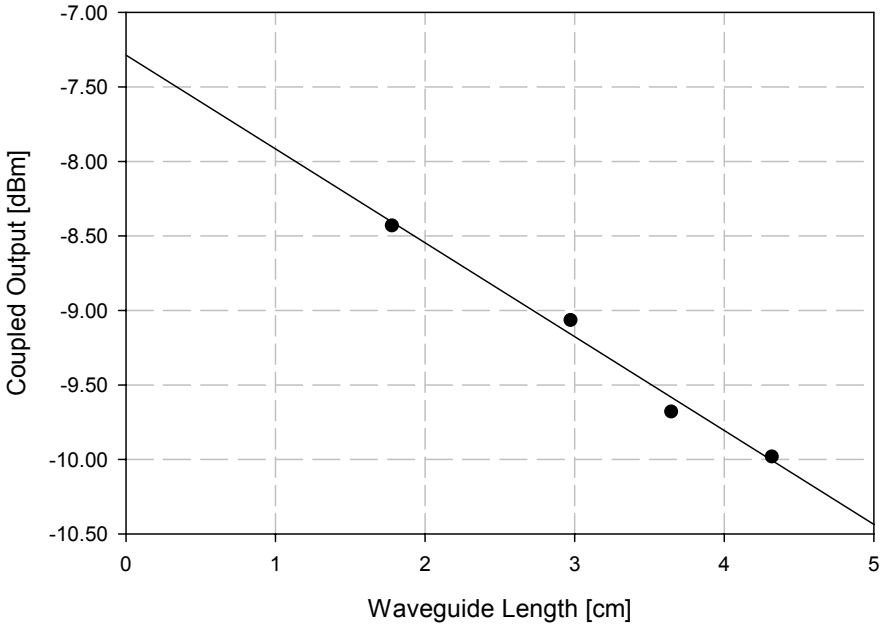


Figure 5.21 Coupled out power as a function of waveguide length. (Cut-back method, slope of the line is propagation loss, propagation loss is 0.6dB/cm at 850nm wavelength).

The crosstalk of parallel channel waveguides is an important factor in communication. The channel spacing of the waveguide array is 250μm, and the width of waveguide is 50μm. The difference of refractive indices between the core and the cladding is about 0.058. To measure crosstalk, the channel waveguide of 5cm long was put on an auto-aligner. And then, the fiber coupled laser light with the wavelength of 630nm was lunched into one channel among the waveguides. The output of the signal was measured at the adjacent channel. Figure 5.21 shows a test setup. Laser light was lunched from the end of fiber ferrule to waveguide. The picture, left side of the Figure 5.21, is enlarged view of coupling area. The lunched input power at waveguide and

output power at the adjacent waveguide end were –21 dBm and -53 dBm, respectively. Measured crosstalk between adjacent channels was 32 dB.

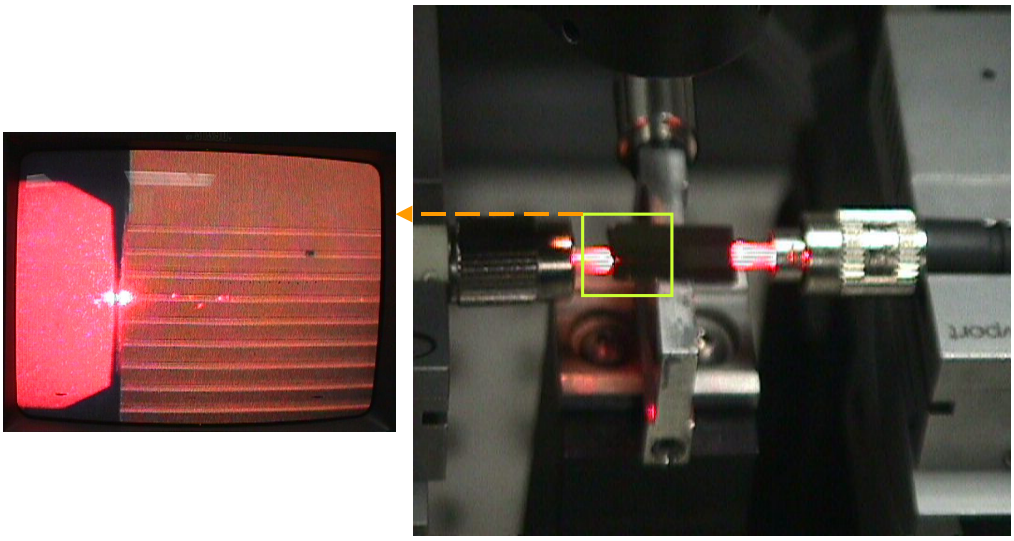


Figure 5.22 Test setup for the crosstalk measurement.

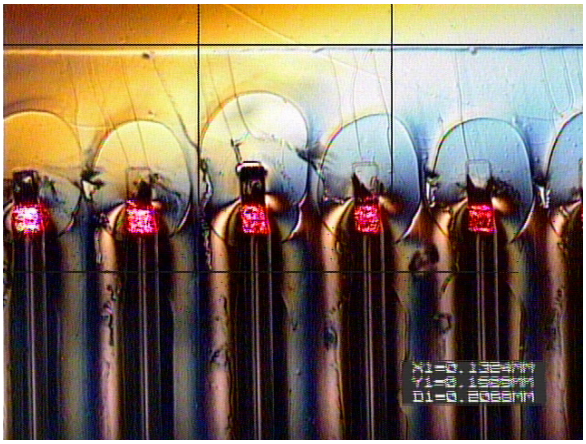


Figure 5.23 Coupled out beams from 45° waveguide mirrors. (Flexible waveguide, 633nm He-Ne laser was lunched from the other side of the wave guide).

Chapter 6: System Integration

6.1 INTRODUCTION

The hybrid integration of optical layer with electrical layers is the most important part in the realization of optical interconnects. PCB technologies is already well matured; therefore, great deviation from current fabrication technique may result in the failure of commercialization. Hence, we have to minimize the change of fabrication process. The optical interconnects in board level can not replace all copper lines. There are slow interconnecting lines such as data, control, power, and ground lines. Especially, slow data lines do not need to be replaced by optical means because the fabrication cost and process of copper lines are very cheap and reliable.

High integration cost must be avoided. This requirement can be satisfied by separating fabrication processes. Obviously, the fabrication of waveguide layer and the integration of optoelectronic devices must be cheap. Optical interconnection layer and electrical layers are fabricated independently. At the final integration step, two different types of layers are laminated together using matured lamination process.

Interface between optoelectronic device and control device is important because of the requirement for high density (HD) packing. Laser drilled micro-via technology is utilized to satisfy HD packing. The thermal management of VCSEL is important also because of reliability concerns. Embedded VCSEL can not be replaced to repair in a fully embedded integration; therefore, we have to be aware of good VCSEL before the integration and provide optimal operating condition.

6.2 INTEGRATION THIN-FILM VCSEL AND DETECTOR ARRAYS ON OIL

The integration of optoelectronic devices with the flexible waveguide film is the most important process among the whole integration steps including the final laminating process with PCB. The flexible waveguide film has the thickness of 127μm. The VCSEL and photo-detector arrays have the diameter of about 95μm. In general, copper electroplating allows plating of a via with aspect ratio of 1; however, it is possible to plate a via with an aspect of 3 in a laboratory environment. The maximum diameter of the laser drilled via is limited by the pad size of devices, the aspect ratio, and the registration error during lamination process. Figure 6.1 illustrates device integration process.

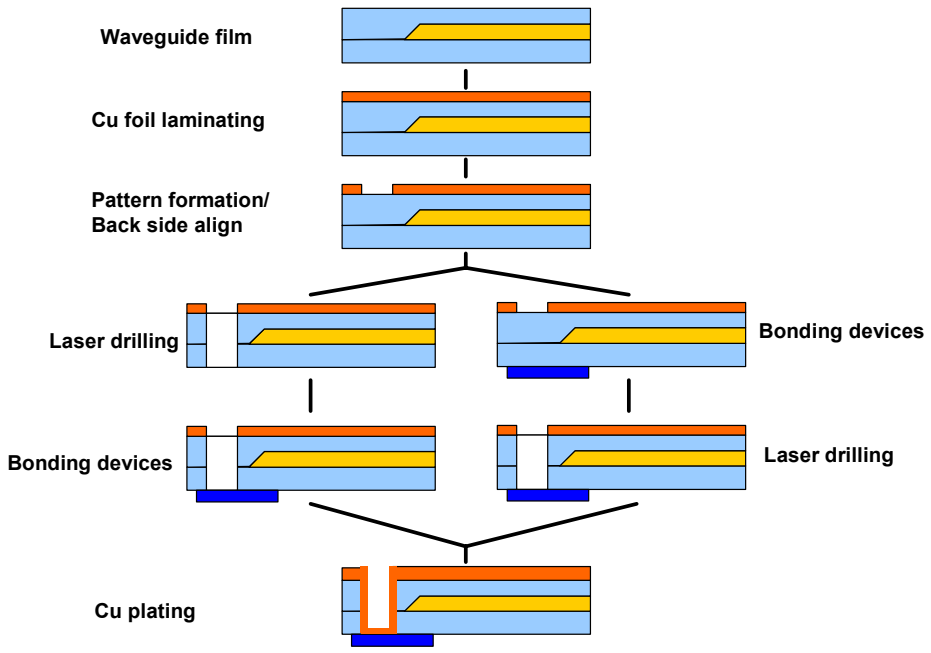


Figure 6.1 Devices integration process flow chart.

First, One mil (25.4μm) thick copper foil is laminated on the top of the flexible wave guide layer by applying heat and pressure. And then, this copper foil is patterned to form the top electrical pads for VCSEL and photo-detector. The main reason for the formation of the laminated copper foil is the limitation of electroplating. The thickness of additional electrical layers easily exceeds 1mm, and the diameter of device pad is 95μm. This translates to an aspect ratio of 100; therefore, this hole can not be electroplated. The aspect ration of via can be reduced by introducing the copper foil just above the waveguide layer; hence, we can electroplate micro via. Furthermore, the patterns on the copper foils can be bigger. This means that larger registration error can be allowed during laminating process with electrical layers.

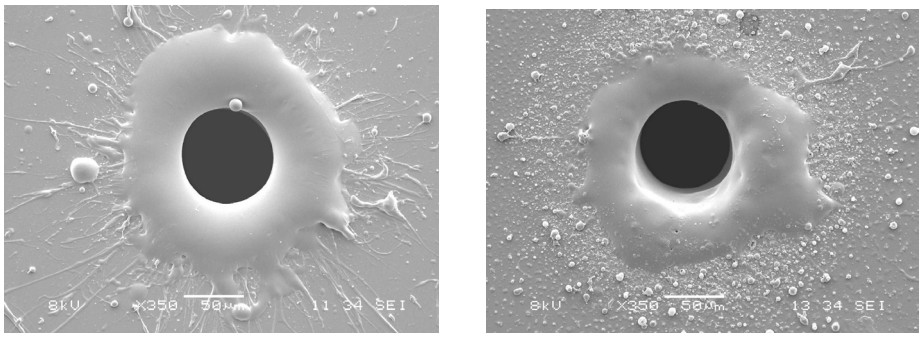
Next step is either laser drilling or device bonding on the waveguide layer. The SEM pictures of laser drilled vias are shown in Figure 6.2-6.4. Laser drilling and taking SEM picture were performed at Sanmina-SCI.

Micro-via on the Topas film is shown in Figure 6.2. Frequency tripled Nd:YAG laser, which has wavelength of 355nm, was used. The Topas film is relatively transparent at 355nm wavelength. Melting and spattering around the hole were observed at both the incident and exit side of film. If copper foil was laminated on the top of Topas film, spatter and melt flow will be reduced. The reduced energy of laser pulse and short pulse width also help clean drilling. Another choice is using the UV- excimer laser which has shorter wavelength.

Micro-vias drilled with CO_2 laser are shown in Figure 6.3. During the laser drilling, a device fell off from the Topas film. Drilling conditions were fixed pulse count

and various pulse widths. When the Topas film was exposed to 5 series pulses of CO_2 laser, which has 10μs pulse width, only bump was created on the incident side. There was no clear hole when the pulse width of the laser was increased to 30μs.

Another example of CO_2 laser drilled vias on the Topas film is shown in Figure 6.4a. The series of laser drilled vias in the upper portion of Figure 6.4a were made by fixed laser pulse width of 10μs and various pulse counts from 1 to 12. Via spacing was 250μm. By increasing the pulse count, melted region was expanded. When the pulse count was fixed at one with pulse width increasing from 1μs to 11μs, melted region, shown in the bottom portion of Figure 6.4a, was increased. The CO_2 laser can not be used to drill via on the Topas film, which is the cladding material of flexible waveguide film.



(a) (b)

Figure 6.2 SEM pictures of the laser drilled micro-via. Frequency tripled Nd:YAG (wavelength:355 nm), 127μm thick Topas film. (a) incident side, (b) exit side. [from Sanmina-SCI]

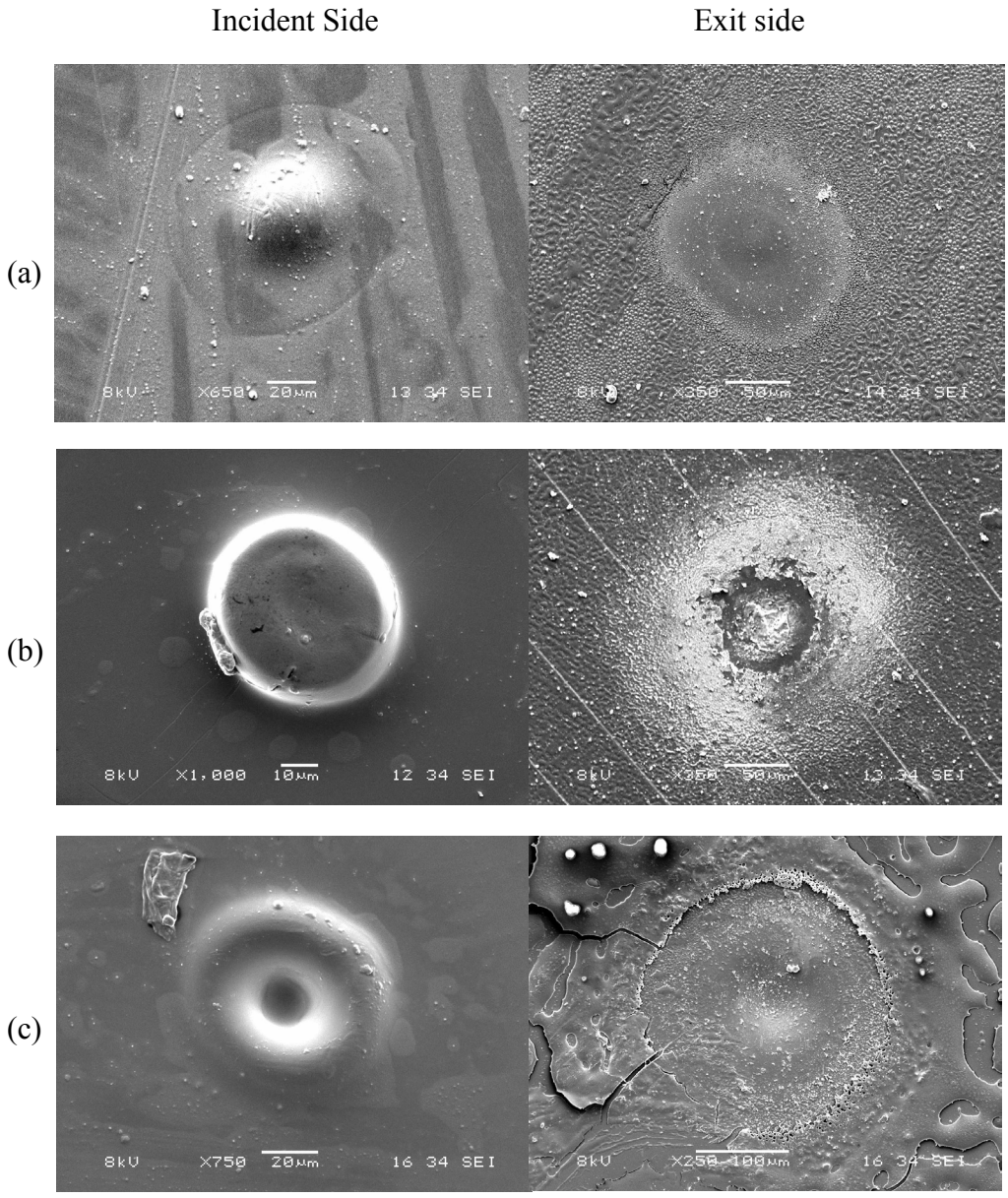
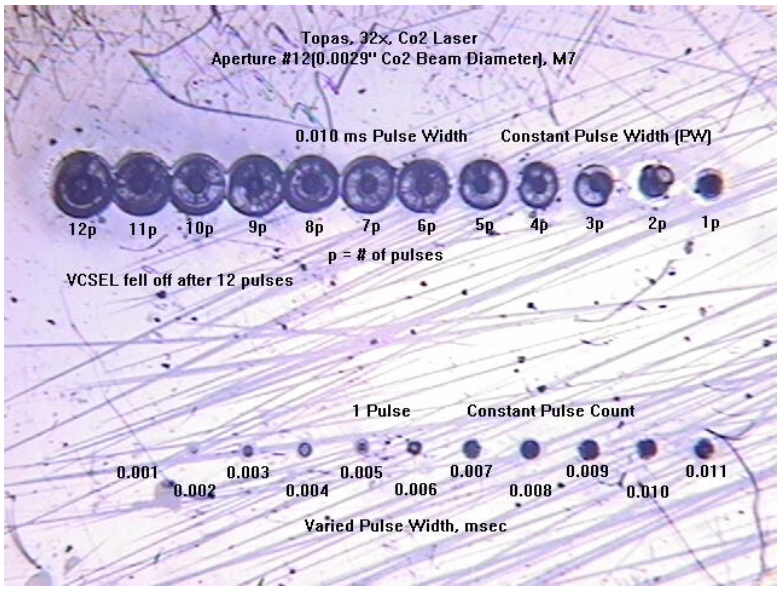
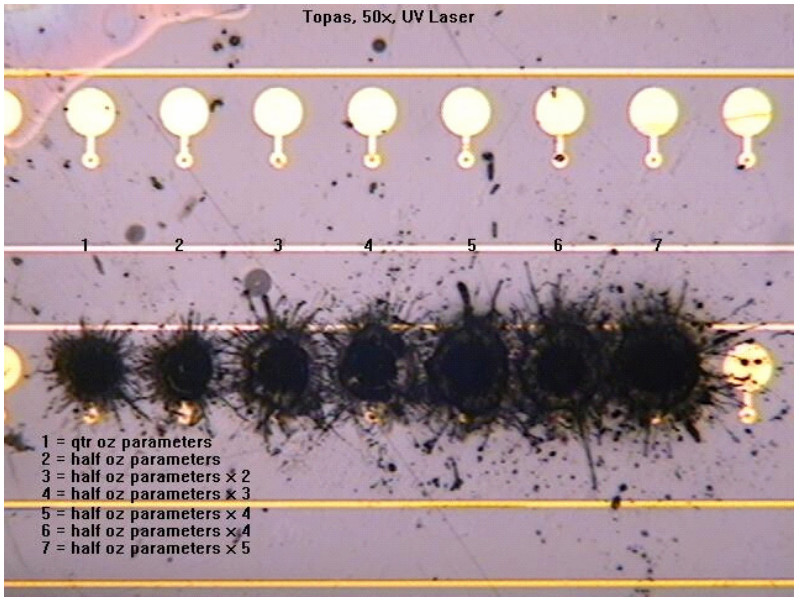


Figure 6.3 SEM pictures of the CO_2 laser drilled micro-vias. (wavelength:10.6µm), 127µm thick Topas film. (a) 5 pulses with 10µs pulse width, (b) 5 pulses with 20µs pulse width and (c) 5 pulses with 30µs pulse width. [from Sanmina-SCI]



(a)



(b)

Figure 6.4 Pictures of laser drilled vias under various drilling conditions. (a) CO_2 Laser and (b) UV-Nd:YAG laser (Frequency tripled). [from Sanmina-SCI]

Picture of the UV-Nd:YAG laser drilled via on the waveguide film which is integrated with device is shown in the Figure 6.4b. The UV-Nd:YAG laser makes extensive damage on the film and it seems to damage the metal pad of the devices as well. Therefore, the integration of devices on the waveguide film should be done after the formation of micro-via drilling.

The thin-film devices are usually bonded on an exotic substrate by Van der Waals force. Palladium is the most common material for the bonding [59]. Although the bonding temperature is low, long bonding time is required. This limits the real world applications from the view point of throughput.

The bonding of devices was performed using an aligner. Typical aligner has two holders; one for mask and the other for substrate. The flexible waveguide film was temporally bonded to a clear glass plate using water and placed on a mask holder. The device to be integrated was put on the substrate holder. Small amount of UV curable adhesive was applied on the top of the device. When device and waveguide micro-mirror coupler were aligned, they were exposed with UV to cure the adhesive. Flexible optical interconnection layer with device integration is shown in Figure 6.5.

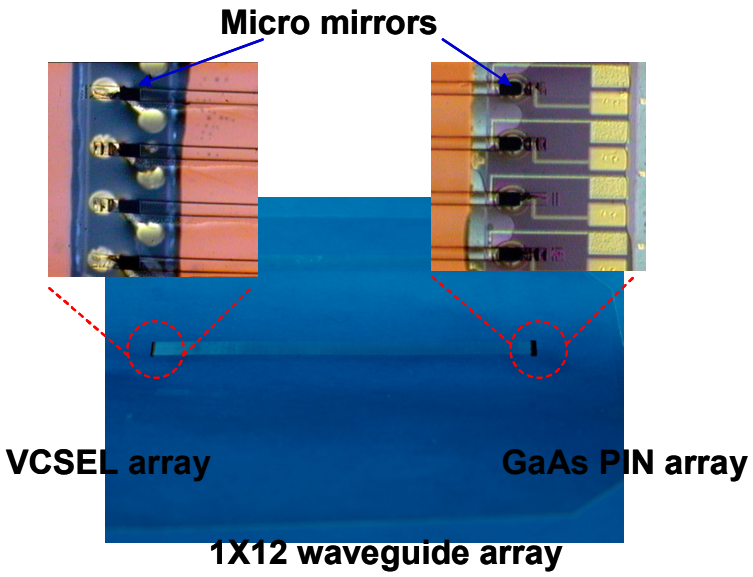


Figure 6.5 Integrated VCSEL and detector arrays on a flexible optical interconnection layer.

The bonding of device to waveguide film can be accomplished by melt bonding without using UV curable adhesive. When alignment is completed, device is heated just above the melting temperature of waveguide film for a short period. And, device is bonded to the waveguide film without deforming the micro-vias.

So far, the integration of devices on the flexible waveguide film is accomplished. The final step is electroplating. Integrated waveguide film was submerged in copper electroplating solution to plate the side walls of micro-vias and device pad. Now, the optical interconnection layer is ready to be laminated with the electrical layers.

6.3 HYBRID INTEGRATION OF OIL AND PRINTED CIRCUIT BOARD.

At the beginning of designing the hybrid system, electrical and optical layouts are designed simultaneously by incorporating each other. After finishing the layout, the electrical and the optical layer are fabricated separately. The electrical fabrication process can be build-up process, laminating process, or mixed process. Fabricated optical interconnection layer will be inserted into electrical layers. Industry standard PCB lamination process uses high temperature and pressure to laminate layers. Typical laminating condition is shown in Figure 6.5. The peak temperature and press pressure are reached at 170°C and 150N/cm^2, respectively. The glass transition temperature of the Topas™ 5013 is only 135°C. However, the melting temperature of the waveguide core material, UV cross-linked SU-8, exceeds 200°C. Therefore, the optical interconnection layer can not survive the standard laminating process. This is one of the reasons for building the electrical layers and the optical layer separately.

Hybrid laminating process is shown in Figure 6.6. The optical interconnection layer was already fabricated [Figure 6.6a]. The electrical layers are partially laminated using the standard laminating process i.e. upper electrical layers above the OIL and lower electrical layers below the OIL [Figure 6.6b]. For better heat removal, the OIL is inserted near the bottom electrical layer. The shorter distance to heat sink provides better heat removing. In the next step, pre-patterned bonding films, which have lower melting temperature than that of Topas, are applied on the both side of the OIL [Figure 6.6c].

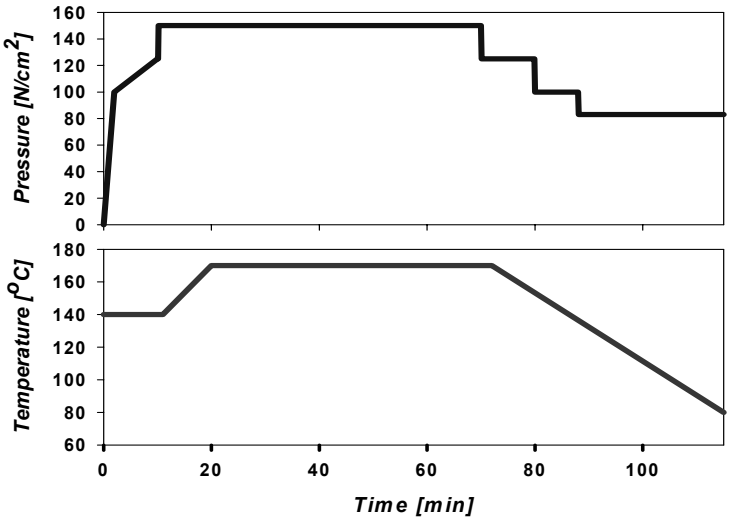


Figure 6.6 Industry standard FR-4 PCB laminating pressure and temperature. [source:LLFa GmbH, Hanover/Germany]

Following step is laminating OIL and electrical layers together by applying heat and pressure [Figure 6.6d]. The final step is electroplating thick copper on the bottom of VCSEL and blind vias, which are used to establish electrical path between top electrical pads and OIL pads [Figure 6.6e].

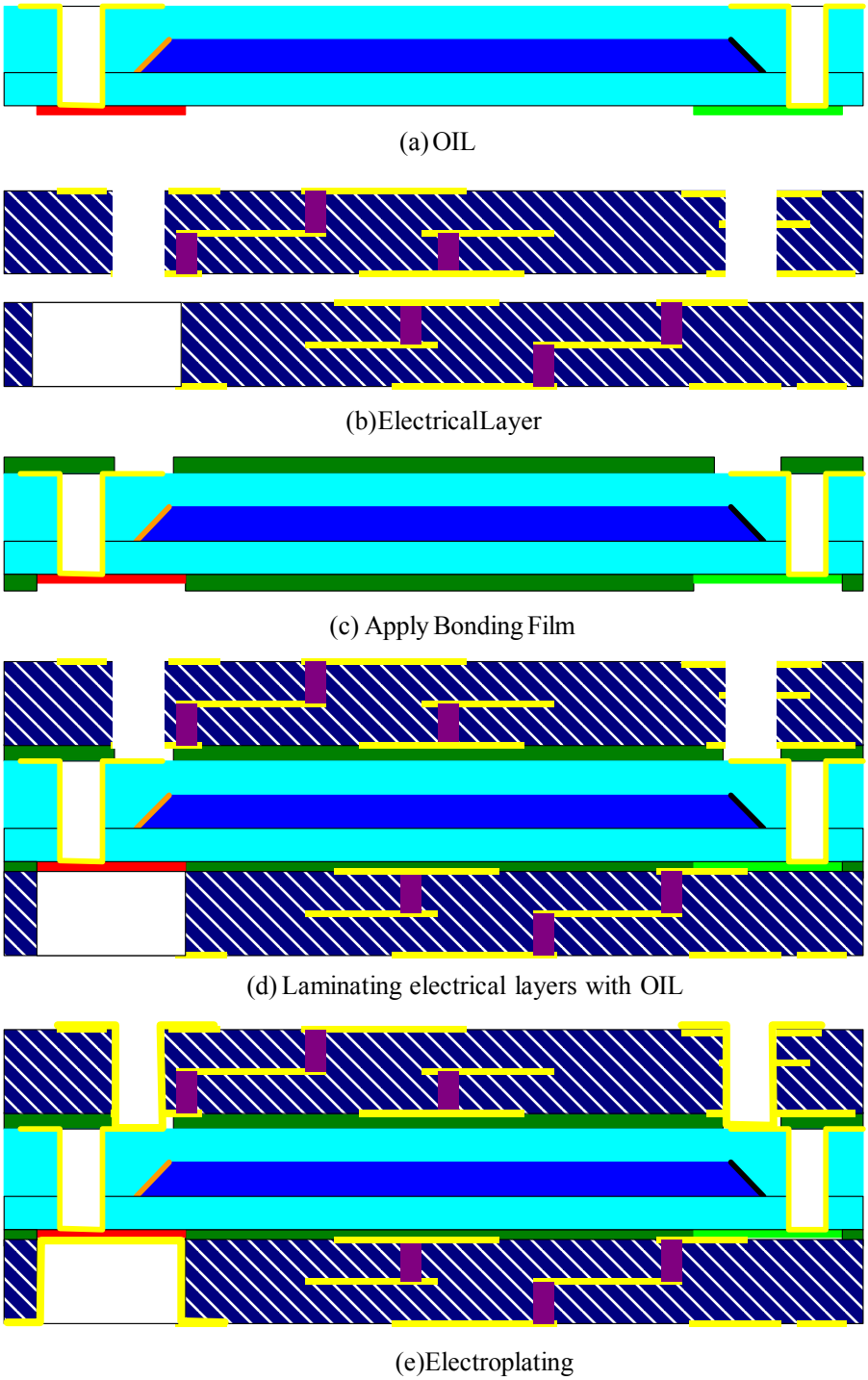


Figure 6.7 Flow chart of laminating electrical and optical interconnection layers.

Chapter 7: Summary

This dissertation describes a fully embedded board level optical interconnects in detail including the fabrication of the thin-film VCSEL array, its characterization, thermal management, the fabrication of optical interconnection layer, and the integration of mentioned devices on a flexible waveguide film.

All optical components are buried within electrical PCB layers in a fully embedded board level optical interconnect. Therefore, we can save foot prints on the top real estate of PCB and relieve packaging difficulty reduced by separating fabrication processes. To realize the fully embedded board level optical interconnection, very thin laser and photo-detector are required. Signals to drive VCSEL and signals from photo-detector flow through the electrical micro-vias.

An 1X12 array of 10μm thick thin-film VCSEL, emitting at 850nm wavelength, was fabricated by substrate removal technique. The GaAs substrate was completely removed by lapping and wet chemical etching. Measured L-I curve shows that 10μm thick VCSEL did not show thermal roll-over even at a high injection current level. Measured thermal resistances of 10μm thick VCSEL has the lowest value, nearly half of the 250μm thick VCSEL. The thin-film VCSEL shows superior characteristics, higher external quantum efficiency, and lower thermal resistance over the thicker VCSEL.

Thermal runaway of the embedded VCSEL is the critical concern due to the reliable operation of VCSEL for a long time. We investigated an effective heat sink structure for VCSEL through the 2D finite element thermal analysis. The 30μm thick,

directly electroplated, copper film on the back side of VCSEL array turns out to be an excellent heat sink without the sacrificing the strategy of easy packaging. We also found the maximum thickness of VCSEL which guaranteed reliable operation. Extremely thin VCSEL is very difficult to handle. As it turns out, 70μm is the maximum thickness for a reliable operation in a fully embed structure. This thick device can be handled by a state of the art automated pick and place machine.

45° waveguide micro-mirror couplers were fabricated by cutting waveguide ends at 45° using a microtome blade. The coupling efficiency of aluminum coated micro-mirror was calculated. The coupling efficiency between 12μm aperture VCSEL mounted at the bottom of 127μm thick cladding layer, and 50μm square waveguide was 92%, nearly 100% ignoring the reflectance of aluminum. The coupling efficiency did not change within ±1.5° angular deviation from 45°. For small aperture (3μm) VCSEL and thin bottom cladding layer (substrate), coupling efficiency was dropped to 34%. In this case, a typical 45° mirror can not be used, and other types of coupler, such as curved mirror or vertical optical via, are required to improve the coupling efficiency.

The optical interconnection layer was fabricated by compressive soft molding process. Molding is a suitable process for mass production. Mold was made of PDMS rubber. The micro-mirrors and waveguide were fabricated at the same time. Mold expansion during the process was compensated by adjusting the mold pressure. The core material of the waveguide was SU-8. Measured propagation loss of the waveguide was 0.6dB/cm at 850nm.

VCSEL and photo-detector array were integrated on the flexible waveguide film. UV-Nd:YAG laser or CO2 laser drilled micro-via was formed on the flexible waveguide film. The quality of micro-via is not good enough at this time. However, if an excimer laser is used to drill vias, the quality of via will be significantly improved.

Hybrid integration of the optical interconnection layer and electrical layers is ongoing at Sanmina-CSI. Reliability of the fully integrated system will be addressed in a future project.

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Vita

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