Two-stage Optimization Method for Efficient Power Converter Design Including Light Load Operation

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Abstract

Power converter efficiency is always a hot topic for switch mode power supplies. Nowadays, high efficiency is required over a wide load range, e.g., 20%, 50% and 100% load. Computer-aided design optimization is developed in this research work, to optimize off-line power converter efficiency from light load to full load. A two-stage optimization method to optimize power converter efficiency from light load to full load is proposed. The optimization procedure first breaks the converter design variables into many switching frequency branches. In each fixed switching frequency branch, the optimal designs for 20%, 50% and 100% load are derived separately in the first stage, and an objective function using the optimization results in the first stage is formed in the second stage to consider optimizing efficiency at 20%, 50% and 100% load. Component efficiency models are also established to serve as the objective functions of optimizations. Prototypes 400V to 12V/25A 300W two-FET forward converters are built to verify the optimization results.

Index Terms:

Computer-aided design, Full load efficiency, Light load efficiency, Optimization, Power converter

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LIST OF SYMBOLS

A_e	effective transformer cross section area
A_{L_AWG}	wire bare area of inductor
A_{L_win}	bobbin window area of inductor
A_{L_g}	effective gap area of inductor
b_{xl}	lower bound vector of design variables
b_{xu}	upper bound vector of design variables
B	flux density swing of transformer
B_L	flux density swing of inductor
B_m	transformer flux density peak-to-peak swing
B_{MAX}	maximum flux density of ferrite core
C_{fs}	a constant of switching frequency in optimization
$C_{Pri\_oss(er)}$	primary MOSFET output capacitance, energy related
$C_{\eta 20\%}$	20% load efficiency constraint
$C_{\eta 50\%}$	50% load efficiency constraint
$C_{\eta 100\%}$	100% load efficiency constraint
d_{AWG}	diameter of AWG wire in transformer primary winding
D	duty
E_{off}	turn-off energy consumed by primary MOSFET
f_{eq}	equivalent frequency for PWM converter for core loss calculation
f_s	switching frequency
F_{Rn}	ratio of AC-DC resistance of transformer
F_{Rn_L}	ratio of AC-DC resistance of inductor
h_{foil}	thickness of foils in transformer secondary winding
I_{out}	output current
I_{MAX}	full load output current
I_{L_rip}	ripple current of inductor current
I_m	magnetic current of transformer
I_{pri_on}	turn-on current of primary MOSFET
I_{pri_off}	turn-off current of primary MOSFET
I_{n_pri}	n^{th} harmonic component of primary transformer RMS current
I_{n_sec}	n^{th} harmonic component of secondary transformer RMS current
I_{SR_RMS}	RMS current of synchronous rectifier
I_{L_MAX}	maximum current of output inductor
I_{pri_rms}	RMS current of primary MOSFET
k_{20}	weighting factors of 20% load
k_{50}	weighting factors of 50% load
k_{100}	weighting factors of 100% load
k_{L_cu}	copper filled factor of inductor
l_{L_g}	length of inductor air gap
l_{MLT}	mean length per turn for output inductor
L	output inductor value
n_{sample}	number of samples in each switching cycle
N_{layer}	number of layers in transformer primary winding
N_L	number of turns of output inductor
N_{Lll}	number of paralleled wires in the inductor
N_p	number of transformer secondary turns
N_s	number of transformer secondary turns
$Optm_{20\%}$	optimized 20% load efficiency
$Optm_{50\%}$	optimized 50% load efficiency
$Optm_{100\%}$	optimized 100% load efficiency
p	number of layers in transformer winding
P_{aux}	loss of auxiliary power supply

Symbol	Description
P_{core}	core loss of transformer
P_{IC}	loss of primary controller
P_{loss}	sum of all losses
P_{L_copper}	copper loss of inductor
P_{L_core}	core loss of inductor
P_{out}	output power
P_{pri_sw}	loss of each primary MOSFET
P_{pri_cond}	conduction loss of primary MOSFET
P_{pri_gate}	gate drive loss of primary MOSFET
P_{pri_copper}	copper loss of transformer primary side
P_{sec_copper}	copper loss of transformer secondary side
P_{SR_sw}	switching loss of synchronous rectifier
P_{SR_gate}	gate drive loss of synchronous rectifier
P_{SR_cond}	conduction loss of synchronous rectifier
P_{SR_BD}	body diode loss of synchronous rectifier
Q_{oss}	output capacitance charge of secondary SR
Q_{pri_gate}	gate drive of power MOSFET
Q_{SR_gate}	gate drive of secondary SR
R_{pri_dc}	transformer DC resistance of the primary side
R_{pri_dson}	on state resistance of primary MOSFET
R_{L_dc}	DC resistance of output inductor
R_{SR_on}	on state resistance of synchronous rectifier
t_{d_on}	turn-on dead-time of synchronous rectifier
t_{d_off}	turn-off dead-time of synchronous rectifier
T_{on}	time of "on" state of primary MOSFET in a switching cycle
T_s	time of switching cycle
V_e	volume of transformer core
V_{in}	input voltage
V_{L_e}	volume of inductor core
V_{out}	output voltage
V_T	transformer voltage at secondary side
V_f	body diode forward voltage of synchronous rectifier
x	vector of design variables
η	general expression for converter efficiency
$\eta_{20\%}$	20% load efficiency
$\eta_{50\%}$	50% load efficiency
$\eta_{100\%}$	100% load efficiency
k, α, β	Steinmetz coefficients, provided by the core manufacture
δ	skin depth
ρ_{cu}	electrical resistivity of copper
μ_0	vacuum permeability
Ω_1	constraint set in stage I
Ω_2	constraint set in stage II

defining P_{IC}

defining V_e

defining *constraint set*

I. INTRODUCTION

Nowadays a power supply is required to have high efficiency over the whole load range. An off-line power supply is often required to meet target efficiencies at 20% load, 50% load and 100% load [1]. As light load efficiency is becoming important alongside full load efficiency, developing a systematic way to design a power supply that

meets the efficiency requirements over a wide load range is desirable. Design through optimization is one of the approaches to achieve these requirements.

Optimization for power electronic systems has been proposed for more than 30 years, and it has drawn attention from both academic and industrial fields. Generally speaking, the optimization of a power electronics system consists of several objective functions, for examples, efficiency, mass or cost models, with several constraints, such as temperature, mass or efficiencies. Optimization programs search a set of solutions and produce global or local optimal solutions. The number of converter design variables is often large. The variables are discrete and continuous. This presents challenges to optimize the infinitely many design combinations.

Early research work [2] utilized conventional optimization techniques, such as the sequential unconstrained minimization technique (SUMT) or the augmented Lagrangian (ALAG) penalty function technique, to optimize the converter mass. Design constraints were included into the optimization program. As an extension of [2], half-bridge converter optimization using a penalty function [3] was proposed to optimize the converter mass. Detailed converter optimization results are presented. A practical converter optimization approach suitable for industrial application was developed [4]. It utilized the nonlinear optimization program to optimize converter design, and both the optimization procedures and results were suitable from the point of applications.

A new insight into optimizing the buck converter power circuit and control parameters simultaneously has been presented [5]. It utilized a weighted objective function to solve the multi-objective optimization problems. The objective function was defined as a weighted sum of structural objectives, such as mass, price, and controller-related objectives. Efficiencies were set to be constraints to be satisfied in the required converter design. However, the optimization solutions are highly dependent on the weighting factors. Trial-and-error cannot be avoided. A gradient based constrained optimization of a fuel cell converter was presented in [6], with the trade-offs between efficiency and converter mass of optimized design given in graphs.

With the development of probabilistic optimization algorithms, such as genetic algorithms (GA), many optimization applications on power electronics system design have been reported. On the basis that power electronics system design variables can be considered as discrete, a GA based algorithm was applied to a boost a power

factor correction converter to optimize the converter cost [7]. The design results have a lower implementation cost when compared with conventional designs satisfying the same specifications. Buck converter transient optimization design has been presented [8], also using GA. A Monte Carlo search method was developed to optimize the volume of an interleave converter for automobile applications [9]. The interleaved converters have more design variables than a single converter, and the optimization improvement of results seem more significant than a single converter optimization. Passive component optimization has been shown [10], in which a GA was applied to optimize the front-end rectifier passive components for inverters.

The idea of Pareto-front in multi-object optimization was investigated in power converter design [11]. The Pareto–front of converter volume and efficiency means no further efficiency improvement can be achieved under a limited converter volume. Converter volume and efficiency were included in the weighted objective function to determine the degree of optimized efficiency or volume. The Pareto-front curve of power density versus efficiency showed that the optimized efficiency was limited by a certain volume constraint. A similar optimization approach was applied to phase-shift PWM converter design [12] to achieve 99% efficiency. Light load efficiency was considered in the optimization procedures.

From an optimization point of view, the objective functions in power converter design are often multi-object and non-convex in nature, with nonlinear constraints involving continuous and discrete variables. In practical converter design optimization, we should also consider the sensitivity of every design variable, e.g. switching frequency, flux density swing or duty cycle. Changes in these variables might influence the converter performance from light load to full load.

In this paper, instead of using a probabilistic algorithm mentioned earlier, we employ a deterministic algorithm to optimize power converter design, since the deterministic algorithms can provide more systematic way on parameter controlling. A two–FET forward converter efficiency optimization example is studied in this research. To solve the multi-objective optimization problem, the weighted objective function is popular for use with weighting factors specified by the designer. However, there are numerous combinations of the weighting factors, and the desirable combination is hard to determine. Trial-and-error cannot be avoided in the optimization processes. In this paper, a two–stage optimization procedure is proposed to optimize converter efficiency over a wide range. The optimization

procedure first divides the converter design process into many switching frequency branches. In each switching frequency branch, the optimal designs for 20%, 50% and 100% load are derived separately in the first stage, and an objective function is formed in the second stage to consider efficiencies optimization over the three loads.

In the paper, component efficiency models and analyzes are established in Section II. The overall optimization structure, including the two-stage optimization procedure, is presented in Section III. Optimization results and experimental results are illustrated in Section IV. Finally, the conclusions are drawn in Section V.

II. COMPONENT LOSS MODELS

The title of Section II is revised

In this section, simplified component models are established for losses analyses. Simplified models are desirable as they reduce computational complexity of optimization, and enhance parameter controlling. The conventional two-FET forward topology, which is widely used in desktop power supply, is selected as an example of converter efficiency optimization. The circuit topology is shown in Fig. 1. Fig. 2 shows the losses breakdown of a 300W two-FET forward converter which is optimized for full load; the distributions of losses from light load to full load

description of Fig. 2

are presented. A typical efficiency curve of the example converter is shown in Fig. 3.

description of Fig. 3

In a conventional off-line power converter, design optimization can help improve the efficiency over a wide load range. The components are pre-selected before the optimization procedure. Primary MOSFETs, an isolation transformer, synchronous rectifiers and an inductor are the major components determining the converter efficiency. To reduce the computation complexity, yet still fulfilling the accuracy of efficiency prediction, 7 design variables are used to optimize converter efficiency. The design variables are summarized in TABLE I. Note that transformer windings and inductor windings are calculated according to such design variables.

To calculate the component loss, the converter operating point will be derived. In the following analyses, we first assume that the converter operation is ideal. The number of primary and secondary turns can be calculated according to (1) and (2). Here, we prefer to use the duty and flux swing rather than the number of turns as the design variables, mainly because they can express the converter and magnetic characteristics from a design point of view. To calculate the harmonics of the current, a numerical method is used to sample a switching cycle with n_{sample} points ($n_{sample} = 256$ in this case) and construct the key current/voltage waveform numerically, as shown

in Fig. 4. The magnetic current is also included in the calculation. The set of governing equations is listed from (1) to (8). The harmonics of the transformer current are calculated by fast Fourier transform in order to calculate copper loss of the transformer, also shown in Fig. 4.

$$D = \frac{V_{out}N_s}{V_{in}N_p} \tag{1}$$

$$B_m = \frac{V_{in}T_{on}}{N_pA_e} = \frac{V_{in}DT_s}{N_pA_e} = \frac{V_{out}}{N_sA_ef_s} \tag{2}$$

$$N_s = \frac{V_{out}}{B_mA_ef_s} \tag{3}$$

$$N_p = \frac{N_sV_{out}}{DV_{in}} \tag{4}$$

$$I_{L\_rip} = \frac{(\frac{N_s}{N_p}V_{in} - V_{out})D}{f_sL} \tag{5}$$

$$I_m = \frac{V_{in}D}{f_sL_m} \tag{6}$$

$$I_{pri\_on} = \frac{N_s}{N_p}(I_{out} - I_{L\_rip}/2) \tag{7}$$

$$I_{pri\_off} = \frac{N_s}{N_p}(I_{out} + I_{L\_rip}/2) + I_m \tag{8}$$

A. Primary MOSFET

In a hard switching converter, accurate prediction of switching loss is important for optimization. Complete MOSFET switching models [13] [14], which include semiconductor characteristics, are complicated and the computational complexity will be dramatically increased. A simple and effective MOSFET switching loss model is desirable for the prediction of the switching loss from light load to full load. It should be noted that at full load condition under which the turn-off current is large, the switching loss is much higher than light load condition [13]. At light load condition, the turn-off current is small, the major loss is capacitive loss. As shown in Fig. 5, for MOSFET IPP50R140CP, the region under which turn-off loss is "flat" is below 5A; for IPP50R520CP, the "flat" region is below 2A. A curve fitting method is employed to record the SPICE simulation results. We can then obtain simple yet effective switching loss estimates. The turn-off energy consumed by primary MOSFETs is given by (9) with parameters summarized in TABLE II; we fixed the input voltage at 370 V in SPICE simulation.

$$E_{off}(I_{pri\_off}) = \begin{cases} a_1 e^{b_1 I_{pri\_off}} + a_2 e^{b_2 I_{pri\_off}} & \text{if } I_{pri\_off} \geq C_1, \\ \\ E_{off}(C_1) & \text{if } I_{pri\_off} < C_1. \end{cases} \qquad (9)$$

It should be noted that during turn–off, there are two currents flowing through the MOSFET and the total energy value is $E_{off}(I_{pri\_off})$. One current is to charge the output capacitance of MOSFET to V_{in} with the energy $1/2C_{Pri\_oss(er)}V_{in}^2 = E_{off}(C_1)$ (assuming $C_{Pri\_oss(er)}$ is constant to simplify calculation), the other current produces energy dissipation in the MOSFET channel with the energy $E_{off}(I_{pri\_off}) - E_{off}(C_1)$. Before turn–on, part of the energy stored in the output capacitance of MOSFET is recovered to the input capacitor (the V_{ds} of MOSFET drops from V_{in} to $1/2V_{in}$, this is particular for two-FET forward topology). During turn–on, the energy stored in the output capacitance $1/2C_{Pri\_oss(er)}(1/2V_{in})^2 = 1/4E_{off}(C_1)$ is discharged . The actual energy dissipated during switching is the energy dissipated in the MOSFET channel during turn–off $E_{off}(I_{pri\_off}) - E_{off}(C_1)$, plus the energy dissipated by discharging the output capacitance during turn–on $1/4E_{off}(C_1)$.

Simplified primary MOSFET switching loss of a two-FET forward converter can be expressed in (10). The conduction loss of primary MOSFET are given by (11).

more words on equation (10)

$$P_{pri\_sw} = f_s[E_{off}(I_{pri\_off}) - E_{off}(C_1) + \tfrac{1}{4}E_{off}(C_1)] \qquad (10)$$

$$P_{pri\_cond} = R_{pri\_dson}I_{pri\_rms}^2 \qquad (11)$$

B. Isolation Transformer

Transformer design is one of the key steps in achieving good efficiency both at light load and full load. The transformer loss models are presented in this part. The accuracy of existing models has been shown in previous research [15] [16], indicating that the models are reliable for predicting transformer loss. Analytical optimized transformer design was also reviewed by [17].

The empirical Steinmetz equation [18] is given by (12) and its related parameters are provided by the manufacturer to predict core loss [19].

$$P_{core} = V_e k f_{eq}^{\alpha} \Delta B^{\beta} \qquad (12)$$

For a unidirectional flux operation, the flux density swing is given by (13). f_{eq} is the equivalent frequency for a PWM converter [16], given by (14).

$$\Delta B = B_m/2 \tag{13}$$

$$f_{eq} = \frac{2}{\pi^2} f_s \frac{1}{D(1-D)} \tag{14}$$

The use of Dowell's Equations [20] is a one-dimensional approach to predict transformer AC resistance, and it is applied in this work. Round wires are applied to the primary side and copper foils to the secondary side, as shown in Fig. 6. DC resistance can be directly calculated by the winding geometry. The AC copper loss at each harmonic frequency can be calculated by summing the loss at each harmonics; here we take the sum up to the 32nd harmonics. The ratio of AC-DC resistance on the transformer primary side is given by (15).

$$F_{Rn\_pri}(p, X) = X \frac{e^{2X} - e^{-2X} + 2\sin(2X)}{e^{2X} + e^{-2X} - 2\cos(2X)} + 2X \frac{p^2-1}{3} \frac{e^{X} - e^{-X} - 2\sin(X)}{e^{X} + e^{-X} + 2\cos(X)} \tag{15}$$

where $X = \frac{h_{foil}}{\delta}$ is for foils and $X = \frac{\sqrt{\pi}d_{AWG}}{2\delta}$ is for round conductors [21].

The transformer primary side copper loss are given by (16). The secondary side transformer copper loss P_{sec_copper} can also be calculated using the same method, see (17). The transformer loss can be expressed as the sum of core loss and copper loss.

$$P_{pri\_copper} = R_{pri\_dc} \sum_{n=0}^{32} F_{Rn\_pri} I^2_{n\_pri} \tag{16}$$

$$P_{\sec\_copper} = R_{\sec\_dc} \sum_{n=0}^{32} F_{Rn\_\sec} I^2_{n\_\sec} \tag{17}$$

C. Synchronous Rectifier

Synchronous rectification (SR) is implemented at the secondary side to achieve high efficiency at the low-voltage-high-current output condition. The current driven synchronous rectifier driving scheme has been implemented in this research work [22]. The major losses for the synchronous rectifier are conduction loss, turn-off switching loss [23] and gate driving loss.

Turn-off switching loss and gate driving loss are almost constant from 20% load to 100% load. Turn-off switching loss can be simplified [23], with the energy stored in the stray inductance being dissipated by the resistive parts of

the circuit, such as PCB routes and transformer windings. The reverse recovery charge is ignored in the calculation.

The simplified model for turn-off loss and gate driving loss of SR are given by (18) and (19).

$$P_{SR\_sw} = \tfrac{1}{2}V_T Q_{oss} f_s \tag{18}$$

$$P_{SR\_gate} = Q_{SR\_gate} V_g f_s \tag{19}$$

The conduction loss of SR is given by (20). The body diode conduction loss during dead time is described in (21).

$$P_{SR\_cond} = I_{SR\_RMS}^2 R_{SR\_on} \tag{20}$$

$$P_{SR\_bd} = V_f(I_{out} - I_{L\_rip}/2)t_{d\_on}f_s + V_f(I_{out} + I_{L\_rip}/2)t_{d\_off}f_s \tag{21}$$

where t_{d_on} and t_{d_off} are the turn-on and turn-off dead-times of the synchronous rectifier. Since a synchronous rectifier conducts in the reverse manner, the body diode conducts before the synchronous rectifier is turned on. Hence, zero voltage turn-on can be achieved in a synchronous rectifier.

D. Output Inductor

The output inductor is also a critical component in an off–line PWM power converter since the secondary side output current is large. A gapped ferrite core is selected to be the inductor core because core loss of ferrite material are relatively low and it has better light load efficiency.

The inductance characteristics can be expressed as follows:

$$B_{MAX} = \frac{L I_{L\_MAX}}{N_L A_{L\_g}} \tag{22}$$

$$k_{L\_cu} A_{L\_win} = N_L N_{Lll} A_{L\_AWG} \tag{23}$$

$$R_{L\_dc} = \frac{\rho_{cu} N_L l_{MLT}}{N_{Lll} A_{L\_AWG}} \tag{24}$$

By inserting (22) and (23) into (24), the inductor DC resistance is as (25):

$$R_{L\_dc} = \frac{\rho_{cu} l_{MNT} L^2 I_{L\_MAX}^2}{k_{L\_cu} A_{L\_win} B_{MAX}^2 A_{L\_g}^2} \tag{25}$$

The required gap length is given by (26).

$$l_{L\_g} = \frac{\mu_0 A_{L\_g} N_L^2}{L} \tag{26}$$

It can be implied by (25) that the DC resistance of the inductor is proportional to the square of the inductor value. Since the current ripple of the output inductor is smooth, the frequency harmonics is summed up to the 5th harmonics to calculate the copper loss of the inductor, given by (27).

$$P_{L\_copper} = R_{L\_dc} \sum_{n=0}^{5} F_{Rn\_L} I_{n\_L}^2 \qquad (27)$$

The flux density swing of the output inductor is given by (28), and the core loss of the inductor can be expressed

using the Steinmetz equation (29).

$$\Delta B_L = \frac{L I_{L\_rip}}{2 N_L A_{L\_g}} \qquad (28)$$

$$P_{L\_core} = V_{L\_e} k f_{eq}{}^{\alpha} \Delta B_L{}^{\beta} \qquad (29)$$

E. Auxiliary power supply denoting auxiliary power supply

The auxiliary power supply provides the power for primary side controller and gate drives of MOSFETs.

$$P_{pri\_gate} = Q_{pri\_gate} V_g f_s \qquad (30)$$

$$P_{aux} = P_{IC} + P_{pri\_gate} \qquad (31)$$

A summary of the losses are listed in TABLE III. The converter efficiency can be expressed as in (30). which

serves as the objective function to be considered in Section III.

$$\eta = \frac{P_{out}}{P_{out} + P_{loss}} \qquad (32)$$

P_{loss} is the sum of all losses in TABLE III.

III. OPTIMIZATION PROCEDURE

the title of section III has been revised

A two-stage optimization procedure is proposed to systematically optimize the power converter efficiency over

a wide load range, as shown in Fig. 7. The description of the two-stage optimization procedure is presented in this

section. The optimization procedure involves breaking the converter design into many fixed switching frequency

branches in order to avoid the optimizer being trapped at some local minima. This will be further explained in

Part A of this section. At each frequency, a two-stage procedure is developed. In Stage I, the best efficiencies for

20%, 50% and 100% load are found separately by the optimizer. In this stage, the problem is a single-objective

optimization. To cater for the multi-objective optimization, a second stage is used. In Stage II, the three optimized

efficiency values at 20%, 50% and 100% load established in Stage I become the reference points for optimizing

the converter efficiency over a wide range. The final design efficiency should be as close to the best efficiency in Stage I as possible. A function which aims to optimize the converter efficiency over 20%, 50% and 100% load is formulated. A detailed explanation of these stages is given in Part B of this section.

The optimization program in this paper is developed under the MATLAB environment. The $\texttt{fmincon}(x)$ function of MATLAB optimization toolbox is applied as the optimizer to solve the non-linear constrained optimization problems. The "active-set" algorithm is used in the $\texttt{fmincon}(x)$ function. Detailed optimization procedures can be found in [24]. Details of the optimizer is described

The characteristics of the power components are discrete, such as primary MOSFET, transformer core and bobbin size. The continuous optimization methods cannot handle such discrete values, so we pre-select the discrete components at the discrete component selection stage. In the continuous optimization stage, the discrete components and their related parameters are fixed.

A. Fixed Switching Frequency Branches

It is an issue whether to set the switching frequency to be a variable in the gradient search optimization or not. When the switching frequency varies over a range, the optimization solutions maybe trapped at the initial switching frequency point, which is regarded as a the local minimum. This problem was also reported in previous research [2], [4], [25]. In order to avoid the optimization to be trapped at the local minima, the switching frequency is kept constant in each optimization branch. This allows us to avoid the solution to be trapped at the local minimum. The final optimized results are a set of design variables at different constant switching frequencies, ranging from 50 kHz to 250 kHz. Hence, a constant switching frequency sub-optimization was developed, as shown in the flow chart Fig. 7.

The local minima problem caused by switching frequency is shown in Fig. 8. In this case the switching frequency is set to be a variable in the gradient search optimization process. Starting from different initial points, the converged results give $Optm_{50\%}$ (minimizing the losses at 50% load). The local minima are clearly shown in Fig. 8. The 50% load losses are also very close at these two local minima.

While considering the optimizing efficiency from light load to full load, the influence of the switching frequency

is significant. In a constant switching frequency PWM converter, a reasonable switching frequency should be chosen. High switching frequency produces more switching loss for semiconductor devices. Low switching frequency needs more winding in the transformer to suppress increasing core loss, hence, increasing the copper loss. The optimized design for each switching frequency has been recorded in each switching frequency branch.

B. Two-Stage Optimization

Here we aim to optimize the converter efficiency from 20% load to 100% load, subject to efficiency constraints. This is a typical multi-objective optimization problem. One conventional method is to use the weighted objective function approach. However, the weighting factors are fixed before the optimization results are found and trial-and-error is still needed to determine the suitable weighting factors. A two-stage optimization procedure is presented to handle such an optimization problem, as depicted in the flow chart Fig. 7. The optimization procedures are described below.

Let x denote a vector containing all the design variables, such as flux swing, duty and diameter of transformer wire and etc. given by (33). The switching frequency is set to be constant in each optimization branch.

$$x = (B_m, D, d_{AWG}, n_{layer}, h_{foil}, L) \tag{33}$$

The lower bound vector and upper bound vector of the design variables are given by (34), where the expression "$x - b_{xl} \geq\geq 0$" denotes "$x - b_{xl}$" to be a vector with non-negative entries.

lower/upper bound vector of design variables

$$\begin{cases} x - b_{xl} \geq\geq 0 \\ b_{xu} - x \geq\geq 0 \end{cases} \tag{34}$$

The 20% load converter efficiency $\eta_{20\%}$ under a constant switching frequency is given by (35):

$$\eta_{20\%}(x) = \frac{P_{out}(I_{out})}{P_{out}(I_{out}) + P_{losses}(x)} \Big|_{\substack{f_s=C_{f_s} \\ I_{out}=0.2I_{MAX}}} \tag{35}$$

Similar expressions are formulated for $\eta_{50\%}$ and $\eta_{100\%}$.

Stage I:

The aim of this stage is to identify the optimal efficiency at each load point through a single object optimization.

$$Optm_{20\%} = \arg \max_{x \in \Omega_1} \eta_{20\%}(x) \Big|_{f_s=C_{f_s}} \tag{36}$$

where the $Optm_{20\%}$ is the argument to optimize 20% load efficiency, the constraint set Ω_1 is given by (37):

arg means argument, which is the output of a function

$$\Omega_1 = \{x \mid x - b_{xl} \geq\geq 0, \ b_{xu} - x \geq\geq 0\} \qquad \text{constraint set in Stage I} \qquad (37)$$

The optimized 20% load converter design given by (36) is aimed at optimizing the 20% load efficiency only. This design may not give good efficiency at 50% and 100% load. $Optm_{20\%}$, however, is a reference point for further optimization in Stage II. It can also provide a guideline for the efficiency to be expected during 20% load condition under the specified switching frequency. The same process is repeated for $Optm_{50\%}$ and $Optm_{100\%}$.

Stage II:

Form the following objective function:

$$f(x) = [Optm_{20\%} - \eta_{20\%}(x)]^2 + [Optm_{50\%} - \eta_{50\%}(x)]^2 + [Optm_{100\%} - \eta_{100\%}(x)]^2 \qquad (38)$$

and consider the optimization problem:

$$\min_{x \in \Omega_2} \ f(x) \qquad (39)$$

where the constraint set Ω_2 is given by (40).

The constraint in stage II

$$\Omega_2 = \{x \mid x - b_{xl} \geq\geq 0, \ b_{xu} - x \geq\geq 0, \ \eta_{20\%}(x) \geq C_{\eta 20\%}, \ \eta_{50\%}(x) \geq C_{\eta 50\%}, \ \eta_{100\%}(x) \geq C_{\eta 100\%}\} \qquad (40)$$

In Stage II, the objective function $f(x)$ is formulated as the sum of squares of the departures of the design objectives $(\eta_{20\%}(x), \eta_{50\%}(x), \eta_{100\%}(x))$ from $(Optm_{20\%}, Optm_{50\%}, Optm_{100\%})$. If one of the departures is larger than the others, it will be amplified by squaring. Thus, more penalties will be imposed for large departure from the target value, causing the optimizer to suppress the amplified departure. The optimized solution is as close as possible to three reference points. The optimizer establishes the minimum value of $f(x)$ in each switching frequency branch.

IV. OPTIMIZATION AND EXPERIMENTAL RESULTS

A. OPTIMIZATION RESULTS

The results of optimization are presented in this part. An example of optimization is given under the fixed switching frequency of 200 kHz. Design variables to optimize for $Optm_{20\%}$, $Optm_{50\%}$ and $Optm_{100\%}$ are presented in TABLE IV. Similar optimization procedures are carried out for frequency in the range from 50 kHz to 250 kHz, with an interval of 10 kHz.

There are three series of designs in Fig. 9, namely the $Optm_{20\%}$ series, the $Optm_{50\%}$ series, and the $Optm_{100\%}$ series. In each series, optimal designs are produced in the frequency range from 50 to 250 kHz, with an interval of 10 kHz. For example, each point in the $Optm_{20\%}$ series represents a converter design. This series gives a set of converter designs for the entire frequency range. The $Optm_{20\%}$ series is optimized for 20% converter load and the 20% load efficiencies are shown in Fig. 9 (a). The designs in this series are then put to 50% converter load and the corresponding efficiencies are shown in Fig. 9 (b). In Fig. 9 (c), the series are put to 100% converter load and results are shown in similar manner.

It can be indicated from Fig. 9 (c) that the $Optm_{20\%}$ series has lower efficiencies at the full load condition for the entire switching frequency range. The $Optm_{100\%}$ series also cannot provide the best efficiencies at 20% load condition. Also, small efficiency differences have been observed between $Optm_{20\%}$ and $Optm_{50\%}$ at 20% load. The efficiency differences between $Optm_{100\%}$ and $Optm_{50\%}$ are also small at 100% load condition. So it is not the best strategy only to optimize power converter full load efficiency or light load efficiency.

Detailed two-stage optimization results are shown in TABLE V, at switching frequency 50, 100, 150 and 200 kHz. TABLE V shows that higher switching frequency produces lower 20% load efficiency. From 50 kHz to 100 kHz, there is 1.1% efficiency improvement at full load and 0.3% efficiency improvement at middle load, with 0.6% efficiency sacrifice at light load condition. The 20% load efficiency of 200 kHz design is 1.6% less than that of the 100 kHz design. At full load, the 200 kHz design is only 0.3% more efficient than the 100 kHz design. This efficiency gain of 0.3% does not justify the 1.6% efficiency drop at light load. 100 kHz is chosen to be the ultimate design, since it produces the best 50% load efficiency, and the second best 20% load efficiency. The full load

efficiency is ranked third among four designs. However, the 95.2% full load efficiency of 100 kHz design is still close enough to 95.5% of 200 kHz design and 1.1% efficiency higher than 94.1% of 50 kHz design.

Further analyzes of 100 kHz design are presented in Fig. 10. If the design is to optimize full load efficiency only, there is a large departure (about 1%) at 20% load compared with $Optm_{20\%}$. When the optimizations are aimed over wide load range using the proposed two-stage method, the departures from the best values $Optm_{20\%}$ and $Optm_{100\%}$ are small (both about 0.2–0.3%). Thus, optimization for wide load range is more desirable than optimizing full load efficiency only.

B. EXPERIMENTAL RESULTS

Two two-FET forward converters are built to verify the optimization results. One converter is designed to optimize the efficiency over a wide load range. The other is designed to optimize the full load efficiency only. The converters have the same specifications. The input voltage is 370 V, output voltage is 12 V loading from 0 to 25 A. Current mode controller UC3844 is implemented on primary side. Current driven synchronous rectifiers are used on secondary side. The circuit parameters are summarized in TABLE VI. The converter schematic diagram is shown in Fig. 11.

The comparison of predicted efficiency optimized for wide load range and its corresponding experimental results are shown in Fig. 12. The predicted results match the experimental results from light load to full load. The loss models are only approximation of the true losses that some non-linear effects are not fully captured in these models. The converter 50% and 100% load efficiencies are higher than 95% and the 20% load efficiency is above 92%, which illustrate the merit of efficiency optimization.

The efficiencies of the two prototype converters are compared in Fig. 13. The efficiency of wide load range design is 1% better than that of full load design at 20% load. On the other hand, the full load efficiency of wide load range design is 0.4% lower than the efficiency of full load design. The converter 20% load efficiency can be increased by optimization without much sacrifice of the full load efficiency.

V. CONCLUSIONS

A two-stage optimization procedure to optimize the power converter efficiency from light load to full load is proposed. The optimization procedure first breaks the converter design variables into many switching frequency branches. In a fixed switching frequency branch, the optimal designs for 20%, 50% and 100% load are obtained separately in the first stage, and an objective function using the results in first stage is formed in the second stage to consider efficiencies optimization over light, medium, and full loads. Efficiency models of power components are established and implemented into the objective function. The proposed optimization procedure determines the optimal efficiency design that fit the efficiency requirements over a wide load range. Optimization results are presented with analyzes over a selected switching frequency range from light load to full load. Two two-FET forward converters example are built and compared as a mean to the verify power converter efficiency optimization. The medium and full load efficiencies are higher than 95%, which illustrate the optimization method can design efficient power converters. Through the optimization, the converter 20% load efficiency can be increased without much sacrificing of the full load efficiency.

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TABLE I
DESIGN VARIABLES

Design variable names	Symbols
Switching frequency	f_s
Flux swing	B_m
Duty	D
Diameter of AWG winding (primary)	d_{AWG}
Number of layers (primary)	N_{layer}
Thickness of secondary foil	h_{foil}
Inductor	L

TABLE II
PARAMETERS FOR PRIMARY MOSFET

MOSFET	R_{Pri_dson} (mΩ)	$C_{Pri\_oss(er)}$ (pF)	Q_g (nC)	a_1	b_1	a_2	b_2	C_1
IPP50R520CP	520	31	13	7.7	-2.3	0.98	0.47	1
IPP50R250CP	250	63	27	4.8	-0.18	0.49	0.52	1
IPP50R140CP	140	110	48	7.9	0.03	$1e-5$	2.15	1

TABLE III
SUMMARY OF MAJOR COMPONENT LOSSES

MOSFET	P_{pri_sw}
	P_{pri_cond}
Transformer	P_{pri_copper}
	P_{sec_copper}
	P_{core}
Synchronous Rectifier	P_{SR_gate}
	P_{SR_sw}
	P_{SR_cond}
	P_{SR_bd}
Inductor	P_{L_copper}
	P_{L_core}
Auxiliary	P_{aux}

TABLE IV
$Optm_{20\%}$, $Optm_{50\%}$ AND $Optm_{100\%}$ AT 200 kHz

$f_s = 200$kHz	$Optm_{20\%}$	$Optm_{50\%}$	$Optm_{100\%}$
B_m	0.10 T	0.13 T	0.17 T
D	0.45	0.45	0.45
d_{AWG}	0.10 mm	0.10 mm	0.10 mm
N_{layer}	6.6	5.0	4.4
h_{foil}	0.1 mm	0.12 mm	0.16 mm
L	8.6μH	6.0μH	6.0μH
$\eta_{20\%}$	91.6	91.4	90.7
$\eta_{50\%}$	94.9	95.1	94.9
$\eta_{100\%}$	94.9	95.6	95.7

TABLE V
OPTIMIZATION RESULTS

	50 kHz	100 kHz	150 kHz	200 kHz
B_m	0.27 T	0.20T T	0.15T T	0.12T T
D	0.27	0.4	0.44	0.45
d_{AWG}	0.10mm	0.10mm	0.10mm	0.10mm
N_{layer}	10.6	7.4	5.5	4.9
h_{foil}	0.10mm	0.13mm	0.12mm	0.12mm
L	24.5μH	12.1μH	8.3μH	6.0μH
$Optm_{20\%}$	93.8	93.4	92.6	91.6
$Optm_{50\%}$	95.2	95.5	95.4	95.1
$Optm_{100\%}$	94.3	95.4	95.6	95.7
$\eta_{20\%}$	93.7	93.1	92.4	91.5
$\eta_{50\%}$	95.2	95.5	95.4	95.1
$\eta_{100\%}$	94.1	95.2	95.4	95.5

TABLE VI
COMPONENTS LIST

Two-FET-Forward converter (100kHz) optimized for wide load range		
Primary MOSFETs	IPP50R299CP	
Isolation transformer	Turn ratio 60 : 5 ETD39 3C90	Primary:AWG40*32 Litz wires Secondary: 0.15mm copper foils
Output inductor	12μH EE36/18/11 N87	AWG25*30 $N_L = 9$
Synchronous rectifier	BSC067N06LS3*2	Current driven SRs Paralleling 2 SRs
Two-FET-Forward converter (100kHz) optimized for full load		
Primary MOSFETs	IPP50R299CP	
Isolation transformer	Turn ratio 50 : 4 ETD39 3C90	Primary:AWG40*40 Litz wires Secondary: 0.15mm copper foils
Output inductor	8μH EE36/18/11 N87	AWG25*40 $N_L = 6$
Synchronous rectifier	BSC067N06LS3*2	Current driven SRs Paralleling 2 SRs
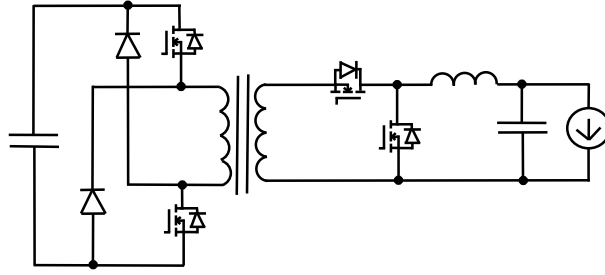
Fig. 1.   Example of two-FET forward converter.
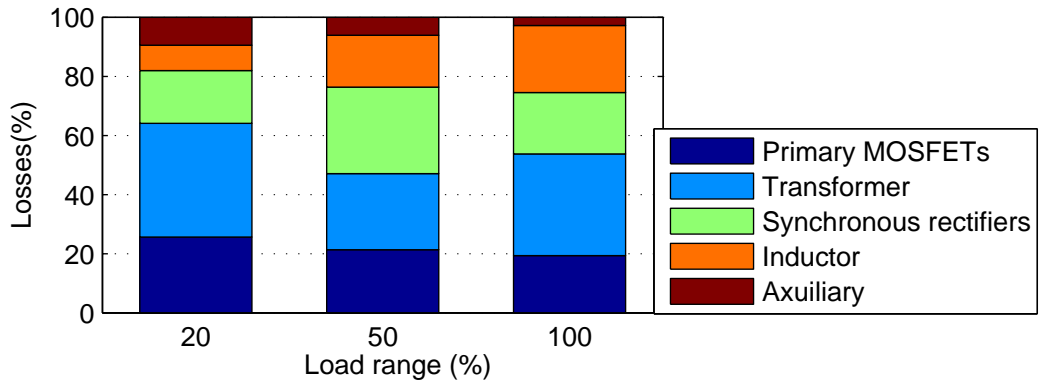
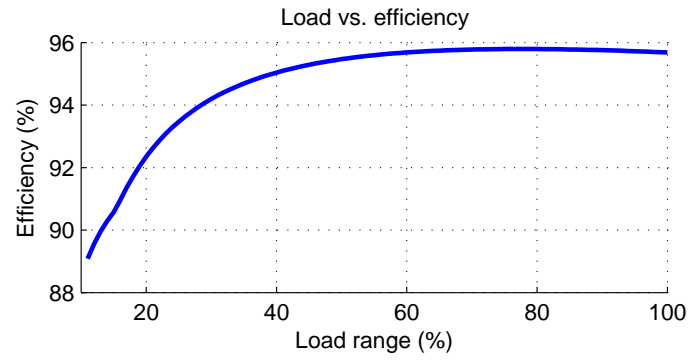Fig. 2.   Losses breakdown of a 300W DC/DC forward converter.

Fig. 3.   A typical efficiency curve for a 300 W off-line PWM DC/DC converter.
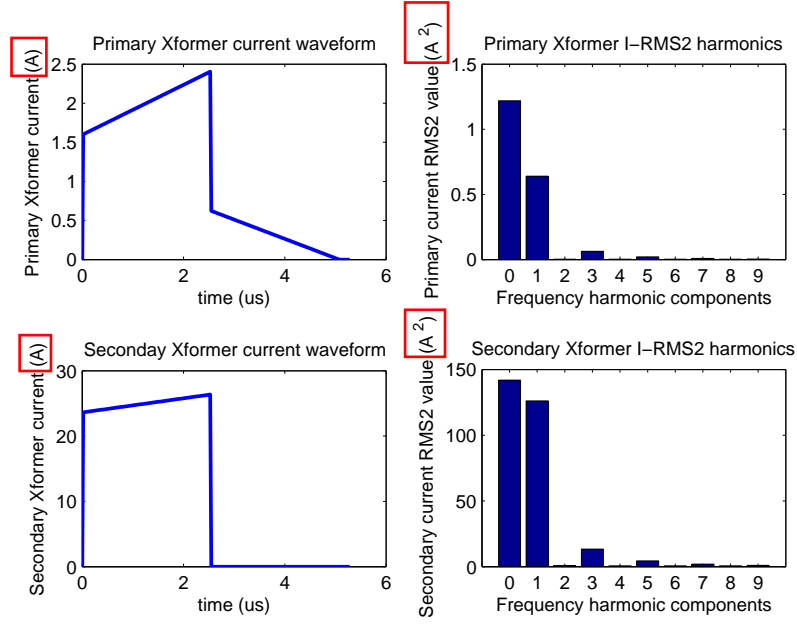
the y-axes units are added

(A)
Primary Xformer current waveform

(A²)
Primary Xformer I–RMS2 harmonics

(A)
Seconday Xformer current waveform

(A²)
Secondary Xformer I–RMS2 harmonics

Fig. 4. Transformer current waveform and harmonic components, calculated by numerical methods.
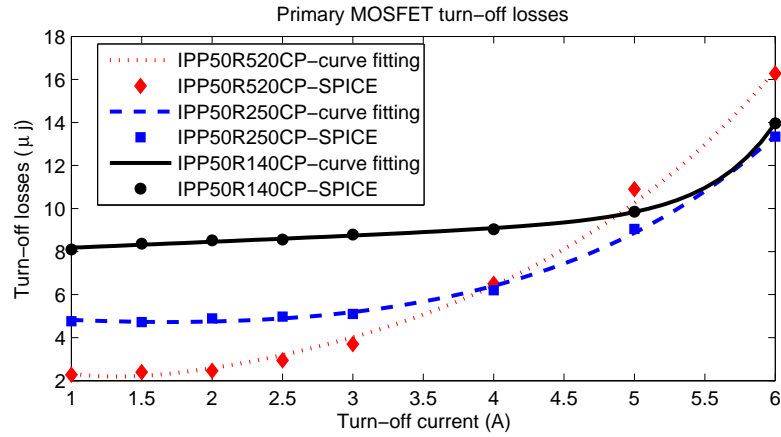
Fig. 5. PSPICE simulated primary MOSFET turn-off loss.
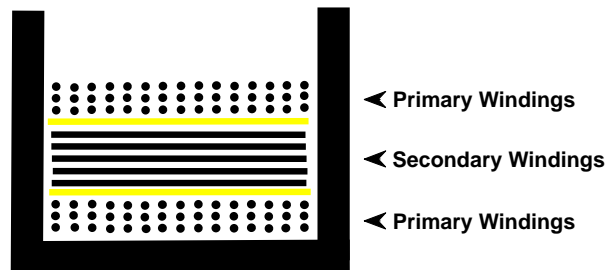
Fig. 6. Transformer winding structure.

Fig. 7.   Flow chart of power converter efficiency optimization.
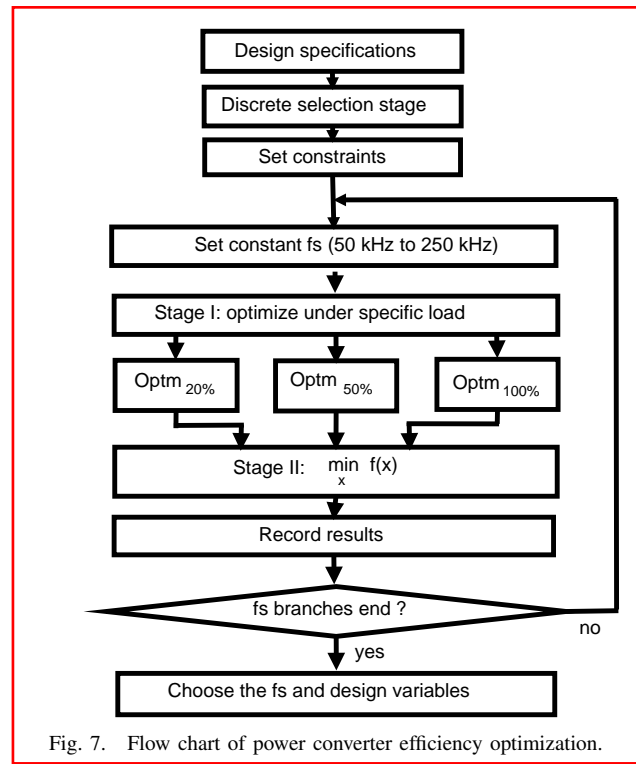
This flow chart is revised
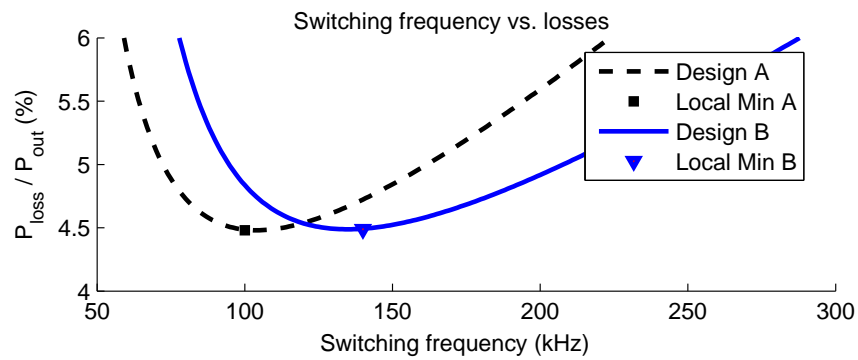
Fig. 8.   Local minima of optimization; Design A and B are two local minima solutions.
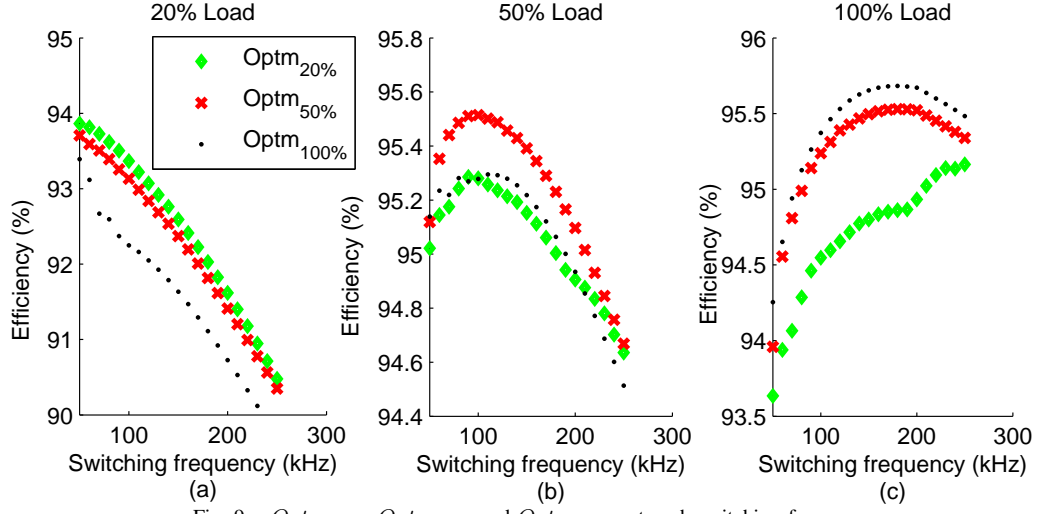
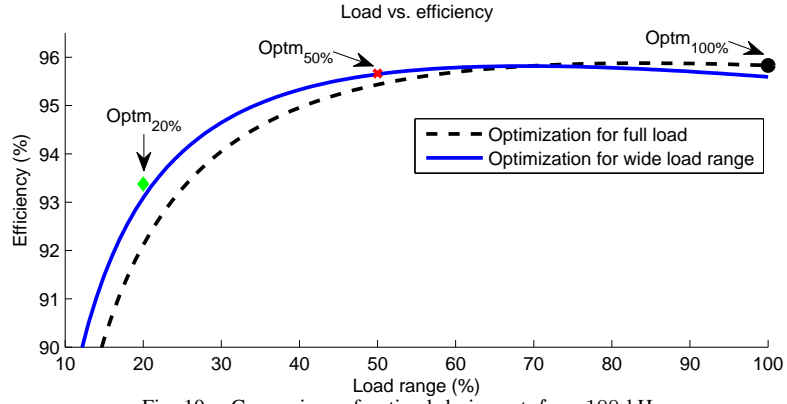Fig. 9. $Optm_{20\%}$, $Optm_{50\%}$ and $Optm_{100\%}$ at each switching frequency.

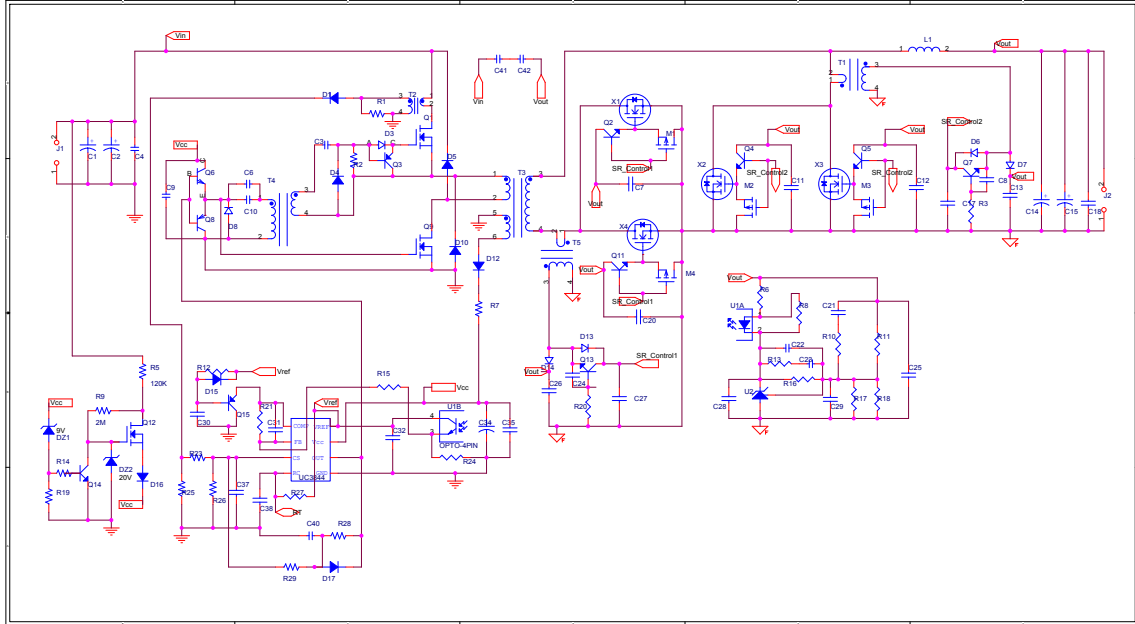
Fig. 10. Comparison of optimal designs at $f_s = 100$ kHz.
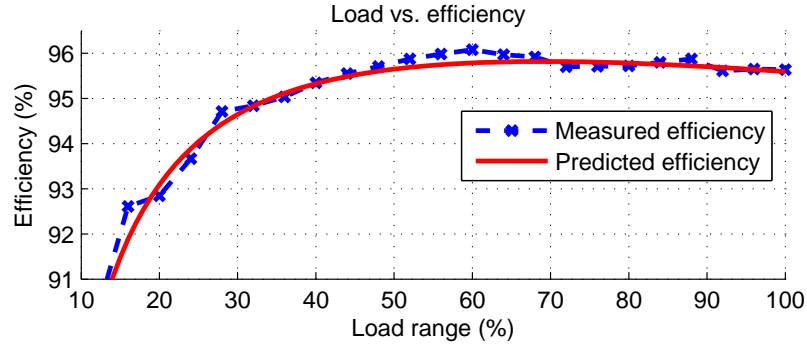

Fig. 11. Schematic of prototype converter.

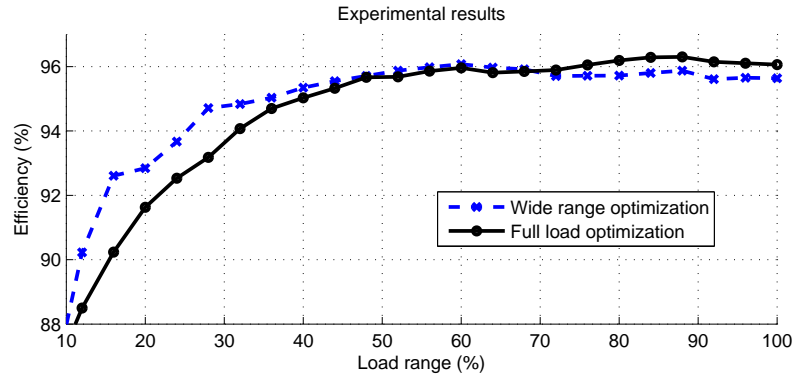Fig. 12. Predicted efficiency and experimental efficiency at 100kHz, $V_{in} = 370V$.

Fig. 13. Experimental efficiency comparisons, $V_{in} = 370V$.