Frequency- and Time-Domain Yield Optimization of a Power Delivery Network Subject to Large Decoupling Capacitor Tolerances

Aurea E. Moreno-Mojica and José E. Rayas-Sánchez

***Abstract*— Sub-optimal design of power delivery networks (PDN) may cause performance deterioration and severe functional failures on high-speed computer platforms. Voltage regulators (VR) distribute controlled voltage in the PDN to the active devices, providing a steady power supply at a desired DC voltage level with an acceptable noise level or ripple. Unacceptable voltage drops can be caused by transient switching currents at the devices. Many decoupling capacitors are commonly used to lower the PDN impedance profile in order to reduce power supply noise and to supply fast transient current to switching devices. However, commercially available decoupling capacitors typically present large manufacturing variability. In this paper, we first propose an optimization methodology that gradually finds the best compensation parameter values of a buck converter VR to meet suitable stability criteria. Simultaneously, the number of parallel decoupling capacitors in the PDN is minimized while meeting a frequency-domain impedance profile specification and a time-domain minimum voltage droop requirement under nominal parameter values. Finally, a statistical analysis, yield estimation, and yield optimization of the nominally optimized PDN subject to large decoupling capacitor tolerances is presented. We consider the impedance profile, transient voltage droop, and voltage regulator stability as the responses of interest for yield calculation.**

***Index Terms*— decoupling capacitors, impedance profile, Monte Carlo, noise control, power delivery network, power integrity, signal integrity, stability, statistical analysis, voltage droop, voltage regulator, yield.**

I. Introduction

A power delivery network (PDN) consists of all the devices and interconnects that distribute the voltage and power throughout a physical board in modern computer platforms. A well-designed PDN should ensure that the distributed voltage is controlled, steady, within the desired margins, and with an acceptable noise level or ripple. Unsuccessful noise control on the PDN can cause a closing of the eye diagram at the receiver of a high-speed link, leading to functional failures in the computer platform since internal core circuits suffer setup and hold-time errors.

At low frequencies, the voltage regulator (VR) is the largest contributor of voltage noise in a PDN [1]. The VR compensation feedback loop maintains a constant voltage in spite of changes in the input voltage or in the effective load impedance [2]. However, undesired output voltage ringing can occur if this compensation feedback loop becomes unstable or with too small stability margins.

At high frequencies, the voltage noise seen on the pads of the die comes from voltage drops caused by transient currents when the devices start switching. The transmitted voltage signal level depends on the frequency spectrum of the current drawn by the devices [1]. The impedance profile is a figure of merit of the acceptability of the PDN design, since by knowing the worst-case current drawn by the chips and the required voltage tolerance, one can determine an impedance profile target that the PDN should meet to keep the supplied voltage at an acceptable level for all the chips.

A common industrial practice consists of using many parallel decoupling capacitors to lower the impedance profile magnitude of the PDN, keeping it below a target that ensures small variations in the power supply voltage when large current load changes occur [3]. Decoupling capacitors are also used to provide switching circuits with extra current when the VR is too slow to respond [4]. The more decoupling capacitors are employed, the better impedance profile is achieved. However, an excessive number of decoupling capacitors might not be feasible to accommodate in the available PDN area, and unnecessarily increases manufacturing costs. Additionally, the actual capacitance of commercially available capacitors used for decoupling can fluctuate significantly from its nominal value, which impacts on the PDN performance.

This paper proposes for the first time a frequency- and time-domain yield optimization approach suitable for power delivery networks considering the impact of large tolerances in the decoupling capacitors. We first propose an optimization-based methodology to determine the best compensation parameter values of a buck converter VR under nominal conditions, aiming to meet adequate stability criteria in the PDN application. At the same time, the number of parallel decoupling capacitors in the PDN is minimized while meeting the impedance profile target and the voltage droop specifications, considering, simultaneously, frequency- and time-domain performances. Next, a statistical analysis, yield estimation, and yield optimization of the nominally optimized PDN subject to large decoupling capacitor tolerances is realized. To the best of the authors' knowledge, this is the first work reported in the scientific literature where yield

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estimation and optimization is performed on a PDN. As the responses of interest for yield calculations, the impedance profile magnitude, the transient voltage droop, and the voltage regulator stability are included. The numerical results obtained from our proposed optimization approach demonstrate its effectiveness to assess and improve the PDN performance and reliability, confirmed by a significantly increased overall yield.

This paper significantly expands our work in [5] by incorporating the following aspects: a) we make a clearer and more rigorous formulation of the nominal optimization of the number of PDN decoupling capacitors and VR compensation parameters; b) we describe the key role of decoupling capacitors in PDN design, along with their practical limitations; c) we assess the impact of the decoupling capacitors variability by performing a statistical analysis and yield estimation of a nominally optimized PDN subject to large decoupling capacitor tolerances; and d) we maximize the overall PDN performance yield considering the large variability in decoupling capacitors, obtaining a high yield in impedance profile, VR stability, and transient voltage droop.

The rest of our paper is organized as follows. Section II briefly reviews the importance of decoupling capacitors in the design of a PDN, addressing their types and variability. Section III briefly describes the PDN considered, and the VR simulation models used. Section IV details the proposed methodology for nominal optimization of the VR stability and the number of decoupling capacitors in a PDN to meet frequency- and time-domain specifications. Section V describes our formulation of the statistical analysis and yield estimation of a PDN and provides criteria to calculate the number of simulations needed for reliable yield estimation. Section VI evaluates the impact of the decoupling capacitor variability in the time- and frequency-domain performance of a PDN. The proposed optimization technique to maximize the yield of a nominally optimized PDN is presented in Section VII. Finally, Section VIII presents our conclusions.

II. Decoupling Capacitors in a PDN

A good PDN design is determined by its ability to keep the load voltage within an acceptable operating range even as the load current changes or the input voltage fluctuates. Furthermore, an optimal PDN impedance profile reduces electromagnetic emissions, which contributes to passing the regulating agency's emission standards [4] [6].

Keeping the impedance of the PDN low across a broad range of frequencies, from DC to several hundred MHz, helps to suppress power supply noise [7]. This is typically done by using several stages of parallel decoupling capacitors to decrease the inductive effect in the loop current path [3] [4].

A key element of a PDN is the VR. Several VRs are typically used to deliver the biasing voltages needed by the different chips on the computer platform. When the chips start operating from an idle stage, they create fluctuations in the load current. Each VR has a control loop that helps to regulate these changes. However, the response time of the VR control loop can be slow, in the order of micro-seconds. As a result, temporary voltage fluctuations may appear on the die before the VR can mitigate the changes. These fluctuations can jeopardize the performance and the reliability of the connected devices [7]. Parallel decoupling capacitors are used in this case as local sources of charge to mitigate the current surges by quickly supplying current to loads and stabilizing voltage levels when the VR is not able to do so [8].

In practice, many decoupling capacitors of different values are usually needed to improve the PDN performance. However, using too many decoupling capacitors may result in excessive manufacturing costs. Additionally, the parallel connection of multiple different capacitors can result in sharp anti-resonant impedance peaks [9]. These peaks can magnify voltage noise problems when current transients contain considerable frequency components close to those impedance resonant peaks. Frequency-domain effects will then translate into the time-domain as voltage droops at different stages, potentially causing operational errors or failures [10]. This imposes the need of verifying the impact of decoupling capacitors in both frequency and transient domains.

A. Optimizing Decoupling Capacitors for PDN Applications

From all the above, it is clear the need of optimizing the number and values of the decoupling capacitors to ensure an impedance profile that is lower than a target impedance in the frequency bands of interest. In this way, the decoupling capacitors can aid in handling fluctuations in the load current without magnifying voltage noise at certain frequencies.

Optimizing a PDN under nominal capacitance values is of very high relevance and a crucial step for improving power and signal integrity [9] [11]. Various techniques have been proposed to optimize the number of decoupling capacitors in PDNs. Simulated annealing is used in [12] and [13] to minimize the number of decoupling capacitors while satisfying a target impedance. A noise-driven simulated annealing optimization approach is used in [14] to minimize the number of decoupling capacitors in packages for power integrity. Genetic algorithms and particle swarm optimization techniques are used in [15]-[18] to optimize the value and placement of decoupling capacitors in a PDN. It becomes clear that population-based heuristic search methods have been employed to deal with the large number of local minima typically found in this arena. In contrast, we propose in [5] an optimization approach based on the classical Nelder-Mead method to find the best values of the compensation elements of a VR and the optimal number of decoupling capacitors in a PDN; Section IV provides the details about it.

B. Decoupling Capacitors Variability

As mentioned before, the actual capacitance of the commercially available capacitors used for decoupling can fluctuate significantly from its nominal value. These capacitors may have tolerances in the range from ±20% to ±80% [19]. Furthermore, their capacitance value can vary with changes in bias voltage or operating temperature.

It is clear that optimizing the number of decoupling

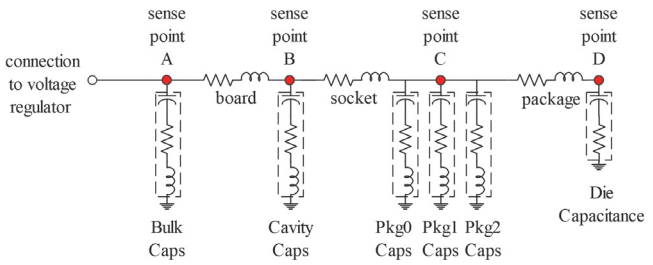


Fig. 1. Lumped equivalent circuit of the power delivery layout schematic of Intel® Xeon® platform. Different sense points can be used to feedback the VR. From [5].

capacitors in a PDN under nominal capacitance values does not allow to anticipate the effects of variability of these key components. Under this scenario, it cannot be assured that the impedance profile will actually be lower than the impedance target after PDN nominal optimization; the same is applicable for other PDN performances, such as transient voltage variations and VR stability.

C. Decoupling Capacitor Types

Several types of decoupling capacitors are typically needed in a PDN. The bulk capacitors are the biggest in the PDN. They act as charge reservoirs to transient currents and are placed on the motherboard at the output filter of the VR to provide large bulk storage [20]. They provide a low impedance at low frequencies, below a few MHz.

Electrolytic capacitors are commonly used to provide the bulk output filter capacitance for the switching regulator on the platform. Aluminum electrolytic capacitors are commonly used on desktops and server platforms. Tantalum polymer capacitors are used on mobile platforms that have height constraints [7].

Cavity capacitors, also known as land side capacitors, are located under the cavity of the package and are effective at middle frequencies, up to several MHz. Package capacitors, or die side capacitors, are effective at higher frequencies, up to several hundred MHz. Despite being subject to significant variation in capacitance as a function of temperature and voltage bias, multi-layer ceramic capacitors (MLCC) are the most common at middle and high frequencies due to their compact size, low loss, and low inductance [7] [20].

In this paper, bulk capacitors are tantalum polymer capacitors with a form factor size code of 2917, the cavity capacitors are MLCC with a size code of 0805, and the package capacitors are also MLCC with size code 0201. The size code defines the capacitor package size in terms of width 0.0X inch and depth 0.0Y inch and is denoted as 0X0Y. These particular capacitors have a maximum manufacturing tolerance of ±20% [21]. Here, the capacitance dependence on temperature and biasing voltages fluctuations is not considered.

III. Representing the PDN Structure and the Voltage Regulator Circuitry

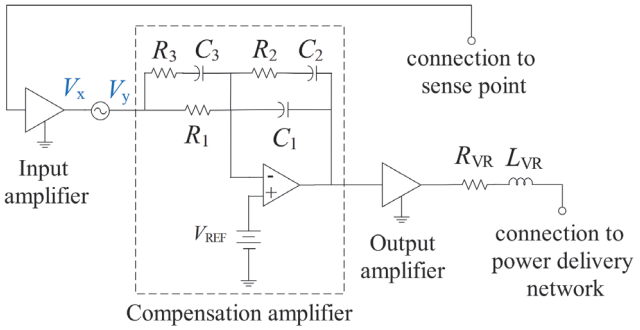


Fig. 2. State average equivalent circuit of a buck voltage regulator (VR). An AC perturbation is inserted to simulate the open-loop Bode plots from V_x/V_y for the VR connected to the PDN. From [5].

A. A PDN Model

We consider the PDN of a CPU power network of an Intel® Xeon® server platform. Its physical layout is described in [22]. The PDN structure can be modelled in a limited frequency band by simple RLC circuits [23], as shown in Fig. 1. This equivalent circuit was obtained from a numerical parameter extraction process to fit laboratory measurements of a CPU power delivery network of an Intel® Xeon® server platform [23] [24] and is considered valid up to a several MHz. For an accurate PDN representation in the GHz range, a physical electromagnetics-based model would be needed to account for the capacitors' placement [17].

B. Voltage Regulator Model

Switched-mode semiconductor devices are preferred for high-efficiency VR to avoid substantial power loss dissipation as heat and prevent a reduction in system reliability due to overheating [25]. The buck converter is one of the most popular switching converters used in voltage regulators [10]. This type of converters is small, easy to incorporate into integrated circuits, and can be controlled with relative ease.

For this work, a state average model of a buck converter is chosen. These models lend themselves nicely for small-signal response to draw Bode or Nyquist plots to assess stability. Since there are no switching components, their simulation is much faster than the corresponding switching model [26]. However, they might inaccurately represent spikes, large ripple, gate charge, and instantaneous switching loss. Nevertheless, state average modelling of voltage regulators is a mainstay of modern control theory, and under the small ripple approximation, they give a good representation of the main regulator characteristics [10].

The equivalent circuit of the converter used in this work is shown in Fig. 2. This circuit consists of a single-ended input amplifier, a compensation amplifier, an output amplifier, and an output filter. The output amplifier is the power stage portion of the regulator. A simple output filter is connected to the power delivery network input. This filter consists of a resistor R_{VR}, an inductor L_{VR}, and the bulk capacitors that are part of the PDN (not shown in Fig. 2). The compensation circuit amplifies the error between the reference voltage and the amplified feedback signal coming from a sense point on the PDN (see Fig. 1).

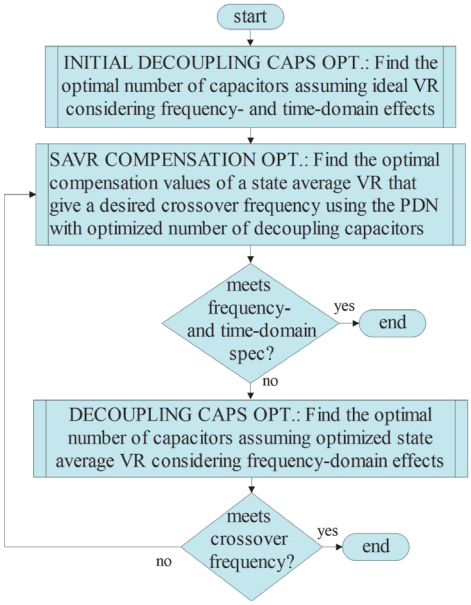


Fig. 3. Flow diagram for the nominal optimization of the number of decoupling capacitors and compensation values in a PDN. From [5].

To obtain the open loop gain Bode plots, the simulation circuit is modified following [27], by adding a small-signal AC perturbation to open the loop. The resulting circuit is shown in Fig. 2. Probing V_x/V_y allows to plot the open loop gain magnitude and phase, which is where the stability criteria are assessed; we selected sense point A (see Fig. 1).

IV. Nominal Optimization of the VR Stability and the Number of Decoupling Capacitors in the PDN

For VR stability it is typically considered sufficient to use the phase margin test, which is a special case of the Nyquist stability theorem. This test measures the difference between 180° and the actual phase when the gain reaches the crossover frequency (at unity gain). The phase margin should be positive to ensure stability, and between 45° to 60° to avoid overshoots and ringing [28].

We initially tried to optimize the number of decoupling capacitors in the PDN to meet all at once a maximum impedance target and a minimum transient voltage droop, along with optimizing the compensation elements of the VR to meet a desired crossover frequency with acceptable phase margin for stability. We were not able to obtain satisfactory results with this approach since the optimization algorithm fails from many different starting points or seeds, which reconfirms the presence of multiple local minima in this high-dimensional space. We found much better results by approaching the problem in a gradual methodology, as illustrated in Fig. 3.

The first step in the methodology is to find the optimal number of decoupling capacitors in the PDN, assuming an ideal VR, that meet a desired maximum impedance in the frequency domain and the target minimum transient voltage droop (see Fig. 3). From the work done in [22], we found that when using an ideal voltage source as the voltage regulator, the bulk capacitors on the PDN do not have a significant effect

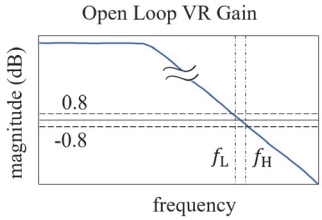


Fig. 4. Open loop VR gain magnitude showing crossover frequency between f_L and f_H.

on the circuit response. This allows us to reduce the number of optimization variables and gives a good starting point for the next optimization steps.

In the second step, we find the optimal values of the compensation components of the state average VR (SAVR) connected to the PDN (see Fig. 2) to comply with the phase margin test. This step uses the optimized number of capacitors from Step 1. After finding the optimal compensation values that meet the required crossover frequency, we check if the entire circuit still meets the maximum impedance and minimum transient voltage (see Fig. 3). If the specifications are not met, we go to a third step, otherwise, we finish.

The third step consists in re-optimizing the decoupling capacitors of the PDN but now using the optimized SAVR. In this step, the bulk capacitors must be included in the optimization variables since we no longer use an ideal VR, instead, we now use a SAVR. After this optimization. we check if the compensation of the VR meets the required crossover frequency; if yes, we finish, otherwise, we go back to Step 2 until the design requirements are met.

In all these steps, we use the efficient Nelder-Mead algorithm [29] available in Matlab to solve the corresponding optimization problem. We use SPICE for circuit simulations in Step 1, and Keysight PathWave Advanced Design System (ADS) for circuit simulations in Steps 2 and 3.

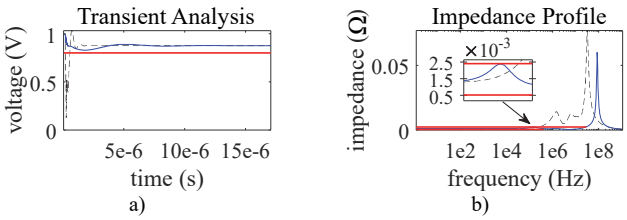
A. Step 1: Optimizing the Number of Capacitors in the PDN Assuming an Ideal VR

We first optimize the number of decoupling capacitors in the PDN shown in Fig. 1 using an ideal voltage source of 1 V as the voltage regulator. The design specifications are a maximum target impedance of 2.4 mΩ for frequencies lower than f_{H1} = 28.8 MHz, a minimum target impedance of 0.52 mΩ for frequencies lower than f_{H2} = 400 kHz and a minimum transient voltage level of 0.8 V. Here we optimize only the number of cavity capacitors ($N_{\text{CavityCap}}$) and the number of capacitors located at the package 0 location (N_{Pkg0Cap}). The bulk capacitors and the capacitors located at package 1 and package 2 locations are kept fixed (see Fig. 1). The optimization variables are $\boldsymbol{x} = [N_{\text{CavityCap}}\ N_{\text{Pkg0Cap}}]^{\text{T}}$.

The optimization problem uses a minimax formulation,

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \max \left\{ \boldsymbol{e}_{\text{Z}}^{\text{T}}(\boldsymbol{x}, f), \boldsymbol{e}_{v}^{\text{T}}(\boldsymbol{x}, t), \boldsymbol{e}_{\text{B}}^{\text{T}}(\boldsymbol{x}) \right\} \quad (1)$$

where the error vector function $\boldsymbol{e}_{\text{Z}}(\boldsymbol{x},f)$ is used to ensure a desired maximum target impedance with f as the simulated frequency, the error vector function $\boldsymbol{e}_{v}(\boldsymbol{x},t)$ is used to ensure a desired maximum transient voltage droop with t as the simulated time, and the error function $\boldsymbol{e}_{\text{B}}(\boldsymbol{x})$.



	Bulk	Cavity	Pkg0	Pkg1	Pkg2	Total
Seed	1	1	1	1	1	5
Optimized	1	63	75	1	1	141

c)

Fig. 5. Results for Step 1 before (dashed line) and after (solid line) nominal optimization: a) impedance profile; b) transient analysis; c) seed values and final values.

The error vector function $\boldsymbol{e}_Z(\boldsymbol{x},f)$ in (1) is defined as

$$\boldsymbol{e}_Z(\boldsymbol{x},f)=\begin{cases}\dfrac{|Z_{11}|(\boldsymbol{x},f)}{2.4\ \text{m}\Omega}-1 & \text{for } f\le f_{H1}\\ 1-\dfrac{|Z_{11}|(\boldsymbol{x},f)}{0.52\ \text{m}\Omega} & \text{for } f\le f_{H2}\end{cases} \tag{2}$$

where $|Z_{11}|(\boldsymbol{x},f)$ is the magnitude of the Z_{11} parameter, which corresponds to the impedance profile of the PDN. Notice that this frequency-domain optimization is performed up to f_{H1} = 28.8 MHz, where the lumped model equivalent circuit is still reliable.

The error vector function $\boldsymbol{e}_v(\boldsymbol{x},t)$ in (1) is defined as

$$\boldsymbol{e}_v(\boldsymbol{x},t)=\begin{cases}1-\dfrac{V_{\text{pulse}}(\boldsymbol{x},t)}{0.8\ \text{V}} & \text{for } 0\le t\le t_{\text{final}}\end{cases} \tag{3}$$

where $V_{\text{pulse}}(\boldsymbol{x},t)$ is the transient voltage response of the power delivery network, and t_{final} is the final simulation time. Details about the load die capacitance and excitation pulse rise time used in our simulations of this CPU PDN of an Intel® Xeon® server platform cannot be disclosed since they are deemed as intellectual property.

The error vector function $\boldsymbol{e}_B(\boldsymbol{x})$ in (1) is defined as

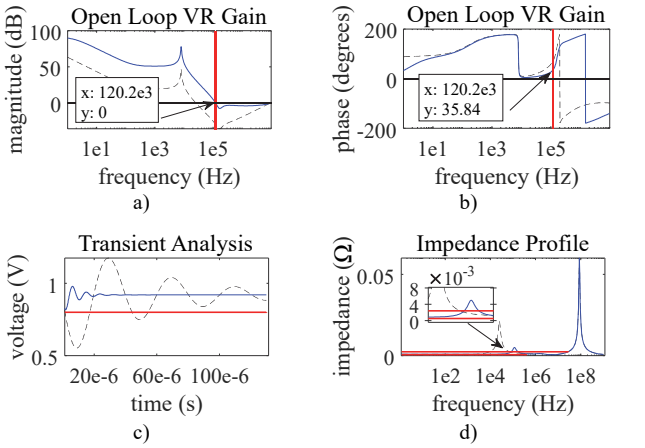
$$\boldsymbol{e}_B(\boldsymbol{x})=\begin{cases}L_B-N_{\text{CavityCap}}\\ L_B-N_{\text{Pkg0Cap}}\\ \dfrac{(N_{\text{CavityCap}}+N_{\text{Pkg0Cap}})}{U_B}-1\end{cases} \tag{4}$$

where L_B is the limiting lower bound for the optimization variables to ensure their values are positive and no less than 1, and U_B is the limiting upper bound for the optimization variables. Notice that U_B allows constraining the optimization problem to fit the available platform area and cost budget. Here we use L_B = 1 and U_B = 140.

B. Step 2: Optimizing the Compensation of a State Average VR for the PDN

We now optimize the compensation parameters of the state average buck regulator to achieve a crossover frequency of 120 KHz with an acceptable phase margin. For this step, the optimized number of capacitors for the PDN found in Step 1 is used.

The optimization variables are now $\boldsymbol{z}$ = [R_2(Ω) R_3(mΩ) C_1(pF) C_2(nF) C_3(nF)]^T (see Fig. 2). To decrease the number of variables R_1 was left at 10 KΩ and L_{VR} at 300 nH.



	R_1	R_2	R_3	C_1	C_2	C_3	L_{VR}
Seed	10	10	100	100	100	100	300
Optimized	10	8.112	21.546	120.544	2.397	92.278	300

e)

Fig. 6. Results for Step 2 before (dashed line) and after (solid line) optimization: a) open loop VR gain magnitude; b) open loop VR gain phase; c) transient analysis; d) impedance profile; e) seed values and final values.

In previous experiments, we found poor results considering the converter's open loop gain phase in the objective function. For this reason, here we only consider the converter's open loop gain magnitude. Consequently, we use the following minimax formulation

$$z^*=\arg\min_z\max\left\{\boldsymbol{e}_B^T(z),\boldsymbol{e}_{VR}^T(z,f)\right\} \tag{5}$$

where the error vector function $\boldsymbol{e}_B(z)$ is used to keep the optimization variables within feasible bounds, and the error vector function, $\boldsymbol{e}_{VR}(z,f)$ is used for the desired open loop frequency response.

The error vector function $\boldsymbol{e}_B(z)$ in (5) is defined as

$$\boldsymbol{e}_B(z)=1-\frac{z}{L_B} \tag{6}$$

where L_B is the limiting lower bound for the optimization variables to ensure their values are positive; an element-wise subtraction is used in (6), with $L_B=1\times10^{-10}$.

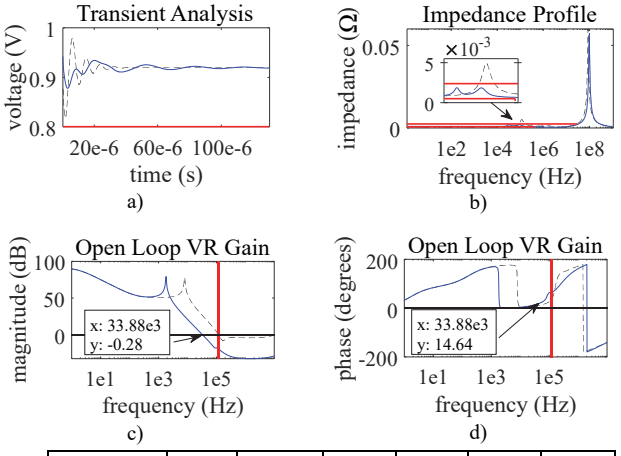
The error vector function $\boldsymbol{e}_{VR}(z,f)$ in (5) is defined as

$$\boldsymbol{e}_{VR}(z,f)=\begin{cases}\dfrac{|A_{OL}(z,f)|}{0.8\ \text{dB}}-1 & \text{for } f\ge f_L\\ \dfrac{|A_{OL}(z,f)|}{-0.8\ \text{dB}}-1 & \text{for } f\le f_H\end{cases} \tag{7}$$

where f_H is the high frequency limit of interest, f_L is the low frequency limit of interest, and $|A_{OL}(z,f)|$ is the open loop VR gain magnitude in dB. Error function in (7) aims at making $|A_{OL}(z,f)|$ as close as possible to 0 dB when the crossover frequency is between f_L and f_H. The effect of this formulation is illustrated in Fig. 4. Here we use f_L = 118 KHz and f_H = 122 KHz.

C. Step 3: Optimizing the Number of Capacitors in the PDN using a State Average Buck VR

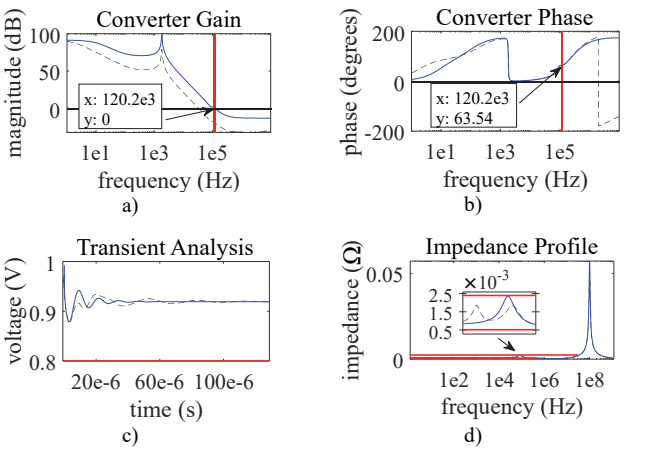
For this step, we solve again the optimization problem (1)



	Bulk	Cavity	Pkg0	Pkg1	Pkg2	Total
Seed	1	63	75	1	1	141
Optimized	53	202	430	1	1	687

e)

Fig. 7. Results for Step 3 before (dashed line) and after (solid line) optimization: a) transient analysis; b) impedance profile; c) open loop VR gain magnitude; d) open loop VR gain phase; e) seed values and final values.



	R_1	R_2	R_3	C_1	C_2	C_3	L_{VR}
Seed	10	8.112	21.546	120.544	2.397	92.278	300
Optimized	10	9.827	22.374	131.170	0.340	149.765	300

e)

Fig. 8. Results for Step 4 before (dashed line) and after (solid line) optimization: a) open loop VR gain magnitude; b) open loop VR gain phase; c) transient analysis; d) impedance profile; e) seed values and final values.

with some modifications. By obtaining a stable compensation in the VR we do not need to consider the error function (3), which helps reducing simulation time significantly; we now use $U_B = 700$ and the error function (4) is modified to consider the bulk capacitors,

$$\boldsymbol{e}_B(\boldsymbol{x}) = \begin{cases} L_B - N_{\text{BulkCap}} \\ L_B - N_{\text{CavityCap}} \\ L_B - N_{\text{Pkg0Cap}} \\ \dfrac{(N_{\text{BulkCap}} + N_{\text{CavityCap}} + N_{\text{Pkg0Cap}})}{U_B} - 1 \end{cases} \tag{8}$$

D. Nominal Optimization Results

Figure 5 shows the results for Step 1; it is seen that the impedance profile and voltage droop specifications are met after optimization. Fig. 6 shows the results for Step 2: the crossover frequency is achieved with a phase margin of 35.84°. When using the SAVR with the PDN circuit, the transient voltage droop and the impedance profile are affected.

After the optimization in this step, the voltage droop meets the design specifications, however, the impedance profile has a large impedance peak of around 5 mΩ. Fig. 7 shows the results for Step 3; the voltage droop and impedance profile meet the specifications, however, the VR compensation's crossover frequency moved to a lower frequency (33.88 KHz).

Following the proposed methodology (see Fig. 3), we now repeat the procedure in Step 2. Fig. 8 shows the results for this last step. We now have the desired crossover frequency with a phase margin of 63.54°; the voltage droop and the impedance profile also meet the design specifications.

We obtain good results by following our proposed methodology. The desired crossover frequency is achieved with a good phase margin to ensure stability, as confirmed in the decreased ringing in the transient analysis. The transient voltage noise meets the design specifications, and the impedance profile also meets the maximum target impedance at all frequencies.

V. Formulation of the Statistical Analysis and Yield Estimation of a PDN

Designing a robust PDN involves accounting for uncontrollable variations, such as the capacitance value fluctuations of the decoupling capacitors due to their tolerance associated to their manufacturing process. A robust design aims at selecting product design parameter values so that uncontrollable variations result in minimal deviation from the expected performance [30]. Ideally, a robust PDN implies designing for high yield and reliability.

For yield analysis, circuit parameter values are randomly varied around a nominal reference design according to their manufacturing tolerances and their probability distribution functions. The corresponding simulated circuit responses, also referred as outcomes, are compared to specified performance criteria. The ratio of the number of circuits that pass the performance specifications to the total number of simulated circuits can be used to approximate the yield around the nominal reference design [30]-[33].

Yield estimation is typically based on the Monte Carlo method. The accuracy of this method for yield estimation is independent of the number of statistical variables [33] as long as the outcomes or system responses available have statistical significance. Typically, many simulations of the complete circuit (outcomes), are needed to achieve statistically significant results, which makes Monte Carlo in general a computationally intensive method for yield prediction.

A. Responses of Interest, Error Functions, and Objectives

Let $\boldsymbol{\varphi} \in \Re^n$ represent the vector of n statistical design parameters of the PDN, whose responses of interest are in

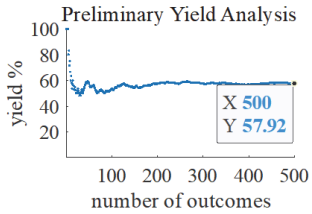


Fig. 9. Preliminary yield analysis for the PDN impedance profile, with only 500 outcomes, to estimate expected yield.

vectors $\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{\varphi},f)$, $\boldsymbol{R}_{\mathrm{Z}}(\boldsymbol{\varphi},f)$, and $\boldsymbol{R}_{v}(\boldsymbol{\varphi},t)$. In our formulation, $\boldsymbol{R}_{\mathrm{VR}}(\boldsymbol{\varphi},f)$ contains the VR stability response, i. e., the frequency-domain open loop VR gain magnitude and phase, $\boldsymbol{R}_{\mathrm{Z}}(\boldsymbol{\varphi},f)$ contains the PDN impedance profile response, i. e., the magnitude of Z_{11} at the frequency band of interest; and finally, $\boldsymbol{R}_{v}(\boldsymbol{\varphi},t)$ contains the PDN voltage droop response, i. e., the amplitude of the transient voltage of the PDN.

Error vector functions are used to measure whether the random outcomes satisfy or violate the performance specifications. Error vector function $\boldsymbol{e}_{\mathrm{VR}}(\boldsymbol{\varphi},f)$ is used for the open loop frequency response of the VR,

$$\boldsymbol{e}_{\mathrm{VR}}(\boldsymbol{\varphi},f)=\begin{cases}\dfrac{\left|A_{\mathrm{OL}}(\boldsymbol{\varphi},f)\right|}{0.8\ \mathrm{dB}}-1 & \text{for } f\geq f_{\mathrm{L}}\\ \dfrac{\left|A_{\mathrm{OL}}(\boldsymbol{\varphi},f)\right|}{-0.8\ \mathrm{dB}}-1 & \text{for } f\leq f_{\mathrm{H}}\end{cases} \tag{9}$$

Error vector function $\boldsymbol{e}_{\mathrm{Z}}(\boldsymbol{\varphi},f)$ is used for the maximum target impedance,

$$\boldsymbol{e}_{\mathrm{Z}}(\boldsymbol{\varphi},f)=\begin{cases}\dfrac{\left|Z_{11}\right|(\boldsymbol{\varphi},f)}{2.4\ \mathrm{m\Omega}}-1 & \text{for } f\leq f_{\mathrm{H1}}\\ 1-\dfrac{\left|Z_{11}\right|(\boldsymbol{\varphi},f)}{0.52\ \mathrm{m\Omega}} & \text{for } f\leq f_{\mathrm{H2}}\end{cases} \tag{10}$$

Error vector function $\boldsymbol{e}_{v}(\boldsymbol{\varphi},t)$ is used for the minimum transient voltage droop,

$$\boldsymbol{e}_{v}(\boldsymbol{\varphi},t)=\left\{1-\frac{V_{\mathrm{pulse}}(\boldsymbol{\varphi},t)}{0.8\ \mathrm{V}}\quad \text{for } 0\leq t\leq t_{\mathrm{final}}\right. \tag{11}$$

The corresponding objective functions to obtain the yield for the three performance domains are

$$U_{\mathrm{VR}}(\boldsymbol{\varphi})=\max\left\{\boldsymbol{e}_{\mathrm{VR}}^{\mathrm{T}}(\boldsymbol{\varphi},f)\right\} \tag{12}$$

$$U_{\mathrm{Z}}(\boldsymbol{\varphi})=\max\left\{\boldsymbol{e}_{\mathrm{Z}}^{\mathrm{T}}(\boldsymbol{\varphi},f)\right\} \tag{13}$$

$$U_{v}(\boldsymbol{\varphi})=\max\left\{\boldsymbol{e}_{v}^{\mathrm{T}}(\boldsymbol{\varphi},t)\right\} \tag{14}$$

B. Statistical Analysis and Yield Estimation

For the statistical yield analysis, we consider that the element values in the k-th vector of decoupling capacitors $\boldsymbol{\varphi}^{k}$ are spread around their nominal values in $\boldsymbol{\varphi}$ according to their individual probability distribution functions and tolerances. The k-th design parameters can be presented as

$$\boldsymbol{\varphi}^{k}=\boldsymbol{\varphi}+\Delta\boldsymbol{\varphi}^{k},\ k=1,2,\ldots,N \tag{15}$$

where N is the number of simulations or outcomes and $\Delta\boldsymbol{\varphi}$ is a k-th random perturbation.

We associate to the k-th outcome an acceptance index for each performance domain, defined by

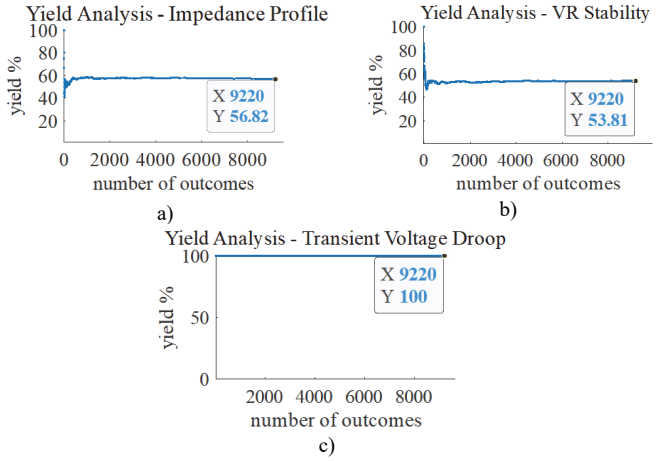


Fig. 10. Yield analysis with 9,220 outcomes at the nominally optimized PDN design: a) impedance profile; b) VR stability; c) transient voltage droop.

$$I_{\mathrm{VR}}(\boldsymbol{\varphi}^{k})=\begin{cases}1 & \text{if } U_{\mathrm{VR}}(\boldsymbol{\varphi}^{k})\leq 0\\ 0 & \text{if } U_{\mathrm{VR}}(\boldsymbol{\varphi}^{k})>0\end{cases} \tag{16}$$

$$I_{\mathrm{Z}}(\boldsymbol{\varphi}^{k})=\begin{cases}1 & \text{if } U_{\mathrm{Z}}(\boldsymbol{\varphi}^{k})\leq 0\\ 0 & \text{if } U_{\mathrm{Z}}(\boldsymbol{\varphi}^{k})>0\end{cases} \tag{17}$$

$$I_{v}(\boldsymbol{\varphi}^{k})=\begin{cases}1 & \text{if } U_{v}(\boldsymbol{\varphi}^{k})\leq 0\\ 0 & \text{if } U_{v}(\boldsymbol{\varphi}^{k})>0\end{cases} \tag{18}$$

If N is sufficiently large for statistical significance, following [31] we can approximate the yield Y at the nominal design $\boldsymbol{\varphi}$ for each performance domain by using

$$Y_{\mathrm{VR}}(\boldsymbol{\varphi})\approx\frac{1}{N}\sum_{k=1}^{N}I_{\mathrm{VR}}(\boldsymbol{\varphi}^{k}) \tag{19}$$

$$Y_{\mathrm{Z}}(\boldsymbol{\varphi})\approx\frac{1}{N}\sum_{k=1}^{N}I_{\mathrm{Z}}(\boldsymbol{\varphi}^{k}) \tag{20}$$

$$Y_{v}(\boldsymbol{\varphi})\approx\frac{1}{N}\sum_{k=1}^{N}I_{v}(\boldsymbol{\varphi}^{k}) \tag{21}$$

C. Number of Simulations for Reliable Yield Estimation

To perform a reliable Monte Carlo yield estimation, it is necessary to approximate how many simulations or outcomes are enough to obtain a reasonably accurate yield estimation. As the number of outcomes increases, the estimated yield approaches the true design yield [33]. However, an excessive number of simulations renders the process unnecessarily long.

To calculate the number of outcomes we follow [30]. This calculation assumes that all statistical system parameters follow a normal or Gaussian probability distribution function. The number of outcomes N needed to have a certainty c when calculating the yield can be obtained from

$$N=\mathrm{round}\left\{\frac{\left[t(c)\right]^{2}}{\varepsilon^{2}}(Y)(1-Y)\right\} \tag{22}$$

where Y is the expected yield ($0<Y<1$), ε is the error in the yield estimation, t is a statistical value with a probability c to happen (c is the area under the bell curve between $-t$ and $+t$).

TABLE I
ESTIMATING THE NUMBER OF MONTE CARLO OUTCOMES

Parameter	Value
confidence	95%
$t(c)$	1.96 (Z-score)
ε	0.01
Y	0.60
number of outcomes	9220

For sample sizes larger than 30, $t(c)$ is the Z-score value for the required confidence level [34].

VI. Evaluating the Impact of Decoupling Capacitors Variability on the PDN Performance

Here, yield estimation is done for the impedance profile and transient voltage droop of the PDN in [5], as well as for the stability of the voltage regulator used in that PDN. We use (9)-(21) as formulated in Section V to evaluate the impact of the variability of the decoupling capacitors on the VR stability, PDN impedance profile, and minimum transient voltage droop.

The statistical parameters are now in vector $\boldsymbol{w}$, which contains the capacitances of all the decoupling capacitors, $\boldsymbol{w} = [C_{Bulk}(\mu F)\ C_{Cavity}(\mu F)\ C_{Pkg0}(\mu F)\ C_{Pkg1}(nF)\ C_{Pkg2}(nF)]^T$.

To evaluate (22), we need in advance the expected yield. Fig. 9 shows a preliminary Monte Carlo yield estimation with only five hundred outcomes, using a 20% tolerance in the capacitance of the decoupling capacitors of the PDN shown in Fig. 1, and using independent Gaussian probability distribution functions for all of them. We can see that the impedance profile yield starts stabilizing at around 60%. Using this value as the expected yield in (22), we calculate the number of required random outcomes for a 95% confidence and 1% error. The parameter values and results for these calculations are shown in Table I. We need 9,220 random outcomes to get a reliable yield estimation with 95% confidence and 1% error.

For the yield simulations we exploit Keysight ADS statistical capabilities to save simulation time and memory, while still allowing automated data processing through Matlab.

We now use 9,220 random outcomes for yield estimations of the three performance domains of interest: impedance profile, VR stability, and transient voltage droop. Fig. 10a shows the yield for the impedance profile; it stabilizes at around 57%. The yield for the stability of the voltage regulator is shown in Fig. 10b, showing a yield of around 53%. Finally, a 100% yield is obtained for the transient voltage droop, as confirmed in Fig. 10c, indicating that the minimum transient voltage droop is not sensitive enough to fluctuations in the capacitance of the decoupling capacitors. The transient voltage waveform does show different levels of voltage ripple for different values in these capacitances, however, the minimum voltage droop maintains a level above the specified performance, as confirmed in Fig. 11c.

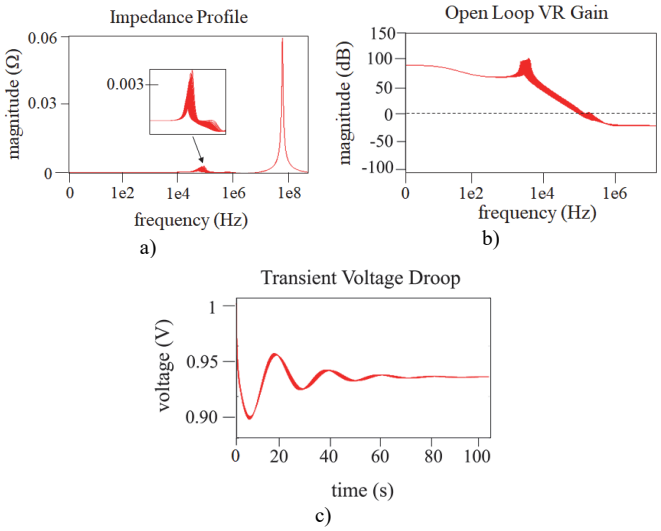


Fig. 11. PDN responses of interest for the 500 random outcomes around the nominally optimized PDN design using ±20% variation in decoupling capacitance values: a) impedance profile; b) open loop VR gain; and c) transient voltage droop.

VII. Yield Optimization of the PDN

We now optimize the yield of the nominally optimized PDN obtained in Section IV, subject to large decoupling capacitor tolerances, considering simultaneously the impedance profile and the VR stability design specifications. In Section VI, we found that the minimum transient voltage droop is not sensitive enough to fluctuations in the capacitance of the decoupling capacitors, so we do not consider this in the yield optimization objective function to speed up the process. However, we do verify the yield of the transient voltage droop with the optimal yield component values.

A. Yield Optimization Formulation

We use the formulation in Section V to estimate the yield of the VR stability and impedance profile at each objective function evaluation when the PDN is subject to variability in the capacitance of the decoupling capacitors. During yield optimization, each of the decoupling capacitors of the same type have the same nominal value perturbed by different random fluctuations that are statistically independent from each other, since they use independent Gaussian probability distribution functions at each simulated outcome, for the 9,220 outcomes calculated at each objective function evaluation.

The design parameters are now in vector $\boldsymbol{s} \in \Re^{10}$, which contains the values of the VR compensation design parameters, $\boldsymbol{z} \in \Re^5$, as defined in Section IV.B, as well as the values of the capacitance of the decoupling capacitors, $\boldsymbol{w} \in \Re^5$, as defined in Section VI; $\boldsymbol{s}^T = [\boldsymbol{z}^T\ \boldsymbol{w}^T]$.

The optimization problem considers simultaneously the yield of the VR stability and the yield of the impedance profile with a minimax formulation,

$$\boldsymbol{s}^* = \arg\min_{\boldsymbol{s}} \max \left\{ e_{YZ}(\boldsymbol{s}), e_{YVR}(\boldsymbol{s}), \boldsymbol{e}_{YB}^T(\boldsymbol{s}) \right\} \quad (23)$$

where $\boldsymbol{s}^*$ is the optimal yield design, $e_{YZ}(\boldsymbol{s})$ and $e_{YVR}(\boldsymbol{s})$ are the

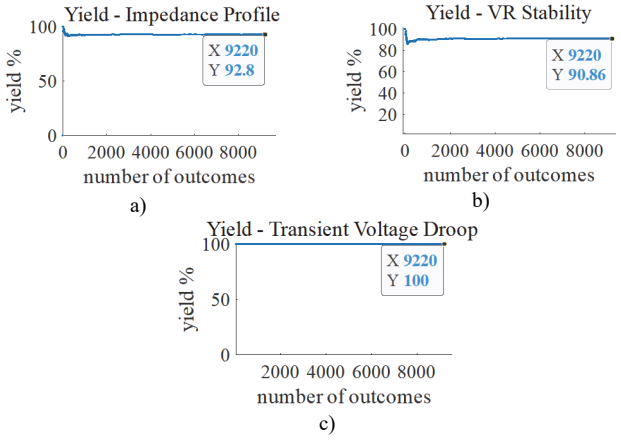


Fig. 12. Yield analysis with 9,220 outcomes at the PDN optimal yield design: a) impedance profile; b) VR stability; c) transient voltage droop.

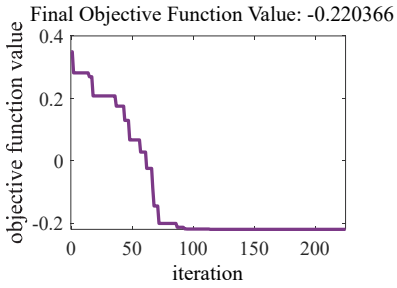


Fig. 13. Evolution of the objective function used in (23) during yield optimization.

error scalar functions used to ensure the impedance profile yield and the VR stability yield are above their respective minimum requirements; and $\boldsymbol{e}_{\mathrm{YB}}(\boldsymbol{s})$ is the error vector function used to keep the optimization variables within certain bounds.

Error scalar function $e_{\mathrm{YZ}}(\boldsymbol{s})$ is defined as

$$e_{\mathrm{YZ}}(\boldsymbol{s}) = 1 - \frac{Y_{\mathrm{Z}}(\boldsymbol{s})}{Y_{\mathrm{Zspec}}} \tag{24}$$

where Y_{Zspec} is the required yield for the impedance profile. Here we use $Y_{\mathrm{Zspec}} = 75\%$.

Error scalar function $e_{\mathrm{YVR}}(\boldsymbol{s})$ is defined as

$$e_{\mathrm{YVR}}(\boldsymbol{s}) = 1 - \frac{Y_{\mathrm{VR}}(\boldsymbol{s})}{Y_{\mathrm{VRspec}}} \tag{25}$$

where Y_{VRspec} is the required yield for the VR stability. Here we use $Y_{\mathrm{VRspec}} = 75\%$.

Error vector function $\boldsymbol{e}_{\mathrm{YB}}(\boldsymbol{s})$ is defined as

$$\boldsymbol{e}_{\mathrm{YB}}(\boldsymbol{s}) = \begin{cases} 1 - \dfrac{\boldsymbol{s}}{\boldsymbol{L}_{\mathrm{B}}} \\ \dfrac{\boldsymbol{s}(6:10)}{\boldsymbol{U}_{\mathrm{B}}} - 1 \end{cases} \tag{26}$$

where $\boldsymbol{L}_{\mathrm{B}} \in \Re^{10}$ is a vector of lower bounds; it contains an arbitrarily small number to ensure the VR compensation elements remain positive (1×10^{-10}), as well as the minimum commercial values of the capacitances. As lower bounds we use 15 µF for the bulk capacitance, 1 pF for the cavity capacitance, and 0.1 pF for the package capacitances. $\boldsymbol{U}_{\mathrm{B}} \in \Re^{5}$ is a vector of upper bounds; it only contains the maximum commercial values of the capacitances. As upper bounds we use 100 µF for the cavity capacitance, 4.7 µF for the package capacitances, and 940 µF for the bulk capacitors (up to two 470-µF maximum commercial value). Notice that operations in (26) are element-wise.

TABLE II
DESIGN PARAMETERS VALUES BEFORE AND AFTER YIELD OPTIMIZATION

Parameter	Initial Value	Final Value	Units
Bulk capacitance	418.71	732.85	µF
Cavity capacitance	12.7	17.62	µF
Pkg0 capacitance	1.14	0.9348	µF
Pkg1 capacitance	402.68	344.94	nF
Pkg2 capacitance	6.34	2.08	µF
R_2	9.827	9.5402	Ω
R_3	22.374	22.1182	mΩ
C_1	131.17	51.3604	pF
C_2	0.34	0.4096	nF
C_3	149.765	173.7384	nF

We use again Matlab's Nelder-Mead algorithm [29] to solve the corresponding optimization problem, and Keysight ADS for the yield evaluations.

B. *Yield Optimization Results*

The design parameter values before and after yield optimization are shown in Table II. Fig. 12 shows the yield calculated with 9,220 random outcomes around the optimal yield design found, $\boldsymbol{s}^*$, for each PDN performance domain. It is seen that we achieve a 92.8% yield for the PDN impedance profile (Fig. 12a) and a yield of 90.86 % for the VR stability (Fig. 12b). Both yields exceed our requirements and show a significant improvement, since they were 56.82% and 53.81%, respectively, before yield optimization (see Section VI). Fig. 12c verifies the yield of the transient voltage droop is still 100% after the optimization. Fig. 13 shows the evolution of the objective function used in (23) during yield optimization.

VIII. Computational Cost of the Proposed PDN Yield Estimation and Optimization

Here we report the computational cost for the proposed PDN nominal optimization, for yield estimation, and for yield optimization. Using a low-cost conventional laptop (Intel Core i7-4700MQ at 2.4 GHz and 16 GB RAM), the average time to obtain each of the simulated responses defined in Section V are reported in Table III, including the yield estimation with 9,220 outcomes. It is seen that the most expensive simulation corresponds to the transient simulation in ADS, as expected, consuming 26.2 seconds. All the other responses are much faster to calculate. The 9,220 outcomes used for yield estimation directly within ADS consumes around two minutes for the impedance profile as well as for the VR stability, while

TABLE III
MODELS COMPUTATIONAL COST

response	average simulation time (s)		
	SPICE	ADS	ADS (yield estimation)
$\boldsymbol{R}_v(\boldsymbol{\varphi},t)$	4.31	26.20	-
$\boldsymbol{R}_Z(\boldsymbol{\varphi},f)$	0.14	1.28	-
$\boldsymbol{R}_{VR}(\boldsymbol{\varphi},f)$	-	1.5	-
$Y_v(\boldsymbol{\varphi})$	-	-	6,855.41
$Y_Z(\boldsymbol{\varphi})$	-	-	130.31
$Y_{VR}(\boldsymbol{\varphi})$	-	-	109.40

TABLE IV
OPTIMIZATION COMPUTATIONAL COST

	nominal optimization				yield optimization
	Step 1 (SPICE)	Step 2 (ADS)	Step 3 (ADS)	Step 4 (ADS)	
responses used in objective function	$\boldsymbol{R}_v$, $\boldsymbol{R}_Z$	$\boldsymbol{R}_{VR}$	$\boldsymbol{R}_Z$	$\boldsymbol{R}_{VR}$	Y_Z, Y_{VR}
objective function evaluations	159	267	344	198	518
Nelder-Mead iterations	81	141	150	103	226
total optimization time (hours)	0.20	0.11	0.12	0.08	34.49

the yield estimation for the transient response consumes less than 2 hours.

Table IV summarizes the number of iterations and objective function evaluations as well as the total optimization time consumed by each Nelder-Mead optimization stage. The responses used in the objective function of each stage are also indicated in Table IV, in consistency with our mathematical formulation described in Sections IV.A-C and VII. It is seen that the proposed nominal optimization methodology consumes around half an hour. It is also seen that even though we are using 9,220 random outcomes at each yield estimation, the entire yield optimization process takes around one and a half days using this low-performance laptop, by virtue of not incorporating the transient yield estimation during yield optimization, as justified in Section VII, although we verify keeping a 100% yield for the voltage transient response at the optimal yield solution found (see Section VII.C).

IX. Conclusion

A frequency- and time-domain yield optimization approach was proposed for power delivery networks considering the impact of large tolerances in the decoupling capacitors. First, we minimized the number of parallel decoupling capacitors in the PDN and optimized the compensation parameter values of a buck converter VR, considering simultaneously the frequency- and time-domain performances. Next, we performed a statistical analysis, yield estimation, and yield optimization of the nominally optimized PDN subject to large decoupling capacitor tolerances. The numerical results obtained from our proposed optimization approach demonstrate its effectiveness to assess and improve the PDN performance and reliability, confirmed by a significantly increased overall yield.

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