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Optimizing a Buck Voltage Regulator and the Number of Decoupling Capacitors for a PDN Application

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***Abstract* — An optimization methodology to determine the best values of the compensation elements of a buck voltage regulator (VR) as well as the optimal number of decoupling capacitors in a power delivery network (PDN) application is proposed. A state average equivalent circuit model of the buck converter is employed. The proposed optimization methodology gradually finds the best compensation parameter values of a buck converter VR to meet some stability criteria in a PDN application. Additionally, the number of parallel decoupling capacitors in the PDN is minimized to simultaneously meet a frequency-domain impedance profile specification and a time-domain voltage droop requirement.**

***Keywords* — impedance profile, noise control, power delivery network, power integrity, voltage droop, voltage regulator.**

I. Introduction

A power delivery network (PDN) consists of all the devices and interconnects that distribute the electrical power and return the electrical current throughout a board of an electronic system. Voltage regulators (VR) distribute controlled voltage to the various active devices, by providing a steady power supply at a desired DC voltage level with an acceptable noise level or ripple.

These VR transfer energy from one place to another, ideally with the highest possible efficiency [1]. Substantial power loss dissipated as heat by the VR elements may lead to reduction in system reliability and could require a large and expensive cooling system, which is critical in cloud computing servers [2].

Switched-mode semiconductor devices are preferred for high-efficiency VR, since they are smaller and easier to incorporate into integrated circuits. The buck converter is one of the most popular switching converters [3]. This type of voltage regulator is simple, small, and efficient; it can also be controlled with relative ease.

Compensation feedback loops [1] in the VR allows keeping a constant voltage in spite of changes in the input voltage or in the effective load resistance. However, undesired output voltage ringing can occur if this feedback loop becomes unstable. Therefore, the VR compensation must be designed to ensure stability. The phase margin test is a special case of the Nyquist stability theorem and is typically considered to be sufficient for designing most voltage regulators. This test measures the difference between 180° and the actual phase when the gain reaches unity gain (at the crossover frequency). For stability, the phase margin should be positive, and to avoid overshoots and ringing in the transient response, it should be between 45° to 60° [4], which is typically used in industry.

When circuits start operating, the changing current flowing through the PDN produces voltage fluctuations, creating voltage noise on the signal pads of the silicon die. This means that the transmitted voltage signal level depends on the frequency spectrum of the current drawn by the chips [5]. Unsuccessful noise control on the PDN can cause the amplitude of the eye diagram in the vertical direction to collapse due to the voltage noise; additionally, the time signal crossing a reference will spread out in the horizontal direction, causing jitter, and further reducing the eye opening. This may lead to functional failures in the computer platform, since internal core circuits suffer setups and hold-time errors. The impedance profile then becomes a figure of merit of the acceptability of the PDN design, since by knowing the worst-case current drawn by the chips and the required voltage tolerance, one can determine an impedance target that the PDN should have to keep the voltage noise at an acceptable level for all chips.

In this paper, an optimization-based methodology is proposed to determine the best compensation parameter values of a buck converter VR, aiming at a desired crossover frequency and phase margin to meet some stability criteria in a PDN application. Additionally, the number of parallel decoupling capacitors in the PDN is also minimized to meet the impedance profile and voltage droop specifications, considering simultaneously frequency- and time-domain performances.

II. Representing the PDN Structure and the Voltage Regulator Circuitry

A. PDN Model

We consider the PDN of a CPU power network of an Intel® Xeon® server platform. Its platform layout is described in [6]. The PDN structure can be modelled in a limited frequency band by simple lumped RLC circuits [7]. Fig. 1 shows the equivalent lumped model extracted from the PDN layout [7], [8].

B. Voltage Regulator Model

For this work, a state average model of a buck converter is chosen. These models lend themselves nicely for small-signal response to draw Bode or Nyquist plots to assess stability. Since there are no switching components, their simulation is much faster than the corresponding switching model [9]. However, it is not possible to see large ripple, spikes, gate charge, and instantaneous switching loss. Nevertheless, state average modelling of voltage regulators is a mainstay of modern control

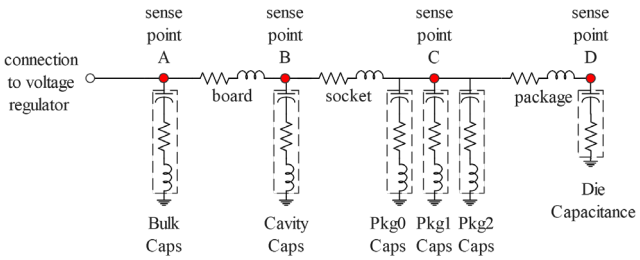


Fig. 1. Lumped equivalent circuit of the power delivery layout schematic of Intel® Xeon® platform. Different sense points can be used to feedback the VR.

theory, and under the small ripple approximation, they give a good representation of the main regulator characteristics [3].

The equivalent circuit of the converter used in this work is shown in Fig. 2. The circuit consists of a single-ended input amplifier, a compensation amplifier, an output amplifier, and an output filter. The output amplifier is the power stage portion of the regulator. A simple output filter is connected to the power delivery network input. This filter consists of a resistor R_{VR}, an inductor L_{VR}, and the bulk capacitors that are part of the PDN (not shown in Fig. 2). The compensation circuit amplifies the error between the reference voltage and the amplified feedback signal coming from a sense point on the PDN.

To obtain the open loop gain Bode plots, the simulation circuit is modified following [10], by adding a small-signal AC perturbation to open the loop. The resulting circuit is shown in Fig. 2. Probing V_x/V_y allows to plot the open loop gain magnitude and phase, which is where the stability criteria are assessed; we selected sense point A (see Fig. 1).

III. Proposed Methodology for Optimizing the Buck VR and the Decoupling Capacitors

We initially tried to optimize the decoupling capacitors in the PDN to meet a maximum impedance target and a minimum transient voltage, along with optimizing the compensation elements of the VR to meet a desired crossover frequency with acceptable phase margin for stability. We were not able to obtain satisfactory results with this approach, since the optimization algorithm fails from many different starting points or seeds. We found much better results by approaching the problem in a gradual methodology, as illustrated in Fig. 3.

The first step is to find the optimal number of decoupling capacitors in the PDN, assuming an ideal VR, that meet a desired maximum impedance in the frequency domain and the

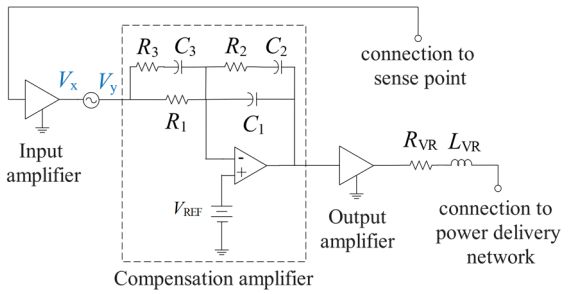


Fig. 2. State average equivalent circuit of a buck voltage regulator (VR). An AC perturbation is inserted to simulate the open-loop Bode plots from V_x/V_y for the VR connected to the PDN.

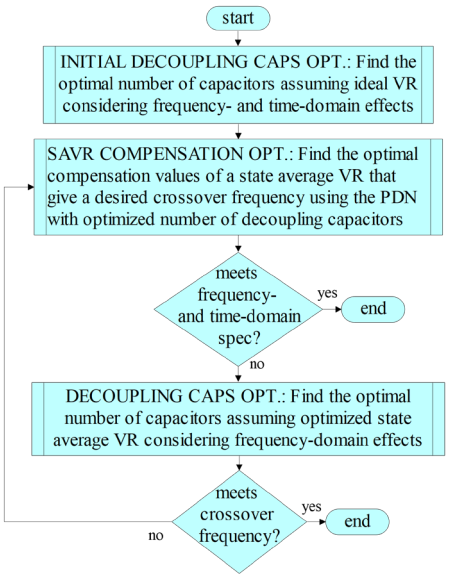


Fig. 3. Flow diagram of proposed methodology.

target minimum transient voltage (see Fig. 3). From the work done in [6] we found that when using an ideal voltage source as the voltage regulator, the bulk capacitors on the PDN do not have a significant effect on the circuit response. This allows us to reduce the number of optimization variables and gives a good starting point for the next optimization steps.

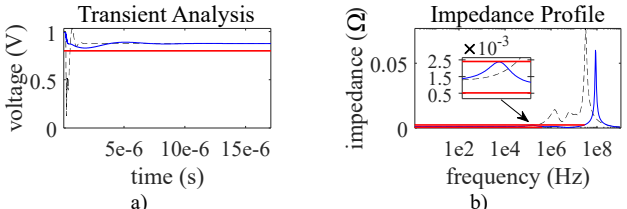
The second step consists of finding the optimal values of the compensation components of the state average VR (SAVR) connected to the PDN (see Fig. 2) with the optimized number of capacitors from the previous step. After finding the optimal compensation values that meets the required crossover frequency, we check if the entire circuit still meets the maximum impedance and minimum transient voltage (see Fig. 3). If the specifications are not met, we go to a third step, otherwise, we finish.

In the third step we re-optimize the decoupling capacitors of the PDN but now using the optimized SAVR. In this step the bulk capacitors must be included in the optimization variables since we use a state average VR. After this optimization we check if the compensation of the VR meets the required crossover frequency; if yes, we finish, otherwise, we go back to Step 2 until the design requirements are met.

In all these steps we use the Nelder-Mead algorithm available in Matlab to solve the corresponding optimization problem. We use SPICE for the circuit simulations in Step 1, and Keysight ADS for the circuit simulations in Steps 2 and 3.

A. Step 1: Optimizing the Number of Capacitors in the PDN Assuming an Ideal VR

We first optimize the number of decoupling capacitors in the PDN shown in Fig. 1 using an ideal voltage source of 1 V as the voltage regulator. The design specifications are a maximum target impedance of 2.4 mΩ for frequencies lower than $f_{H1} = 28.8$ MHz, a minimum target impedance of 0.52 mΩ for frequencies lower than $f_{H2} = 400$ kHz, and a minimum transient voltage level of 0.8 V. Here we optimize only the number of cavity capacitors ($N_{\mathrm{CavityCap}}$) and the number of



	Bulk	Cavity	Pkg0	Pkg1	Pkg2	Total
Seed	1	1	1	1	1	5
Optimized	1	63	75	1	1	141

c)

Fig. 4. Results for Step 1 before (dashed line) and after (solid line) optimization: a) impedance profile; b) transient analysis; c) seed values and final values.

capacitors located at the package 0 location (N_{Pkg0Cap}). The bulk capacitors and the capacitors located at package 1 and package 2 locations are left fixed (see Fig. 1). The optimization variables are $\boldsymbol{x} = [N_{\text{CavityCap}} \quad N_{\text{Pkg0Cap}}]^{\text{T}}$.

The optimization problem uses a minimax formulation,

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \max\{\boldsymbol{e}_{\text{f}}^{\text{T}}(\boldsymbol{x}, f), \boldsymbol{e}_{\text{t}}^{\text{T}}(\boldsymbol{x}, t), \boldsymbol{e}_{\text{B}}^{\text{T}}(\boldsymbol{x})\} \tag{1}$$

where the error vector function $\boldsymbol{e}_{\text{f}}(\boldsymbol{x}, f)$ is used to ensure a desired maximum target impedance, where f is the simulated frequency, the error vector function $\boldsymbol{e}_{\text{t}}(\boldsymbol{x}, t)$ is used to ensure a desired maximum transient voltage droop, where t is the simulated time, and the error function $\boldsymbol{e}_{\text{B}}(\boldsymbol{x})$ is used to keep the optimization variables within feasible bounds.

The error vector function $\boldsymbol{e}_{\text{f}}(\boldsymbol{x}, f)$ in (1) is defined as

$$\boldsymbol{e}_{\text{f}} = \begin{cases} \frac{|Z_{11}|(\boldsymbol{x},f)}{2.4\ \text{m}\Omega} - 1 & \text{for } f \le f_{\text{H1}} \\ 1 - \frac{|Z_{11}|(\boldsymbol{x},f)}{0.52\ \text{m}\Omega} & \text{for } f \le f_{\text{H2}} \end{cases} \tag{2}$$

where $|Z_{11}|(\boldsymbol{x}, f)$ is the magnitude of the Z_{11} parameter, which corresponds to the impedance profile of the PDN.

The error vector function $\boldsymbol{e}_{\text{t}}(\boldsymbol{x}, t)$ in (1) is defined as

$$\boldsymbol{e}_{\text{t}} = \left\{1 - \frac{V_{\text{pulse}}(\boldsymbol{x},t)}{0.8\ \text{V}} \quad \text{for } 0 \le t \le t_{\text{final}} \right. \tag{3}$$

where $V_{\text{pulse}}(\boldsymbol{x}, t)$ is the transient voltage response of the power delivery network, and t_{final} is the final simulation time.

The error vector function $\boldsymbol{e}_{\text{B}}(\boldsymbol{x})$ in (1) is defined as

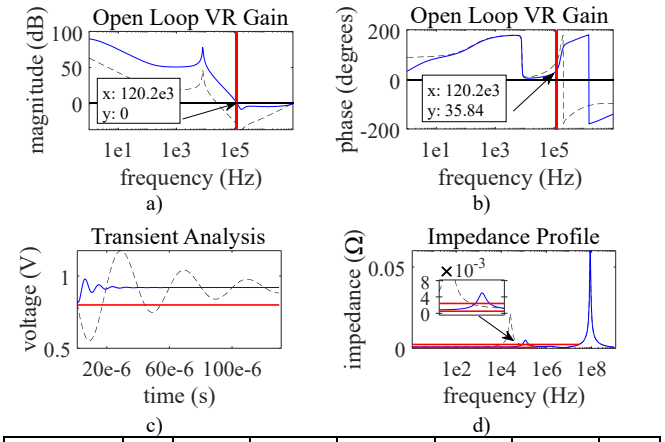
$$\boldsymbol{e}_{\text{B}} = \begin{cases} L_{\text{B}} - N_{\text{CavityCap}} \\ L_{\text{B}} - N_{\text{Pkg0Cap}} \\ \frac{(N_{\text{CavityCap}} + N_{\text{Pkg0Cap}})}{U_{\text{B}}} - 1 \end{cases} \tag{4}$$

where L_{B} is the limiting lower bound for the optimization variables to ensure their values are positive and no less than 1, and U_{B} is the limiting upper bound for the optimization variables. Here we use $L_{\text{B}} = 1$ and $U_{\text{B}} = 140$.

B. Step 2: Optimizing the Compensation of a State Average VR for the PDN

We now optimize the compensation of the state average buck regulator to achieve a crossover frequency of 120 kHz with an acceptable phase margin. For this step, the optimized number of capacitors for the PDN found in Step 1 is used.

The optimization variables now are $\boldsymbol{x} = [R_2(\Omega) \ R_3(\text{m}\Omega) \ C_1(\text{pF}) \ C_2(\text{nF}) \ C_3(\text{nF})]^{\text{T}}$ (see Fig. 2). To decrease the number of variables, R_1 was left at 10 kΩ and L_{VR} at 300 nH.



	R_1	R_2	R_3	C_1	C_2	C_3	L_{VR}
Seed	10	10	100	100	100	100	300
Optimized	10	8.112	21.546	120.544	2.397	92.278	300

e)

Fig. 5. Results for Step 2 before (dashed line) and after (solid line) optimization: a) open loop VR gain magnitude; b) open loop VR gain phase; c) transient analysis; d) impedance profile; e) seed values and final values.

In previous experiments we found poor results considering the converter's open loop gain phase in the objective function. For this reason, here we only consider the converter's open loop gain magnitude. Consequently, we use the following minimax formulation:

$$\boldsymbol{x}^* = \arg\min_{\boldsymbol{x}} \max\{\boldsymbol{e}_{\text{B}}^{T}(\boldsymbol{x}), \boldsymbol{e}_{\text{f}}^{T}(\boldsymbol{x}, f)\} \tag{5}$$

where the error function $\boldsymbol{e}_{\text{B}}(\boldsymbol{x})$ is used to keep the optimization variables within feasible bounds, and the error vector function $\boldsymbol{e}_{\text{f}}(\boldsymbol{x}, f)$ is used for the desired open loop frequency response.

The error vector function $\boldsymbol{e}_{\text{B}}(\boldsymbol{x})$ in (5) is defined as

$$\boldsymbol{e}_{\text{B}} = 1 - \frac{\boldsymbol{x}}{L_{\text{B}}} \tag{6}$$

where L_{B} is the limiting lower bound for the optimization variables to ensure their values are positive; an element-wise subtraction is used in (6), with $L_{\text{B}} = 1{\times}10^{-10}$.

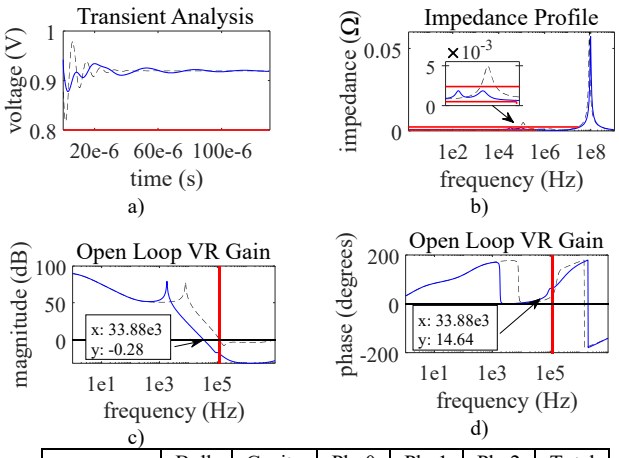
The error vector function $\boldsymbol{e}_{\text{f}}(\boldsymbol{x}, f)$ in (5) is defined as

$$\boldsymbol{e}_{\text{f}} = \begin{cases} \frac{comp_{\text{mag}}(\boldsymbol{x})}{0.8\ dB} - 1 & \text{for } f \ge f_{\text{L}} \\ \frac{comp_{\text{mag}}(\boldsymbol{x})}{-0.8\ dB} - 1 & \text{for } f \le f_{\text{H}} \end{cases} \tag{7}$$

where f_{H} is the high frequency limit of interest, f_{L} is the low frequency limit of interest, and $comp_{\text{mag}}(\boldsymbol{x})$ is the open loop VR gain magnitude in dB. Error function (7) aims at making $comp_{\text{mag}}$ as close as possible to 0 dB when the crossover frequency is between f_{L} and f_{H}. Here we use f_{L} = 118 kHz, and f_{H} = 122 kHz.

C. Step 3: Optimizing the Number of Capacitors in the PDN using a State Average Buck VR

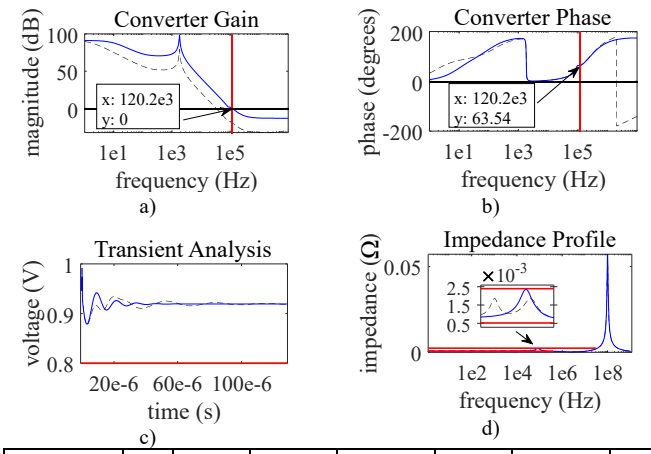
For this step, we solve again the optimization problem (1) with some modifications. By obtaining a stable compensation in the VR we do not need to consider the error function (3), which helps reducing simulation time significantly; we now use $U_{\text{B}} = 700$ and the error function (4) is also modified to consider the bulk capacitors,



	Bulk	Cavity	Pkg0	Pkg1	Pkg2	Total
Seed	1	63	75	1	1	141
Optimized	53	202	430	1	1	687

e)

Fig. 6. Results for Step 3 before (dashed line) and after (solid line) optimization: a) transient analysis; b) impedance profile; c) open loop VR gain magnitude; d) open loop VR gain phase; e) seed values and final values.



	R_1	R_2	R_3	C_1	C_2	C_3	L_{VR}
Seed	10	8.112	21.546	120.544	2.397	92.278	300
Optimized	10	9.827	22.374	131.170	0.340	149.765	300

e)

Fig. 7. Results for Step 4 before (dashed line) and after (solid line) optimization: a) open loop VR gain magnitude; b) open loop VR gain phase; c) transient analysis; d) impedance profile; e) seed values and final values.

$$\boldsymbol{e}_{\mathrm{B}} = \begin{cases} L_{\mathrm{B}} - N_{\mathrm{BulkCap}} \\ L_{\mathrm{B}} - N_{\mathrm{CavityCap}} \\ L_{\mathrm{B}} - N_{\mathrm{Pkg0Cap}} \\ \frac{(N_{\mathrm{BulkCap}} + N_{\mathrm{CavityCap}} + N_{\mathrm{Pkg0Cap}})}{U_{\mathrm{B}}} - 1 \end{cases} \tag{8}$$

IV. Results and Discussion

Figure 4 shows the results for Step 1; it is seen that the impedance profile and voltage droop specifications are met after optimization. Fig. 5 shows the results for Step 2: the crossover frequency is achieved with a phase margin of 35.84°. When using the SAVR with the PDN circuit, the transient voltage droop and the impedance profile are affected. After the optimization in this step, the voltage droop meets the design specifications, however, the impedance profile has a large impedance peak of around 5 mΩ. Fig. 6 shows the results for Step 3; the voltage droop and impedance profile meet the specifications, however, the VR compensation's crossover frequency moved to a lower frequency.

Following the proposed methodology (see Fig. 3), we now repeat the procedure in Step 2. Fig. 7 shows the results for this last step. We now have the desired crossover frequency with a phase margin of 63.54°; the voltage droop and the impedance profile also meet the design specifications.

We obtain good results by following our proposed methodology. The desired crossover frequency is achieved with a good phase margin to ensure stability, as confirmed in the decreased ringing in the transient analysis. The transient voltage noise meets the design specifications, and the impedance profile also meets the maximum target impedance at all frequencies.

V. Conclusion

An optimization methodology was proposed to gradually find the best compensation parameter values of a buck VR to meet some stability criteria. Additionally, the number of parallel decoupling capacitors was optimized considering simultaneously frequency- and time-domain performance specifications. By using optimal VR compensation parameter values and a minimum number of decoupling capacitors, we were able to meet the desired crossover frequency with good phase margin, while the transient voltage and the impedance profile were able to meet the design specifications.

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