A NON-SEQUENTIAL PHASE DETECTOR FOR LOW JITTER CLOCK RECOVERY APPLICATIONS

by

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Abstract

Clock and data recovery (CDR) circuits form the backbone of high speed receivers. These receivers are used in various applications such as chip to chip interconnects, optical communications and backplane routing. The received data in CDR circuits are potentially noisy and asynchronous, i.e. they are not accompanied by a clock. The CDR circuit has to generate a clock from the data and then retime the data. The CDR circuit that recovers the clock and retimes the data has to remove the jitter that is accumulated during its transport through channels due to inter symbol interference (ISI). There are stringent jitter specifications defined by various communication standards that must be addressed by CDR circuits. These make the design of CDR circuits more difficult for system designers as well the circuit designer. Many parameters have to be taken into consideration while designing a CDR circuit. The problem becomes even more interesting as there are various tradeoffs in the design. As speeds of communications increase, the maximum allowable jitter decreases.

Jitter in CDR circuits arises due to a lot of factors and is also dependent on the method used for clock and data recovery. In CDR circuits that use phase locked loops to recover the clock and retime the data, jitter may be caused by the metastability of sequential elements used in phase detectors. Jitter is also caused by the phase noise of the VCO used in the PLL. In CDR circuits that use the delay locked loop to recover the clock and data, jitter may be caused by the metastability of sequential elements in phase detectors as well as the quality of reference clock that is used to re-time the data. Additional effects that can cause jitter in CDR circuits include the use of spread spectrum clocking, delta sigma noise shaping performance, etc.

In this thesis a non-sequential linear phase detector has been proposed which does not use any sequential elements to avoid metastability issues in phase detectors. The output jitter in a CDR circuit that uses the proposed phase detector is measured and compared to a Hogge Phase Detector [5].

Acknowledgements

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Dedication

Dedicated to my family

for their constant source of love and encouragement.

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Chapter 1 – Introduction

1.1 Objective

The objective of this research is to minimize the recovered clock jitter in Clock and Data Recovery (CDR) circuits that use phase locked loops. CDR circuits are used in high speed wireline communication systems to recover the clock and retime the data that was fed as input to the CDR circuit. In this research a new non-sequential phase detector has been proposed that uses only non-sequential elements to reduce the jitter caused by the metastable operation of phase detectors that use sequential elements such as flip-flops and latches. This goal is addressed in this thesis by simulating the proposed phase detector and incorporating it in a CDR circuit used for high speed wireline communications. The complicated nature of such a system required a focused study that did not address many of the issues that are present in a similar commercially designed product.

The clock that is generated by the decision circuit has to satisfy certain important conditions. The frequency of the generated clock should be equal to the frequency of the incoming data. For example, if the data rate is equal to 1Gb/s then the clock frequency should also be equal to 1GHz. The generated clock should also have fixed phase relationship with the data which allows for optimal sampling of the data. Ideally the data should be sampled by the clock at exactly the mid-point of each data bit. This allows for more margin for jitter and intersymbol interference that can be reduced but cannot be entirely eliminated in the CDR's system. The third and the most important feature of the recovered clock is that it should have the lowest jitter. Since the data is retimed with the recovered clock, it is essential that the recovered clock have low jitter so that the jitter is not passed on to the data and result in high bit error rates (BER).

1.2 Why this Research is Necessary?

As speeds of communication increases, the total amount of jitter allowed in CDR circuits decreases. Jitter in CDR circuits can be defined as the total variation of the recovered clock and data once lock in attained. There are various reasons for jitter in CDR circuits such as

metastability of phase detectors, supply and substrate noise, VCO noise performance, spread spectrum clocking, etc. Jitter in CDR circuits leads to higher Bit Error Ratios. Therefore, reducing the jitter in CDR circuits reduces the BER. High speed communication circuits have extremely stringent jitter tolerances and need new and better designs.

Increased BER is not the only negative effect of jitter. In a repeater, where the recovered clock acts as the transmit clock for the next data link, phase jitter decreases the number of links that can be cascaded before the jitter becomes unacceptable.

It is beyond the scope of this research to reduce the jitter due to all the factors that are mentioned in the first paragraph. Therefore we focused on the problem of metastability in phase detectors that cause output jitter. At high speeds of communications, typical circuit techniques of designing logic circuits do not work properly and the problem of metastability increases. In this thesis, logic gates and flip flops have been designed using CML techniques that can accurately work at higher speeds. The charge pump is a differential charge pump that is used for high speed communication CDRs. Finally an LC VCO is used for clock recovery in the CDR circuit as an LC VCO has better phase noise performance compared to other VCOs such as the ring oscillator VCO which is widely used in CDR circuits. It should be noted that higher phase noise translates into more jitter in the CDR circuit because phase noise is the frequency domain analogue to jitter in the time domain.

1.3 What is Metastability?

Before we understand what the term metastability is we need to understand what set-up and hold times are for a flip flop. The set up time of a flip flop is the time required for a incoming data signal to be valid before the clock edge arrives. The hold time of a flip flop can be defined as the time required for the input data signal to be held after the clock edge arrives. Whenever there are setup and hold time violations in flip-flops, they enter into a state called metastable state. During this metastable period, the output of the D-flip flops is unpredictable. The time it takes to settle down to a stable state depends on both the process and the technology. While technology and processes of semiconductor design have both improved tremendously over the years, they have been accompanied by a comparable

increase in clock rates over the same period. Hence, issues such as metastability continue to cause problems in design endeavours.

Since the popularly used linear and binary phase detectors such as the Hogge [5] and the Alexander [8] phase detectors use more than one flip-flop, their susceptibility to giving out erroneous signals is very high as they are prone to metastable states. This in turn means significant jitter in the CDR circuit due to false phase detection errors by the phase detector. To overcome this problem, the phase detectors that are to be used in CDR circuits should be non-sequential but at the same time be able to detect any transition on the data edges.

Chapter 2- Clock and Data Recovery Architectures in Serial Communications

2.1 Introduction

Clock and data recovery (CDR) Circuits are widely used in high speed serial communication links. Bandwidth increases have led to higher speeds of communication links that vary from 1 Gb/s per lane in PCI™ express to 100 Gb/s in high speed ethernet links. Parallel communication has been almost completely wiped out by serial communication to achieve higher speeds and lower costs. In serializer–deserializer (SERDES) architectures, the parallel data goes through a parallel-in-serial out (PISO) block in the transmitter and a serial-in-parallel out (SIPO) block in the receiver. Several SERDES architectures have been proposed and their implementation is application specific. The data is not accompanied by a clock in these architectures to avoid clock skew problems and decrease costs.

SERDES architectures are used in high definition multimedia interfaces (HDMI™) and the next generation multimedia interface, DisplayPort™. DisplayPort™ can support 4 different channels with each channel capable of sending upto 2.7Gb/s thus having a total throughput of 10.4Gb/s [1] with 4 channels. It uses SERDES architecture and transmits data in the 8b/10b encoding format to ensure data transitions over a shorter period of time. The jitter tolerance in these multimedia interfaces is very stringent. USB™ 3.0 [2] also supports speeds upto 5.4Gb/s.

The serially transmitted data is passed through an equalizer after travelling through the channel links that distort the data because of inter-symbol interference (ISI). There are generally two ways to recover the clock and the data. The first method that is used to generate the clock is by using PLL and the other method that is used to generate the clock and retime the data is by using a delay locked loop (DLL). The data passed through the equalizer is fed to the clock and data recovery circuit where the clock is extracted from the data using a phase locked loop (PLL) when there is no availability of a reference clock at the correct frequency of the transmitted data. Delay locked loops (DLL) are used when a reference clock is available at exactly the correct frequency of the transmitted data.

Typically DLLs have lower output jitter compared to PLLs as oscillator noise and resulting jitter from it are not factors [3].

The block diagram of CDR circuit can be seen in Fig.1.

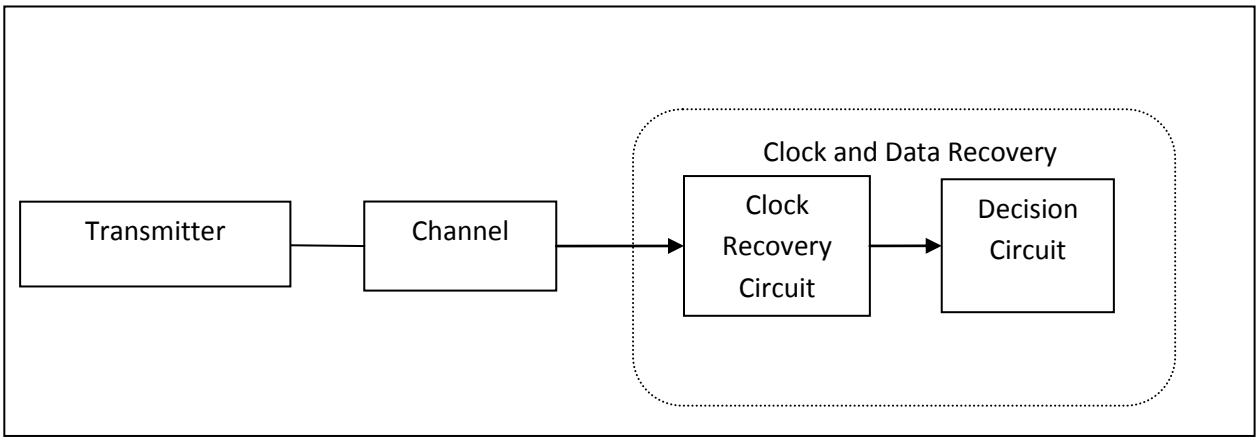

Figure 1. Block Diagram of Clock and Data Recovery

PLL based clock recovery has various advantages over other methods. It offers the advantage that it can be integrated in a chip and is relatively inexpensive. This thesis addresses clock recovery using a PLL with low output jitter. PLLs consist of various non-ideal blocks and these blocks contribute to the output jitter. Thus, it is of utmost importance to design a PLL that minimizes the amount of jitter in the CDR circuit.

2.2 Clock and Data Recovery Using Phase Locked Loops

In this section CDR architecture using the PLL method is studied and its various tradeoffs are outlined. CDR architectures using the PLL method can be considered as a second order feedback system where a clock is generated whose output phase is aligned with the phase of the incoming data. Once the phase is aligned, the system is said to be in lock. As the phase is the integration of the frequency, the PLL is locked both in frequency and phase. The phase alignment is achieved by comparing the phase of the data and the generated clock. If the phases of the data and clock are not the same, then the difference in phase is fed to the charge pump and low pass filter which generate a control voltage. The Voltage Controlled Oscillator (VCO) then generates a clock and through negative feedback in the entire loop,

the control voltage forces the VCO to generate a clock that is phase aligned to the data. The block diagram of a CDR architecture using the PLL method of clock recovery is shown in Fig.2.

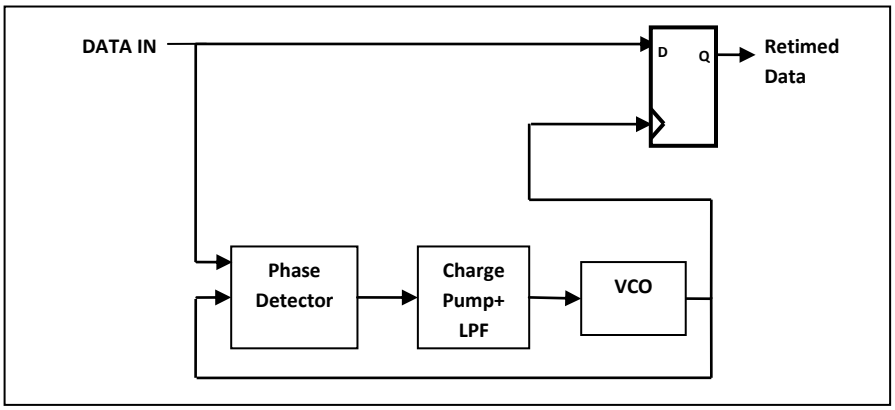

Figure 2. CDR block diagram using PLL to recover clock

It can be seen in Fig.2 that the PLL used in a CDR architecture consists of a phase detector, charge pump, low pass filter and a voltage controlled oscillator. The phase detector detects the phase difference between the clock and the input data and then sends the corresponding early/late information to the VCO via the charge pump and low pass filter. The resulting current from the charge pump is fed into the low pass filter. The resulting control voltage that comes out of the loop filter varies the output frequency of the VCO.

The loop filter that is used with the charge pump is shown in Fig.3. When there is a slow variation in the phase, the current from the charge pump linearly charges the capacitors C1 and C2. Thus it works with an averaging effect. However, for fast variations in the phase, the current in the charge pump drives only the resistor as C2 is generally small. This way the VCO tracks the moving variations of the input quickly if there are large phase variations.

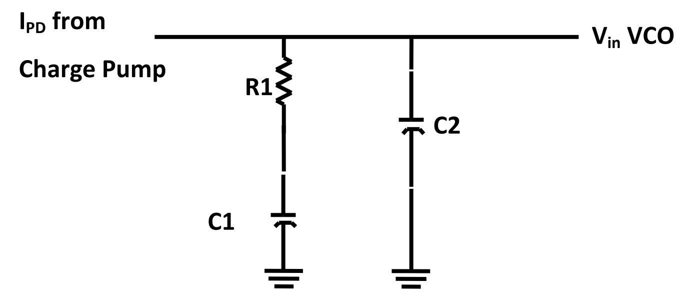

Figure 3. Loop filter

The transfer function for the loop filter used with a charge pump is given in equation 1.

$$\frac{V_{in}VCO}{I_{PDI}} = \frac{1+sRC1}{s(C1+C2).\left[1+sR\frac{C1.C2}{C1+C2}\right]} = K_F \text{ ……………..…………..…(1)}$$

where I_{PDI} is the current in the charge pump. The output voltage is a function of the charge pump current.

Generally the value of capacitor C2 is about 1/10th the value of capacitor C1. Thus, we can neglect C2 for the transfer function calculations. The loop filter transfer function neglecting C2 simplifies to:

$$K_F = \frac{1+sRC1}{sC1} \text{……………………………............... (2)}$$

Using these equations, we can write that the feedback loop transfer function of the entire PLL is given by

$$H(s) = \frac{K_{PDI}.K_{VCO}.(1+sRC1)}{s^2+s\left(\frac{K_{PD}K_{VCO}R}{N}\right)+\left(\frac{K_{PDI}K_{VCO}}{NC1}\right)} \text{………………………………..(3)}$$

where K_{PDI} is the gain of the phase detector and K_{VCO} is the gain of the VCO.
The natural frequency is given by

$$\omega_n = \frac{\sqrt{K_{PDI}K_{VCO}}}{\sqrt{NC1}} \text{………………………..………………(4)}$$

The damping factor is given by

$$\varsigma = \frac{\omega_n}{2}.RC1 \text{……………………………………………(5)}$$

In CDR Circuits that use PLL, there are various factors that can cause output jitter such as metastability in phase detectors, supply and substrate noise in oscillators [4], delta-sigma modulation noise shaping performance, spread spectrum clocking (SSC) impacts etc.

Phase detectors that are used in CDR Circuits can be generally divided into linear and non-linear (bang-bang) categories. Linear phase detectors output the magnitude of the phase difference between the clock and the data while bang-bang phase detectors such as the Alexander phase detector output only early/late information depending on whether the clock is leading or lagging the data. The magnitude of the early/late pulses is not proportional to the phase difference between the data and clock in bang-bang phase detectors.

Chapter 3– Jitter and Sources of Jitter in PLL based Clock Recovery

Jitter is defined by NIST[12] as " the short term phase variation of the significant instants of a digital signal from their ideal positions in time." It is the most important characteristic in CDR circuits. It should be understood that jitter is a time domain measurement while phase noise is a frequency domain measurement. The dual Dirac model is universally accepted as the best way of estimating the total acceptable jitter at a particular BER. The dual Dirac model assumes that the total jitter in a CDR circuit can be broadly classified into two categories namely random jitter (RJ) and deterministic jitter (DJ). RJ is caused by the accumulation of various processes that have very small magnitudes such as thermal noise, shot noise and flicker noise. DJ is caused by a relatively small number of processes that may not be independent and have comparatively larger magnitude such as electromagnetic interference and channel frequency response.

The total jitter in a CDR circuit can be represented by the block diagram shown in Fig.4.

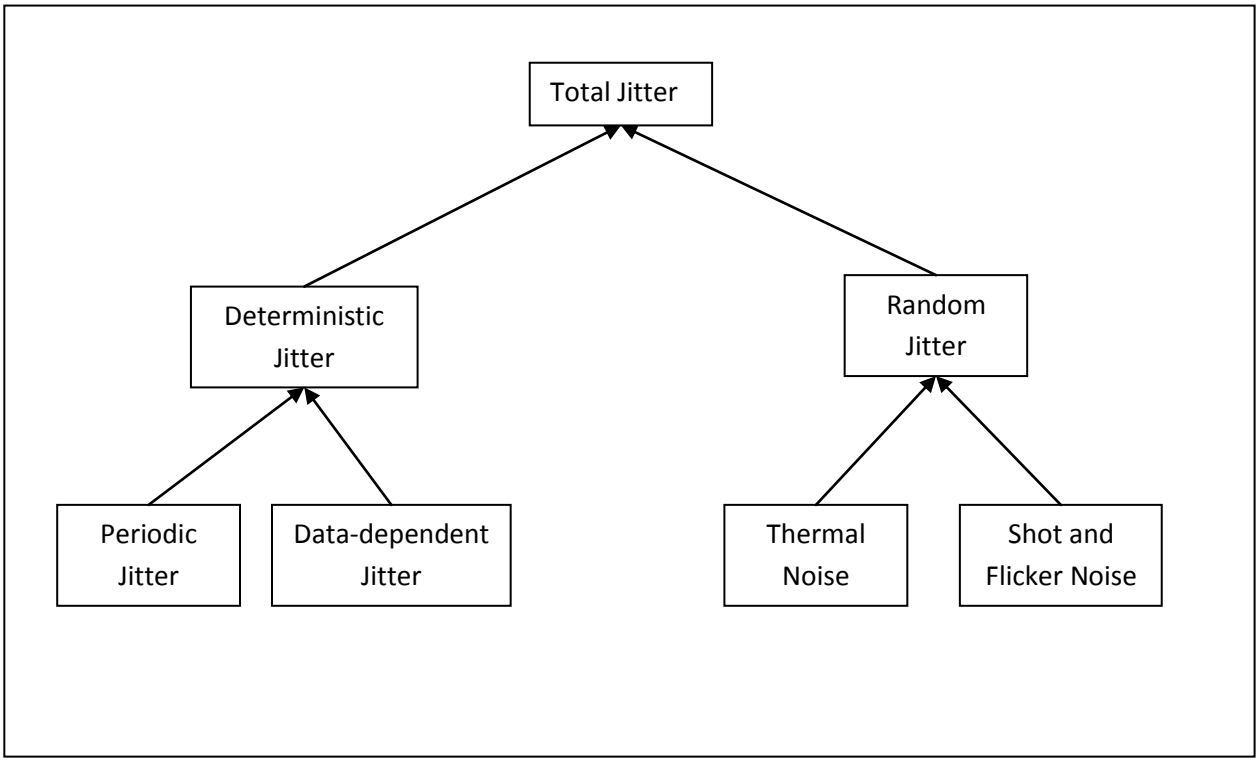

Figure 4. Jitter in CDR circuits

3.1 Random Jitter

Random jitter (RJ) is jitter that has no determinable pattern. The probability density function (PDF) of RJ is unbounded. As random jitter is approximated by a Gaussian PDF, theoretically there is no maximum limit to its magnitude. In other words, it does not have a well defined peak to peak value. RJ is described as a Gaussian function and the width or the standard deviation is enough to describe the magnitude of RJ. The PDF of RJ is expressed in Eq.6.

$$\mathrm{PDF_{RJ}}(x) = \frac{1}{\sqrt{2*\pi}*\sigma}\exp[\frac{-x^2}{2\sigma^2}] \quad \text{.....(6)}$$

where σ is the width of the Gaussian distribution.

As the primary reason for random jitter is noise from the circuits such as shot and thermal noise, it can only be reduced but cannot be completely removed from a system.

3.2. Deterministic Jitter

Deterministic jitter is jitter that does not have a Gaussian PDF. Thus it has a well defined peak-to-peak value in contrast to random jitter. DJ follows a distribution formed by two Dirac-delta functions. The time-delay separation of the two delta functions gives the dual-Dirac model-dependent DJ and is shown in Fig.5. RJ and DJ components of jitter combine through convolution to give us the relation expressed in Eq.7.

$$\mathrm{PDF}(x) = \mathrm{PDF_{DJ}}(x) * \mathrm{PDF_{RJ}}(x)$$

$$= \int \mathrm{PDF_{DJ}}(u) * \mathrm{PDF_{RJ}}(x-u).du \quad \text{.....(7)}$$

The width of the DJ is expressed by the dual Dirac approximation in equation 8.

$$\mathrm{DJ_{(peak\text{-}to\text{-}peak)}} = \mu_R - \mu_L \quad \text{.....(8)}$$

Figure 5 shows the dual Dirac model of DJ and the Gaussian representation of RJ and their convolution results.

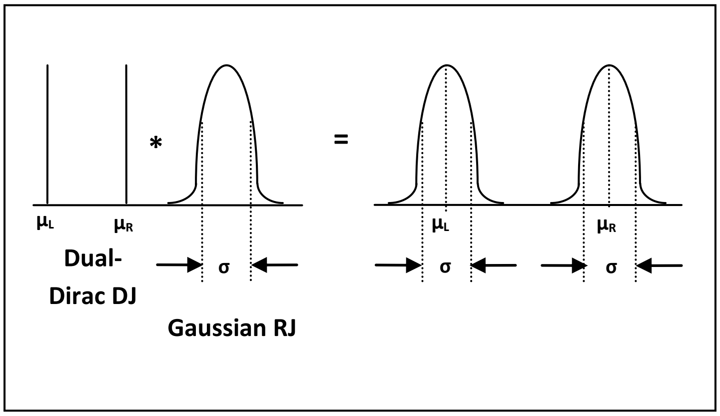

Figure 5. Convolution of Deterministic and Random Jitter

3.3 Jitter and BER

The jitter PDF is the convolution of random and deterministic jitter as shown in Fig.5. The total jitter at any given BER is given as

$$TJ(BER) = 2*Q_{BER}*\sigma + DJ_{(peak\text{-}peak)} \quad \text{……………………..…….(9)}$$

where Q_{BER} is the multiplicative constant and is calculated from the complementary error function. The value of Q_{BER} for various values of BER [11] is given in Table 1.

Q_{BER}	BER
6.4	1.00E-09
6.7	1.00E-10
7	1.00E-11
7.3	1.00E-12
7.6	1.00E-13

Table 1. BER for Various QBER values

3.3 Measurement of Jitter

The most important performance characteristic of CDR circuits is jitter and hence it is important to know how jitter is measured. There are three measurements that are needed to define the total amount of jitter in a signal. These three distinct measurements of jitter are called root mean squared (RMS) jitter, peak-to-peak jitter and BER. The relationship of BER and total jitter is discussed in section 3.2.

3.4 Root Mean Squared Jitter

The root mean squared (RMS) jitter in a signal is a measurement of the average amount of jitter in a signal. RMS jitter is computed using the following equations.

$$\mu_j = \frac{1}{N}\sum_{n=1}^{N} j(n)$$

$$\sigma_j = \sqrt{\frac{1}{N-1}\sum_{n=1}^{N}\left(j(n)-\mu_j\right)^2} \quad \text{.....(10)}$$

where μ_j is the mean value of the jitter and N is the number of jitter samples used to calculate the jitter. σ_j is the RMS value of the jitter in the signal.

3.5 Peak-to-Peak Jitter

The peak to peak jitter measurement of jitter gives the maximum values of jitter over a period of N jitter samples. The sample size N should be large enough so that the peak-to-peak jitter can be properly estimated. Peak-to-peak jitter is represented by the following equation.

$$Jitter_{p-p} = \max[j(N)] - \min[j(N)] \quad \text{.....(11)}$$

Chapter 4– Phase Detectors in Prior Art

There is a lot of literature on linear and non-linear phase detectors. Most of the phase detectors that are commonly used have sequential elements in them. There are some linear phase detectors that have been proposed that do not use sequential elements but to the best of my knowledge there are no bang-bang phase detectors that do not use sequential elements.

A linear phase detector that works for random NRZ data was first proposed in [5]. This phase detector is called the Hogge phase detector and is named after its inventor, C.R. Hogge. It uses two D-flip flops and two XOR gates for its operation. It is however speed limited because of the flip flops going into metastable regions at high speeds. A non-sequential phase detector that can be used in a PLL that employs the ring oscillator type VCO is shown in [6]. The phase detector proposed in this thesis is similar to the phase detector proposed in [6] but it does not require a ring oscillator type VCO. It also has an additional XOR gate to compensate for static offset. The low performance of a ring oscillator type VCO can lead to high output jitter in the CDR system. In [7], another non sequential phase detector that generates a reference and difference pulse at every data transition is shown but it cannot be used as a self correcting phase detector such as the Hogge phase detector.

Bang-bang or binary phase detectors are another category of phase detectors. These phase detectors have an output that is not proportional to the magnitude of the phase difference between the clock and data. The Alexander type bang-bang phase detector [8] is the most popular bang-bang phase detector. In [9] a novel binary phase detector is proposed that samples the clock with respect to data with a probable lock detector. A new current integrating bang-bang type phase detector is shown in [10]. Most bang-bang phase detectors that are used in CDR circuits are made of sequential elements. Bang-bang phase detectors have higher output jitter compared to linear phase detectors.

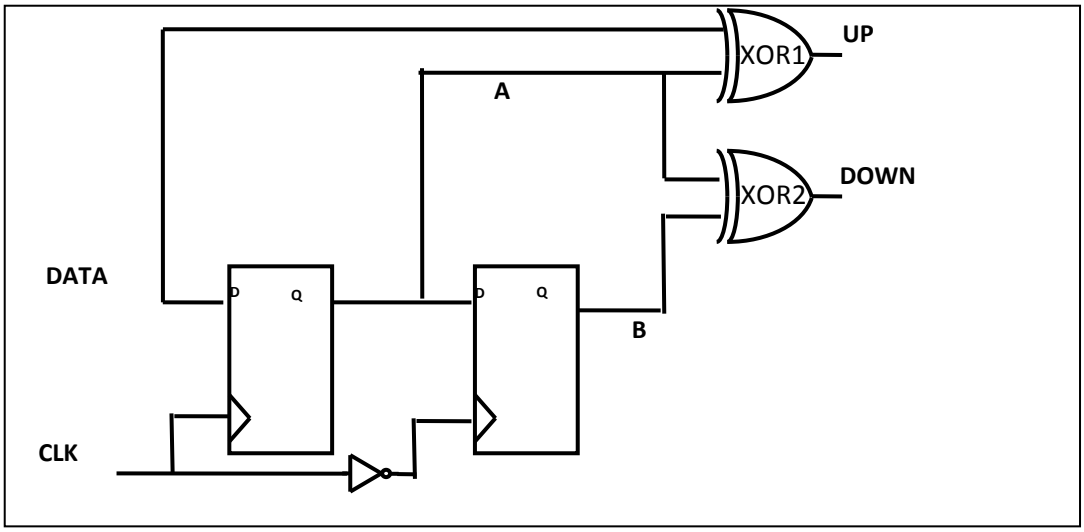

Figure 6. Hogge Phase Detector

4.1 Linear Phase Detectors

The most commonly used linear phase detector for recovery for random NRZ data is shown in Fig.6. The Hogge phase detector essentially subtracts two pulses that come out of the XOR gates. The charge pump accomplishes this subtraction. XOR1 generates a reference pulse that is exactly half a bit time in width. XOR2 generates a pulse whose width depends on the phase error between the edges of Data and the edges of CLK. When the phase difference between DATA and CLK is half a bit, the two pulses cancel each other thus generating very little change in the PD output. This little change in the phase detector output is due to the fact that the UP and DOWN pulses are not generated simultaneously. The linear characteristics of Hogge phase detector is shown in Fig.7. The linearity results from the net pulse width at the output being linearly proportional to the phase difference between the center of Data and the edges of Clk. The saw-tooth shape of the transfer function is due to phase being a modulo-2π quantity. Phase detector gain (KPD) is defined as the slope of the transfer function when the phase error is close to zero.

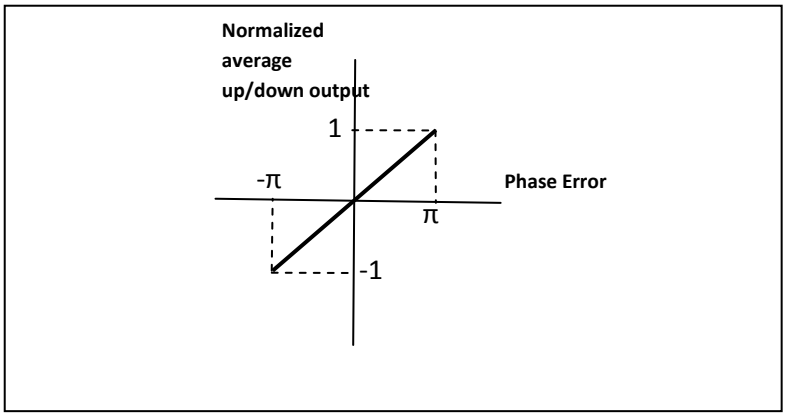

Figure 7. Linear Characteristics of Hogge Phase Detector

Linear phase detectors suffer from a phenomena called dead zones. Dead zones are defined as the state in which there is no activity on the control lines when the phase error is close to zero. Dead zones arise from the inability of digital gates to generate infinitely small pulses. Several papers have proposed various different architectures to avoid dead zones [15], [16]. The timing diagrams for the Hogge Phase detector under lock conditions is shown in Fig. 8. Figure 9 shows the timing diagram of the Hogge Phase detector when the DATA leads the CLK and Fig.10 shows the timing diagram when the DATA lags the CLOCK.

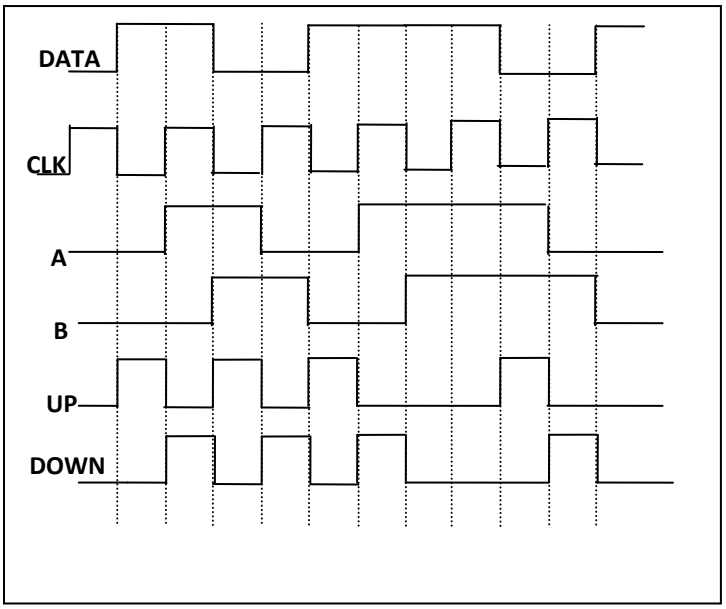

Figure 8. Timing diagram of Hogge phase detector under lock conditions

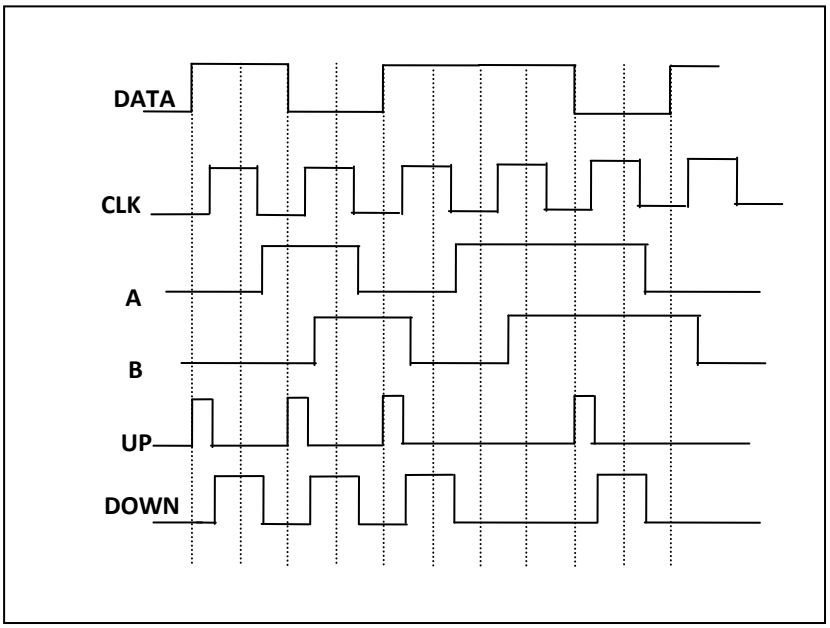

Figure 9. Timing diagrams of Hogge phase detector when DATA leads CLK

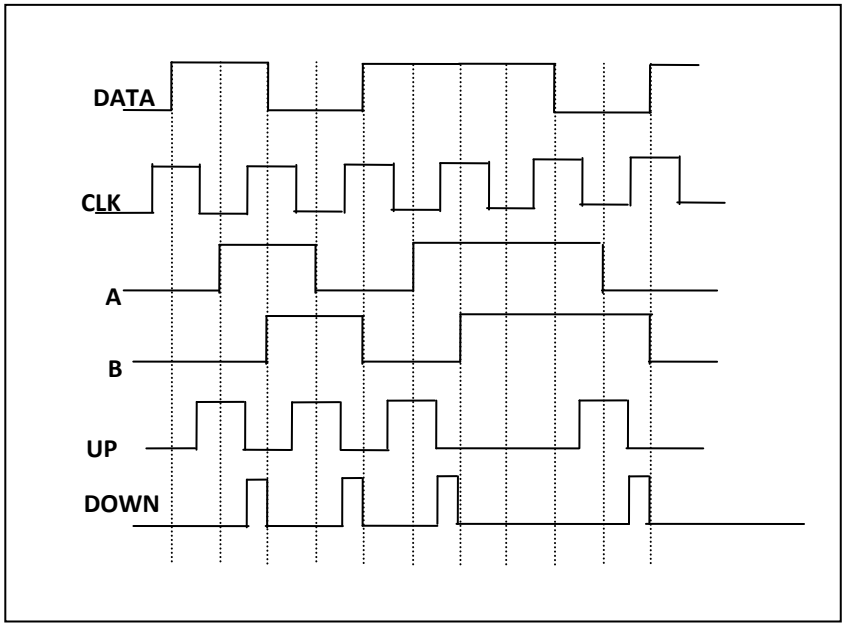

Figure 10. Timing diagrams of Hogge phase detector when DATA lags CLK.

4.3 Bang Bang Phase Detectors

Bang-bang phase detectors are another category of phase detectors that are used in CDR circuits. Bang-bang phase detectors are also known as binary phase detectors and exhibit a non-linear behavior. The Alexander phase detector is the most popular binary phase detector. It is shown in Fig.11.

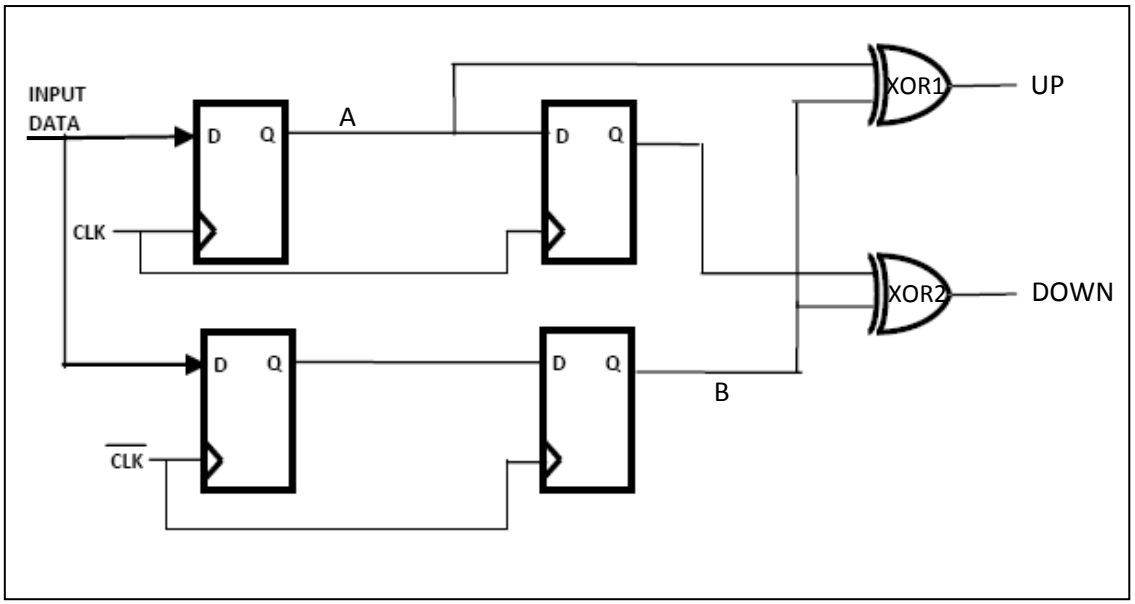

Figure 11. Alexander Phase Detector

Similar to the linear PD, it subtracts two pulses each generated from the XOR gates. However, both pulses are a bit period wide. The output of the XOR1 is high when the previous data sample and the current edge sample are not equal. XOR2 is high when the next data sample is not equal to the current edge sample. The PD output is zero when both XOR gates are low (denoting no transitions in the data and hence no timing information) and when both are high (invalid state). When only XOR1 high, the clock is sampling the data late and the PD output is positive. When XOR2 is high, the edge sampling is early compared to the transition and the PD output is negative. The PD is binary as it can only decide the early or late relationship but loses the phase error magnitude information. K_{PD} is difficult to define as the slope of the curve through the zero crossing is infinite. Bang-bang phase detectors are associated with significant output jitter because once in lock the phase offset

drifts inside the two extreme values of the dead band. Since binary phase detectors are non-linear they give rise to limit cycles in steady state operation and this leads to higher jitter. The non-linear characteristics of binary phase detectors are shown in Fig.12.

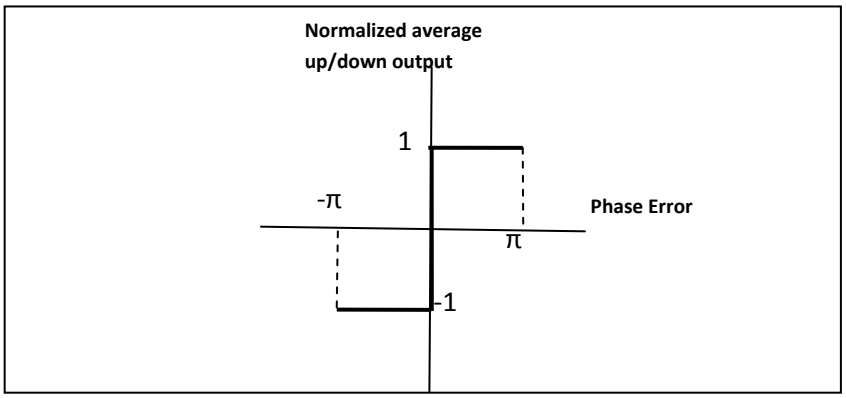

Figure 12. Non-linear Characteristics of Binary Phase Detectors

Figures 13 and 14 shown the timing diagrams of the Alexander phase detector when the DATA leads the CLK and vice versa respectively.

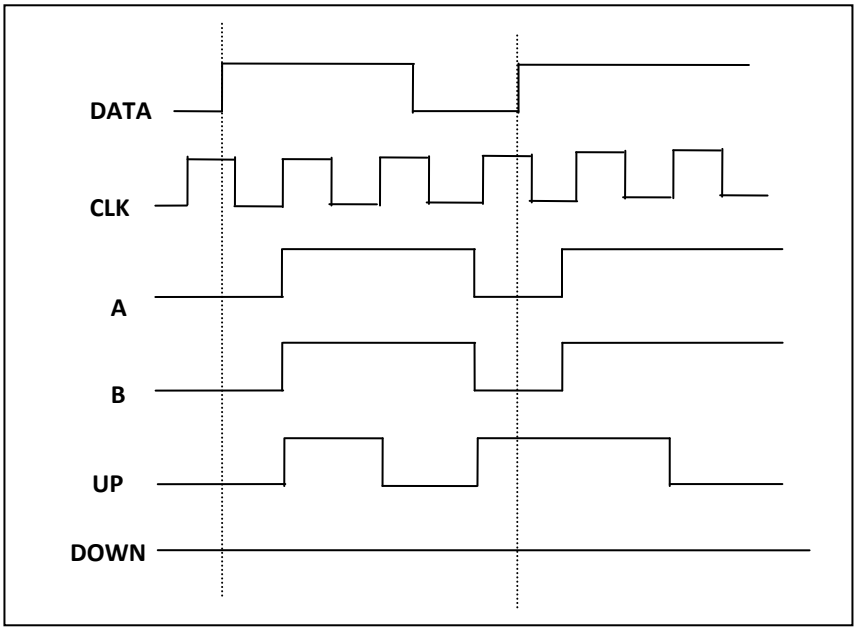

Figure 13. Alexander phase detector timing diagram when DATA leads CLK edge

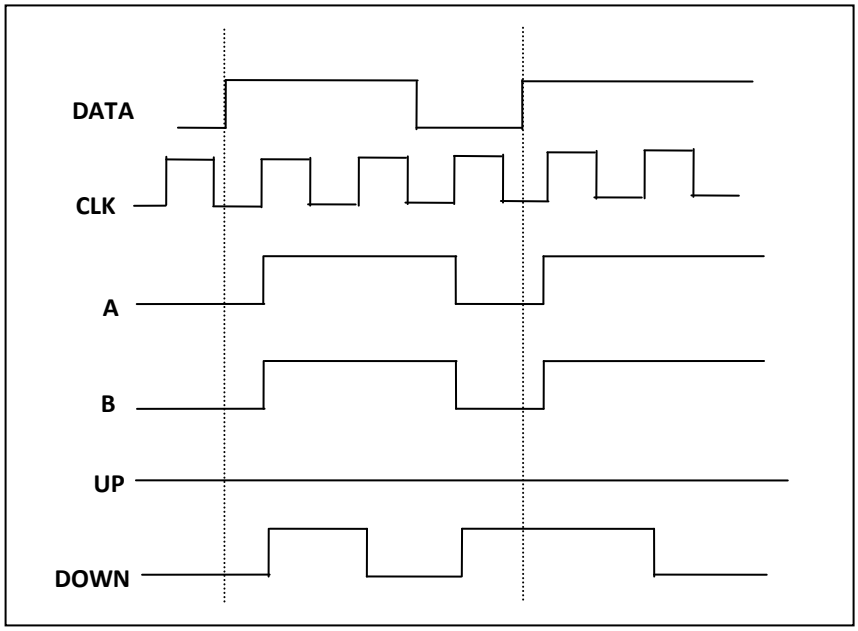

Figure 14. Alexander phase detector timing diagram when DATA lags CLK edge

From the discussion of linear and binary phase detectors, one can conclude that for low jitter applications, linear phase detectors are preferred. In this thesis, therefore, a linear phase detector is proposed and incorporated into the CDR circuit.

Chapter 5 – Proposed Phase Detector

The proposed phase detector that operates without flip-flops is shown in Fig.15. This phase detector is very simple and just uses 3 XOR gates, 2 delays and 2 AND gates.

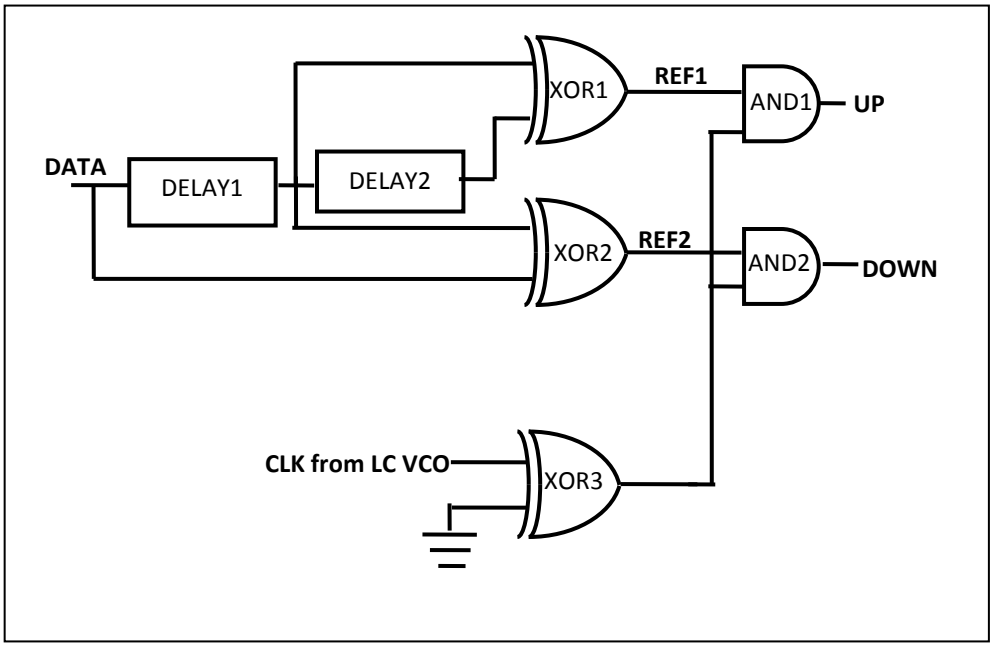

Figure 15. Proposed Phase Detector

The phase detector detects the data transitions in the same way as the phase detector proposed in [6] but does not use a ring oscillator type VCO. It also improves the phase detector proposed in [6] by adding another XOR gate to compensate for the static offset mismatch. The phase detector operates by generating two references from the data, REF1 and REF2. REF1 is generated by the XOR operation of the DATA and DELAY1 and REF2 is generated by the XOR operation of DELAY1 and DELAY2. The timing diagram of the proposed phase detector under lock conditions is shown in Fig.16. Since the delay times are not critical in this design, they can be implemented with a series of inverters and can be controlled for process and temperature variations.

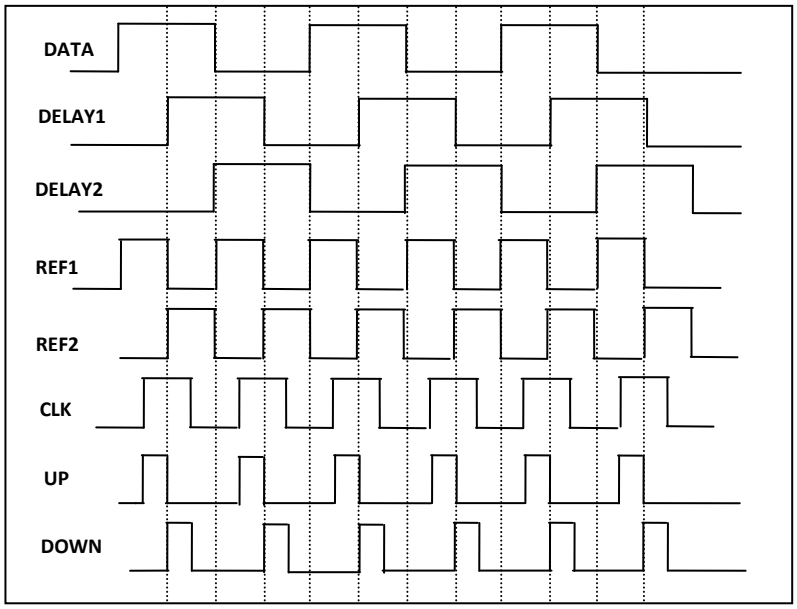

Figure 16. Timing Diagram of Proposed Phase Detector at Lock Conditions

The clock pulse is XORed to the ground to delay it so that it minimizes static offset. The output of XOR3 is just a delayed version of the CLK. The output of the AND1 and the AND2 will be equal if the DELAY1 is sampled at the midpoint of the clock. This can be seen in Fig.4. If the CLK is lagging behind the DATA then the UP pulse will be wider compared to the DOWN pulse and if the CLK pulse is leading the DATA, then the DOWN pulse will be more compared to the UP pulse. It is to be noted that in this case the CLK will lock to DELAY1 as it samples DELAY1 at the middle of the CLK. However, since DELAY1 is just a delayed replica of the DATA, so the recovered clock will be the same if the CLK would sample the DATA.

The proposed phase detector will have a control voltage line that is similar to the Hogge Phase detector and the jitter in the circuit can be reduced by reducing the gain of the phase detector. This is achieved by reducing the current in the charge pump.

Figure 17 shows the timing diagram of the proposed phase detector when the DATA lags the CLK and Fig.18 shows the timing diagram of the proposed phase detector when the DATA leads the CLK.

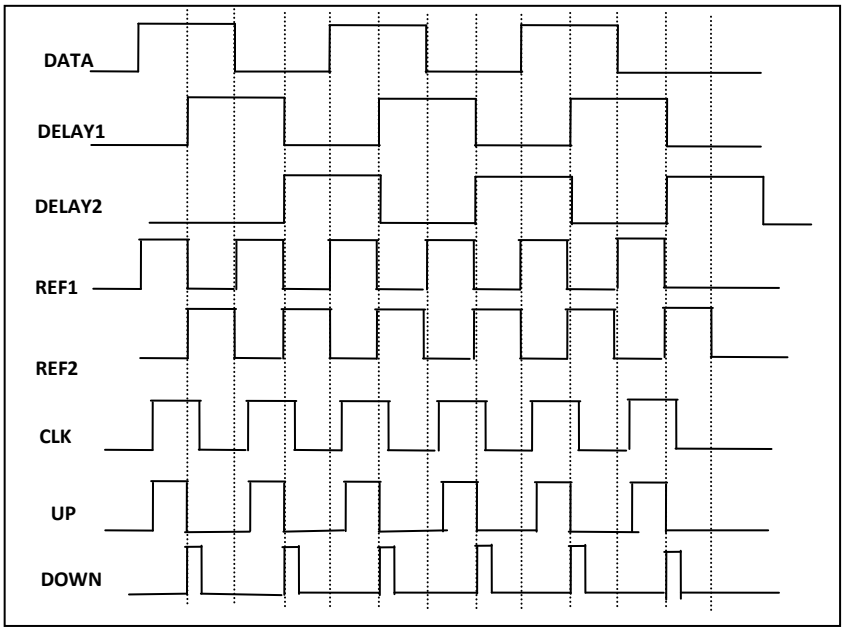

Figure 17.Timing Diagram of proposed phase detector when DATA Lags CLK

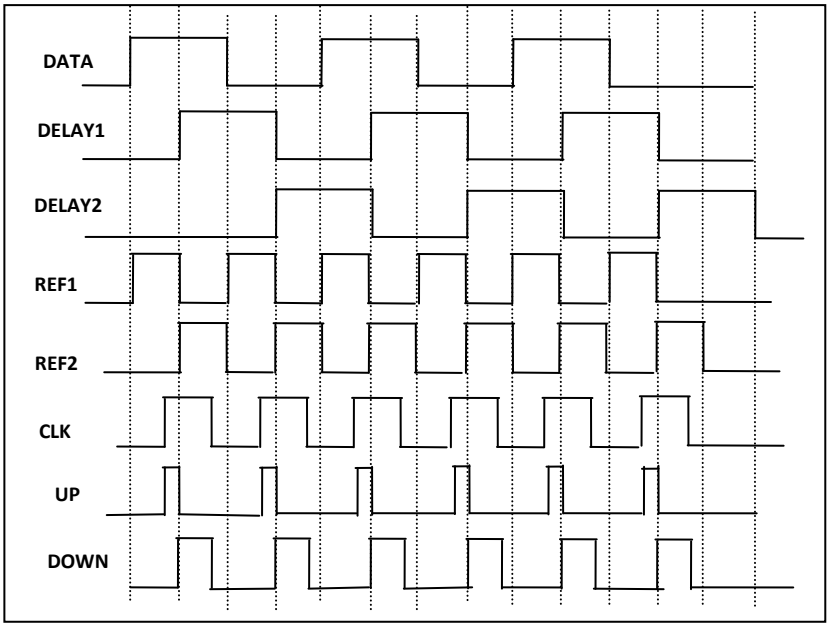

Figure 18.Timing Diagram of proposed phase detector when DATA Leads CLK

It can be seen that the proposed phase detector has a linear characteristic similar to the Hogge phase detector. Since the phase detector has similar characteristics to the Hogge

phase detector but does not use sequential elements, this phase detector will have better jitter performance for high speed applications.

The architecture of the complete CDR using the proposed phase detector is shown in Fig.19.

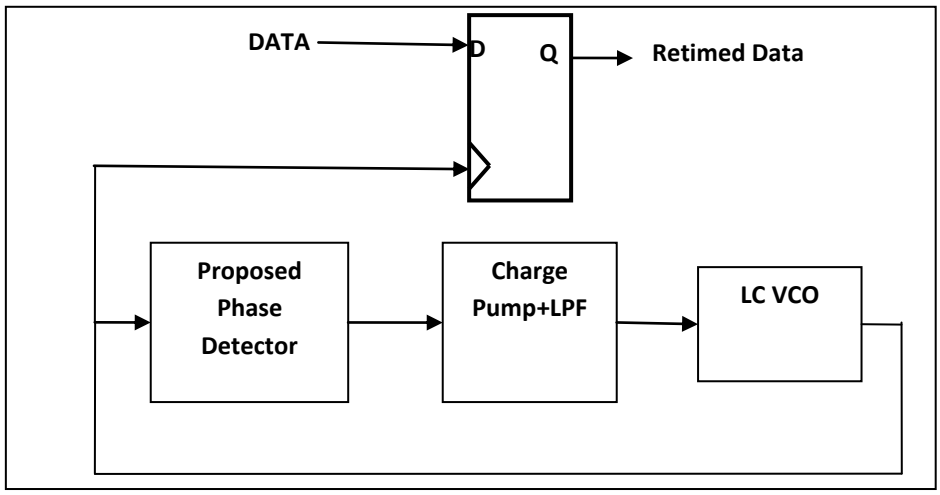

Figure 19.Complete architecture of the CDR

Chapter 6 – Implementation of Clock and Data Recovery Circuit

The phase detector that was discussed in the earlier chapter has been implemented using Agilent ADS tools. For the MOSFET's BSIM 3.1 models have been used. BSIM 3.1 models for the TSMC 0.18μ process have been used from MOSIS website. The spice parameters for the BSIM3.1 PMOS and NMOS are given in Table 4 and Table 5 in the appendix.

The implementation of a LC VCO requires varactors for frequency control. Due to the unavailability of process development kits, the varactors have been realized using MOS technology by connecting the FETS as diodes.

At high speeds of communications, typical digital logic circuits do not work properly. Hence, CML logic gates and flip-flops are used in this thesis. CML is a differential logic technique that used for gigabit communication speeds. CML logic offers various advantages over conventional static logic gates. At higher frequencies, CML logic has less power dissipation compared to static logic gates.

6.1 CML AND Gate

Figure 20 shows the schematic of a CML AND gate.

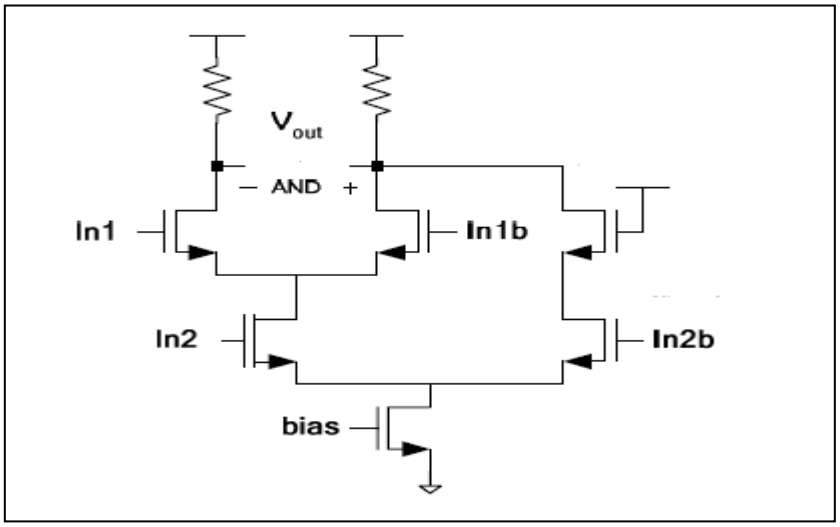

Figure 20. CML AND gate

6.2 CML XOR Gate

The CML implementation of XOR gate is shown in Fig.21.

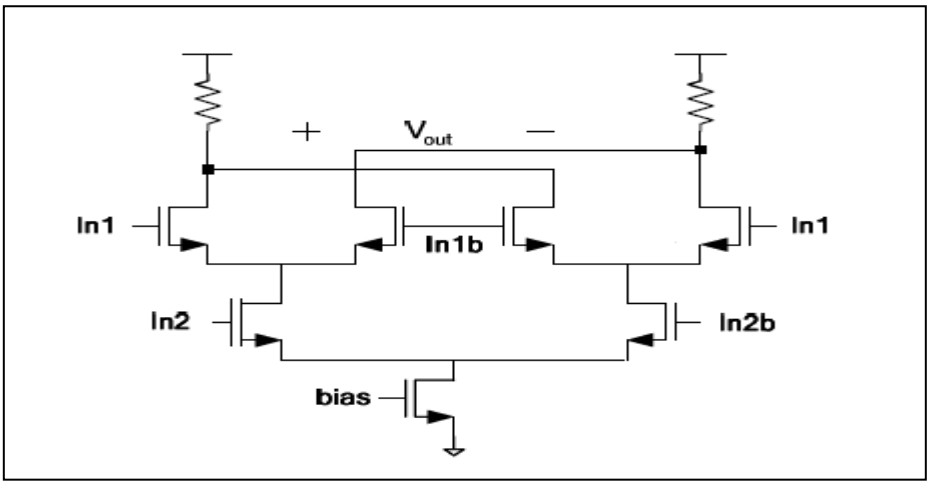

Figure 21. CML XOR Gate

6.3 CML D Latch

Figure 22 shows the implementation of a CML D-latch

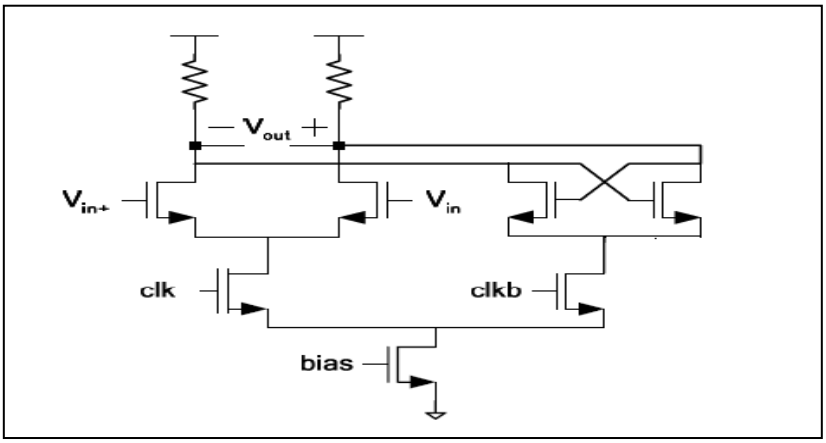

Figure 22. CML D-Latch

6.4 Implementation of the Proposed Phase Detector

The Agilent ADS implementation of the proposed phase detector is shown in Fig.23.

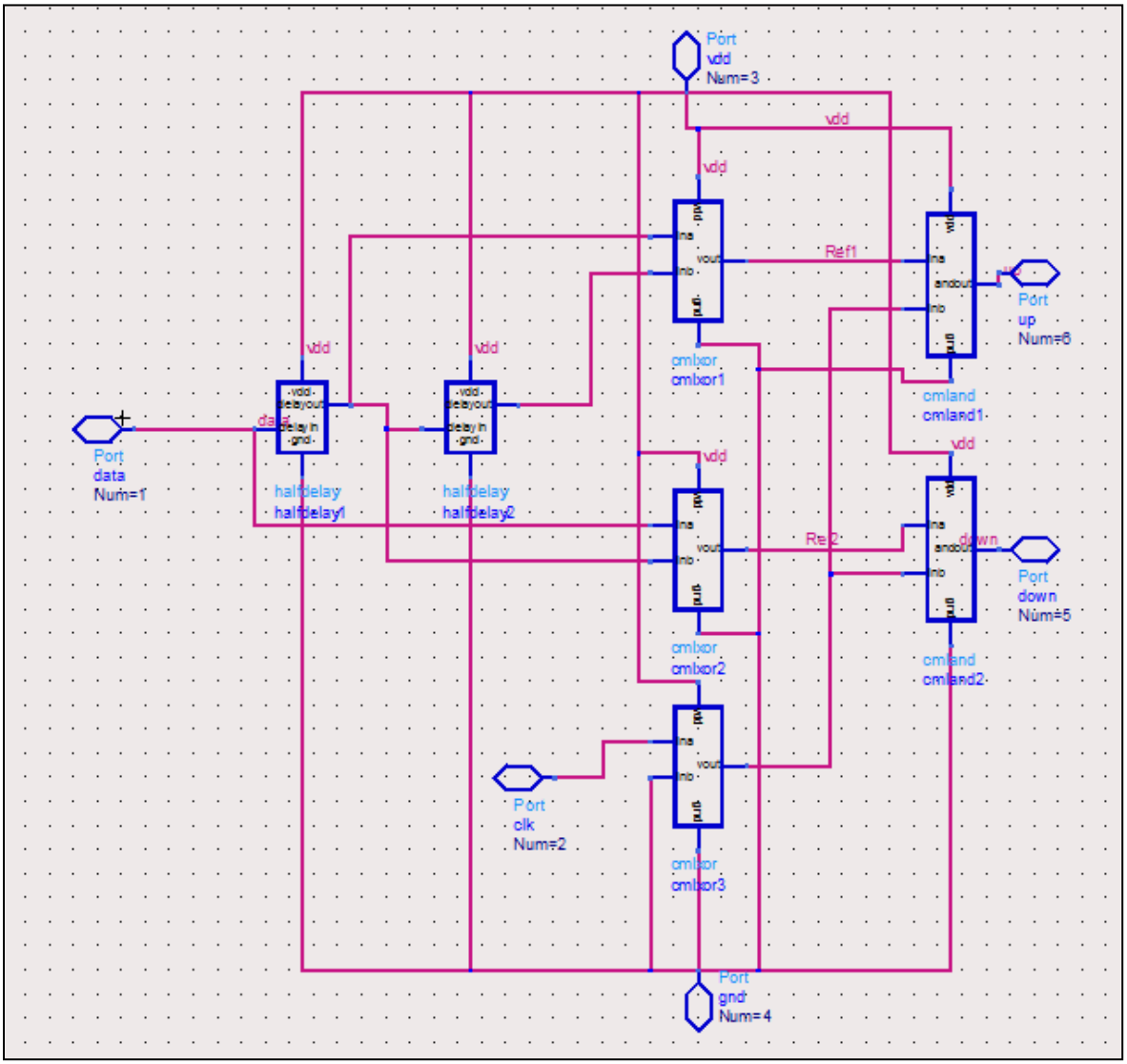

Figure 23.Agilent simulation of the Proposed Phase Detector.

6.5 Implementation of the Charge Pump

The charge pump is the circuit that translates the UP and DOWN pulses that come from the phase detector. The conceptual schematic of a charge pump circuit can be in Fig.24. The charge pump has two current sources that drive the loop filter. The charge pump is switched on and off by the output signals of the phase detector. Therefore the charge pump can have three different control stages that can be seen in Table 2.

Up	DOWN	Charge Pump Output
0	0	No change
0	1	Current increases the VCON
1	0	Current decreases VCON

Table 2. Charge Pump Control States

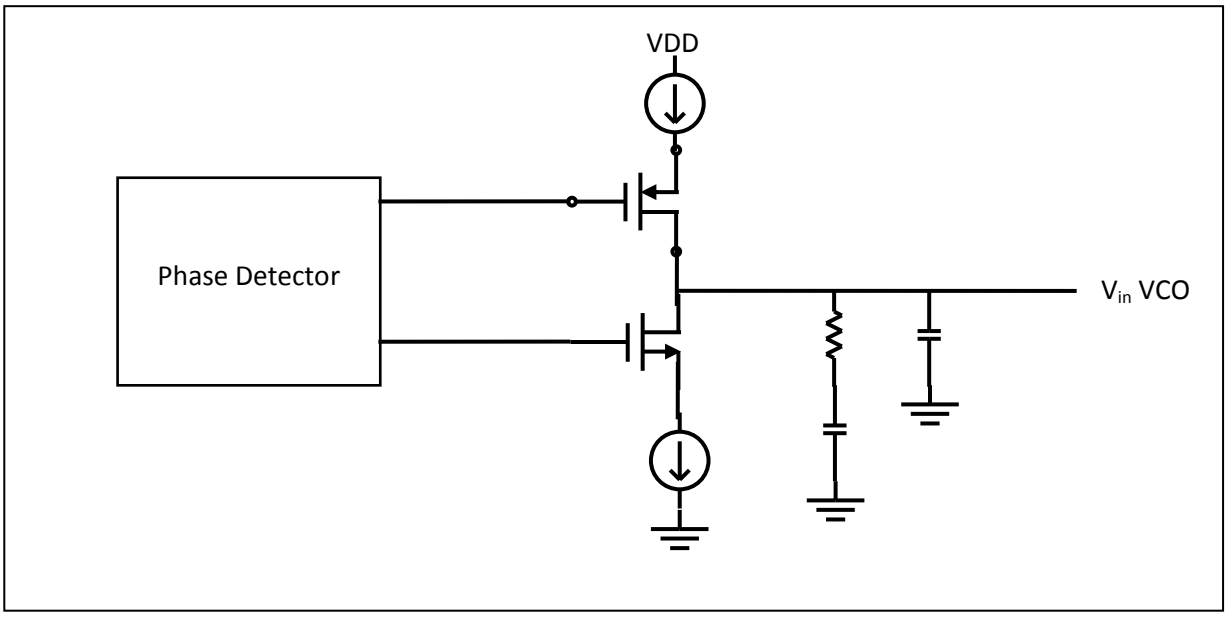

Figure 24. Charge Pump Schematic

The operation of the charge pump can be understood as follows. When UP signal is high and the DOWN signal is low, the transistor M1 will switch on. On the other hand, when the

DOWN signal is high and the UP signal is low, then M2 is ON and M1 is off, thus the current in the circuit will be less.

For multi gigabit CDR circuits, a current steering differential charge pump is generally used [13].Current steering charge pumps operate at very higher frequencies compared to charge pumps that use static logic. Differential charge pumps help to reduce the common mode noise. The schematic of a differential current steering charge pump is shown in Fig.25.

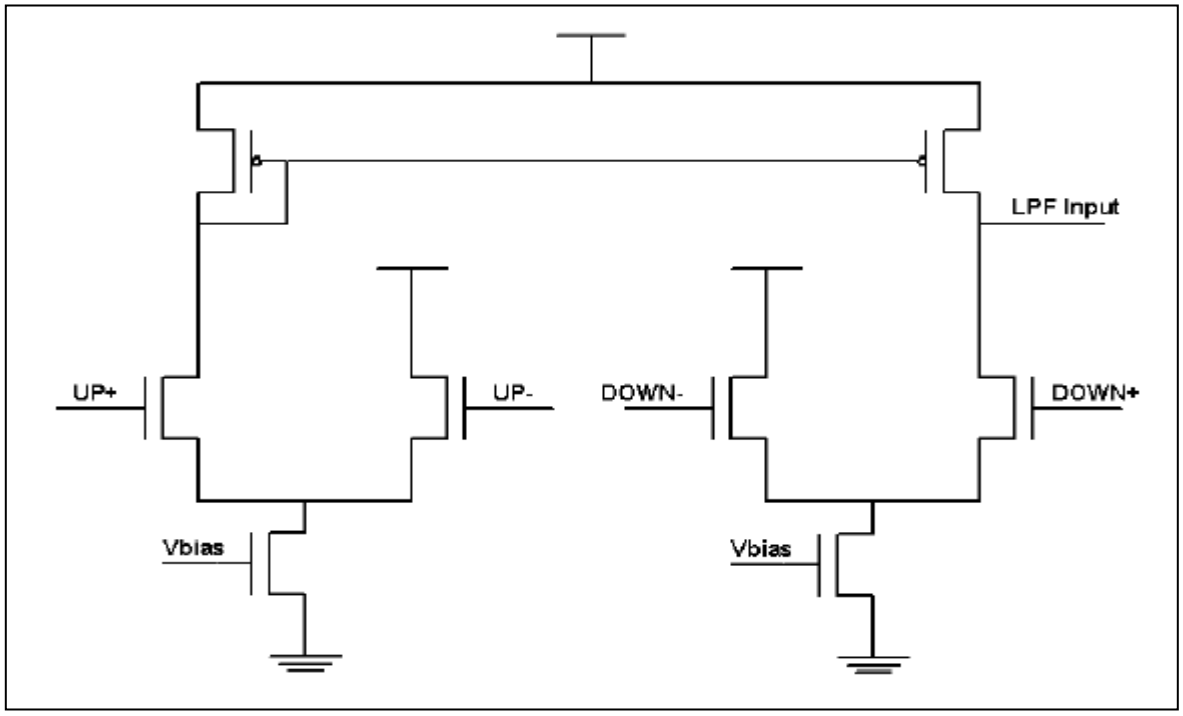

Figure 25. Schematic of the Differential Current Steering Charge Pump[13]

6.6 LC Voltage Controlled Oscillator

A voltage controlled oscillator (VCO) is a circuit whose output is a signal that oscillates at a particular frequency for a fixed control voltage. There are various types of VCOs that have been studied in various papers. The commonly used monolithic VCOs are ring oscillator type VCOs and LC VCOs. Ring oscillator type VCOs have more phase noise than LC VCOs and thus have more output jitter. At higher frequency of operation, the phase noise of a ring oscillator type VCO is unacceptable for CDR circuits. The VCO implemented in this design is an LC VCO. An LC tank has been shown in Fig.26.

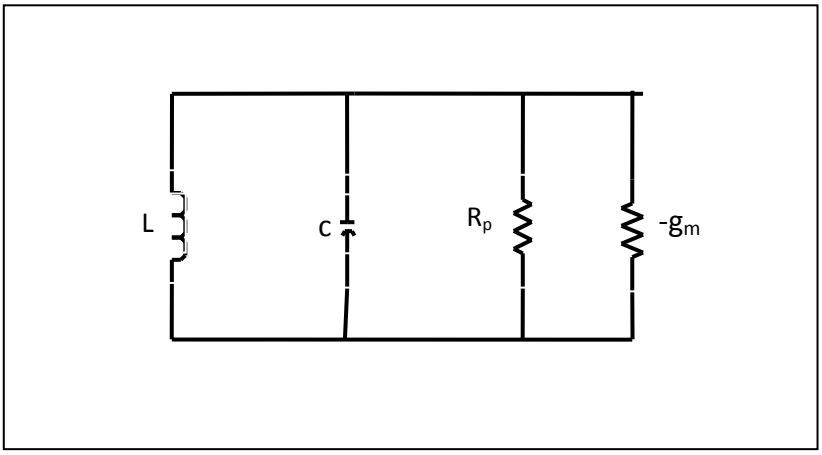

Figure 26. LC Tank

The oscillator consists of an inductor and a capacitor which can be seen as a parallel resonance tank. For a LC VCO to have sustained oscillation the following condition needs to be met.

$$g_m > \frac{1}{R_p} \text{.....(11)}$$

The natural frequency of oscillations of a LC VCO is given as

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \text{.....(12)}$$

It can be seen from the above equation that the frequency of oscillation can be changed the values of either the capacitor or the inductor. Since the value of inductors cannot be changed as a function of voltage easily, hence, varactors or variable capacitors are used to change the

frequency of oscillation of the VCO for different control voltages. Varactors can be realized in CMOS technology by connecting the FET as a diode [14]. There are two methods to connect a FET as a diode. The first method is to connect the source, drain and bulk of a FET. The voltage is applied across the gate and the body, souce and bulk connected together. The control voltage has to be kept below the weak inversion so that the capacitance keeps reducing with increase in control voltage. Figure 27 shows the capacitance variation of such a varactor with increase in control voltage.

The other method to realize varactors using FETs is to apply the control voltage to the gate and the bulk only while the source and the drain are kept unconnected. This type of varactor is known as accumulation varactor. The variation of capacitance with increase in voltage for such a varactor is shown in Fig.28.

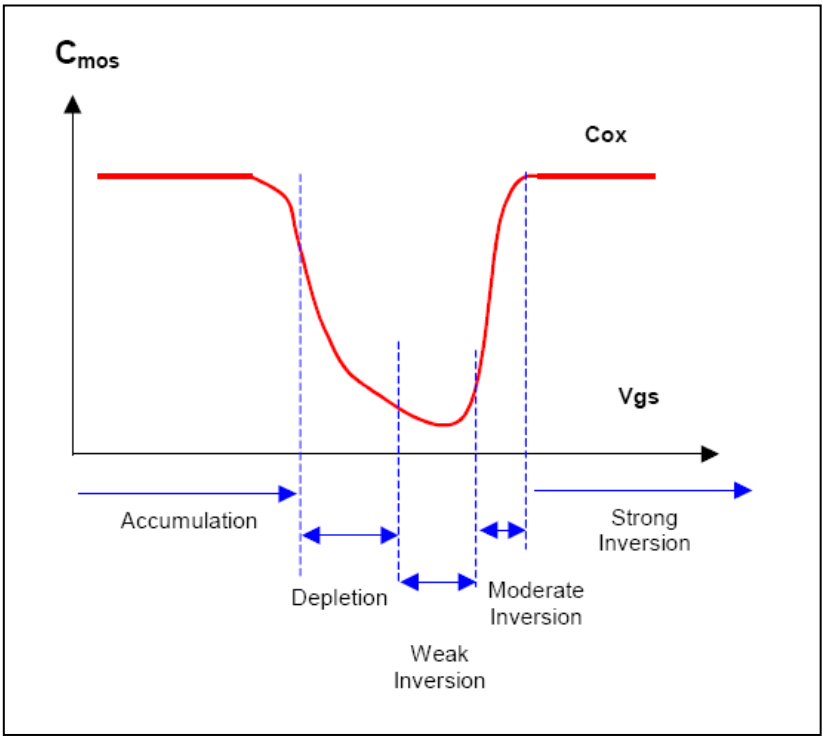

Figure 27. Depletion Type Varactor Capacitance [14]

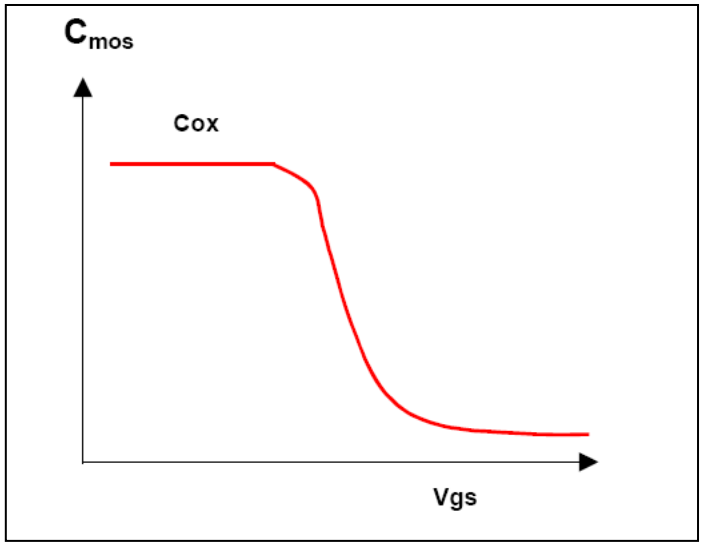

Figure 28. Accumulation type varactor [14]

For this research the first method of connecting the source, bulk and drain and applying a reverse bias voltage across the gate and the connected source, bulk and drain is used as varactor.

The LC VCO used in this research is not a perfectly optimized LC tank oscillator. It is a LC VCO with reasonable phase noise. The architecture of the LC VCO is shown in Fig.29. Transistors M1 and M2 form a cross coupled differential pair to provide the negative resistance that is essential for oscillation.

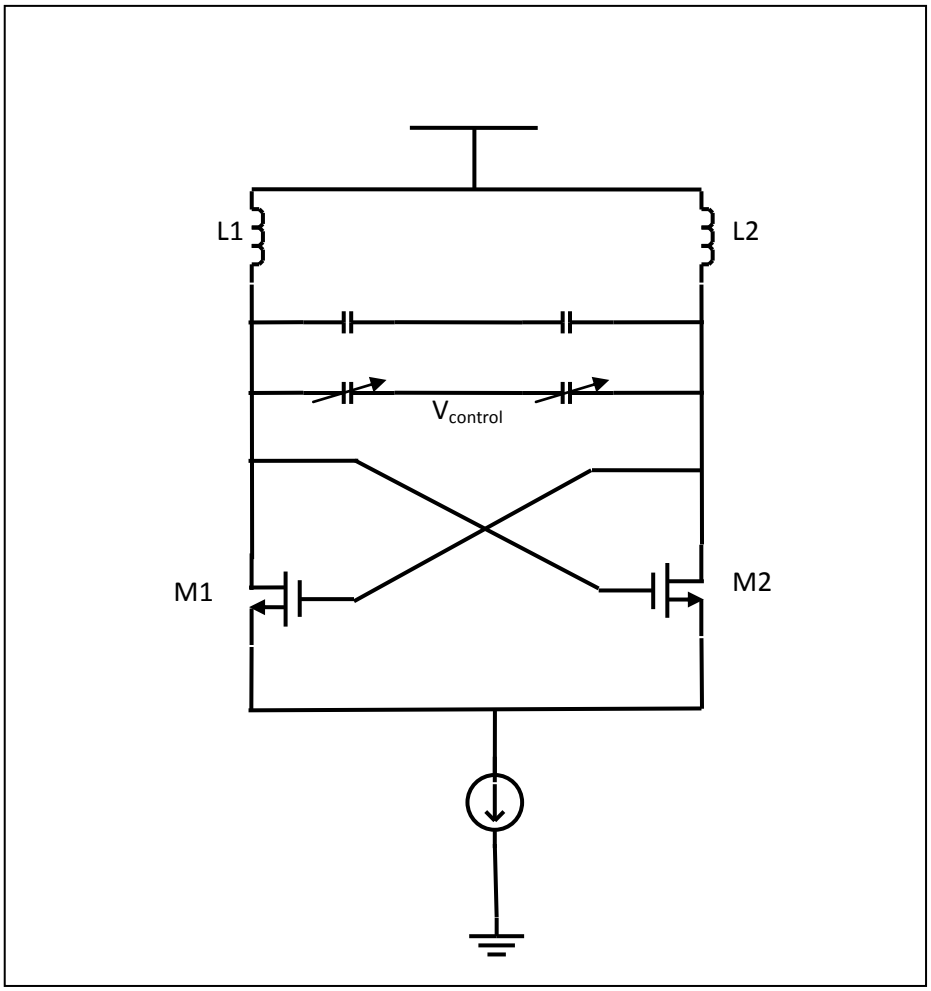

Figure 29. LC VCO Core schematic

6.7 Implementation of Delay Cells

The delay cells in the proposed phase detector have been implemented using a series of inverters since the delays are not very critical for operation of the phase detector. The delays can be controlled for temperature and process variations. The schematic of the delay cells in shown in Fig.30.

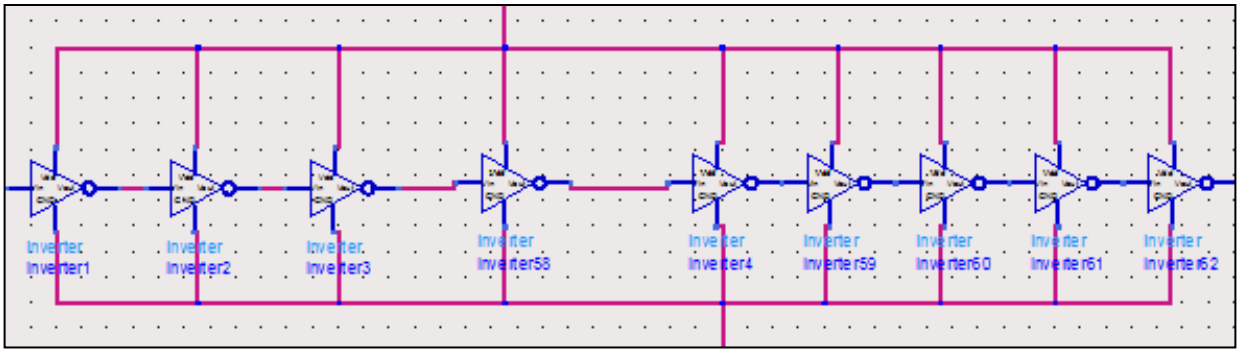

Figure 30. Implementation of Delay Cells

6.5 Hogge Phase Detector Implementation

To compare the results of the proposed linear phase detector with the popular linear phase detectors a Hogge phase detector isimplemented. The schematic of the Hogge phase detector is shown in Fig.31. The operation of the Hogge phase detector is explained in chapter 4 of this thesis.

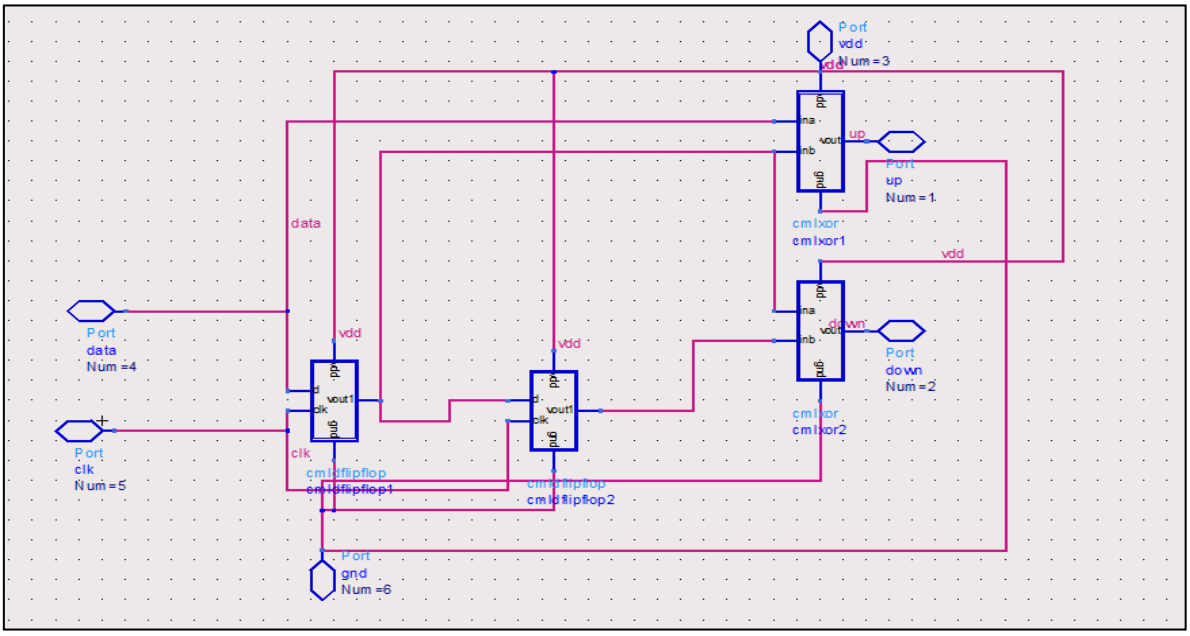

Figure 31. Implementation of the Hogge Phase Detector

Chapter 7. Results

For testing the two CDR systems, two CDR circuits were implemented in Agilent ADS using a standard 0.18 CMOS process and simulated to see the output jitter in both the circuits. In the first CDR, the proposed phase detector was used and in the second CDR the Hogge phase detector was used. The data rate for both the CDRs was 2Gbps/s. The peak-to-peak jitter and random jitter was measured in both the cases for the same time period. Figure 32 and Fig.33 show the recovered clock eye diagram of the CDR systems with the proposed phase detector and the Hogge phase detector respectively. Figure 34 shows the jitter histograms for the first CDR systems that uses the proposed phase detector and Fig.35 shows the eye histogram of CDR system using the Hogge phase detector with random NRZ type data.

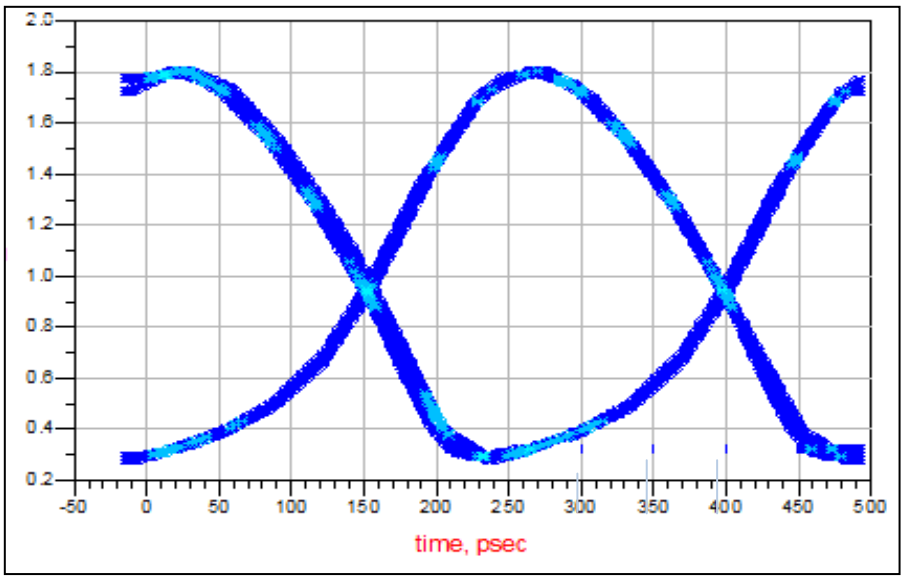

Figure 32. Recovered clock eye diagram with proposed phase detector

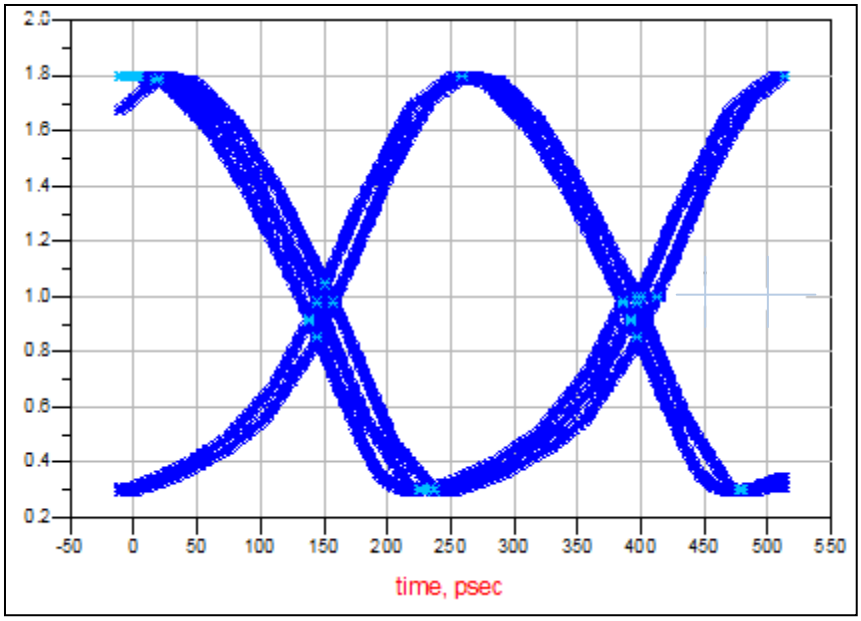

Figure 33. Recovered clock eye diagram with Hogge phase detector

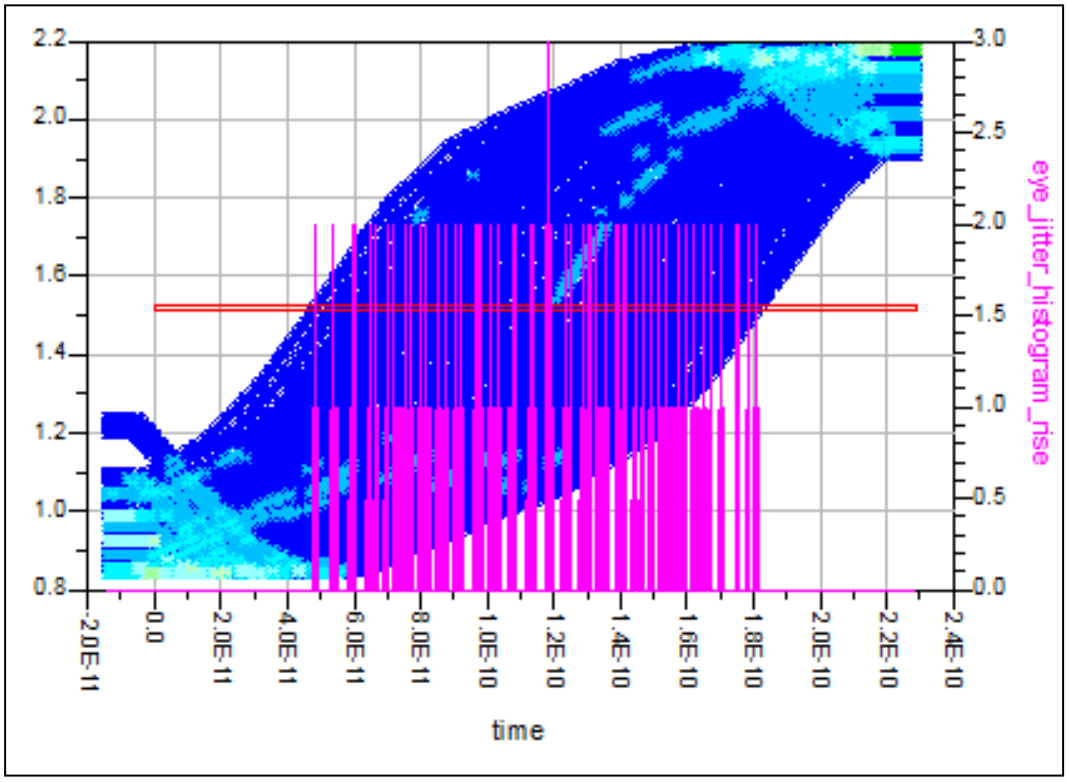

Figure 34. Eye jitter histogram of proposed phase detector

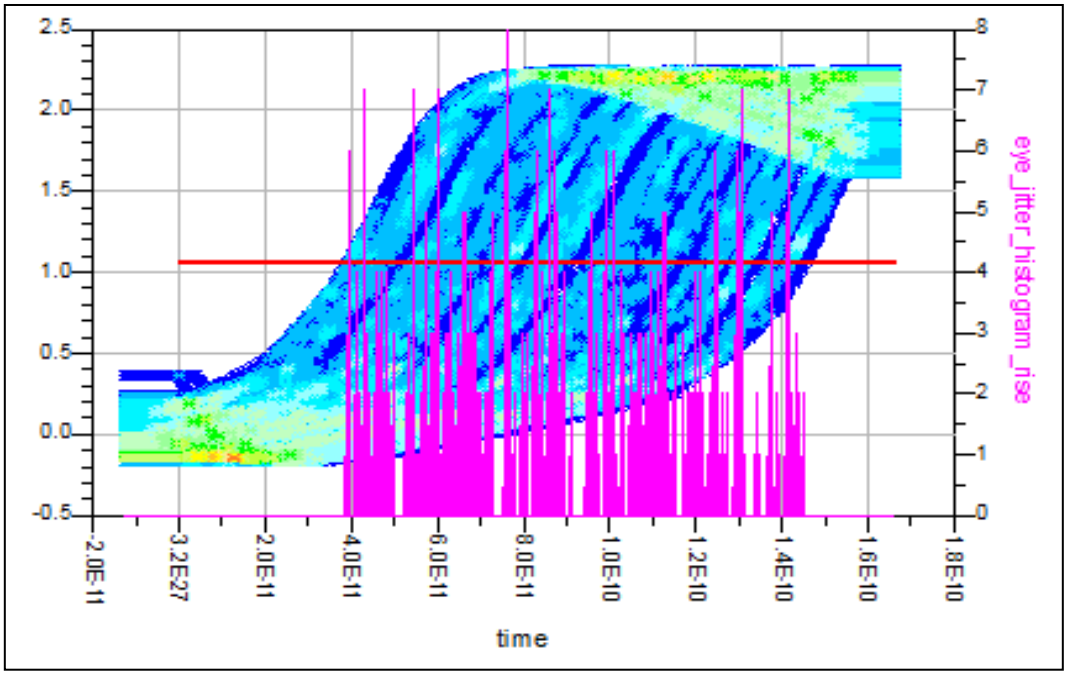

Figure 35. Eye jitter histogram with Hogge phase detector

The peak-to-peak jitter and rms jitter in both the cases have been tabulated in Table 3.

Observed Jitter	CDR with Hogge Phase Detector	CDR with Proposed Phase Detector
Eye Jitter (P-P)	28.13*E-12	20*E-12
Eye Jitter (RMS)	9*E-12	6.004*E-12

Table 3. Observed Jitter In the two CDR circuits

The recovered data eye diagrams for the CDR circuit using the proposed phase detector and the Hogge phase detector are shown in Fig.36 and Fig.37 respectively.

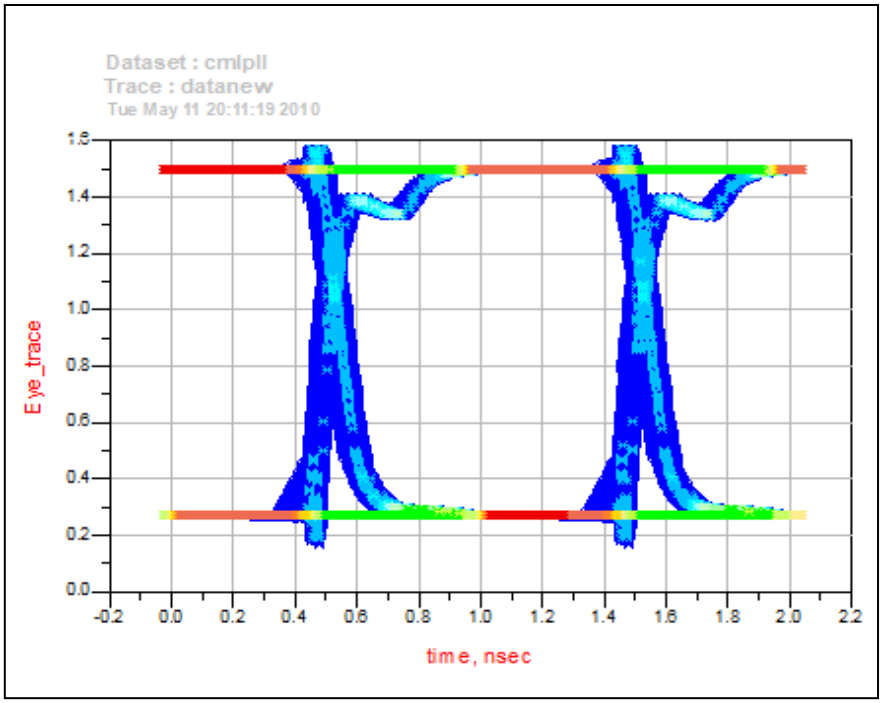

Figure 36. Recovered data eye diagrams with proposed phase detector

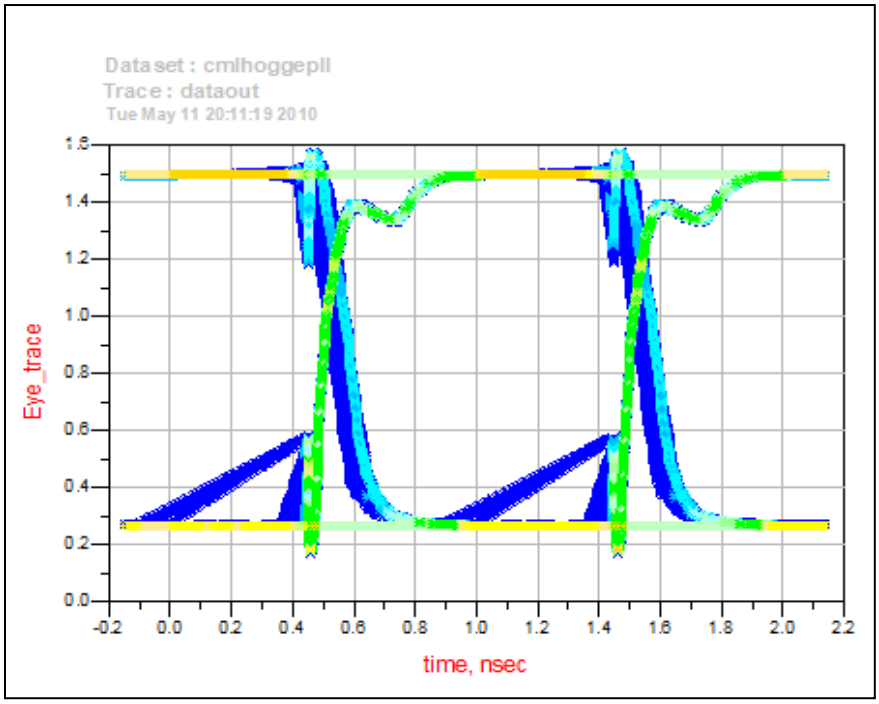

Figure 37. Recovered data eye diagram with Hogge phase detector

The output jitter in the recovered data is tabulated in table 4.

Observed Jitter	CDR with Hogge Phase Detector	CDR with Proposed Phase Detector
Eye Jitter (P-P)	35e-12	24E-12
Eye Jitter (RMS)	18E-12	14E-12

Table 4. Recovered data jitter

7.1 Conclusions

A new phase detector has been proposed in this thesis. The proposed phase detector does not use any sequential elements and thus eliminates metastability issues in CDR circuits. The proposed phase detector works with an LC type VCO. The proposed phase detector has a better jitter performance than a conventional linear phase detector such as the Hogge phase detector for random NRZ type data. The measured jitter in the proposed circuit is very less compared to similar architectures but it cannot be assumed to be exact because BSIM models have been used for simulations and also because the data input to this CDR circuit is not noisy and jittered as in real high speed communication circuits.

7.2 Future Research

The CDR circuit described in this thesis used BSIM 3.1 spice parameters for the MOSFET models. For further research, this CDR circuit should be simulated with a process development kit and the chip fabricated. The robustness of the proposed phase detector should be observed with various types of incoming data and the jitter in the circuit should be measured using industry standard equipments.

The LC VCO that is used in this research is not optimized for low phase noise. The VCO that should be used in future CDR circuits should have an optimized LC VCO for the low phase noise.

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Appendix

BSIM version 3.1 models for TSMC 0.18µ process are given in Table 5 and Table 6 for PMOS and NMOS respectively.

```
.MODEL CMOSP PMOS (
        LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 4.1589E17      VTH0    = -0.3823437
+K1      = 0.5722049      K2      = 0.0219717      K3      = 0.1576753
+K3B     = 4.2763642      W0      = 1E-6           NLX     = 1.104212E-7
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 0.6234839      DVT1    = 0.2479255      DVT2    = 0.1
+U0      = 109.4682454    UA      = 1.31646E-9     UB      = 1E-21
+UC      = -1E-10         VSAT    = 1.054892E5     A0      = 1.5796859
+AGS     = 0.3115024      B0      = 4.729297E-7    B1      = 1.446715E-6
+KETA    = 0.0298609      A1      = 0.3886886      A2      = 0.4010376
+RDSW    = 199.1594405    PRWG    = 0.5            PRWB    = -0.4947034
+WR      = 1              WINT    = 0              LINT    = 2.93948E-8
+XL      = 0              XW      = -1E-8          DWG     = -1.998034E-8
+DWB     = -2.481453E-9   VOFF    = -0.0935653     NFACTOR = 2
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 3.515392E-4    ETAB    = -4.804338E-4
+DSUB    = 1.215087E-5    PCLM    = 0.96422        PDIBLC1 = 3.026627E-3
+PDIBLC2 = -1E-5          PDIBLCB = -1E-3          DROUT   = 1.117016E-4
+PSCBE1  = 7.999986E10    PSCBE2  = 8.271897E-10   PVAG    = 0.0190118
+DELTA   = 0.01           RSH     = 8.1            MOBMOD  = 1
+PRT     = 0              UTE     = -1.5           KT1     = -0.11
+KT1L    = 0              KT2     = 0.022          UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11       AT      = 3.3E4
+WL      = 0              WLN     = 1              WW      = 0
+WWN     = 1              WWL     = 0              LL      = 0
+LLN     = 1              LW      = 0              LWN     = 1
+LWL     = 0              CAPMOD  = 2              XPART   = 0.5
+CGDO    = 7.82E-10       CGSO    = 7.82E-10       CGBO    = 1E-12
+CJ      = 1.214428E-3    PB      = 0.8461606      MJ      = 0.4192076
+CJSW    = 2.165642E-10   PBSW    = 0.8            MJSW    = 0.3202874
+CJSWG   = 4.22E-10       PBSWG   = 0.8            MJSWG   = 0.3202874
+CF      = 0              PVTH0   = 5.167913E-4    PRDSW   = 9.5068821
+PK2     = 1.095907E-3    WKETA   = 0.0133232      LKETA   = -3.648003E-3
+PU0     = -1.0674346     PUA     = -4.30826E-11   PUB     = 1E-21
```

Table 5. BSIM parameters for TSMC 0.18 micron process (PMOS) [17]

```
.MODEL CMOSN NMOS (                                    LEVEL   = 49
+VERSION = 3.1            TNOM    = 27                 TOX     = 4.1E-9
+XJ      = 1E-7           NCH     = 2.3549E17          VTH0    = 0.3694303
+K1      = 0.5789116      K2      = 1.110723E-3        K3      = 1E-3
+K3B     = 0.0297124      W0      = 1E-7               NLX     = 2.037748E-7
+DVT0W   = 0              DVT1W   = 0                  DVT2W   = 0
+DVT0    = 1.2953626      DVT1    = 0.3421545          DVT2    = 0.0395588
+U0      = 293.1687573    UA      = -1.21942E-9        UB      = 2.325738E-18
+UC      = 7.061289E-11   VSAT    = 1.676164E5         A0      = 2
+AGS     = 0.4764546      B0      = 1.617101E-7        B1      = 5E-6
+KETA    = -0.0138552     A1      = 1.09168E-3         A2      = 0.3303025
+RDSW    = 105.6133217    PRWG    = 0.5                PRWB    = -0.2
+WR      = 1              WINT    = 2.885735E-9        LINT    = 1.715622E-8
+XL      = 0              XW      = -1E-8              DWG     = 2.754317E-9
+DWB     = -3.690793E-9   VOFF    = -0.0948017         NFACTOR = 2.1860065
+CIT     = 0              CDSC    = 2.4E-4             CDSCD   = 0
+CDSCB   = 0              ETA0    = 2.665034E-3        ETAB    = 6.028975E-5
+DSUB    = 0.0442223      PCLM    = 1.746064           PDIBLC1 = 0.3258185
+PDIBLC2 = 2.701992E-3    PDIBLCB = -0.1               DROUT   = 0.9787232
+PSCBE1  = 4.494778E10    PSCBE2  = 3.672074E-8        PVAG    = 0.0122755
+DELTA   = 0.01           RSH     = 7                  MOBMOD  = 1
+PRT     = 0              UTE     = -1.5               KT1     = -0.11
+KT1L    = 0              KT2     = 0.022              UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11           AT      = 3.3E4
+WL      = 0              WLN     = 1                  WW      = 0
+WWN     = 1              WWL     = 0                  LL      = 0
+LLN     = 1              LW      = 0                  LWN     = 1
+LWL     = 0              CAPMOD  = 2                  XPART   = 0.5
+CGDO    = 8.58E-10       CGSO    = 8.58E-10           CGBO    = 1E-12
+CJ      = 9.471097E-4    PB      = 0.8                MJ      = 0.3726161
+CJSW    = 1.905901E-10   PBSW    = 0.8                MJSW    = 0.1369758
+CJSWG   = 3.3E-10        PBSWG   = 0.8                MJSWG   = 0.1369758
+CF      = 0              PVTH0   = -5.105777E-3       PRDSW   = -1.1011726
+PK2     = 2.247806E-3    WKETA   = -5.071892E-3       LKETA   = 5.324922E-4
+PU0     = -4.0206081     PUA     = -4.48232E-11       PUB     = 5.018589E-24
```

Table 6. BSIM parameters for TSMC 0.18 micron process (NMOS) [17]