

© 2021 IEEE. Personal use of this material is permitted. Permission from IEEE must be obtained for all other uses, in any current or future media, including reprinting/republishing this material for advertising or promotional purposes, creating new collective works, for resale or redistribution to servers or lists, or reuse of any copyrighted component of this work in other works.

Digital Object Identifier [10.1109/ECCE47101.2021.9595289](https://doi.org/10.1109/ECCE47101.2021.9595289)

2021 IEEE Energy Conversion Congress and Exposition (ECCE)

Quasi-Reference PWM for 3-level Voltage Source Inverters

Anatolii Tcai

Thiwanka Wijekoon

Jun-Hyung Jung

Marco Liserre

Suggested Citation

A. Tcai, T. Wijekoon, J. -H. Jung and M. Liserre, "Quasi-Reference PWM for 3-level Voltage Source Inverters," 2021 IEEE Energy Conversion Congress and Exposition (ECCE), 2021.

Quasi-Reference PWM for 3-level Voltage Source Inverters

Anatolii Tcai, Thiwanka Wijekoon
Power Conversion Technologies
Huawei Technologies Düsseldorf, GmbH
 Nürnberg, Germany
 Email: anatolii.tcai@huawei.com

Jun-Hyung Jung, Marco Liserre
Chair of Power Electronics
Kiel University
 Kiel, Germany
 Email: {ml, jj}@tf.uni-kiel.de

Abstract—3-Level Voltage Source Inverters (3L-VSI) have emerged as effective approach to achieve high efficiency and better harmonic distortion performance. As a State-of-Art (SoA), two types of carrier arrangement methods are used for carrier-based pulse width modulation (PWM), namely, phase disposition (PD) and alternate phase opposite disposition (APOD). PD PWM gives better performance in terms of current quality and Total Harmonic Distortion (THD) whereas, APOD PWM is more effective for suppression of Common-Mode Voltage (CMV) with the expense of increased THD. In this paper, a novel Quasi-reference PWM method for 3L-VSIs is presented which results in low CMV as that of the APOD along with the reduced THD. The proposed method can be considered as a distinct trade-off between the two SoA methods, which maintains the merits of both. This paper presents the detail analysis and experimental verification of the proposed PWM technique.

Keywords—PWM inverters, common mode voltage, CMV, modulation techniques, multilevel inverter, t-type inverter, neutral-point-clamped inverter, VSI

I. INTRODUCTION

3-Level Voltage Source Inverters (3L-VSI) are the most commonly used multilevel converters. They have superior electrical performances compared to those of the conventional 2L-VSIs, but the implementation complexity and cost difference is not very prominent as compared to 2L-VSIs. 3L-VSIs overpass 2L-VSI in terms of the AC current quality, Common-Mode Voltage (CMV), semiconductor switching losses, DC capacitor stress etc [1]–[3]. Moreover, due to increased degrees of freedom, the operation methods of the 3L VSIs keep improving. 3L VSIs can be operated using two different ways of PWM carrier arrangements, namely Alternative Phase-Opposite Disposition (APOD) and Phase-Disposition (PD) [4], [5]. Both ways provide different performance and thus, being selected upon the requirement of a particular application. The former has much lower CMV, but higher Total-Harmonic Distortion (THD), whereas the latter has lower THD of the output current, but the CMV is increased in comparison to that of the APOD-PWM [6], [7]. Therefore, the 3L-VSI utilizing the APOD-PWM requires decreased insulation requirement and smaller CMV choke filter, while the output filter size will be significantly increased compared to that of the PD-PWM due to higher THD of the output current. However, this method of carrier arrangement is preferred to be used in interleaved

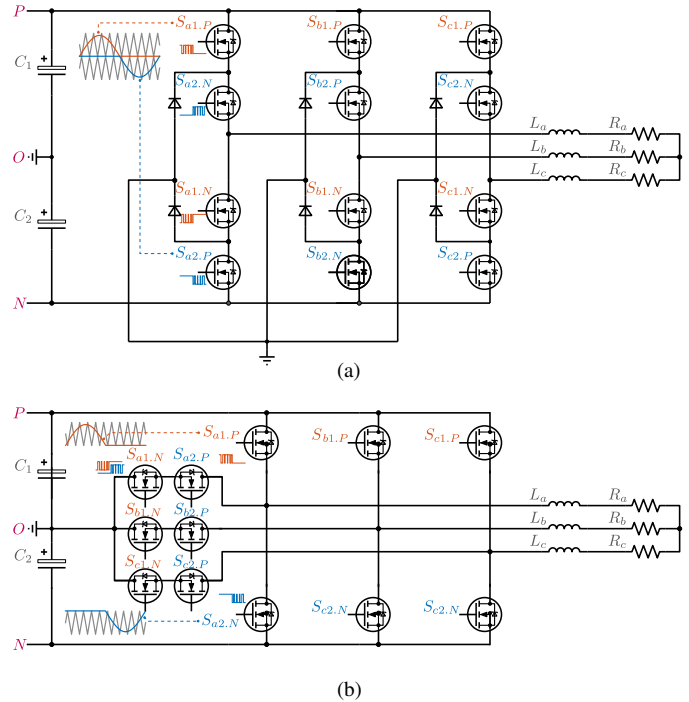


Fig. 1. Common 3L-VSI topologies with passive RL load. (a) Neutral-Point Clamped 3L-VSI and (b) T-Type 3L-VSI.

operation of parallel 3L-VSIs, owing to decreased amplitude of the CMV, resulting in lower circulating current among the inverters [8].

Recently, a trend of double signal Pulse-Width Modulation methods has been investigated [9], [10]. It provides capability to improve the performance of 3L VSIs in terms of neutral point balancing or decreased CMV. The idea is to generate overlapping symmetrical reference signals for both upper carrier wave and lower carrier wave. The overlapping area then will contribute to the generation of additional PWM pulses to either balance the neutral point voltage [9] or to reduce the CMV of the VSI [10].

Quasi-Reference PWM (QR-PWM) method, proposed in this paper is derived using double signal PWM approach of generating the PWM output, however unlike the former methods, the latter generates reference signals in the middle

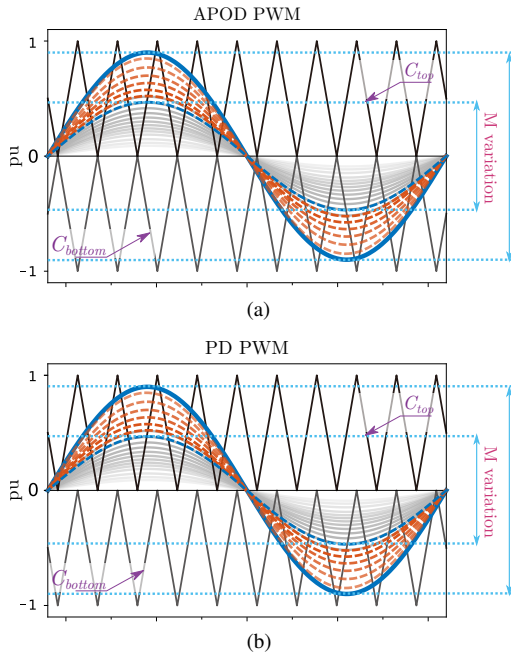


Fig. 2. Carrier arrangement of 3L-VSI. Blue solid line shows $M = 0.9$, dashed orange lines represent $0.5 < M < 0.9$, blue dashed line shows $M = 0.5$ and grey lines show values of $M < 0.5$. (a) APOD PWM and (b) PD PWM.

of each carrier wave and has relatively low CMV as compared to that of the PD, while the THD of the output current is lower than that of the APOD. The performance of the proposed method is verified via harmonic analysis and experiments.

II. STATE OF ART PD AND APOD MODULATIONS

Fig.1 shows 3L Neutral-Point Clamped (NPC) VSI and 3L T-Type VSI with a passive LR load attached at the AC output. 3-phase sine-wave AC current is achieved by providing power switches S_{x1} and S_{x2} ($x = a, b, c$) with the PWM signals, where $S_{x1,P}$ and $S_{x1,N}$ are complementary signals as well as signals $S_{x2,P}$ and $S_{x2,N}$.

As is shown in Fig. 2, sine-wave reference signals are being compared with two high frequency triangular carriers, upper carrier and lower carrier, generating two sets of PWM signals, which in turn are applied to 4 power switches of each phase.

The harmonic solution V_{2L} for a single phase of 2L-VSI can be expressed in terms of its harmonic components

$$\begin{aligned}
 V_{2L} &= V_{dc}M \cos(\omega_o + \theta_o) \\
 &+ \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_0\left(m\frac{\pi}{2}M\right) \sin m\frac{\pi}{2} \cos(m[\omega_c + \theta_c]) \\
 &+ \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_n\left(m\frac{\pi}{2}M\right) \sin\left([m+n]\frac{\pi}{2}\right) \\
 &\times \cos(m[\omega_c + \theta_c] + n[\omega_o + \theta_o]) \quad (1)
 \end{aligned}$$

where M – modulation index, ω_o and ω_c are angular values of the fundamental and the PWM frequencies, θ_o and θ_c are the initial angle of the aforementioned frequencies, J_n is n-

order Bessel function of the first kind, n and m are harmonic indices of the fundamental and carrier components.

In the equation above, the first term is the 1st harmonic of the fundamental, the first sum with the indice m is the switching frequency harmonic group and the last term is the sum of side-bands harmonics.

To obtain the harmonic expression for 3L-VSIs, V_{2L} with $\theta_o = 180^\circ$ should be subtracted from V_{2L} with $\theta_o = 0^\circ$. Due to the subtraction, for the APOD-PWM, θ_c should be equal for both equations, whereas in the case of PD-PWM, θ_c should have 180° difference. Like this, the carrier harmonic content for the APOD-PWM will be fully canceled out as

$$\begin{aligned}
 V_{apod.c} &= \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} J_0\left(m\frac{\pi}{2}M\right) \sin m\frac{\pi}{2} \\
 &\times [\cos(m[\omega_c + \theta_c]) - \cos(m[\omega_c + \theta_c])] = 0 \quad (2)
 \end{aligned}$$

After some manipulations, the harmonic expression of the output voltage of 3L-VSI using APOD-PWM is given below

$$\begin{aligned}
 V_{apod} &= 2V_{dc}M \cos \omega_o \\
 &+ \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_n(m\pi M) \sin\left(n\frac{\pi}{2}\right) \\
 &\times \cos(m\omega_c + n\omega_o) \quad (3)
 \end{aligned}$$

On the other hand, after similar manipulations, the harmonic expression of the 3L-VSI PD-PWM is expressed as

$$\begin{aligned}
 V_{pd} &= 2V_{dc}M \cos \omega_o \\
 &+ \frac{16V_{dc}}{\pi^2} \sum_{m=1}^{\infty} \frac{1}{m} \sum_{k=1}^{\infty} \frac{J_{2k-1}(m\pi M)}{2k-1} \sin m\frac{\pi}{2} \cdot \cos m\omega_c \\
 &+ \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{\sin\left([m+n]\frac{\pi}{2}\right)}{m} \\
 &\times \left[J_n(m\pi M) - \frac{4}{\pi} \sum_{k=1}^{\infty} J_{2k-1}(m\pi M) \frac{[2k-1] \cos\left(n\frac{\pi}{2}\right)}{[n+2k-1][n-2k+1]} \right] \\
 &\times \cos(m\omega_c + n\omega_o) \quad (4)
 \end{aligned}$$

Comparing the above expression, it is clear that the APOD-PWM does not have carrier harmonics components around $m\omega_c$, whereas in the case of the PD-PWM, the amplitude gain of such harmonics is $16V_{dc}/\pi^2$, which increases the amplitude of the CMV. The CMV of (3) and (4) can be evaluated by adding to each of the equations the same expressions with the added $\theta_o = -120^\circ$ and $\theta_o = 120^\circ$ and then by dividing the result by 3.

Due to the symmetry of the 3-phase sinusoidal systems, the fundamental harmonics will cancel out, however the side-bands will have eventually non-zero regions due to

$$\begin{aligned}
 &\cos(m\omega_c + n\omega_o) + \cos\left(m\omega_c - n\frac{2}{3}\pi + n\omega_o\right) \\
 &+ \cos\left(m\omega_c + n\frac{2}{3}\pi + n\omega_o\right) = \\
 &\left[1 + 2\cos\left(n\frac{2}{3}\pi\right)\right] \cdot \cos(m\omega_c + n\omega_o) \quad (5)
 \end{aligned}$$

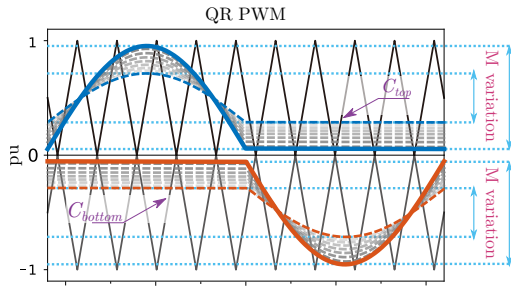


Fig. 3. Carrier arrangement of the proposed QR-PWM for 3L-VSI. Solid blue line shows upper reference signal at $M = 0.9$, dashed blue line represents upper reference signal at $M = 0.5$. Solid orange line is lower reference signal at $M = 0.9$, dashed orange line shows lower reference signal at $M = 0.5$. Grey dashed line represent the variation of M between 0.5 and 0.9.

In (5), the square brackets will be 0 for all values of n which are not multiples of 3.

Like this, the CMV of the APOD-PWM and PD-PWM can be derived. The DC-component and fundamental harmonics will be canceled out leaving only carrier harmonic components and side-bands. After some manipulations the expressions of the CMV for each modulation method will be

$$V_{\text{apod.cm}} = \frac{4V_{\text{dc}}}{3\pi} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_n(m\pi M) \sin\left(n\frac{\pi}{2}\right) \times \left[1 + 2\cos\left(n\frac{2}{3}\pi\right)\right] \cdot \cos(m\omega_c + n\omega_o) \quad (6)$$

$$V_{\text{pd.cm}} = \frac{16V_{\text{dc}}}{\pi^2} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{1}{m} J_{2k-1}(m\pi M) \sin\left(m\frac{\pi}{2}\right) \times \cos(m\omega_c) + \frac{16V_{\text{dc}}}{3\pi^2} \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{\sin\left([m+n]\frac{\pi}{2}\right)}{m} \times \left[\frac{\pi}{4} J_n(m\pi M) - \sum_{k=1}^{\infty} \frac{J_{2k-1}(m\pi M) \cdot [2k-1] \cos\left(n\frac{\pi}{2}\right)}{[n+2k-1][n-2k+1]}\right] \times \left[1 + 2\cos\left(n\frac{2}{3}\pi\right)\right] \cdot \cos(m\omega_c + n\omega_o) \quad (7)$$

Obviously, the CMV of PD-PWM has more harmonic components, especially around the carrier frequency ω_c for odd values of m , with prominent first-order harmonic due to the amplitude of the Bessel function $J(m\pi M)$. On the other hand, the APOD-PWM will have only side-bands at each index of the carrier frequency for fundamentals which are multiples of 3.

III. PROPOSED QR-PWM

The implementation of the proposed QR-PWM is shown in Fig. 3. The main idea is to use two half-sine waves as modulation signals and compare each of them with a triangular carrier using center symmetry, i.e. the middle points of modulation signals and triangular signals always match.

The detailed modulation principle of the QR-PWM is shown in Fig. 4 and Fig. 5 for the values of $M > 0.5$ and $M < 0.5$, respectively. The figures show that the output PWM waveform

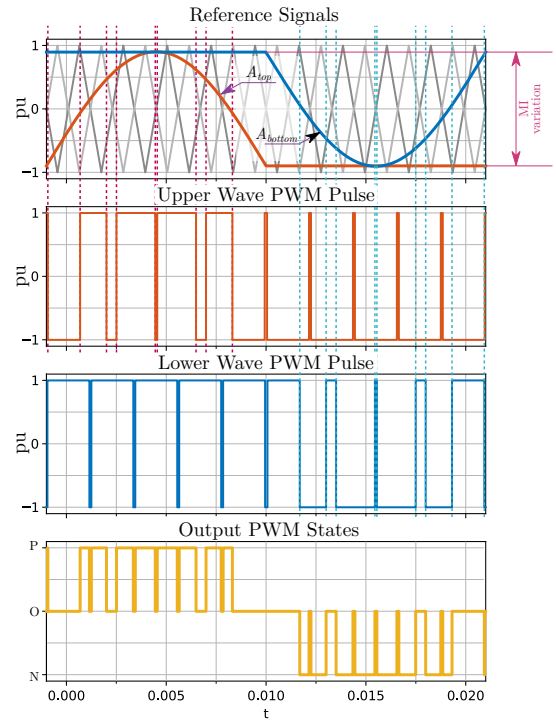


Fig. 4. QR-PWM modulating waveform for $M > 0.5$. Orange solid line represents upper reference and PWM signals and blue solid line shows the lower reference and PWM signals. The final PWM waveform is shown as yellow line.

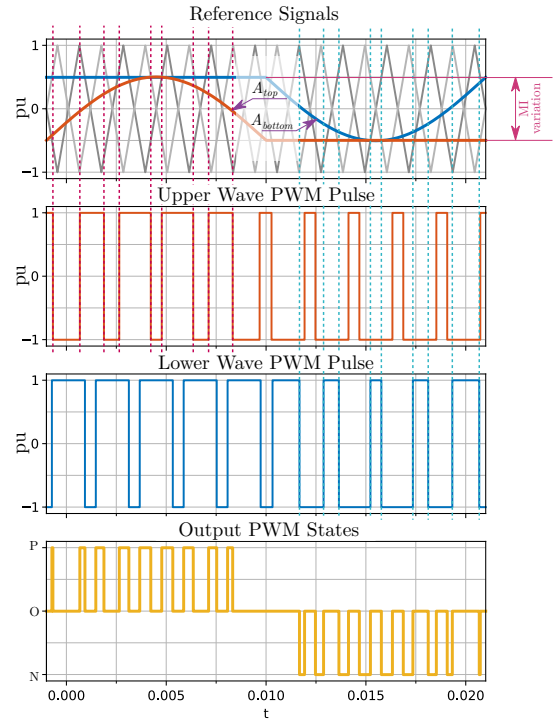


Fig. 5. QR-PWM modulating waveform for $M < 0.5$. Orange solid line represents upper reference and PWM signals and blue solid line shows the lower reference and PWM signals. The final PWM waveform is shown as yellow line.

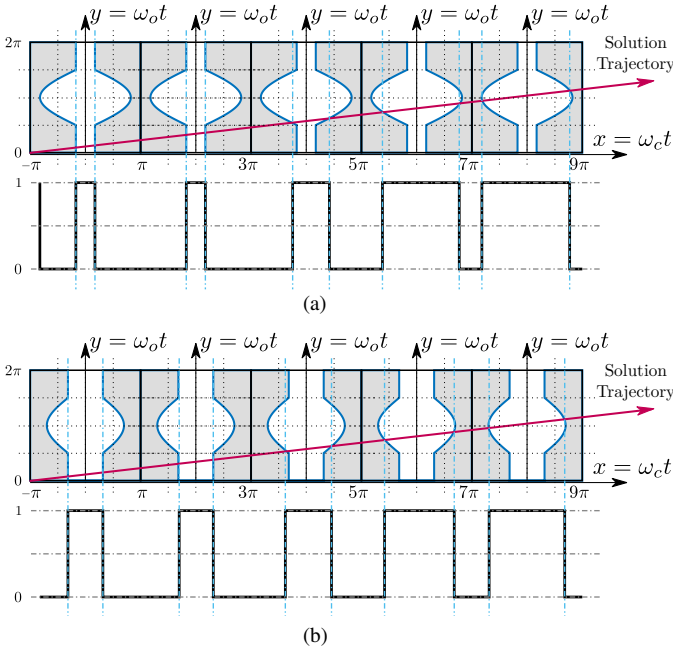


Fig. 6. Solution trajectory of the proposed QR-PWM for establishing limits of Double Fourier Integral. (a) $M > 0.5$ and (b) $M < 0.5$.

is generated as a superposition of the upper and the lower PWM pulses. It can be observed, that intermediate pulses are created in the areas at which the reference waveforms are flat, like that of the blue waveform in the left half of the figure or that of the orange waveform in the right half of the figure. These pulses increase the total switching count around the zero-crossing regions.

To derive harmonic expression of the proposed method, double-fourier integral needs to be solved with the integration limits given in Table I. The limits are derived using a unit-cell approach, which is well explained in [11]. The solution trajectory, required for the unit-cell approach is given in Fig.6. Fig.6(a) gives the example of unit-cell with high value of M , whereas Fig.6(b) shows the change of the unit-cell when the M is lower. The integral limits will not change for different values of the M .

The harmonic equation needs to be derived as a difference of two waveforms with different fundamental angles, as it was calculated for (3) and (4). A single carrier equation needs to be obtained first and then the same equation with 180° shifted fundamental angle to be subtracted from the former part. The final expression of the QR-PWM voltage output is:

$$\begin{aligned}
 V_{qr} = & 2V_{dc}M \cos(\omega_o) - \frac{8V_{dc}}{\pi} [1 - M] \sum_{n=1}^{\infty} \frac{\sin\left(n\frac{\pi}{2}\right)}{n} \cos(n\omega_o) \\
 & + \frac{4V_{dc}}{\pi} \sum_{m=1}^{\infty} \frac{1}{m} \sum_{n=-\infty}^{\infty} \sin\left(n\frac{\pi}{2}\right) \\
 & \times \left[J_n(m\pi M) - \frac{2}{n} \sin(m\pi[1 - M]) \right] \cdot \cos(m\omega_c + n\omega_o)
 \end{aligned} \quad (8)$$

TABLE I
DOUBLE FOURIER INTEGRAL LIMITS

$Y_s(i)$	$Y_e(i)$	$X_r(i)$ rising edge	$X_f(i)$ falling edge
$\frac{\pi}{2}$	π	$-\pi(1 - M)/2$	$\pi(1 - M)/2$
$-\frac{\pi}{2}$	$\frac{\pi}{2}$	$-\frac{\pi}{2}([2M - 1] \cos y + [1 - M])$	$\frac{\pi}{2}([2M - 1] \cos y + [1 - M])$
$-\pi$	$-\frac{\pi}{2}$	$-\pi(1 - M)/2$	$\pi(1 - M)/2$

It can be seen, that the CMV of the QR-PWM does not have carrier harmonic components, similar to (3), resulting in lower CMV as compared to that of the PD. On the other hand, the side-band harmonics of the QR-PWM are lower than those of the APOD.

The CMV of the QR-PWM voltage output is calculated using the same principle as for the previous cases. The final equation is then derived:

$$\begin{aligned}
 V_{qr,cmv} = & \frac{4V_{dc}}{3\pi} \sum_{m=1}^{\infty} \frac{1}{m} \sum_{n=-\infty}^{\infty} \sin\left(n\frac{\pi}{2}\right) \left(1 + 2 \cos\left(n\frac{2}{3}\pi\right)\right) \\
 & \times \left[J_n(m\pi M) - \frac{2}{n} \sin(m\pi[1 - M]) \right] \cdot \cos(m\omega_c + n\omega_o) \\
 & - \frac{8V_{dc}}{3\pi} [1 - M] \sum_{n=1}^{\infty} \frac{\sin\left(n\frac{\pi}{2}\right)}{n} \left(1 + 2 \cos\left(n\frac{2}{3}\pi\right)\right) \cos(n\omega_o)
 \end{aligned} \quad (9)$$

As in the previous case, there is no carrier harmonics components. Therefore, the CMV does not have prominent periodical voltage spikes like those of the PD. On the other hand, the side-bands of the QR-PWM are similar in amplitude to those of the APOD. This concept can be further improved by injecting third-harmonic offsets or implementing discontinuous modulation.

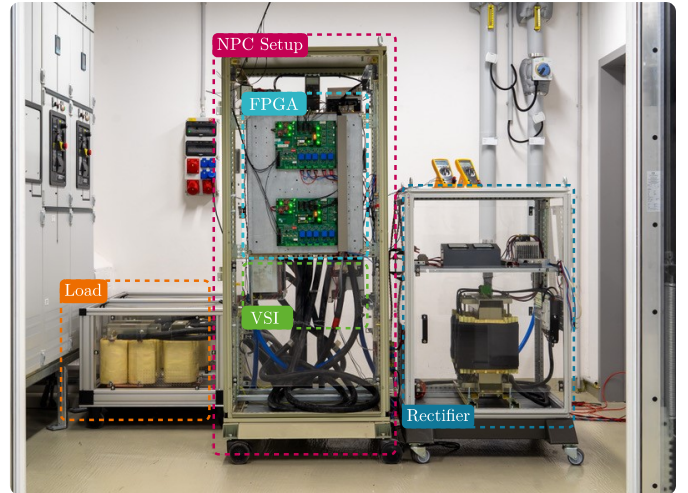


Fig. 7. Experimental setup of NPC 3L-VSI, operated from Spartan-3 FPGA unit with implemented modulation methods considered in this work.

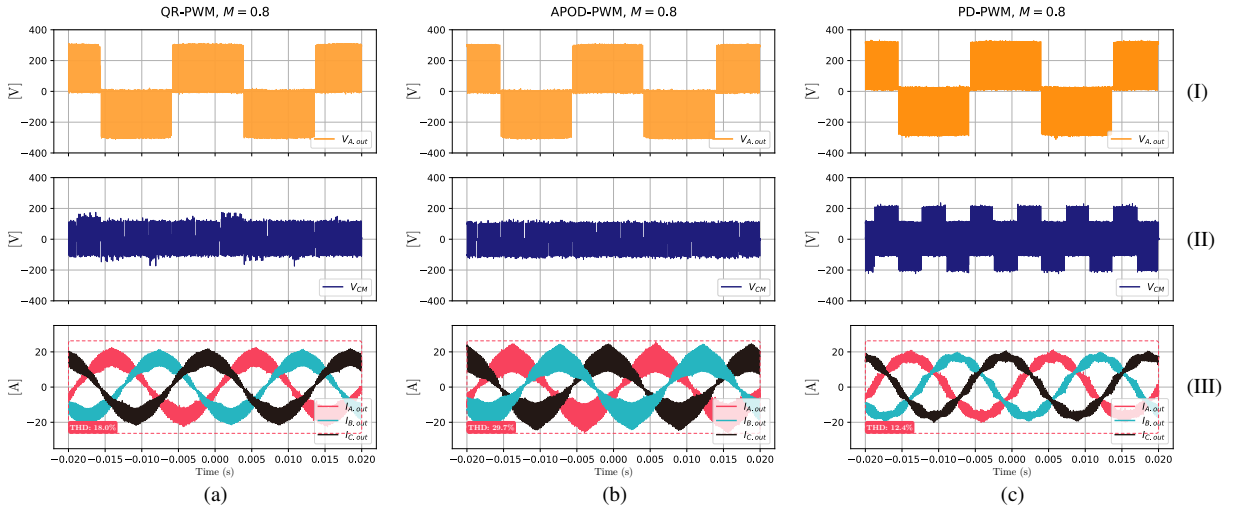


Fig. 8. Experimental results of the compared modulation methods. The line-voltage output (I), CMV (II), and output currents (III). (a) QR-PWM, (b) APOD-PWM and (c) PD-PWM at modulation index $M = 0.8$.

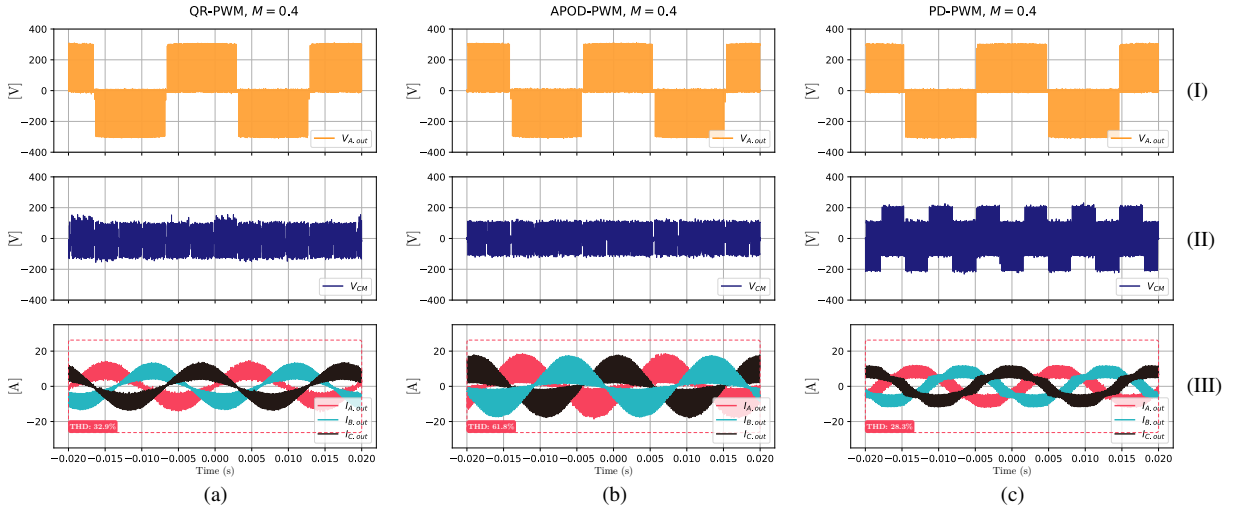


Fig. 9. Experimental results of the compared modulation methods. The line-voltage output (I), CMV (II), and output currents (III). (a) QR-PWM, (b) APOD-PWM and (c) PD-PWM at modulation index $M = 0.4$.

IV. EXPERIMENTAL RESULTS

The performance of the investigated methods is validated on an NPC 3L-VSI experimental setup shown in Fig. 7. The modulation references and PWM outputs are generated in Spartan-3 FPGA. The experiment parameters are provided in Table II.

Fig. 8 and Fig. 9 show the experimental results for the three considered modulations at $M = 0.8$ and $M = 0.4$, respectively. As shown, the CMV of the QR-PWM has the same amplitude as that of the APOD-PWM, while the CMV of the PD-PWM has periodic prominent voltage spikes at doubled amplitude due to the carrier-harmonic components, which were discussed in the previous section. Furthermore, the output current quality is the highest when using the PD-PWM and is only 12.4% at higher value of M and 28.3% at lower M , while APOD-PWM has the lowest performance quality between the all methods of 29.7% and 61.5%, accordingly. It

is more than doubled as compared to that of APOD-PWM. In contrast, the QR-PWM offers a trade-off between the two State-of-art methods with the THD being only 18% and 32.9% for the considered modulation indexes.

The FFT comparison of the CMVs for the three modulation methods at $M = 0.8$ is given in Fig. 10. The first thing to notice is that both QR-PWM and APOD-PWM do not have a carrier harmonic components, whereas PD-PWM has a prominent harmonic peak in the 1st order band. Moreover, the carrier harmonics appear in the odd-multiples of the switching frequency, which is the reason of earlier mentioned voltage spikes with doubled amplitude. The amplitude of the CMV harmonics of the other two methods is determined only by the side-band components and as the result, the amplitude of the CMV is reduced as compared to that of the PD-PWM. Furthermore, in the case of the proposed QR-PWM the even-order harmonics are insufficient, as is clearly pointed at Fig. 10 with dashed orange lines.

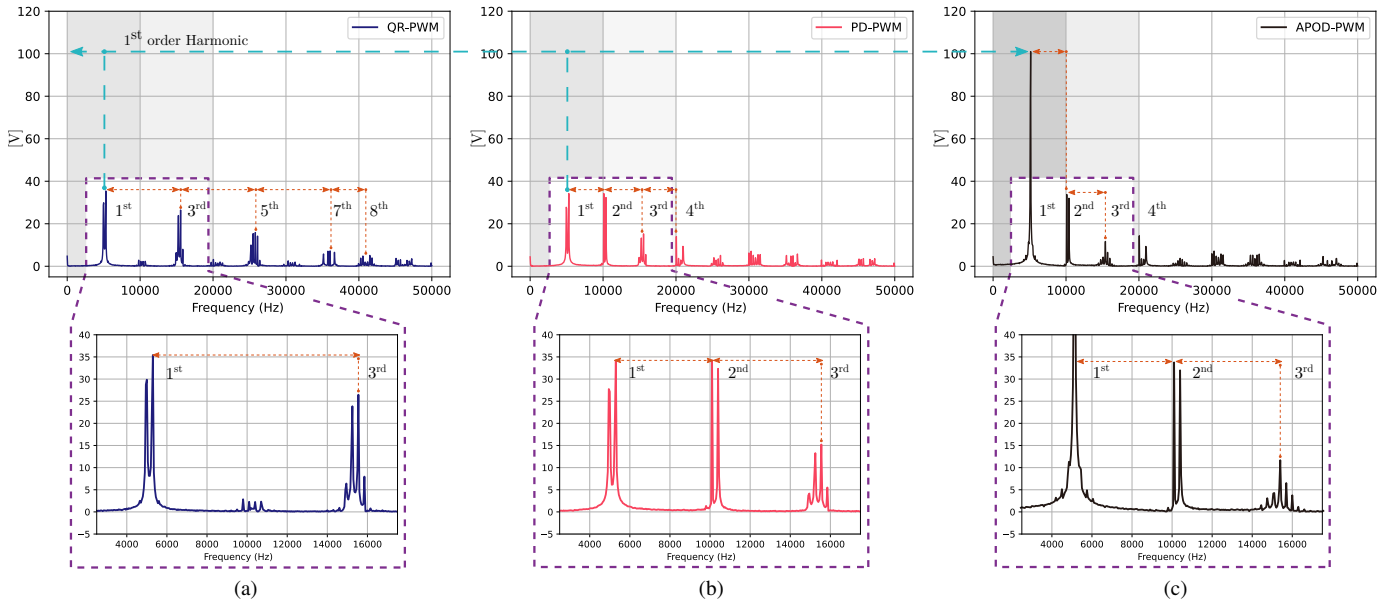


Fig. 10. FFT comparison of the CMVs of the three methods at $M = 0.8$. (a) QR-PWM, (b) APOD-PWM and (c) PD-PWM.

TABLE II
SYSTEM PARAMETERS OF NPC 3L-VSI.

Symbol	Description	Value
f_{sw}	Switching frequency	5 kHz
f_o	Fundamental frequency	50 Hz
V_{dc}	DC-link voltage	600 V
L	Load inductance	0.3 mH
R	Load resistance	10 Ω
C_{dc}	DC-link capacitance	2 mF

V. CONCLUSION AND FUTURE WORK

3-level Voltage Source Inverters (3L-VSI) have more degrees of freedom due to increased number of power switches and voltage levels as compared to 2-level VSIs. State-of-Art Pulse-Width Modulation (PWM) methods, such as Phase Disposition (PD) and Alternative Phase-Opposite Disposition (APOD) offer low Total Harmonic Distortion (THD) for the former and low Common-Mode Voltage (CMV) for the latter. Either of the PWM methods can be used depending on application needs. On the other hand, the proposed Quasi-Reference PWM (QR-PWM) can be considered as a trade-off between the two methods as it has CMV as low as that of the APOD and the THD value between those of the APOD and PD. The proposed method is not limited to 3L-VSI topologies, but can be further adapted for multilevel converters with different number of levels. Moreover, the proposed method

can be further improved with addition of various modulation techniques, such as third-harmonic injection or discontinuous operation. These possibilities will be investigated in future studies.

REFERENCES

- [1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: a survey of topologies, controls, and applications," *IEEE Transactions on Industrial Electronics*, vol. 49, no. 4, pp. 724–738, 2002.
- [2] U.-M. Choi, K.-B. Lee, and F. Blaabjerg, "Diagnosis and tolerant strategy of an open-switch fault for t-type three-level inverter systems," *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 495–508, 2014.
- [3] B. Wu, *High-Power Converters and AC Drives*, 2006.
- [4] B. Cougo, G. Gateau, T. Meynard, M. Bobrowska-Rafal, and M. Cousineau, "Pd modulation scheme for three-phase parallel multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 690–700, 2012.
- [5] B. McGrath and D. Holmes, "A comparison of multicarrier pwm strategies for cascaded and neutral point clamped multilevel inverters," in *2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, vol. 2, 2000, pp. 674–679 vol.2.
- [6] A. Tcai, S. Pugliese, and M. Liserre, "Comparison of modulation methods to reduce the circulating current in paralleled npc-converters with common dc-link," in *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1, 2019, pp. 5739–5745.
- [7] Z.-X. Zou, F. Hahn, S. Brueske, S. Guenter, G. Buticchi, M. Liserre, and F. W. Fuchs, "Interleaved operation of parallel neutral-point clamped inverters with reduced circulating current," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 5254–5261.
- [8] Z.-X. Zou, F. Hahn, G. Buticchi, S. Günter, and M. Liserre, "Interleaved operation of two neutral-point-clamped inverters with reduced circulating current," *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10 122–10 134, 2018.
- [9] S. K. Giri, S. Chakrabarti, S. Banerjee, and C. Chakraborty, "A carrier-based pwm scheme for neutral point voltage balancing in three-level inverter extending to full power factor range," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 3, pp. 1873–1883, 2017.
- [10] A. Tcai, Y. Kwon, S. Pugliese, and M. G. Liserre, "Reduction of the circulating current among parallel npc inverters," *IEEE Transactions on Power Electronics*, pp. 1–1, 2021.
- [11] D. G. Holmes and T. A. Lipo, *Width Modulation for Power Converters: Principles and Practice*, 2003.