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Zero-sequence Circulating Current Suppression with Stand-alone Feedforward Control for Power Hardware-in-the-Loop System

Jun-Hyung Jung
Marius Langwasser
Sante Pugliese
Marco Liserre

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Zero-sequence Circulating Current Suppression with Stand-alone Feedforward Control for Power Hardware-in-the-Loop System

Jun-Hyung Jung
Chair of Power Electronics
Kiel University
Kiel, Germany
jj@tf.uni-kiel.de

Marius Langwasser
Chair of Power Electronics
Kiel University
Kiel, Germany
mlan@tf.uni-kiel.de

Sante Pugliese
Chair of Power Electronics
Kiel University
Kiel, Germany
sapu@tf.uni-kiel.de

Marco Liserre
Chair of Power Electronics
Kiel University
Kiel, Germany
ml@tf.uni-kiel.de

***Abstract*—A PWM converter based power hardware-in-the-loop (PHIL) system can provide rapid and low-cost alternatives for prototype testing of high-power converters for electric vehicles or smart grid industries. To achieve simple configuration avoiding an additional bidirectional DC supply, the power amplifier (PA) in the PHIL can share the DC-link of the device under test (DUT). However, due to the coupling of AC and DC ports and differences in the zero-sequence voltage (ZSV) of the two converters, an inevitable low-frequency zero-sequence circulating current (ZSCC) results. This paper proposes a stand-alone control method using ZSV feedforward control to suppress the ZSCC flowing through the PWM converters of the PA and DUT. The ZSV of the DUT can be estimated from the d-q voltage equation in the PA, and feedforward term is applied with a proportional resonant (PR) controller. The effectiveness of the proposed method is verified by experimental results.**

***Index Terms*—parallel-connected converters, zero-sequence circulating current, feedforward control**

I. Introduction

Industry sectors, such as electric vehicles and smart grids, show an increasing demand for high-power PWM converters, requiring rapid and low-cost testing facilities [1,2]. Power-hardware-in-the-loop (PHIL) testing, including switching power amplifier (PA) provides new alternatives for hardware testing under various testing conditions with limited risk (without affecting the real grid or loads) and time [3-5]. The PA that shares the DC-link with the device under test (DUT) has a simpler and cheaper configuration since an additional bidirectional DC power supply for the PA can be avoided. However, in the case of shared DC-link, a current loop is created between the two converters because the DC and AC ports of the two converters are connected, and a low-frequency zero-sequence circulating current (ZSCC) can flow through this loop [4, 5].

The generation of ZSCC is a main issue for parallel converter systems, and it is known as a prominent source of additional losses and distortion of the phase current. In parallel converters under symmetrical conditions, the ZSCC can be sufficiently suppressed by a basic proportional-integral (PI) controller proposed in [6]. However, if the parallel-connected converters are designed asymmetrically or operated under the unbalanced load conditions, a periodic ZSCC occurs because each converter outputs a different zero-sequence voltage (ZSV) and its voltage difference causes the periodic ZSCC [7]. Since a simple linear PI controller has steady-state error the periodic disturbances such as the ZSCC [8], this controller is not suitable to suppress the periodic ZSCC [9], several researches have proposed the ZSCC suppressing controller using the P-resonant (PR) controller [10] and feedforward control [11, 12].

The presented PHIL system, consisting of parallel-connected PA and DUT, shows the characteristics of asymmetric operation of parallel converters, and the asymmetry is much greater than the typical operation of parallel converters because the current flowing through the PA and DUT are exactly opposite to each other. For this reason, a large periodic ZSCC distorting the phase current is generated, and the current should be suppressed for the PHIL testing. In [4] and [5], a passive method using a common-mode (CM) choke on the DC lines is proposed for a motor simulator system. Although a CM choke has a positive effect on suppressing ZSCC, this method has limitations in terms of volume and cost. ZSV feedforward methods can be applied in the PA control structure for ZSCC suppression purpose [9-11]. However, this approach requires the exact knowledge of the ZSV generated by the DUT, which implies a data communication system between the PA and the DUT is essential. In general, there is no guarantee that the DUT can send the data about the ZSV to the PA in real-time. Therefore, stand-alone implementation of the feedforward compensation is needed.

This paper proposes a feedforward control method for a stand-alone ZSCC suppression controller. For the feedforward control, the three-phase voltage references of DUT are estimated using the d-q voltage equation and measured phase current. Then, the ZSV of DUT can be obtained from the estimated three-phase voltage references. In addition, a generation of the residual ZSCC ripple due to the parameter errors in filters is analyzed. Based on this analysis result, a PR controller, which can effectively reduces the periodic error, is applied as the ZSCC controller instead of the basic

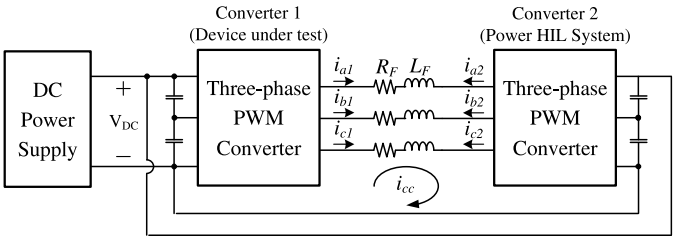


Fig. 1. PHIL system configuration for evaluating DUT with PA.

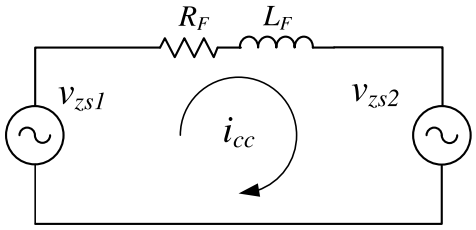


Fig. 2. Equivalent circuit on zero-sequence for DUT and PA converters.

PI controller to remove the residual ripple of ZSCC. Finally, the effectiveness of the proposed feedforward control method is validated with experimental results.

II. PHIL System Sharing DC-link of DUT and ZSCC

Fig. 1 shows the PHIL system configuration, which consists of the PA based on the three-phase PWM converter, evaluating the performance of the DUT. Three-phase AC ports of the PWM converter in the PHIL system are connected with the DUT side converter through inductors (L_F). In addition, the PA side converter shares a DC-link of the DUT instead of using an additional bidirectional DC supply. Although this configuration has advantages in terms of space and cost for the test, the ZSCC can flow through between the PA and DUT because the DC and AC ports of the two converters are connected, and it makes a path for the ZSCC. Generally, the ZSCC, i_{cc}, is defined as the current flowing through parallel-connected converters on the zero-sequence, and it can be expressed with the sum of the three-phase currents as given in (1).

$$i_{cc} = \frac{i_{a1} + i_{b1} + i_{c1}}{3} = -\frac{i_{a2} + i_{b2} + i_{c2}}{3} \tag{1}$$

Since the DUT and PA in Fig. 1 are connected through DC and AC ports, this configuration is the same with the parallel converter system, and the generation of the ZSCC is a matter of course.

The output voltage equation for each phase of the converters in Fig. 1 can be obtained in (2).

$$v^*_{x1p} = R_F i_{x1} + L_F \frac{di_{x1}}{dt} + v^*_{x2p} \quad (x = a, b, c) \tag{2}$$

$$v^*_{xnp} = v^*_{xn} + v_{zsn} \quad (n = 1, 2) \tag{3}$$

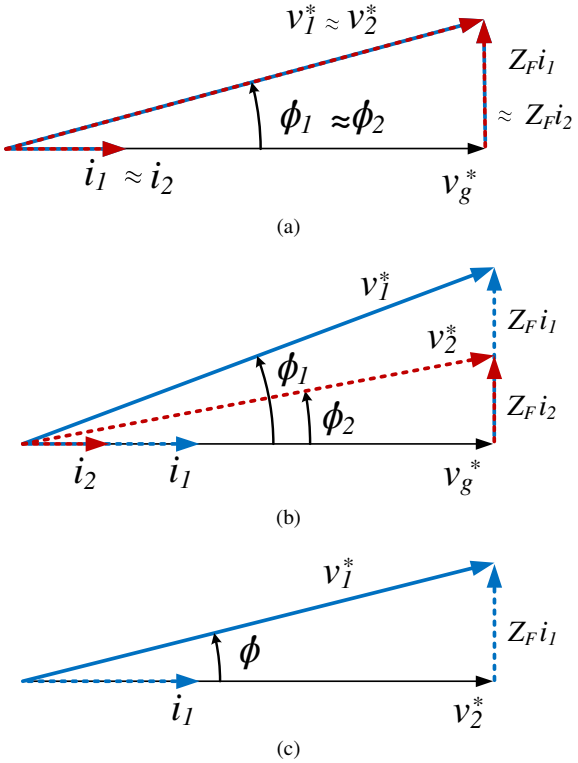


Fig. 3. Voltage vectors of parallel-connected converters. (a) symmetrical condition. (b) asymmetrical condition. (c) PHIL system in this paper

Where, v^*_{xnp} is the phase voltage of the converter 'n' and can be found as the sum of output voltage from a current controller (v^*_{xn}), and the ZSV, v_{zsn}. i_{xn} is the output phase current of the converter 'n', and R_F and L_F are resistance and inductance of the common AC bus filters, respectively.

Summing up the three-phase voltages in (2), the ZSV can be derived as in (4).

$$v_{zs1} = R_F i_{cc} + L_F \frac{di_{cc}}{dt} + v_{zs2} \tag{4}$$

Laplace-transformation and mathematical manipulation lead to the ZSCC expression in (5). This analysis confirms that the ZSCC is generated by the difference between ZSVs of DUT and PA side converters, as shown in Fig. 2, which depicts the equivalent circuit for the CM (i.e., zero-sequence).

$$i_{cc} = \frac{1}{sL_F + R_F}(v_{zs1} - v_{zs2}) \tag{5}$$

In the general case of grid-connected parallel converters, for example, the three-phase voltage references and the voltage vectors (V^*_n), synthesized by the converters, are assumed to be almost the same each other, as presented in Fig. 3(a) if the parallel-connected converters are identical in terms of hardware and current control conditions. For this reason, the ZSVs of the two converters are almost the same, as shown in Fig. 4(a), because the ZSV is based on the three-phase voltage references. Under this symmetrical condition, only a small ZSCC occurs, which can be suppressed to zero by a

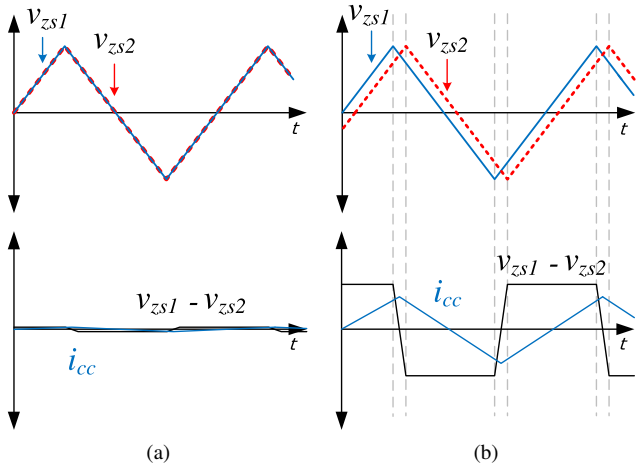


Fig. 4. ZSV of two parallel converter and ZSCC due to the difference of ZSV. (a) symmetrical condition (b) asymmetrical condition.

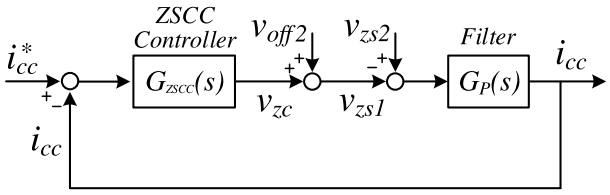


Fig. 5. Block diagram of the ZSCC suppression control system.

conventional proportional controller as proposed in [6]. On the other hand, Fig. 3(b) shows that the voltage vectors have different magnitude and phase angles when the converters are controlled with different current conditions. As a result, the two ZSVs are different in magnitude and phase, and this difference leads to the generation of the periodic ZSCC. In the case of the PHIL system in Fig. 1, the difference in ZSVs increases more than the case in Fig. 3(b). Fig. 3(c) shows the voltage vectors between converter 1 (DUT) and converter 2 (PA). Basically, as the magnitude of the phase current flowing between the two converters increases, the phase and the voltage difference between the two voltage vectors increases. Furthermore, the difference between the two voltage vectors may increase further depending on the load conditions simulated by the PHIL system. In other words, a much larger ZSCC can occur than the case of the parallel converters even under the unbalanced load conditions described in Fig. 3(b).

III. ZSCC Suppression Using Proposed Feedforward Control

A. Feedforward Control based on ZSV estimation

Fig. 5 shows a control block diagram for suppressing ZSCC considering the equivalent circuit of Fig. 2 and (5). Transfer functions $G_{ZSCC}(s)$ and $G_P(s)$ are about a controller for suppressing the ZSCC and filter between the two converters, respectively. From the control point of view, the difference in the ZSVs can be seen as the disturbance, which generates the periodic ZSCC.

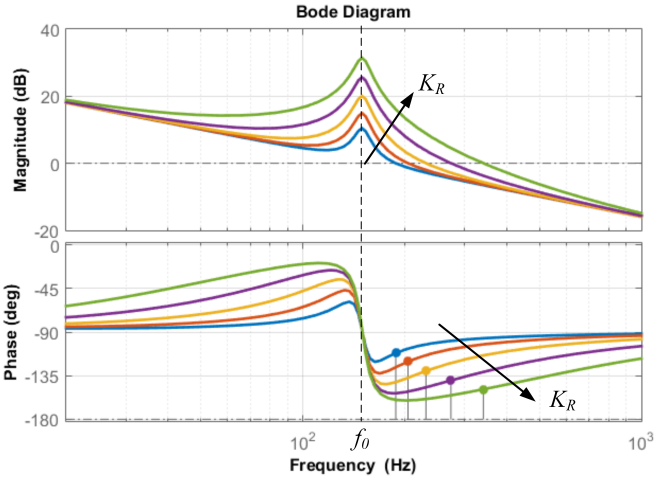


Fig. 6. Bode plot result of the open-loop transfer function for different resonance gains.

A conventional proportional-integral (PI) controller is not effective in reducing the periodic ZSCC because this controller does not incorporate the model of a periodic signal and it cannot provide zero steady-state error to periodic disturbances. On the other hand, a P-resonant (PR) controller ($G_{PR}(s)$) in (6) is known as to be effective in removing the periodic errors and there are studies that apply the PR controller to the parallel converter to reduce the ZSCC. As mentioned above, however, a large ZSCC occurs in the DUT and PA converters compared to general parallel converters. In this case, it is necessary to use a high gain for the PR controller to obtain the high impedance at the resonant frequency (f_0), but the problem of poor the robustness of the system can be issued as the phase margin decreases, as shown in Fig. 6.

$$G_{PR}(s) = K_P + \frac{K_R s}{s^2 + 2\zeta\omega_c s + \omega_0^2} \tag{6}$$

For these reason, it is essential to apply a feedforward control to the PA converter to remove the disturbance. In existing feedforward methods, each parallel-connected PWM converter can obtain ZSVs of the other converters by using the data communication. In the PHIL system presented in this paper, there is usually no direct communication interface between the controllers of DUT and PA. In other words, the existing feedforward methods for suppressing the ZSCC cannot be applied in this case of the stand-alone ZSCC suppression control.

In this paper, a feedforward compensation using the estimated ZSV of the DUT (v_{zs1}) is proposed to suppress the ZSCC using the PA side converter stand-alone. Since the ZSV is based on the three-phase voltage references, the ZSV of the DUT-side converter can be estimated if it is possible to obtain the three-phase voltage reference. From (2), which is the voltage equation between DUT and PA converters, three-phase voltage references of the DUT can be estimated using the equivalent model with the resistance (L_F) and inductance

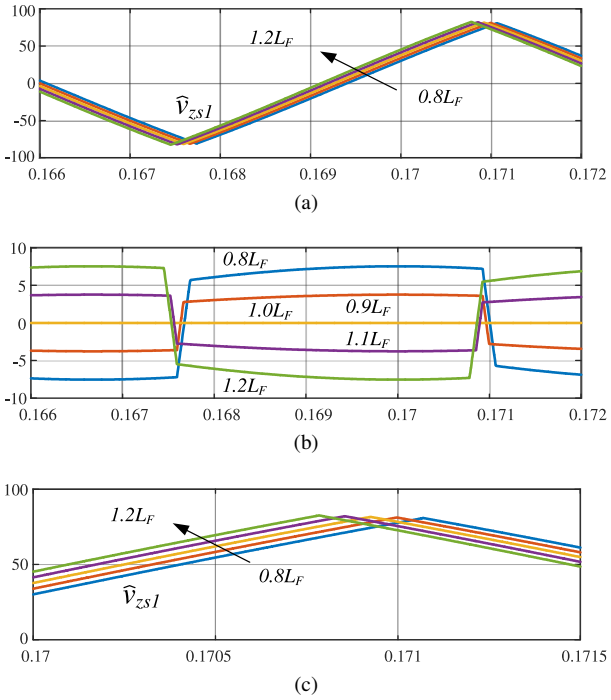


Fig. 7. Estimated ZSV depending on inductance. L_F errors (a) Estimated ZSV. (b) ZSVs difference (c) Zoom-in estimated ZSV.

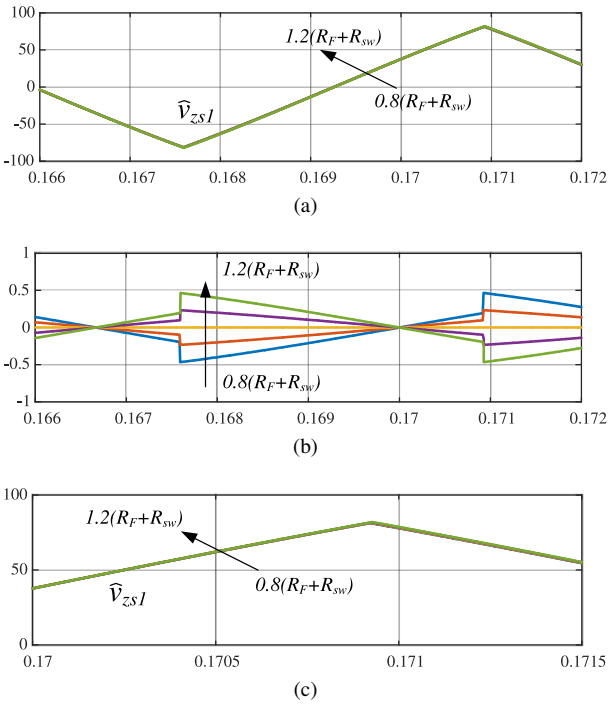


Fig. 8. Estimated ZSV depending on resistance. (R_F and R_{sw}) errors (a) Estimated ZSV. (b) ZSVs difference (c) Zoom-in estimated ZSV.

(R_F), the output voltages from the PA converter, and measured phase currents. However, due to a derivative term in (2), a process of the estimation is complicated and amplified ripple and noise inside the measured current may be included in the estimated ZSV. Therefore, this paper uses synchronous d-q frame voltage equations in (7) and (8) to estimate v^*_{d1} and v^*_{q1}.

$$\hat{v}^*_{d1} = v^*_{d2} - R_F i_{d2} - L_F \frac{di_{d2}}{dt} + \omega L_F i_{q2} \tag{7}$$

$$\hat{v}^*_{q1} = v^*_{q2} - R_F i_{q2} - L_F \frac{di_{q2}}{dt} - \omega L_F i_{d2} \tag{8}$$

From the estimated d-q voltage (v^*_{dq1}), the three-phase voltage references (v^*_{abc1}) can be obtained using the inverse d-q transformations. Finally, the estimated ZSV of DUT ($\hat{v}_{zs1}$) can be obtained using the min-max third-harmonic injection in (9).

$$\hat{v}_{zs1} = -\frac{max(\hat{v}^*_{a1}, \hat{v}^*_{b1}, \hat{v}^*_{c1}) + min(\hat{v}^*_{a1}, \hat{v}^*_{b1}, \hat{v}^*_{c1})}{2} \tag{9}$$

B. Analysis on Effects of Parameter Errors

If the conditions in (7) and (8) are ideal, the proposed feedforward compensation method is capable of eliminating most of the difference between the ZSVs and it could be enough to apply the simple P or PI controller to close the loop. However, the proposed feedforward method utilizes nominal filter parameters to estimate the ZSV of the DUT, so if there are errors between the parameters used for the estimation and the actual values, a small ZSV difference remains. Thus, in this paper, the effects of the errors on the estimation are analyzed.

Fig. 7 shows the effects of the inductance (L_F) error (-20 % +20 %) on the estimation of the ZSV. As shown in Fig. 7(a) and 7(c), the inductance error has a more significant effect on the phase than the magnitude of the ZSV. Considering that the power flows from the DUT into the PA, the estimated ZSV lags behind the actual ZSV if it is smaller than the actual inductance. On the other hand, when the inductance is larger than the actual value, it can be confirmed that the estimated ZSV is leading the actual voltage. As a result, the ZSV difference occurs, as shown in Fig. 7(b).

Fig. 8 presents the effect of the resistance error on the ZSV difference. The ratio of error is the same as the case of the inductance in Fig. 7. Compared with the results in Fig. 7, the effects of the error are small as presented in Fig. 8(c). This is because the resistance (R_F) of the filter between the DUT and PA converters is much smaller than the impedance of the inductance, even if the IGBT resistance (R_{sw}) is taken into account.

Consequently, it can be seen that the inductance error has a significant influence on the generation of residual ZSV. The inductance of the filter on the PA converter side can be measured relatively accurately, but it is not easy to guarantee that the correct value is always known in the inductance on the DUT side. Therefore, it is essential to apply a PR controller to suppress ZSCC caused by the residual ZSV. A block diagram of the proposed feedforward control with the PR controller for the PA converter is shown in Fig. 9.

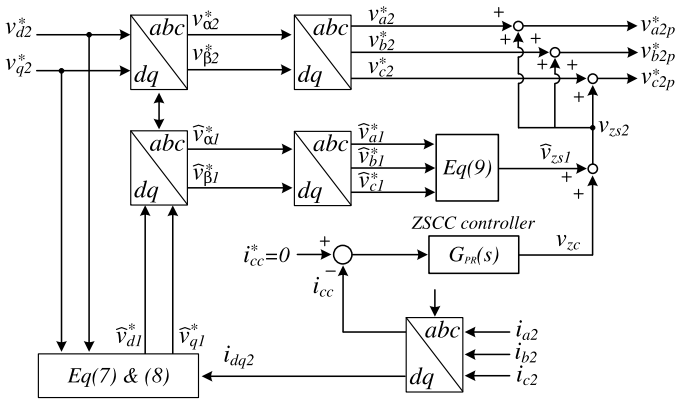


Fig. 9. Entire block diagram of proposed feedforward control with PR controller for the PA converter.

TABLE I
EXPERIMENTAL CONDITIONS

Symbol	Parameter	Value
L_F	Inductance of filter	$0.6\,mH$
R_F	Resistance of filter	$2\,m\Omega$
V_{DC}	DC-link voltage	$400\,V$
V^*_{abc2}	Output phase voltage of PA	$180\,V_{pk}$
f	Output frequency	$50\,Hz$
f_{sw}	switching frequency	$10\,kHz$

IV. EXPERIMENTAL RESULTS

In order to validate the proposed feedforward control method for suppressing the ZSCC, two three-level NPC converters with a rated power of 500 kW in Fig. 10 are used for the experiments while the overall system parameters are given in Table 1. The PA side converter outputs the three-phase voltage sources to provide ideal grid voltage with a 50 Hz for the DUT side converter and the DUT converter is controlled to output the current of 100 A.

Fig. 11 shows experimental results when PA converter is operated with only the conventional P controller without the proposed feedforward control for the ZSCC suppression. Fig. 11(a) shows the ZSVs of two converters, their voltage difference and the periodic ZSCC. It can be seen that v_{zs2} cannot keep up with v_{zs1} and lags behind, resulting in the periodic ZSV difference. This is because the P controller cannot remove steady-state error due to the ZSV difference. As a result, a large periodic ZSCC of about 30 A corresponding to three times the fundamental frequency (150 Hz) occurs, leading to the severe distortion of the three-phase currents, as shown in Fig. 11(b).

Fig. 12 shows the experimental results when applying the proposed feedforward control with the P controller. Compared to the result in Fig. 11, Fig. 12(a) shows that ZSVs of two converters are overlapped, and the ZSV difference is reduced. As a result, the ZSCC is significantly reduced, improving the three-phase current waveform close to the sinusoidal wave despite a little distortion, as shown in Fig. 12(b). However, a

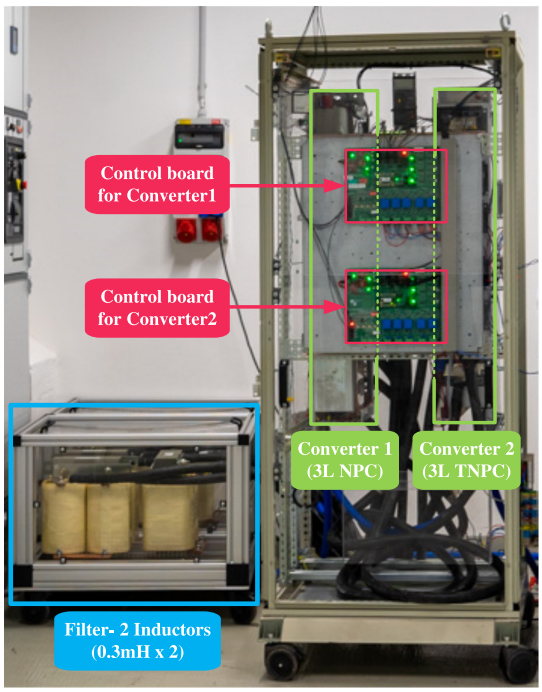
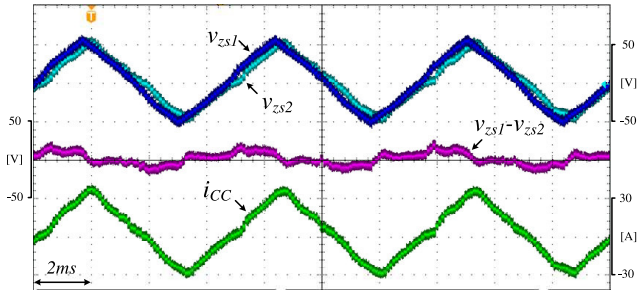
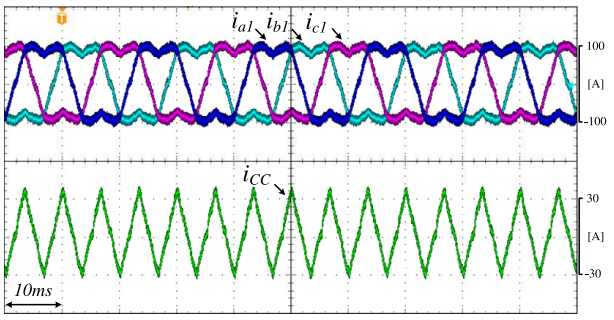


Fig. 10. DUT and PA converters used in the experiment.



(a)



(b)

Fig. 11. Experimental results with the conventional P controller without the feedforward control. (a) ZSVs and ZSCC. (b) Three-phase currents and ZSCC.

ripple in the ZSCC of about 6 A remains, and this is the effect of the parametric error, especially in inductance, as described in Section III.

To suppress the residual ZSCC due to the parametric errors, the PR controller is applied with the feedforward control. Fig. 13(a) shows that the application of the PR controller overlaps

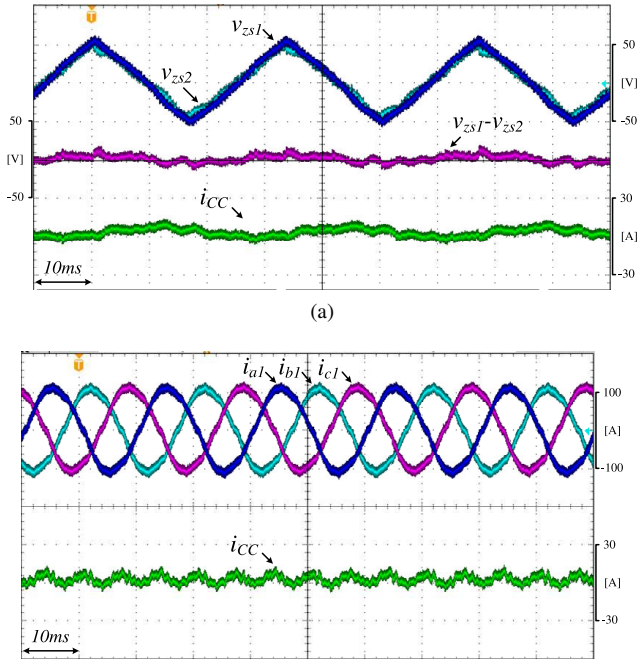


Fig. 12. Experimental results of the feedforward control with the P controller. (a) ZSVs and ZSCC. (b) Three-phase currents and ZSCC.

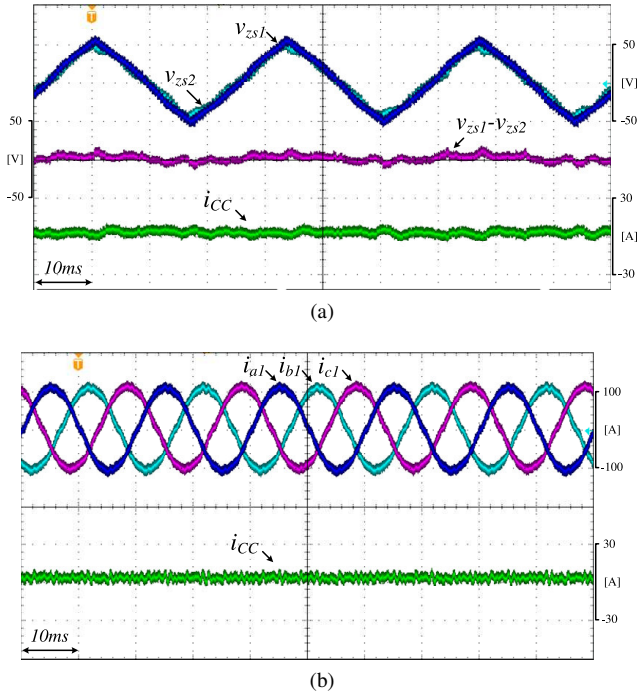


Fig. 13. Experimental results of the feedforward control with the PR controller. (b) Three-phase currents and ZSCC.

v_{zs1} and v_{zs2} more than the result in Fig. 12(a), even though it is small effects. As a result, it can be confirmed in Fig. 13(b) that most of the ZSCC ripple corresponding to three times the fundamental frequency (150 Hz) in Fig. 12 is reduced. In addition, the distortion of the phase current is further improved compared to the results of Fig. 12.

In Fig. 13(a), it can be confirmed that the residual ZSCC is reduced and a little distortion in the three-phase current is also improved.

V. Conclusion

The PA of the PHIL system, represented in this paper, shares the DC-link of the DUT to configure the simple and low-cost setup for testing high-power converter systems. However, it has been analyzed that the generation of large periodic ZSCC is inevitable because the ZSV difference between DUT and PA is input to the ZSCC control system as a disturbance. Therefore, this paper proposed the feedforward control method estimating the ZSV difference based on the d-q equivalent circuit to suppress the ZSCC without using big CM chokes and receiving the ZSV from the DUT. In addition, the application of the PR controller to the feedforward method was proposed to remove the residual ZSCC due to the parametric errors on the equivalent circuit. In experimental results, approximately 80% of the ZSCC was removed by applying the proposed feedforward compensation to the simple P controller. Furthermore, it was confirmed that the proposed feedforward control method, including the PR controller, can completely remove the ZSCC at 150Hz. Thus, the proposed feedforward control method has proved effective in removing the ZSCC in the PHIL system.

References

[1] M. Kesler, E. Ozdemir, M. C. Kisacikoglu and L. M. Tolbert, "Power Converter-Based Three-Phase Nonlinear Load Emulator for a Hardware Testbed System," in IEEE Transactions on Power Electronics, vol. 29, no. 11, pp. 5806-5812, Nov. 2014.

[2] B. Benkendorff, F. W. Fuchs and M. Liserre, "Simulated and measured efficiency verification power circulation method of a high power low voltage NPC converter for wind turbines," in ECCE Europe, 2016, pp. 1-10.

[3] K. Upamanyu and G. Narayanan, "Improved Accuracy, Modeling, and Stability Analysis of Power-Hardware-in-Loop Simulation With Open-Loop Inverter as Power Amplifier," in IEEE Transactions on Industrial Electronics, vol. 67, no. 1, pp. 369-378, Jan. 2020.

[4] J. Itoh and T. Abe, "Circulation current reduction for a motor simulator system using a power converter with a common mode transformer," 2009 IEEE 6th International Power Electronics and Motion Control Conference, 2009, pp. 1662-1667

[5] K. Saito and H. Akagi, "A Real-Time Real-Power Emulator of a Medium-Voltage High-Speed Induction Motor Loaded With a Centrifugal Compressor," in IEEE Transactions on Industry Applications, vol. 55, no. 5, pp. 4821-4833, Sept.-Oct. 2019.

[6] Zhihong Ye, D. Boroyevich, Jae-Young Choi and F. C. Lee, "Control of circulating current in two parallel three-phase boost rectifiers," in IEEE Transactions on Power Electronics, vol. 17, no. 5, pp. 609-615, Sept. 2002.

[7] R. Zhu, M. Liserre, Z. Chen and X. Wu, "Zero-Sequence Voltage Modulation Strategy for Multiparallel Converters Circulating Current Suppression," in IEEE Transactions on Industrial Electronics, vol. 64, no. 3, pp. 1841-1852, March 2017.

[8] R. Teodorescu, F. Blaabjerg and Liserre, M. and P.c. Loh, "Proportional-resonant controllers and filters for grid-connected voltage source converters", IEE Proceedings Electric Power Applications, vol.153, no.5, pp. 750-762, Sep. 2006.

[9] D. Panprasert and B. Neammanee, "The d and q Axes Technique for Suppression Zero-Sequence Circulating Current in Directly Parallel Three-Phase PWM Converters," in IEEE Access, vol. 9, pp. 52213-52224, 2021, doi: 10.1109/ACCESS.2021.3069702.

[10] C. Qin, C. Zhang, A. Chen, X. Xing and G. Zhang, "Circulating Current Suppression for Parallel Three-Level Inverters Under Unbalanced Operating Conditions," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 7, no. 1, pp. 480-492, Mar. 2019.

[11] X. Zhang, T. Wang, X. Wang, G. Wang, Z. Chen and D. Xu, "A Coordinate Control Strategy for Circulating Current Suppression in Multiparalleled Three-Phase Inverters," in IEEE Transactions on Industrial Electronics, vol. 64, no. 1, pp. 838-847, Jan. 2017.

[12] G. Mademlis, Y. Liu, N. Sharma and X. Huang, "Circulating Current Reduction in Common DC-Link Power-HIL for Drives using SVM with Zero-Sequence Compensation," IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society, 2020, pp. 4673-4678.