Reliability-Oriented Strategies for Multichip Module Based Mission Critical Industry Applications

Dissertation

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M. Sc. *Victor de Nazareth Ferreira*

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Declaration

I declare in lieu of oath that I have completed the dissertation on the topic:

Reliability-Oriented Strategies for Multichip Module Based Mission Critical Industry Applications

apart from the supervision of Prof. Marco Liserre and Prof. Braz Cardoso, I have prepared the following documents independently and without assistance and have not yet submitted, published or submitted for publication, either in whole or in part, to any other body within the framework of an examination procedure. Furthermore, I hereby affirm that I have prepared the present dissertation in accordance with the rules of good scientific practice of the German Research Foundation (Deutsche Forschungsgemeinschaft) and that all passages taken over verbatim from other authors as well as the explanations of my work that closely follow the thought processes of other authors are specially marked and the sources are indicated.

Kiel, 08. Dec 2020

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To my family. At the end of the day, it's all for you.

Kiel in Dec 2020

Contents

Abstract xii

Resumo xiv

Kurzfassung xvi

List of Tables xix

List of Figures xxx

Abbreviation List xxxi

1 Introduction **1**

1.1 Mission Critical Industry Applications 3

1.2 Thermal Mismatches in MCM-based Power Converters 5

1.3 Research Proposal 6

1.3.1 Target 1 - Thermal Balancing in MCM-based Mission Critical Power Converters 6

1.3.2 Target 2- Reliability-Oriented Design for MCM-based Mission Critical Applications 7

1.4 Thesis Structure 7

1.4.1 Publications During the Doctoral Project 8

2 Thermal Distribution and Reliability Impacts in Multichip Modules **11**

2.1 Introduction 12

2.2 Thermal Mismatches in Multichip Power Modules 13
2.2.1 Current Unbalance 14
2.2.2 Thermal Cross-Coupling 17
2.2.3 Cooling Challenges 18
2.3 Thermal Modeling of Multichip Modules 19
2.3.1 Equivalent Thermal Networks 19
2.3.2 FEM-based Thermal Modeling 21
2.3.3 Thermal Validation 25
2.4 Thermally-Related Failures in Power Modules 27
2.4.1 Instabilities 27
2.4.2 Severe Overloads 28
2.4.3 Wear-out failures in power modules 29
2.4.4 Accumulated Degradation Unevenness in MCMs 30
2.5 Proposed Solutions to Mitigate Thermal Mismatches in MCMs 31
2.6 Short Summary of the Chapter 32

3 Die-Level Design for Reliability of MCM-based Converters 33

3.1 Introduction 35
3.2 Design for Reliability of Power Semiconductor Devices 36
3.2.1 Mission Profile 36
3.2.2 Converter Analysis 37
3.2.3 Thermal Analysis 38
3.2.4 Lifetime Analysis 40
3.2.5 Statistical Analysis for Reliability Prediction 42
3.2.6 System-Level Reliability Analysis 43
3.3 Die-Level Design for Reliability 44
3.4 Design for Reliability of Mission Critical Industry Applications - A case study 46
3.4.1 Mission Profile 47

3.4.2 Converter Analysis . . . 49
3.4.3 Thermal Analysis . . . 50
3.4.4 Lifetime, Statistical and Reliability Analysis . . . 50
3.5 Short Summary of the Chapter . . . 53

4 Thermal Balancing in Power Converters 54

4.1 Introduction . . . 56
4.2 Thermal Control in Power Electronics Devices . . . 56
4.2.1 Finite Control Set Model Predictive Control . . . 57
4.2.2 Adaptive Dc-Link Voltage Control . . . 59
4.2.3 Power Routing . . . 59
4.3 Power Routing in Multiphase Drives . . . 60
4.3.1 Soft-Unbalance Operation of Multiphase Machines . . . 61
4.3.2 Power Routing in Multiphase Drives . . . 64
4.3.3 Thermal Validation . . . 65
4.3.4 Reliability Analysis of the Power Routing in MCIAs . . . 68
4.4 Thermal and Aging Monitoring of Power Semiconductor Devices . . . 70
4.4.1 Sensor-based Temperature Monitoring . . . 70
4.4.2 Gate Voltage Monitoring . . . 71
4.4.3 Gate Resistance Monitoring . . . 73
4.4.4 Transient Monitoring . . . 74
4.4.5 Device Current Monitoring . . . 76
4.4.6 On-State Voltage Monitoring . . . 77
4.4.7 Comparison of Thermal and Aging Monitoring Strategies . . . 87
4.5 Validation of a V_{on}-based Thermal Balancing Strategy . . . 89
4.5.1 V_{on}-based T_j Sensing . . . 90
4.5.2 V_{on}-based Thermal Balancing . . . 91
4.6 Short Summary of the Chapter . . . 93

5 Die-Level Thermal Balancing in Multichip Modules 95

5.1 Introduction . . . 97

5.2 The Multi-gate Multichip Structure . . . 97

5.3 Die-Level Thermal Balancing . . . 98

5.3.1 Pulse-Shadowing Based Thermal Balancing . . . 99

5.3.2 Turn-off Losses Manipulation for Thermal Balancing . . . 108

5.3.3 Comparison of the Thermal Balancing Solutions . . . 115

5.4 Indirect Thermal Balancing for Diodes . . . 118

5.5 Selective T_j Sensing and the Pre-Programmed Thermal Balancing . . . 120

5.6 Reliability and Efficiency Analysis of the Die-Level Thermal Balancing in MCIA . . . 122

5.7 Technical Analysis of the Proposed Solution . . . 126

5.7.1 Multi-Gate Driver Considerations . . . 126

5.7.2 Power Level Margins . . . 127

5.8 Short Summary of the Chapter . . . 128

5.8.1 Evaluation System with Equivalent Multi-gate Multichip Module 129

6 Conclusions and Future Research 132

6.1 Summary . . . 134

6.2 Future Research I - Die-Level Thermal Balancing in Wide-Bandgap Devices . . . 136

6.3 Future Research II - Degradation Control Through SOH of Power Semiconductor Devices . . . 136

A V_{on}-based Sensing Circuit Design 137

A.1 Design of a V_{on}-based Sensing Circuit . . . 137

A.1.1 Power Supply . . . 137

A.1.2 Operational Amplifier . . . 138

A.1.3 Isolation . . . 138

A.1.4 Transient Performance . . . 139

A.1.5 Steady-State Performance 140
A.1.6 Moving Average Digital Filter for High Precision 140

B Design and Control of the Adopted Electrical Drives 142

B.1 Electrical Drive Design and Control 142
B.1.1 Indirect Field Orientation Control 144
B.1.2 Control Tuning 145
B.1.3 Time Domain Response 147

Abstract

The availability is defined as the portion of time the system remains operational to serve its purpose. In mission critical applications (MCA), the availability of power converters are determinant to ensure continue productivity and avoid financial losses. Multichip Modules (MCM) are widely adopted in such applications due to the high power density and reduced price; however, the high number of dies inside a compact package results in critical thermal deviations among them. Moreover, uneven power flow, inhomogeneous cooling and accumulated degradation, potentially result in thermal deviation among modules, thereby increasing the temperature differences and resulting in extra temperature in specific subset of devices. High temperatures influences multiple failure mechanisms in power modules, especially in highly dynamic load profiles. Therefore, the higher failure probability of the hottest dies drastically reduces the reliability of mission critical power converters. Therefore, this work investigate reliability-oriented solutions for the design and thermal management of MCM-based power converters applied in mission critical applications. The first contribution, is the integration of a die-level thermal and probabilistic analysis on the design for reliability (DFR) procedure, whereby the temperature and failure probability of each die are taken into account during the reliability modeling. It is demonstrated that the die-level analysis can obtain more realistic system-level reliability of MCM-based power converters. Thereafter, three novel die-level thermal balancing strategies, based on a modified MCM - with more gate-emitter connections - are proposed and investigated. It is proven that the temperatures inside the MCM can be overcame, and the maximum temperate reduced in up to 8 %. Moreover, a power routing strategy for multiphase

drives is presented for the first time, whereby thermal deviations of up to $10\,^{\circ}C$ can be considerably reduced without degrading the electromagnetic machine performance. A finite elements model of a 24-dies MCM is developed to validate the MCM thermal distribution as well as the proposed balancing strategies. As a complementary contribution, a very low noise on-state voltage (V_{on}) sensing circuit with $0.3\,mV$ of precision is implemented, and its capability to close the loop of thermal control is strategies is demonstrated. The proposed solutions are also validated by an experimental setup which has an equivalent three-chips multi-gate MCM, a V_{on}-based junction temperature sensing capability and high resolution thermal camera. In addition, to evaluate the impact of the proposed strategies on the reliability and availability of MCA power converters, a case study based on a real high power mission critical application, is conducted. It is demonstrated that the power converter lifetime can increase in up to 50% when the proposed thermal balancing strategies are adopted.

Resumo

A disponibilidade é definida como a porção de tempo que o sistema permanece operacional para servir ao seu propósito. Em aplicações de missão crítica (MCA), a disponibilidade de conversores de energia é determinante para garantir a continuidade da produtividade e evitar perdas financeiras. Os Módulos Multichip (MCM) são amplamente adotados em tais aplicações devido à alta densidade de potência e preço reduzido; entretanto, o grande número de chips dentro de um pacote compacto resulta em desvios térmicos críticos entre eles. Além disso, o fluxo de energia desigual, o resfriamento não homogêneo e a degradação acumulada podem resultar em desvio térmico entre os módulos, aumentando assim as diferenças de temperatura e resultando em temperatura extra em subconjuntos específicos de dispositivos. As altas temperaturas influenciam vários mecanismos de falha nos módulos de potência, especialmente em perfis de carga altamente dinâmicos. Portanto, a probabilidade de falha mais alta das chips mais quentes reduz drasticamente a confiabilidade dos conversores de energia de missão crítica. Desta maneira, este trabalho investiga soluções orientadas para confiabilidade para o projeto e gerenciamento térmico de conversores de energia baseados em MCM em aplicações de missão crítica. A primeira contribuição é a integração de uma análise térmica e probabilística no nível de chip no procedimento de projeto para confiabilidade (DFR), em que a temperatura e a probabilidade de falha de cada chip são levadas em consideração durante a modelagem da confiabilidade. É demonstrado que a análise de nível de chip pode obter confiabilidade de nível de sistema mais realista de conversores de energia baseados em MCM. Posteriormente, três novas estratégias de balanceamento térmico em nível de chip, com base em um MCM modificado - com

mais conexões gate-emissor - são propostas e investigadas. É comprovado que as temperaturas dentro do MCM podem ser superadas, e o temperado máximo reduzido em até 8 %. Além disso, uma estratégia de roteamento de energia para drives multifásicos é apresentada pela primeira vez, em que desvios térmicos de até $10°C$ podem ser reduzidos consideravelmente sem degradar o desempenho da máquina eletromagnética. Um modelo de elementos finitos de um MCM de 24 chips é desenvolvido para validar a distribuição térmica do MCM, bem como as estratégias de balanceamento propostas. Como contribuição complementar, um circuito de detecção de tensão no estado de ruído muito baixo (V_{on}) com 0,3 mV de precisão é implementado e sua capacidade de fechar o loop de controle térmico é demonstrada. As soluções propostas também são validadas por um setup experimental que conta com um MCM com multiplos gates equivalente de três chips, um circuito de detecção de temperatura de junção baseada em V_{on} e câmera térmica de alta resolução. Além disso, para avaliar o impacto das estratégias propostas na confiabilidade e disponibilidade dos conversores de energia, é realizado um estudo de caso baseado em uma aplicação real de missão crítica de alta potência. É demonstrado que a vida útil do conversor de potência pode aumentar em até 50% quando as estratégias de balanceamento térmico propostas são adotadas.

Deutsch Kurzfassung der Arbeit

Die Verfügbarkeit ist definiert als der Teil der Zeit, die das System betriebsbereit bleibt, um seinen Zweck zu erfüllen. In missionskritischen Anwendungen (MCA) ist die Verfügbarkeit von Stromrichtern entscheidend, um die Produktivität zu gewährleisten und finanzielle Verluste zu vermeiden. Multichip-Module (MCM) werden in diesen Anwendungen aufgrund der hohen Leistungsdichte und des reduzierten Preises häufig eingesetzt. Die hohe Anzahl von Halbleitern in einem kompakten Gehäuse führt jedoch zu kritischen thermischen Abweichungen ihrer Temperaturen. Darüber hinaus führen ungleichmäßiger Leistungsfluss, inhomogene Kühlung und Alterung potenziell zu Abweichungen im thermischen Verhalten der Module, wodurch die Temperaturunterschiede erhöht werden und zu einer erhöhten Temperatur Teilen der Module führt. Hohe Temperaturen beeinflussen dabei mehrere Ausfallmechanismen in Leistungshalbleitermodulen, insbesondere bei hochdynamischen Lastprofilen. Dadurch steigt die Ausfallwahrscheinlichkeit der heißesten Halbleiter und die Zuverlässigkeit von einsatzkritischen Leistungswandlern sinkt drastisch. Aus diesem Grund untersucht diese Arbeit zuverlässigkeitsorientierte Lösungen für den Entwurf und das thermische Management von MCM-basierten Leistungswandlern, die in missionskritischen Anwendungen eingesetzt werden. Der erste Beitrag ist die Integration einer thermischen und probabilistischen Analyse auf Chipebene in das DFR-Verfahren (Design for Reliability), wobei die Temperatur und die Ausfallwahrscheinlichkeit jedes Chips bei der Zuverlässigkeitsmodellierung berücksichtigt werden. Es wird gezeigt, dass mit der Analyse auf Chipebene eine realistischere Zuverlässigkeitsabschätzung von MCM-basierten Leistungswandlern auf Systemebene erreicht werden kann. Danach werden drei neuar-

tige thermische Ausgleichsstrategien auf Matrizenebene vorgeschlagen und untersucht, die auf einem modifizierten MCM - mit mehr Gate-Emitter-Verbindungen - basieren. Es wird demonstriert, dass die Temperaturen innerhalb des MCMs ausgeglichen und die maximale Temperatur um bis zu 8 % reduziert werden kann. Darüber hinaus wird erstmals eine Power-Routing-Strategie für mehrphasige Antriebe vorgestellt, wodurch thermische Abweichungen von bis zu $10\,°C$ erheblich reduziert werden können, ohne den Maschinenbetrieb zu beeinflussen. Zur Validierung der thermischen Verteilung der MCM sowie der vorgeschlagenen Ausgleichsstrategien wird eine MCM mit 24 Chips konstruiert. Als zusätzlicher Beitrag wird ein sehr rauscharmer Schaltkreis zur Erfassung der Spannung im eingeschalteten Zustand (V_{on}) mit einer Genauigkeit von $0{,}3\,mV$ implementiert und seine Fähigkeit zur Schließung des Regelkreises der thermischen Regelungsstrategien demonstriert. Die vorgeschlagenen Lösungen werden auch durch einen Versuchsaufbau validiert, der eine äquivalente Drei-Chip-Multi-Gate-MCM, eine auf V_{on} basierende Sperrschichttemperaturerfassungsfähigkeit und eine hochauflösende Wärmebildkamera aufweist. Um die Auswirkungen der vorgeschlagenen Strategien auf die Zuverlässigkeit und Verfügbarkeit von MCA-Leistungswandlern zu evaluieren, wird außerdem eine Untersuchung auf der Grundlage einer realen missionskritischen Hochleistungsanwendung durchgeführt. Es wird gezeigt, dass die Lebensdauer von Leistungswandlern um bis zu 50 % erhöht werden kann, indem die vorgeschlagenen thermischen Ausgleichsstrategien angewendet werden.

List of Tables

2.1 Simulation parameters for the validation of the thermal distribution. . . 25

2.2 Material characteristics of a power module. 29

3.1 Fixed parameters in Bayerer's equation. 41

3.2 Fixed parameters of wire bond lifetime model. 41

3.3 Simulation parameters. 49

4.1 Rated and equivalent circuit parameters of the $690\,V/\,1.4\,MW$ nine-phase induction machine. 66

4.2 Comparative analysis for the presented cases of the multiphase drive in the mine hoist system, showing the temperature and B_{10} lifetime. . . . 70

4.3 Comparison of Thermal Sensitive Parameters. 87

4.4 Comparison among CM techniques. 88

4.5 Validation parameters for the the V_{on}-based thermal control. 92

5.1 Die-Level proportional control parameters. 103

5.2 E_{off} comparison of multiple devices considering a single device with 1 pu of current and two with 0.5 pu each. 112

5.3 Comparative analysis for the presented thermal strategies, showing the highest thermal deviation and temperature among the dies. 117

5.4 Efficiency comparison for the MCM operating with 0.33 pu, 0.66 pu and 1 pu of power, considering four operating conditions: without thermal balancing, pulse-shadowing, turn-on losses and turn-off losses manipulation. 117
5.5 Comparative analysis for the presented thermal strategies in the mine hoist system, showing the highest temperature, the B_{10} lifetime, the energy consumption only by losses in 15 years of operation (E_{15}), and their differences comparing with the system with thermal deviations. . 126
5.6 Validation parameters. 130

B.1 Rated and equivalent circuit parameters of the $690\,V/\,1\,MW$ three-phase induction machine. 143

List of Figures

1.1 Steel industry plants (a) Rolling Mills (b) Wire Rods. 3

1.2 Photo of the gold ore mine hoist plant. 4

1.3 Mission profile of critical industry applications (a) Mine hoist systems (b) Steel rolling mills system. 4

1.4 Temperature distribution in a 24-dies MCM obtained from FEM analysis for the same power and different cooling flows (a) $h = 4440\,W/K.m^{-2}$ (b) $h = 3960\,W/K.m^{-2}$. 5

1.5 Thesis organization and related publications. 9

2.1 Power module structure. 13

2.2 Multichip power module: single-switch, $1.7\,kV$ / $1600\,A$, 16 IGBTs and 8 diodes in a $140\,x\,130\,cm$ structure. 14

2.3 Equivalent circuit of single-switch MCM with N parallel dies. 15

2.4 Thermal impacts on the transient time of Si IGBTs (a) Turn-on (b) Turn-off. 16

2.5 Impact of the temperature on the conductivity of Si IGBTs. 17

2.6 Thermal cross-coupling effects: a heat source is generated in one device and the temperature spread on its neighbors. 18

2.7 Dimensions of a multichip power module with 36 dies. 18

2.8 Dynamic thermal model of power modules with heatsink. 19

2.9 Cauer thermal model. 20

2.10 Foster thermal model. 20

2.11 Impedance curves used to obtain the power module equivalent foster network. 20
2.12 Finite Elements Model of a 1700 V/ 1600 A single-switch, with 24-dies. 22
2.13 Superposition methodology to obtain the equivalent MCM thermal network, whereby the transient curves of all dies are obtained heating a single die at a time. The process is done for each die, but specific ones are shown as examples: (a) T1 (b) T7 (c) D1 (d) D3. 23
2.14 Second-order exponential fitting of the transient temperature obtained through FEM analysis, $f(x) = a \cdot e^{bt} + c \cdot e^{dt}$. 24
2.15 Simulation process, where the thermal network is exported from FEM software and embedded in numeric model. The losses are extracted from the electrothermal model and fed back to FEM software. The process works iteratively for losses and temperature analysis. 25
2.16 FEM analysis of the 24-dies MCM, showing a thermal deviation among the dies of 17.4 $°C$ (a) Steady-State analysis (b) Transient analysis. . . 26
2.17 Temperature on the 24-dies MCM obtained from FEM analysis (a) Standard cooling system ($h = 4440\,W/K.m^{-2}$) (b) Defected cooling system ($h = 3960\,W/K.m^{-2}$). 26
2.18 Classification of failures in power modules based on root cause. 27
2.19 Aging failures in power modules (a) Bond wire metallurgic damage, heel crack, fracture and liftoff. (b) Solder damages. 30

3.1 Design for reliability of power semiconductor devices of a converter applied to mission critical applications. 37
3.2 Switching losses extracted from the datasheet of a power semiconductor device: (a) IGBT Turn-on (b) IGBT Turn-off (c) Diode reverse-recovery . 39
3.3 Conduction losses extracted from the datasheet of a power semiconductor device: (a) IGBT (b) Diode. 39
3.4 Normal distribution with a confidence of 99.73 %. 42

3.5 Unreliability curve with: B_x - time when the device achieve $x\%$ of failure probability; U_x - The failure probability in a specific operation time. . . 44
3.6 The reliability series association, which is adopted when a failure of a single device results in a system interruption. 44
3.7 Die-Level design for reliability flowchart, including - light green - the thermal deviation and the system-level reliability modeling of the MCM dies. 45
3.8 Mine hoist system (a) General diagram (b) Photo of the electrical system of the mine hoist.. 46
3.9 Electrical measurements of the mine hoist during one trip, measured in the real field environment. 48
3.10 Mission profile of the mine hoist system driven by an induction machine with FOC. 49
3.11 Dc-Link current profile of the designed converter feeding the induction machine which drive the mine hoist system. 50
3.12 Junction temperature profile of one MCM in the 2-level inverter with (a) Foster thermal network (b) Matrix with cross-coupling impedance extracted from finite elements analysis. 51
3.13 Monte-Carlo analysis to account the failure distribution over time, considering parametric deviations in V_{ce}, without thermal deviation (purple) - foster thermal network - and with thermal deviation (black) - FEM-based thermal network with cross-coupling. 51
3.14 Series-connected reliability modeling, whereby the failure of a single component means system interruption, for the procedures: (a) System-Level Design for Reliability (b) Die-Level Design for Reliability. 52
3.15 Unreliability analysis of the multichip modules composing the mine hoist power converter, for system-level reliability (purple) and die-level reliability (black) approaches. A B_{10} lifetime difference of 100 % is observed. 52

4.1 Temperature related control variables and strategies for thermal control and power routing, in power electronics devices. 57
4.2 Module and system layout : (a) One phase ANPC open module. (b) Simplified system model scheme of ANPC converter using model predictive control. 58
4.3 59
4.4 Adaptive minimum dc-link control to increase PV lifetime 59
4.5 Power Routing concept, the power is reduced in the most damaged cell to equalize the remaining useful lifetime. 60
4.6 (a) Current diagram of the nine-phase machine in balanced condition (b) Basic construction diagram of the 9PIM with two poles. 61
4.7 Current diagram of the a nine-phase machine in balanced condition, considering a reduction in phase A_1 - current I_1. 62
4.8 Magnetomotive force for the balanced and the re-calculated currents for the soft-unbalanced operation, showing a circular MMF in both conditions. 63
4.9 Flowchart of the power routing for thermal balancing in nine-phase induction machines. 64
4.10 Power routing diagram of a nine-phase machine, whereby the soft-unbalance currents are calculated to balance the temperatures; and it is imposed via a Z-subspace current control. The speed IFOC control is implemented in dq synchronous in the same way of an ordinary three phase induction machine. The T9 matrix generates the voltage references for the 9PH modulator. 65
4.11 FEM-based thermal simulation schematic of the nine-phase machine. . 66

4.12 Transient results of the power routing - triggered at t = 15 s - in a 9PIM fed by a nine-phase inverter with 24-dies MCMs and a defected heatsink in phase A_1 (a) Current in all phases, whereby the current in phase A_1 is reduced to smooth its thermal stress. (b) Temperature of the hottest dies in the MCMs of phases A_1 and A_2, showing a balancing when the power routing is activated. 67

4.13 FEM analysis of the 24-dies MCM in phases A_1 and A_2 of the nine-phase induction machine (a) Without power routing (b) With power routing. 67

4.14 Temperature profile for the die T7 of the 24-dies MCM at the top of phase A_1 of the nine-phase converter applied to the mine hoist profile, considering three cases: standard heatsink (black), defected heatsink (red) and defected heatsink with power routing (blue). 68

4.15 Die-level reliability analysis for the mine hoist system driven by a multiphase machine, for the standard system (black), defected heatsink in phase A1 (red) and power routing (blue) (a) Statistical Analysis (b) Unreliability Analysis. 69

4.16 Classification of the thermal sensitive and aging parameters. 71

4.17 Regulation of the collector current for T_j estimation using $V_{ge,i}$. 72

4.18 The T_j estimation by the internal gate resistance through a predefined dc current injection. 73

4.19 High power IGBT module parasitic-based equivalent circuit. 75

4.20 Gate impedance assist circuit. 75

4.21 The T_j estimation by the saturation current through a regulated V_{gs}. . 76

4.22 The T_j estimation by the short-circuit current. 77

4.23 The timeline of the proposed on-state voltage sensing circuits. 79

4.24 The V_{on} sensing circuit with clamping Zener diodes: (a) 0-600 V (b) 0-2000 V 80

4.25 The V_{on} sensing circuit with series connection of Zener and a diode to clamp the voltage. 80
4.26 The V_{on} sensing circuit with series connection of diode to clamp the voltage and cascode current source. 80
4.27 The V_{on} sensing circuit with series connection of high voltage diodes and single current source. 81
4.28 The V_{on} sensing circuit based on a sensing current and a series connection of high voltage diodes and Zener. 81
4.29 The V_{on} sensing circuit based on a V_{dc} clamping 82
4.30 The V_{on} sensing circuit with active voltage clamping. 83
4.31 The real-time V_{on} sensing circuit with active voltage clamping. 83
4.32 The off-line V_{on} sensing circuit with relay-based voltage isolation. . . . 84
4.33 Low current T_j calibration curve experimentally obtained from a 25 A IGBT (DP25H1200T01667). 85
4.34 Operating region of an IGBT depending on the collector current. The temperature does not impact the V_{ce} with a specific current - i.e. at the inflection point. 86
4.35 The V_{on} sensing circuit with series connection of high voltage diodes, single current source, low noise dc power supply and isolation (a)Schematic (b) Board 89
4.36 V_{ce}-based T_j under fixed current $I_c = 1\,A$ and temperature $T_j = 52\,°C$ (a) Junction temperature measured via fiber optic sensors (b) V_{avg} obtained from a fifty sample move average filter using an 1 MSPS ADC in burst mode (c) Fitting curve obtained with fixed low current of 1 A . 91
4.37 Validation setup consisting of two buck converters in parallel with V_{on} sensing capability, whereby one is placed over a heatsink to obtain a specific thermal deviation. A fiber optic system is used to measure the temperature on the chips and validate the strategy (a) Photo (b) Schematic. 92

4.38 V_{on}-based on-off thermal balancing strategy, whereby the junction temperatures are sensed and the device with highest one has its PWM command blocked. 92

4.39 Experimental validation of the V_{on}-based thermal control. The junction temperature starts with a deviation of $9\,°C$, and it is equalized after the thermal control is triggered at $t = 3\,s$. (a) V_{on} of each switch (b) Measured temperature of each switch. 93

5.1 Multichip Modules (a) Standard Structure (b) Multi-gate Structure . . 97

5.2 Proposed packaging with four equivalent switching groups. (a) Open package with switching groups (b) Package structure with four gate-emitter connections. 98

5.3 Full diagram of the thermal balancing in multichip multi-gate modules, with V_{on}-based T_j sensing 99

5.4 The pulse-processing approaches for die-level thermal balancing: pulse-Shadowing, turn-on losses manipulation and turn-off losses manipulation. 99

5.5 The pulse-shadowing based thermal balancing pulse pattern. 100

5.6 Die-Level proportional control based on average losses. 100

5.7 Frequency response for the equivalent thermal model. 102

5.8 Frequency response for the proportional die-level thermal control system (a) Dynamic stiffness (b) Magnitude gain and phase marging of the open-loop control system. 103

5.9 Transient thermal results of the pulse-shadowing strategy, showing the junction temperature of one die per switching group. The thermal balancing is triggered at $t = 20\,s$, and the temperatures are balanced. . . 105

5.10 Transient thermal results of the pulse-shadowing strategy considering 10% of variation on the R_{th} of SW1, showing the junction temperature of one die per switching group. The thermal balancing is triggered at $t = 20\,s$, and the temperatures are balanced, with deviations below $1°C$.105

5.11 Control diagram of the on-off based die-level thermal control strategy. . 106
5.12 Transient thermal results of the on-off control with pulse-shadowing strategy, showing the junction temperature of one die per switching group. The thermal balancing is triggered at $t = 20\,s$, and the temperatures are perfectly balanced. 106
5.13 Electrical results of the pulse-shadowing strategy, showing the gate commands (S_x), one IGBT/diode current (I_{s1}), output voltage (V_{out}) and current (I_{out}) 107
5.14 Steady-state thermal analysis of the pulse-shadowing strategy: (a) Without balancing. (b) With balancing. 108
5.15 Turn-off process of an IGBT under inductive load. 109
5.16 Physical structure of an IGBT. 110
5.17 Schematic and flowchart of the two double pulse tests applied to the DUT to demonstrate the effects of I_c - 1 and 0.5 pu - on the turn-off time of IGBTs. 111
5.18 Experimental results for the turn-off of an $1.2\,kV/\,25\,A$ IGBT for different currents. (a) $25\,A$ (b) $12.5\,A$. 112
5.19 Pulse pattern of the turn-off losses manipulation strategy, whereby the hottest device - or SW - has its duty time reduced and turned-off before the others, in soft-switching. 113
5.20 Implementation schematic of the on-off control based on turn-off losses manipulation for thermal balancing, with online $t_{off-red}$ calculation. . . 113
5.21 Transient thermal results of the on-off control with pulse-shadowing strategy, showing the junction temperature of one die per switching group. The thermal balancing is triggered at $t = 20\,s$, and the temperatures are perfectly balanced. 114
5.22 Electrical results of the turn-off losses manipulation, showing the gate commands (S_x), one IGBT/diode current (I_{s1}), output voltage (V_{out}) and current (I_{out}) 115

5.23 Steady-state thermal analysis of the turn-off losses manipulation strategy: (a) Without balancing. (b) With Balancing. 115
5.24 Finite element analysis comparison for the presented thermal balancing strategies: (a) Without Balancing (b) Pulse-Shadowing (c) Turn-on Losses (d) Turn-off Losses. 116
5.25 Flowchart of the thermal stress reduction in MCM diodes by acting on the thermal spread. 119
5.26 Finite element analysis of the thermal balancing for MCMs in reverse power flow applications: (a) Without thermal balancing (b) With thermal balancing. 120
5.27 Flowchart of the pre-programmed thermal balancing for load cycling applications, with selective T_j sensing process under reduced load. . . . 121
5.28 Validation of the die-level V_{ce} sensing, pre-programmed thermal balancing and transient performance of the turn-off losses manipulation strategy. The pulse pattern is defined with 7.5 A by sensing the T_j, and it is repeated for 15 A and 23 A keeping the temperatures balanced during the whole power cycling. (a) Current profile. (b) Junction temperature of each device. 122
5.29 (a) Dc-Link current of the mine hoist system mission profile under reduced load, whereby the pulse-pattern of the thermal balancing strategies are obtained with a full T_j sensing capability, a shown in green. The adopted thermal balancing strategies according to the power flow, are also highlighted in red. (b) Junction temperature of each die inside the MCM for the mission profile with reduced load, whereby the temperatures are sensed, balanced and the pulse-pattern is defined. . . 123

5.30 FEM-based temperature analysis for the mine hoist mission profile considering the following thermal balancing strategies: (a) None (b) Pulse-Shadowing in direct power flow and diode stress reduction in reverse power flow (c) Turn-on Losses in direct power flow and diode stress reduction in reverse power flow (d) Turn-off Losses in direct power flow and diode stress reduction in reverse power flow 124
5.31 Die-level reliability analysis for the mine hoist system considering the presented thermal balancing strategies (a) Statistical Analysis (b) Unreliability Analysis. 125
5.32 Hardware schematic of the Multi-gate driver structure for control and monitoring of multi-gate MCMs. 127
5.33 Validation Setup consisting of: an equivalent multi-gate multichip power module in two heatsinks, driver board, V_{ce} sensing, variable load and infrared camera : (a) Wide view of the open three-dies module, V_{ce} sensing and drivers. (b) Schematic. 129
5.34 Validation system with equivalent multi-gate multichip modules : (a) Output waveforms (b) Thermal distribution on the equivalent multichip module. 130

A.1 Transient performance of the V_{on} sensing circuit, using a square wave generator with duty cycle of 0.5 and switching frequencies of: (a) $5\,kHz$ (b) $10\,kHz$ (c) $15\,kHz$ (d) $20\,kHz$ 139
A.2 Steady-state validation of the sensing circuit showing an output voltage for V_{on} (pink) and V_{filter} (green) with a fluctuation of around $5\,mV$ (a) Full view (b) Zoom. 140

B.1 Induction machine equivalent magnetic circuit. 143
B.2 Simulation of the induction machine with equivalent magnetic circuit parameters under nominal load (a) Line voltages (b) Stator Currents. . 143
B.3 Photo of the electrical system of the mine hoist. 144

B.4 Indirect field orientation control for a three-phase induction machine. . 145

B.5 Frequency response of the system, for the current loop. 146

B.6 Frequency response of the system, for the speed loop. 147

B.7 Time domain response of the IFOC applied in the selected induction machine: (a) Reference and measured speed (b) Electrical and load torque. 148

Symbol and Abbreviation List

MCM *Multichip Modules*;

MCIA *Mission Critical Industry Applications*;

DFR *Design for Reliability*;

CM *Condition Monitoring*;

TB *Thermal Balancing*;

ATC *Active Thermal Control*;

DL *Die-Level*;

ac *Alternate Current*;

dc *Direct Current*;

MMF *Magneto-motive force*;

FEM *Finite Elements Model*;

EOL *End of Life*;

PDF *Probability Density Function*;

CDF *Cumulative Density Function*;

TSEP *Thermal Sensitive Electrical Parameters*;

APP *Aging Precursor Parameter*;

DUT *Device Under Test*;

ADC *Analog-Digital Converter*;

SW *Switching Group*;

IGBT *Insulated Gate Bipolar Transistor*;

LC *Lifetime Consumption*;

RUL *Remaining Useful Lifetime*;

EOL *End of Life*;

PWM *Pulse-Width Modulation*;

T_j	*Junction Temperature*;
T_{jm}	*Mean Junction Temperature*;
ΔT_j	*Thermal Cycle Amplitude*;
V_{on}	*On-State Voltage*;
V_{ge-th}	*Gate-Emitter Threshold Voltage*;
V_{ge}	*Gate-Emitter Voltage*;
V_{ce}	*Collector-Emitter Voltage*;
V_{dc}	*Dc-link Voltage*;
V_{ds}	*Drain-Source Voltage*;
I_c	*Collector Current*;
R_{g-int}	*Internal Gate-Resistance*;
R_{g-ext}	*External Gate-Resistance*
t_{d-off}	*Turn-off Time Delay*;
L_{kE}	*Kelvin-Emitter Parasitic Inductance*;
I_{css}	*Saturation Current*;
I_{sc}	*Short-Circuit Current*;
V_f	*Diode Forward Voltage Drop*;
V_{iso}	*Isolated On-State Voltage*;
V_{fil}	*Filtered On-State Voltage*;
C_{gc}	*Gate Capacitance*;
C_{ox}	*Oxide Capacitance*;
V_{gp}	*Miller-Plateau Capacitance*;
ΔI_{ch}	*MOS-Chanel Current*;
W_{cd}	*Depletion Layer*;
T_L	*Load Torque*;
n	*Machine Speed*;
η	*Efficiency*;
I_L	*Load Current*;
F_{System}	*Component Unreliability*;
F_{System}	*System-Level Unreliability*;
FIT	*Failure in Time*;
9PIM	*Nine-phase Induction Machine*;

Chapter 1

Introduction

Contents

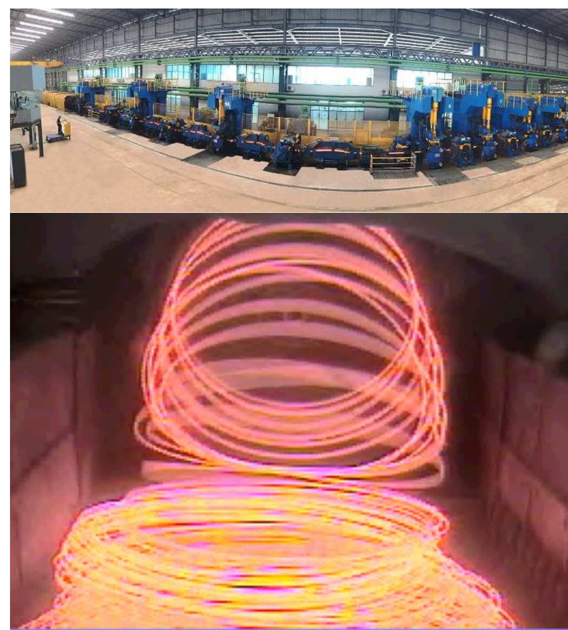
1.1 Mission Critical Industry Applications 3
1.2 Thermal Mismatches in MCM-based Power Converters 5
1.3 Research Proposal 6
1.3.1 Target 1 - Thermal Balancing in MCM-based Mission Critical Power Converters 6
1.3.2 Target 2- Reliability-Oriented Design for MCM-based Mission Critical Applications 7
1.4 Thesis Structure 7
1.4.1 Publications During the Doctoral Project 8

1.1 Mission Critical Industry Applications

In Industry, a single failure may lead to high financial losses due to long production pauses, parts replacement, travel for maintenance and penalty charges [1]. However, the high power demand and critical load variation of many deep mining extraction and steel industry processes, challenge the design of their power electronics systems. The steel industry, is nowadays the worlds most important material, with an annual production over 1.5 billion tons [2]. The rolling mills, shown in Fig. 1.1 (a), is a widely used process, whereby the mill is responsible for controlling the strip speed in precise limits to provide high production and quality of the final product [2]. Wire rod plants, shown in Fig. 1.1 (b), are composed by 30 stands responsible for reducing the cross-section of a metal bloom, and produce steel for automobile components, barbed wires, wire ropes and hardware manufactures [3]. In such application, vibration in the finishing-blocks, reduces the quality of the coil formation. Therefore, a ripple free robust torque control is required for the best wire-rod winding formation [3].

The deep gold ore mineral extraction is carried out through several levels, whereby the ore is drilled and transported to its first crushing stage. After that, it is transported

(a)



(b)

Figure 1.1: Steel industry plants (a) Rolling Mills (b) Wire Rods.

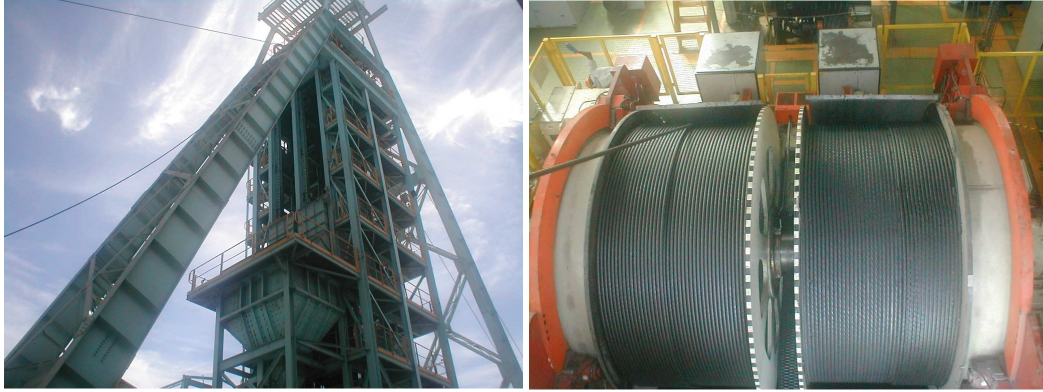


Figure 1.2: Photo of the gold ore mine hoist plant.

to the surface, and according to the characteristics of the ore body, there are guidelines indicating the proper method of transportation. In gold deposits of more than 500 meters in depth, for example, the use of electrical driven mine hoist, shown in Fig. 1.2, is qualified as the preferred solution [4]. The mine hoist is responsible for the transportation of the overall gold ore production and the mining workers; therefore, its reliability is of utmost importance to ensure continuity of service and preserve human lives.

In addition to the high reliability requirements, the vertical hoist acceleration and the bidirectional rolling process with material thickness variation, result in very critical mission profiles, as shown in Fig. 1.3. Thereby, the torque (T_L) and velocity dynamics (w^*) with eventual overload conditions, result in highly dynamic power variation, and ultimately critical thermal cycling for the power semiconductor devices.

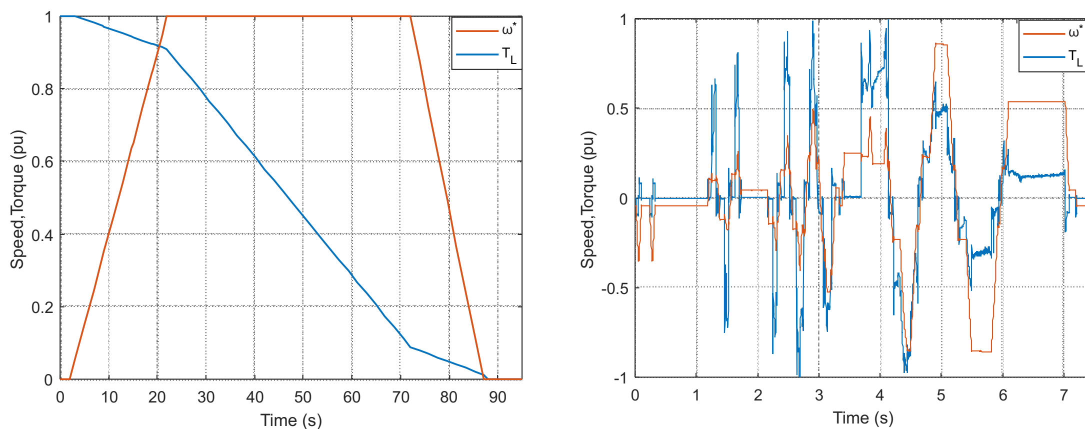


Figure 1.3: Mission profile of critical industry applications (a) Mine hoist systems (b) Steel rolling mills system.

1.2 Thermal Mismatches in MCM-based Power Converters

Multichip power modules (MCM) are widely adopted in mission critical industry applications, due to its high power density, ease of maintenance and instalation [5, 6]. The MCM, is a very engaging solution containing a plurality of chips inside the same package, shortening the interconnection time, whereas decreases weight and size [7]. Consequently, the MCM has been widely adopted in high power density applications over hundred of amperes [8]. Conversely, the incessant desire for miniaturization has been shrinking the package area without reducing - or even increasing - the number of chips, thereby resulting in parametric - circuit and device - deviations, thermal cross-coupling, inhomogeneous thermal resistances and ultimately, thermal mismatches among the dies and modules, as shown in Fig. 1.4 [7, 9, 10, 11, 12, 13, 14]. Indeed, high temperatures affects multiple failure mechanisms of power modules and has been reported as the root cause of most failures in industry [1, 15, 16, 17, 18, 19, 20, 21]. Consequently, an extra temperature in a subset of devices facing critical thermal cycling of mission critical industry applications, reduces the reliability of their power electronics converters [1, 20, 21].

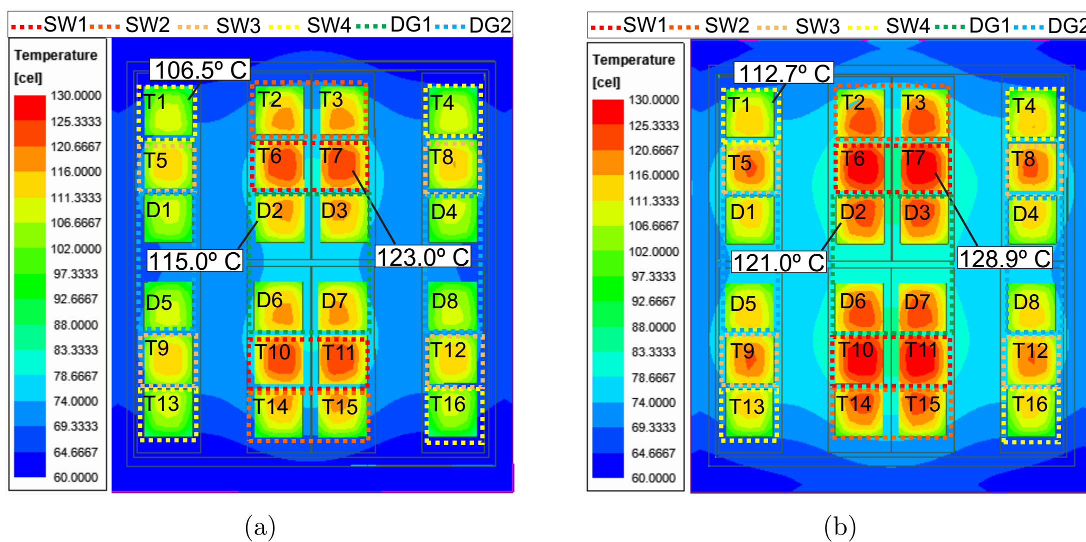


Figure 1.4: Temperature distribution in a 24-dies MCM obtained from FEM analysis for the same power and different cooling flows (a) $h = 4440\,W/K.m^{-2}$ (b) $h = 3960\,W/K.m^{-2}$.

1.3 Research Proposal

This work, proposes and investigates reliability-oriented solutions to mitigate the effects of thermal mismatches and improve the reliability of MCM-based mission critical industry applications (MCIA). Therefore, four novel strategies to balance the power among dies and modules of non-modular high power MCM-based converters, are presented and deeply investigated. Furthermore, the addition of a die-level thermal and failure probability analysis is proposed to improve the design for reliability of MCM-based power converters

1.3.1 Target 1 - Thermal Balancing in MCM-based Mission Critical Power Converters

In the last 30 years many solutions have been proposed to solve thermal unbalance in MCMs such as: thermal optimization design, modified layout and optimized water cooling systems [7, 9, 22, 23, 24, 25, 26, 27]. Nevertheless, the increasing power density demand and the advent of new technologies stills affecting the thermal balancing in multichip modules, and critical thermal deviations have been recently reported [28, 29]. Besides the thermal mismatches among the dies; inhomogeneous air cooling, aging process and power unbalance among phases, can potentially result in thermal deviation among the modules of high power converters, as shown in Fig. 1.4. In modular systems, active thermal control and power routing strategies have been proposed to redistribute the power among their modules and alleviate the most thermally stressed devices [30, 31, 32]. However, the standard structure of MCMs and the non-modularity of three-phase power converters limit the application of such strategies.

Therefore, the first research target is to propose and investigate solutions to balance the temperature among dies and modules in MCM-based power converters. Thereby, a die-level thermal balancing based on a more flexible MCM structure is introduced, and its capability to increase the reliability of MCM-based power converters is investigated. Moreover, a power routing strategy for multiphase drives is proposed, whereby the

power is distributed to overcome thermal mismatches among different MCMs without affecting the electromagnetic machine performance.

1.3.2 Target 2- Reliability-Oriented Design for MCM-based Mission Critical Applications

The design for reliability (DFR) has been widely applied in mission critical application power converters, whereby power modules and cooling systems are designed aiming at achieving a predefined lifetime [33, 34, 35, 36]. The proposed methods, however, do not consider the thermal mismatches and the high number of devices prone to failure is neglected, which potentially results in less realistic reliability levels in MCM-based power converters.

Therefore, the second research target is to propose a die-level thermal and probabilistic analysis in the design for reliability of MCM-based power converters. In this proposal, the temperature of each die is obtained through finite elements analysis, rather than using simplistic thermal models. Moreover, the failure probability of each die is calculated and combined to obtain the power converter system-level reliability.

Complementary Contributions

As a complementary contribution, the capability of an on-state voltage (V_{on}) based junction temperature (T_j) sensing circuit to feedback thermal balancing strategies, is experimentally demonstrated.

1.4 Thesis Structure

This thesis is organized in six chapters, as shown in Fig. 1.5. In the first chapter, the influences of temperature on the failure mechanisms of power semiconductor devices, are explained. The first contribution is presented in Chap. 3, whereby the impacts of a die-level thermal and reliability analysis on the design for reliability pro-

cedure is demonstrated. Thereafter, in Chap. 4, a state-of-the art of the methods to monitor and control the temperature in power devices is described, and a power routing strategy for multiphase drives, is proposed. Furthermore, V_{on}-based T_j sensing circuit is implemented and its capability to feedback thermal balancing strategies, is demonstrated. Based on the presented thermal control solutions, pulse processing based thermal balancing strategies are presented in Chap. 5. In addition, the impact of the thermal balancing on the lifetime and efficiency of mission critical industry applications, are evaluated. Finally, the conclusions are stated and future research topics based on this thesis are suggested in Chap. 6.

1.4.1 Publications During the Doctoral Project

Conference

The conference publications correlated to the doctoral research project are summarized as follows:

- - [K1] Power Routing to Enhance the Lifetime of Multiphase Drives (ECCE 2019)
- - [K2] Active Redundancy in the Low Voltage Stage of Smart Transformers (ECCE 2018)

Journal

The journal publications correlated to the doctoral research topic are summarized as follows:

- - [J1] Design and Selection of High Reliability Converters for Mission Critical Industrial Applications: A Rolling Mill Case Study (Transactions on Industry Applications)
- - [J2] Mission Critical Analysis and Design of IGBT-based Power Converters Applied to Mine Hoist Systems (Transactions on Industry Applications)

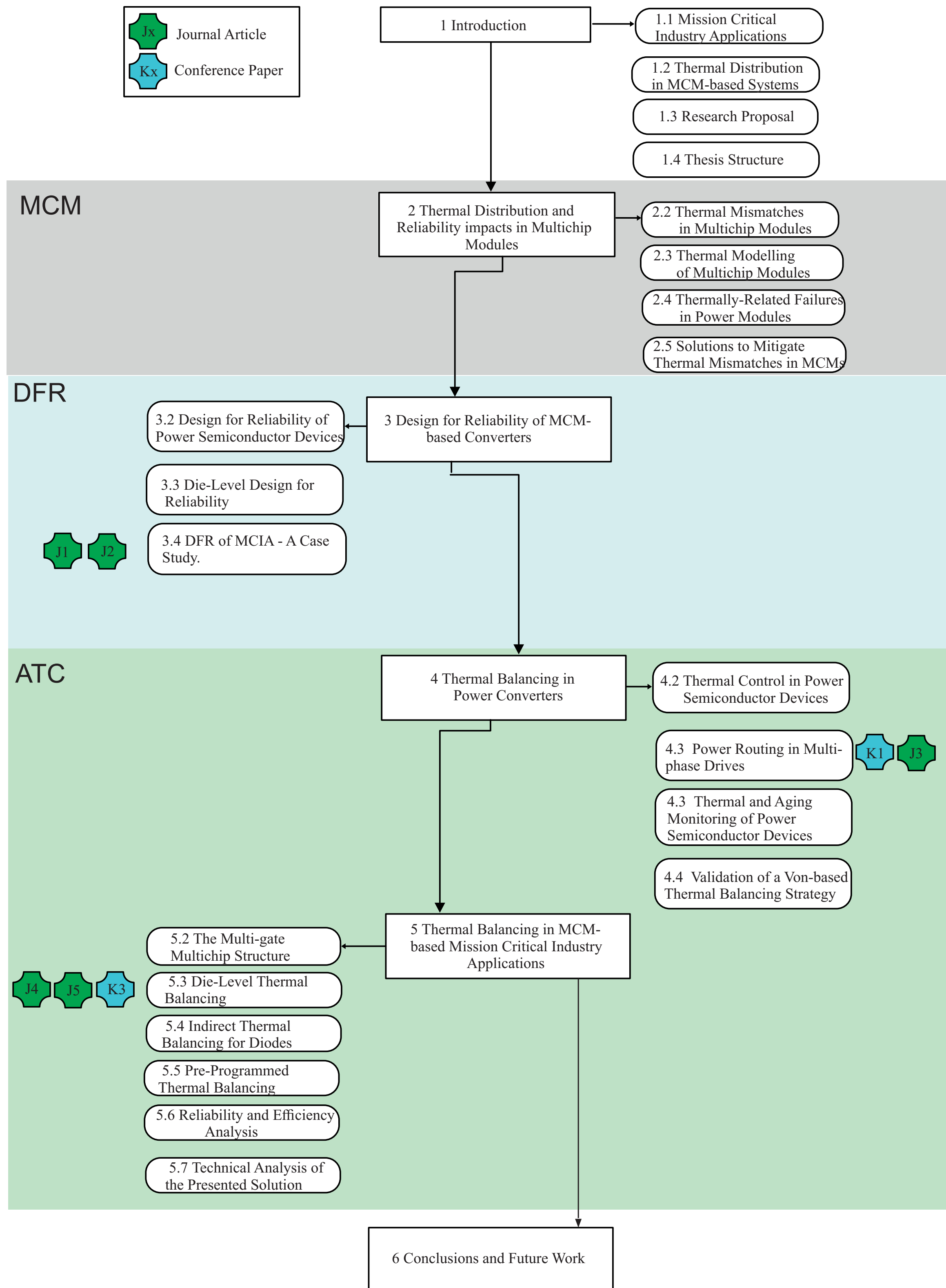


Figure 1.5: Thesis organization and related publications.

- - [J3] Soft-Unbalance Operation for Power Routing in Multiphase Drives (Transactions on Industry Applications)

- - [J4] Pulse-Shadowing based Thermal Balancing in Multichip Modules (Transactions on Industry Applications).
- - [J5] Selective Soft-Switching in Multichip Systems (Journal of Emerging and Selected Topic in Power Electronics).

Chapter 2

Thermal Distribution and Reliability Impacts in Multichip Modules

Contents

2.1 Introduction 12
2.2 Thermal Mismatches in Multichip Power Modules 13
2.2.1 Current Unbalance 14
2.2.2 Thermal Cross-Coupling 17
2.2.3 Cooling Challenges 18
2.3 Thermal Modeling of Multichip Modules 19
2.3.1 Equivalent Thermal Networks 19
2.3.2 FEM-based Thermal Modeling 21
2.3.3 Thermal Validation 25
2.4 Thermally-Related Failures in Power Modules 27
2.4.1 Instabilities 27
2.4.2 Severe Overloads 28
2.4.3 Wear-out failures in power modules 29
2.4.4 Accumulated Degradation Unevenness in MCMs 30
2.5 Proposed Solutions to Mitigate Thermal Mismatches in MCMs 31
2.6 Short Summary of the Chapter 32

2.1 Introduction

Multichip power modules (MCMs) are widely adopted in high power converters, and it is expected to still the standard solution in a foreseeing future [37, 38]. MCMs are indeed a very engaged solution with small size and short commutation loops; how-

ever, the high number dies in limited space result in thermal deviations and, consequently, extra temperature in specific dies [8, 17, 39, 40, 41]. Indeed, high temperatures have a strong influence on multiple failure mechanisms of power devices, and has been reported as the root cause of most failure events in industry [1, 15, 16, 17, 18, 19, 20, 21]. This chapter, presents the causes and reliability impacts of extra temperature in specific dies of a multichip modules. To demonstrate the uneven thermal distribution, a finite elements model of a 24-dies MCM is constructed.

2.2 Thermal Mismatches in Multichip Power Modules

For high power semiconductor devices two options are available in the market: press-pack technology and power modules. Although the first one has high power density, low failure rate and small thermal resistances, the multichip power module technology has been widely adopted mainly because of its lower price, ease of maintenance and installation [42]. As shown in Fig. 2.1, the power module is composed by several layers. A single-die power module, for example, is composed by a Silicon (Si) chip soldered in a direct copper-bonded (DCB) substrate, and contacted on the top side by aluminum (Al) bond wires. The DCB, insulates the chip from the base plate and conducts the heat dissipated to the cooling system [43].

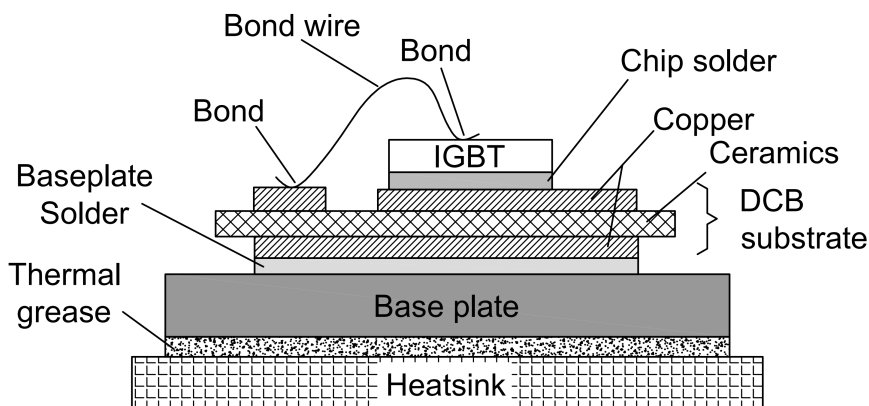


Figure 2.1: Power module structure.

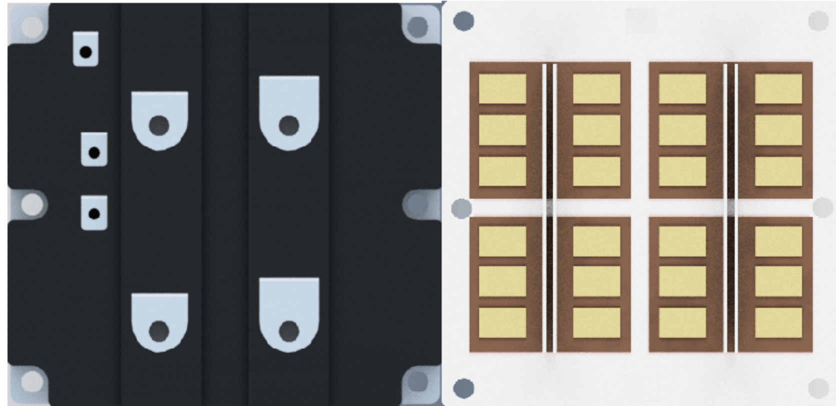


Figure 2.2: Multichip power module: single-switch, 1.7 kV / 1600 A, 16 IGBTs and 8 diodes in a 140 x 130 cm structure.

To achieve high current capability a multichip module structure is adopted, whereby several semiconductors are connected in parallel inside the same package. The MCM is a very engaging solution which reduces size and shorts interconnections of parallel devices to obtain very compact high current switches - up to 3600 A [7]. Fig. 2.2, shows an 1.7 kV / 1600 A single-switch, whereby 16 IGBTs and 8 diodes are embedded in a 140 x 130 cm structure. Although the MCM is a very engaging structure, its design is quite challenging, and multiple factors influence thermal mismatches among the dies, as detailed in sequence.

2.2.1 Current Unbalance

Transient and static current unbalances impact directly the performance of MCMs, thereby generating thermal mismatches among the devices. There are many factors influencing the current distribution among the parallel devices, such as circuit mismatches, device parametric variations and temperature influences, as detailed in sequence.

Circuit Mismatches

The equivalent circuit of parallel devices is shown in Fig. 2.3. The switching loop (L_C) and common emitter (L_E) stray inductance, are the main causes of current unbal-

ance in this structure [44]. L_E affects the switching characteristics, whereby the device with larger L_E turns on and off slower taking less and more current in both process, respectively. Conversely, L_C impacts on the on-state voltage (V_{on}) during switching transient, thereby affecting the on-state current balancing in case of inductive load current [44].

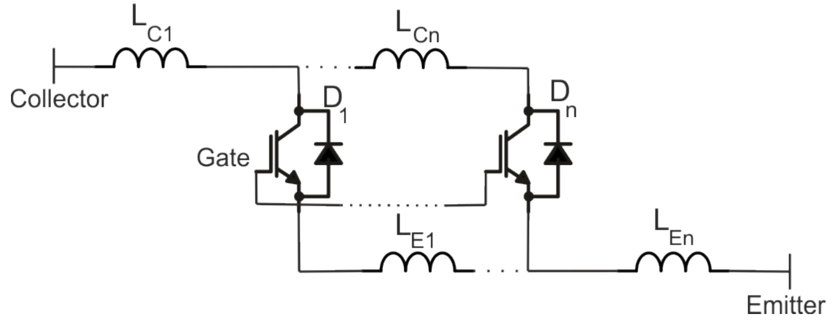


Figure 2.3: Equivalent circuit of single-switch MCM with N parallel dies.

A comprehensive analysis of circuit influence in transient currents is conducted in [40], whereby the stray inductances are measured for a six-chips structure considering five different frequencies. At 10 KHz, the stray inductance inside the module can vary between 34 nH to 86 nH, thereby resulting in peak current deviations of up to 200 A during the turn-on process. Consequently, the devices with lower equivalent series inductance can reach up to twice of the switching losses comparing to the other ones.

The Kelvin emitter influences on the current sharing is also studied, showing a higher parasitic asymmetry and consequently higher current unbalance and losses increase in up to 20 %, for a three-chips structure [14].

Temperature Influences

The gate-emitter threshold voltage V_{ge-th} is a crucial parameter influencing the current distribution among parallel devices [45, 46]. Such parameter is related to the Fermi energy ϕ_{FB}, which is in turn dependent to the junction temperature as shown in 2.1 [47]:

$$\phi_{FB} = \frac{kT_j}{q} ln \frac{N_{Amax}}{n_i} \tag{2.1}$$

Therefore, the correlation of V_{ge-th} with ϕ_{FB} shown in 2.2 makes the gate-emitter voltage also dependent on the temperature, with a variation defined in 2.3 [46]:

$$V_{ge(th)} = -V_{ms} - \frac{Q_{ss}}{C_{ox}} + 2\phi_{FB} + \frac{\sqrt{2\epsilon_o\epsilon_{si}qN_{Amax}(2\phi_{FB})}}{C_{ox}} \tag{2.2}$$

$$\frac{dV_{ge(th)}}{dT_j} = \left[\frac{\phi_{FB}}{T_j} - \frac{k}{q}(\frac{E_g}{2kT_j} + 1.5)\right](2 + \frac{\sqrt{2\epsilon_o\epsilon_{si}qN_{Amax}(2\phi_{FB})}}{2\phi_{FB}C_{ox}} \tag{2.3}$$

Therefore, looking at 2.2.1, it can be concluded that the gate threshold voltage is inversely proportional to T_j. V_{ge-th} in turn, influences the turn-on delay time t_{d-on} as shown in 2.4 :

$$t_{d-on} = -R_G(C_{GE} + C_{GC}) \cdot ln\left(1 - \frac{V_{ge-th}}{V_{ge}}\right) \tag{2.4}$$

From the variation of V_{ge-th} with T_j demonstrated in , the t_{d-on} variation with T_j can be obtained as shown in 2.5 [46]:

$$\frac{dt_{d-on}}{dT_j} = -\tau_1\left(\frac{V_{ge(th)}}{V_{(ge)} - V_{ge(th)}}\right) \cdot \frac{dV_{ge(th)}}{dTj} > 0 \tag{2.5}$$

The turn-off delay time derivation is similar to the t_{d-on}, and according to 2.5, both are increasing function of the junction temperature. Fig. 2.4, shows the thermal impacts on the turn-on and turn-off times of an IGBT, obtained from reference [46]. When a parallel IGBT has shorter t_{d-on} or longer t_{d-off} it takes more current than

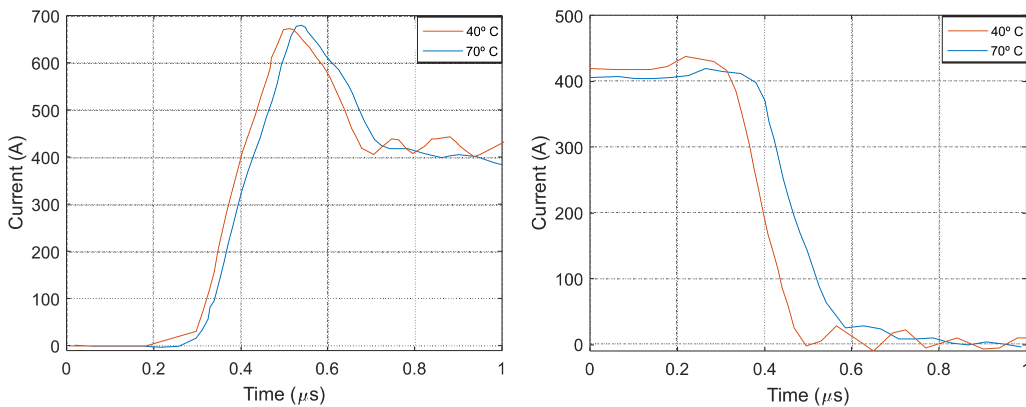


Figure 2.4: Thermal impacts on the transient time of Si IGBTs (a) Turn-on (b) Turn-off.

the others, thereby influencing the transient current during the switching process of parallel devices [46].

Considering the carrier mobility as decreasing function of T_j, V_{on} is also proportional to the temperature which directly influence the static current balancing, as shown in 2.6 [46]. The temperature dependency of the on-state voltage, has a negative coefficients at high load conditions; therefore, the temperature act reducing the thermal mismatch, since hotter devices has lower conductivity and carry less current [48]. The temperature impact on a Si IGBT device is shown in Fig. 2.5, which is obtained from reference [48].

$$V_{on} = I_c R_{ch} = \frac{I_c l}{z\mu_{ns}(T_0)(T_j)^{-m} C_{ox}(V_{ge} - Vge(th))} \tag{2.6}$$

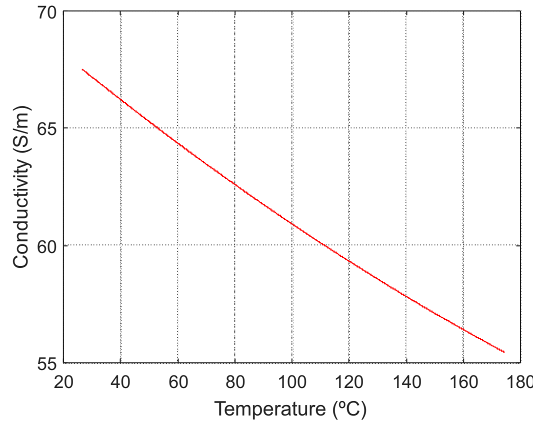


Figure 2.5: Impact of the temperature on the conductivity of Si IGBTs.

2.2.2 Thermal Cross-Coupling

The thermal cross-coupling is defined by the impact of the heat spreading of one device on its neighbors, which mainly depends on the power level and chip positioning [9]. Thereby, for a specific power and chip distance, one device induce a proportional thermal stress on the others. Consequently, several chips processing high power over very close distances result in critical cross-coupling effects [9]. Considering multichip modules which are designed for high power density, the devices are placed relatively

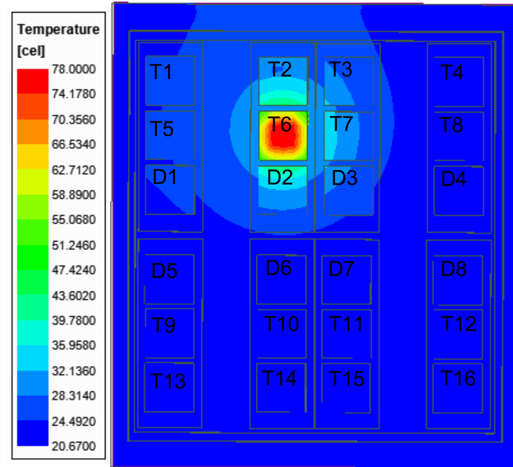


Figure 2.6: Thermal cross-coupling effects: a heat source is generated in one device and the temperature spread on its neighbors.

close - as shown in Fig. 2.6. As a result, the thermal spread of one device has high influences on the temperature of its neighbors.

2.2.3 Cooling Challenges

In MCMs, the dissipation power per unit is bigger, and the removal of heating from this structure is more challenging [13]. In addition, some chips can be up to 18 cm distant from each other, as shown in Fig. 2.7, and it is hard to obtain homogeneous cooling in the whole structure [13]. In air cooling systems, for example, the chips near to the fan has lower thermal resistance comparing to the ones in the other extreme.

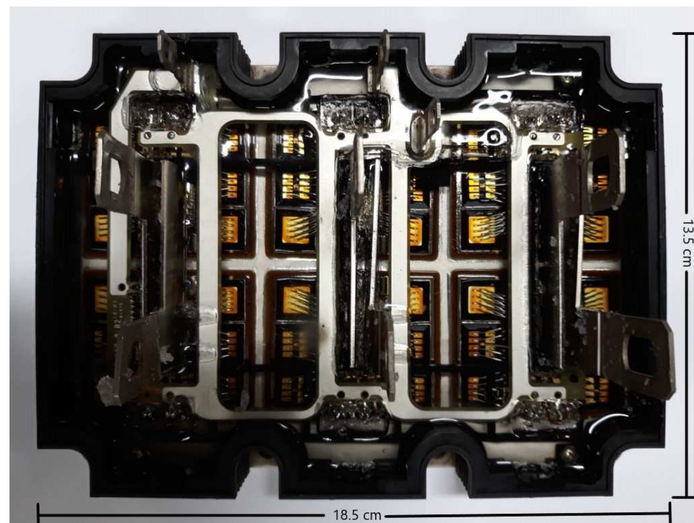


Figure 2.7: Dimensions of a multichip power module with 36 dies.

2.3 Thermal Modeling of Multichip Modules

The thermal model of a power module, is composed by an equivalent circuit based on the thermal impedance (Z_{th}) of its different layers. $Z_{th(x,y)}$ is defined by the temperature difference measured in point x to y, divided by a step change of power dissipation [49]. As shown in Fig. 2.8, the impedance $Z_{th(j-c)}$, $Z_{th(c-h)}$ and $Z_{th(h-a)}$ are referred to the heat dissipated between the die and the module encapsulation; the package and the heatsink and from the heatsink to the environment, respectively [50].

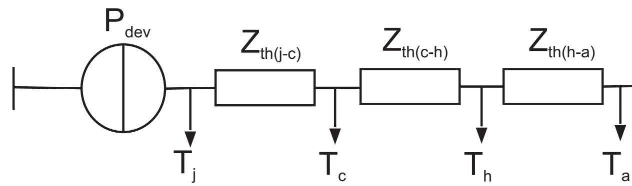


Figure 2.8: Dynamic thermal model of power modules with heatsink.

2.3.1 Equivalent Thermal Networks

The equivalent thermal model, in turn, is usually represented by resistance and capacitance (RC) thermal network, whereby thermal resistance R_{th} and capacitance C_{th} are cascaded connected to represent the thermal behavior of the materials [51]. Thereby, there are two traditional ways to obtain the thermal model of a power module, as described in sequence.

Cauer Model

The first one is the cauer Model, which is based on the geometry and property of the materials of each layer, which gives physical sense to each power module thermal capacitance and resistance. As shown in Fig. 2.9, the number of RC modules is defined by the number of layers within the IGBT [51].

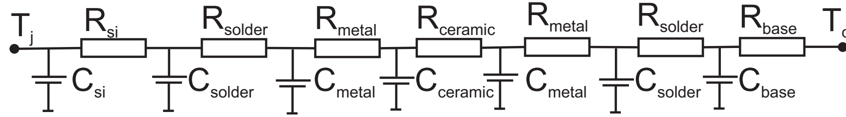


Figure 2.9: Cauer thermal model.

Foster Model

The foster model shown in Fig.2.10, however, is a mathematical approximation without any physical behavior [51]. This model, is obtained from fitting parameters of transient thermal tests, such as the one shown in Fig.2.11. The analytical formula that relates the thermal impedance to the thermal resistance is represented by 2.7, whose parameters are in general provided in datasheets:

$$Z_{th(j-c)}(t) = \sum_{i}^{n} R_i(1 - e^{\frac{-\tau}{\tau_i}}) \qquad ; \qquad \tau_i = R_i.C_i \tag{2.7}$$

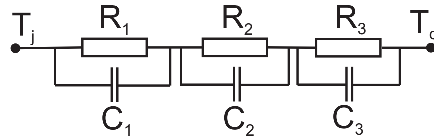


Figure 2.10: Foster thermal model.

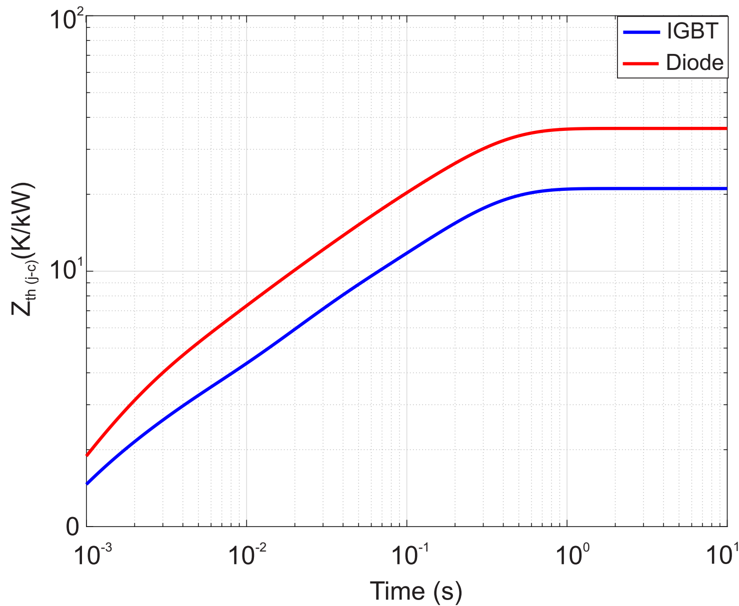


Figure 2.11: Impedance curves used to obtain the power module equivalent foster network.

Heatsink Thermal Modeling

As previously shown in Fig. 2.1, the power module is placed over a heatsink to increase its warm dissipation capability. The heatsink, in turn, is commonly aided by a cooling system to increase its heat transfer capability and achieve high power density. The forced air is the standard solution for applications with low cooling demand; however, to achieve a high thermal performance, fluid cooled systems are required [50]. Thereby, the cooling system selection with specific flow rate, pressure, concentration and fluid temperature directly affects the steady-state (R_{th}) and transitory (τ) thermal resistance. Although many factors influence the dynamics of a heatsink system, its thermal model is commonly obtained by the aforementioned Cauer and Foster approaches.

2.3.2 FEM-based Thermal Modeling

Although equivalent thermal networks have been adopted for the design of power converters, they are not capable of reflecting the effects of thermal mismatches inside a multichip module. In addition, a die-level thermal analysis is not possible, whereby only an overall junction temperature can be calculated. Therefore, to obtain a more accurate thermal behavior of multichip modules, and validate the thermal distribution, a finite elements (FEM) based modeling is implemented in this work. Hence, a 24-dies MCM structure previously shown in Fig. 2.2 is modeled in the FEM software Ansys Icepack. Fig. 2.12, shows a cross section of the model, as well as the dimensions and parameters, where d is the device thickness, λ the thermal conductivity and h the homogenous heat transfer coefficient [52].

Equivalent Thermal Network Extraction

Even though the FEM-based analysis is quite precise, it is not realistic to conduct real-time simulations due to the high computational effort and very long time consumption. Nevertheless, it is possible to obtain an equivalent thermal network

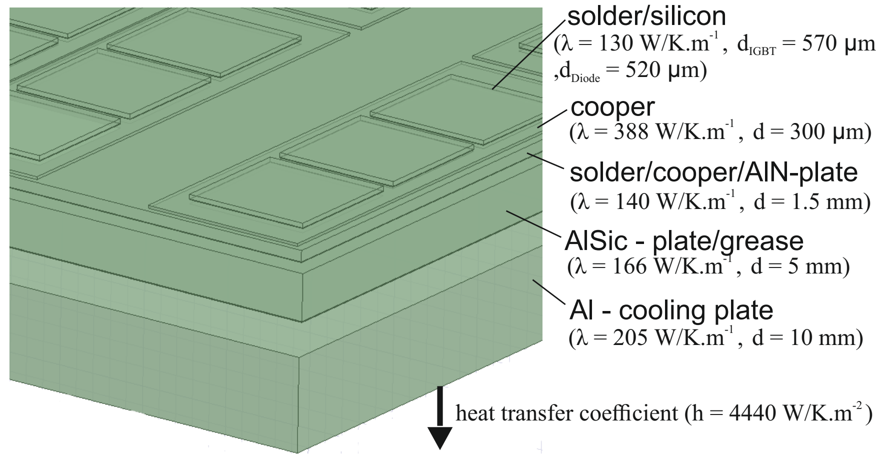


Figure 2.12: Finite Elements Model of a 1700 V/ 1600 A single-switch, with 24-dies.

with self and cross-coupling thermal impedance from the FEM model by using superposition [22, 52]. Thereby, the obtained system of equation can be embedded in an electrothermal simulation software, and enable a faster FEM-based co-simulation procedure.

The Superposition Methodology

The thermal performance of power modules is defined by the thermal impedance $Z_{th}(j-a)$ from the device to the environment. This information is provided by manufacturers in documents such as datasheets, which in case of MCM are represented by the $Z_{th}(j-a)$ of the whole parallel string. Although effective for single-die devices, this parameter is pretty limited for MCMs, due to multiple dies dissipating power inside the same package [53].

One solution is to obtain an effective thermal network is the superposition approach, which account the multiplicity of heat sources inside the package to obtain a matrix of thermal impedance. The principle of superposition to generate the steady-state thermal resistance matrix $R_{th}(j-a)$ was introduced in references [22, 23, 54, 55], and extended in [52] to include the transient behavior $Z_{th}(j-a)$.

In this approach, a known power is the applied - in a controlled environment - to one specific die at a time and the temperature rising of the whole group is measured in every step. Therefore, the matrix representing the self and coupling impedance (Z_{th-x-y}) of

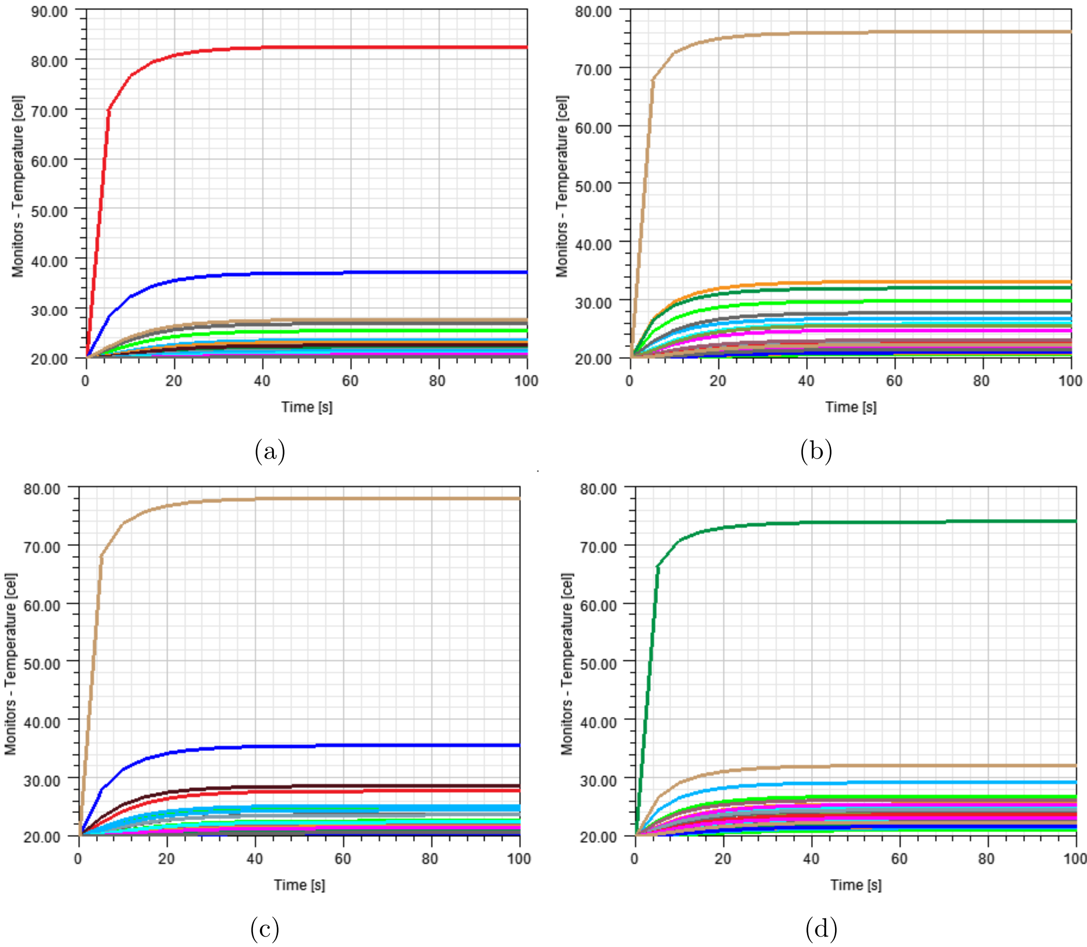


Figure 2.13: Superposition methodology to obtain the equivalent MCM thermal network, whereby the transient curves of all dies are obtained heating a single die at a time. The process is done for each die, but specific ones are shown as examples: (a) T1 (b) T7 (c) D1 (d) D3.

each die can be obtained, where x-y represents the effect of die y on the impedance of die x. This matrix, in turn, can be used to to calculate the junction temperature of each single die (T_{jx}), for a respective dissipated power (P_x), and ambient temperature (T_a), as shown in the equation system below:

$$\begin{bmatrix} T_{j1} \\ T_{j2} \\ \vdots \\ T_{24} \end{bmatrix} = T_a + \begin{bmatrix} Z_{th-1,1} & Z_{th-1,2} & \cdots & Z_{th-1,24} \\ Z_{th-2,1} & Z_{th-2,2} & \cdots & Z_{th-2,24} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{th-24,1} & Z_{th-24,2} & \cdots & Z_{th-24,24} \end{bmatrix} \cdot \begin{bmatrix} P_1 \\ P_2 \\ \vdots \\ P_{24} \end{bmatrix} \tag{2.8}$$

Then, the superposition methodology is applied to the FEM model to extract the impedance matrix of the 24-dies multichip module. Hence, a power loss of 200 W is injected in the FEM model in one die at a time and the transient curves of each device on every step is obtained. Fig. 2.13, shows the transient response of all dies, whereby four (T1-T8, D1-D4) are adopted as examples and fed with 200 W of power at a time. The 24 obtained heating curves - one per single die - are then loaded in a numeric software and fitted to obtain the matrix impedance terms [52]. As shown in Fig. 2.14, each impedance term is represented by a second-order exponential equation.

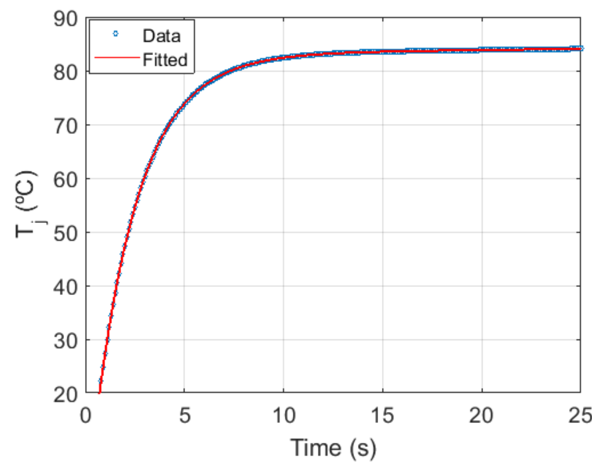


Figure 2.14: Second-order exponential fitting of the transient temperature obtained through FEM analysis, $f(x) = a \cdot e^{bt} + c \cdot e^{dt}$.

FEM-based Electrothermal Simulation

The developed FEM-based simulation structure is shown in Fig. 2.15, with a three-phase converter designed in a electrothermal software containing six equivalent MCMs. To represent the second-order exponential thermal behavior of each die, an equivalent foster circuit is implemented by using the terms obtained from the fitting process shown in Fig. 2.14. The simulation process works iteratively, whereby the losses are obtained from the electrothermal software and used to feed the equation system described in 2.3.2 for the calculation of the T_js. The junction temperatures, in turn, are fed back to the model for the correct measurements of the desirable outputs: losses and temperatures.

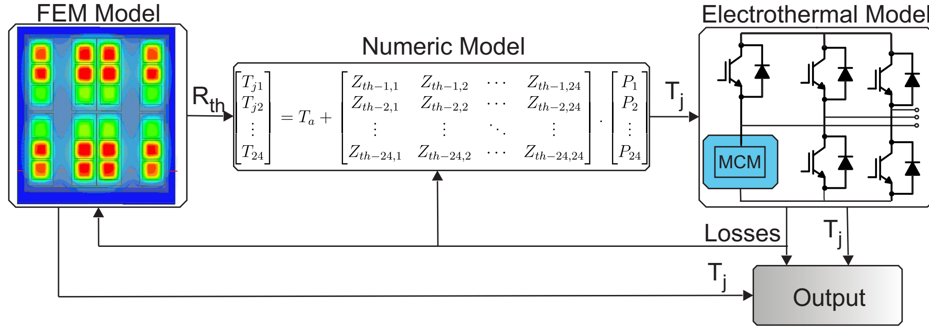


Figure 2.15: Simulation process, where the thermal network is exported from FEM software and embedded in numeric model. The losses are extracted from the electrothermal model and fed back to FEM software. The process works iteratively for losses and temperature analysis.

2.3.3 Thermal Validation

To demonstrate the thermal distribution in a 24-dies MCM, the FEM-based electrothermal simulation is realized considering the parameters stated in Tab. 2.1. Fig. 2.16, shows the steady-state and transient response of the FEM software, whereby the losses are calculated in the electrothermal software. Thereafter, the power losses of each die are applied the same time in the FEM software as a step. As can be seen, there is a thermal deviation of $17.4\,°C$ comparing the middle with the edge transistors (T_x). Moreover, the middle diodes D_x, show higher temperature than the edge transistors even with reduced losses - around $70\,\%$ - due to high cross-coupling effects in its critical positioning on the MCM.

Table 2.1: Simulation parameters for the validation of the thermal distribution.

V_{dc}	980 V
V_{out}	690 V
I_{out}	1000 A
F_{sw}	5 kHz
$cos(\phi)$	1

Thermal Deviation Among Modules

As aforementioned and demonstrated, multiple factors such as thermal cross-coupling, current deviation, inhomogeneous cooling and uneven aging results in thermal mis-

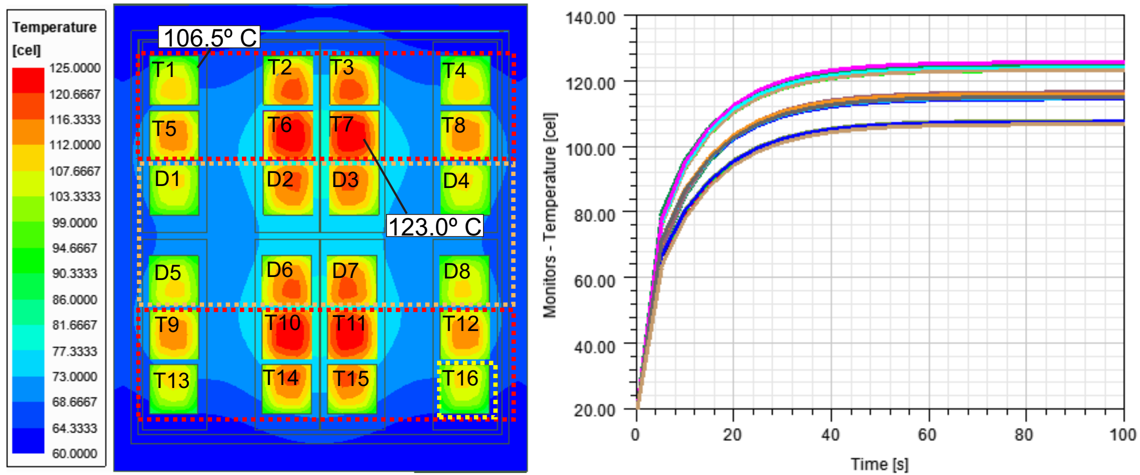


Figure 2.16: FEM analysis of the 24-dies MCM, showing a thermal deviation among the dies of 17.4 $°C$ (a) Steady-State analysis (b) Transient analysis.

matches among the dies and, ultimately, reduced lifetime. Moreover, the same factors can also influence thermal mismatches among different modules, which are not - necessarily - in parallel. To demonstrate this effect, a reduction on the heat transfer coefficient of 10% representing a defect on the water cooling system, is simulated in the FEM model, with the same procedure and parameters described above. Fig. 2.17 (a) shows the thermal results obtained in the FEM software with the standard cooling $h = 4440\,W/K.m^{-2}$ and Fig. 2.17 (b), the results for the defected cooling $h = 3960\,W/K.m^{-2}$. As can be seen, there are temperature differences of around

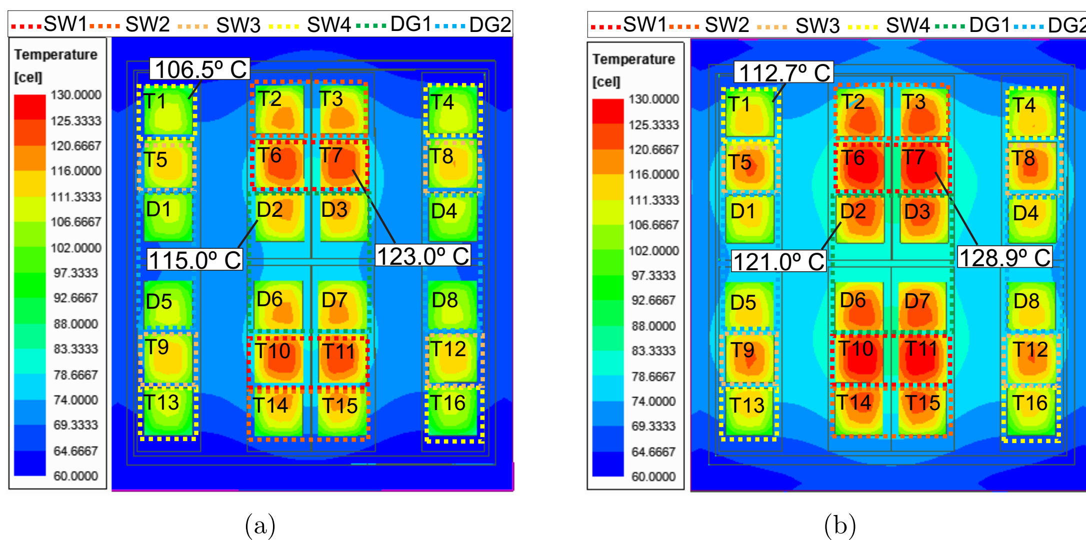


Figure 2.17: Temperature on the 24-dies MCM obtained from FEM analysis (a) Standard cooling system ($h = 4440\,W/K.m^{-2}$) (b) Defected cooling system ($h = 3960\,W/K.m^{-2}$).

$6\,°C$, thereby resulting in a total thermal deviation, from the hottest to the coldest die of the two modules of $22.4\,°C$.

2.4 Thermally-Related Failures in Power Modules

As validated in the previous section, the thermal mismatches in MCMs result in induced extra temperature in a subset of devices. Indeed, the temperature has an influence on multiple failure mechanisms of power semiconductor device, and have been reported as the root cause of most failures in industry [1, 20, 21]. This section, examine the correlations of temperature with the failure mechanisms in power semiconductor devices. In power modules, failures can be classified in wear-out and catastrophic, as shown in flowchart of Fig. 2.18. Looking at the root causes, aging failures are basically due to wear-out of electronic parts, mostly at package level, whereas catastrophic failures basically come from severe overloads and instabilities [15].

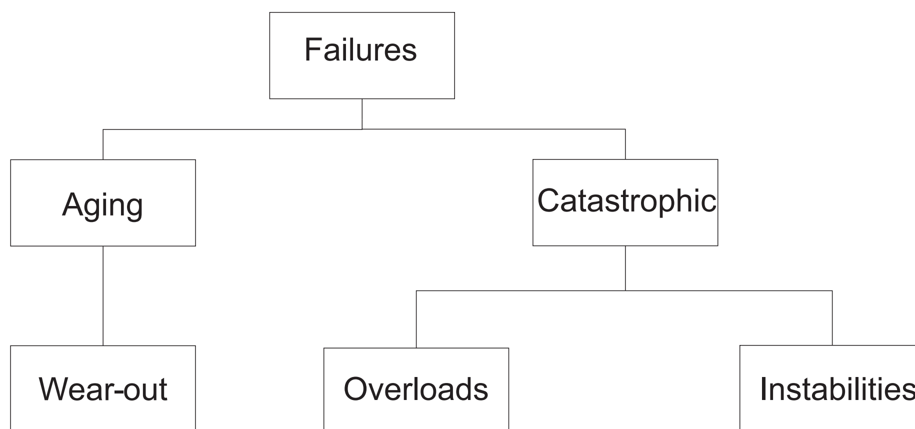


Figure 2.18: Classification of failures in power modules based on root cause. [15]

2.4.1 Instabilities

Instabilities are strongly related to internal aspects, which are characterized by a loss of control that leads to destruction, i.e., whose evolution does not depend on the external circuit but rather only on regenerative phenomena internal to the device [15].

Instabilities are a very dangerous phenomena that must be deeply understood before using power devices. It is worth to noting that neither protection circuits nor control strategies can help in avoiding instabilities because there is no clear external evidence when they occur [15]. However, the understanding of the root causes may help on avoiding potential events.

High temperatures has been reported as root cause of instabilities in the off-state of fast switching diodes [56]. It is demonstrated that the increasing leakage current, due to higher temperature level, can provoke thermal runaway and damage a small region of the junction peripheral surface, thereby resulting in a short-circuit catastrophic event. In power Mosfets, high temperatures can be deterministic for a thermal runaway, when the gate voltages are lower than the stability boundary [57]. The contribution of temperature on instabilities of IGBTs under unclamped inductive switching (UIS) have been also presented. Experimental results have shown a negative resistance under high temperatures, allowing current unbalance in few cells and inducing hot spots in specific regions of the die [58, 59].

2.4.2 Severe Overloads

The temperature can also influence on the failures triggered by severe overloads. When the device exceeds its blocking voltage limits, for example, the high electric field accelerate and generate mobile carriers through impact ionization, thereby creating a significant current flow in the depletion region [47]. As a result, an avalanche breakdown occurs increasing the current and disabling the power device voltage blocking capability. High temperatures contribute to the generation of carriers and can potentially activate a dynamic avalanche breakdown with reduced electric field - i.e lower voltage level [17, 60]. This phenomena has presented higher risk in multichip modules, where thermal deviations can result in a dynamic avalanche breakdown of the hotter devices [17].

The tendency for current filaments during an IGBT turn-off with a current signif-

icantly higher than the nominal is investigated in [19]. The related work demonstrate that the thermal heating during the turn-off is the main reason of a non-extiguishing current filament and the probable cause of device destruction under over current. Furthermore, the temperature can also initiate a thermal activation process according to Arrhenius law, triggering a degradation process in the dies [47]. In fact, the devices have a temperature limit for a safe operation, which varies in general between 125° C and 175° C.

2.4.3 Wear-out failures in power modules

The power module is based on several layers consisting of different materials with different coefficients of thermal expansion, heat conductivity and heat storage, as summarized in Tab. 2.2 [50]. The previously shown Fig. 2.1, display the structure of a single-die power module, which is composed by a Silicon (Si) chip soldered in a direct copper-bonded (DCB) substrate, and contacted on the top side by aluminum (Al) bond wires. The DCB, insulates the chip from the base plate and conducts the heat dissipated to the cooling system, which in turn is composed by a heatsink, and commonly aided by forced air or water cooling system [43].

Table 2.2: Material characteristics of a power module.

Material	Heat Conductivity [W/(m*K)]	Heat storage [$kW/(m^3 * K)$]	Coefficient of Thermal expansion [$10^{-6}/K$]
Silicon	148	1650	4.1
Copper	394	3400	17.5
Aluminum	230	2480	17.5
Silver	407	2450	19
Molybdenum	145	2575	5
Solders	70	1670	15-30
$Al_2O_3 - DBC$	24	3025	8.3
AlN DBC	180	2435	15-30
AlSiC (75% SiC)	180	2223	7

[50]

The temperature is the main factor influencing the aging of power semiconductor

devices, whereby repetitive thermal cycling cause expansion and shrinkage at different rates in the power module materials. As a result, crack growth at the bond wire/chip interface and propagation of cracks or voids between the module substrates, ultimately results in failure by bond wire liftoff or solder fatigue, as shown in Fig.2.19 [16, 61].

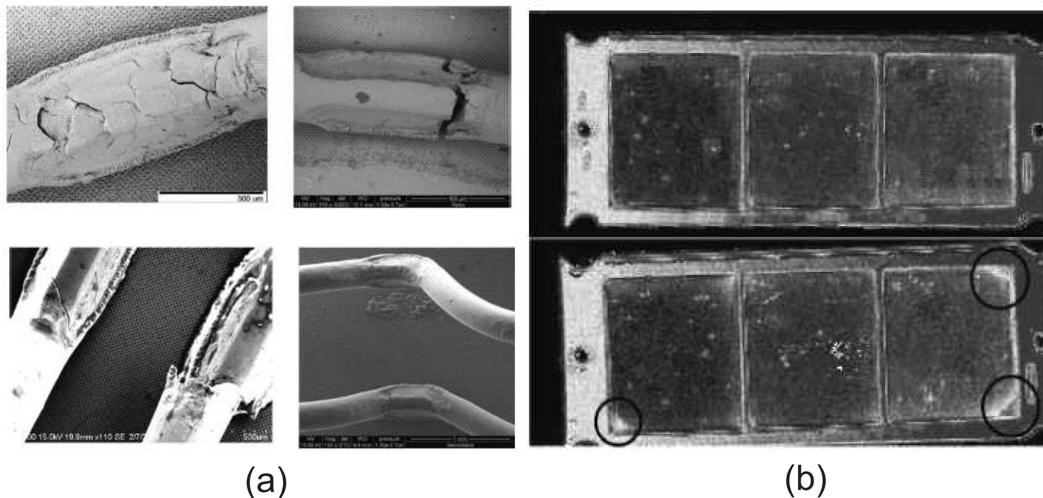


Figure 2.19: Aging failures in power modules (a) Bond wire metallurgic damage, heel crack, fracture and liftoff. (b) Solder damages.
[16]

Thermal cycling can also result in reconstruction of the aluminum metalization due to its different CTE comparing to the Si chip. Reconstruction are mostly more evident in the middle of the dies, where the temperature achieve its maximal [62]. Indeed, surface reconstruction in the middle of the chip operating over $110^{\circ}\,C$ has been demonstrated. Conversely, no noticeable effect on its periphery, which operates under lower temperature has been observed [62].

2.4.4 Accumulated Degradation Unevenness in MCMs

As aforementioned, the power module wear out is directly related to the temperature; therefore, the many factors influencing thermal deviations, ultimately result in degradation unevenness inside MCMs [40, 63, 64]. In long term cycling, this problem become worst, because the aging can increase the device parameters and circuit mismatches, thereby resulting in a cumulative degradation process [44]. Imperfections

caused by oxide traps on the atomic level can vary the V_{ge-th}, thereby decreasing the device turn-on time, increasing losses, temperature and accelerating the aging. Delamination, in turn, can influence the R_{on} changing the conduction losses and the static current distribution among the devices [65]. The liftoff of wire bonds can also impact the current distribution in MCMs by increasing the ohmic resistances of specific devices [66]. Changes in the case temperature (T_c) distribution after aging is also reported impacting the thermal unevenness inside MCMs [67]. Considering a 9-chips MCM, where temperature sensors are placed near each chip, the non uniformity is more significant after aging, and an extra deviation of 6.37° C is measured among the dies. Therefore, case imperfections contributes ultimately to the degradation unevenness inside MCM, and this problem become worst over time [67].

2.5 Proposed Solutions to Mitigate Thermal Mismatches in MCMs

The thermal mismatch has been addressed in the design of power modules to improve thermal and current distribution in MCMs. To reduce static and transient current unbalance, a modified split-output DCB layout is proposed, whereby the common stray inductance and the di/dt mismatches are reduced [68]. To overcome thermal cross-coupling effects, an optimum design based on the position of each chip is proposed in [9]. Indeed, the thermal cross-coupling effects can be eliminated respecting a predefined space among the chips during the design process. Nevertheless, the demand for increasing the power density challenges to keep the distance among the dies. To solve inhomogeneous cooling problems, optimized direct water cooling system shows up as a solution. However the higher cost, size and reduced reliability contradicts the philosophy of safe power electronics miniaturization [69]. As a result, the reliability of MCMs stills an open-point even after 30 years of multidisciplinary research.

2.6 Short Summary of the Chapter

This section has presented the thermal deviations and the reliability impacts on MCM-based systems. Circuit and parametric deviations have been reported as root-cause of current unbalance in parallel devices, which ultimately contribute to the thermal deviation. A finite elements model of a 24-dies MCM has shown a thermal deviation of around $17\,°C$. Moreover, the influences of temperature in aging and catastrophic failure events is presented, justifying the reasons why the temperature is responsible for most failures in industry. The proposed approaches to solve the related issues, point out that the problem stills open for alternative solutions.

Chapter 3

Die-Level Design for Reliability of MCM-based Converters

Contents

3.1 Introduction 35
3.2 Design for Reliability of Power Semiconductor Devices 36
3.2.1 Mission Profile 36
3.2.2 Converter Analysis 37
3.2.3 Thermal Analysis 38
3.2.4 Lifetime Analysis 40
3.2.5 Statistical Analysis for Reliability Prediction 42
3.2.6 System-Level Reliability Analysis 43
3.3 Die-Level Design for Reliability 44
3.4 Design for Reliability of Mission Critical Industry Applications - A case study 46
3.4.1 Mission Profile 47
3.4.2 Converter Analysis 49
3.4.3 Thermal Analysis 50
3.4.4 Lifetime, Statistical and Reliability Analysis 50
3.5 Short Summary of the Chapter 53

3.1 Introduction

To reduce the temperature impacts during the design stage of power converters, reliability-oriented solutions have been applied for many years in industry and traction applications. Therefore, power converters have been designed to respect specific thermal cycling limits to avoid wear out failures during their power modules lifetime [70, 71, 72, 73]. The design for reliability (DFR) is based on the same concept, whereby physics of failure (PoF) analysis are conducted to define the thermal cycling limits [74]. Considering power electronics devices, this approach calculates the number of cycles to failure - which can be traduced to lifetime - based on mathematics models, obtained from accelerated lifetime tests [75, 76]. The mathematical models, however, depends on the devices parameters which can vary within a large group of dies. Therefore, statistical tools has been adopted to take into account the variations and calculate the failure probabilities inside a specific confidence interval [77]. Furthermore, the failure probability - or unreliability - of each device are combined towards the system-level reliability evaluation [78, 79].

In the DFR of MCM-based power converters, however, the thermal deviations and the high number of dies are not considered in conventional procedures. Thereby, the power module lifetime is calculated based on a lower temperature and reduced failure probabilities, thereby resulting in higher system-level reliability. Therefore, a die-level analysis is proposed to improve the DFR procedure of MCM-based systems and . For that, the temperature of each die is obtained separately via finite elements analysis and the die-level failure probabilities are combined to obtain a more realistic system-level reliability. To evaluate the impacts of a die-level analysis on the DFR of MCM-based power converters, a case study based on a real mine hoist system is carried out.

3.2 Design for Reliability of Power Semiconductor Devices

Based on Physics-of-Failure, the DFR has been introduced in power electronics aiming at understanding and fixing reliability problems during the design stage to ensure a system to achieve a predefined target lifetime - or reliability level - within a given environment [5, 6, 34, 36, 74, 77, 78]. The main characteristic of the DFR is the application focus, whereby the lifetime depends on each case, which according to the European industry varies mostly between 10 and 30 years [20]. This procedure is, in general, based in seven steps, as shown in Fig. 3.1 and described in the following subsections.

3.2.1 Mission Profile

The first step is the obtaining of the mission profile for the considered application, which fidelity is of utmost importance and must be as close as possible to the real operational conditions, otherwise it can compromises the analysis [80].

Mission profile in railway applications has been extensively studied by the LESIT (1994-1996) and RASPSDRA (1996-1998) programs, leading to a definition of power cycling and life cycle prediction methods. For trains with a known load cycle, a possible approximation is to consider the total charge cycle on a given service line, assuming maximum load conditions, and then repeat the short term period for long period profiles [72].

In applications with more complex mission profiles with random variations, such as wind and solar energy systems , however, this approximation can generate a significant deviation from the reality [81]. The correct characterization of the mission profile in wind energy systems is indeed a very hard task. Firstly due to the different factors that directly influence the thermal cycling of the devices, such as wind speed, variations in the environment, behavior of the mechanical and electrical parts of the system and

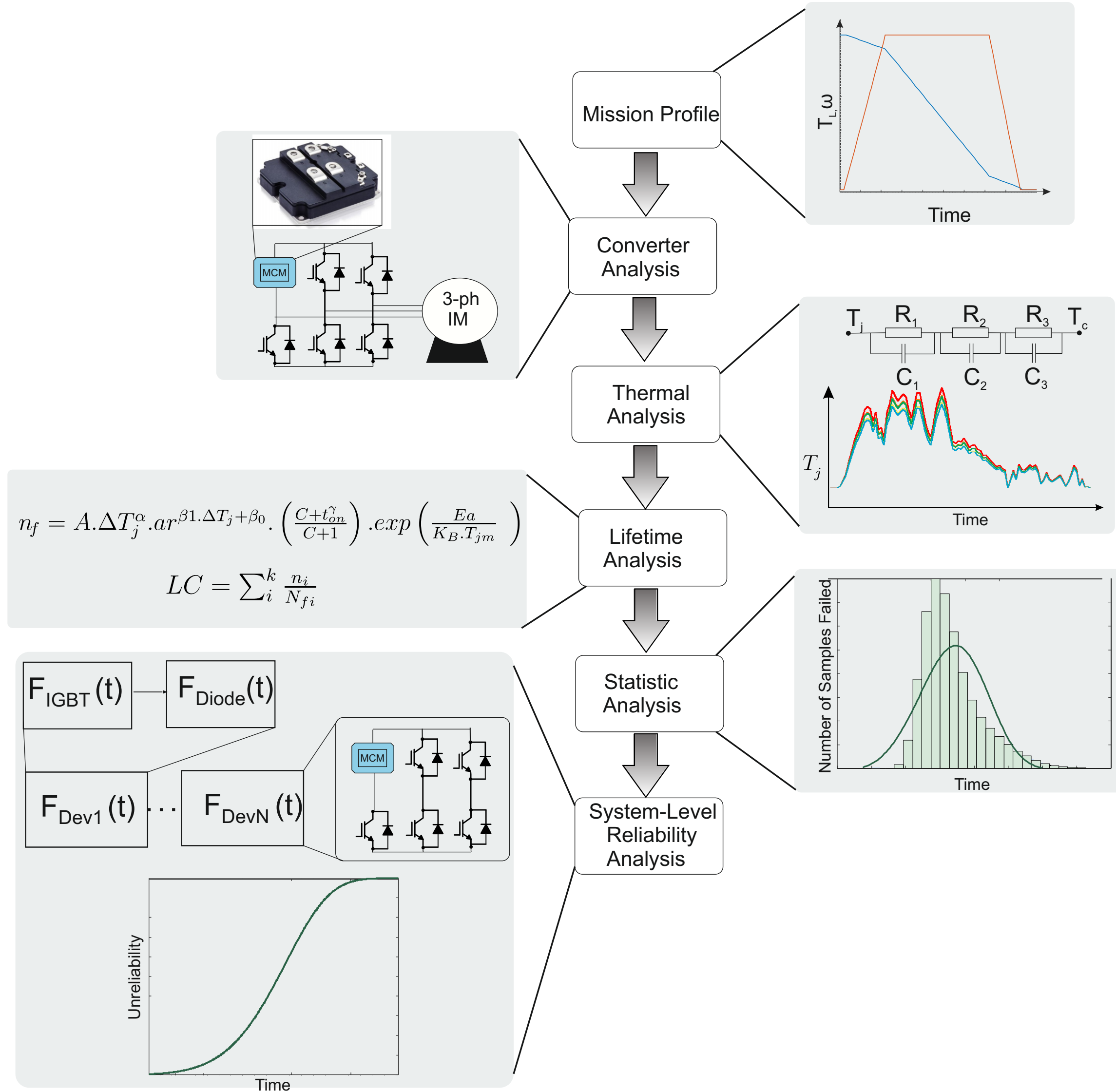


Figure 3.1: Design for reliability of power semiconductor devices of a converter applied to mission critical applications.

grid conditions. These conditions may involve multidisciplinary models with different time constants; therefore, further scrutiny in the mission profile is required. Therefore, alternative approaches based on separating the mission profile time constants in: long period, average period and short period have been proposed [81].

3.2.2 Converter Analysis

Knowing the mission profile, the power converter can be modeled in an electrothermal software to obtain the power, dc-link voltage and currents. Thereafter the devices

can be selected respecting the primary design criteria: voltage blocking and conduction current. This first design serve as a basis, yet this procedure has to be repeated until the system achieve the predefined reliability level [35].

Power Losses Modeling

After modeling the power converter in the electothermal software, the next step is to obtain the power losses of the semiconductor devices, which are extracted from the datasheet. The modeling of the switching losses is based on a four-dimensional matrix, with the respective inputs: blocking voltage, current, and junction temperature. As demonstrated in Fig 3.2, each factor is directly proportional to the losses, in other words, higher voltage, current and temperature results in higher losses.

Similarly, the same procedure is adopted to model the conduction losses of the power modules, which is in turn represented by a two-dimensional matrix, with the respective input data: junction temperature and conduction current. As shown in Figs. 3.3, the output data for the IGBT and diodes are the collector-emitter voltage (V_{ce}) and forward voltage (V_f), respectively. Then, the obtained lookup-tables are loaded in the electrothermal software, for the losses calculation of each device, under the respective mission profile.

3.2.3 Thermal Analysis

For the thermal analysis, the power modules are modeled as equivalent circuits, as demonstrated in Sec. 2.3.1. Then, the model is fed with the power losses profile and the junction temperatures are obtained. After obtaining the temperatures of the power devices, the next step is to characterize the cycle profile. Commonly, rainflow cycling count algorithms are used to detect peaks and valleys to calculate the mean temperature (T_m), variation (ΔT_j) and duty time (T_{on}) [82, 83].

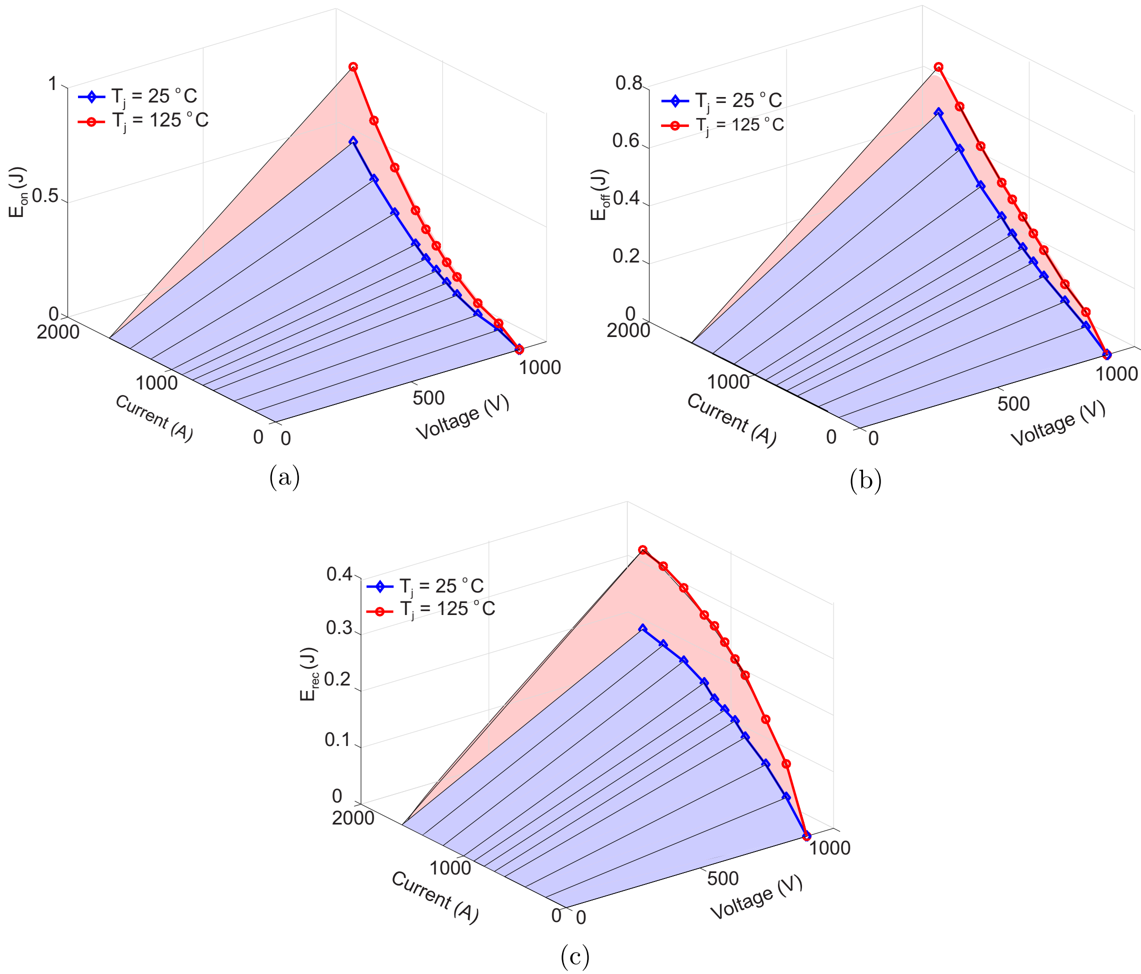


Figure 3.2: Switching losses extracted from the datasheet of a power semiconductor device: (a) IGBT Turn-on (b) IGBT Turn-off (c) Diode reverse-recovery .

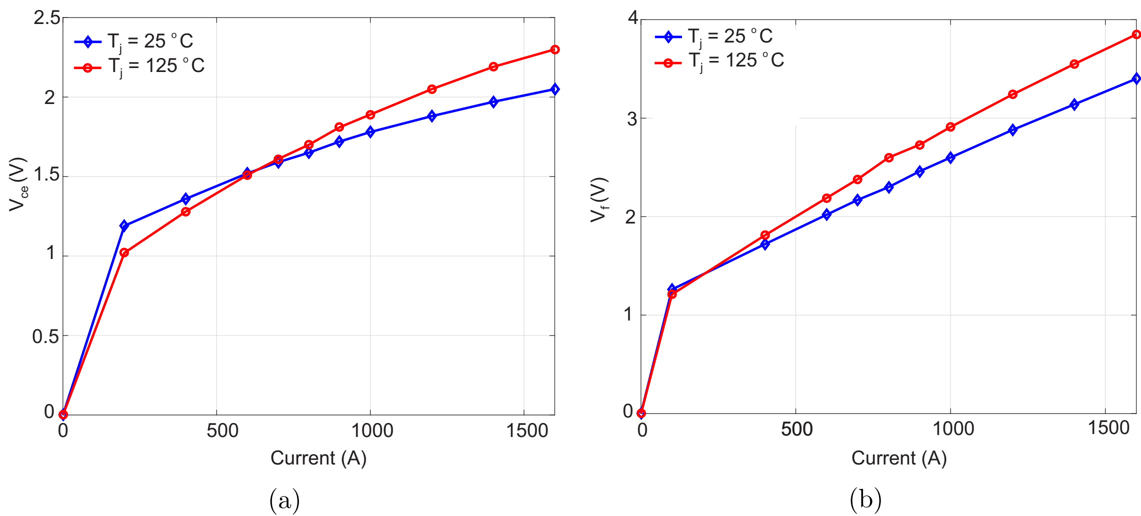


Figure 3.3: Conduction losses extracted from the datasheet of a power semiconductor device: (a) IGBT (b) Diode.

3.2.4 Lifetime Analysis

Thereafter, lifetime models of power devices are used to obtain an expected number of cycles to failure (N_f) based on the specific thermal cycling mission profile. To obtain such models, in short, a power profile with heavy load variation is applied to a group of device until they reach of the previous established end of life (EOL) criteria [84]. Then, the obtained samples are fitted in mathematical models, whose parameters vary with the characteristics of each device, as demonstrated in the following examples.

Coffin-Manson-Arrhenius Model

This model is based on the Coffin-Manson simple model and takes into account the mean temperature (T_m) and the fluctuation T_j, as shown in equation 3.1.

$$N_f = \alpha.(\Delta T_j)^{-n}.e^{(E_a/k.T_m)} \tag{3.1}$$

where k is the Boltzmann constant and E_a is the energy activation parameter.

Bayerers Model

Reference [85] proposed the most analytically comprehensible model, which considers the power module features and variation in different thermal cycling parameters.

$$N_f = A.(\Delta T_j)^{\beta_1}.e^{\beta_2/(T_{j,min}+273K)}.t_{on}^{\beta_3}.I^{\beta_4}.V^{\beta_5}.D^{\beta_6} \tag{3.2}$$

where ΔT_j is the temperature variation, $T_{j,min}$ the minimum junction temperature, t_{on} the duty time, V the blocking voltage, D the bond-wire diameter, I the current per wire, A, β_1, β_2, β_3, β_4, β_5 e β_6 are the adjustable parameters, exhibited in table 3.1.

Wire-bond lifetime model

The limitation of lifetime models is introduced in reference [86], claiming the difficulty to dissociate the impacts of wire bond deterioration and solder fatigue. As a solution, a wire bond based lifetime model is proposed. For that, pressure modules without baseplate (SKIM63) are selected for 97 power cycling tests, with a wide parameter variation in an interval of 5 years [87]. To compress the impact of design

Table 3.1: Fixed parameters in Bayerer's equation.

Parameter	Unity
A	$9.34e14$
$\beta 1$	4.416
$\beta 2$	1285
$\beta 3$	-0.463
$\beta 4$	-0.761
$\beta 5$	-0.5
$\beta 6$	-0.5
V	1700
D	75μm

parameters, different bond wires are adopted during the tests. The obtained lifetime model is shown in 3.3, and its fixed parameters are stated in Tab. 3.2.

$$n_f = A.\Delta T_j^{\alpha}.ar^{\beta 1.\Delta T_j + \beta_0}.\left(\frac{C + t_{on}^{\gamma}}{C+1}\right).exp\left(\frac{Ea}{K_B.T_{jm}}\right).f_{Diode} \tag{3.3}$$

Table 3.2: Fixed parameters of wire bond lifetime model.

Parameter	Unity	Experimental data range
A	$3.4368e14$	
α	-4.923	$64\text{K} \leq \Delta T_j \leq 113\text{K}$
$\beta 1$	$-9.012e-3$	$0.19 \leq \text{ar} \leq 0.42$
$\beta 0$	1.942	$0.19 \leq \text{ar} \leq 0.42$
C	1.434	$0.07\text{s} \leq t_{on} \leq 63\text{s}$
γ	1.208	$0.07\text{s} \leq t_{on} \leq 63\text{s}$
E_a[eV]	0.06606	$32.5°C \leq \Delta T_j \leq 122°C$
f_{diode}	0.6204	

Accumulated Damage

As shown above, the lifetime models indicate the number of cycles to failure for a device under a specific thermal profile. To obtain the expected end-of-life (EOL) of the devices in years, however, it is firstly necessary to calculate the accumulated damage caused by each thermal cycle [88]. For that, the damage of each cycle is accounted by the Palmgren-Miner rule, thereby obtaining the lifetime consumption shown in 3.4 [89].

$$LC = \sum_{i}^{k} \frac{n_i}{N_{fi}} \tag{3.4}$$

where $n_(i)$ is the number of cycles and N_{fi} the number of cycles to failure. Hence, considering the LC over one year is therefore possible to estimate the remaining useful lifetime and the expected year for the device to achieve its EOL - in other words, its lifetime [88].

3.2.5 Statistical Analysis for Reliability Prediction

Deviations in lifetime model and device parameters may result in different lifetime estimation [77]. The on-state voltage drop of an IGBT (V_{ce}), for example, presents variation even within the same manufacturing batch, which ultimately impact T_{jm} and ΔT_j [44, 71]. Therefore, statistical analysis are adopted to improve the confidence level of lifetime predictions, whereby stochastic parameters are converted into equivalent deterministic values [77]. For that, a normal distribution with a mean value (μ) and standard deviation (σ) is defined to obtain a specific confidence interval. Fig. 3.4, for example, shows a distribution with a confidence interval of 99.73%, i.e. a variation equals $3\,\sigma$.

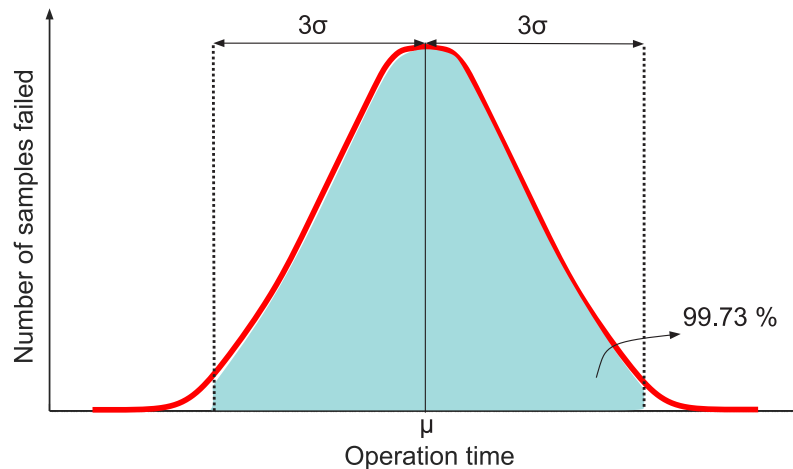


Figure 3.4: Normal distribution with a confidence of 99.73 %.

For the implementation the Monte Carlo analysis have been adopted, whereby the parameter variation obtained from normal distributions is applied to a specific

number of samples. Thereby, the EOL of each sample, which has specific parameters defined by the normal distribution, is calculated as detailed in Sec. 3.2.4. Although the number of samples is not limited, the selection of 10000 has been adopted in such analysis, due to its capability to ensure a good confidence level and low computational effort [77, 90]. After calculating the lifetime for each sample, the obtained distribution - which represents the number of samples on its expected end-of-life year - is fitted within the Weibull probability density function (PDF) f(x), by using 3.5 [90].

$$f(x) = \frac{\beta}{\eta^{\beta}} \cdot x^{(\beta-1)} \cdot exp\left[-\left(\frac{x}{\eta}\right)^{\beta}\right] \tag{3.5}$$

where β, η and x are the shape, scale and operating time parameters, respectively.

Finally, the cumulative density function (CDF) is calculated by integrating the PDF, as shown in 3.6. As a result, the probability of one sample to failure over time is defined by the CDF curve - F(x) [78]. From that, the statistical-based B_x lifetime, which is the probability of $x\%$ samples to fail in a specific time can be obtained, and used as a reliability metric for the design of systems. Alternatively, the failure probability - or unreliability - in a specific time, can be represented by the U_x factor introduced in [35]. Fig. 3.5, shows the unreliability curve - or CDF - highlighting the B_x and U_x factors, which are the time for a specific failure probability and the failure probability for a defined operation time, respectively.

$$F(x) = \int_0^x f(x)dx \tag{3.6}$$

3.2.6 System-Level Reliability Analysis

Once the unreliability curve of each component is obtained, the next step is to combine them to obtain the reliability of the entire system, via system-level block diagram approach. The reliability modeling is based on the system interruption; therefore, the blocks, which represent the unreliability of a each component, are connected accord-

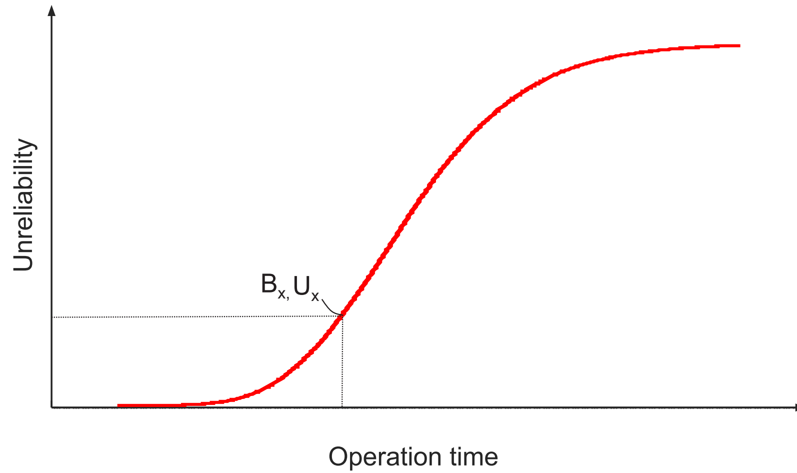


Figure 3.5: Unreliability curve with: B_x - time when the device achieve $x\%$ of failure probability; U_x - The failure probability in a specific operation time.

ing to the consequence of its failure [78]. For example, if a failure of one single device means a system interruption, the unreliability - or reliabilities - are combined in a series association, as shown in Fig. 3.6 [78].

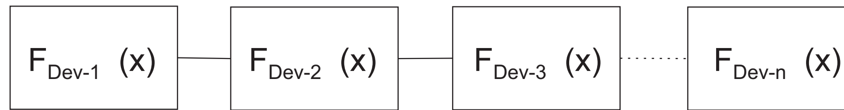


Figure 3.6: The reliability series association, which is adopted when a failure of a single device results in a system interruption.

Therefore, the system-level reliability, or the probability of an interruption in such systems due to a single failure, is the product of the failure probability of each series-connected component ($F_{Comp-i}(x)$), as modeled in 3.7 [78]:

$$F_{System}(x) = 1 - \prod_{i=1}^{n}(1 - F_{Comp-i}(x)). \tag{3.7}$$

3.3 Die-Level Design for Reliability

The failure-in-time (FIT) is a statistical value that represents a failure rate based on the number of failures that occurs every 10^9 hours [91]. For the reliability modeling considering failure-in-time (FIT), the failure probabilities are calculated for a specific power module and scaled to others with similar chips - same blocking voltage -, yet

with different current level [91]. In other words, the result is obtained for a specific number of dies, and modeled as a reliability series-connected system, to calculate the failure rate of MCMs with different number of dies. Although the design for reliability has been applied for proper selection of power devices in very complex systems, the specificity of multichip modules have not been considered. As demonstrated in Sec. 2.3.2, the critical thermal mismatches results in considerable extra temperature in specific dies which is not estimated in ordinary designs. Moreover, to obtain the system reliability of modular or multiphase systems the failure probability of each device is combined in a product, as shown in Sec. 3.2.6. Nevertheless, the multiple devices inside the MCM prone to fail is neglected and its failure probability is calculated as a single die solution.

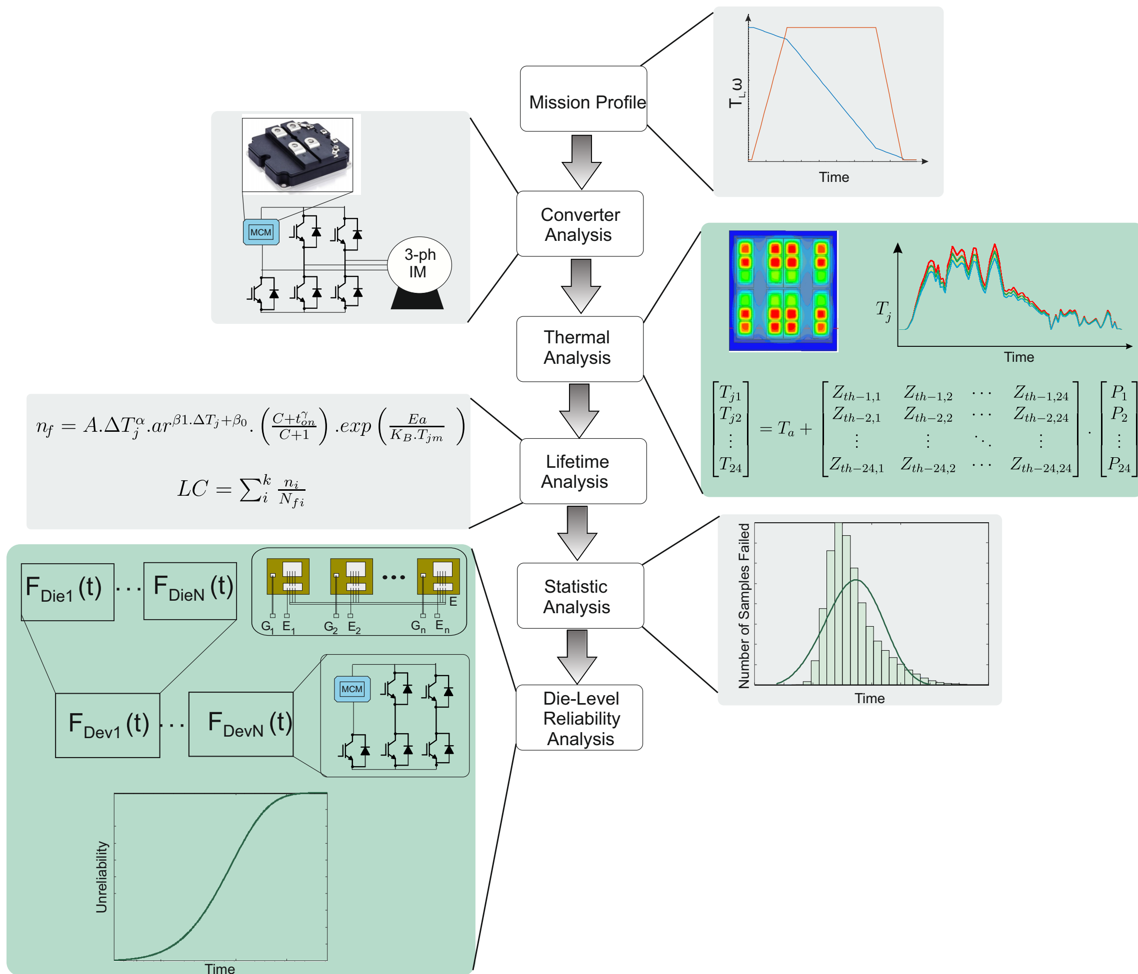
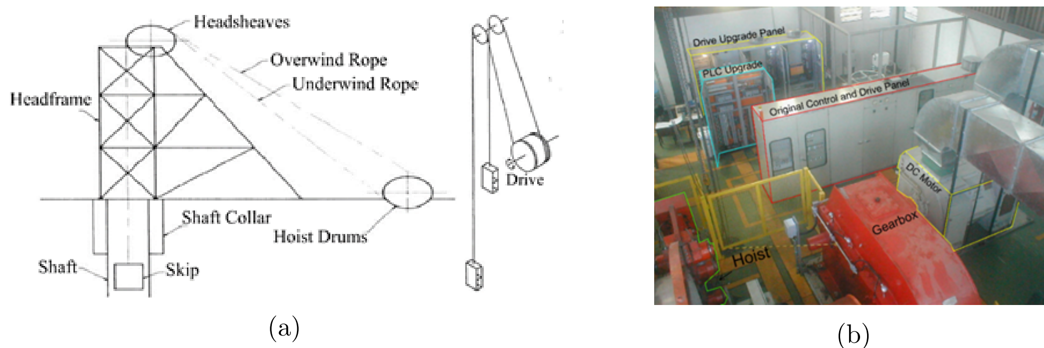


Figure 3.7: Die-Level design for reliability flowchart, including - light green - the thermal deviation and the system-level reliability modeling of the MCM dies.

Therefore, this work proposes a die-level reliability design for MCM-based mission critical application power converters. This structure has two basic differences, the thermal modeling via superposition methodology to obtain the matrix with cross-coupling impedance - as described in Sec. 2.3.2 -, and the reliability modeling of the MCM as a system composed by multiple dies with different failure probabilities, as highlighted - light green - in Fig. 3.7. To evaluate the impact of the thermal deviation and a die-level failure probability analysis on the reliability of mission critical applications, a case study based on an aforementioned mine hoist system is presented in sequence.

3.4 Design for Reliability of Mission Critical Industry Applications - A case study

The conducted case study is based on a real gold ore mine hoist system located in southeastern Brazil, which operates with a maximum speed of 12 m/s and a payload of 4.2 tons. This system, which dates back to the late eighties, is currently driven by a 1 MW/900 V dc motor fed by a fully controlled thyristor rectifier, as shown its electrical layout of Fig. 3.8. However, for this study a retrofit is realized, whereby the new system is composed by induction machine fed by a two-level inverter. This new system is driven by an 1 MW / 690 V induction machine, with a current of 1070 A



(a) (b)

Figure 3.8: Mine hoist system (a) General diagram (b) Photo of the electrical system of the mine hoist..

[4]

at full load (I_L) and 560 A at no load (I_{NL}) whilst the locked rotor current (I_i/I_n) achieves up to 6520 A and the breakdown torque (T_{bd}) is 200 %. This machine has a frequency of 50 Hz and six poles, thereby achieving a speed of 990 rpm at full load, with a total slip of 1%. For that, an indirect field oriented control (IFOC) strategy is realized, whereby the machine starts in a controlled velocity ramp. The induction machine parameters, equivalent magnetic circuit estimation and validation, as well as the control tuning information are included in Appendix. B.

3.4.1 Mission Profile

The real field measured mission profile of the mine hoist including the driven dc current, speed (commanded and measured) and skip position is shown in Fig. 3.9. The mission profile initiates with the reference skip stopped at the top of the tower, and it is accelerated to the deep during 40 s, thereby achieving the maximum velocity of 12 m/s. When the skip achieves nominal speed, it remains constant for about 50 s. Thereafter, the skip starts breaking (regenerative breaking), which is represented by the armature negative current. Finally, before the skips come to a complete stop, there is a low constant speed region. The mission profile finishes with the reference skip at the bottom of the mine, with a total time of 120 s. In the respective production plant, it is expected around 11800 similar trips during a year of operation.

As can be seen, the skip is accelerated via small speed steps, and the current achieves up to 2560 A, i.e. around 150% of overload. To reduce the thermal cycling stress, the skip is accelerated in a constant ramp, as shown in 3.11. The static load torque, in turn, results from the force exerted by the skip load, and varies with its position from bottom as shown in 3.8

$$F_{skip} = g \cdot (D_{wd} - 2 \cdot D_{Bt}) \cdot R_w + P_L \tag{3.8}$$

where, g is the gravity, D_{wd} the winding distance, R_w the rope weight, P_L the payload and DB_t the skip distance from bottom. Hence, the static torque on drum

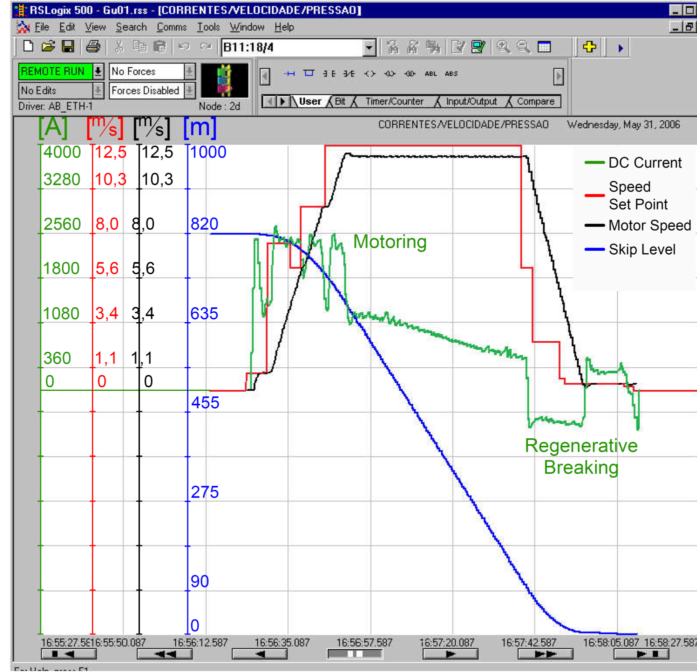


Figure 3.9: Electrical measurements of the mine hoist during one trip, measured in the real field environment.

(T_{DS}) is obtained by:

$$T_{DS} = F_{skip} \cdot \frac{D_{ia}D}{2} \cdot (1 + F_C) \tag{3.9}$$

where, DiaD is the drum diameter and FC the friction torque. The torque on motor is then obtained by converting it with the gearbox ratio (G_R) and efficiency (G_{EF}), as shown in 3.10.

$$T_{MS} = \frac{T_{SD}}{G_R \cdot G_{EF}} \tag{3.10}$$

Therefore, with the mission profile based on the trip from the top to the bottom of the mine, the measured torque profile starts from its maximum and vary with negative coefficient, as shown in 3.11. For the respective system, the load torque in worst case - i.e. with the skip at the top of the mine, 860 m - is $T_{MS-1pu} = 10015\,Nm$. The total inertia on the motor side, accounting the mechanical parts of the system is also calculated in the real mine hoist project, totaling $J_{MS} = 650\,kgm^2$. The mechanical parameters of this project are confidential, and not relevant for the conducted case

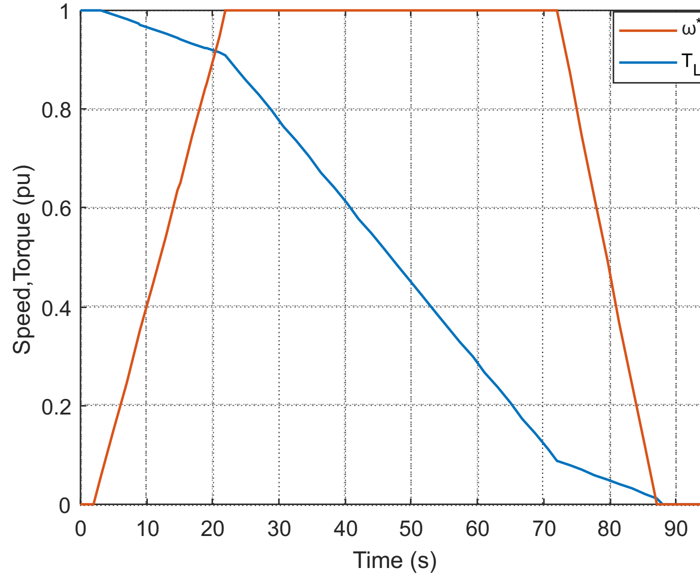


Figure 3.10: Mission profile of the mine hoist system driven by an induction machine with FOC.

study which requires only the mentioned T_{MS} and J_{MS}.

3.4.2 Converter Analysis

To select the proper devices for the designed system, the mechanical load parameters and the mission profile are applied in the simulation software, which contains an induction machine fed by a two-level inverter, and the parameters shown in Tab. 3.3. Therefore, knowing the dc-link voltage $V_{dc} = 1150\,V$, only the current is necessary for the first selection of the devices. Fig. 3.11 , shows the output current of the converter which achieve up to $I_{dc} = 2200A$, and operates with reverse power flow during breaking process. Therefore, to ensure a reasonable temperature without compromising the lifetime [5, 6], two 24-dies MCM devices are adopted in parallel, totaling twelve MCMs.

Table 3.3: Simulation parameters.

Parameter	Value
V_{dc}	$1150\,V$
V_{out}	$690\,V$
F_{sw}	$5\,kHz$

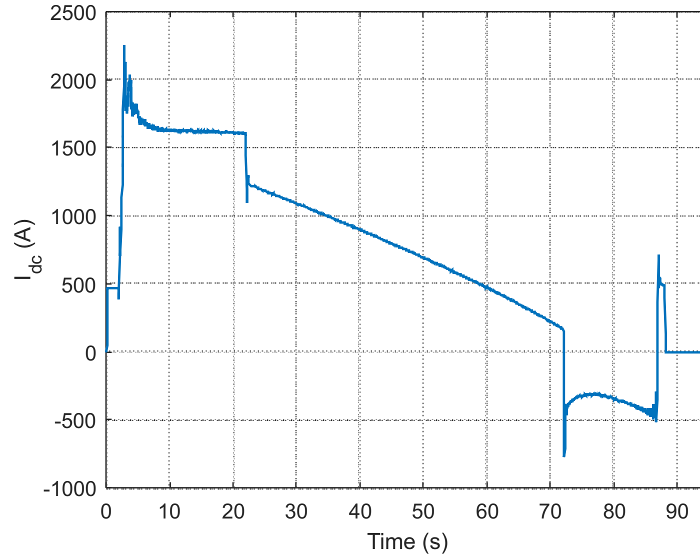


Figure 3.11: Dc-Link current profile of the designed converter feeding the induction machine which drive the mine hoist system.

3.4.3 Thermal Analysis

For the thermal analysis, two thermal circuits are adopted, one based on a ordinary foster thermal network and the other obtained through the FEM analysis. Therefore, in the first analysis shown in Fig. 3.12(a), the MCM has only one temperature for the IGBTs and other for the diodes. For the second analysis, however, there are 24 temperatures - one for each die inside the MCM - including the self and thermal cross-coupling effects, thereby resulting in a maximum junction temperature $7.64\,°C$ higher.

3.4.4 Lifetime, Statistical and Reliability Analysis

With the temperature profiles, the expected lifetime of both approaches are calculatde through the model described in Sec. 3.2.4 [86]. To represent the uncertainties, a Monte-Carlo analysis with a population of 10000 samples, considering variations in V_{ce} obtained from die-level measurements, is realized [92]. Fig. 3.13, shows the failure distribution over time for the two-level inverter feeding the mine hoist induction machine, for the T_j profiles obtained by a single foster network (purple) and the equivalent thermal network with cross-coupling thermal impedance (black). As can

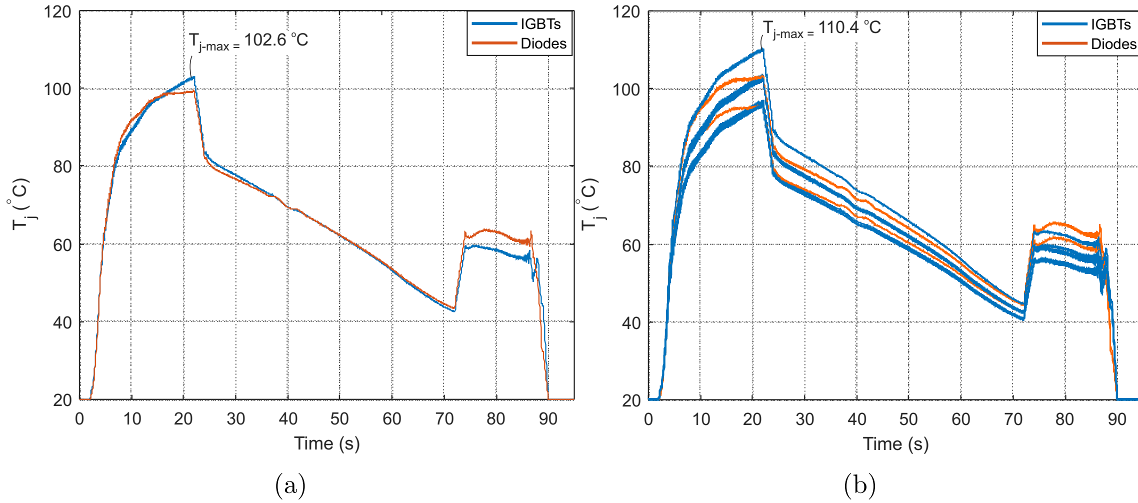


Figure 3.12: Junction temperature profile of one MCM in the 2-level inverter with (a) Foster thermal network (b) Matrix with cross-coupling impedance extracted from finite elements analysis.

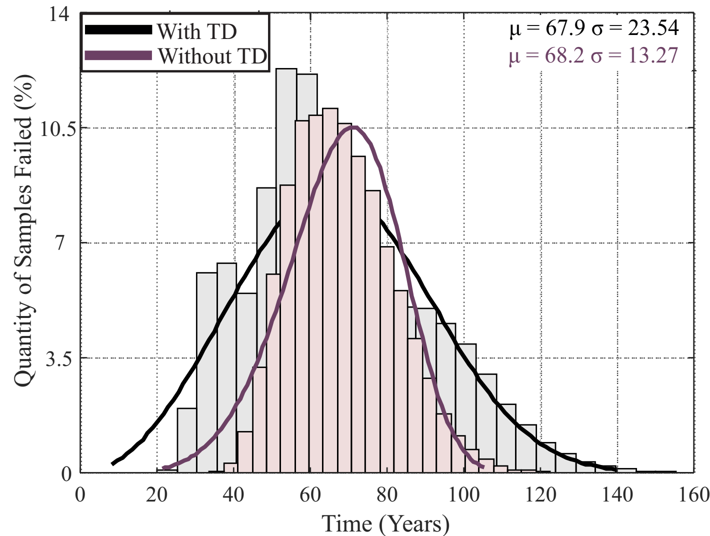


Figure 3.13: Monte-Carlo analysis to account the failure distribution over time, considering parametric deviations in V_{ce}, without thermal deviation (purple) - foster thermal network - and with thermal deviation (black) - FEM-based thermal network with cross-coupling.

be seen, considering the thermal distribution inside the MCM and a die-level lifetime calculation - as proposed in the die-level design for reliability (DL-DFR) procedure - the number of failed samples are more scattered over time, thereby resulting in some samples failed in the first years of operation.

Thereafter, the failure probabilities over time are obtained through cumulative density functions (CDF) of the distributions shown in Fig. 3.13. For the first case, the system-level design for reliability approach is used, whereby the failure probability

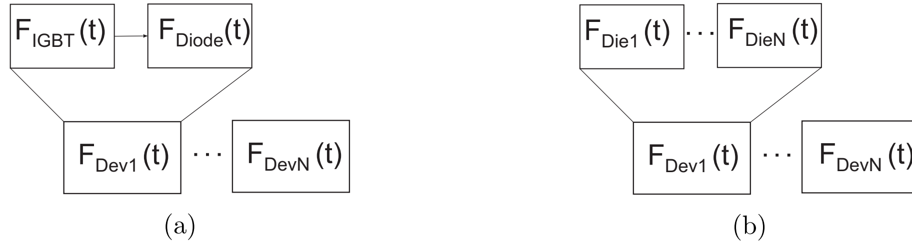


Figure 3.14: Series-connected reliability modeling, whereby the failure of a single component means system interruption, for the procedures: (a) System-Level Design for Reliability (b) Die-Level Design for Reliability.

per module - one IGBT and one Diode -, are combined in a series-reliability block, as shown in Fig. 3.14 (a) and described in 3.2.6. Conversely, for the second analysis the CDF of each die is obtained as proposed in the DL-DFR approach. Therefore, the failure probability of each die is combined in a series-reliability block, and the system-level reliability is calculated, as shown in Fig. 3.14 (b).

Fig. 3.15, shows the unreliability analysis for the mine hoist power converter, with a system-level and die-level reliability modeling. As can be seen in blue, the obtained B_{10} lifetime, i.e. the time when 10 % of the samples fail, is B_{10} = 28.8 years. Nevertheless, considering the thermal deviations inside the MCMs, and a die-level reliability modeling, the resulting lifetime is B_{10} = 14.36 years, as shown in green line of Fig. 3.15.

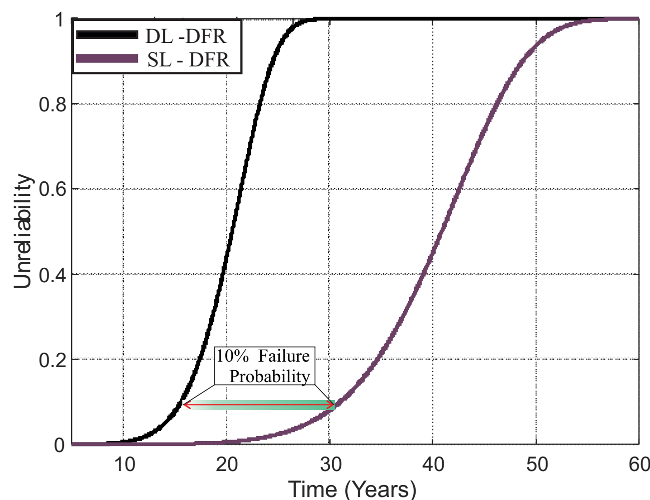


Figure 3.15: Unreliability analysis of the multichip modules composing the mine hoist power converter, for system-level reliability (purple) and die-level reliability (black) approaches. A B_{10} lifetime difference of 100 % is observed.

3.5 Short Summary of the Chapter

A power routing strategy to overcome thermal deviation among modules of a multiphase drive is proposed. It is demonstrated that the proposed strategy, can overcome thermal deviations of $10\,°C$ and enhance the power converter lifetime in up to $23\,\%$, without degrading the electromagnetic machine performance.

The design for reliability has been presented as a solution to mitigate thermal stress, whereby the power converter is designed to obtain a predefined lifetime considering the mission profile of a specific application. Although the DFR has been increasing the reliability of systems, the system-level reliability approaches may result in wrong lifetime prediction. Therefore, this chapter has presented an alternative DFR approach, whereby a FEM-based thermal model and a die-level reliability modeling are adopted. As a result, the procedure is capable of accounting the failure probability of each die for a specific temperature, thereby predicting the system-level lifetime which can diverge in up to $100\,\%$ of the traditional procedure. Moreover, the results point out that the unequal thermal distribution inside the MCM, results in reduced system lifetime.

Chapter 4

Thermal Balancing in Power Converters

Contents

4.1 Introduction 56
4.2 Thermal Control in Power Electronics Devices 56
4.2.1 Finite Control Set Model Predictive Control 57
4.2.2 Adaptive Dc-Link Voltage Control 59
4.2.3 Power Routing 59
4.3 Power Routing in Multiphase Drives 60
4.3.1 Soft-Unbalance Operation of Multiphase Machines 61
4.3.2 Power Routing in Multiphase Drives 64
4.3.3 Thermal Validation 65
4.3.4 Reliability Analysis of the Power Routing in MCIAs 68
4.4 Thermal and Aging Monitoring of Power Semiconductor Devices 70
4.4.1 Sensor-based Temperature Monitoring 70
4.4.2 Gate Voltage Monitoring 71
4.4.3 Gate Resistance Monitoring 73
4.4.4 Transient Monitoring 74
4.4.5 Device Current Monitoring 76
4.4.6 On-State Voltage Monitoring 77
4.4.7 Comparison of Thermal and Aging Monitoring Strategies 87
4.5 Validation of a V_{on}-based Thermal Balancing Strategy 89
4.5.1 V_{on}-based T_j Sensing 90
4.5.2 V_{on}-based Thermal Balancing 91
4.6 Short Summary of the Chapter 93

4.1 Introduction

The thermal control has been proposed to mitigate thermal stress during the power converter operating stage by influencing the losses of the semiconductors, and ultimately reduce the thermal stress on the devices [30, 93, 94, 95, 96]. The power routing, is an alternative solution for modular converters, whereby the power is distributed to balance the temperature and degradation among their building blocks [31, 32, 97, 98, 99]. Although multiphase drives are commonly fed by non-modular converters, its higher number of phases allow a soft-unbalance operation capability without affecting its magnetic performance. Thereby, this chapter presents a power routing strategy for multiphase drives to balance the temperature and even the degradation among its phases.

Even though several thermal balancing strategies have been proposed, its implementation with a practical temperature sensing has been scarcely explored. Indeed, the temperature sensing of power semiconductor devices stills an open research topic due to multiple factors, such as high resolution and isolation requirements. Thereby, in this chapter a V_{on}-based sensing circuit is furthermore implemented and its capability to feedback thermal balancing strategies, is experimentally validated.

4.2 Thermal Control in Power Electronics Devices

Fig. 4.1, shows a summary of the adopted temperature-related control variables for thermal control and stress mitigation of power semiconductor devices. A simple approach is the switching frequency adjustment to direct influence the losses, which can be realized without noticeable effects on the operating point if adjusted within system constraints [30]. The current limiting under heavy load conditions has been also proposed to reduce the thermal stress of electrical vehicle (EVs) converters operating under variable load cycling [100]. Another possibility is to act on the gate driver to control the semiconductor losses, either varying the gate voltage or manipulating

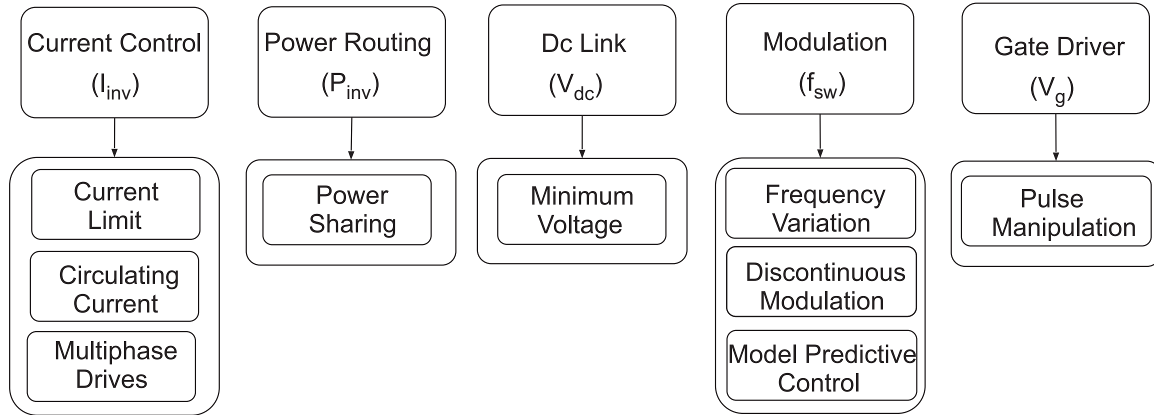


Figure 4.1: Temperature related control variables and strategies for thermal control and power routing, in power electronics devices.

the gate resistance [101, 102]. The first one, for example, has shown good performance on reducing temperature without affecting the power device mission profile. Alternative modulation strategies have been also applied for thermal balancing in modular converters [93, 94, 95, 96]. Moreover, finite control set model predictive control, dc-link voltage control strategies and power routing are also adopted, as reviewed in the following.

4.2.1 Finite Control Set Model Predictive Control

Active thermal control can also benefit from the non-linear control structure of model predictive control applying a particular space vector directly to the inverter without modulator. In [103] a finite control set MPC (FCS-MPC) algorithm is proposed to minimize the fatigue of the devices by reducing the thermal stress in electrical drive applications. In this proposal, the load current and the junction temperature for all possible vectors of the next sampling instant are predicted and used to derive the FCS-MPC cost function parameters. These cost functions include the error from the current reference, the temperature difference among the dies and the total power losses. Thereafter, the factors are weighted and the vector with lowest cost function is directly applied to the power converter. As a result, the temperature of the dies inside a six-pack power module can be better balanced. The FCS-MPC is also proposed to

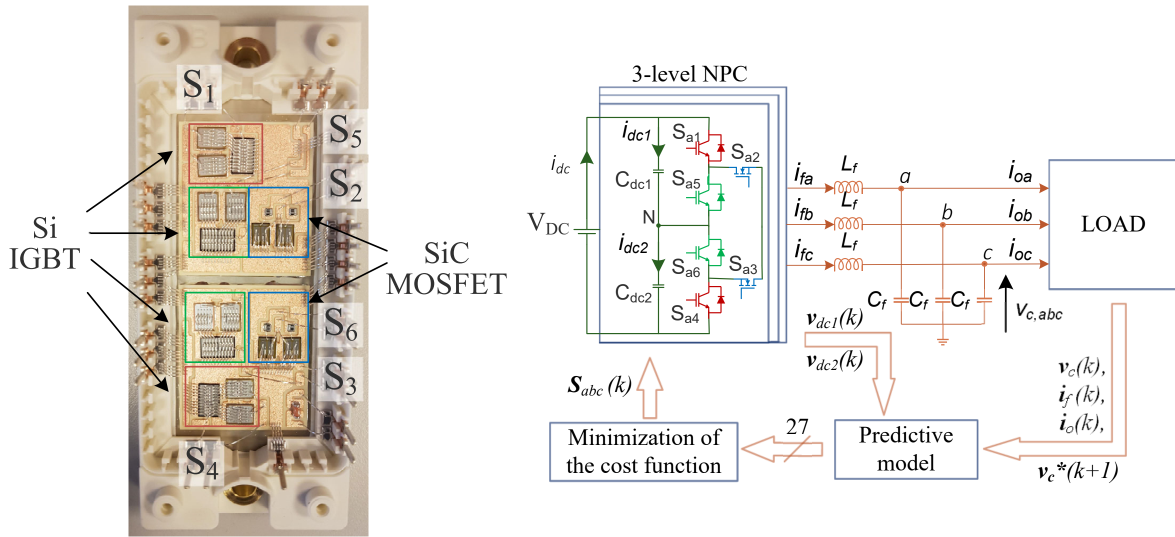


Figure 4.2: Module and system layout : (a) One phase ANPC open module. (b) Simplified system model scheme of ANPC converter using model predictive control.
[105]

better distribute the thermal stress among the devices of a three level NPC converter [31, 32, 104]. In this method, the vector which devices would switch higher currents are avoided, and the temperature between inner and outer devices are balanced.

The Active NPC is an alternative solution to even the thermal stress among the phase devices, by acting on the active clamping ones [106]. The Hybrid ANPC (H-ANPC) converter has been recently proposed to increase its efficiency with a reduced additional cost. As shown in Fig. 4.2 (a), the inner switches are exchanged by SiC MOSFET devices [107]. Therefore, modified modulation strategies can be adopted making the inner devices to operate under fast switching, whereas the outer devices switch at line frequency. As a result, the converter efficiency is optimized due to the lower switching losses of inner SiC Mosfets [108]. Nevertheless, this alternative modulation is not focused on thermal balancing potentially resulting in thermal deviation even in an ANPC structure. Hence, a FCS-MPC for optimized operation of a H-ANPC converter to improve thermal balancing whilst keeps the thermal and the dc-link voltages balanced, is proposed [105]. As shown in Fig. 4.2 (b), the current and

the dc-bus voltages are sensed, and the vector with lowest weighting factor is applied in the respective sampling time.

4.2.2 Adaptive Dc-Link Voltage Control

According to IEC 61727, photovoltaic systems must remain connected with the grid floating between 0.85 and 1.1 pu; therefore, manufacturers design dc-link to meet the requirements in the worst case - 1.1 pu. Conversely, the fixed high dc-link voltage results in high switching losses and, consequently, higher temperatures and reduced reliability. Therefore, an adaptive control to operate the dc-link voltage in the minimum required level to remain connected and inject power to the grid, is proposed [109]. As shown in 4.4, the minimum dc voltage is selected considering the instantaneous grid voltage, and a linear overmodulation strategy is used in case of fast grid transients. As a result, the switching losses are reduced and the inverter lifetime increases in up to 75%, without impacting the MPP tracking and needing additional measurements.

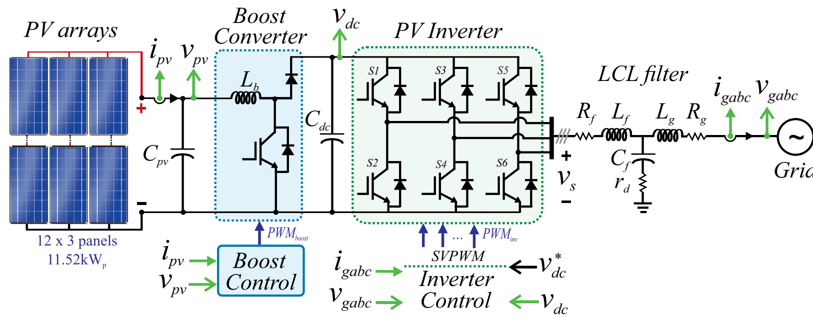


Figure 4.3

Figure 4.4: Adaptive minimum dc-link control to increase PV lifetime [109]

4.2.3 Power Routing

The power routing concept is based on uneven loading of building blocks in modular power converters to control the thermal stress and equalize the useful remaining lifetime (RUL) of the power devices. Fig. 4.5, shows the power routing concept in two parallel inverters [97]. In addition to parallel inverters, the power routing is further-

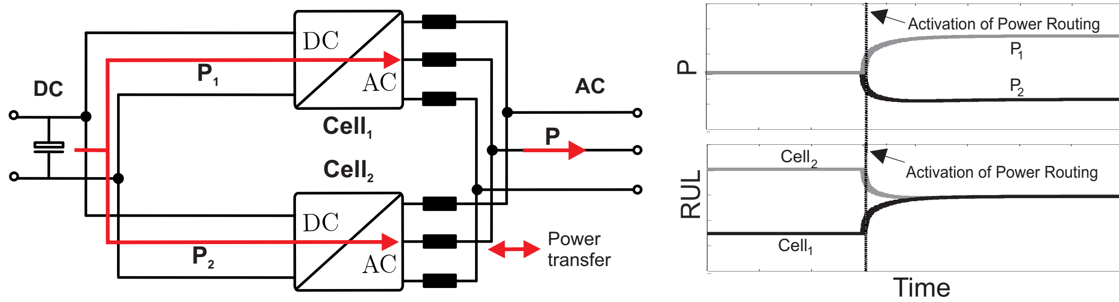


Figure 4.5: Power Routing concept, the power is reduced in the most damaged cell to equalize the remaining useful lifetime.

more proposed for the lifetime control of Cascaded H-Bridge (CHB) [98], Quadruple Active Bridge (QAB) [110], MMC [99] and overall modular systems such as smart transformers (ST) and more electric aircraft (MEA) [31, 32]. Moreover, the power routing has been also proposed to improve the maintenance schedule of modular system, whereby the quantity of maintenance can be reduced whilst the time between aging failures is increased [111].

4.3 Power Routing in Multiphase Drives

As demonstrated in Sec. 2.3.3, deviations among the modules - demonstrated in - can potentially uneven MCMs degradation and reduce even further the reliability of high power converters. Therefore, the power routing has been proposed as a potential solution, whereby the power is directed to lower stressed device to increase the entire system lifetime [31, 32]. Based on this concept, this section presents a power routing strategy which takes advantage of the capability of multiphase drives to operate under soft-unbalanced condition [112]. Due to the higher number of phases, the temperature of the hottest phases can be reduced redistributing the power among the other ones, thereby balancing the temperature without magnetic performance degradation. To validate the capability of the multiphase machine to operate under soft-unbalance condition and balance the temperatures, finite elements analysis are conducted. Furthermore, the impact of such strategy on the reliability of mission critical applications, a case study based on the mine hoist system described in Sec. 3 - with higher power

- is carried out.

4.3.1 Soft-Unbalance Operation of Multiphase Machines

The nine-phase induction machine (9PIM) can be seen as three three-phase systems with the windings are star-connected, yet displaced 40 ° among each other with connected neutrals [113]. Fig. 4.6, shows the construction and currents diagrams of a symmetrical nine-phase induction machine of two poles (9PIM), which has three times the number of phases. Therefore, the 9PIM can produce a circular magnetomotive force (MMF) under severe unbalanced conditions. The 9PIM, for example, can produce circular MMF even after losing one phase, and still operating with only 16 % of extra current in the remaining ones without affecting its magnetic performance [114, 115, 116]. As a result, multiphase machines have been proposed to increase the reliability of mission critical drives, due to its inherent fault tolerance capability [3, 117, 118].

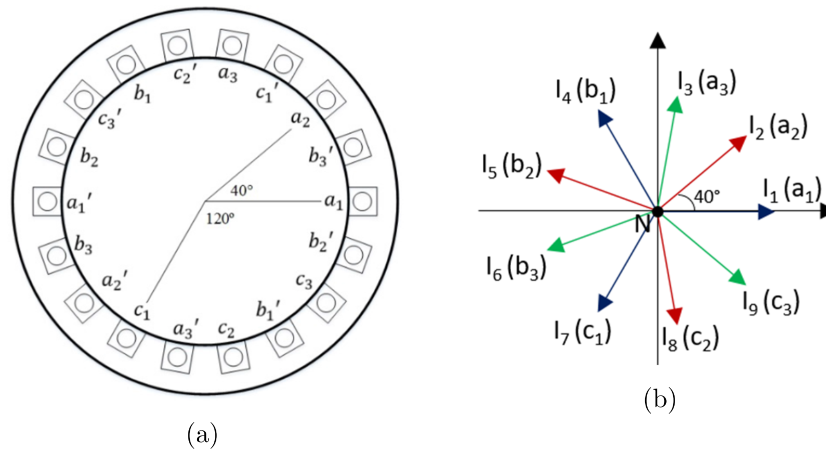


Figure 4.6: (a) Current diagram of the nine-phase machine in balanced condition (b) Basic construction diagram of the 9PIM with two poles.
[115]

The multiphase machine, can furthermore operate under soft-unbalance conditions, whereby the current is slightly reduced in specific phases, and redistributed among the others. To operate under soft-unbalance conditions, however, the currents - magnitude and phases - must be recalculated to keep a circular MMF, as shown in Fig. 4.7. For

that, it is necessary to solve two equations, one for the imaginary and other for the real part of the MMF [115]. To obtain the system of equations and calculate the currents for the soft-unbalance operation, the balanced MMF for the 9PIM has to be defined. According to [115], the MMF generated by nine balanced stator currents is given as in 4.1.

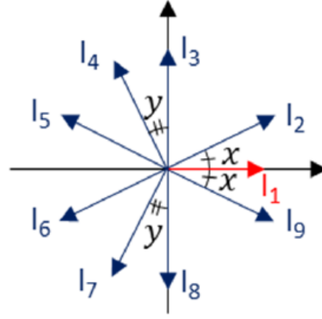


Figure 4.7: Current diagram of the a nine-phase machine in balanced condition, considering a reduction in phase A_1 - current I_1.
[112]

$$MMF_{Balanced} = \left(\frac{9}{2}\right) N\hat{I}e^{j\theta} \tag{4.1}$$

where, $\hat{I}$ is the peak of the phase current and $\theta = \omega t$, is the time varying angle. Thereafter, it is necessary to separate the imaginary to the real parts of the $MMF_{Balanced}$, thereby obtaining 4.2 and 4.3, respectively [115].

$$\frac{9}{2}N\hat{I}sin(\theta) = N[(I_2-I_9)sin(40°)+(I_3-I_8)sin(80°)+(I_4-I_7)sin(60°)+(I_5-I_6)sin(20°)] \tag{4.2}$$

$$\frac{9}{2}N\hat{I}cos(\theta) = N[I_1+(I_2+I_9)cos(40°)+(I_3+I_8)cos(80°)-(I_4+I_7)cos(60°)-(I_5+I_6)cos(20°)] \tag{4.3}$$

Considering a reduction in the current magnitude of phase A, it is necessary to recalculate the current magnitude and phase displacement of the other ones, as shown

in Fig. 4.7. As can be seen in (4.4), the currents from I_2 to I_9 have the same magnitude and some cancel each other [112].

$$\begin{cases} I_2 = -I_6 \\ I_3 = -I_8 \\ I_5 = -I_9 \\ |I_2| = |I_3| = \cdots = |I_9| = I_p\hat{I} \end{cases} \tag{4.4}$$

To avoid neutral current circulation, the sum of the nine currents must be null. Therefore it is required that I_4 and I_7 cancel I_1, and the relation shown in (4.5) has to be respected [112].

$$I_1 = -(I_4 + I_7) \tag{4.5}$$

Thereby, the problem is resumed in three equations - 4.2, 4.3 and 4.5 - with three incognitos: where I_p is the magnitude of the currents - except I_1 -, whilst x and y are the phase shifts related to the reduction of $|I_1|$ - as shown in 4.7 [112]. As shown in Fig. 4.8, a circular magnetomotive force can be obtained in soft-unbalance condition when the currents are recalculated by following the mentioned procedure [112]. As a result, the multiphase machine can operate under soft-unbalanced condition without interfering its magnetic performance, as validated in reference [112].

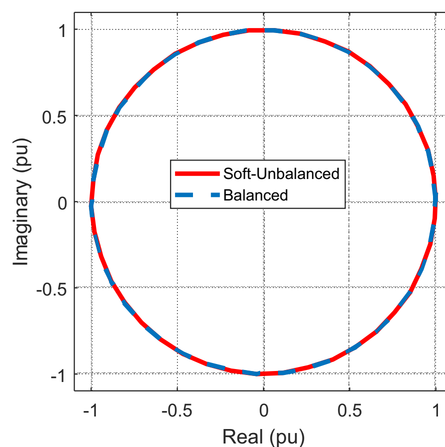


Figure 4.8: Magnetomotive force for the balanced and the re-calculated currents for the soft-unbalanced operation, showing a circular MMF in both conditions. [112]

4.3.2 Power Routing in Multiphase Drives

Although the high number of devices in a nine-phase drive increases the probability of thermal mismatches among its power modules. Therefore, this work proposes a power routing strategy, whereby the phase power of the hotter devices are reduced,to balance the temperature among the MCMs. The power routing procedure with each step is described in the flowchart of Fig. 4.9. As can be seen, at the beginning, balanced currents are applied to the stators of the 9PIM. Thereafter, the temperatures are sensed; if the temperatures are balanced, the machine stills operating under balancing conditions. Conversely, if a thermal deviation is detected, the current of the hottest phase is reduced; the other currents are then re-calculated to keep circular MMF - as described in Sec. 4.3.1 - and the obtained unbalanced currents are applied to the phases. This process works iteratively, until the thermal balancing is achieved [112].

To implement the power routing in a nine-phase machine the control schematic

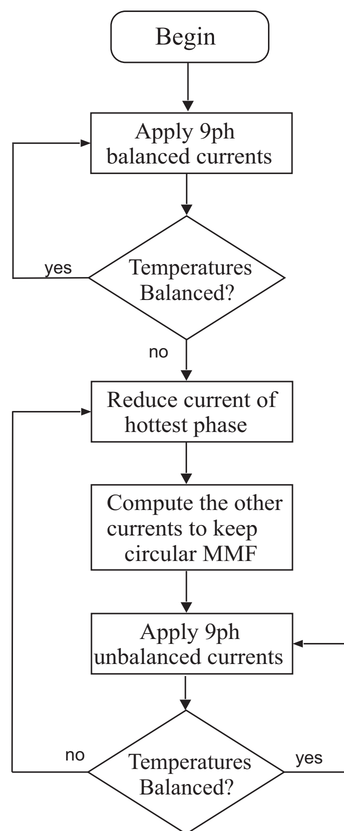


Figure 4.9: Flowchart of the power routing for thermal balancing in nine-phase induction machines.

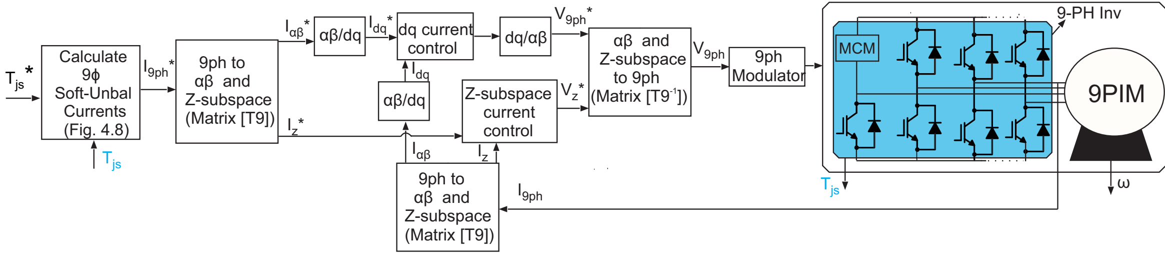


Figure 4.10: Power routing diagram of a nine-phase machine, whereby the soft-unbalance currents are calculated to balance the temperatures; and it is imposed via a Z-subspace current control. The speed IFOC control is implemented in dq synchronous in the same way of an ordinary three phase induction machine. The T9 matrix generates the voltage references for the 9PH modulator.

shown in Fig. 4.10 is used. The speed control of the 9PIM is realized in the dq synchronous frame in the same way of an ordinary three-phase induction machine - as demonstrated in Sec. B.1. However, a T9 matrix is required to transform the nine-phase currents to $\alpha\beta$ and the Z-subspace currents [119]. To realize the power routing, the current references are calculated to obtain thermal balance whilst keep circular magnetomotive force. Thereafter, the Z-subspace and the speed control - in $\alpha\beta$ - outputs are applied to the inverse T9 matrix, which in turn calculate the nine-phase voltages as a reference to the modulator. To synthesize the voltages, a nine-phase space-vector pulse-width modulator is adopted.

4.3.3 Thermal Validation

To validate the power routing in a 9PIM, a similar FEM-based thermal simulation based on the previous one, yet with a nine-phase converter and a MCM with defected heatsink is developed - as shown in Fig. 4.11. For that, the superposition procedure is applied to the 24-dies module with reduced heat transfer coefficient (h = 3600), and its impedance matrix is also loaded to the numeric software. For the machine simulation, the dynamic model of a nine-phase squirrel-cage developed in [115] is used. For this thermal validation, a real $690\,V/\,1.4\,MW$ three-phase induction machine is taken as a basis, and the parameters are adopted to obtain the equivalent nine-phase machine ones. The rated and equivalent circuit parameters are shown in Tab. 4.1.

The indirect vector control and its tuning process are imlemented in a similar process of an equivalent three-phase machine, as detailed in Appendix B.1.

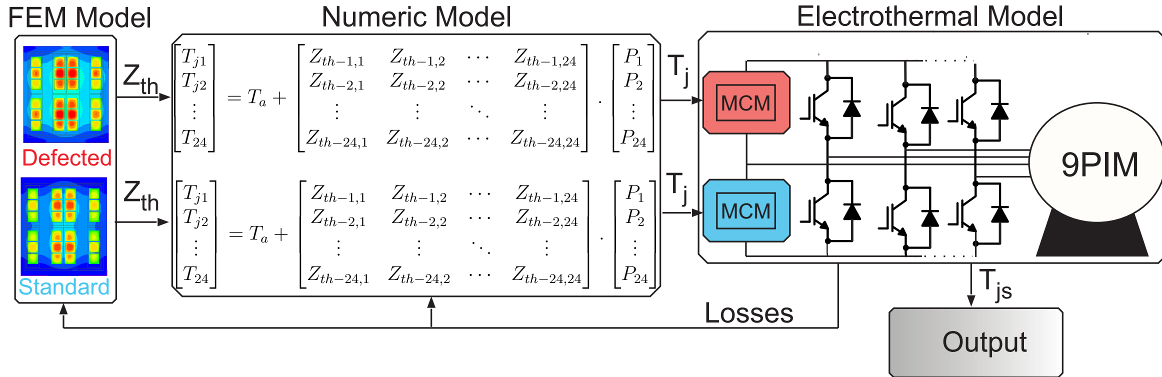


Figure 4.11: FEM-based thermal simulation schematic of the nine-phase machine.

Table 4.1: Rated and equivalent circuit parameters of the 690 $V/$ 1.4 MW nine-phase induction machine.

Parameter	Value
Power	1.4 MW
V_{line}	690 V
I_L	526 A
T_{bd}	200 %
Frequency	50 Hz
Poles	6
Speed	990 rpm
$cos(\phi)$	0.83
η	94.9 %
Slip	1%
J	42.46 kgm^2

Parameter	Value
r_r	8.4 $m\Omega$
r_s	5.8 $m\Omega$
L_r	6.1 mH
L_s	6.1 mH
L_m	5.7 mH

To validate the performance of the proposed power routing strategy, a simulation considering the equivalent nine-phase machine and the 24-dies MCMs in the FEM-based system, shown in Fig. 4.11, is realized. For that, the machine starts at no-load condition, and a load step of 180 % of the nominal torque is applied after the machine achieves nominal speed. As can be seen in Fig. 4.12 (a), the machine operates in balance condition at the beginning, whereby the currents have the same magnitude with the phase displacement of 40 °. The power routing is applied at t = 15 s, and the current of phase A_1 is reduced by 8 %, whilst the other ones increase only by 2.5 %,

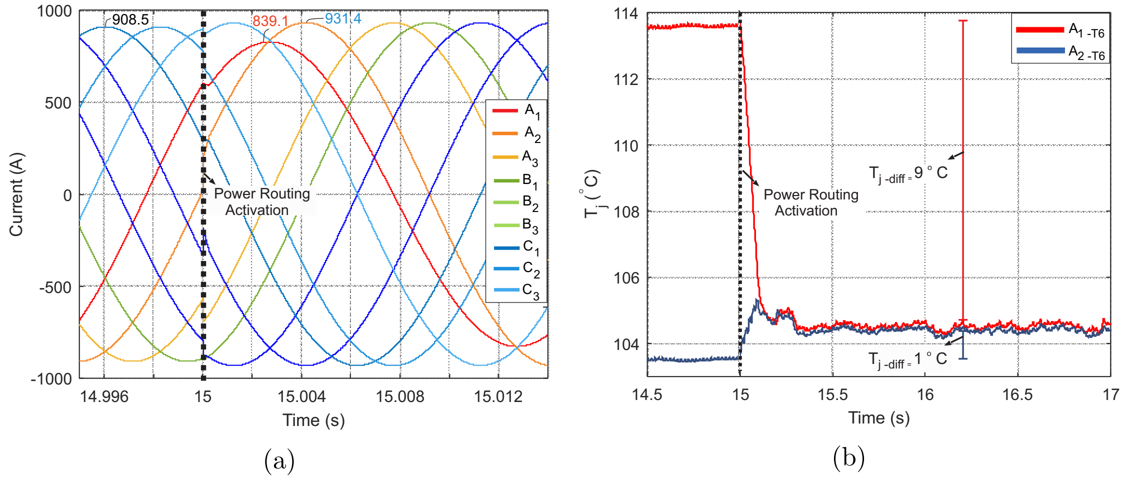


Figure 4.12: Transient results of the power routing - triggered at t = 15 s - in a 9PIM fed by a nine-phase inverter with 24-dies MCMs and a defected heatsink in phase A_1 (a) Current in all phases, whereby the current in phase A_1 is reduced to smooth its thermal stress. (b) Temperature of the hottest dies in the MCMs of phases A_1 and A_2, showing a balancing when the power routing is activated.

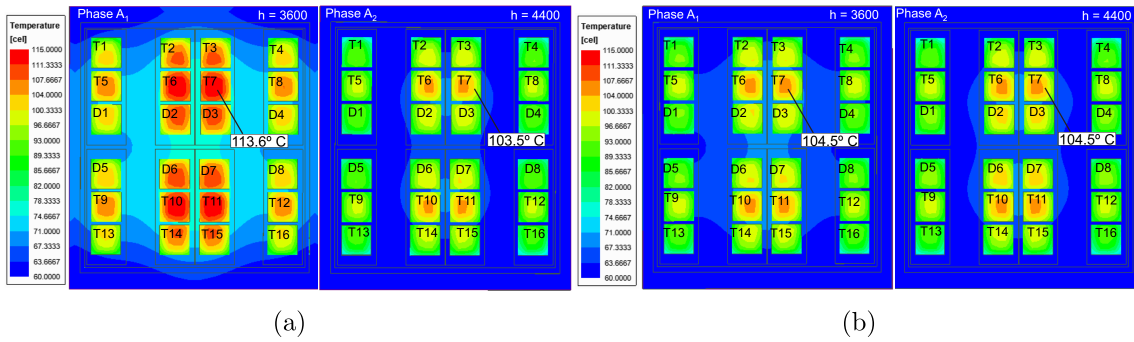


Figure 4.13: FEM analysis of the 24-dies MCM in phases A_1 and A_2 of the nine-phase induction machine (a) Without power routing (b) With power routing.

as highlighted in Fig. 4.12 (a). Moreover, the resulting phase displacement to keep circular magnetomotive force during the soft-unbalance condition - as demonstrated in Sec. 4.3.1 -, is observed . As a result, the temperatures are balanced after triggering the power routing, whereby the hottest die of phase A_{1-T7} (red) - which has a defected heatsink - is reduced by $9\,°C$, whereas the temperature of the hottest die of phase A_{2-T7} (blue) are increased by only $1\,°C$, as shown in Fig. 4.12 (b). Fig. 4.13 (a) and (b), show the FEM results for the temperature of each die for the modules of phases A_1 and A_2 without and with power routing, respectively. As can be seen, there is a temperature reduction - of up to $9\,°C$ -, in all dies of the module with defected heatsink.

4.3.4 Reliability Analysis of the Power Routing in MCIAs

To evaluate the impact of power routing in a 9PIM, a similar case study based on the Mine Hoist presented in Sec. 3.4, is carried out. For that, a 690 $V/$ 1.4 MW 9PIM is adopted, thereby increasing the Hoist payload capacity to 7.4 tons. Therefore, for the new payload, the obtained values for load inertia and static torque on the motor side - firstly calculated in Sec. 3.4 - are now $J_{MS} = 1391\,kgm^2$ and $T_{SM-1pu} = 14250\,Nm$, respectively. Then, one load cycle profile of this new 9PIM- based system is applied to the multiphase converter with the FEM-based thermal models shown in 4.11. Fig. 4.14, shows the resulting junction temperature of the hottest die - T_7 - of the upper module of phase A_1 - with defected heatsink - before (red) and after power routing (blue), thereby showing temperature reductions of up to 9 $°C$. For sake of comparison, the system is simulated again changing the defected heatsink of phase A_1 for a healthy one and its T_j is also demonstrated in Fig. 4.14. As can be seen, the temperature difference of the system with only healthy heatsink to the power routing (blue) is only 1 ° C.

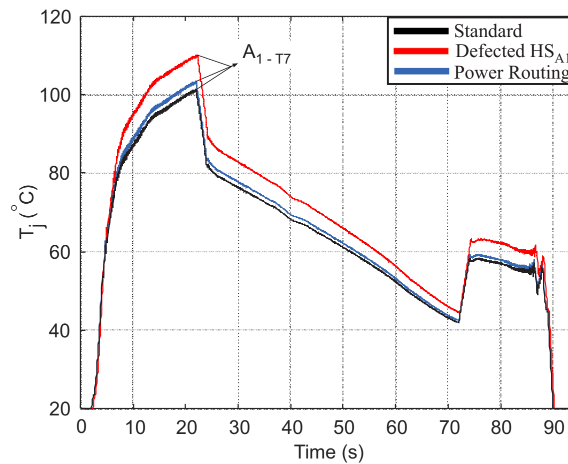


Figure 4.14: Temperature profile for the die T7 of the 24-dies MCM at the top of phase A_1 of the nine-phase converter applied to the mine hoist profile, considering three cases: standard heatsink (black), defected heatsink (red) and defected heatsink with power routing (blue).

From the temperature profiles, it is possible to account the impact of the power routing on the reliability of the hoist system power devices composing the selected multiphase system. For that, the same procedure described in Sec. 3.4.4 is adopted;

thereby, a Monte Carlo analysis considering 10000 samples and same variations, is conducted. Fig. 4.15 (a), shows the quantity of samples failed over time for all the dies of the nine-phase converter for three scenarios: One without any deviation (black), the second one with a thermal deviation of $10°C$ - shown in 4.14 - and the third one considering the power routing. As can be seen, the samples start to fail earlier in phase A_1 with defected heatsink, due to the extra induced temperature. The system-level unreliability of the three cases are shown in Fig. 4.15 (b), whereby the failure probabilities of each die - and modules - are combined, as demonstrated in Sec. 3.4.4. As can be seen, the B_{10} lifetime of the nine-phase power converter is increased from 13 to 16 years - 22 % -, which is only 3 % lower than the system without any thermal deviation among the modules. The temperature and obtained reliability results are summarized in Tab. 4.2.

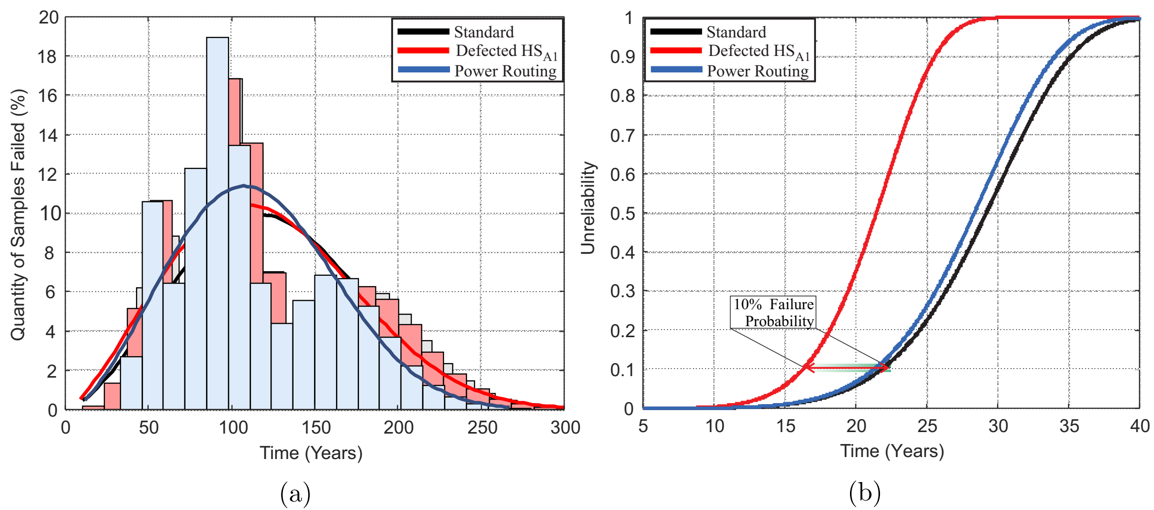


Figure 4.15: Die-level reliability analysis for the mine hoist system driven by a multiphase machine, for the standard system (black), defected heatsink in phase A1 (red) and power routing (blue) (a) Statistical Analysis (b) Unreliability Analysis.

Table 4.2: Comparative analysis for the presented cases of the multiphase drive in the mine hoist system, showing the temperature and B_{10} lifetime.

Case	Standard HS	Defected HS_{A1}	Power Routing
$T_{j-max}\,(°C)$	103.5	113.5	104.5
$T_{j-diff}\,(°C)$	-	10	1
$B_{10}\,(years)$	22.13	16.8	21.58
$\Delta\,B_{10}\,(pu)$	1	0.75	0.97

4.4 Thermal and Aging Monitoring of Power Semiconductor Devices

The demonstrated possibility to increase the reliability during operation through active thermal balancing, motivates the monitoring of junction temperature and state-of-health (SOH) of the power semiconductor devices. In fact, a recently European industry survey has been reported such procedure as the most promising solution to increase reliability of power electronics systems in a near future [20]. Therefore, many research effort has been addressed to this topic in the last years, whereby academia and industry have been looking for a suitable solution to meet all the challenging requirements [66, 120, 121]. This section, presents the proposed methods for temperature and aging monitoring of power devices, demonstrating the variety of solutions and comparing the specificity of each one.

4.4.1 Sensor-based Temperature Monitoring

For the junction temperature sensing, it is possible to directly integrate sensors into the chip. *Mitsubishi*, for example, has developed a commercial solution based on a string of diodes, whereby the junction temperature is obtained through its linear relation with the diode forward voltage [122]. *Fuji*, in turn, has embedded sensors located above the dies, which are integrated to pre-drive control circuit for protection of its intelligent power modules (IPM) [123]. Aiming at detecting temperature variations inside the same device, a solution with several sensors on its surface has been also

proposed [124].

The sensor-based solutions, however, are quite complex and invasive, thereby motivating the monitoring of thermal sensitive electrical parameter (TSEP) for an indirect T_j sensing approach [121, 125, 126]. In addition to the non-invasive and simple implementation, T_j and some TSEPs are also aging precursor parameters (APP), as shown in Fig. 4.16 [66, 127, 128]. The characteristics and implementation challenges of the TSEPs and APPs are detailed in sequence.

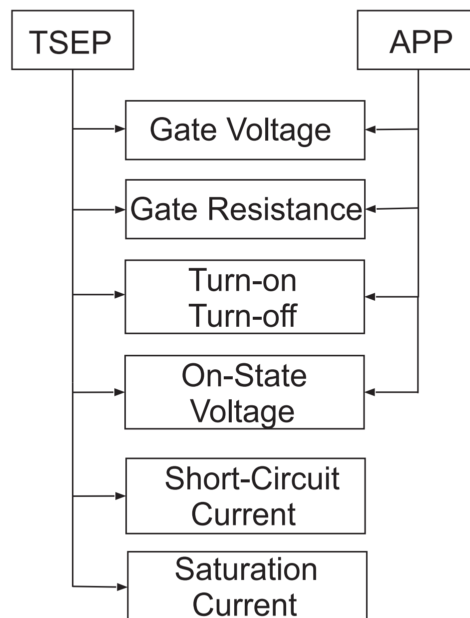


Figure 4.16: Classification of the thermal sensitive and aging parameters.

4.4.2 Gate Voltage Monitoring

The gate-emitter voltage under a specific collector-current value ($V_{ge,i}$) has been proposed as a TSEP, with a sensitivity of $-6.5\,mV/°C$ for lower temperatures and $-8\,mV/°C$ for higher temperatures [129]. Fig. 4.17 shows the proposed methodology schematic, whereby I_c is measured by shunt and regulated through gate-voltage. In this proposal, the calibration procedure is made using pulse currents to avoid self-heating, which can generate errors during the measurement [130]. In addition, $V_{ge,i}$ can vary drastically between devices generating errors of around $10°C$ inside the same module, thereby requiring single calibration process in case of multichip systems. In

addition, increase on the $V_{ge,i}$ rate has been also presented as a potential parameter do detect aging of power semiconductor devices [131].

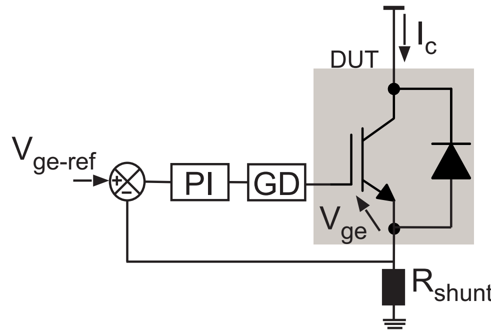


Figure 4.17: Regulation of the collector current for T_j estimation using $V_{ge,i}$. [130]

The V_{ge-th} is also proposed for junction temperature estimation of MOSFET and IGBTs [132, 133, 134, 135]. In this case, the calibration step is made with very low current regulation acting on the gate-emitter voltage. The V_{ge-th} sensitivity varies between $-2\,mV/°C$ and $-10mV/°C$ depending on the semiconductor device. The gate-emitter voltage threshold (V_{ge-th}) is also a precursor parameter to detect aging in the gate-oxide [136]. Operating over 100°, traps accumulate in the IGBT gate-oxide, building up a leakage path, decreasing the oxide area and gate capacitance, thereby increasing the V_{ge-th} during the device lifetime.

The gate-plateau voltage has been presented as a TSEP, showing a linear sensitivity for a fixed current and varying between 1.5 and $7\,mV/°C$ for the entire operating range [137]. Moreover, an in-situ monitoring of the Miller-plateau during the IGBT turn-on is also proposed an aging precursor parameter. For that, the Miller-plateau duration shows a sensitivity for gate oxide degradation and bond wire fatigue [138]. It is demonstrated that bond wire liftoff and aluminum reconstruction overlap doped regions with the surface of the gate polysilicon, thereby resulting in decrease of oxide capacitance and ultimately shortening its duration [138].

4.4.3 Gate Resistance Monitoring

The gate-resistance (R_{g-int}) variation with temperature is also investigated as a TSEP in references [139, 140, 141].In this case, a differential amplifier with an integrator is applied to detect the peak voltage (V_{peak}) - which is directly proportional to the peak current (I_{peak}) - over the external gate-resistance (R_{g-ext}) [139]. Then, the I_{peak} is - indirectly - measured during the turn-on charging cycle, as well as the negative (V_{g-neg}) and positive (V_{g-pos}) voltages of the gate-driver. Hence, the R_{g-int} can be estimated as shown below:

$$R_{g-int} = \frac{V_{g-pos} - V_{g-neg}}{(I_{peak})} - R_{g-ext} \tag{4.6}$$

A method to estimate R_{g-int} with simple modification in the gate driver is presented in [140]. In this approach, a dc current is injected into the gate, and V_{ge} is sensed in two different time instants, as shown in Fig. 4.18. Since the injected current is already known, the R_{g-int} and consequently T_j can be estimated, with an accuracy of roughly $1°C$ and standard deviation of $0.4°C$. This method can be applied independent on the device state - on or off-, but if applied in off-state an special attention has to be taken to avoid an undesirable turn-on [140]. It is furthermore proven these strategies can keep providing good accuracy without considerable deviations even after long operating time [139, 140].

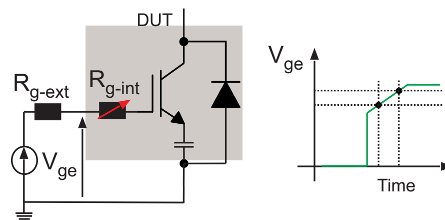


Figure 4.18: The T_j estimation by the internal gate resistance through a predefined dc current injection.

[140]

The sensing process, however, is quite complex because R_{g-int} is tied to the gate

capacitor and the momentary disconnection of the external gate driver is required. The addition of a kelvin resistance as a part of the entire R_{g-int}, is proposed in [142]. In this case, the resistor is added to the die at the kelvin-emitter position, thereby enabling its sensing without gate capacitance influences. The proof-of-concept of this proposal has shown good precision, and further results with kelvin-emitter resistor inside the chip are promised in future publications.

4.4.4 Transient Monitoring

The switching behavior of Si IGBTs [125, 143, 144] and Silicon Carbide Mosfets [145] are also influenced by the temperature. The turn-on time delay, for example, is proposed as a TSEP, whereby a very fast detection circuit counts the time between the V_{ge} rising detection and the starting of the I_c current rising during the turn-on [125, 146]. The turn-on delay increase has presented a linear relation with the temperature, current independence, and a sensitivity close to $2\,ns/°C$. The time span, however, is very short, and the use of high external gate resistance to increase the sensing time, is proposed in [147]. Moreover, the dV_{ce}/dt during the turn-off is also investigated as a TSEP, due to its negative temperature dependence, i.e. as lower the temperature higher the dV/dt. This TSEP also presents an I_c and V_{dc} dependency, as well as high linearity and fixed sensitivity around 6.7 $V/\mu s°C$.

The turn-off time (t_{d-off}) of Si IGBTs has been also studied as a solution for junction temperature sensing [143]. The t_{d-off} - the time between the turn-off command and $V_{ce} = V_{dc}$ - is obtained by measuring the induced voltage on the kelvin emitter parasitic inductor (L_{kE}) of high power module, as shown in Fig. 4.19. Even though the turn-off time is dependent on the I_c and V_{dc} requiring calibration, it has shown a fixed sensitivity of $4\,ns/°C$ and high linearity [143].

The implementation of a smart gate driver with an online monitoring of t_{d-off} SiC Mosfets is presented in [145]. Due to the fast switching and high dV_{ds}/dt of SiC Mosfets, the sensitivity has to be enhanced to achieve online T_j sensing with enough

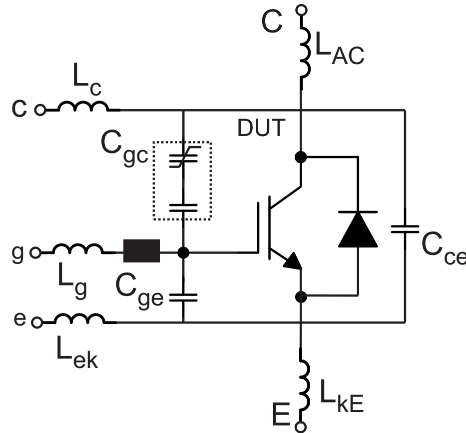


Figure 4.19: High power IGBT module parasitic-based equivalent circuit. [143]

accuracy. One possibility is to insert R_{g-ext}, as suggested in [147]. Nevertheless, the required external resistance is in order of 150-300 Ω, which would dominate the total gate loop impedance and increase the switching time and losses. Therefore, a gate impedance assist circuit is proposed, whereby the auxiliary gate resistor (R_{g-aux}) is associated in series with the gate loop impedance only during the sensing process, as shown in Fig. 4.20. As a result, the sensitivity is improved by a factor of 60, resulting in 760 $ps/°C$. Moreover, a unit base for real time sensing with resolution less than 104 ps, is also developed [145].

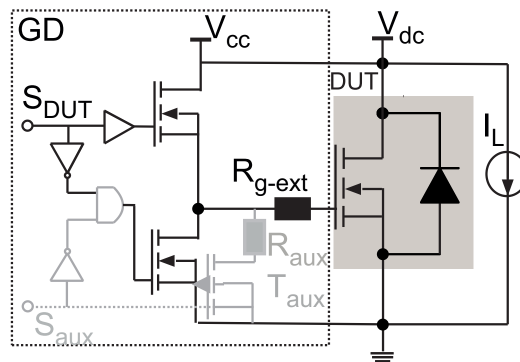


Figure 4.20: Gate impedance assist circuit. [145]

Most of the switching properties of power devices are also affected by aging, and its potential to detect degradation in power devices has been investigated [66]. T_{d-off} and $dVce/dt$ during turn-off has presented a potential to detect soldering and wire

bond degradation [148, 149, 150]. The thermal path degradation increase the die temperature, which ultimately impact the turn-off time [148], whereas the bond wire aging vary the stray inductance, thereby changing the voltage transient [144].

Indeed, a method to estimate t_{d-off} based on very fast sampling - hundreds of MSPS - of the V_{ce} rising during turn-off is proposed for aging detection [151]. For that the V_{ce} is sensed in multiple switching transition when its value is between 20% and 80% of the dc bus, and the Standard Error of the Mean (SEM) is used to calculate the expected t_{d-off} error with statistical precision.

4.4.5 Device Current Monitoring

In IGBT and MOSFETS, the saturation current I_{css} has been proposed as a TSEP [130, 152, 153]. During the measurement, a low V_{gs}/V_{ge} - slightly higher than V_{gs-th}/V_{ge-th} - is regulated through a controller (Fig. 4.21), and the temperature is estimated through its dependence of the electron mobility, which in turn impacts I_{css} [130, 153]. Even though gate-emitter voltage pulses are applied to reduce the self-heating, an interpolation process is necessary to limit the temperature error. Moreover, this TSEP is not linear, the sensitivity is not fixed and presents very poor precision under low temperatures [130].

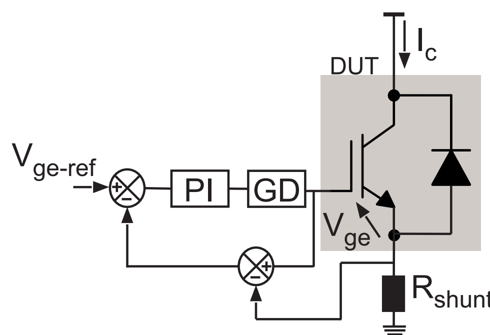


Figure 4.21: The T_j estimation by the saturation current through a regulated V_{gs}.

The short-circuit current (I_{sc}) of an IGBT is also a function of the temperature, and has been investigated for T_j sensing purpose [154]. As shown in 4.22, the temperature of an IGBT can be sensed by applying a short-circuit current pulse to the device under

test (DUT). To eliminate the effect of the auxiliary IGBT, a bypass device with higher current capability is added in parallel. During the sensing process, the bypass device is turned-on, and the dc bus voltage is blocked by the DUT. In sequence, the DUT is turned-on in short-circuit, I_{sc} rapidly reaches the peak and the DUT is turned-off. For that, the current peak shall be defined avoiding to exceed the device short-circuit capability [154]. Although the method has presented an adequate sensitivity $-0.17\,\%/°C^{-1}$ - and linearity, the very high thermal dissipation during the test can compromise the reliability of the devices due to the cumulative degradation effect resulting from repetitive short-circuits.

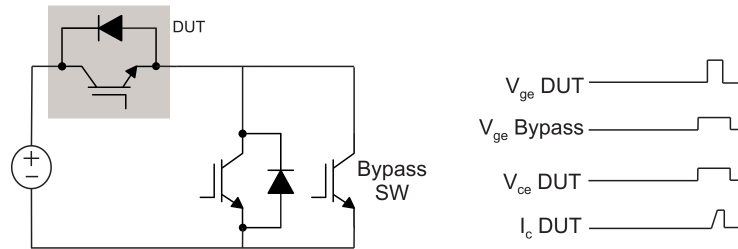


Figure 4.22: The T_j estimation by the short-circuit current.

4.4.6 On-State Voltage Monitoring

The on-state voltage (V_{on}) has been recognized as an effective indicator to predict aging, whereby variations from 5% to 20% comparing with its initial value might indicate a wear out failure by bond wire lift-off or solder joint degradation [120, 155, 156, 157, 158, 159]. Moreover, V_{on} has been presented as a promising TSEP parameter due to its linear sensitivity [160, 161, 162, 163]. However, the requiring of mV-level accuracy, kV-level isolation and noise rejection has challenged its development; therefore, multiple on-state voltage sensing circuits for T_j sensing and condition monitoring have been proposed in the last years [65, 75, 161, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 179].

Fig. 4.23, shows a timeline of the proposed structures in the last 20 years of research. The on-state voltage sensing circuits are designed considering the purpose and application requirements. Considering online junction temperature and device char-

acterization, for example, the circuit has to be immune to switching noise and operate in variable electrical conditions [171]. In addition, the circuits need fast response, which can be in order of few μs considering wide bandgap semiconductor devices [179]. Therefore, fast passive - Zener or diodes - or active - transistor - voltage clamping during the off-state are required for online sensing [164, 171, 176]. Conversely, the condition monitoring can be realized *in* - *situ* - off-line -, thereby taking away the need of fast response and enabling the use of slow devices such as mechanical switches, as also shown in Fig. 4.23 [169].

Online Passive Clamping

The on-state voltage of power devices was firstly adopted to detect zero-voltage crossing in soft switching devices at the beginning of 90's [180]. The introduction of the on-state voltage as a TSEP, however, was presented only in 98's, with the purpose to optimize heat management of IGBTs with two solutions; one with limit of 600 V (Fig. 4.24 (a)) and the other reaching up to 2000 V (Fig. 4.24 (b)) [164]. In such structures, the diodes are responsible to block the high voltage during the off-state and the Zener diodes clamp the output voltage in a reduced level enabling an analog to digital conversion (ADC).

An evolution of this proposal is presented in [169], whereby one Zener is changed by a diode, aiming at reducing the effective stray capacitance, as shown in Fig. 4.25. In addition, two resistors are added, one to limit the current of the Zener and the other to balance the input impedance network to minimize the common-mode error. The clamping circuit, however, has an inherent leakage current during the off-state, which can be really critical in high dc-link [169].

Another variation was proposed in 2015, whereby the Zeners are completely removed and changed by series-connected diodes [172]. Therefore, a cascode current mirror is added to provide equal currents flowing through the high voltage diodes during the on-state, as shown in Fig. 4.26. Hence, the potential at the drain - or collector - is the voltage drop V_d in the upper diode plus V_{on} whilst V_d is the potential at the

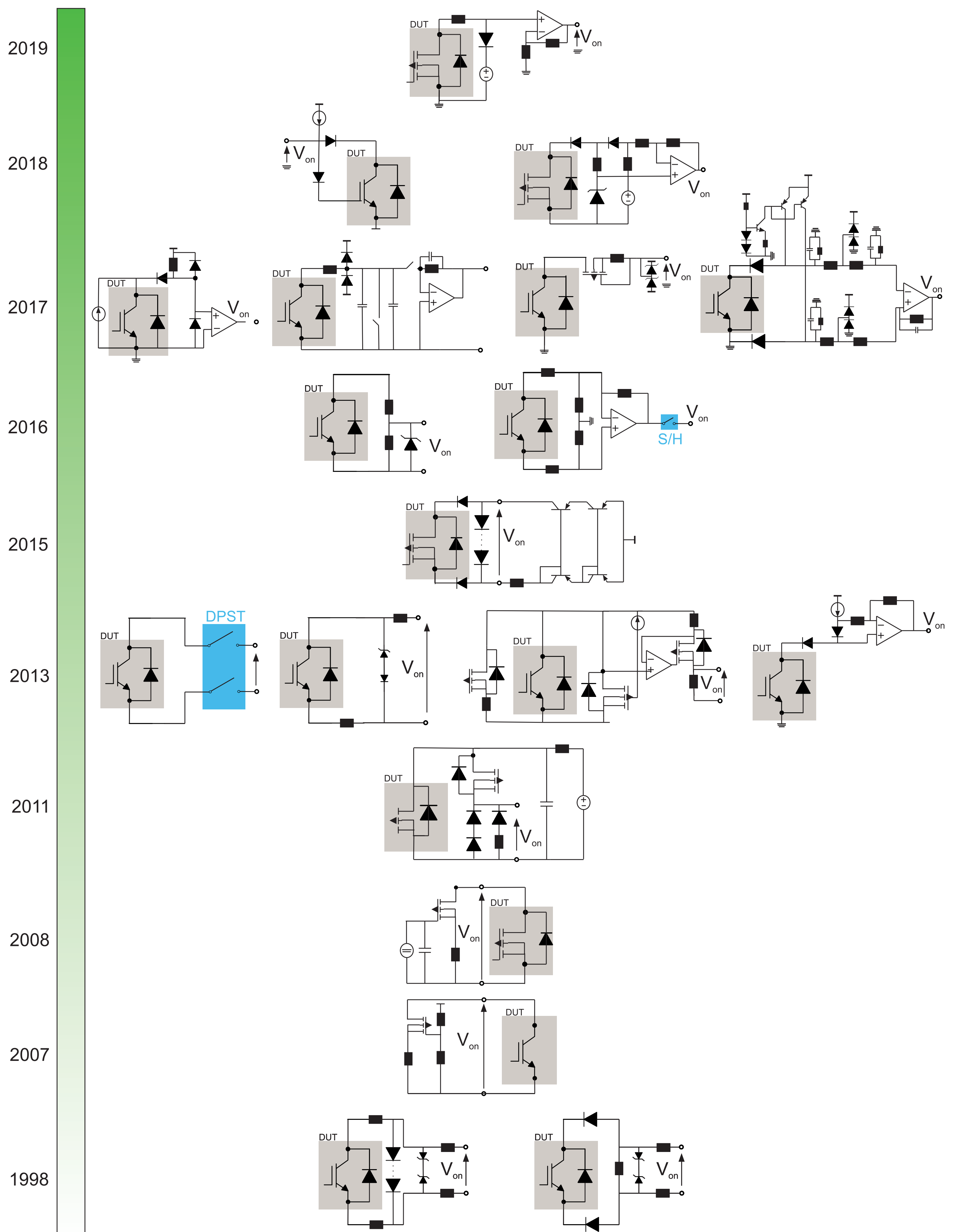


Figure 4.23: The timeline of the proposed on-state voltage sensing circuits.

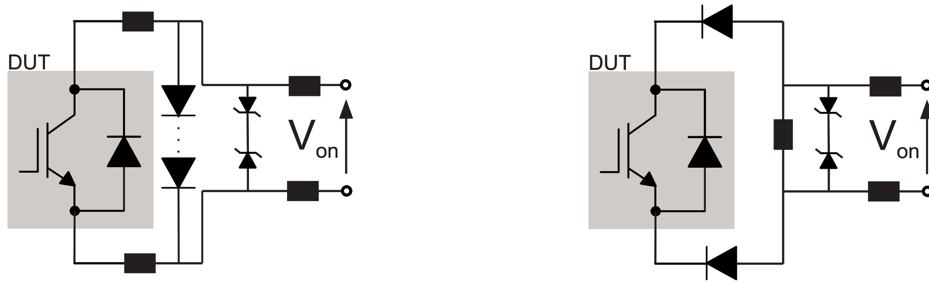


Figure 4.24: The V_{on} sensing circuit with clamping Zener diodes: (a) 0-600 V (b) 0-2000 V

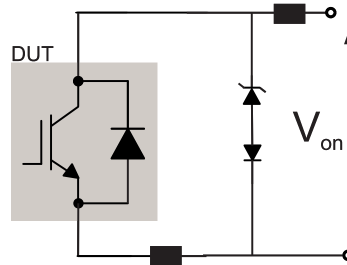


Figure 4.25: The V_{on} sensing circuit with series connection of Zener and a diode to clamp the voltage.

source - or emitter. As a result, V_{on} is measured in the output, considering the same voltage drop in both diodes. During the off-state, on the other hand, the upper current source flows through the clamping diodes, and the output voltage is clamped by the voltage drop of the series association of the devices.

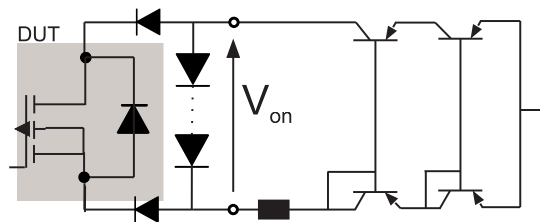


Figure 4.26: The V_{on} sensing circuit with series connection of diode to clamp the voltage and cascode current source.

From the same concept of current injection, a single source solution was presented in [171]. As shown in Fig. 4.27, when the DUT is blocking voltage, the diode is reversely polarized and isolate the measurement circuit. During the conduction phase, however, the source starts to provide current through the two diodes, and considering the same V_d, the diode drop voltages cancel each other and only V_{on} is seen at the amplifier output, as shown in (4.7).

$$V_{on} = 2(V_{on} + V_{d1}) - (V_{on} + V_{d1} + V_{d2}) \quad (4.7)$$

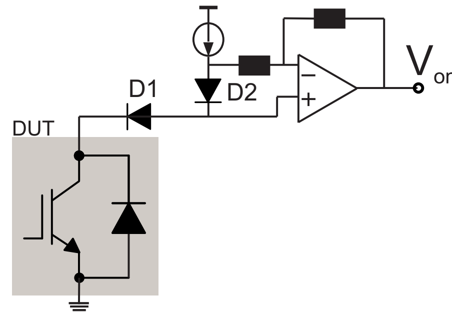


Figure 4.27: The V_{on} sensing circuit with series connection of high voltage diodes and single current source.

A variation of the latest presented circuit, is the one proposed in [178], whereby a similar functionality is brought in a alternative structure. As shown in Fig. 4.28, during on-state the current is provided by the voltage source series-connected to the resistor. Due to the Zener, the D2 voltage drop can be measured and used to 'correct' the offset introduced by D1 [178]. Moreover, the mentioned work presents a design for high switching frequencies, resulting in bandwidths higher than 50 MHz and dynamic response lower than 50 ns - without isolation.

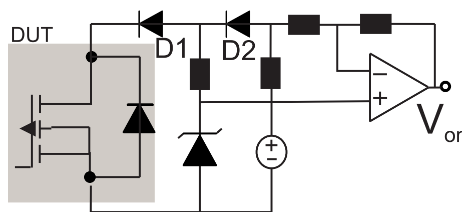


Figure 4.28: The V_{on} sensing circuit based on a sensing current and a series connection of high voltage diodes and Zener.

Even with an identical current provided for both devices by the cascode sources [172] or the series connection of the diodes [171, 178], parametric and thermal deviations result in different V_d, and ultimately voltage offset in the sensing circuit output [179].

To remove the possibility of an offset, a new structure with a voltage source V_{cc} is proposed [179]. As shown in Fig. 4.29, the V_{cc} is selected to be higher than the

maximum V_{on}. Thereby, selecting a diode with very low leakage current and a low input bias operational amplifier, it is possible to ensure a low voltage across the resistor. In addition, a proportional amplifier is added to reduce the common-mode voltage.

In the off-state, the diode is directly polarized and the output measure its voltage drop plus V_{dc}. During the on-state, V_{on} can be measured in the output without V_d and Zener leakage current in the path, thereby eliminating any possible relevant offsets. As a result the circuit provides good accuracy with errors below 0.13 % in a wide T_j and a time response lower than 19 μs.

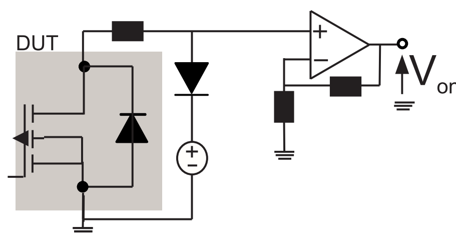


Figure 4.29: The V_{on} sensing circuit based on a V_{dc} clamping .

Online Active Clamping

The active voltage clamping circuit was firstly introduced in the patent 2008/0309355, whereby a MOSFET is included between the terminals of the DUT, as shown in Fig. 4.30 [181]. In short, the auxiliary transistor is turned-off by the voltage raise generated by the current flowing through the resistor, during the off-state. As a result, the output voltage is clamped to $V_{clamp} = V_g - V_{th}$. In on-state, however, the auxiliary transistor starts to conduct, and V_{on} is measured in the output [181]. This solution presents voltage peaks several times higher to the clamping due to parasitic capacitance of the transistor, which can led the device to destruction. In addition, a large dv/dt is present across the DUT capacitance during the transition to the off-state, causing a large current flowing through the voltage supply, potentially leading it to fail [172].

Despite the drawbacks, a real-time V_{on} sensing circuit based on an active clamping circuit is proposed in [176], whereby a N-channel depletion mode Mosfet is adopted.

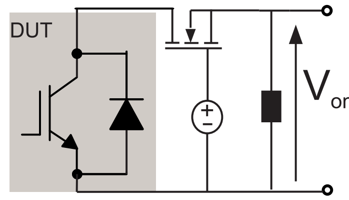


Figure 4.30: The V_{on} sensing circuit with active voltage clamping.

During the on-state of the DUT, the current is not flowing through the Mosfet, thereby turning it on and enabling the V_{on} sensing in the output as shown in Fig. 4.31. Conversely, the current flowing in the clamping circuit during off-state, turns-off the Mosfet through the resistor voltage drop, and the clamping voltage is seen in the output.

Offline Isolation

The offline isolation based V_{on} sensing circuits are generally applied general to monitor the degradation of the devices $In - situ$.This realization can be , for example, during a start-stop of a electric vehicle or programmed pauses in Industry [6, 161, 169]. Fig. 4.32, shows a relay-based isolation for V_{on} sensing in applications with high dc-link, whereby the main goal is the reduction of the leakage current and parameter mismatches of semiconductor devices impacts during the sensing process. In short, relays are turned-on - offline - only during the sensing process and a specific current is applied to the DUT without disturbances. As a result, the V_{on} is sensed with very high precision, presenting deviations lower than 0.05% [169].

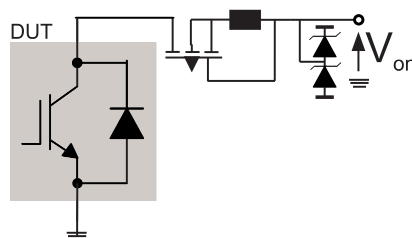


Figure 4.31: The real-time V_{on} sensing circuit with active voltage clamping.

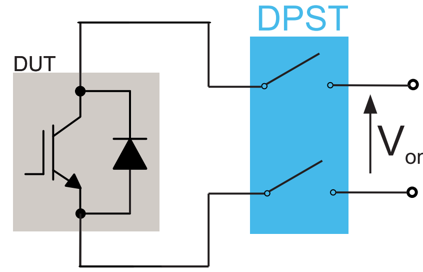


Figure 4.32: The off-line V_{on} sensing circuit with relay-based voltage isolation.

Methods for Tj Estimation throuh V_{on}

- Low current T_j Sensing

The V_{on} under low current sensing was firstly introduced in [182] and is nowadays the most common method to obtain the chip temperature of a bipolar transistor [183]. in this method, a low sensing current is applied to the device under different temperatures and a 2-D fitting curve $V_{on}(Tj)$ is obtained [182]. As a result, the simple calibration process is not affected by the self-heating of the dies.

Fig. 4.33, shows an experimentally obtained fitting curve, whereby an $1\,A$ dc current is applied to a single IGBT device under different fixed temperatures. In this process, the IGBT module $DP25H1200T01667$ $(1200\,V/25\,A)$ is adopted, which is placed over a heatplate to apply the temperature variation. As it can be seen, this curve is linear in a wide temperature range, presenting a slope of $1.8\,mV/°C$ and a negative thermal coefficient (NTC). To estimate the temperature, the same current is applied to the device during operation, the V_{on} is sensed and the fitting curve is interpolated to obtain T_j [163].

In general, an auxiliary circuit to apply the sensing current is required and the system stop may change the temperature even in a fraction of second [184]. An alternative solution for V_{on} sensing under low current without stopping the system is proposed in [183]. In this strategy, the load current is modified intermittently during very short times - around 100 μs - and the V_{on} is sensed when the current cross the respective I_{sense} . This method, however, impact the output current quality and generate electromagnetic interference. Furthermore, it is limited to converter with low

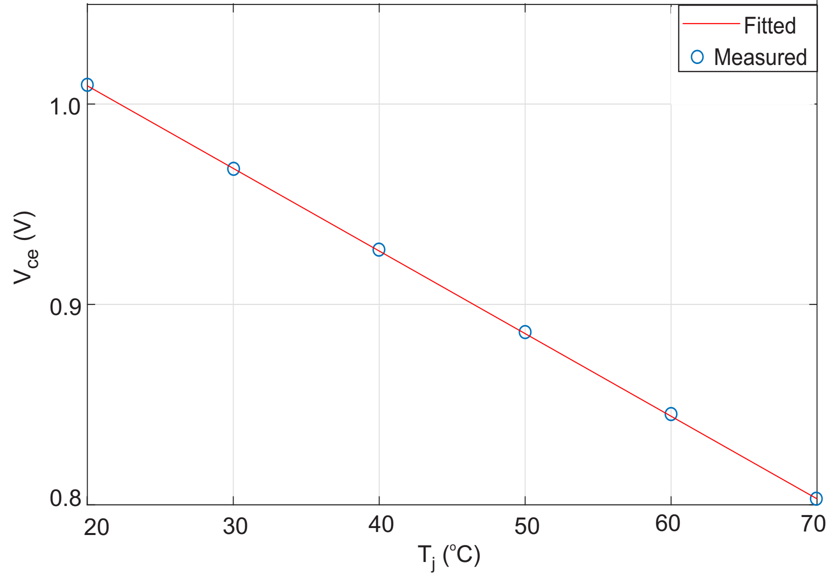


Figure 4.33: Low current T_j calibration curve experimentally obtained from a 25 A IGBT (DP25H1200T01667).

inductive load, whereby specific current values can be applied in a short time.

- High current T_j Sensing

The T_j can be also sensed through V_{on} under high and variable current [61, 163, 163]. The calibration procedure, however, is done monitoring the temperature to take the self-heating into account. In [164], it is proposed to sense the device temperature during the calibration by using an infrared camera, which is indeed limited for most applications. A more common method based on the monitoring of the baseplate temperature is proposed in reference [169]. Nevertheless, the electrical connections voltage drop and its temperature sensitivity results in considerable sensing errors [169]. The possibility to sense V_{on} using the Kelvin emitter to avoid the connection voltage has not shown effectiveness to overcome this problem, and an alternative solution based on an assumption of the resistivity and temperature of them is proposed in [61]. Another calibration procedure adopting a controlled cooling system is demonstrated in [185], proposing furthermore a mathematical model to embed the variable sensitivity by fitting results obtained from different currents, as shown in (4.8).

$$T_j = T_{j0} + \frac{V_{on}(I_c,T_j) - V_{on}(I_c,T_{j0})}{\alpha I_c + \beta}. \quad (4.8)$$

where, α and β are the fitting parameters to define the shape of V_{on} (I_c) at certain calibration temperature.

The possibility to sense T_j only under rated load current is proposed to reduce the calibration effort. In this strategy, the V_{on} sensing is triggered only when the current crosses the calibrated value. This strategy has demonstrated good sensing capability, yet with low bandwidth in low-frequency sinusoidal application (50 Hz), and not suitable for load variable applications [183].

Aging Impacts and Compensation

The aging of the power module structure such as chip delamination, solder degradation and wire bond liftoff can impact the V_{on} sensing, ultimately generating errors on the T_j sensing in long term [185, 186, 187]. Therefore, some strategies to sense and compensate the degradation effects have been proposed. In short, the V_{on} is sensed at the inflection point to obtain only the aging-related variation due to the zero thermal coefficient (ZTC) in this region - as shown in Fig. 4.34 [176, 188, 189].

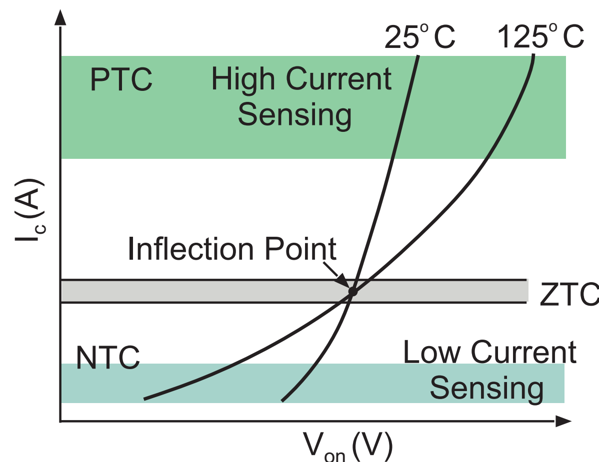


Figure 4.34: Operating region of an IGBT depending on the collector current. The temperature does not impact the V_{ce} with a specific current - i.e. at the inflection point.

There are also challenges to detect the aging through V_{on}, due to the concurrence of different failure mechanisms which can change the trend of on-state voltage variation [190]. As a solution, the decoupling of such influences by sensing at different points and using auxiliary APPs - e.g. V_{ge-th} has been proposed [191, 192].

4.4.7 Comparison of Thermal and Aging Monitoring Strategies

Due to the multiple strategies proposed in the last years, a considerable number of papers comparing condition monitoring [66, 120, 193, 194] and junction temperature sensing strategies [121, 130, 160] has been published. This section brings a comparative analysis regarding the characteristics, pros and cons, related in the mentioned references.

Thermal Sensitive Parameters

In Tab. 4.3 a comparison among the proposed thermal sensitive parameters is stated. The short-circuit current (I_{sc}) has shown a good linearity and performance, yet not safety during the application [154]. Even though the saturation current presents a good linearity, it has a variable sensitivity which can disturb its applicability [130]. The on-state voltage (V_{ce}) has indeed good linearity, low calibration requirements and simplicity during implementation - if compared with the other solutions. Conversely, the low resolution challenge its online implementation, and the heating of other ele-

Table 4.3: Comparison of Thermal Sensitive Parameters.
[121]

Method	Device	Dependents	Linearity	Resolution	Considerations
I_{sc}	IGBT	T	Good	150 $mA/°C$	Low safety
V_{sat}	MOS	T,V	exponential	Varies	Unknown frequency
V_{on} Low Current	All	T,I	Good	$mV/°C$	Only fixed current
V_{on} High Current	All	T,I	Good	$mV/°C$	Affected by elements (wb)
R_{g-int}	MOS	T	Good	$m\Omega/°C$	Current injection required
T_{off}	IGBT	T,I,V,Rg	Good	$ns/°C$	Affected by harmonics
T_{on} delay	MOS	T,Rg	Good	$ns/°C$	Rg changes required
dV/dt	MOS	T,I,V,Rg	Good	$ns/°C$	Rg changes required

ments can impact its sense under high current [182]. Therefore, the possibility to sense it only at fixed and low current shows up as a solution, yet showing limited implementation, as detailed in section 4.4.6 [183]. The transient behavior of devices have also been proposed as a TSEP, such as the turn-on/turn-off times and the dV/dt, showing good linearity but requiring very fast sensing circuits, especially for SiC Mosfets [125, 143, 144].

Condition Monitoring

Tab. 4.4, brings a comparison among existing CM techniques for power modules with degraded parts they can detect, advantages and shortcomings. As can be seen the V_{on} is a mature technique which can be successfully applied offline and $In-situ$ to detect three different failure mechanisms [84, 169]. Even though the threshold gate-emitter voltage (V_{ge-th}) and the gate current (I_g) have presented the same maturity, it is limited only to detect the gate oxide degradation [65]. The thermal resistance has shown capability to detect thermal path deterioration in controlled conditions, yet showing poor performance in variable losses and environment conditions. Another possibility is a thermal sensor solution, which is capable of detecting wire bond degradation in any conditions, but presenting high cost due to the necessity of multiple sensors and limitations in multichip systems.

Table 4.4: Comparison among CM techniques.

Parameters	Detection	Advantages	Shortcomings
V_{on}	Metalization Wire bonds Gate oxide	Mature In-Situ Offline	Affected by multiple mechanisms Hard to sense online
V_{ge-th}	Gate oxide	Mature Low Fsw	Hard to sense under working conditions
I_g	Gate Oxide	Mature	Hard to sense under working conditions
R_{th}	Thermal Path	Easy in Lab In-Situ Offline	Hard to sense under variable conditions
dV_{on}/dt	Wire bond	Integrable	Influenced by gate oxide and GD circuit
Sensors	Wire bond	Easy to measure	Multidamage indicator High Cost Not applicable in MCM

4.5 Validation of a V_{on}-based Thermal Balancing Strategy

Although many thermal balancing strategies have been presented, their implementation with a practical junction temperature sensing structure is scarcely explored. Therefore, a thermal balancing with thermal sensitive parameter (TSEP) based T_j sensing is implemented and validated in this section. Based on the conducted analysis in the previous section, a V_{on} sensing circuit is selected, due to its capability to detect aging and sense the junction temperature in a relatively simple structure; therefore, the circuit described and shown in Fig. 4.27 is implemented [171]. This structure, is the base of recent proposed solutions [178, 179] and stands out due to the lower number of components which furthermore involves only passive devices.

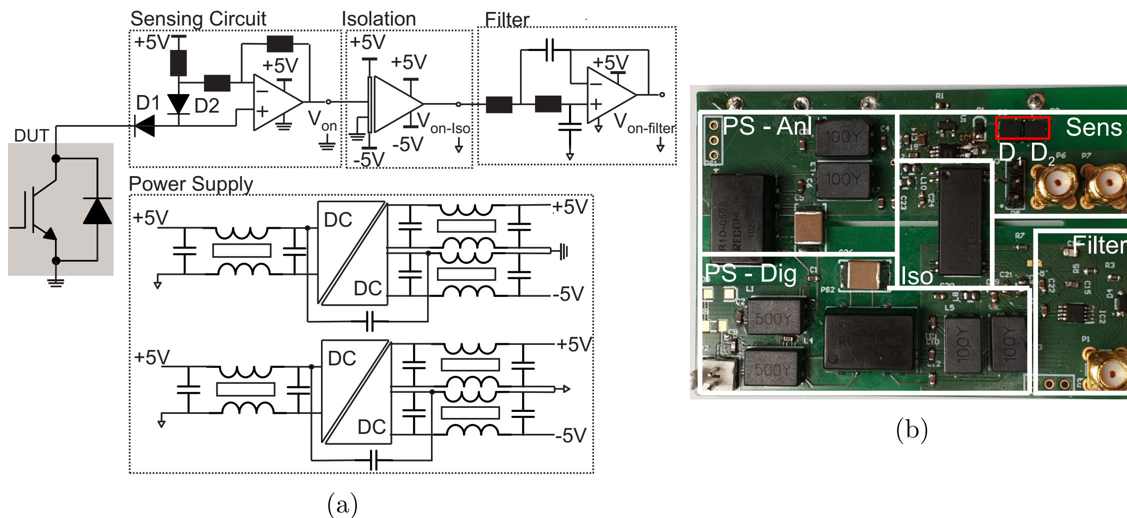


Figure 4.35: The V_{on} sensing circuit with series connection of high voltage diodes, single current source, low noise dc power supply and isolation (a)Schematic (b) Board

The first working condition of the sensing circuit is when the device is blocking voltage, whereby D1 is reversely polarized to isolate the measurement circuit from high-voltage. During the conduction phase, however, the current source composed by the power supply and a series resistor, starts to inject a current current of $10\,mA$ to the two diodes and the device under test (DUT). To extract only the on-state voltage, an operational amplifier is added and configured to cancel the voltage drops (V_d) in D1

and D2, as demonstrated in (4.9). Thereby, considering the same V_d for both diodes, only V_{on} is sensed in the output [171]. Nevertheless, parametric deviations and thermal mismatches between the diodes can result in different V_d and ultimately a V_{on} offset in the output, as detailed in Sec. sec:Tsep. To mitigate the impact of thermal deviations, SiC Schottky diodes (C3D1P7060Q) are selected due to its negligible reverse recovery. Moreover, the injection current is selected to make the diode operate in ZTC region - where the current does not affect the voltage drop - and they are placed very close to each other for better thermal coupling to reduce potential thermal deviation, as shown in Fig. 4.35 (b). In addition, very low noise devices with high bandwidth and digital filters are implemented to achieve high resolution, and further details are given in Appendix A

$$V_{on} = 2(V_{on} + V_{D1}) - (V_{on} + V_{D1} + V_{D2}) \tag{4.9}$$

4.5.1 V_{on}-based T_j Sensing

To validate the capability of the proposed V_{on}-based circuit to sense T_j, the on-state voltage of an IGBT - DP-25F1200T-101666 - conducting $1\,A$ dc under fixed temperature, is measured. For that, the power module is placed over a heatplate with controlled temperature at $52\,°C$, as shown in 4.36 (a) . As can be seen in Fig. 4.36 (b), a $V_{on} = 882.5\,mV$ with precision of $0.3\,mV$ is obtained, after applying a 50 samples moving average filter as described in Appendix A. Thereby, interpolating the fitting curve experimentally obtained for the device conducting the same dc current - detailed in Sec. 4.4.6 -, the capability of the V_{on} circuit to sense the temperature is demonstrated. As shown in Fig. 4.36 (c), the measured $V_{on} = 882.5\,mV$ matches the fitted $T_j = 52\,°C$, with very small difference.

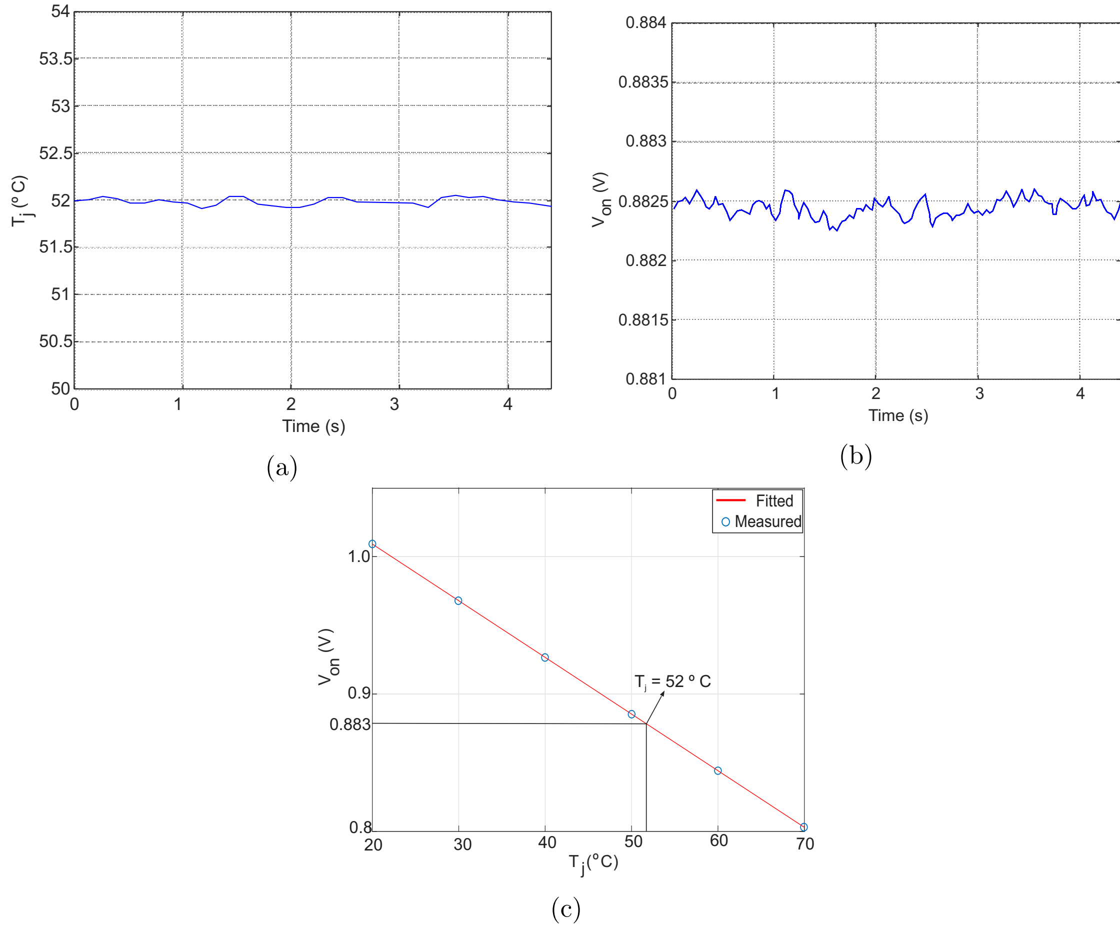


Figure 4.36: V_{ce}-based T_j under fixed current $I_c = 1\,A$ and temperature $T_j = 52\,°C$ (a) Junction temperature measured via fiber optic sensors (b) V_{avg} obtained from a fifty sample move average filter using an 1 MSPS ADC in burst mode (c) Fitting curve obtained with fixed low current of $1\,A$.

4.5.2 V_{on}-based Thermal Balancing

After demonstrating the capability of the V_{on} to sense T_j, the next step is to validate its effectiveness to feedback thermal balancing strategies. As shown in Fig. 4.37, the validation setup is composed by two buck converters connected in parallel with the same dc-bus. As it can be seen, the setup is composed by two buck converters, each one with a specific V_{on} sensing circuit, and open modules without gel. To obtain a homogeneous emissivity the module is also painted in black. Moreover, one converter is placed over a heatsink to generate a specific thermal mismatch, and a fiber optic system to measure the device temperatures is adopted. The validation parameters are stated in Tab. 4.5.

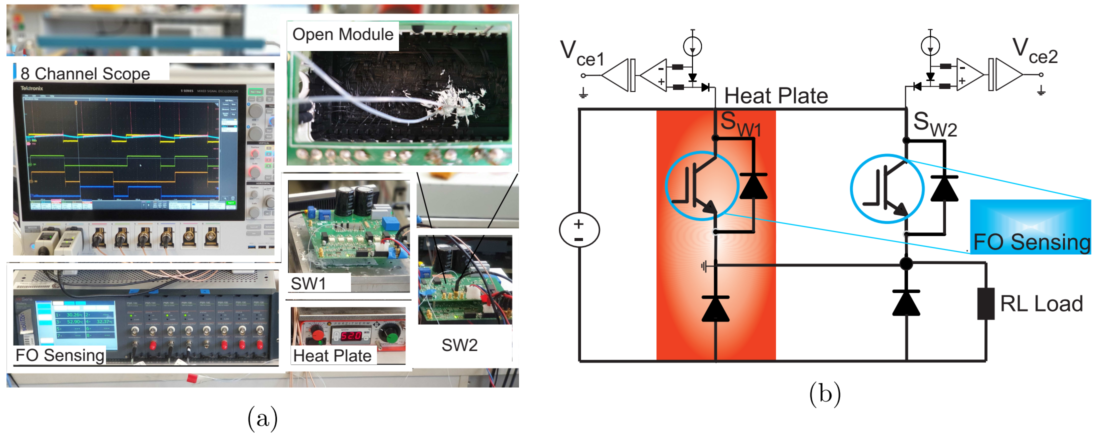


Figure 4.37: Validation setup consisting of two buck converters in parallel with V_{on} sensing capability, whereby one is placed over a heatsink to obtain a specific thermal deviation. A fiber optic system is used to measure the temperature on the chips and validate the strategy (a) Photo (b) Schematic.

Table 4.5: Validation parameters for the the V_{on}-based thermal control.

Power Module	DP-25F1200T-101666
Power Capability	2x 25 A/1200 V
V_{dc}	250 V
$I_{out-peak}$	15 A
F_{sw}	1 kHz
Duty Cycle	0.5

For the thermal balancing, an on-off control strategy is implemented, whereby the hotter device is turned-off during specific periods. As shown in Fig. 4.38, the V_{ce} of each device is sensed and the T_j estimated by the lookup table. Then, the IGBT with highest temperature has its PWM blocked by the comparator output connected to an

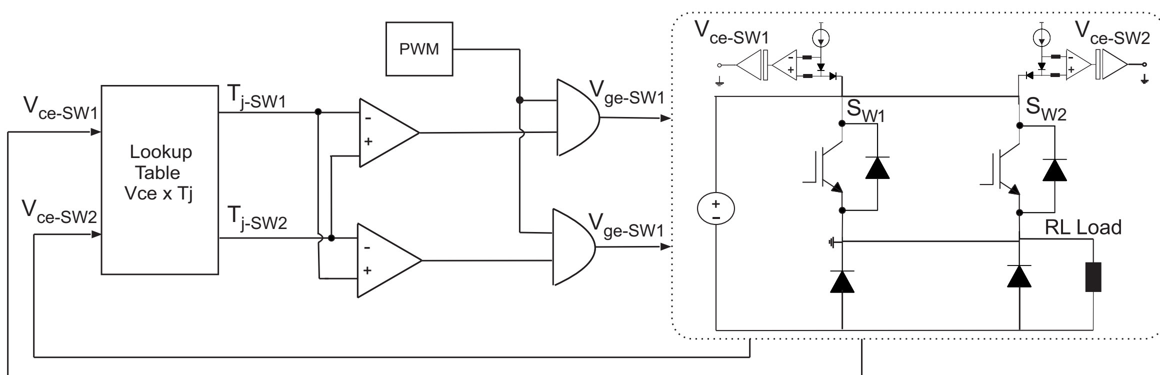


Figure 4.38: V_{on}-based on-off thermal balancing strategy, whereby the junction temperatures are sensed and the device with highest one has its PWM command blocked.

AND logic port. In this case, only one device is conducting at a time and the on-state voltage can be used to sense its temperature during the balancing process. As shown in Fig. 4.39, a deviation of $9\,°C$ is generated by the heatplate at the beginning of the operation. At $t = 3\,s$, the thermal balancing is triggered, the V_{ce}s are sensed and the device with higher temperature is deactivated in the next period, thereby transferring the total power to the colder one. As a result, the T_js are equalized by indirect sensing T_j through the V_{on} of the devices, as shown in Fig. 4.39.

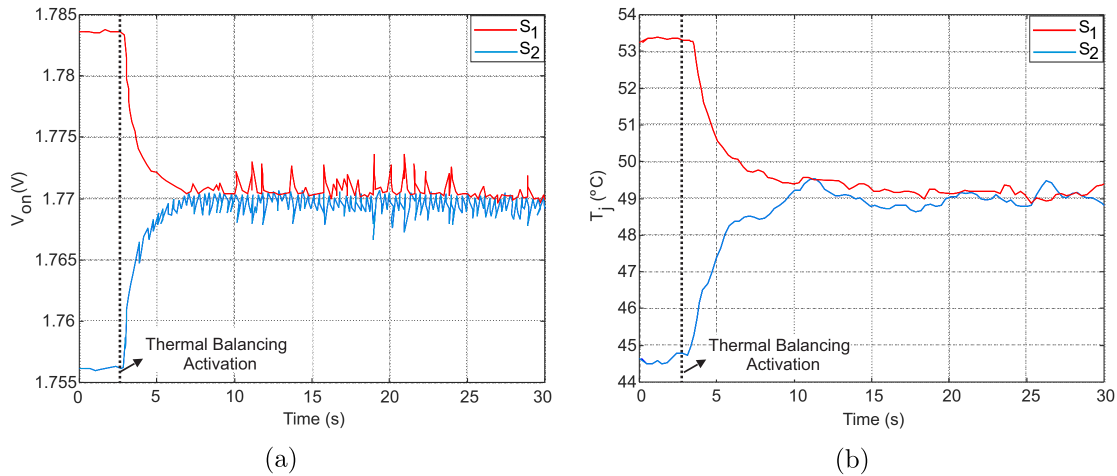


Figure 4.39: Experimental validation of the V_{on}-based thermal control. The junction temperature starts with a deviation of $9\,°C$, and it is equalized after the thermal control is triggered at $t = 3\,s$. (a) V_{on} of each switch (b) Measured temperature of each switch.

4.6 Short Summary of the Chapter

In this chapter, the thermal control is presented as a solution to balance uneven temperatures and alleviate thermal stress of devices by manipulating its losses. Moreover, a state-of-the-art of the junction temperature sensing and aging detection of power semiconductor devices is described, whereby the proposed solutions are presented and compared. The V_{on} based monitoring has presented some advantages in comparison with others, such as linearity, reasonable resolution, capability to detect multiple imminent failures and relative implementation simplicity. Therefore, a V_{on} sensing circuit with a very low noise design is implemented and validated, showing a

resolution of $0.3\,mV$. Moreover, its capability to sense T_j and close the loop of thermal control is experimentally validated.

Chapter 5

Die-Level Thermal Balancing in Multichip Modules

Contents

5.1 Introduction . . . 97
5.2 The Multi-gate Multichip Structure . . . 97
5.3 Die-Level Thermal Balancing . . . 98
5.3.1 Pulse-Shadowing Based Thermal Balancing . . . 99
5.3.2 Turn-off Losses Manipulation for Thermal Balancing . . . 108
5.3.3 Comparison of the Thermal Balancing Solutions . . . 115
5.4 Indirect Thermal Balancing for Diodes . . . 118
5.5 Selective T_j Sensing and the Pre-Programmed Thermal Balancing . . . 120
5.6 Reliability and Efficiency Analysis of the Die-Level Thermal Balancing in MCIA . . . 122
5.7 Technical Analysis of the Proposed Solution . . . 126
5.7.1 Multi-Gate Driver Considerations . . . 126
5.7.2 Power Level Margins . . . 127
5.8 Short Summary of the Chapter . . . 128
5.8.1 Evaluation System with Equivalent Multi-gate Multichip Module 129

5.1 Introduction

Even after 30 years of research, multichip modules still presenting high thermal deviations and extra heat in a subset of devices, as detailed in Sec. 2.3.2. As a result, MCM-based power converters has been operating with reduced reliability, especially in mission critical applications - Chap. 3. As validated in Chap. 4, thermal balancing strategies are able to overcome thermal mismatches and increase lifetime of power converters. This chapter, presents and investigates a die-level solution to overcome thermal mismatches among the dies of a more flexible MCM structure. Thereby, three novel balancing strategies to reduce thermal stress in transistors and diodes of an IGBT-based MCM, are proposed. To evaluate the impacts of the proposed solutions in mission critical applications, a case study based on the aforementioned mine hoist system, is conducted. To validate, evaluate and compare the presented solutions, FEM-based thermal analysis and experimental tests are conducted.

5.2 The Multi-gate Multichip Structure

As shown in Fig. 5.1 (a), a standard high power multichip module is composed by several devices with a single gate-emitter connection. Therefore, a high number of devices are controlled by a single gate driver and, consequently, the same pulse-pattern. The multi-gate multichip module concept, however, is based on the traditional MCM structure, yet with multiple gate-emitter connections, as shown in Fig. 5.1 (b).

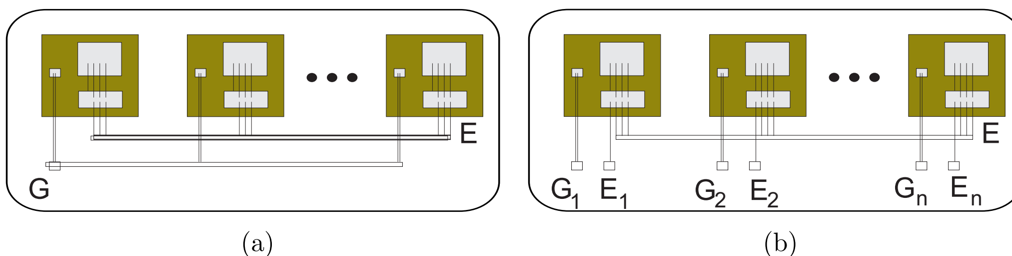


Figure 5.1: Multichip Modules (a) Standard Structure (b) Multi-gate Structure

The purpose of the multi-gate MCM structure is to to give flexibility to the structure, which enabled the control of specific group of dies by independent gate drivers.

To select the groups, the temperature distribution inside the MCM - Fig. 2.16 - is analyzed and the devices with similar thermal stresses are grouped in equivalent switches (SWx). Considering the presented 24-dies MCM, the sixteen IGBT dies can be divided into four equivalent switches with respective gate-emitter connections, as shown in Fig. 5.2. Even though the internal structure of the MCM is modified, the parallel devices are connected through the same collector/emitter - or drain/source - busbar structure, as shown in Fig. 5.1. Therefore, this structure has the same collector-emitter stray inductance and the gate-emitter loop can be even reduced, compared to an ordinary MCM [195].

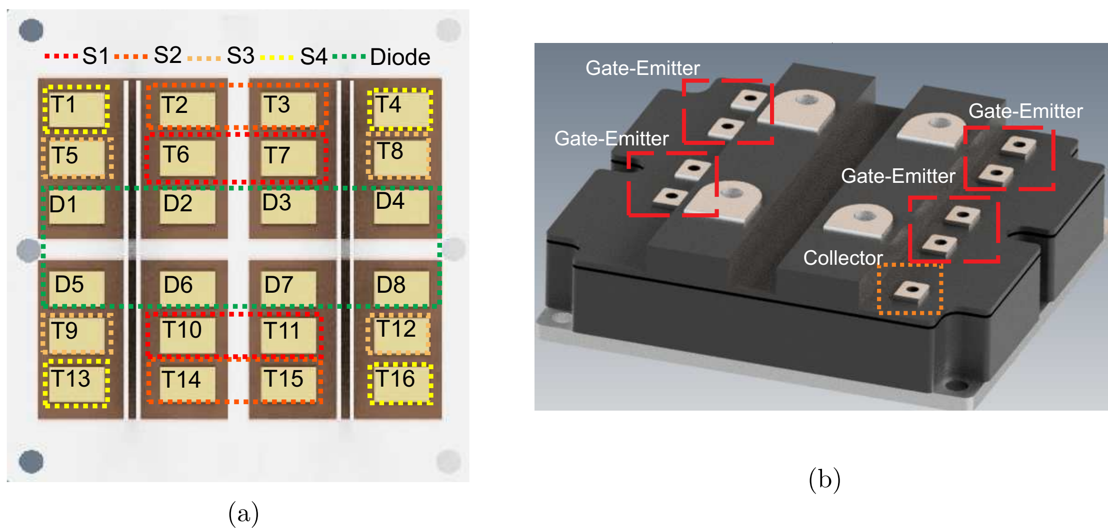


Figure 5.2: Proposed packaging with four equivalent switching groups. (a) Open package with switching groups (b) Package structure with four gate-emitter connections.

5.3 Die-Level Thermal Balancing

Based on the more flexible multi-gate structure, this work proposes the die-level thermal balancing to overcome thermal mismatches in MCMs. As shown in Fig. 5.3, the junction temperature of the devices - or switching groups (Fig. 5.2 (a)) - are sensed and the pulses are processed to manipulate the losses among them. This control is realized in a gate-driver level, whereby the pulses come from the modulator and are manipulated without modifying the converter control structure. Therefore, it

is possible to act on the turn-on [28, 39], turn-off or even shadow the pulses during a complete period [63], as shown in Fig. 5.4 and detailed in sequence.

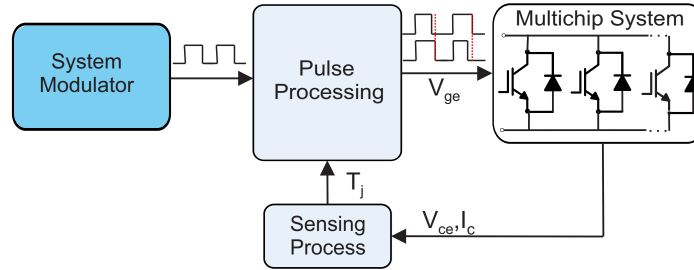


Figure 5.3: Full diagram of the thermal balancing in multichip multi-gate modules, with V_{on}-based T_j sensing

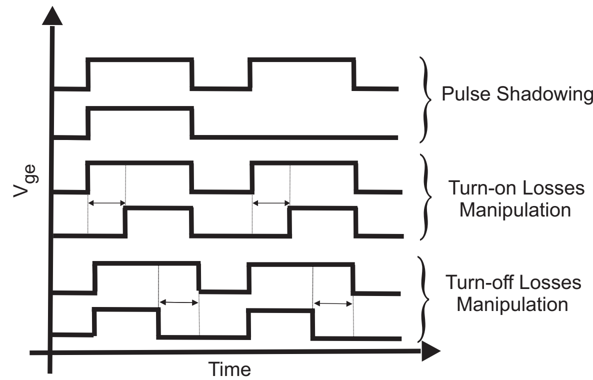


Figure 5.4: The pulse-processing approaches for die-level thermal balancing: pulse-Shadowing, turn-on losses manipulation and turn-off losses manipulation.

5.3.1 Pulse-Shadowing Based Thermal Balancing

One solution to achieve thermal balancing in MCMs is by shadowing pulses of the devices - or SW [29, 63]. Therefore, this work proposes and investigate the pulse-shadowing strategy for thermal balancing in MCMs. As shown in Fig. 5.5 the temperatures are sensed and the hotter devices remain turned-off during specific switching periods. Thereby, the shadowed device dissipates lower mean losses - switching and conduction - and the temperatures are balanced by alternating the process among them over time.

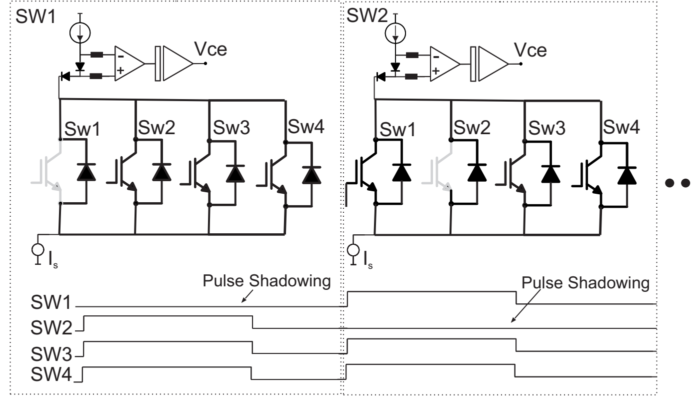


Figure 5.5: The pulse-shadowing based thermal balancing pulse pattern.

Proportional Control

To realize the die-level thermal control a linear strategy based on average losses and a proportional controller is proposed. In this strategy, the average losses of the devices are manipulated inside a limited period defined by a specific number of pulses. As shown in Fig. 5.6, a mean temperature is defined as a set-point (T_{j-avg}) and it is compared to the measured junction temperatures, this temperature set-point is obtained online by an average of the measured junction temperatures, as shown in 5.1.

$$T^*_{j-avg} = \sum_{i=1}^{N_{dev}} \frac{T_{ji}}{N_{dev}} \tag{5.1}$$

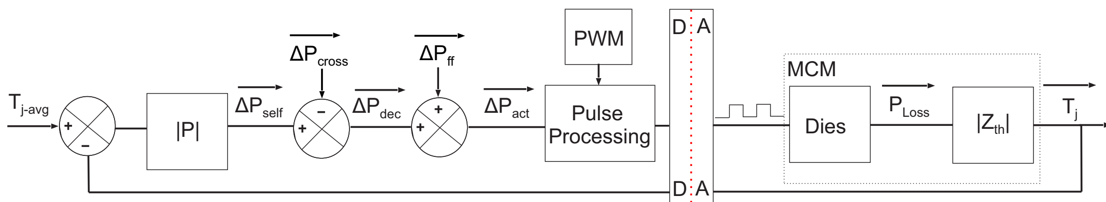


Figure 5.6: Die-Level proportional control based on average losses.

Based on the temperature differences, the proportional controller ($|P|$) acts on the die average losses - represented by the vector $\overrightarrow{P_{loss}}$ - aiming at equalizing the $T_j s$ to the reference one. As detailed in Sec. 5.2, the dies of presented MCM is divided in four groups, each one with a single gate-emitter connection. Therefore, the temperature of one device per group is compared to the set-points, which results in four errors ($\overrightarrow{e_{tj}}$). Hence, the control variable vector ($\overrightarrow{\Delta P_{self}}$) is composed by four

elements, and the proportional controller can be represented by a 4x4 matrix, as shown in 5.2. The proportional losses variation is given to the pulse processing block, which is then responsible for applying the specific extra - or reduced - losses to each group of devices.

$$\overrightarrow{\Delta P_{self}} = \overrightarrow{e_{tj}} \cdot \begin{bmatrix} P & 0 & 0 & 0 \\ 0 & P & 0 & 0 \\ 0 & 0 & P & 0 \\ 0 & 0 & 0 & P \end{bmatrix} \tag{5.2}$$

Once the thermal network is fully knowing, it is possible decouple the effects of the thermal cross-coupling on the temperatures, by applying a decoupling vector ($\overrightarrow{\Delta P_{cross}}$). The $\overrightarrow{\Delta P_{cross}}$, calculates online the proportional power generated by the neighbor devices after a variation on the $\overrightarrow{\Delta Ploss}$, from one control period to the next. The decoupling vector is shown in 5.3, whereby $\overrightarrow{P_{Loss}}$ are the online losses of each die, $|Z_{th}|$ the steady-state thermal model and $|I_{24}|$ an identity matrix.

$$\overrightarrow{\Delta P_{cross}} = \overrightarrow{\Delta P_{act}} \cdot \overrightarrow{P_{Loss}} \cdot \frac{|Z_{th}|}{Z_{th-x,x}} - \overrightarrow{\Delta P_{act}} \cdot \overrightarrow{P_{Loss}} \cdot \frac{|Z_{th}|}{Z_{th-x,x}} \cdot |I_{24}| \tag{5.3}$$

Moreover, considering the FEM model, it is possible to obtain the power losses vector which is capable of balancing compensating the effects of thermal cross-coupling and insert it as a feed-forward action to the closed-loop control ($\overrightarrow{\Delta P_{ff}}$). Therefore, the compensator (|P|) becomes responsible for removing only additional temperature errors, caused by power deviation, uneven cooling, aging or parametric deviations. Consequently, the decoupled power $\overrightarrow{\Delta P_{dec}} = 0$ and the closed-loop control has no action to the system in case the $\overrightarrow{\Delta P_{ff}}$ is perfectly estimated. Finally, the $\overrightarrow{\Delta P_{ff}}$ is summed to the $\overrightarrow{\Delta P_{dec}}$, and the proportional power difference ($\overrightarrow{\Delta P_{act}}$) is delivered to the pulse processing block. As previously shown in Fig. 2.14, the thermal impedance of the dies can be fitted by a second order exponential function. Therefore, the proportional open and closed-loop control structures, can be represented by 5.4 and 5.5, respectively.

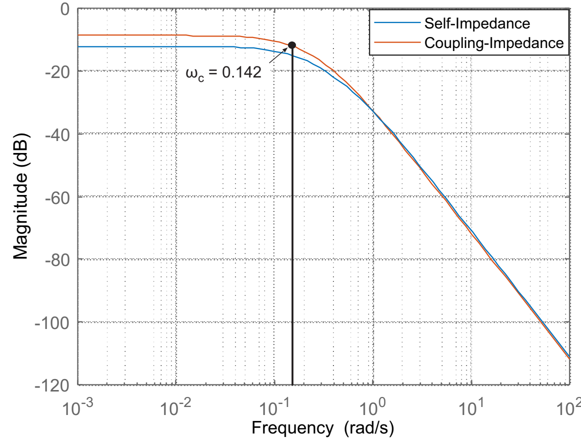


Figure 5.7: Frequency response for the equivalent thermal model.

$$\frac{T_j}{T^*_{j-avg}} = \frac{Kp \cdot K}{(T_1 s + 1)(T_2 s + 1)} \tag{5.4}$$

$$\frac{T_j}{T^*_{j-avg}} = \frac{Kp \cdot K}{(T_1 s + 1)(T_2 s + 1) + K_p \cdot K} \tag{5.5}$$

To obtain the controller proportional gain, a strategy based on dynamic stiffness is adopted. This concept is based on the system capability to reject a specific disturbance magnitude [196]. In other words, it measures the amount of disturbance magnitude necessary to generate a unit deviation on the system output [196]. As shown in Fig. 5.6, the dynamic stiffness of the presented control system is designed based on the effect of thermal cross-coupling power (ΔP_{cross}) variation on the junction temperature of a die (T_j). Therefore, the dynamic stiffness transfer function can be represented as in 5.6.

$$\left|\frac{P_{cross}}{T_j}\right| = \frac{(T_1 \cdot T_2) \cdot s^2 + (T_1 + T_2)s + 1 + (Kp \cdot K)}{K} \tag{5.6}$$

Considering the main goal is to regulate cross-coupling disturbances, the proportional controller is designed based on the cross-coupling impedance response. Fig. 5.7, shows the frequency response of one self (red) and the equivalent cross-coupling impedance of a middle device (blue). As it can be seen, the cross-coupling impedance cutoff frequency is $\omega_c = 0.142$. Therefore, the dynamic stiffness zeros - i.e. the con-

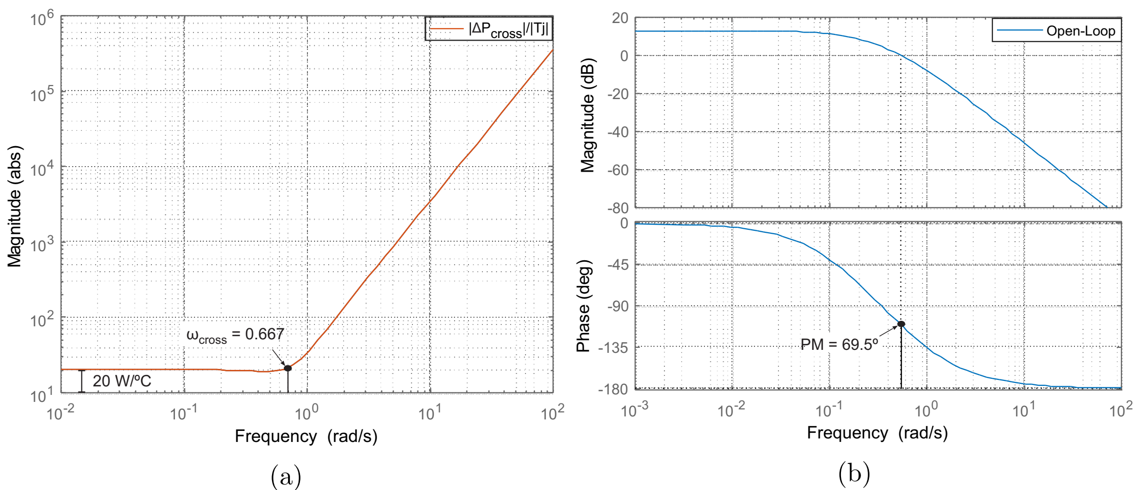
trol system poles - are allocated in order to obtain a response five times faster than the cross-coupling impedance $\omega_{cross} = 0.71$. Thereby, the proportional gain can be obtained as shown in 5.7.

$$K_p = \frac{(T_1 + T_2) \cdot \omega_{cross} - 1}{K} \tag{5.7}$$

Fig. 5.14 (a), shows the frequency response of the dynamic stiffness transfer function considering the calculated proportional gain and parameters shown in Tab. 5.1. As it can be seen, a ΔP_{cross} variation of $20\,W$ is required to generate a deviation of $1°\,C$, considering low frequency disturbances. Moreover, the dynamic stiffness increases for frequencies above ω_{cross}, whereby high frequency disturbances are rejected by system inertia. To demonstrate the control system stability, the the bode plot of the open-loop plant is obtained (Fig. 5.14 (b)), whereby a phase margin of 69.5° is observed.

Table 5.1: Die-Level proportional control parameters.

T_1	1.406
T_2	6.155
K	0.2475
K_p	17.64



(a) (b)

Figure 5.8: Frequency response for the proportional die-level thermal control system (a) Dynamic stiffness (b) Magnitude gain and phase marging of the open-loop control system.

As a second dynamic stiffness criteria, it is desired a maximum tolerance of 10% of maximum power deviation per degree. Therefore, considering the presented 24-dies MCM the minimum low frequency dynamic stiffness is calculated by the equivalent cross-coupling thermal disturbances on a specific die (T_x), as shown in 5.8. For the pulse-shadowing process, the power loss $P_{Loss(Tx)}$ is calculated considering a shadowing in one SW under nominal load - i.e. only twelve IGBTs carrying the nominal current. Thereby, considering the devices with higher cross-coupling effects (SW1) $R_{th(Tx-n)} = 0.69\,K/W$, $R_{th(Tx,x)} = 0.30\,K/W$ and a pulse-shadowed power of $145.48\,W$, the minimum dynamic stiffness results in $18.79\,W/K$. Consequently, considering the obtained dynamic stiffness shown in Fig. 5.14 (a), the system is capable of keeping thermal deviatios below $1°C$ considering disturbances variation (ΔP_{cross}) of up to 10%.

$$\left|\frac{\Delta P_{cross}}{T_j}\right| > P_{Loss(Tx)} \cdot \frac{R_{th(T1-n)} - R_{th(Tx,x)}}{R_{th(Tx,x)}} \cdot \frac{1}{10} \tag{5.8}$$

For the pulse-shadowing implementation, a range of ten periods is selected to manipulate the mean power losses. Thereby, the temperature of the devices are sensed and the number of shadowed pulses are selected based on the mean power losses on every ten switching periods. As a result, the hotter dies remain off for more periods, thereby directing a portion of the mean losses to the colder ones. To validate the control system, the FEM-based electrothermal simulation system previously described in Sec. 2.3.2 with respective parameters, is adopted. Since the FEM model is symmetric, only one device per switching group - SW and DG - is simulated for this transient analysis to reduce the computational effort. At the beginning of the thermal simulation, the MCM operates with a thermal deviations of up to $17.2\,°C$, as shown in Fig. 5.9. The pulse-shadowing based thermal balancing is triggered at $t = 20\,s$, the temperatures are balanced - with a small temperature difference - and the highest temperature is reduced by $6.8\,°C$.

To validate the dynamic stiffness, the system is simulated again considering a

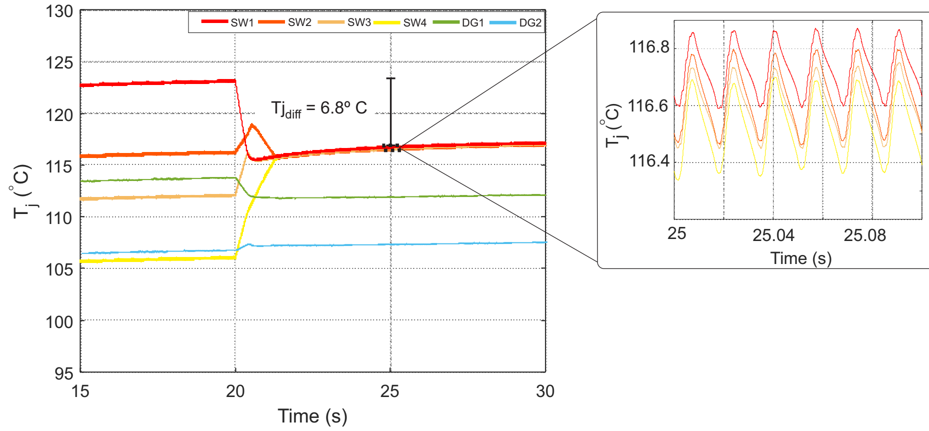


Figure 5.9: Transient thermal results of the pulse-shadowing strategy, showing the junction temperature of one die per switching group. The thermal balancing is triggered at $t = 20\,s$, and the temperatures are balanced.

thermal resistance of one device of group SW1 10% higher than the estimated value. As shown in Fig. 5.10, the thermal balancing is activated at $t = 20\,s$, and the temperatures still balanced with thermal deviations below $1°C$. Moreover, a thermal reduction of $11\,°C$ can be observed, due to the higher thermal deviation caused by the different thermal resistance.

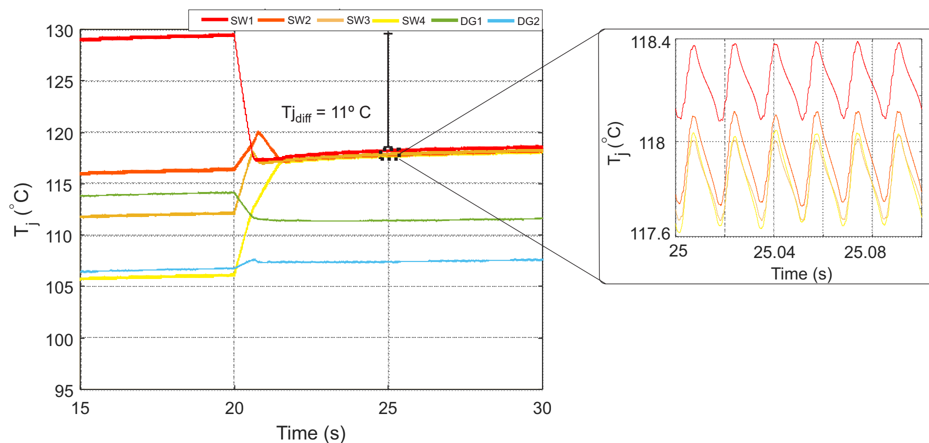


Figure 5.10: Transient thermal results of the pulse-shadowing strategy considering 10% of variation on the R_{th} of SW1, showing the junction temperature of one die per switching group. The thermal balancing is triggered at $t = 20\,s$, and the temperatures are balanced, with deviations below $1°C$.

On-Off Control

Although the proportional controller has several advantages, a parametric evaluation of the thermal network is required. Alternatively, an on-off control structure can

be adopted, whereby the temperature of the devices are manipulated on each switching periods. In this approach, the temperatures are used as a feedback and compared through logic elements. For the pulse-shadowing approach, the temperature of each switching group (T_{j-SWx}) is sensed and compared the all others ($T_{j-SW-All}$), and the SW with highest temperature has its PWM signal blocked ($Lock_{SWx}$), as shown in 5.11. Since only logic elements are used and no control tuning is required, this strategy does not require the thermal network parameters, and it can be directly applied to any multi-gate multichip structure.

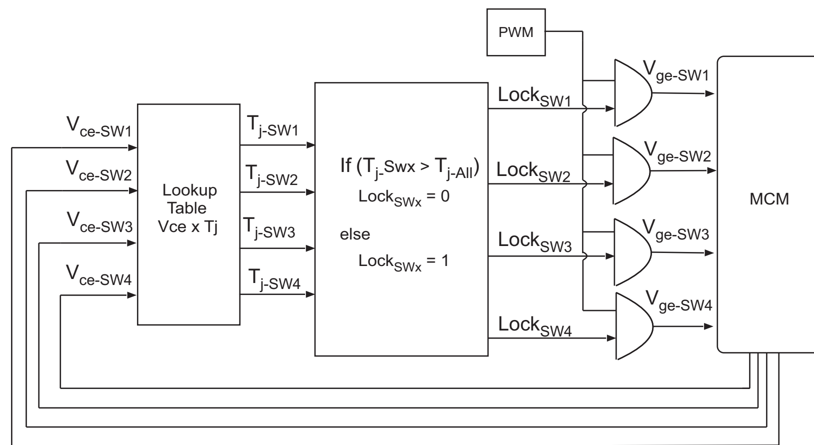


Figure 5.11: Control diagram of the on-off based die-level thermal control strategy.

The on-off control strategy is also validated on the FEM-based electrothermal simulation system. A shown in Fig. 5.12, the pulse-shadowing based thermal balancing

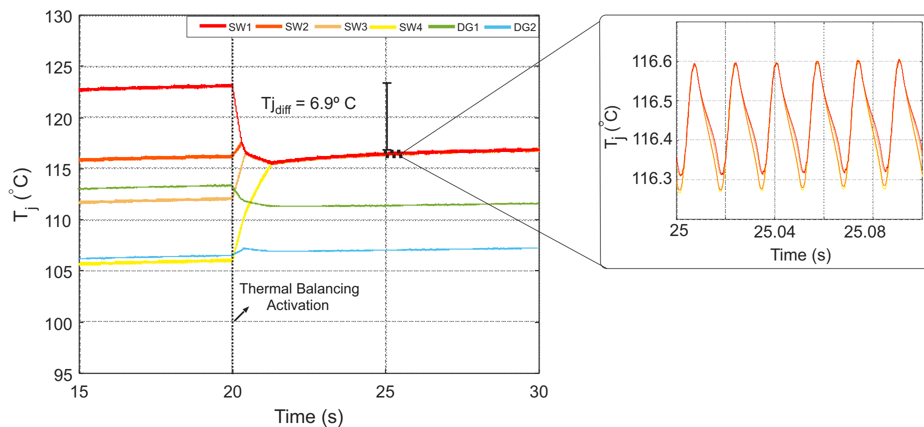


Figure 5.12: Transient thermal results of the on-off control with pulse-shadowing strategy, showing the junction temperature of one die per switching group. The thermal balancing is triggered at $t = 20\,s$, and the temperatures are perfectly balanced.

is triggered at $t = 20\,s$, the temperatures are balanced and the highest temperature is reduced by $6.9\,°C$. Looking at the zoom of the balanced temperatures, it can be seen that the steady-state error is even lower compared to the proportional controller, shown in Fig. 5.9.

Experimental Validation

For the experimental validation, the on-off control strategy is implemented on the evaluation system with three-devices with independent gate-commands described in the end of this chapter - Sec. 5.8.1. The electrical results of the on-off pulse-shadowing strategy, with gate commands (S_x), IGBT/diode current (I_{s1}), output voltage (V_{out}) and current (I_{out}) is shown in Fig. 5.13. For the thermal balancing validation, two thermal images are collected, one without thermal balancing strategy and other with pulse-shadowing. As shown in Fig. 5.14 (a), there is a maximum thermal deviation of $6.43\,°C$, and the temperatures are balanced resulting in a temperature reduction of $0.43\,°C$, as displayed in Fig. 5.14 (b).

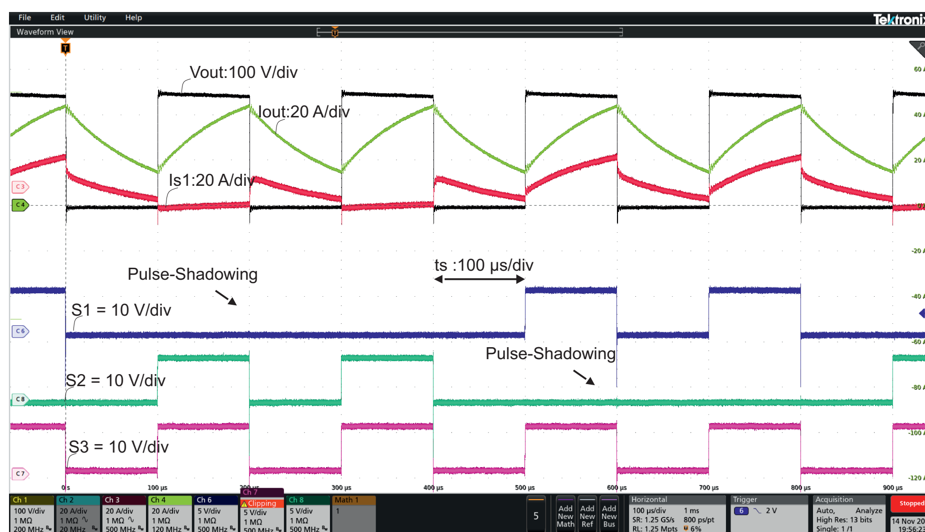
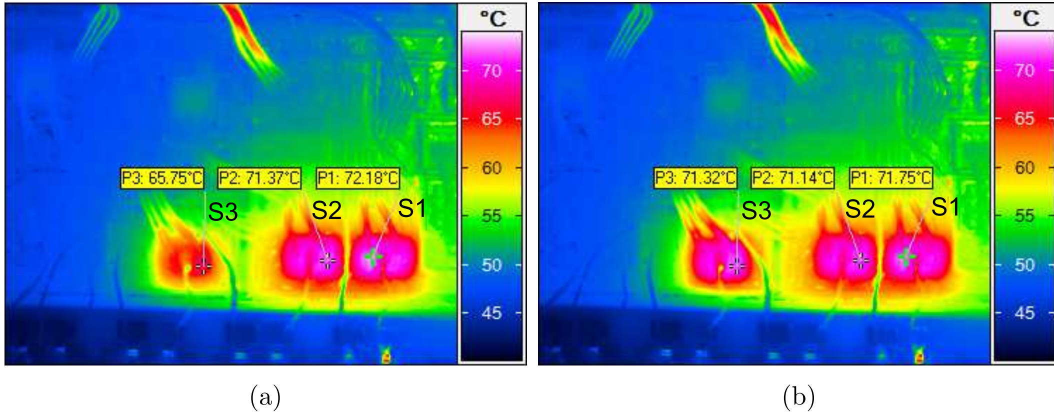


Figure 5.13: Electrical results of the pulse-shadowing strategy, showing the gate commands (S_x), one IGBT/diode current (I_{s1}), output voltage (V_{out}) and current (I_{out})



(a) (b)

Figure 5.14: Steady-state thermal analysis of the pulse-shadowing strategy: (a) Without balancing. (b) With balancing.

5.3.2 Turn-off Losses Manipulation for Thermal Balancing

Alternatively to the complete pulse shadowing, the turn-off losses of the devices can be separately manipulated to obtain thermal balancing. Moreover, the turn-off manipulation has a potential to reduce the total losses of power devices due to the direct relation between I_c and t_{off}. Therefore, this work proposes and investigates the turn-off loses based thermal balancing for multichip modules. A physics-based analysis of the method and its thermal validation are conducted in sequence.

IGBT Turn-off - A Physics-Based Analysis

The turn-off process of an IGBT is defined by the sweep away of remaining charges from the conduction period. As shown in Fig. 5.15, the first turn-off stage is defined by the time between the turn-off command and the gate-voltage reaching the miller plateau (V_{gp}). In this stage, the voltage decay is defined by the gate (C_{gc}) and oxide (C_{ox}) capacitances, which are constant during the process. However, the difference between V_{ge} and V_{gp} is proportional to the I_c. Therefore, higher collector current shorts the duration of the first stage, as shown in 5.9 [143].

$$t_1 = R_g(C_{ge} + C_{gc})ln\left(\frac{V_{gg(on)} - V_{gg(off)}}{(V_{th} + \frac{I_c}{g_m}) - V_{gg(off)}}\right) \tag{5.9}$$

During the second stage, the charges are extracted from the N^- drift region to

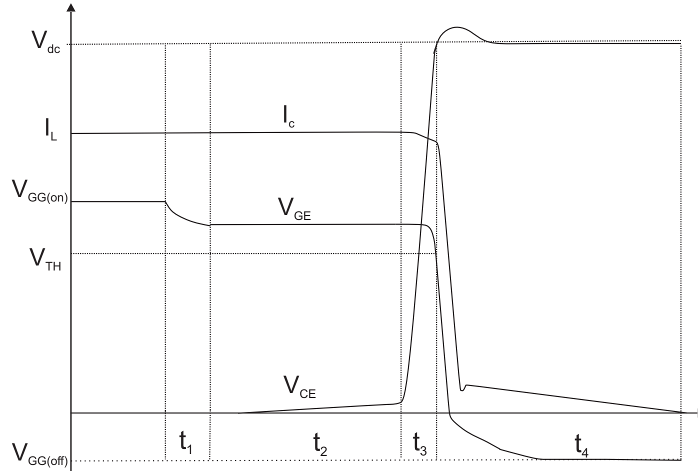


Figure 5.15: Turn-off process of an IGBT under inductive load.

maintain a constant I_c and compensate the decreasing of the MOS channel electron current. As a result, the charges in the accumulation layer under the gate region - shown in Fig. 5.16 - are swept out; the depletion region starts to widen and V_{on} rises slowly [144]. The evolution of the depletion layer located under the gate region (W_{cd}) is proportional to the MOS current decrease (ΔI_{ch}), and ultimately related to the collector-current, defines the duration of this stage (t_2) [143]. Therefore, I_c impacts the evolution of the depletion layer and is inversely proportional to the duration time of the second stage (t_2), as shown in 5.10.

$$t_2 = \frac{L_M \cdot q \cdot \eta_{ac}}{2 \cdot \Delta V_{ge} \cdot \sqrt{(1 - \alpha_{pnp}) \cdot K_c \cdot I_c}} \tag{5.10}$$

where ΔVge is the gate-emitter voltage, L_M the length of the depletion region, q the unit charge and η_{ac} the carrier distribution. η_{ac} is the carrier distribution,ΔVge the variation of gate-emitter voltage, q the unit charge, α_{pnp} the current gain and K_c an electron mobility coefficient [143].

The third stage starts when the accumulation layer disappear from the gate region, the miller capacitance decrease suddenly and the evolution of the space-charge layer (W_n) conducts the voltage rising [144]. In this step, the concentration of the drift region, which is related to the collector current, dictates the evolution of W_n. Therefore, I_c also affects the third stage, as shown in 5.11 [47].

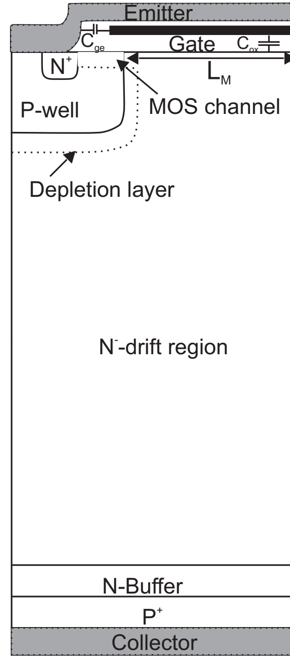


Figure 5.16: Physical structure of an IGBT.

$$t_3 = \frac{\varepsilon_S \cdot \eta_{wnb^+} \cdot V_{dc} \cdot A_c}{W_n \cdot (N_D + \eta_{sc}) \cdot I_c} \tag{5.11}$$

Thereby, N_D and W_n are the doping concentration and width of the of N^- drift region, respectively. η_{sc} the hole concentration in the space-charge region and η^+_{wnb} the drift region interfacing the N-buffer layer. ε_S is the Boltzmann constant, I_c the on-state current, A_c the active IGBT area and V_{dc} the total dc-bus voltage. The t_3, is also dependent on the collector current through η_{sc}, which in turn increase the hole concentration in the depletion layer. As a result, high I_c accelerate its evolution and, consequently, reduces t_3.

The collector current decay is the process of the fourth stage, which starts after the voltage rising. The space-charge layer, in most cases, extend trough the entire N-base, whereby the recombination of trapped holes on the N-buffer layer conduct this process. Therefore, the I_c decay and the current falling time, depends only to the buffer layer lifetime ($\tau_{p0,NB}$), as modeled in 5.12 [47].

$$t_4 = \tau_{p0,NB} \cdot ln(10) \tag{5.12}$$

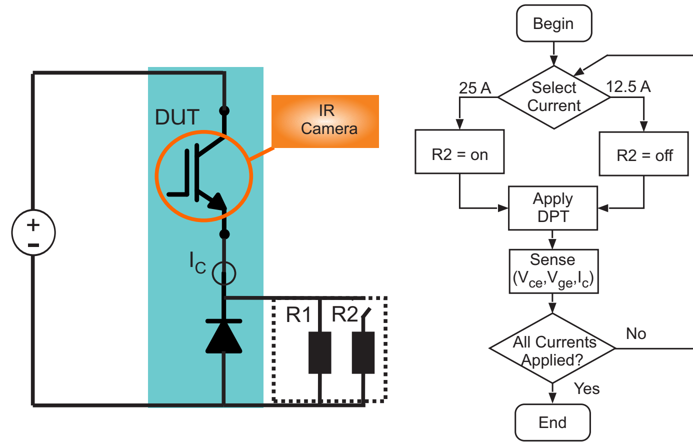


Figure 5.17: Schematic and flowchart of the two double pulse tests applied to the DUT to demonstrate the effects of I_c - 1 and 0.5 pu - on the turn-off time of IGBTs.

Notably, the collector current influences the first three turn-off stages, whereby higher I_cs results in lower turn-off times (t_{off}) in all steps. Indeed, variations on the dV/dt during the third stage of around $20\,V/\mu s/A$ in $1.7\,kV/50\,A$ devices, has been demonstrated in reference [144]. Reduction of $1\mu s$ is furthermore demonstrated with with 25% of current increase in medium-voltage high-current devices ($3.3\,kV/1500\,A$) [143].

Therefore, to validate the aforementioned physics behavior, a double-pulse test - removing the effects of temperature - is realized in a $1.2\,kV/25\,A$ device (DP25F1200T). In this experiment, the nominal and half currents are applied, as shown the diagram and schematic of Fig. 5.17. As a result, the t_{off} of the second and third stage are reduced by $41\,ns$ in full load, as shown in Fig. 5.18 (a).

Losses Analysis

The energy (E_{off}) dissipated during the turn-off is related to its duration, whereby short t_{off} results in lower losses, as deduced in 5.13. As detailed above, the I_c is proportional to the turn-off time, and comparing the turn-off losses of one device conducting the same current with two in parallel - supposing the same temperature -, the single one is more efficient. In other words, the turn-off losses of one device under nominal load is lower than two devices with half load each. To illustrate it in a

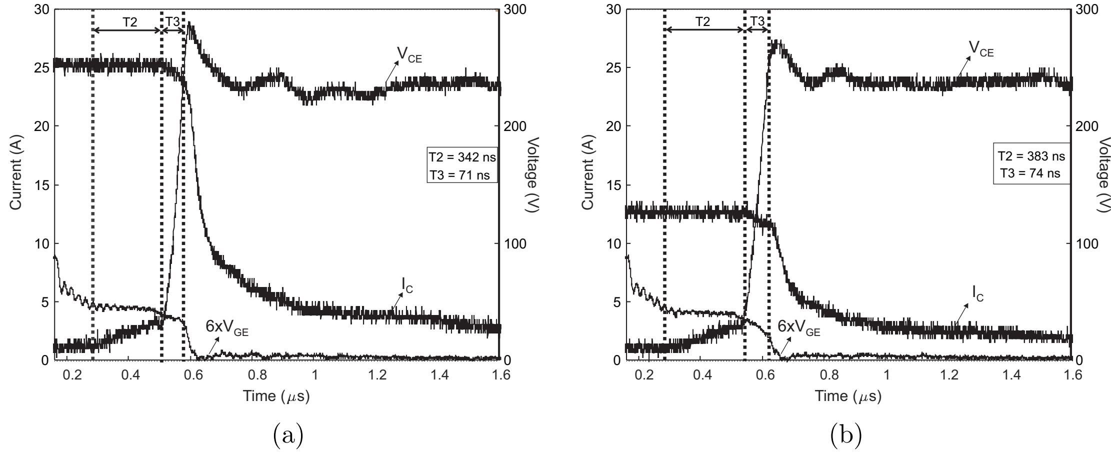


Figure 5.18: Experimental results for the turn-off of an $1.2\,kV/\,25\,A$ IGBT for different currents. (a) $25\,A$ (b) $12.5\,A$.

practical scenario, the turn-off energy of multiple devices from different manufacturers is summarized in Tab. 5.2. As expected, the E_{off} of one device with total current (1 -E_{off}) is , in general, lower than the energy of two devices with half current (2 -E_{off}).

$$E_{off} = \int_0^{t_{off}} V_{ce}(t) \cdot I_c(t) dt \tag{5.13}$$

Table 5.2: E_{off} comparison of multiple devices considering a single device with 1 pu of current and two with 0.5 pu each.

Device	Technology	Characteristics	1 -E_{off}	2 - E_{off}
IKW40N120C6S (Inf)	Trenchstop 6	1200 V/40 A	2.9 mJ	3.33 mJ
IKFW50N65DH5 (Inf)	Trenchstop 5	650 V/50 A	3.67 mJ	4.20 mJ
FD100R12W2T7 (Inf)	IGBT 7 - T7	1200 V/100 A	10.02 mJ	11.30 mJ
IRG7PH35UD (IR)	Generation 7	1200 V/20 A	1.16 mJ	1.42 mJ
5SNG 0150Q170300 (ABB)	62Pak	1200 V/150 A	35.83 mJ	41.22 mJ
SK100GH12T4T (Sem)	4-Trench	1200 V/100 A	10.13 mJ	11.36 mJ
SKM75GB12V (Sem)	V-IGBT	1200 V/75 A	7.1 mJ	8.2 mJ

Turn-off Losses Manipulation

The turn-off losses manipulation strategy is based on turning-off the hotter device - or SW - before in soft-switching, as shown in Fig. 5.19. Thereby, the E_{off} of the hotter dies are reduced and the current is redistributed among the colder ones for its turn-off process. Consequently, the remaining devices turn-off under higher current, thereby

balancing the temperatures and reducing the overall losses due to the shorter turn-off time. Fig. 5.20, shows the adopted on-off control structure considering the turn-off losses manipulation for the multi-gate MCM. As it can be seen, the junction temperatures are sensed, compared, and the equivalent switch with highest temperature has its duty (T_{duty}) reduced by a specific time ($t_{off-red}$). Thereby, this device is turned-off in soft-switching to reduce its E_{off}. To manipulate only the turn-off losses without affecting the conduction one, the $t_{off-red}$ is calculated online to ensure a thermal balancing on its lowest possible value. As shown in Fig. 5.20, the $t_{off-red}$ starts with an initial value, the temperatures with highest difference are compared and $t_{off-red}$ is decremented by a specific step. Thereby, the optimum turn-off reduction value is obtained automatically, when a minimum value that ensures balancing is reached.

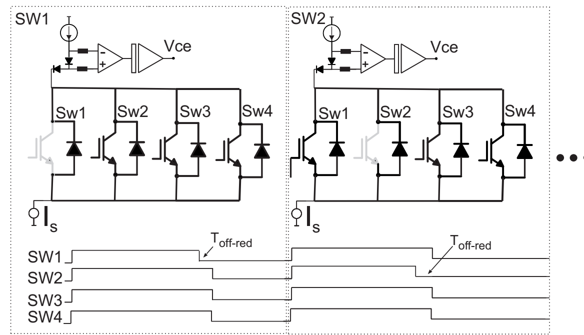


Figure 5.19: Pulse pattern of the turn-off losses manipulation strategy, whereby the hottest device - or SW - has its duty time reduced and turned-off before the others, in soft-switching.

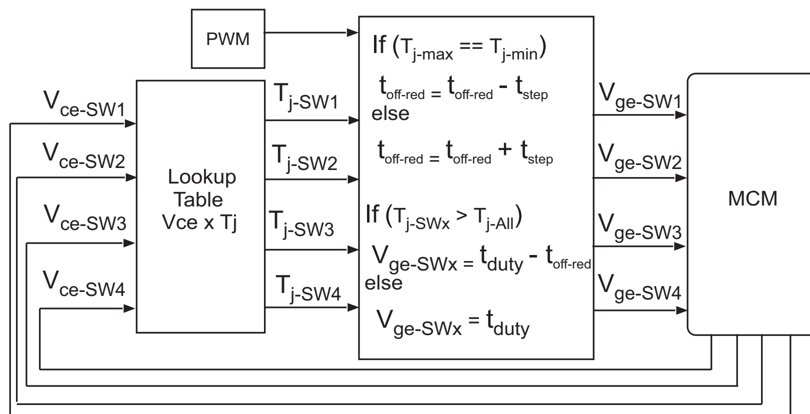


Figure 5.20: Implementation schematic of the on-off control based on turn-off losses manipulation for thermal balancing, with online $t_{off-red}$ calculation.

Thermal Analysis

The validation of the proposed turn-off losses manipulation, with its additional capability to slightly reduce the switching losses, is firstly validated by using the previously presented FEM-based simulation process. As shown in Fig. 5.21, the temperatures are equalized when the thermal balancing strategy is activated at $t = 20\,s$. Moreover, there is a total thermal reduction of $8.7\,°C$ when the $t_{off-red}$ is shortened to its minimum possible level, thereby slightly reducing the MCM overall losses.

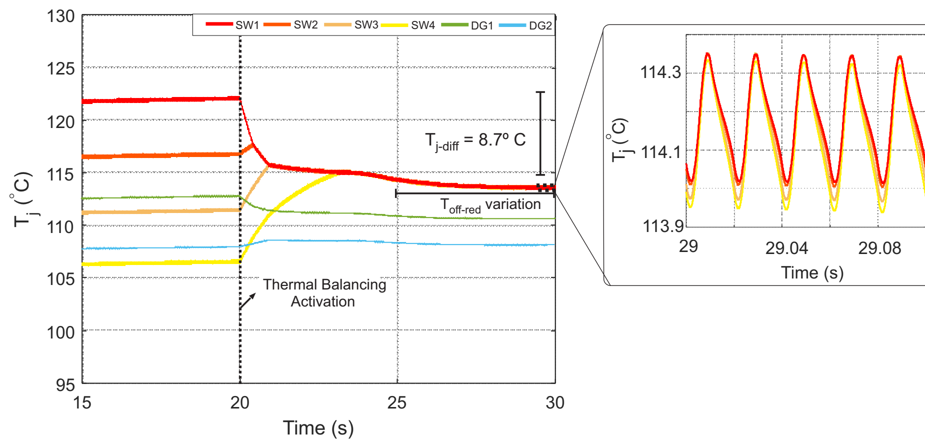


Figure 5.21: Transient thermal results of the on-off control with pulse-shadowing strategy, showing the junction temperature of one die per switching group. The thermal balancing is triggered at $t = 20\,s$, and the temperatures are perfectly balanced.

Experimental Validation

The turn-off losses manipulation is also applied in the validation system described in Sec. 5.8.1. Fig. 5.22, shows the electrical results, whereby the device current increases by 33% at the of the period, when another device is switched-off before a calculated turn-off time. The thermal validation is shown in Fig. 5.23, whereby the temperatures are balanced by manipulating the turn-off losses with a reduction of $2.2\,°C$ in the hottest device.

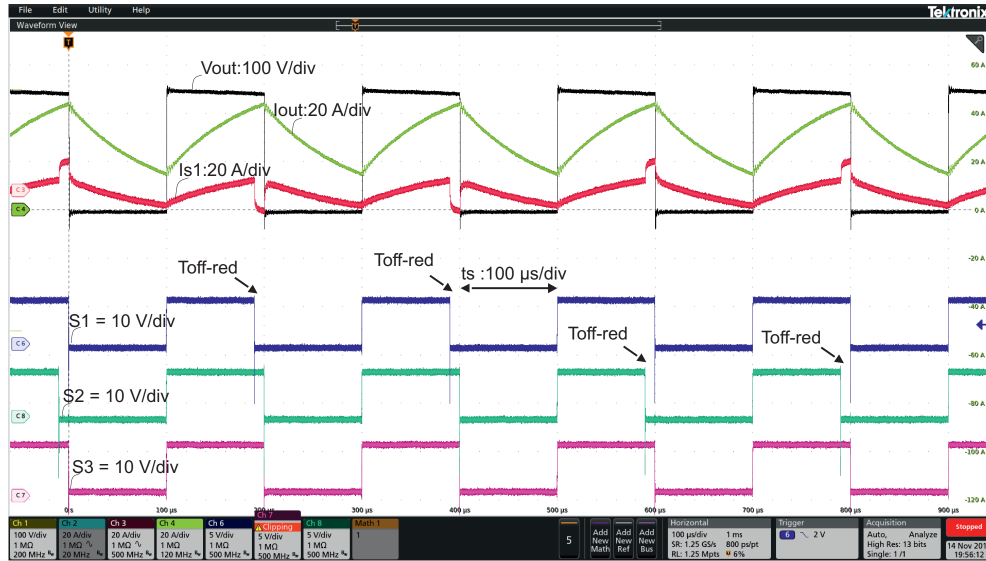
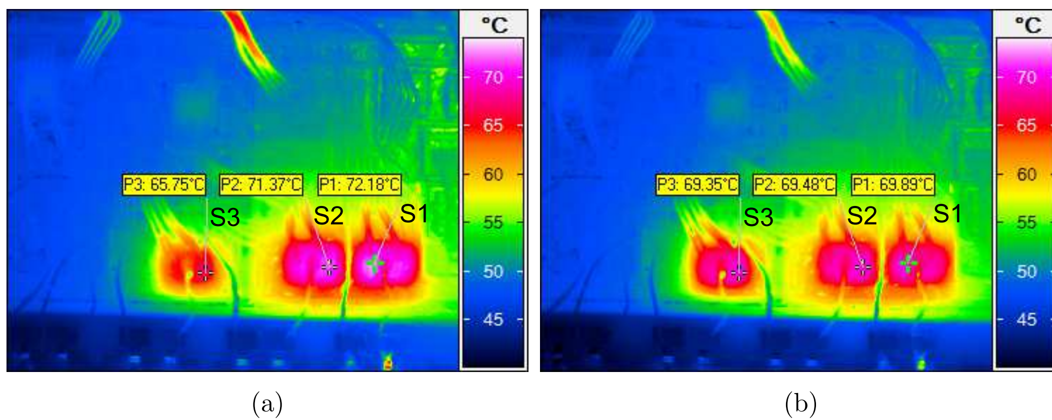


Figure 5.22: Electrical results of the turn-off losses manipulation, showing the gate commands (S_x), one IGBT/diode current (I_{s1}), output voltage (V_{out}) and current (I_{out})



(a) (b)

Figure 5.23: Steady-state thermal analysis of the turn-off losses manipulation strategy: (a) Without balancing. (b) With Balancing.

5.3.3 Comparison of the Thermal Balancing Solutions

For a better visualization of the thermal distributions considering the impact of the presented strategies on the temperature of all 24-dies, the obtained losses are loaded on the finite elements software. Moreover, the turn-on losses manipulation proposed by different authors, is also implemented for sake of comparison [28, 39, 195]. In this strategy, a group of parallel devices are turned-on displaced in time to manipulate its turn-on switching energy (E_{on}). As a result, the temperature among the devices are balanced by alternating the turn-on sequence over time. As shown in Fig. 5.24 (a), without any strategy there is a critical uneven thermal distribution among the

dies, whereby the MCM operates with a maximum deviation of 16.5 °C. As shown in Fig. 5.24 (a), the temperature in the hottest die is reduced from 123.0 °C to 116.7 °C, when the pulse-shadowing strategy is applied. The results of the turn-on and turn-off losses manipulation are shown in Figs. 5.24 (c) and 5.24 (d), whereby the maximum temperatures are even reduced achieving maximum of 115.5 °C and 114.5 °C, respectively. The cross-coupling effects are also displayed in the FEM analysis, whereby a reduced impact in the middle dies with thermal balancing, is observed. Consequently, the temperature of the diodes (D_x) are reduced in up to 2.1 °C, 3.0 °C and 3.3 °C, for the pulse-shadowing , turn-on losses and turn-off losses manipulation, respectively. The comparative analysis, with the thermal deviation (T_{j-dev}), maximum temperature

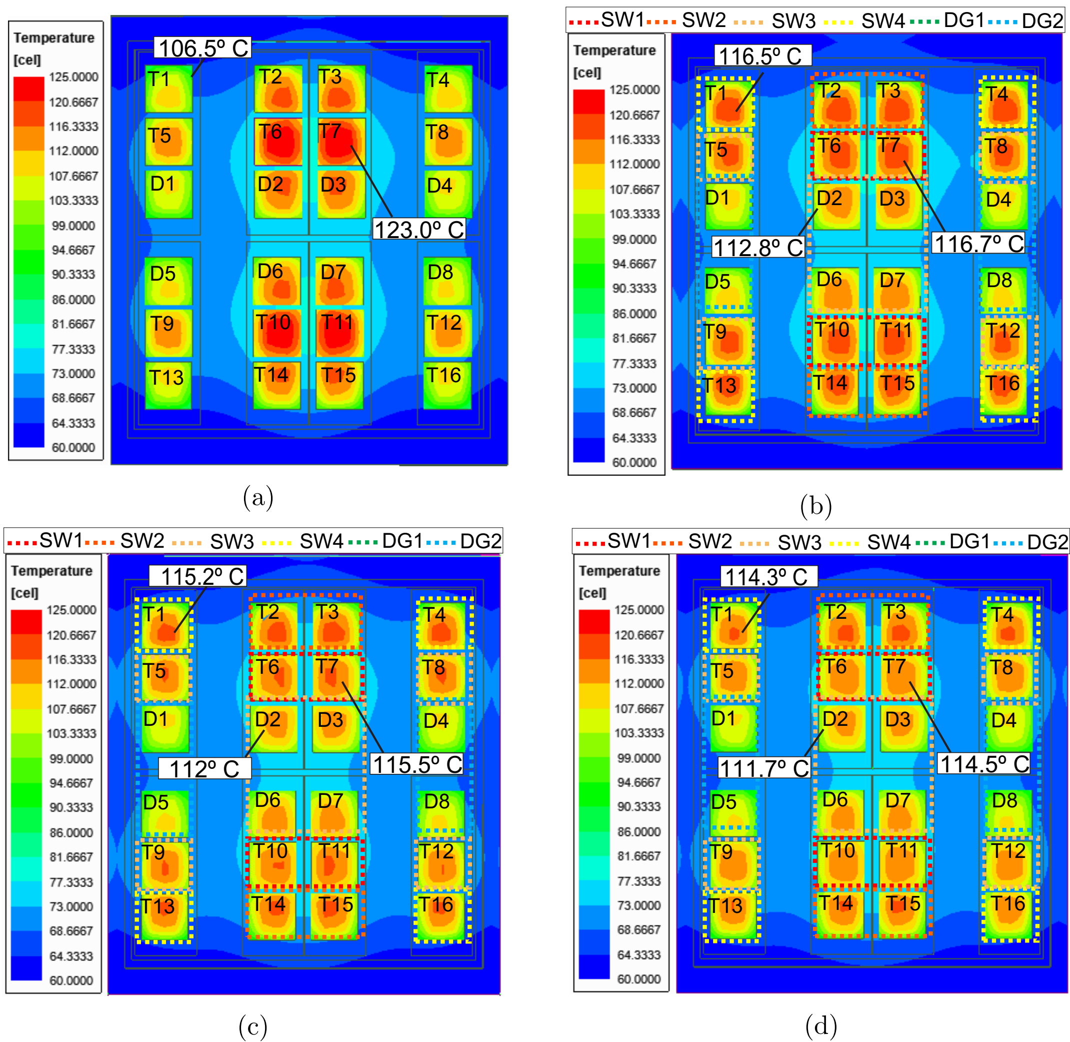


Figure 5.24: Finite element analysis comparison for the presented thermal balancing strategies: (a) Without Balancing (b) Pulse-Shadowing (c) Turn-on Losses (d) Turn-off Losses.

(T_{j-max}) and obtained reduction on the transistors ($T_{j-Red-T}$) and diodes ($T_{j-Red-D}$), are summarized in Tab. 5.3.

Table 5.3: Comparative analysis for the presented thermal strategies, showing the highest thermal deviation and temperature among the dies.

Strategy	T_{j-max}	$T_{j-Red-T}$	$T_{j-Red-D}$
None	$123\,°C$	-	-
Pulse-Shadowing	$116.7\,°C$	$6.3\,°C$	$2.2\,°C$
Turn-on	$115.5\,°C$	$7.5\,°C$	$3\,°C$
Turn-off	$114.5\,°C$	$8.5\,°C$	$3.3\,°C$

Experimental Efficiency Analysis

To validate the impact on losses of the presented thermal balancing strategies, their efficiencies are measured for different power levels. For that, a power analyzer is connected in the input and output of the buck converter, the power is varied through the resistors, the thermal balancing strategy is triggered in the software, and the efficiency is calculated through the measured input and output power. The obtained results are shown in Tab. 5.4, whereby the losses differences are very small with a slightly higher efficiency for the turn-off losses manipulation in all operating points.

Table 5.4: Efficiency comparison for the MCM operating with 0.33 pu, 0.66 pu and 1 pu of power, considering four operating conditions: without thermal balancing, pulse-shadowing, turn-on losses and turn-off losses manipulation.

Strategy	0.33 pu	0.66 pu	1 pu
None	76.126 %	86.638 %	90.172 %
Pulse-Shadowing	76.013 %	86.557 %	90.048 %
Turn-on	76.124 %	86.621 %	90.165 %
Turn-off	76.128 %	86.647 %	90.184 %

5.4 Indirect Thermal Balancing for Diodes

The thermal balancing strategies has been demonstrated the effectiveness to overcome temperature and degradation of active switches inside MCMs. Nevertheless, the diodes are passive devices and the losses manipulation among them is not possible. Looking at Fig. 5.24, it can be noticed that the diodes are in the middle of the MCM, thereby suffering high thermal cross-coupling influences. As a result, high thermal deviations and high temperature - especially in case of the extreme middle ones: D2, D3, D6 and D7 - can be observed. The thermal deviation among diodes is even worst, because it has positive on-resistance coefficient, whereby the temperature mismatches result in higher current deviations and, consequently, a cascaded effect.

The diode thermal stress, however, is not critical in most applications, whereby a positive power factor results in considerably higher thermal stress on the IGBTs. Nevertheless, in specific applications, such as active front end (AFE) [197] and reactive power processing [198], the negative power factor results in higher stress on the diodes. Therefore, the thermal mismatch and extra heating due to cross-coupling effects can result in high thermal stress on the diodes, which counts with a reduced number of dies and higher thermal resistance [198]. Hence, an alternative strategy to reduce the thermal stress and ensure high reliability in such applications has high relevance.

Although the hotter diodes are not controllable, there is a possibility to act on the active devices of their neighborhood, to enhance the thermal spread in the middle of the MCM. Therefore, this work proposes an indirect thermal balancing for MCM diodes in applications where the diodes suffer from higher thermal stresses. The main focus is to reduce the thermal cross-coupling effects on the diodes, by manipulating the losses of the IGBTs close to them. As can be seen in Fig. 5.24, the immediate neighbors of the middle diodes - T2, T7, T10 and T11, are grouped in the same equivalent switch (SW1). Therefore, it is possible to reduce the temperature of the diodes by manipulating the losses of SW1. Considering the pulse-shadowing strategy, the pulses of SW1 is shadowed until the temperature of the others IGBTs reach the

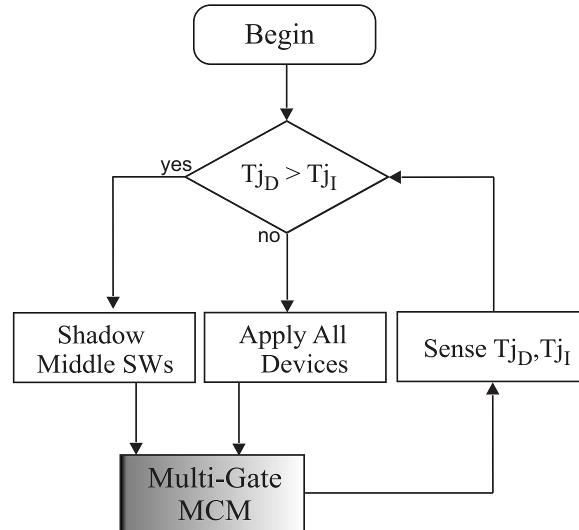


Figure 5.25: Flowchart of the thermal stress reduction in MCM diodes by acting on the thermal spread.

T_j of the diodes, as shown in the flowchart Fig. 5.25.

Thermal Analysis

The thermal balancing for MCMs in reverse power flow applications is validated considering the same parameters of the previous analysis, yet with a power factor of $cos(\phi) = -1$. In this strategy, the middle dies (SW1) and diodes are sensed and compared; if SW1 is hotter than the diodes, its pulse is shadowed in the next period. As shown in Fig. 5.26 (a), the diodes located in the middle of the MCM have the highest thermal stress, operating under $124\,°C$ in ordinary conditions. Nevertheless, with the thermal balancing, the thermal stress of the middle IGBTs - SW1 - is directed to the edge ones - SW2, SW3 and SW4 -, thereby reducing its temperature and changing the thermal spread on the MCM, as clearly shown in Fig. 5.24 (b). Therefore, the thermal cross-coupling in the middle dies - DG1 - is drastically reduced, thereby lowering their temperatures in up to $9.9\,°C$, as also displayed in Fig. 5.24 (b).

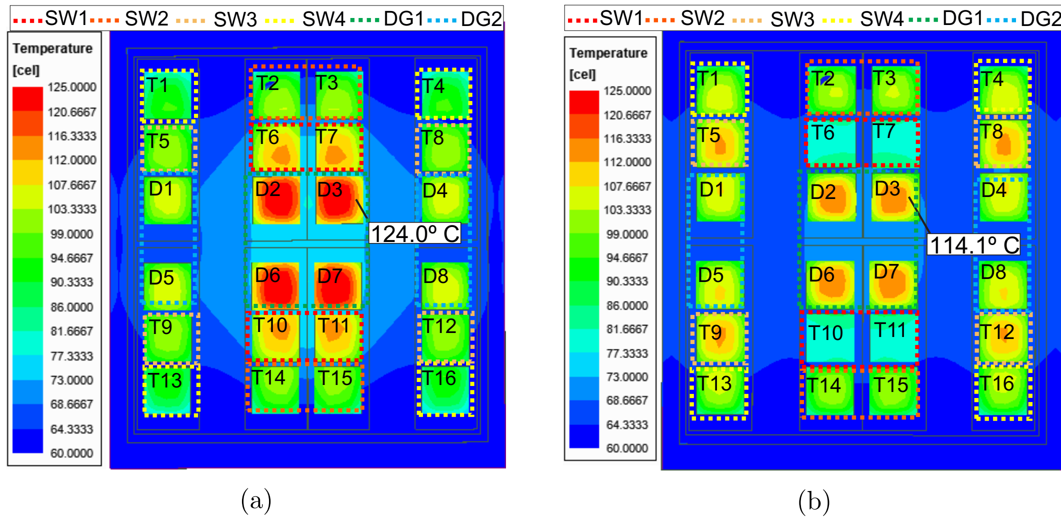


Figure 5.26: Finite element analysis of the thermal balancing for MCMs in reverse power flow applications: (a) Without thermal balancing (b) With thermal balancing.

5.5 Selective T_j Sensing and the Pre-Programmed Thermal Balancing

Considering V_{on} as a TSEP for die-level thermal balancing strategies, the single collector-emitter connection challenges the sensing of the specific devices inside the parallel group. By sensing V_{ce} of all dies at the same time, only a mean temperature is obtained thereby hiding the die-level temperatures. Therefore, it is possible to apply a selective T_j sensing, whereby the V_{ce} of each device - or SW - is sensed at time only under the currents below its limit. Therefore, this strategy can be applied in partial load conditions or with the current crossing lower level - as discussed in section 4.4.6. Considering the presented 24-dies module, for example, the sensing process can be applied in its four groups with currents up to 400 A. Since this work is focused on the reliability of power devices, which is more critical in load cycling applications, as well detailed in Chap. 3, the sensing process can be safely applied in many steps of the mission profile. Therefore, a pre-programmed thermal balancing strategy is proposed, whereby the T_js are sensed only at low load through a V_{on} sensing circuit. In this strategy the close-loop thermal balancing is applied only under low load conditions, and the obtained pulse-pattern is replicated in other operating points, as shown in

the flowchart of Fig. 5.27. As a result, the temperature per device - or SW - can be safely sensed with required precision, and the temperatures balanced in the entire load range, due to the relation between losses and thermal deviation.

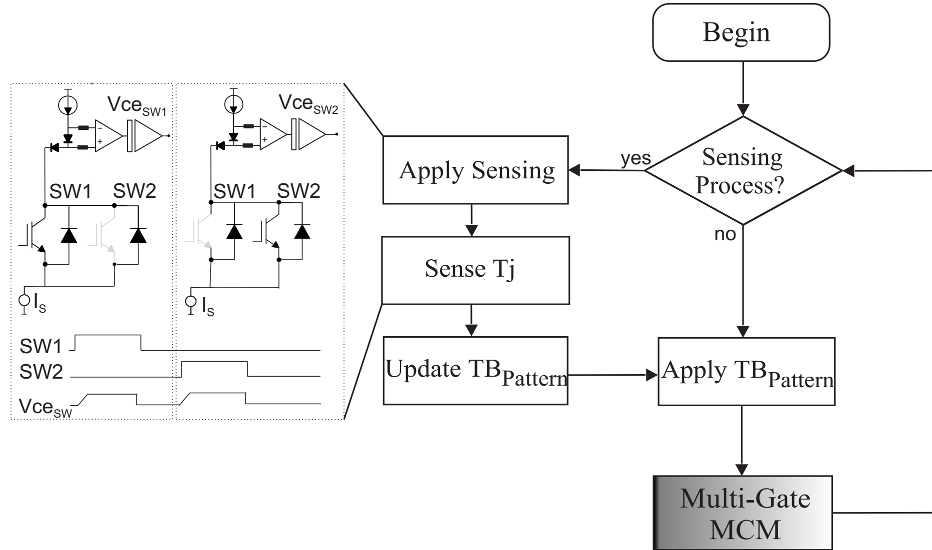


Figure 5.27: Flowchart of the pre-programmed thermal balancing for load cycling applications, with selective T_j sensing process under reduced load.

Experimental Validation

The pre-programmed thermal balancing is also validated in the experimental setup (Fig. 5.33), by applying the turn-off losses manipulation strategy with the implementation process shown in Fig. 5.27. As shown in Fig. 5.28 (a), the system starts operating without thermal balancing and with $0.33\,pu$ of power - $15\,A$ peak. At $t = 30\,s$ the thermal balancing is triggered, and the die-level V_{ce} sensing strategy is activated. The temperature of each device is sensed at a time, and the pulse pattern is updated until the temperatures are balanced, as shown in Fig. 5.28 (a). In this experiment, a sensing process is applied after each ten soft-switching periods. Thereafter, a step current is applied at $t = 60\,s$ by switching-on the dc breaker and adding one more resistor in parallel, making the system to operate with $0.66\,pu$ of power. In this stage, the die-level V_{ce} sensing is deactivated, and the pulse-pattern responsible for balancing the temperature under $0.33\,pu$ of load is replicated. In sequence, another resistor is added to the parallel group with a second dc breaker - $t = 60\,s$ -, and the system

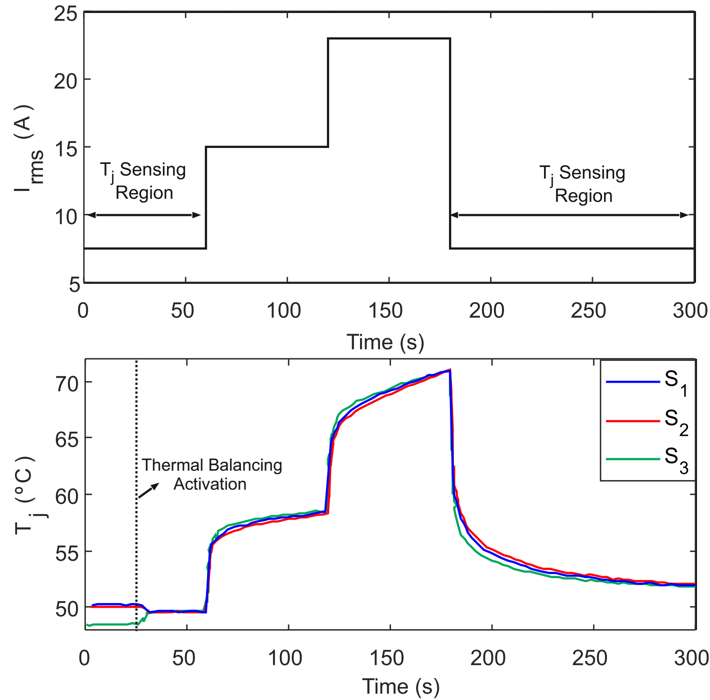


Figure 5.28: Validation of the die-level V_{ce} sensing, pre-programmed thermal balancing and transient performance of the turn-off losses manipulation strategy. The pulse pattern is defined with $7.5\,A$ by sensing the T_j, and it is repeated for $15\,A$ and $23\,A$ keeping the temperatures balanced during the whole power cycling. (a) Current profile. (b) Junction temperature of each device.

starts to operate with $1\,pu$ of power for a specific time. Finally, the two resistors are removed by switching-off the dc breakers at the same time, taking the system again to $0.33\,pu$ of power. As shown in Fig. 5.28 (b), the temperatures are balanced in the whole cycling process, with the same pulse pattern pre-programmed at low load condition.

5.6 Reliability and Efficiency Analysis of the Die-Level Thermal Balancing in MCIA

To evaluate the performance the pre-programmed die-level thermal balancing and its impact on mission critical application, a reliability and efficiency analysis of the presented strategies is conducted. In this study, the mine hoist system presented in Sec. 3.4 is adopted. In this application, the skip is accelerated until the nominal

speed, and is braked when approaching the final destination - the top or bottom of the mine. Therefore, the converter experience direct power flow during acceleration and a reverse power flow during the regenerative breaking process. Thereby, the thermal balancing strategies are switched to reduce the thermal stress on the IGBTs or diodes depending on the current direction, as highlighted in 5.29 (a). In the figure, the junction temperature sensing region of the aforementioned pre-programmed strategy can be also observed, whereby the sensing per group can be applied in up to 800 A due to the adoption of two parallel MCMs. In gold ore production, the mine hoist operates with a fixed fixed trajectory and variable payload. As shown in Fig. 5.29 (a), the pulse pattern can be obtained in trips with reduced load, and then reproduced in the full load ones - as previously demonstrated in Fig. 5.28. Fig. 5.29 (b) shows the junction temperature of each device with turn-of losses manipulation for thermal balancing, considering one trip with half of the load. In this case, the temperatures are sensed during the whole profile, the pulse pattern is stored and thereafter used for the full load trips. Fig. 5.30 (d), shows the MCM junction temperatures for the mine hoist operating with full load, yet applying the pulse pattern obtained with the

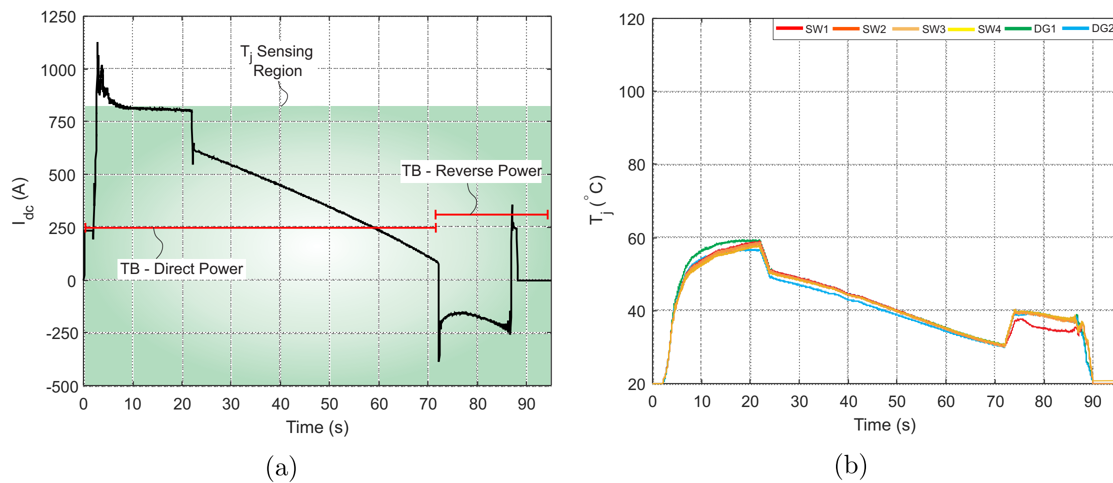


Figure 5.29: (a) Dc-Link current of the mine hoist system mission profile under reduced load, whereby the pulse-pattern of the thermal balancing strategies are obtained with a full T_j sensing capability, a shown in green. The adopted thermal balancing strategies according to the power flow, are also highlighted in red. (b) Junction temperature of each die inside the MCM for the mission profile with reduced load, whereby the temperatures are sensed, balanced and the pulse-pattern is defined.

turn-off losses manipulation under low load. As can be seen, the temperatures are balanced in a similar way.

Thereafter, the procedure is repeated for all presented strategies, whereby the pulse-pattern is obtained under load load and repeated for higher ones. Fig. 5.30 (b) shows the results for the pulse-shadowing strategy which has a temperature reduction of up to $T_{j-max-dir} = 5\,°C$ comparing to Fig. 5.30 (a). For the turn-on losses manipulation strategy, the reduction in direct power flow is upt $T_{j-max-dir} = 6.8\,°C$ as shown in Fig. Fig. 5.30 (c). Due to the slightly better efficiency, the junction temperature reduction of the turn-off losses manipulation strategy reaches up to $T_{j-max-dir} = 8.3\,°C$, as demonstrated in Fig. 5.30 (d). In reverse power flow, the indirect thermal balanc-

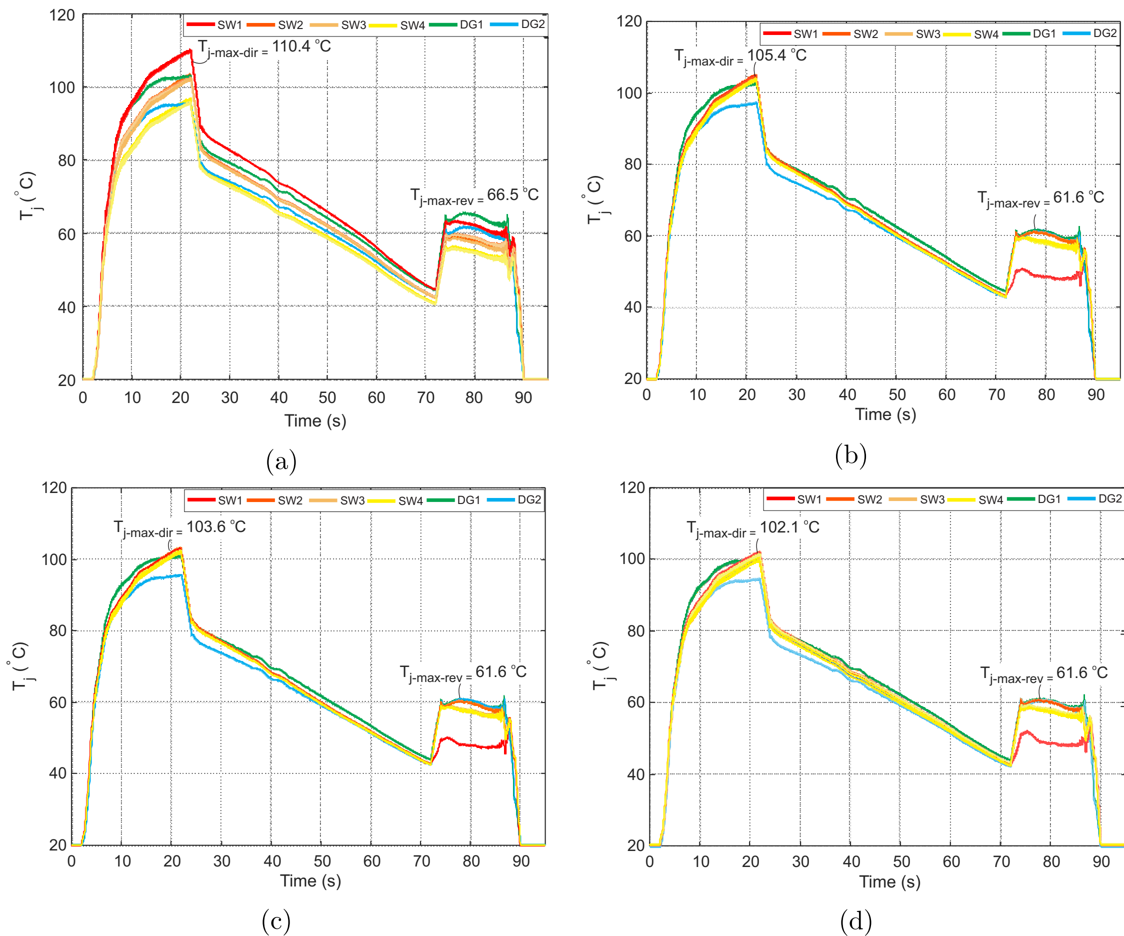


Figure 5.30: FEM-based temperature analysis for the mine hoist mission profile considering the following thermal balancing strategies: (a) None (b) Pulse-Shadowing in direct power flow and diode stress reduction in reverse power flow (c) Turn-on Losses in direct power flow and diode stress reduction in reverse power flow (d) Turn-off Losses in direct power flow and diode stress reduction in reverse power flow

ing for diodes is adopted for the three cases, whereby a temperature reduction of $T_{j-max-rev} = 4.9\,°C$ in the maximum highlighted thermal cycling can be observed.

To evaluate the impact of the thermal balancing strategies on the lifetime of the studied mine hoist system, the die-level reliability procedure - proposed in Sec. 3.7 - is applied. Thereby, the statistical and reliability analysis are realized considering the temperature and failure probabilities of each die. Hence, the monte carlo analysis is conducted for the four cases presented in Fig. fig:TransientHoist - without balancing (None) and the presented thermal balancing strategies. As can be seen in Fig. 5.31 (a), without balancing the failure probabilities are more scattered, which results in a higher failure percentage in the first operating years. The thermal balancing strategies, however, shift the failures over time, whereby the samples start to failure later depending on the thermal stress reduction provided by the respective technique. The system-level unreliability results which consider the failure probability of each die composing the system, is shown in 5.31 (b). As it can be seen, the B_{10} lifetime is increased by 22 %, 36 % and 51 % when the pulse-shadowing, turn-on and turn-off losses manipulation strategies - with the indirect strategy in reverse power flow - are adopted, respectively. The temperature and lifetime differences are summarized in Tab. 5.5.

The last analysis evaluates the impact of the thermal balancing strategies on the

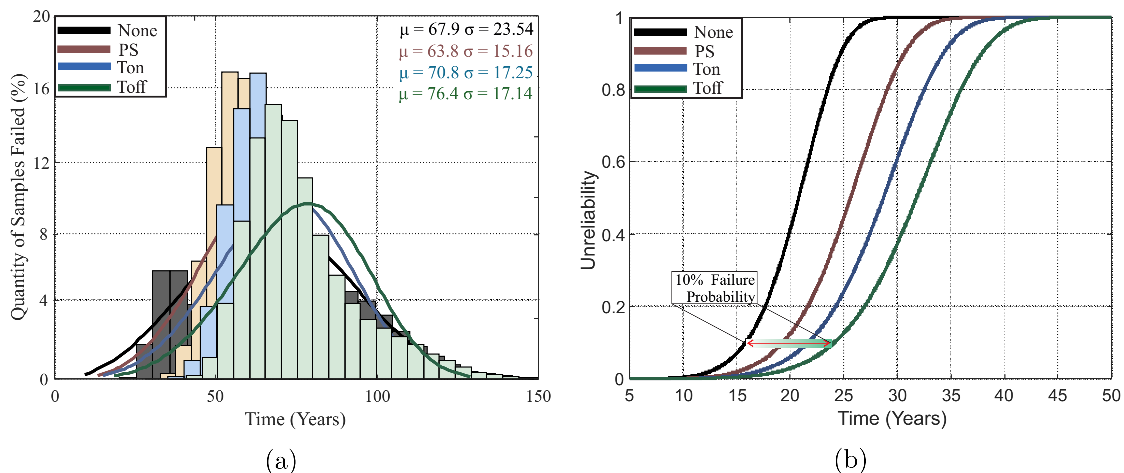


Figure 5.31: Die-level reliability analysis for the mine hoist system considering the presented thermal balancing strategies (a) Statistical Analysis (b) Unreliability Analysis.

energy losses consumption of the system during an expected operating time of 20 years (E_{15}). As can be seen in Tab. 5.5, the turn-off losses manipulation shows a slightly reduced losses consumption.

Table 5.5: Comparative analysis for the presented thermal strategies in the mine hoist system, showing the highest temperature, the B_{10} lifetime, the energy consumption only by losses in 15 years of operation (E_{15}), and their differences comparing with the system with thermal deviations.

Strategy	None	Pulse-Shadowing	Turn-on	Turn-off
$T_{j-max}\,(°C)$	110.4	105.4	103.6	102.1
$T_{j-red}\,(°C)$	-	5	6.8	8.3
$B_{10}\,(years)$	15.9	19.43	21.7	24.03
$\Delta\,B_{10}\,(pu)$	1	1.22	1.36	1.51
$E_{15}\,(GWh)$	205.36	204.40	204.64	204.97

5.7 Technical Analysis of the Proposed Solution

Although the die-level thermal balancing has presented effectiveness to increase the reliability of MCM-based power converters, its technical implementation requires specific considerations which are discussed in this section.

5.7.1 Multi-Gate Driver Considerations

To control this structure with multiple SWs, a multi-gate driver structure is required. As shown in Fig. 5.32, the multi-port structure contains a digital logic processor which receives the PWM from the main controller, manipulate the pulses and generate the gate-emitter voltage to the the parallel devices. Even though additional components are required, the potential and the gate charge are preserved and the same power supply of the ordinary solution can be maintained. As a result, the additional cost is small and the reliability is not considerably modified, because the power supply is the only component in the gate-driver with enough failure rate to impact the system-level reliability of a high-power electronics system [199]. Furthermore, the

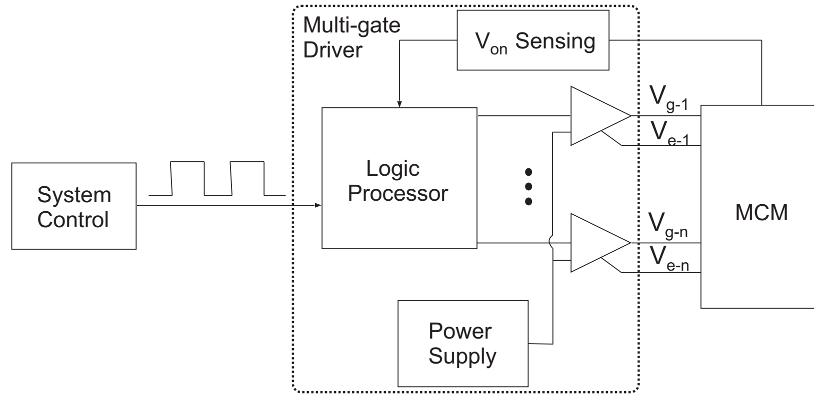


Figure 5.32: Hardware schematic of the Multi-gate driver structure for control and monitoring of multi-gate MCMs.

multi-gate driver structure allows the condition monitoring of a reduced group of dies and wire-bonds. Therefore, a degradation can be detected earlier, which for ordinary multichip modules is possible only after several wire-bond liftoffs [161].

Considering the intelligent power modules (IPM) as a future trend of power electronics, pre-driver unities can be locally embedded inside the MCM to reduce even more the commutation loops [200, 201]. As demonstrated in [195], the adoption of a selective gate driven approach decouple the commutation paths of one die to the others, thereby resulting in turn-on switching energy reduction of up to 30%.

5.7.2 Power Level Margins

Another important consideration is the power level margins for the die-level thermal balancing application. The limiting margins during a design and selection of the power devices are defined by voltage, current, temperature and transient power - current x voltage. Indeed, the voltage is not a concern during the presented thermal strategies, due to the parallel connection among the dies. Even though the devices face higher current during the pulse processing, their temperatures are reduced and any strategy can be safely applied if the natural distribution - i.e. without thermal balancing - is not exceeding the device limits. The factor limiting current during thermal balancing is the transient turn-off process, whereby the voltage and current can not overtake a predefined safe operating area (SOA). Since the voltage is fixed, the equivalent switches

shall be selected by respecting a limit of dies as well and, in case of applications with severe overload conditions, a specific operating point. Otherwise, the devices have higher probability to fail by dynamic avalanche breakdown or due to a inextinguishable current filament [17, 19]. Considering the proposed 24-dies 1.6 kA MCM, however, all the strategies can be applied at nominal and moderate overloads, whereby each device will face only 33% of extra current in the absence of one equivalent switch, and the SOA limits - of this specific device - is twice the rated current [202].

5.8 Short Summary of the Chapter

In this section thermal balancing strategies are presented to overcome thermal mismatches among the dies of a modified MCM structure. Therefore, two different strategies for direct power flow and one to reduce thermal stress on the diodes in reverse power, are proposed. It is proven that the temperatures can be balanced and the highest thermal stress reduced in up to $9.9\,°C$. A pre-programmed thermal balancing strategy is presented, eliminating the necessity of continuous T_j sensing. The possibility to apply a pre-programmed balancing, as well as the impact of each presented thermal balancing strategy in a mine hoist systems are demonstrated. The thermal balancing strategies are capable of increasing the mine hoist converter lifetime by 22 %, 36 % and 51 %, considering the pulse-shadowing, the turn-on and turn-off losses manipulation, respectively. Moreover, a technical analysis is conducted, explaining the considerations and limiting margins for a real field application of the presented strategies. The presented and studied strategies are validated by FEM-based thermal simulations and experimental results.

5.8.1 Evaluation System with Equivalent Multi-gate Multichip Module

The multichip MCM with multiple dies is not available in the time development of this thesis; therefore, an equivalent multi-gate multichip module structure is constructed through a six-pack power module (DP-25F1200T-101666). Hence, the phase devices are placed in parallel, via a small bus bar directly connected to the collector of the upper devices, as shown in Fig. 5.33(a). In addition to the three parallel devices, the bottom diodes are also attached to the circuit, thereby resulting in a buck converter, as shown in Fig. 5.33 (b). To enable thermal analysis capability, the power module has its silicone gel removed and is painted in black to ensure homogeneous emissivity. To obtain a considerable thermal mismatch, the power modules is coupled to two different heatsinks, whereby S1 and S2 are over heatsink H1 whilst S3 is over heatsink H2, as detailed in Fig. 5.33 (a). Therefore, turning on the cooler of H2 the

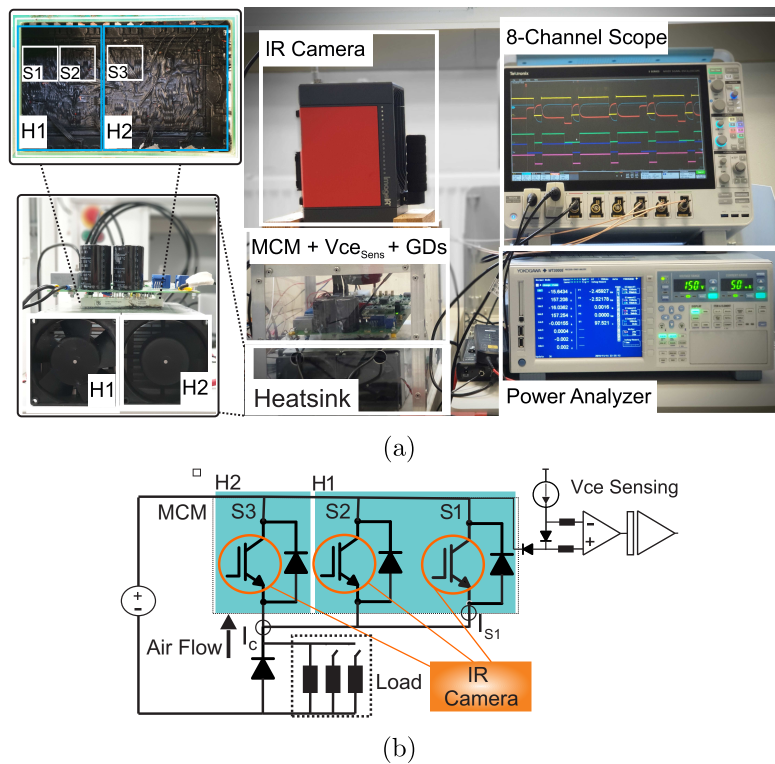
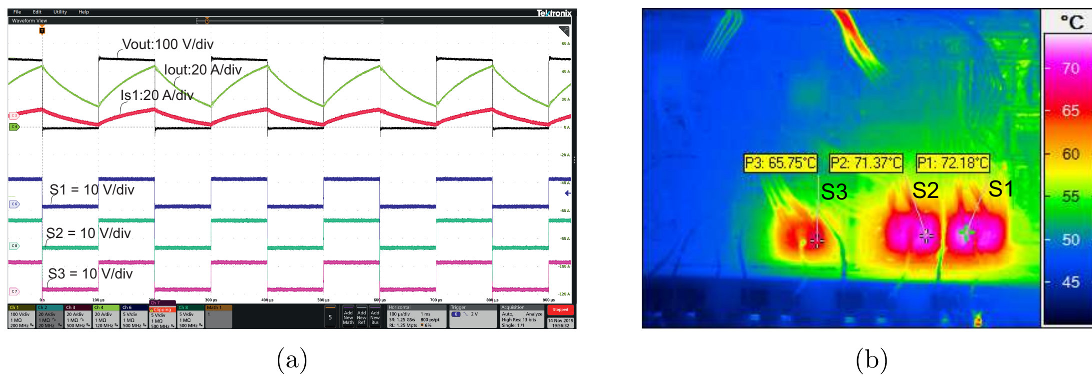


Figure 5.33: Validation Setup consisting of: an equivalent multi-gate multichip power module in two heatsinks, driver board, V_{ce} sensing, variable load and infrared camera : (a) Wide view of the open three-dies module, V_{ce} sensing and drivers. (b) Schematic.

temperature of S3 is reduced, thereby increasing the thermal mismatch with S1 and S2, which are in turn naturally hotter due to the thermal cross-coupling between them. To drive the parallel group and sense the temperature, a driver board with the V_{ce} sensing circuit developed in Sec. 4.5 is adopted. To interface with the driver board a Microlab Box Dspace which has an embedded logic processor and a very fast analog-to-digital converter (ADC) - as previously mentioned - and it is used for the modulation and pulse processing of the the proposed strategies. For the thermal validation of the balancing strategies, it is used an infrared (IR) camera with high resolution as shown in Fig. 5.33 (b). In addition, three resistors are placed in parallel, where two of them are connected through circuit breakers, enabling online current variations, as also demonstrated in Fig. 5.33 (b). The adopted operating parameters are stated in Tab. 5.6.



(a) (b)

Figure 5.34: Validation system with equivalent multi-gate multichip modules : (a) Output waveforms (b) Thermal distribution on the equivalent multichip module.

Fig. 5.34 (a), show the electrical results of the three dies buck converter, including the output voltage, output current, current in one device (S1) and the gate commands.

Table 5.6: Validation parameters.

Power Module	DP-25F1200T-101666
Power Capability	3x 25 A/1200 V
V_{dc}	250 V
I_{out} (1 pu)	23 A
F_{sw}	5 kHz
Duty Cycle	0.5

Fig. 5.34 (b), shows the obtained thermal distribution among the three devices, with a maximum deviation of $6.43\,^{\circ}C$ due to the cross-coupling effects of the closer devices (S1, S2) and the lower thermal resistance of the third one (S3), which has influences of the turned-on air cooling system.

Chapter 6

Conclusions and Future Research

Contents

6.1 Summary 134
6.2 Future Research I - Die-Level Thermal Balancing in Wide-Bandgap Devices 136
6.3 Future Research II - Degradation Control Through SOH of Power Semiconductor Devices 136

6.1 Summary

The multichip power modules (MCM) will remain the standard solution for high power mission critical applications in a foreseeable future. This structure, contains a plurality of chips inside the same package, thereby achieving high power density and lower cost. However, its structure limitation results in critical thermal mismatches which ultimately induces substantial thermal stress in specific subset of devices. Although many strategies to mitigate this effect have been proposed in the last 30 years, the MCM-based converter still operating with a reduced reliability. Therefore, this work proposed reliability-oriented solutions to reduce the impact of uneven thermal stress and improve the reliability of MCM-based mission critical applications.

The first section has discussed the causes and consequences of uneven thermal distribution in MCMs. A FEM model of a 24-dies MCM is developed to demonstrate the thermal deviation among the MCM dies. It is concluded that the thermal cross-coupling affects the thermal unevenness by up to $17.4°C$. The consequences of the extra thermal stress in specific dies is presented in sequence, thereby demonstrating that the temperature affects multiple failure mechanisms of power semiconductor devices, potentially provoking either catastrophic or aging failures. At the end, the already proposed solutions to mitigate such effects and avoid premature failures are presented; however, it is concluded that further research are necessary, because the MCM remains experiencing critical thermal deviations nowadays.

The next section has evaluated the impact of the degradation unevenness on the lifetime of MCMs, and presents one research target: the addition of a die-level thermal and reliability analysis on the design for reliability procedure of MCM-based systems. In this methodology, the temperature and failure probability of each die are taken into account. It is furthermore demonstrated, that the common DFR processes may result in considerably high erroneous lifetime prediction in MCM-based mission critical applications.

Thereafter, a review of the proposed thermal control and aging monitoring strate-

gies is presented. For the monitoring, the V_{on} has stood out due to its relatively simplicity, reasonable resolution requirements and capability to sense temperature and detect degradation. Therefore, a high-resolution circuit is implemented and its capability to close the loop of thermal control strategies is experimentally validated. It is demonstrated a resolution of $0.3\,mV$ and capability to sense online temperatures in applications of up to $15\,kHz$. Moreover, another contribution is presented in this section, whereby a power routing strategy for multiphase machines is proposed. This strategy was based oon the capability of a multiphase machine to work under soft-unbalanced condition without degrading its magnetic performance. Thereby, the strategy proposes to direct the power from the hottest MCM to other phases to alleviate its thermal stress. It is demonstrated that the temperature of one phase can be reduced by $9°C$, adding only $1°C$ to the remaining ones. As a result, the converter lifetime can be increased in up to 22%, thereby overcoming a thermal deviation effects caused by a defected heatsink.

Based on the implemented review, the next section proposes a die-level thermal balancing to overcome the critical mismatches among the dies in multichip modules. For that, a hypothetical packaging structure with four gate-emitter commands is considered. Thereby, two novel strategies are proposed, one shadowing pulses and the other turning-off softly the hottest devices, to balance the temperature among the IGBT dies in direct power flow. As a result, a thermal reduction of up to $8.5°C$ in the hottest devices, is demonstrated. Moreover, a strategy is proposed to reduce the thermal stress among the diodes in negative power factor applications, by shadowing specific devices and reducing the cross-coupling effects, thereby achieving a thermal reduction of up to $9.9°C$ is achieved. A reliability and losses analysis, has demonstrated better performance for the turn-off losses manipulation in direct power flow, due to its additional capability to reduce the overall MCM losses. This strategy, allied to the diode thermal stress reduction in reverse power flow, can increase the lifetime of a MCM-based mine hoist system converter in up to 51%.

6.2 Future Research I - Die-Level Thermal Balancing in Wide-Bandgap Devices

The thermal mismatches in parallel wide-bandgap devices is even more critical, due to its not consolidated fabrication process. In very high switching frequency applications, for examples, thermal deviations of up to $50°C$ have been reported [38, 44, 45]. A statistical analysis of the parametric deviation impact on the transient current distribution and the resulting thermal mismatches of a parallel association of multiple samples of SiC devices, is conducted in reference [45]. It is demonstrated that thermal deviations of up to 10, 18 and 32 ° C for parallel devices switching at 50, 100 and 200 kHz, respectively, even limiting the deviations to $\sigma < 0.5$ by selecting similar devices. Moreover, wear out resulting from thermal cycling has been more evident and even more critical in latest technologies such wide-bandgap based power modules [203]. Therefore, investigating the effects and implementation concerns of a die-level thermal balancing in wide-bandgap based MCMs, has a high relevance for the future of power electronics.

6.3 Future Research II - Degradation Control Through SOH of Power Semiconductor Devices

Even though many methods for online T_j sensing of power devices have been proposed, its implementation in industrial environment stills challenging, whereby a noisy environment can disturb the accuracy of the sensing circuits. An alternative for this solution is to use a data-driven methodology to detect the aging rather than the temperature of the devices. Therefore, the devices can be sensed $in - situ$ and the pulse-patterns updated seasonally, thereby avoiding on-line sensing disturbances. The V_{ce} sensing circuit, which is implemented in this work, has a huge potential to be the aging detector parameter

Appendix A

V_{on}-based Sensing Circuit Design

A.1 Design of a V_{on}-based Sensing Circuit

This appendix give detailes about the technical implementation of the V_{on} sensing circuit presented in Sec. 4.5.

A.1.1 Power Supply

The biggest challenge of the online V_{on} sensing is the precision required to obtain the T_j sensing resolution ensuring isolation capability. Consequently, the necessity of isolated power supplies operating at few kHz can generate noise - ranging up to 20 MHz -, which may result in interference via coupling capacitance. Moreover,the pulsating energy flow can cause output voltage ripple and a reflected input ripple current. The pulsating ripple is generated from each switching cycle, which provokes voltage rising and falling in the output capacitors which supply the load by itself between the power transfer cycles. In addition, the switching of the isolated dc-dc converter induces a high frequency and a common mode noise to the output voltage and input current ripple, respectively. Although the input and output ripple can be reduced with additional output capacitance, it has no effect on the common mode noise [204].

Therefore, three separate filters to reduce ripple and noise to very low levels are necessary, whereby each one handles a specific part of the interference spectrum [205]. The step-by-step of a a very low noise filter implementation, considering the adopted dc-dc source (R1ZX-0505), which has a inherent $30\,mVp-p$ ripple, is presented in

reference [205]. The first step is to add $2\,nF$ capacitors across V_{out} and V_{in}, which provides quite lower impedance return path compared to the 100 pF transformer coupling capacitance. Thereafter, two 10 μF multilayer ceramic capacitors are connected in parallel to reduce the ESR, which considerably reduce the input and output ripple. However, to filter the high frequency common mode noise, the addition of capacitance to the LC filters is not effective. Therefore, 50 μH and 10 μH chokes forming common mode Pi-filters are added to the input and output, respectively [205]. The resulting circuit is shown in 4.35 (a), which is implemented in the developed V_{on} sensing board.

A.1.2 Operational Amplifier

The precision of the output sensing is also the main criteria for the selection of the operational amplifier. Therefore, a high-precision, ultra-low noise operational amplifier (ADA4528-1), is selected. In this work, the goal is to sense only the junction temperature of the transistor (V_{on}), and a single-supply device is adopted and fed with +5 V referenced to the digital ground. Moreover, the selected amplifier has high common mode - $CMRR = 135\,dB$ - and power supply - $PSRR = 135\,dB$ - rejection ratio, which contributes to reduce even more the impact of common mode and power supply interferences.

A.1.3 Isolation

The isolation is also a critical part of the sensing circuit, which is connected to a high-voltage reference. For that, a cost-effective precision amplifier with capacitive isolation is selected (ISO124) [206]. This component, has a $50\,kHz$ signal bandwidth, and a $2\,pF$ differential capacitive barrier rated for up to $1500\,Vrms$. This isolator, however, introduce a $20\,mVp{-}p$ ripple to the signal which has to be filtered, to achieve the required precision. Therefore, a Sallen-Key filter, shown in Fig. 4.35, is added in the output, to eliminate the ripple and keeps full bandwidth [207].

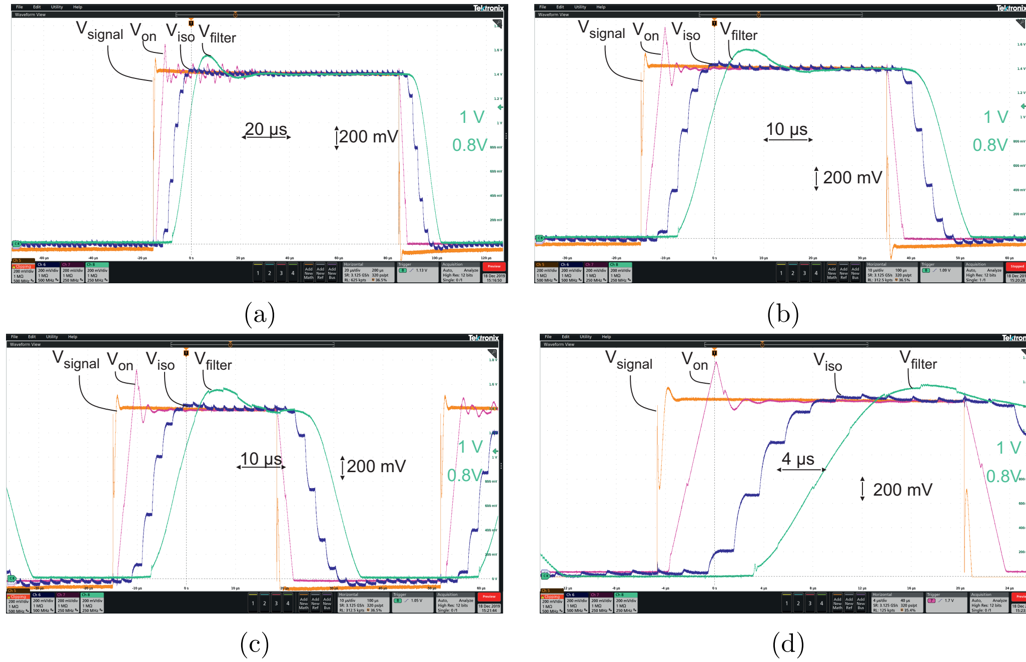
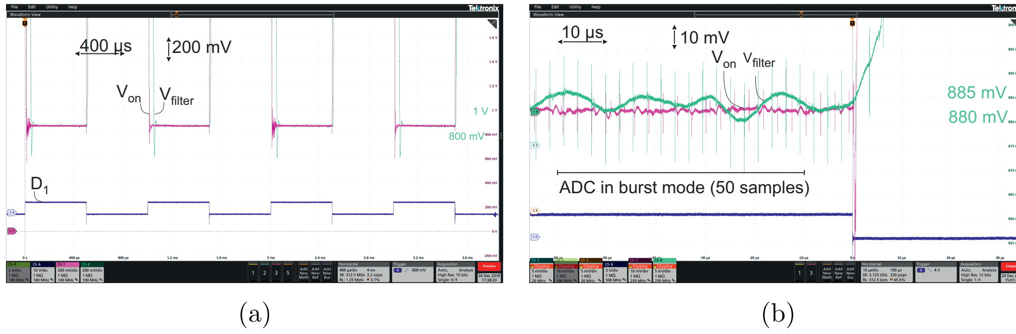


Figure A.1: Transient performance of the V_{on} sensing circuit, using a square wave generator with duty cycle of 0.5 and switching frequencies of: (a) $5\,kHz$ (b) $10\,kHz$ (c) $15\,kHz$ (d) $20\,kHz$

A.1.4 Transient Performance

The transient performance validation of the V_{on} sensing on each stage of the developed circuit is demonstrated in Fig. A.1. For that, square waves with 5, 10, 15 and $20\,kHz$ and a duty cycle of 0.5 are applied, whereby a signal wave generator is connected to the board terminals to emulate the V_{on} of a transistor. The generated signal is represented in orange, the Op amp output (V_{on}) is in pink, the isolated signal (V_{iso}) is in blue and the filtered (V_{filter}) is the green signal. As can be seen in Fig. A.1, V_{on} has a fast transient response, and low disturbance in steady-state. V_{iso}, however, has an additional ripple and an additional response delay. Moreover, the filter capability to mitigate the signal ripple and provide a cleaner signal in the output, is also observed. As shown in Fig. A.1 (a) and (b), the circuit has a satisfactory response in 5 and $10\,kHz$, despite the additional delays provided by each circuit part. Nevertheless, for 15 and $20\,kHz$, the output filter can not achieve steady-state, thereby compromising the V_{on} sensing. In this case, the Sallen-Key has to be bypassed and alternative methods shall be adopted.



(a) (b)

Figure A.2: Steady-state validation of the sensing circuit showing an output voltage for V_{on} (pink) and V_{filter} (green) with a fluctuation of around $5\,mV$ (a) Full view (b) Zoom.

A.1.5 Steady-State Performance

To validate the steady-state performance, the sensing board is connected to the collector-emitter terminals of an IGBT in a buck converter switching at $1\,kHz$, operating with $40\,V$ and a current of $1\,A$. Fig. A.2, shows the V_{ce} sensing during the conduction stage of the device, with an output voltage varying between 850 and $855\,mV$. As clearly seen in Fig. A.2, V_{filter} has a higher fluctuation comparing with V_{on} due to the additional ripple generated by the isolation circuit which is mitigated but not eliminated by the output filter.

A.1.6 Moving Average Digital Filter for High Precision

Although the proposed hardware can effectively sense V_{on} with a reasonable precision ($5\,mV$), a higher resolution is required to achieve T_j sensing capability. Therefore, a digital filter is implemented in the Dspace Microlab Box system. For that, the analog-digital converter (ADC) channels - which has $1\,MSPS$ (million samples per second), 16 bits and burst mode operation - are used to realize multiple sequential sampling with an interval of 1 μs. Then, 50 samples are acquired per period during the steady-state circuit operating region, and used for a moving average filter implementation, as shown in (A.1). Since the ADC in burst mode, the multiple sampling is realized inside the same period, without interfering the sensing bandwidth.

$$V_{on-avg} = \frac{V_{on}[0] + V_{on}[1] + \cdots + V_{on}[49]}{50} \tag{A.1}$$

Appendix B

Design and Control of the Adopted Electrical Drives

B.1 Electrical Drive Design and Control

The electrical drive design of the mine hoist system study is presented in this appendix. Firstly, a research in the e-catalog of the company WEG is realized, and the rated characteristics of the selected machine are stated in Tab. B.1. As can be seen, the induction machine of 1 MW, has a nominal voltage of 690 V and current of 1070 A at full load (I_L). The current at no load is 560 A (I_{NL}), whilst the locked rotor current (I_i/I_n) achieves up to 6520 A and the breakdown torque (T_{bd}) is 200 %. This machine has a frequency of 50 Hz and six poles, thereby achieving a speed of 990 rpm at full load, with a total slip of 1%. Although the machine rated characteristics are available in the catalog, the parameters of its magnetic equivalent circuit - shown in Fig. B.1 - are necessary, for simulation purpose and field orientation control realization. The parameters are based on the rated characteristics provided by the manufactures, and its parameters are also shown in Tab. B.1, where r_r, r_s and r_m are the rotor, stator and magnetizing resistances, whereas X_r, X_s and X_m are the respective reactances.

To validate the equivalent circuit parameters, the values are loaded in an induction machine model of the electrothermal software. Thereafter, the machine is fed by a three phase voltage source with V_{line} = 690 V, thereby achieving the nominal current at full load, as shown in Fig. B.2. As can be seen in Fig. B.3, a nominal load step is applied

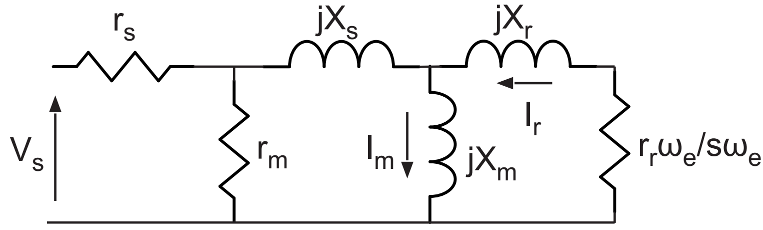


Figure B.1: Induction machine equivalent magnetic circuit.

Table B.1: Rated and equivalent circuit parameters of the 690 V/ 1 MW three-phase induction machine.

Parameter	Value
Power	1 MW
V_{line}	690 V
I_L	1070 A
I_{NL}	560 A
I_i/I_n	6.1
T_{bd}	200 %
Frequency	50 Hz
Poles	6
Speed	990 rpm
$cos(\phi)$	0.83
η	94.9 %
Slip	1%
J	29.46 kgm^2

Parameter	Value
r_r	4 $m\Omega$
r_s	3.9 $m\Omega$
r_m	9.5 Ω
L_r	0.2 mH
L_s	0.13 mH
L_m	3.2 mH

at t = 4 s and the machine rotates with nominal speed, showing the rated slip of 1 %.

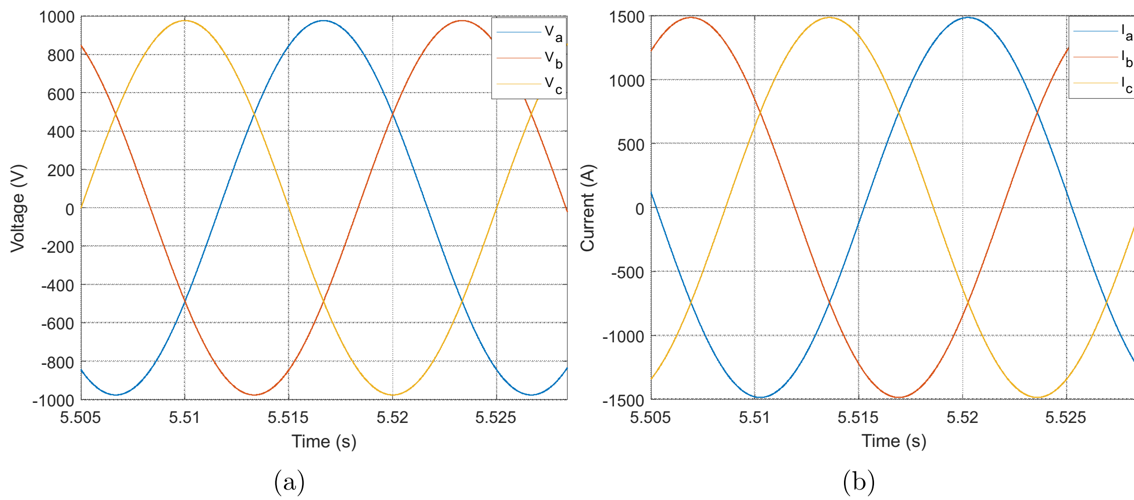


Figure B.2: Simulation of the induction machine with equivalent magnetic circuit parameters under nominal load (a) Line voltages (b) Stator Currents.

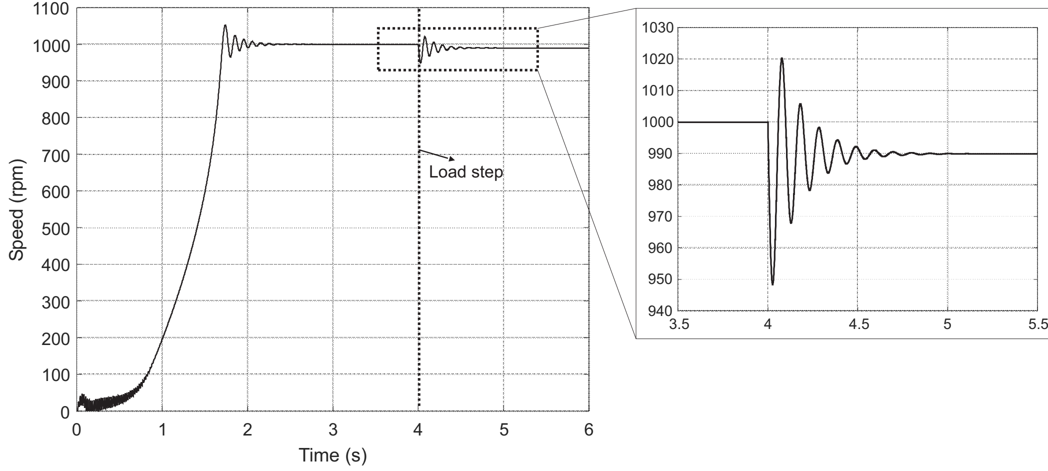


Figure B.3: Photo of the electrical system of the mine hoist.

B.1.1 Indirect Field Orientation Control

To drive the mine hoist, the speed of the induction machine has to be controlled, and the indirect field orientation control (IFOC) is adopted. In this strategy, the angle of the rotor flux is calculated by the slip relation B.1. As can be seen, it includes the lag in flux response ($\hat{\tau_r}$) in a non linear calculation and it is entirely based on current commands (I^*_{ds}, I^*_{qs}) [208]. The slip and angle calculator is represented in green in the general diagram of the IFOC, shown in Fig. B.4.

$$S\omega^*_e = \frac{\frac{1}{\hat{\tau_r}} \cdot I^*_{qs}}{\frac{1}{1+\rho\hat{\tau_r}} \cdot I^*_{ds}} \tag{B.1}$$

In the field oriented control, the currents noted in d,q are decoupled, whereby I^*_{ds} represent the flux command whilst I^*_{qs} is the torque command. I^*_{ds} is applied to magnetize the machine; therefore, it is has a fixed value, which is calculated based on the estimated magnetizing inductance ($\hat{L_m}$) and the rotor flux (λ^*_{dr}) as presented in B.2. Since the skip velocity is controlled in this application, the torque reference (T^*) is provided by the output of the speed controller, and I^*_{qs} is calculated by its relation with the estimated rotor inductance ($\hat{L_r}$), $\hat{L_m}$ and λ^*_{dr}, as shown in B.3.

$$I^*_{ds} = \frac{1}{\hat{L_m}} \cdot (1 + \hat{\tau_r}\rho) \cdot \lambda^*_{dr} \tag{B.2}$$

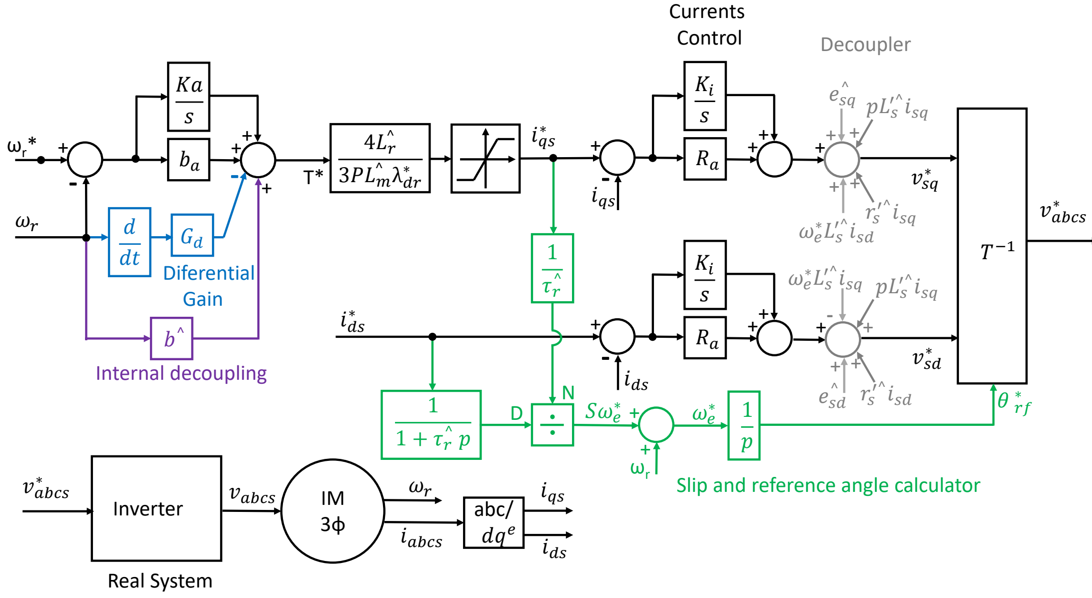


Figure B.4: Indirect field orientation control for a three-phase induction machine.

$$I_{qs}^{*} = T^{*} \cdot \frac{4 \cdot \hat{L}_{r}}{3 \cdot P \cdot \hat{L}_{m} \cdot \lambda_{dr}^{*}} \tag{B.3}$$

B.1.2 Control Tuning

As shown in Fig. B.4, the inner current loop has a proportional controller, which is modeled by the transfer function shown in B.4.

$$\frac{i_s}{i_s^*} = \frac{G}{\tau_s + 1} \tag{B.4}$$

where, $G = \frac{R_a}{R_a + r_s}$ and $\tau_s = \frac{L_s'}{R_a + r_s}$; $L_s' = \frac{L_s - L_m^2}{L_r}$. Therefore, considering a cutoff frequency of 500 Hz - one decade below the switching frequency - the proportional gain of the current loop is $R_a = 1.02\ \Omega$. To verify the capacity of the control loop to reject the disturb caused by the back electromotive force (E_s) and follow the trajectory, its dynamic roughness is modeled. As shown in B.5, it correlates the obtained proportional gain with machine parameters.

$$\left| \frac{E_s}{i_s} \right| = sL_s' + (R_a + r_s) \tag{B.5}$$

Fig. B.5 shows the frequency response of the control loop and its dynamic roughness. As can be seen, the transfer function has the selected cutoff frequency and a small attenuation of G = 0.99, due to the coupling of r_s. The dynamic roughness is $R_a + r_s = 1.03$ and increase with frequency following the slope of L'_s.

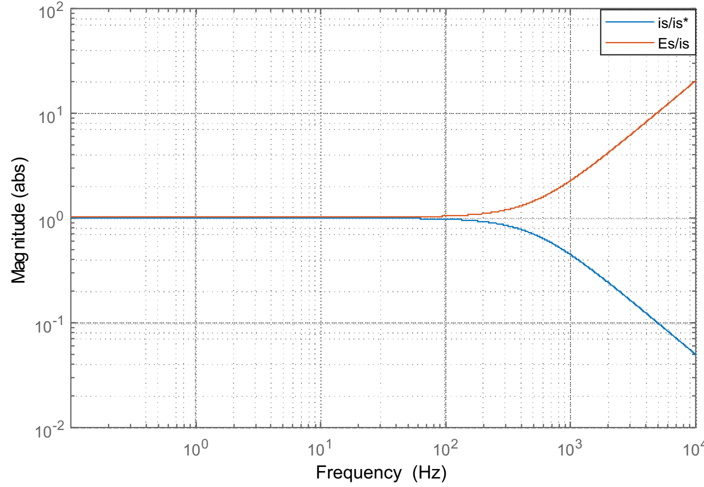


Figure B.5: Frequency response of the system, for the current loop.

The outer speed loop control, however, has an additional integral gain and is modeled as shown in B.6.

$$\frac{w}{w^*} = \frac{sGb_a + GK_a}{J\tau_s s^3 + s^2(J + b\tau_s + G_d G) + s(b + b_a G) + K_a G} \tag{B.6}$$

where, G_d is a differential gain to reduce the effects of load variation in the motor speed, b_a the proportional gain, k_a the integral gain, J the momentum of inertia and b the viscous friction. The cutoff frequencies are selected to be one and two decades below the inner control loop, i.e. 50 Hz and 5 Hz. As a result, considering $G_d = 0$, the proportional and integral gains are $b_a = 1.081e^4$ and $k_a = 2.9e^5$, respectively. The dynamic roughness of the speed control loop is based on its capacity to follow the trajectory and reject the disturb caused by the torque, as shown in B.7.

$$\left|\frac{T_L}{w}\right| = \frac{J\tau_s s^3 + s^2(J + b\tau_s + G_d G) + s(b + b_a G) + K_a G}{s^2\tau_s + s} \tag{B.7}$$

The frequency response of the transfer function and dynamic roughness of the speed

loop are shown in Fig. B.6. The speed control loop has an attenuation of 10/decade between 50 and 500 Hz, and 100/decade after 500 Hz due to the cutoff frequency of the current loop. Different to the current loop, the gain of the w/w^* is unitary even at low frequencies due to the integral action of the speed loop. The dynamic roughness T_L/w is infinite for constant disturbs - constant load torque. For frequencies between 5 and 50 Hz, the dynamic roughness presents its lower values with minimum around $b_aG = 1.0e^4$. For frequencies higher than 50 Hz, the dynamic roughness starts to increase again with slope defined by J. Therefore, the high frequency disturbs are rejected only by the inertia of the system.

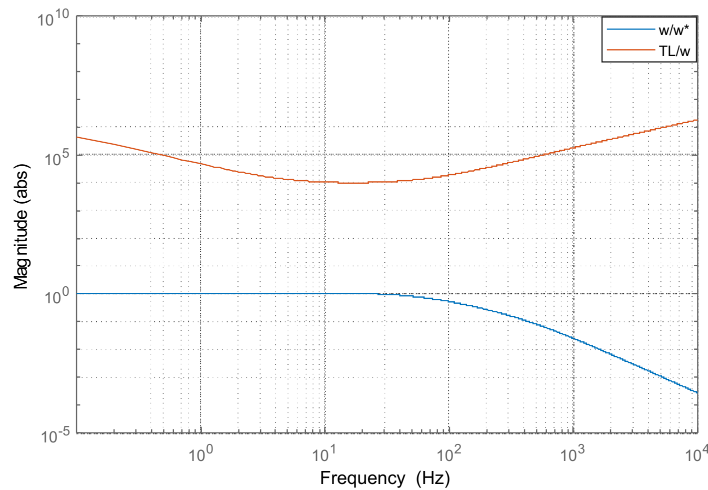


Figure B.6: Frequency response of the system, for the speed loop.

B.1.3 Time Domain Response

To evaluate the time domain response of the control system, the induction machine is started in a ramp of 100 rpm/s, and a nominal load step is applied when the machine achieve the nominal speed, as shown in Fig. B.7. In Fig. B.7 (b), an electrical torque (T_e) is observed during the starting and T_e follows the reference when the load step is applied at t= 15 s. The speed control performance in time domain is demonstrated in Fig. B.7 (a), whereby the measured speed follows the reference with small overshoot, even after a nominal load step.

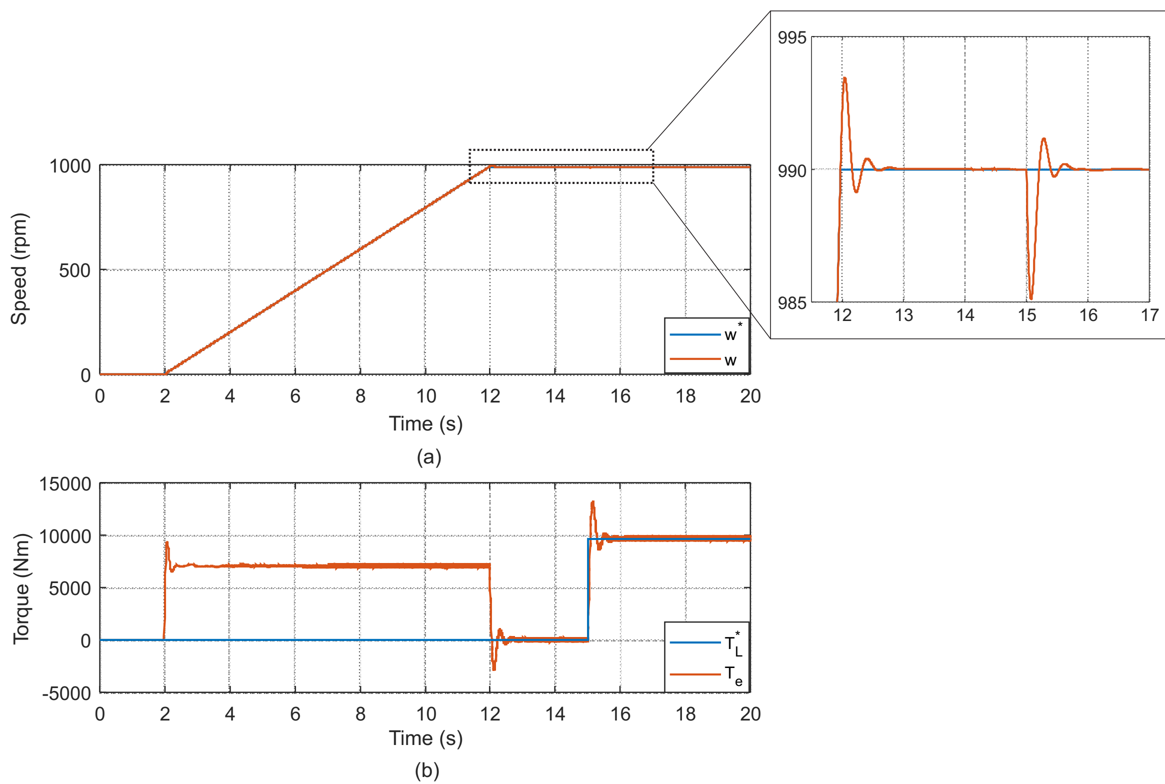


Figure B.7: Time domain response of the IFOC applied in the selected induction machine: (a) Reference and measured speed (b) Electrical and load torque.

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