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Power loss investigation of series-connected current source inverters

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Power Loss Investigation of Series-Connected Current Source Inverters

by

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AUTHOR'S DECLARATION

I hereby declare that I am the sole author of this thesis. This is a true copy of the thesis, including any required final revisions, as accepted by my examiners. I understand that my thesis may be made electronically available to the public.

Abstract

Current-source inverters (CSIs) are a type of direct current (DC) to alternating current (AC) converters that generate a defined AC output current waveform from a DC current supply. As the counterpart of voltage source inverters (VSIs), they feature a simple converter structure, low switching *dv/dt* on the ac-side, and reliable short-circuit protection. These advantages have made CSIs widely used in high power medium voltage drives. Besides, they have also been studied in other applications, such as wind energy conversion systems, superconducting magnetic energy storage (SMES) systems, and microgrid systems. Different topologies of CSIs and modulation schemes have been evolved to tailor various application requirements. For those applications with a higher power rating, two or more CSIs can be connected in series to form series-connected CSIs (SC-CSIs) to increase the power handling capability. To the best of the author's knowledge, three topologies of SC-CSIs have been developed so far. The first topology referred to as topology A is constructed by connecting several identical CSIs in series. These CSIs are identical in terms of topology, modulation, and control. A multi-winding transformer is employed at the output to provide a clear current path for each CSI and step up the voltage if necessary. In the second topology designated as topology B, the multi-winding transformer is replaced by a phase-shifting transformer, and a phase-shifting modulation scheme is implemented. This topology features an increased DC current utilization, decreased switching losses, and reduced passive components. The third topology denominated as topology C adopts a different arrangement of switches leading to a reduced number of switching devices. A multi-winding transformer is used at the output in this topology. Power losses are an important attribute of SC-CSIs since they have a significant impact on the efficiency of the system. Besides, it is necessary to find out the power loss distribution of inverters to design an appropriate cooling system. However, the power losses and the power loss distribution of these three topologies have not been figured out.

In this thesis, the power losses and the power loss distribution of each topology are investigated in a comparative method. This is divided into two parts. In the first part, the power losses of the switching device used in SC-CSIs are introduced. The factors which can

influence the power losses of SC-CSIs are analyzed in detail. The parameter of each factor is compared in the three topologies of SC-CSIs. The power loss distribution of each topology is figured out. The total power losses of these three topologies are compared under one modulation scheme first to find out the topology which has the fewest total power losses. In the second part, three typical pulse width modulation (PWM) schemes and how they influence the power losses of SC-CSIs are analyzed. The power losses of the three topologies are compared under different modulation schemes. The topology and the modulation scheme with the fewest power losses are recommended. Simulations are used to assist the investigation and verify the results.

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Publications

[1] B. Jiang, Z. Wang, and Q. Wei, "Power Loss Investigation of Series-Connected Current Source Inverters," *IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society*, pp. 1-6, Oct. 2021.

[2] Z. Wang, B. Jiang, and Q. Wei, "DC-link Inductor Investigation for Series-Connected Current Source Converter," *2021 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 3211-3215, Oct. 2021.

[3] B. Jiang "Power Loss Investigation of Series-Connected Current Source Inverters with Different Modulation Schemes." (To be submitted)

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List of Symbols

Symbol	Meaning
A, B, C	inverter output terminals
$C_f, C_1 \ldots C_n$	CSI output filter capacitance
dv/dt	voltage rate-of-change
E_{off}	the turn-off energy losses of IGBTs
E_{on}	the turn-on energy losses of IGBTs
E_{rr}	reverse recovery energy losses of diodes
F_{sw}	switching frequency
$g_1 \ldots g_6$	gating signals
i_a, i_b, i_c	phase currents
I_c	conduction current
I_{dc}	dc-link current
i_s	inverter output current
i_w	inverter output PWM current
$L_1 \ldots L_n$	inductance
m_a	modulation index
P_{con}	conduction losses
P_{sw}	switching losses
Q_{rr}	Reverse recovery charge of diodes
$R, R_1 \ldots R_n$	resistance
$S_1 \ldots S_6$	switching devices of inverters
$S_1 \ldots S_6, S_{n1} \ldots S_{n6}, S_w, S_{w'}$	switching devices of inverters
T_s	sampling period
V_{AB}	line to line voltage
V_B	reverse blocking voltage
V_{on}	saturation voltage
θ	angle of a vector in the space vector plane
ω	fundamental angular frequency

List of Abbreviations

Abbreviation	Meaning
AC	alternating current
APOD	alternative phase opposition disposition
CH7	current source H7 inverter
CMV	common-mode voltage
CSI	current source inverter
CS-MMC	current source modular multilevel converter
CSR	current source rectifier
DC	direct current
GCT	gate commutated thyristors
GTO	gate turn-off thyristors
IGBT	insulated-gate bipolar transistor
MCSI	multilevel current source inverter
MOSFET	metal-oxide semiconductor field-effect transistor
MV	medium voltage
MVSI	multilevel voltage source inverter
NS-SVM	natural sampling SVM
PU	per unit
PWM	pulse width modulation
SC-CSIs	series-connected current source inverters
SGCT	symmetric gate commutated thyristors
SHE	selective harmonics elimination
SMES	superconducting magnetic energy storage
SQ1	sequence 1
SQ2	sequence 2
SQ3	sequence 3
SQ4	sequence 4
SQ5	sequence 5
SQ6	sequence 6

SVM	space vector modulation
TPWM	trapezoidal pulse width modulation
UPS	uninterruptable power system
VSI	voltage source inverter

Chapter 1
Introduction

The PWM CSI was proposed in the early 1970s [1] and has been receiving more and more attention. It produces a defined three-phase AC current waveform from a stiff DC current source. The input DC current can be obtained by connecting a relatively large inductor in series with a DC voltage supply. CSIs use switching devices with self-extinguishable capability and bipolar voltage blocking capability. By implementing an appropriate switching control strategy, the magnitude and the frequency of the output current can be controlled. Compared with voltage source inverters (VSI), CSIs exhibit several advantages, such as a simple converter structure, low switching *dv/dt* on the output side, inherent four-quadrant operation, and reliable overcurrent and short-circuit protection [2]. They have been widely used in high power medium voltage (MV) drives [2]–[7] in industry and drawing increasing attention in other applications, such as wind energy conversion systems [8]–[11], superconducting magnetic energy storage systems [12]–[13], microgrid systems [14]–[15], and photovoltaic power system [16]–[17].

Different topologies of CSIs have been developed to satisfy various application requirements since the beginning of power electronics. In general, CSIs can be classified into three-level CSIs, multilevel CSIs, parallel CSIs, and SC-CSIs. The three-level CSI can only generate three current levels in each phase (line current) [18]. The typical three-leg CSI is the basic structure of three-level CSIs. Based on this, other topologies such as four-leg CSI [19], five-leg CSIs [20], and current source H7 (CH7) inverters [17] have been developed to improve the inverter performance, including reducing the common-mode voltage (CMV) and improving the reliability. Besides, the output current waveforms of CSIs can be multilevel. Unlike multilevel VSIs (MVSIs) which have been widely studied and commercialized, the research on multilevel CSIs (MCSIs) is a recent subject [21]. The topologies of MCSIs can be classified into single-rating inductor MCSIs, multi-rating inductor MCSIs, paralleled H-bridge MCSIs, two-stage MCSI, buck-boost derived MCSIs, Ćuk-derived MCSIs, and current source modular multilevel converter (CS-MMC) [21]. Among them, the topologies of single-rating inductor, multi-rating inductor, and paralleled

H-bridge MCSIs are developed from classical MVSIs by applying the principle of duality [21]. The two-stage MCSI consists of a three-level DC-DC boost converter stage and an H-bridge inverter stage [21], which is a single-phase inverter. Thus, it will not be discussed in this thesis. The main advantages of MCSIs are the improved output power quality and the reduced current stress of the switching devices [22]. In MCSIs, many topologies can be seen as parallel CSIs since several CSI modules are connected in parallel to increase the number of the levels of the output current waveforms. Besides, parallel CSIs are also used in applications with high power ratings due to the increased power handling capability of the inverter [23]–[25]. Apart from parallel CSIs, two or more CSIs can also be connected in series [9], [25]–[32] to increase the power rating of the inverter. To the best of the author's knowledge, three types of SC-CSIs have been developed so far.

This chapter starts with a review of the CSI topologies, including three-level CSI, multilevel CSIs, parallel CSIs, and SC-CSIs. Then the power losses of SC-CSIs are discussed, and the objectives of the dissertation are defined.

1.1 Current source inverter topology

According to the number of the levels of the inverter output current, CSIs can be divided into three-level CSIs and multilevel CSIs. Besides, two or more CSIs can be connected in parallel or in series to increase the power rating of the inverter. Based on the connection manner, CSIs can be classified into single CSI, parallel CSIs, and SC-CSIs.

1.1.1 Three-level current source inverter

Figure 1-1 shows the configuration of a conventional three-phase current-source inverter with a three-phase balanced load [3]. It is the typical topology in CSIs. The function of the CSI is converting the DC current to a defined three-phase PWM output current i_w. The DC side of the CSI is a stiff DC current source I_{dc}. In practice, the DC current source I_{dc} can be obtained by a current source rectifier (CSR), and a DC choke is needed to make the DC current smooth and continuous. The inverter consists of six switching devices which are composed of insulated-gate bipolar transistors (IGBTs) series connected with diodes. By

using an appropriate switching control strategy, the frequency and the magnitude of the output current can be controlled. The inverter output has three current levels in each phase (line current). Normally, a three-phase capacitor C_f is employed at the output side to assist the commutation of the switching devices and filter out the harmonics in the output current.

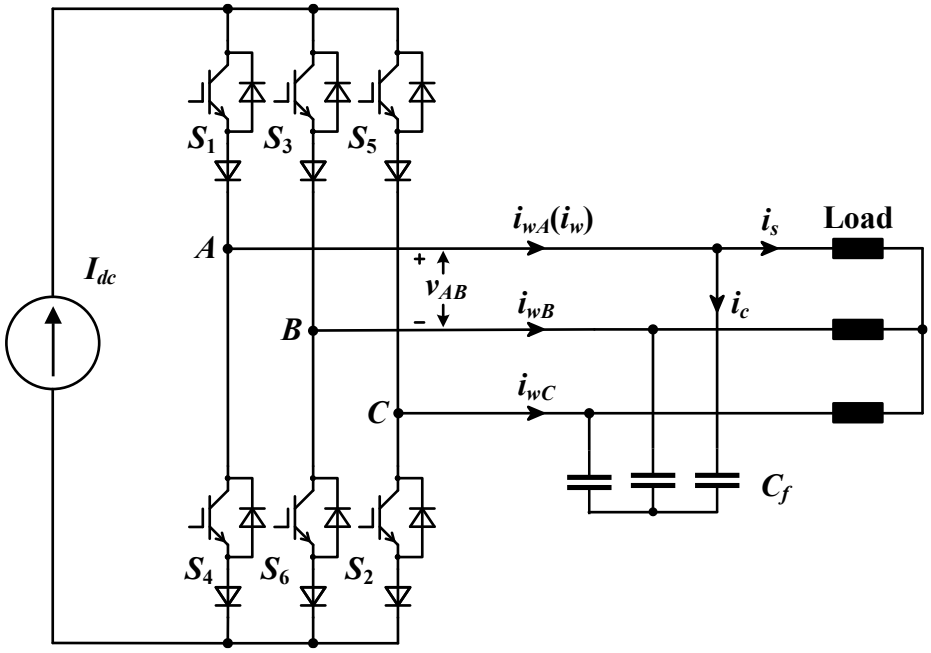

Figure 1-1 The typical three-phase PWM current source inverter [3].

CSIs use switching devices with self-extinguishable capability and these switching devices must have bipolar voltage blocking capability. Before the advent of gate commutated thyristors (GCTs), symmetric gate turn-off thyristors (GTOs) were the main switching device for CSIs. They were gradually replaced by symmetric gate commutated thyristors (SGCTs) which were developed from GTO devices with improved switching characteristics and lower losses. However, SGCTs can hardly be found in the current market. IGBTs and power MOSFETs are advanced switching devices with superior switching characteristics. Both of them need to be connected with diodes in series when used for CSIs. The series-connected diodes provide the reverse voltage blocking capability. Nevertheless, the voltage ratings of power MOSFETs are comparatively low, which limits the application of power MOSFETs. By contrast, the voltage ratings of IGBTs can reach

6500 V [39]. Therefore, IGBTs series-connected with diodes become a promising switching device for CSIs in high power MV applications.

The CSI exhibits several advantages compared with VSIs. It features a simple converter topology since the antiparallel freewheeling diodes are not needed for switching devices. Besides, the high switching *dv/dt* issue in VSIs does not exist in CSIs. The output current and voltage waveforms are close to sinusoidal after being filtered by the capacitor. Furthermore, it has inherent reliable overcurrent and short-circuit protection because the rate of rising of the DC current is limited by the dc choke, which provides sufficient time for protection circuits to work once a short circuit happens at the output terminals. However, the dynamic performance of CSIs is limited since the DC current cannot be changed instantaneously during transients.

1.1.2 Multilevel current source inverter

MCSIs use a couple of inductors to divide the input current into several equal parts to generate multilevel output currents. The topologies of MCSIs can be classified into single-rated inductor MCSIs, multi-rating inductor MCSIs, paralleled H-bridge MCSIs, two-stage MCSIs, buck-boost derived MCSIs, Ćuk-derived MCSIs, and CS-MMCs. Figure 1-2 shows a five-level single-rating inductor MCSI [35]. It is composed of two modules to generate five-level output current waveforms. The number of the output current levels can be increased by employing more modules. The input DC current is equally shared in these modules. There are two inductors used in each module to smooth the current in the module and provide equal impedance among phases. And all the inductors in this topology have the same current rating. The high current capacity, low conduction losses, and good harmonics performance are the main advantages of this topology [21]. However, the unbalancing of the inductor currents is one issue in these modules. Several solutions have been proposed to deal with this issue by improving the modulation schemes or control [33]-[34]. Another challenge is the great number of inductors make the inverter bulky. An improved configuration of the five-level single-rating inductor MCSI is shown in Figure 1-3 [35]. The modified topology employs interphase inductors to replace the single-rating inductors leading to the reduction of current ripples and overall system size.

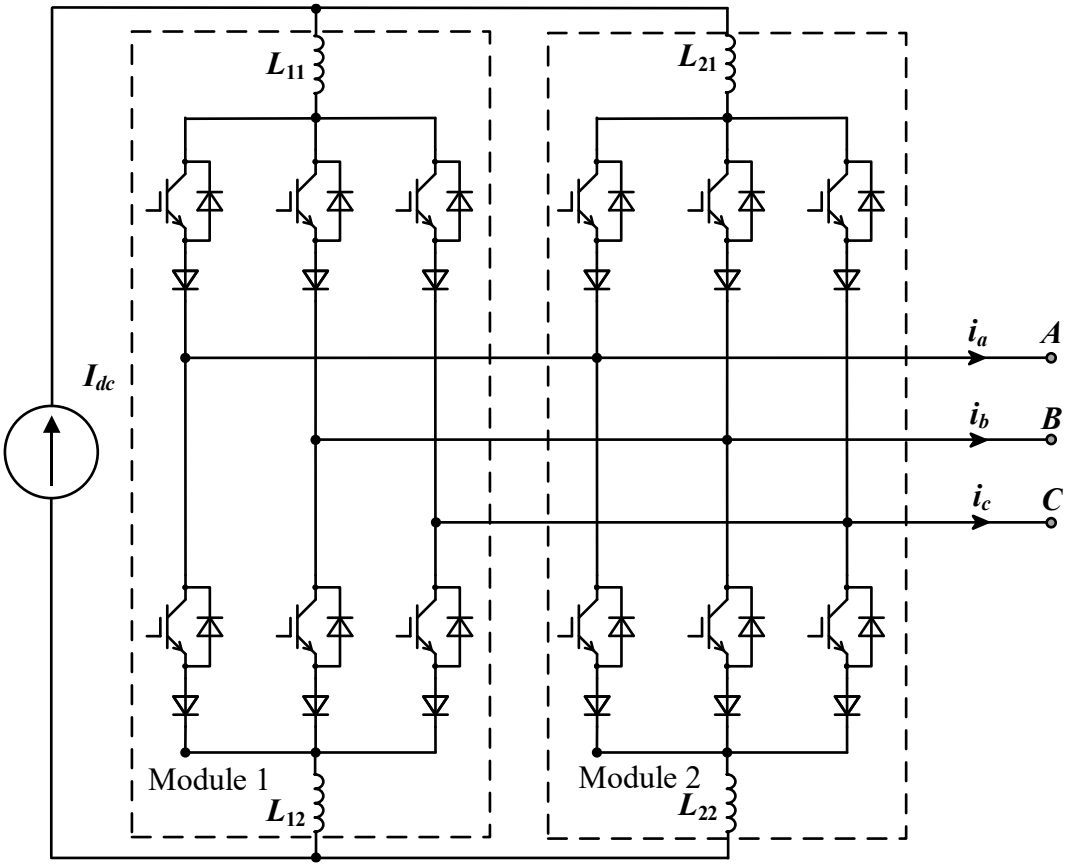

Figure 1-2 Three-phase five-level single-rating inductor CSI with four inductors of the same rating [35].

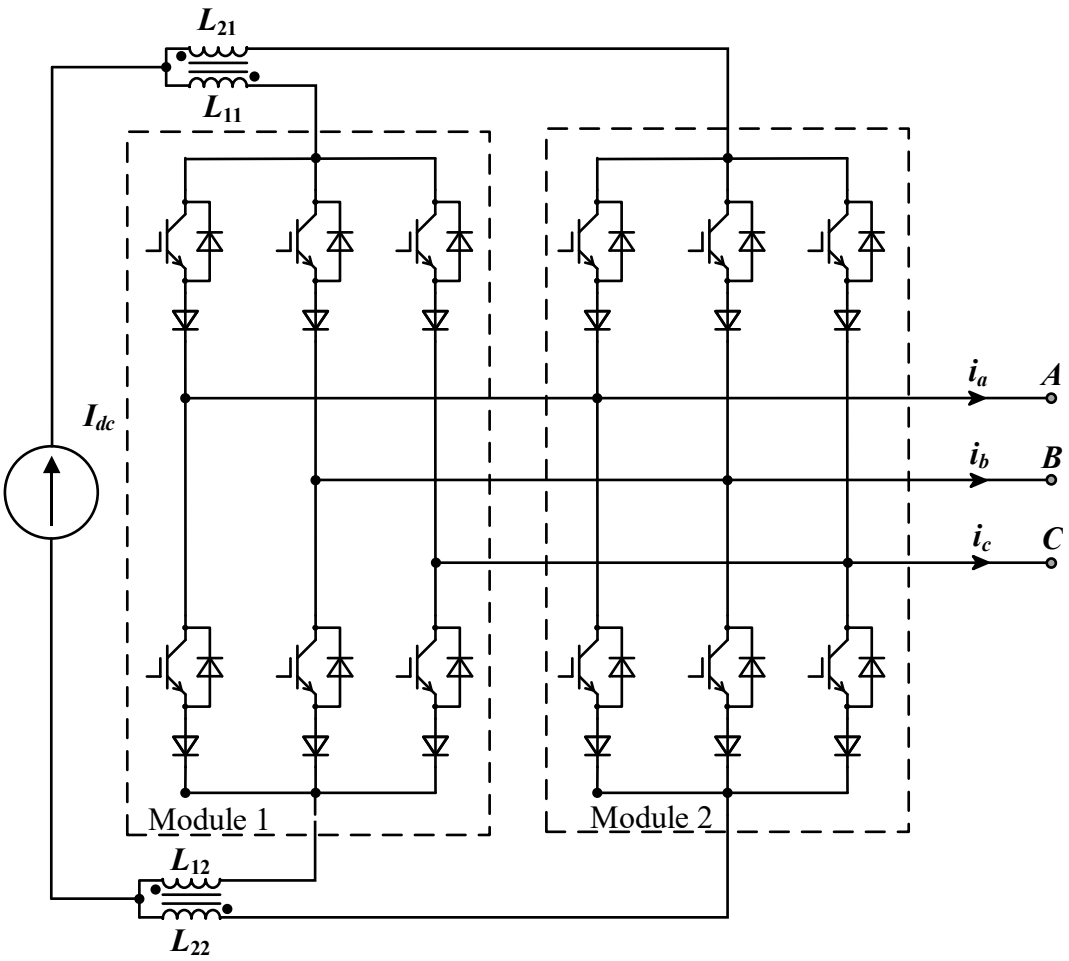

Figure 1-3 Five-level single-rating inductor CSI with two interphase inductors [35].

The topology of a three-phase multi-rating inductor MCSI is shown in Figure 1-4 [22]. It consists of two H6 CSI modules with two multi-rating inductors and can produce five-level current waveforms at the ac output side. The number of the output current levels can be increased by adding more modules and inductors. In this topology, the DC current is divided into different current ratings by these inductors. The inductor current balancing is also an issue in three-phase multi-rating inductor MCSIs. The imbalanced currents can be caused by the mismatched resistances of the inductors. The problem can be solved by utilizing an appropriate modulation technique or applying closed-loop control techniques [36].

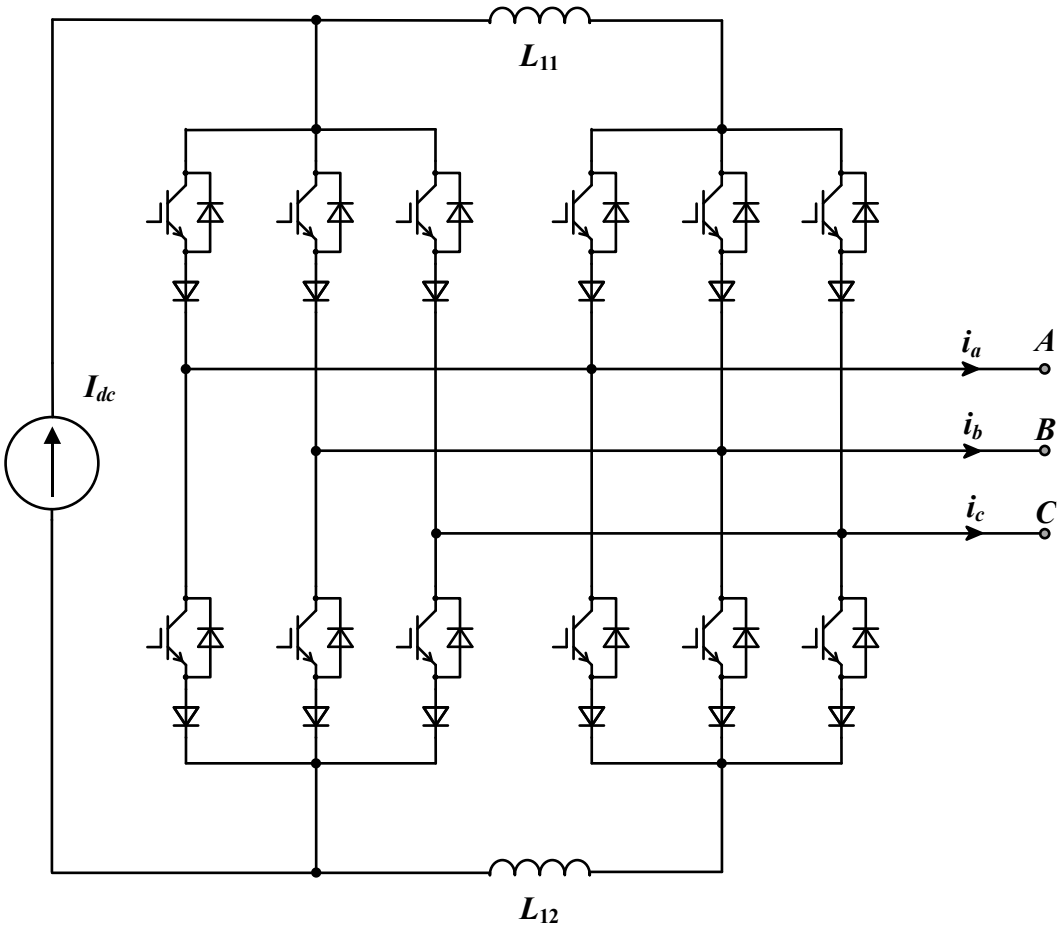

Figure 1-4 Three-phase five-level CSI with two multi-rating inductors [22].

The paralleled H-bridge topology is shown in Figure 1-5 [22]. It is different from the single-rated inductor MCSI and the multi-rating inductor MCSI since it utilizes independent current sources. Therefore, the circulating current and current imbalance issues do not exist in this topology [37]. However, it is complicated to derive multiple current sources, particularly in drive applications [21].

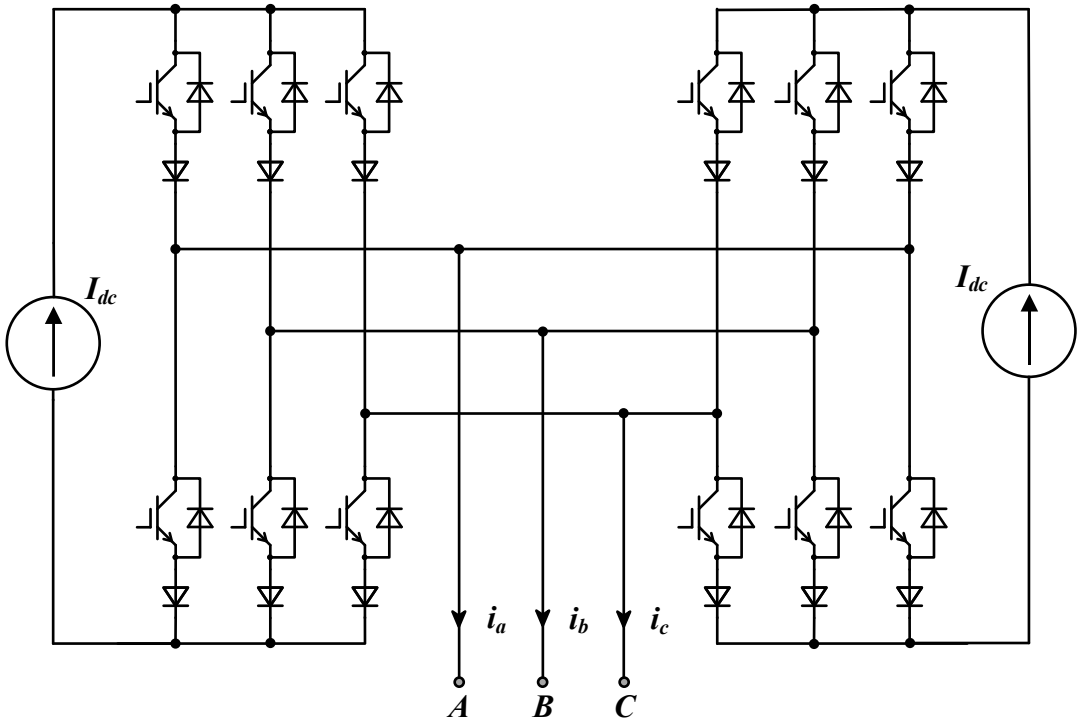

Figure 1-5 Three-phase paralleled H-bridge five-level CSI [22].

Buck-boost derived CSIs are one of the emerging topologies of MCSIs. Different from other MCSIs which aspire to boost the voltage, this topology utilizes the buck-boost technique to extend the operating range. As shown in Figure 1-6 [38], The five-level buck-boost derived CSI consists of a voltage source and two inductors with two CSIs. Two additional semiconductor devices S_W and $S_{W'}$ are employed to isolate the input dc rails preventing the current circulation between the two CSIs.

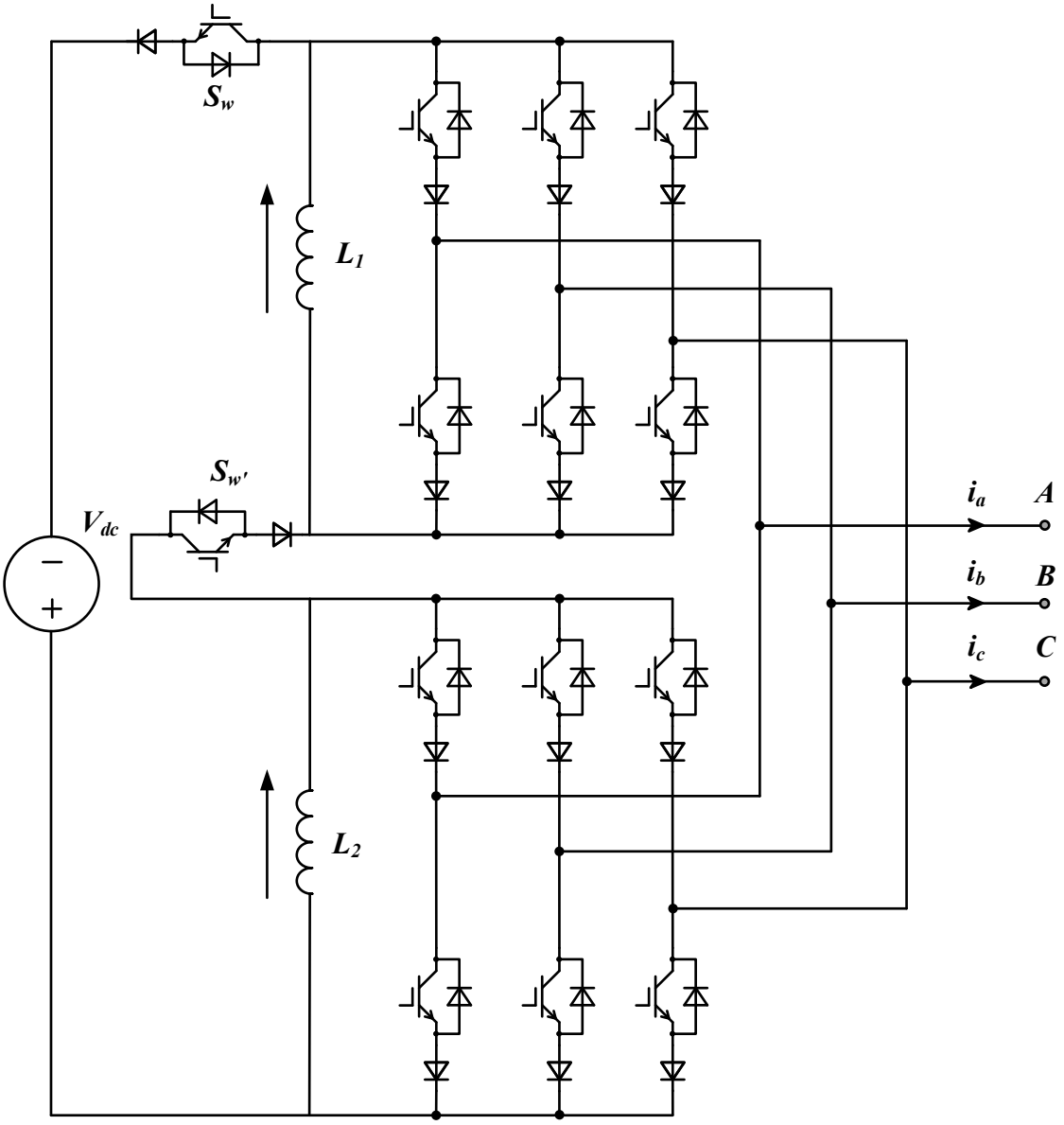

Figure 1-6 Three-phase five-level buck-boost derived multilevel CSI [38].

The two switching devices are turned on or off simultaneously, which leads to discontinuous inductive charging. When they are both turned on, the inductors are charged by the voltage source charges simultaneously resulting in no current flowing through the inverters. When they are both turned off, the proposed CSI can operate in voltage-buck or voltage-boost state as designed, and the circuit operates like the directly cascaded inverter [38]. One advantage of this topology is the dc-link inductor currents are naturally balanced within each switching cycle without additional hardware or control manipulation [22].

Furthermore, the number of the components can be reduced by removing the switch $S_{w'}$ with applying the alternative phase opposition disposition (APOD) modulation [38]. Both input and output performances are not degraded. The modified topology is shown in Figure 1-7 [38].

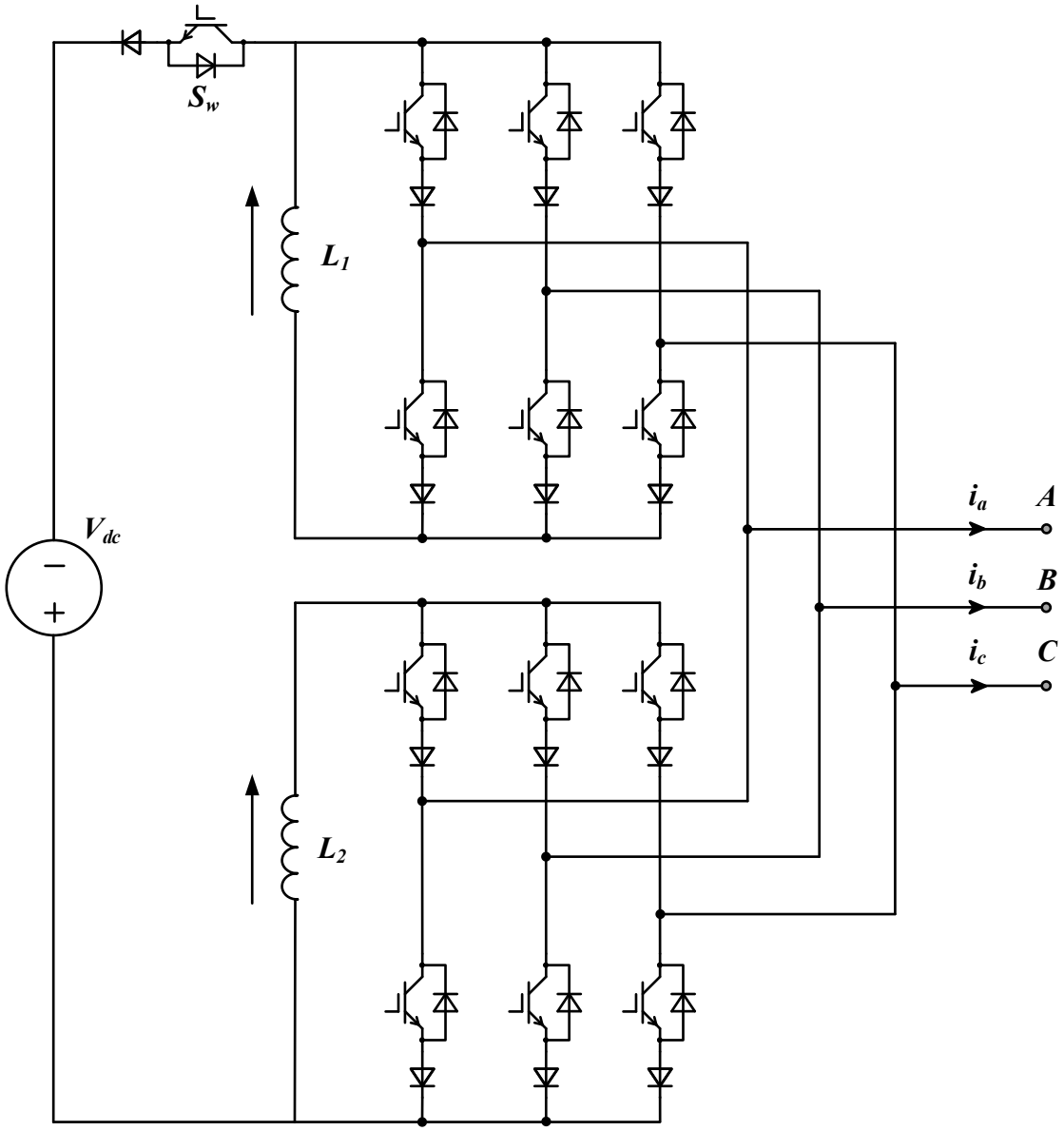

Figure 1-7 Modified five-level buck-boost derived multilevel CSI [38].

To further enhance the current buck-boost capability, the single voltage source can be replaced by a current source parallel-connected with a capacitor which stores inductive

charging energy for DC current boosting. This topology is denominated as Ćuk-derived five-level CSI and is shown in Figure 1-8 [38]. The operational principle for the rear-end inverters in this topology is the same as that in the buck-boost derived CSI, whereas the current boost principles are different [38]. When the switching device *Sw* is off, the current source would charge the capacitor. When *Sw* is on, both the input current and the capacitor current flow through inductors. Therefore, the current stress of the front-end voltage source and the series inductor can be reduced, which is the advantage of this topology [38].

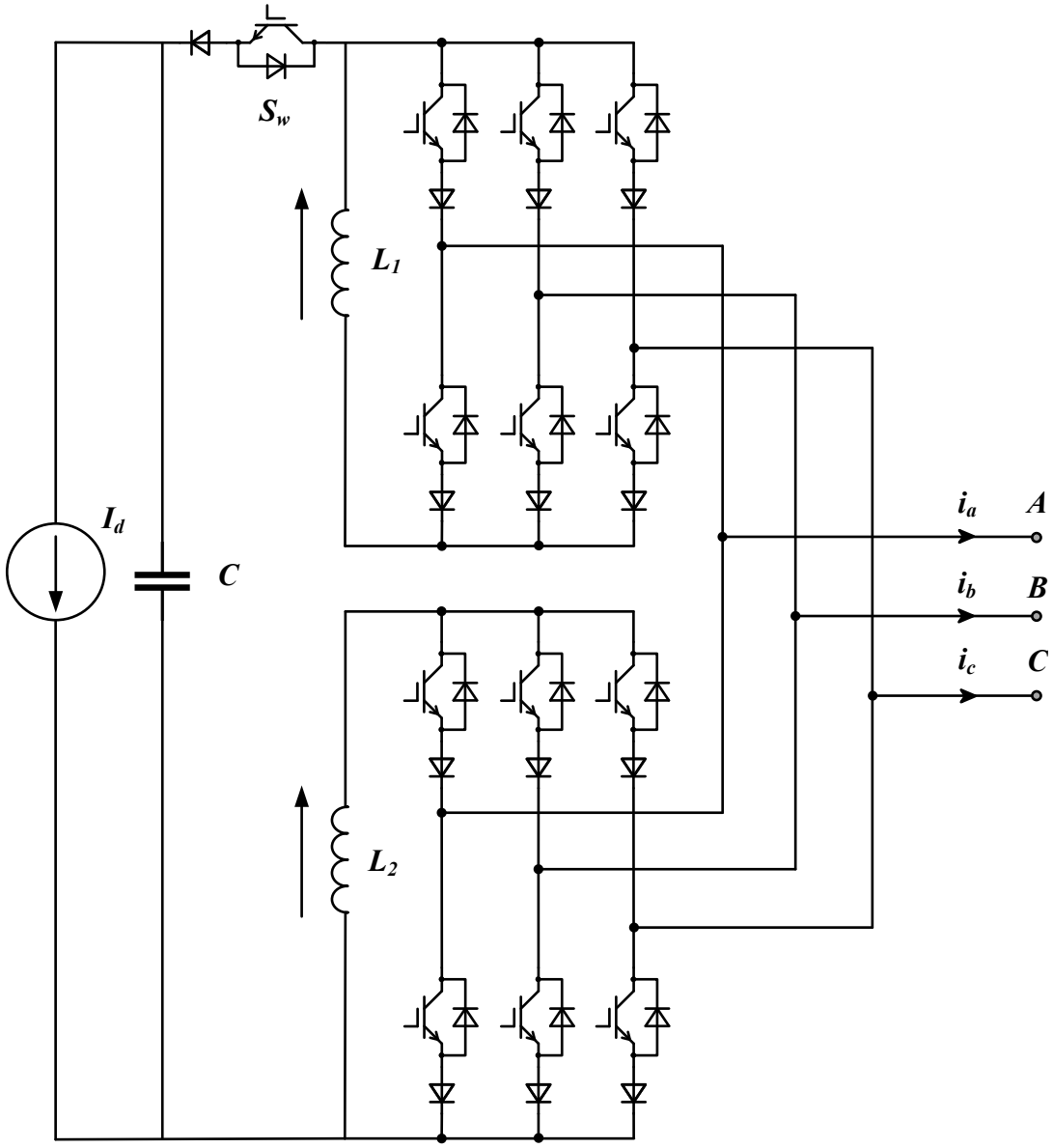

Figure 1-8 Ćuk-derived five-level CSI [38].

The CS-MMC is another topology of MCSIs. Several inductor-based cells are employed in this topology and connected in parallel to produce multilevel output waveforms as shown in Figure 1-9 [35]. The advantage of this topology is its high-power operation capability. However, this topology is costly due to a great number of power devices and inductors.

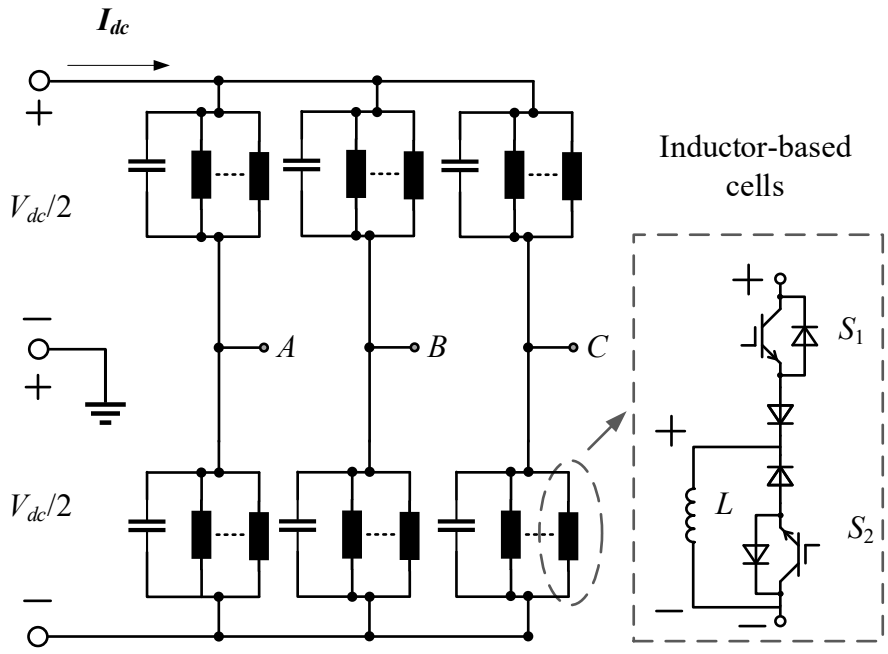

Figure 1-9 Three-phase CS-MMC topology with its inductor-based cells [35].

1.1.3 Parallel current source inverters

In MCSIs, parallel connection is a way to produce more levels of the output current waveforms and improve the power quality. All the topologies mentioned in MCSIs in this thesis can be seen as parallel CSIs. Those topologies connect several CSI modules in parallel except the CS-MMC which utilizes several paralleled inductor-based cells on each arm. Parallel CSIs can also produce three-level output currents by using adequate modulation schemes. Apart from increasing the number of the levels of the output current waveforms to reduce harmonics, the parallel connection also increases the power rating of the inverter since the current stress of the switching devices is shared. The DC source in parallel CSIs can be a single input DC source or several independent input DC sources. One example of the parallel CSIs using two independent current sources is the three-phase paralleled H-bridge five-level CSI which has been shown in Figure 1-5. Different from the topology

presented in Figure 1-5. A new configuration of three-phase parallel CSIs which only employs a single input DC source is shown in Figure 1-10. In this topology, every inverter has its own DC choke. A three-phase filter capacitor is shared by the two inverters at the output. The values of the DC choke must be identical to promise the balanced currents in two inverters.

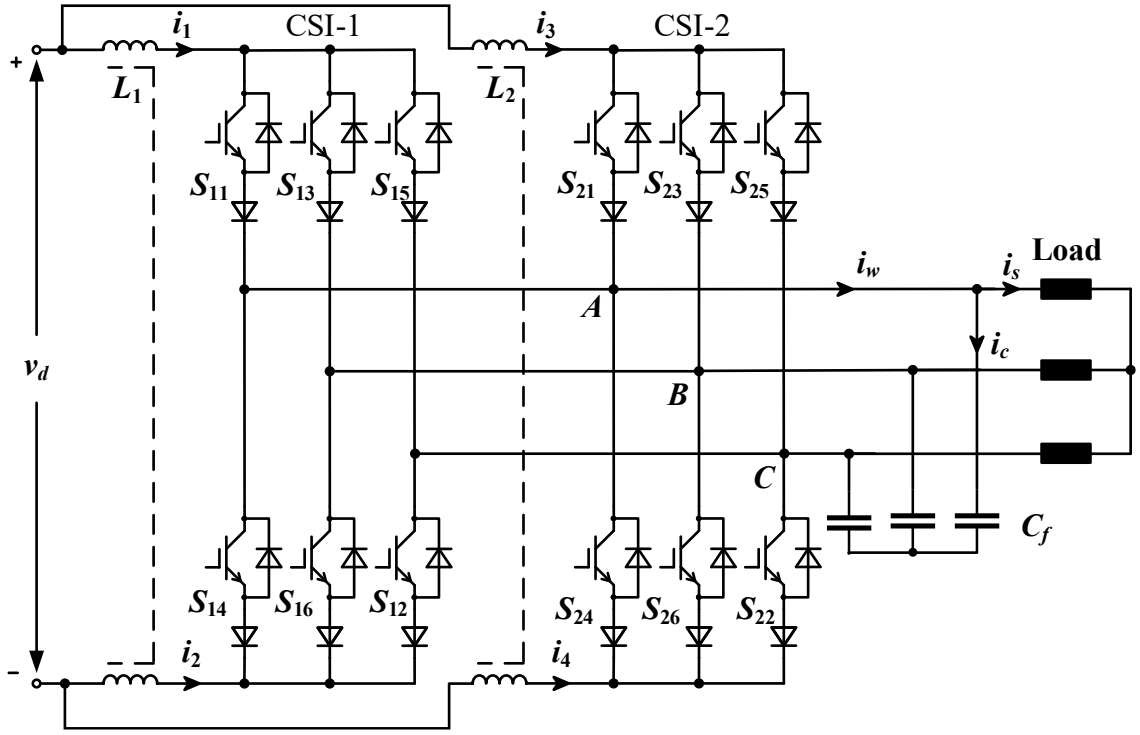

Figure 1-10 Parallel current source inverters with a three-phase load [3].

Parallel CSIs are suitable for high power applications with high current levels. They can be adopted in uninterruptable power system (UPS) applications, such as high-speed elevators, high power electric drives, and distributed generation systems, due to the increased power rating, improved fault tolerance, and high reliability [40]-[43]. However, in practice, unbalanced dc currents are one of the main issues in parallel CSIs. It can be caused by several reasons, including unequal on-state voltages of the semiconductor devices, variations in time delay of the gating signals of the two inverters, and manufacturing tolerance in dc choke parameters. This problem can be solved by using the SVM-based DC current balance control algorithm [23]. And the circulating current may

exist in this topology due to the common input DC source. Besides, the CMV and common-mode (CM) resonances are also the challenges in parallel CSIs. Unfortunately, most methods of CMV suppression reported in the literature focus on single CSI and are not valid for parallel CSIs. Few studies have been done in the literature [24].

1.1.4 Series-connected current source inverters

In addition to the parallel operation for high power applications, several CSIs can also be connected in series to form SC-CSIs to increase the power rating and DC voltage level of the inverter. SC-CSIs have been studied in CSC-based offshore wind farm systems. So far, three topologies of SC-CSIs have been developed in the literature.

(a) Topology A

As shown in Figure 1-11 [31], several identical CSIs are connected in series composing topology A [9], [29]. These CSIs are identical in terms of topology, modulation, and control. Each CSI consists of six switches. The total number of the switches employed in topology A which is constructed by n CSIs is $6n$. The switching frequency of these switches depends on the power rating of each CSI and the employed switching device. For high power applications, such as high-power (megawatt-level) MV drives, the switching frequency is usually limited to around 500 Hz [1]. Besides, a multi-winding transformer is required at the output. The functions of the multi-winding transformer are providing a clear current path for each CSI and stepping up the voltage if necessary.

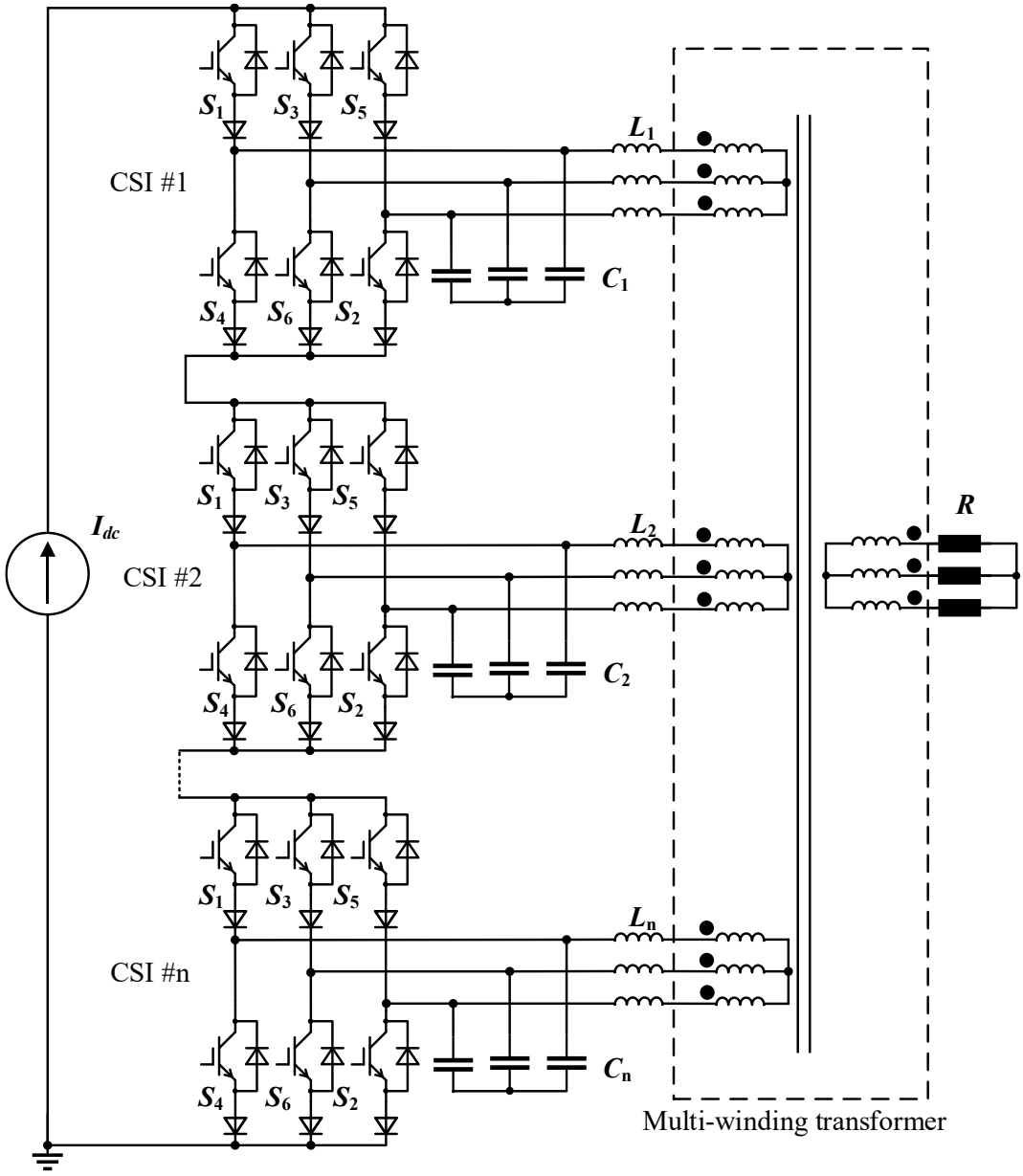

Figure 1-11 Topology A of SC-CSIs [31].

(b) Topology B

In [31], A SC-CSIs with a switching frequency of 60 hertz was proposed. The configuration of this topology is shown in Figure 1-12 [31]. Compared with topology A, the switching frequency of the switches used in topology B is decreased to 60 Hz. However, the low switching frequency results in significant low-order harmonics in the output PWM currents. The significant low-order harmonics can be filtered out by using the combination

of phase-shifting modulation and the phase-shifting transformer. Besides, the LC filter is reduced by utilizing the phase-shifting transformer to eliminate the harmonics. And a reduction in the DC inductor is realized because of the phase-shifting modulation.

Compared with topology A, topology B has several advantages, including lower switching losses, a higher DC current utilization, and reduced passive components. However, the phase-shifting transformer has a complicated winding connection which may increase the cost. Besides, the input current I_{dc} cannot be controlled by the proposed modulation scheme.

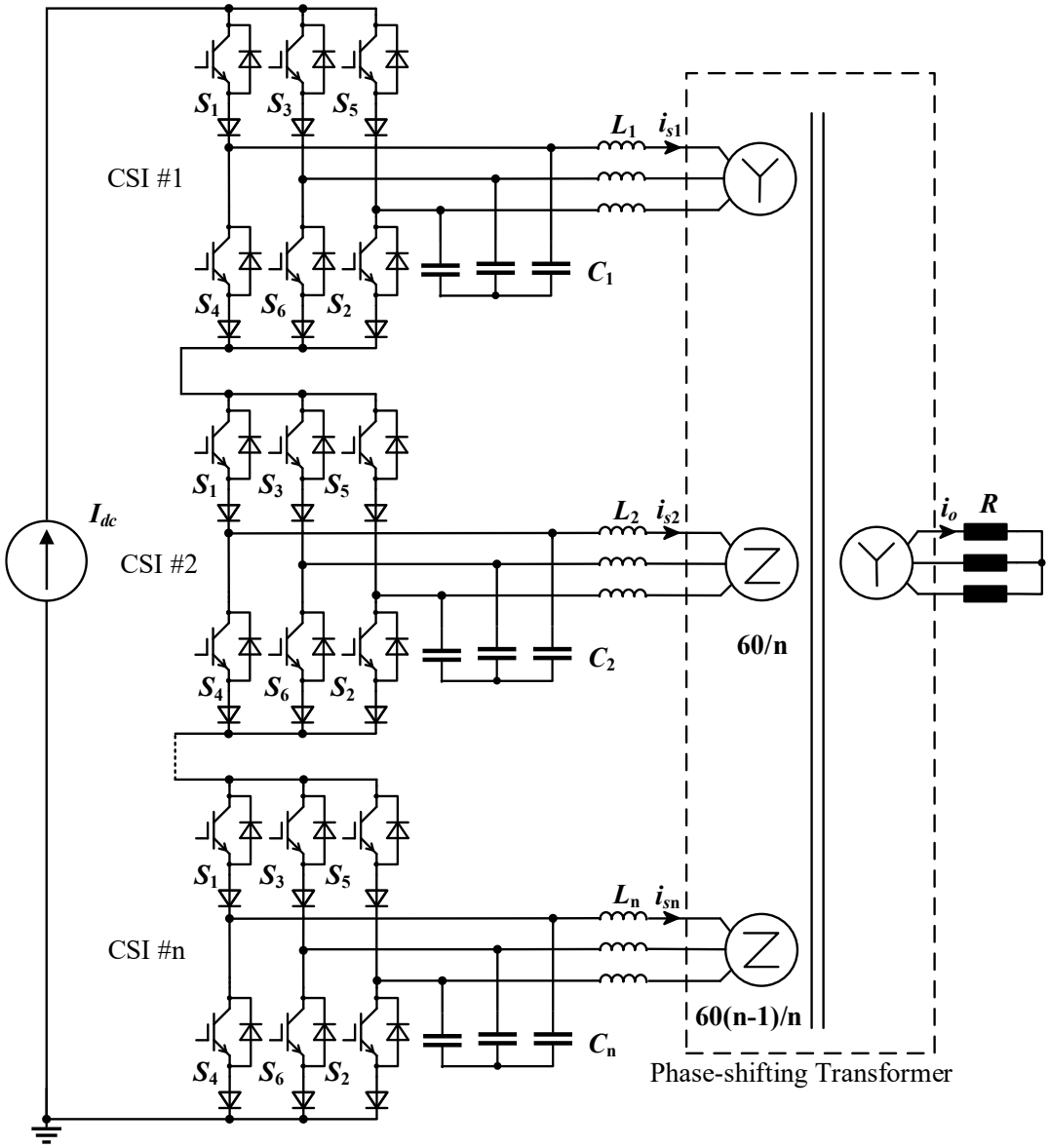

Figure 1-12 SC-CSIs with switching frequency of 60 hertz (topology B) [31].

(c) Topology C

To reduce the number of switching devices, a new topology using fewer switches with a developed modulation scheme was proposed in [32]. The configuration of this topology is presented in Figure 1-13 [32]. In topology C, each CSI is composed of six switches, and adjacent two CSIs share three switches. For example, shown in Figure 1-13, CSI#1 is constructed by the switches S_{11}, S_{12}, S_{13}, S_{21}, S_{22}, and S_{23}, and CSI#2 is formed by the switches S_{21}, S_{22}, S_{23}, S_{31}, S_{32}, and S_{33}. The switches S_{21}, S_{22}, and S_{23} are shared by CSI#1 and CSI#2. Due to this arrangement, the total number of the employed switches is reduced from $6n$ ($n \geq 2$) in topology A to $3(n+1)$ in topology C.

However, the output currents of any two adjacent CSIs have a phase shift of 180° due to the developed modulation scheme. This phase shift can be eliminated by employing a multi-winding transformer that has a different configuration of the inverter-side transformer windings at the output. This transformer is the same as the transformer used in topology A except for the connection of the inverter-side windings. After the transformer, the currents are in phase. Compared with topology A, topology C features fewer switches and lower complexity. The comparison among the three topologies of SC-CSIs is shown in Table 1-1.

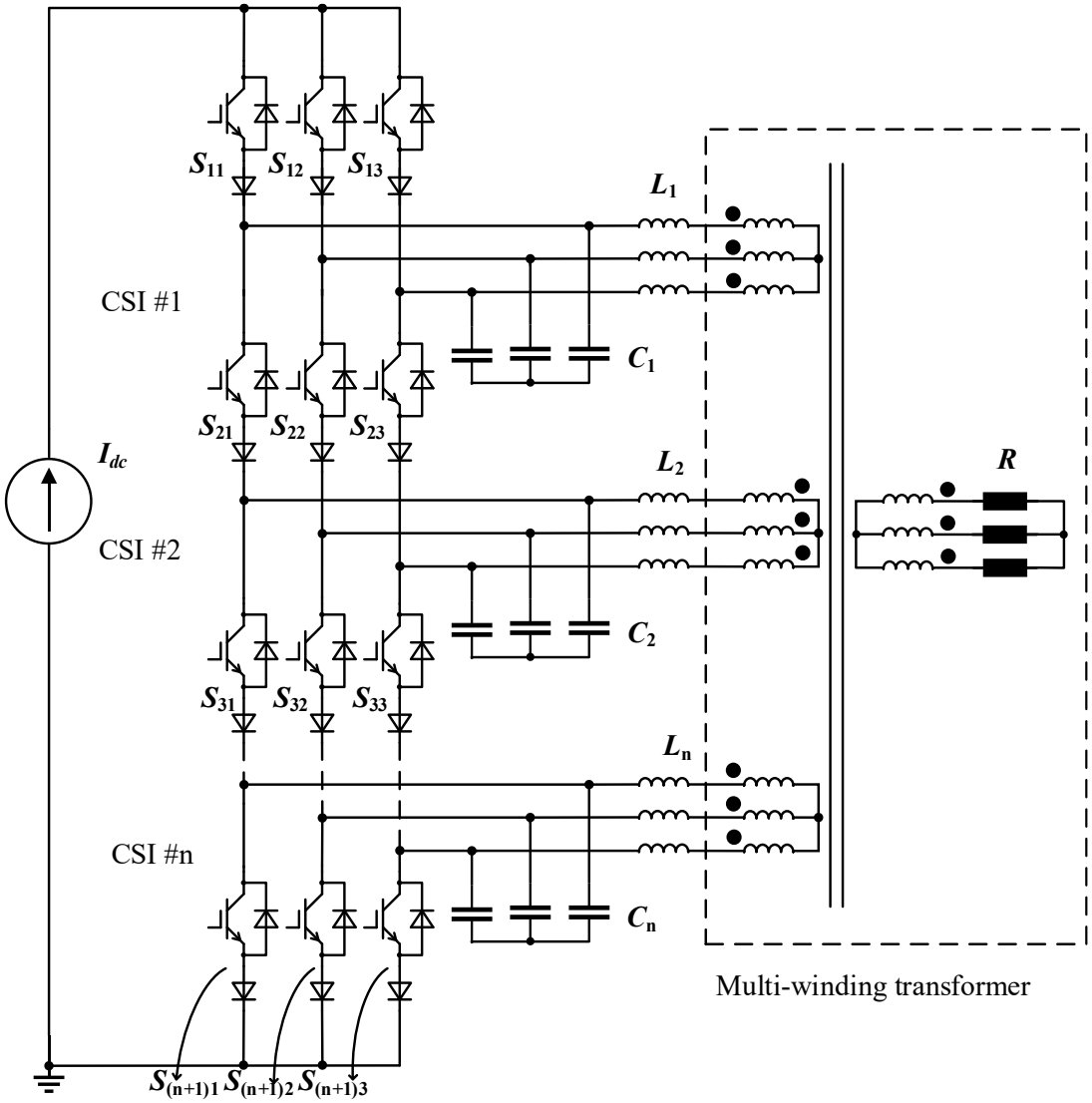

Figure 1-13 Topology C of SC-CSIs [32].

Table 1-1 The comparison among the three topologies of SC-CSIs

Aspect	Topology A	Topology B	Topology C
The number of switches (involving *n* CSIs)	6*n*	6*n*	3(*n*+1)
Output current	In phase	In phase	180° phase shift between adjacent CSIs
Transformer type	Multi-winding	Phase-shifting	Multi-winding
Switching frequency	Around 500 Hz	60 Hz	Around 500 Hz

1.2 Power losses of SC-CSIs.

Among various CSIs, SC-CSIs are suitable for applications with high power ratings and high DC voltage levels. In high power applications, power losses are one of the important attributes of SC-CSIs since they have a significant impact on the efficiency of the system. The fewer power losses of the SC-CSIs lead to the higher efficiency of the system, which can lower the operation cost. Besides, it is very important to figure out the power loss distribution of SC-CSIs to design an appropriate cooling system.

The power losses of SC-CSIs can be influenced by several factors, including the conduction current, the line-to-line voltage, the switching frequency, the modulation scheme, the modulation index, and the characteristics of the switching device, such as the saturation voltage and the turn-on and turn-off energy losses. Some of these factors are different in the three topologies of SC-CSIs, which can result in different total power losses and power loss distributions. Therefore, SC-CSIs in different topologies probably have different efficiencies and power loss distributions.

1.3 Dissertation objectives

As mentioned earlier, the power losses of SC-CSIs are one of the important parameters in high power applications since they are not only related to the efficiency of the system but also crucial for cooling system design. Different topologies of SC-CSIs probably result in different total power losses and power loss distributions. However, it has not been studied which topology of SC-CSIs has the fewest total power losses. Therefore, this thesis aims at investigating the power losses of SC-CSIs and finding out the topology and the modulation scheme that have the best performance in terms of efficiency.

The main objectives of this dissertation are summarized as follows:

(1) Power loss investigation of SC-CSIs.

In Chapter 2, the power losses of the switching device (IGBTs series connected with diodes) will be analyzed. The factors that can influence the power losses of SC-CSIs will be discussed in detail and will be compared in the three topologies of SC-CSIs. The power

loss distribution of each topology will be analyzed. The power losses and the efficiencies of the SC-CSIs in these three topologies will be compared under one typical modulation scheme.

(2) Power loss investigation of SC-CSIs with different modulation schemes.

In Chapter 3, three typical PWM modulation schemes are introduced, including trapezoidal pulse width modulation (TPWM), selective harmonic elimination (SHE), and space vector modulation (SVM). How different modulation schemes influence the power losses of SC-CSIs will be investigated. The power losses and the efficiencies of the SC-CSIs with different modulation schemes will be compared in the three topologies. The topology and the modulation scheme with the lowest power losses will be found out and recommended.

Chapter 2
Power Loss Investigation of Series-Connected Current Source inverters

As mentioned in the previous chapter, power losses are an important attribute of SC-CSIs because they directly affect the efficiency of the system. Besides, it is crucial to figure out the power loss distribution of SC-CSIs to design an appropriate cooling system. So far, three topologies of SC-CSIs have been developed. However, the power losses of SC-CSIs have not been studied yet. Therefore, the objective of this chapter is to investigate the power losses of the SC-CSIs in these three topologies.

This chapter starts with an introduction of the power losses in the switching device, IGBTs connected with diodes in series. Then analyzing the factors that can influence the power losses of the switching device. Each factor is investigated and compared in the three topologies in detail. Finally, the power losses of the SC-CSIs in each topology are analyzed in a comparative method. And the power loss distribution of topology C is figured out. Simulation results are provided to assist and verify the analysis.

2.1 Power losses of IGBTs and diodes

The losses in a semiconductor component, such as an IGBT or a diode, can be classified into conduction losses, switching losses, and blocking (leakage) losses. The blocking losses are normally neglected since the leakage current is negligibly small during the off-state of the device [44]. Only conduction losses and switching losses are considered in the power losses of IGBTs and diodes. Therefore, the total power losses of a switching device are the sum of the conduction losses and the switching losses of the IGBT and the diode.

2.1.1 Conduction losses

Conduction losses are the losses that occur when a semiconductor device is on-state and conducting current. The value of the conduction losses is based on the output characteristic

of the device [45]. The instantaneous value of the conduction losses in an IGBT or a diode can be calculated by [52]

$$P_{CON}(t) = V_{ON}(t) \times I_C(t) \tag{2-1}$$

where V_{ON} is the on-state saturation voltage of the device and I_C is the conduction current. The on-state saturation voltage of an IGBT can be approximated as a DC voltage source, which represents the IGBT on-state zero-current collector-emitter voltage V_{CE0}, connected with a collector-emitter on-state resistance R_C in series. Therefore, the on-state saturation voltage of an IGBT V_{CE} can be approximated as a linear function of the conduction current [52]

$$V_{CE}(I_C) = V_{CE0} + R_C \times I_C \tag{2-2}$$

The same approximation can be used for the series-connected diode [52]

$$V_F(I_C) = V_{F0} + R_D \times I_C \tag{2-3}$$

where V_F is the forward on-state voltage of the diode, V_{F0} is the zero-current on-state voltage, and R_D is the on-state resistance of the diode.

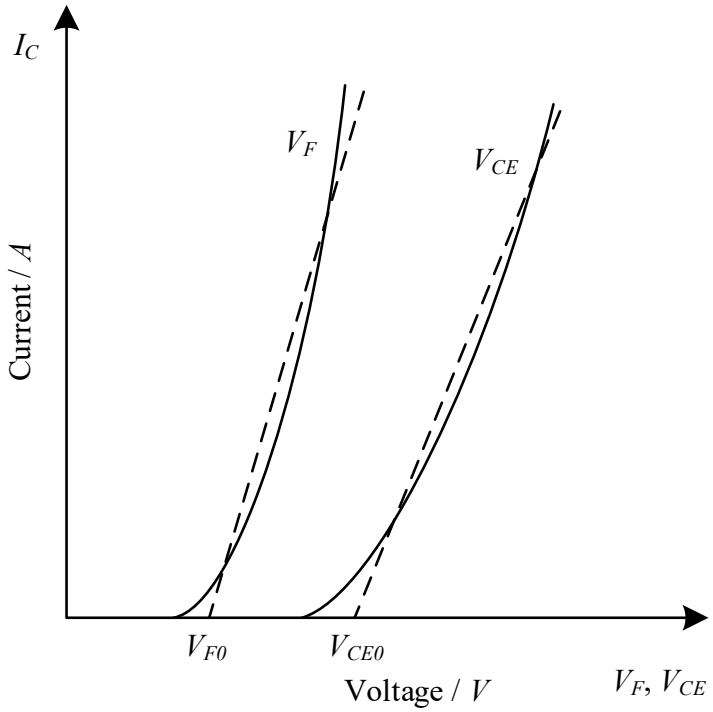

Figure 2-1 Typical output characteristics of IGBTs and diodes [45].

The relation between the instantaneous values of the on-state saturation voltage and the conduction current is the output characteristic of the IGBT or the diode. The typical output characteristics of IGBT and diode are shown in Figure 2-1 [45]. The instantaneous value of the IGBT conduction losses P_{CI} and the instantaneous value of the diode conduction losses P_{CD} can be calculated by [52]

$$\begin{cases} P_{CI}(t) = V_{CE}(t) \times I_C(t) = V_{CE0} \times I_C(t) + R_C \times I_C^2(t) \\ P_{CD}(t) = V_F(t) \times I_C(t) = V_{F0} \times I_C(t) + R_D \times I_C^2(t) \end{cases} \tag{2-4}$$

Therefore, the average value of IGBT conduction losses P_{CIav} and the average value of the diode conduction losses P_{CDav} are [52]

$$\begin{cases} P_{CIav} = \dfrac{1}{T}\displaystyle\int_0^T P_{CI}(t)dt = V_{CE0} \times I_{Cav} + R_C \times I_{Crms}^2 \\ P_{CDav} = \dfrac{1}{T}\displaystyle\int_0^T P_{CD}(t)dt = V_{F0} \times I_{Cav} + R_D \times I_{Crms}^2 \end{cases} \tag{2-5}$$

where I_{Cav} is the average value of the conduction current, and I_{Crms} is the rms value of the conduction current. From the equation (2-5), it can be seen that the total average conduction losses of the switching device depend on the duty cycle, the on-state saturation voltage, and the conduction current.

2.1.2 Switching losses

Switching losses are the power dissipation of a power device during turn-on and turn-off switching transitions. The IGBT switching losses P_{SWI} can be calculated by [32]

$$P_{SWI} = (E_{on} + E_{off}) \times F_{sw} \times \frac{V}{V_{nom}} \times \frac{I}{I_{nom}} \tag{2-6}$$

where E_{on} is the turn-on energy losses per pulse of the IGBT, E_{off} is the turn-off energy losses per pulse of the IGBT, F_{sw} is the switching frequency of the device, V_{nom} and I_{nom} are the rated voltage and current of the IGBT, V and I are the instantaneous values during switching/conducting.

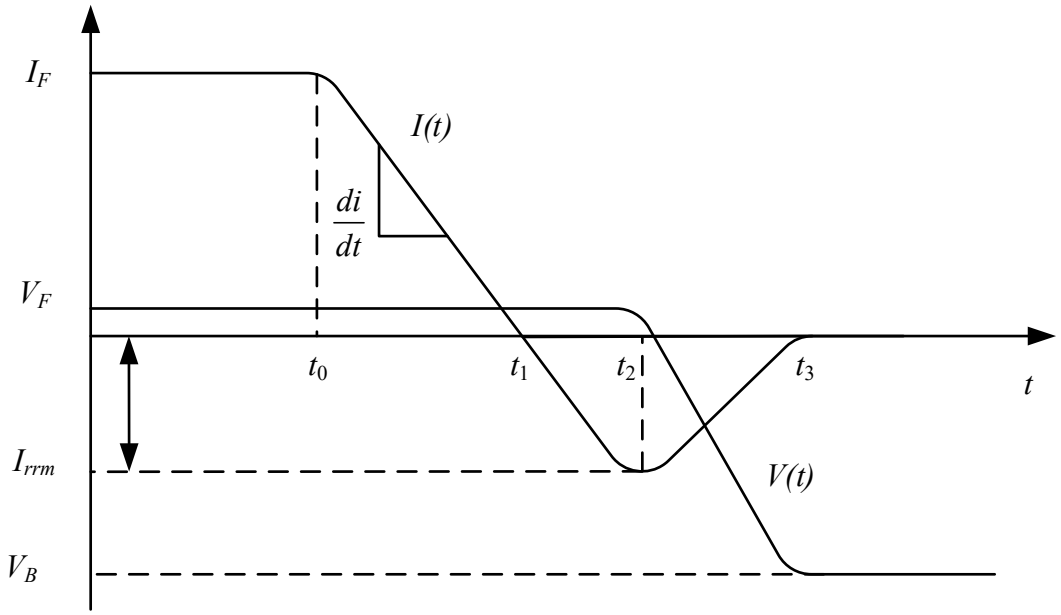

Figure 2-2 The typical power diode current and voltage waveforms during turn-off [47].

When calculating the diode switching losses, the turn-on losses are usually neglected in practice, but the turn-off losses also named reverse recovery losses should be considered due to the reverse recovery current caused by the carrier storage effect [46]. The typical power diode current and voltage waveforms during turn-off are shown in Figure 2-2 [47]. The reverse current reaches its maximum I_{rrm} at t_2. The diode switching losses P_{SWD} can be calculated by [45]

$$P_{SWD} = P_{REC} = E_{rr} \times F_{Doff} \times \frac{V_B}{V_{Bnom}} \tag{2-7}$$

where E_{rr} is the reverse recovery energy losses of the diode, F_{Doff} is the diode turn-off frequency, V_B is the reverse blocking voltage, and V_{Bnom} is the rated reverse blocking voltage. Sometimes, the reverse recovery energy losses E_{rr} are not provided. Alternatively, the figure presents the relationship between the reverse recovery charge Q_{rr} and the current slope di/dt with the forward current I_F is given. In this way, the reverse recovery losses of diodes can be calculated by [46]

$$P_{REC} = k_E \times V_B \times Q_{rr} \times \frac{S}{S+1} \times F_{Doff} \tag{2-8}$$

where Q_{rr} is the recovered charge, S is the reverse recovery softness factor, and k_E is a constant unique to each circuit that compensates for non-ideal voltage switching waveform. The value of k_E is decided by not only the characteristics of the diode but also the commutation circuit [46]. If experimental loss values are available, k_E can be chosen to provide a good match between the calculated and experimental values. If not, k_E can be assumed a value between 0.5 to 1 [46].

2.2 Factors related to power losses

The power losses of the switching device are decided by the current and voltage waveforms of the IGBT and the diode and can be approximately calculated by using the above equations. Under a certain temperature, the power losses of the switching device can be influenced by several factors. The conduction losses of the SC-CSIs can be influenced by the conduction current and the saturation voltage of the switching devices. The switching losses of the SC-CSIs can be affected by the modulation scheme, the modulation index, the switching frequency, the current and voltage of the switching device when switching, and the turn-on and turn-off energy losses of the switching devices.

2.2.1 Modulation scheme

The switching pattern of the switching device is decided by the applied modulation scheme. In other words, the applied modulation scheme determines when the switches should be turned on and off. For high power CSIs operating with a switching frequency of around 500 Hz, three typical PWM schemes have been developed, including TPWM, SHE, and SVM [3]. Different modulation schemes have different principles to generate various gating signals. These different gating signals influence the switching moments and lead to different current and voltage waveforms of the switching device, which can result in different power losses. For example, different turn-on and turn-off moments may lead to different instantaneous values of the voltage on the switching device, which can affect the IGBT switching losses shown in equation (2-6). How the different modulation schemes influence the power losses of SC-CSIs will be analyzed in chapter four in detail. To make

SC-CSIs with different topologies have the same operating conditions, one modulation scheme SVM with switching sequence 1 (SQ1) is used in topology A and C in this chapter. Since topology B operates with a fundamental switching frequency of 60 Hz, the modulation proposed in [31] is adopted in topology B.

2.2.2 Modulation index

Modulation index m_a is an important part of modulations. It is defined by

$$m_a = \frac{\hat{I}_{w1}}{I_{dc}} \tag{2-9}$$

where $\hat{I}_{w1}$ is the peak value of the fundamental frequency component in the output PWM current i_w, and I_{dc} is the value of the input DC current. The CSI output currents can be directly controlled by adjusting modulation index m_a. However, this method is rarely used because it causes additional power losses due to the bypass operation [3]. In practice, the CSI output currents are regulated by controlling the input DC current through the front-end rectifiers. Therefore, to lower the power losses, the modulation index m_a is set to its maximum value of 1 in this thesis.

2.2.3 Switching frequency

Switching frequency has a significant impact on switching losses. It can be seen from equations (2-6) and (2-7) that a higher switching frequency results in more switching losses. In the industry, the switching frequency of CSIs for high-power applications is usually limited to around 500 Hz to reduce the switching losses and satisfy the thermal requirements [3]. In this thesis, a switching frequency of 540 Hz is adopted in topology A and topology C. The switching frequency in topology is reduced to 60 Hz as introduced in Chapter 1.

2.2.4 Conduction current

As shown in equations (2-5) and (2-6), both the conduction losses and the switching losses of a switching device can be affected by the conduction current I_c. The power losses

of the SC-CSIs will increase if raising the conduction current. In the three topologies of SC-CSIs, all the CSIs are connected in series and every CSI satisfies the switching constraint to operate normally. At any instant of time (excluding commutation intervals) only two switches are conducting in a CSI, one in the top half of the bridge and the other in the bottom half [3]. Therefore, every switching device in these three topologies has the same conduction current, which is equal to the dc-link current I_{dc}.

2.2.5 Voltage stress of the switching devices

Switching devices will produce more switching losses when they are suffering higher voltage stress during switching/conducting. This can be seen from equations (2-6) and (2-7). To illustrate the voltage stress of the switches in these topologies, the equivalent circuits of topology A and topology C under one switching state are presented. The equivalent circuit of topology B is the same as topology A. The voltage stress of these switching devices under other switching states is the same as the one illustrated here.

As shown in Figure 2-3, switches S_1 and switches S_6 are conducting. The voltage stress of the switch S_3 in CSI # 1 is V_{a1b1}. In CSI # 2, the voltage stress of the switch S_3 is V_{a2b2}. Since the CSIs are identical in topology A, they have the same output line-to-line voltage.

$$V_{a1b1} = V_{a2b2} = V_{anbn} \tag{2-10}$$

Therefore, all the switches S_3 have the same voltage stress, which is the output line-to-line voltage. The same conclusion can be found in other switches in topology A under different switching states. Since all the switches in topology A have the same voltage stress, conduction current, and switching frequency, they generate the same power losses. The same conclusion can be found in topology B.

The equivalent circuit of topology C is shown in Figure 2-4. The voltage stress of the switches on the first and last rows (S_{11}, S_{12}, S_{13} and S_{31}, S_{32}, S_{33}) is the same as that in topology A, which is also the output line-to-line voltage. However, the voltage stress of the inner switches in topology C is double. For instance, the voltage stress of the switch S_{12} in topology C is V_{a1b1}, which is the output line-to-line voltage. The voltage stress of the switch S_{21} in topology B is V_{a1a2}. Note that there is a 180° phase shift between any two adjacent

CSIs in topology C due to the modified modulation scheme. The voltage stress of the switch S_{21} is the twice output line-to-line voltage. The same result can also be found in any other inner switches in topology C.

$$\begin{cases} V_{a1a2} = V_{a1b1} + V_{b2a2} \\ V_{b2a2} = V_{a1b1} \\ V_{a1a2} = 2V_{a1b1} \end{cases} \tag{2-11}$$

The identical IGBTs and diodes can be used in topology A and on the first and last rows in topology C due to the same conduction current and voltage stress, whereas the IGBTs and diodes with the double-voltage rating should be chosen as the inner switches in topology C since the voltage stress of its inner switches is twice that of other switches.

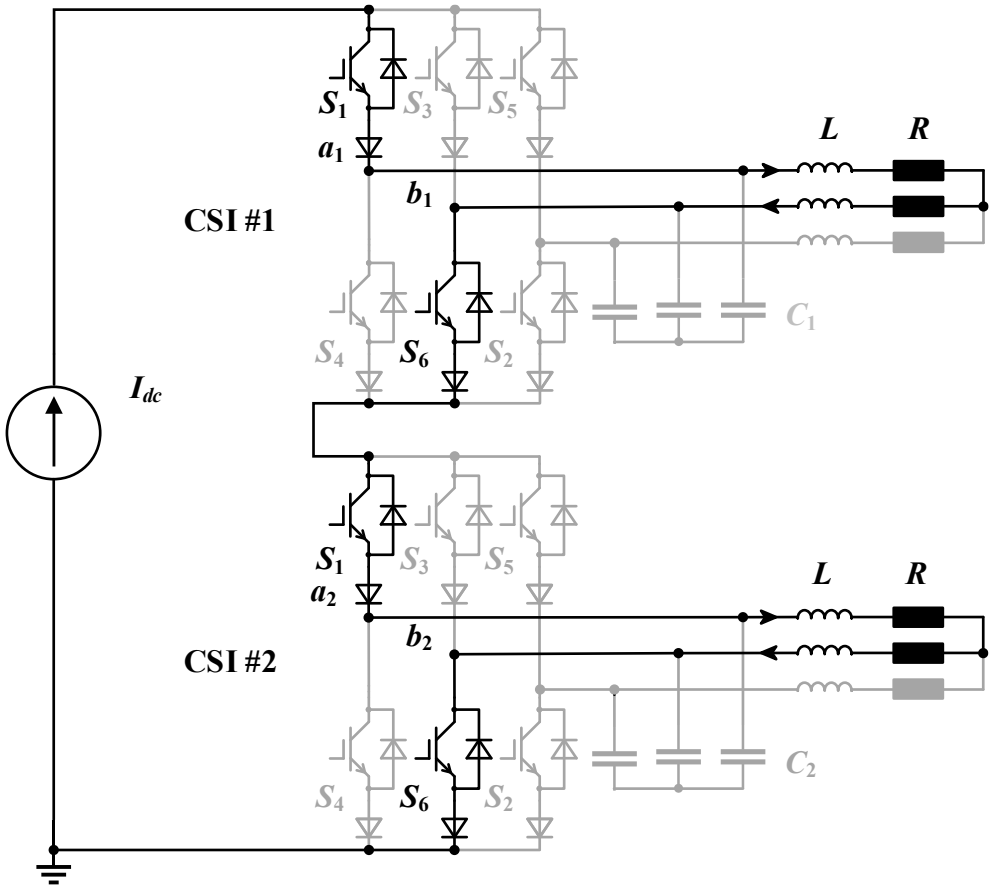

Figure 2-3 The equivalent circuit of SC-CSIs in topology A [32].

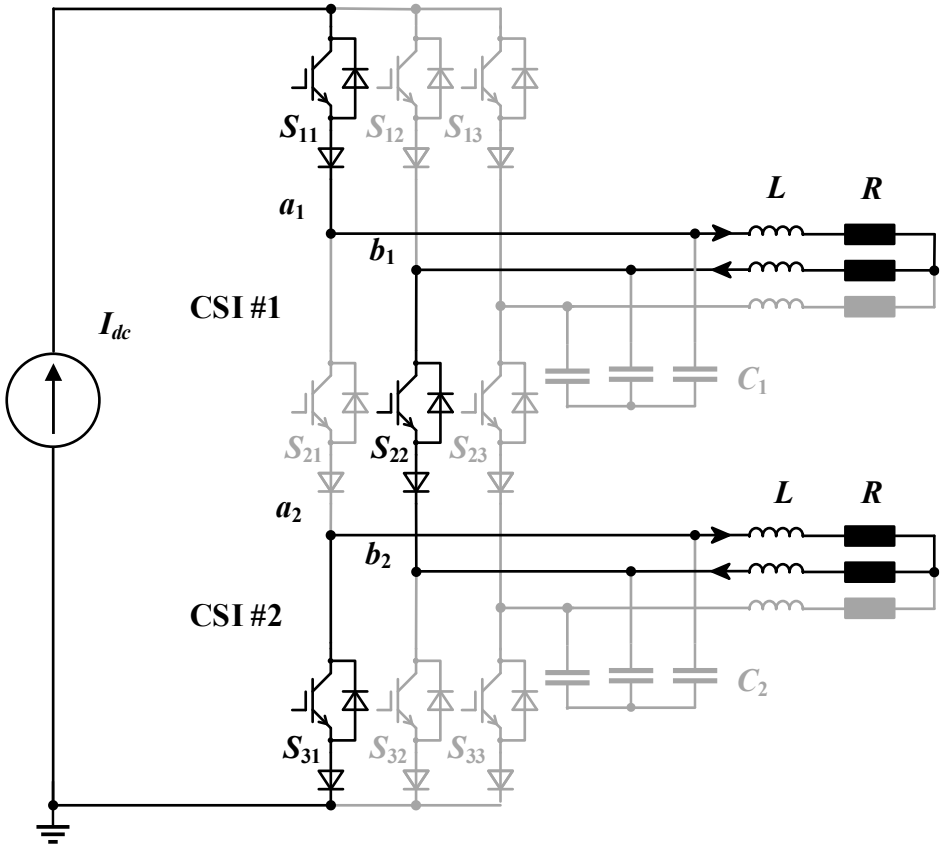

Figure 2-4 The equivalent circuit of SC-CSIs in topology B [32].

2.2.6 Characteristics of the switching device

As analyzed before, the conduction losses of IGBTs and diodes are related to their output characteristics. Besides, the switching losses of IGBTs can be affected by the turn-on and turn-off energy. And the switching losses of diodes can be influenced by the reverse recovery energy. Under the same current rating, switching components with a higher voltage rating usually have a higher saturation voltage V_{on}. Nevertheless, the saturation voltage V_{on} of the IGBT with the double voltage rating is less than twice that of the IGBT with the original voltage rating. This can also be found in power diodes. The value of V_{on} is ranging from 3 to 4.2 V for 6600 V IGBTs, 2.4 to 3.28 V for 3300 V IGBTs, and 1.95 to 2.45 V for 1700 V IGBTs [39].

However, the turn-on energy losses E_{on} and the turn-off energy losses E_{off} of the IGBT with the double voltage rating are approximately three to six times that of the IGBT with the original voltage rating. For example, a comparison of turn-on energy losses E_{on} and the

turn-off energy losses E_{off} between a 3300 V IGBT and a 6500 V IGBT is shown in Figure 2-5 [49], [50]. The IGBTs have the same current rating of 1000 A. With a conduction current I_c of 500 A, the sum of the turn-on energy losses E_{on} and the turn-off energy losses E_{off} of the 6500V IGBT is around 6.1 J, which is approximately triple that of the 3300V IGBT. Furthermore, the recovered charge Q_{rr} of the diode with the double-voltage rating is usually more than that in the diode with the original voltage rating.

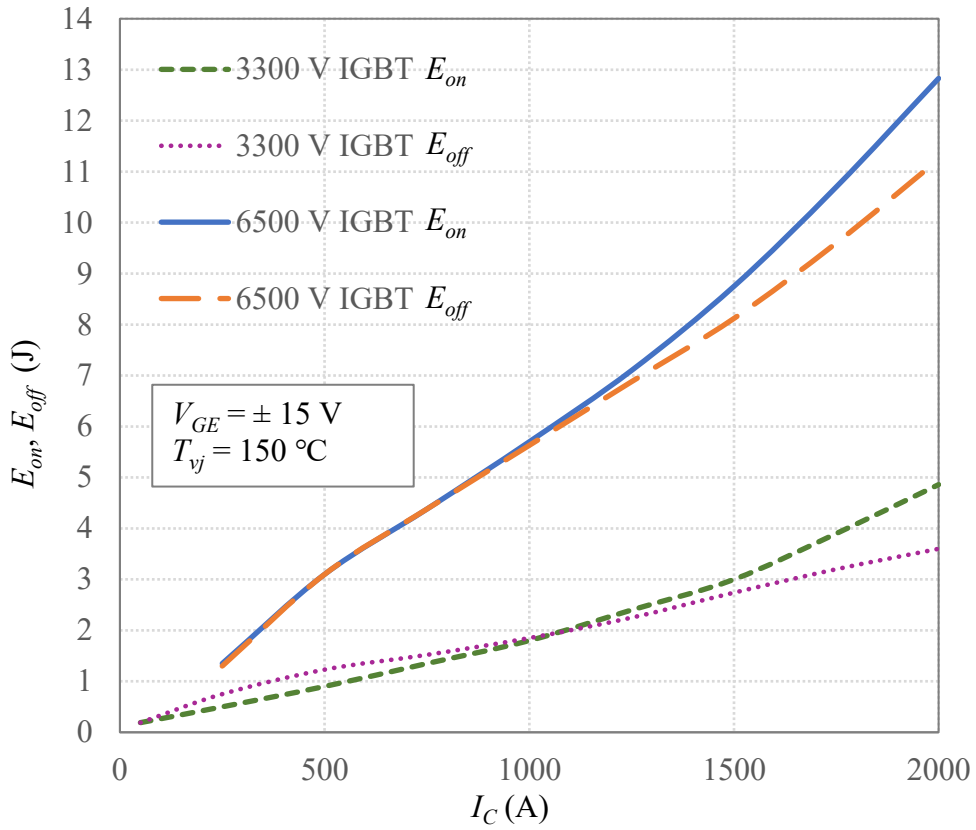

Figure 2-5 The turn-on energy losses E_{on} and the turn-off energy losses E_{off} of the IGBTs [49], [50].

2.3 Total power losses and power loss distribution

Under the same operating conductions, the factors analyzed above are the same in topology A and topology B except modulation schemes and switching frequencies. The switching devices are identical in topology A and topology B with the same conduction current and duty cycle. Thus, topology B has the same conduction losses as topology A.

Whereas the switching losses are reduced by nine times in topology B since the switching frequency is reduced from 540 Hz in topology A to 60 Hz in topology B. The power losses of topology B can be figured out if knowing the conduction losses and switching losses of topology A. Therefore, the following analysis is mainly focusing on the comparison between topology A and topology C.

When the SC-CSIs in topology A and topology C operate under the same conditions, every switch on the first and last rows in both topology A and topology C produces the same power losses. However, the total power losses of the inner switches in these two topologies are different because of the different voltage stresses, characteristics, and quantities. Therefore, to compare the total power losses of these topologies, the power losses of inner switches are crucial.

2.3.1 Total power losses comparison

Firstly, the total conduction losses of the inner switches in topology C are fewer than that in topology A. This is because:

1) The number of the inner switches is halved in topology C.

2) The saturation voltage V_{on} of the switch with the double-voltage rating is less than twice that of the switch with the original voltage rating.

Secondly, the total switching losses of the inner switches in topology C are more than that in topology A. The reasons are:

1) The number of inner switches is halved in topology C.

2) The voltage stress of each inner switch in topology C is twice that of any inner switch in topology A.

3) The turn-on energy losses E_{on} and the turn-off energy losses E_{off} of the IGBT with the double voltage rating are approximately three to six times that of the IGBT with the original voltage rating when they have the same current rating. Moreover, the recovered charge Q_{rr} of the diode with the double voltage rating is more than that in the diode with the original voltage rating.

2.3.2 Power loss distribution

In topology A, every switch has the same power losses since they are identical and have the same condition current, voltage stress, and switching frequency. The same power loss distribution can be found in topology B. However, the power loss distribution in topology C is different. In topology C, every inner switch generates more power losses than any switch on the first and last rows. This is because the voltage stress of the inner switch is doubled. Moreover, the inner switch has a higher saturate voltage V_{on}, more turn-on energy losses E_{on}, and more turn-off energy losses E_{off} than the switch on the first and last rows.

2.4 Simulation investigation

To verify the analysis and compare the total power losses among the SC-CSIs in the three topologies. A simulation investigation is conducted. The simulation models are built based on PSIM_2021a. The simulation parameters of the SC-CSIs are presented in Table 2-1. Each SC-CSIs consists of two PWM CSIs, and each CSI is loaded with a three-phase balanced inductive load. The inductors are employed as the leakage inductance from the transformers. Filter capacitors are employed at the output side of each inverter to assist the commutation of the switching devices and filter out harmonics. The filter capacitor is larger in topology B to filter out the significant low-order harmonics.

Table 2-1 Simulation parameters of the SC-CSIs

Parameters	Topology A and topology C	Topology B
DC link current (A)	500	500
Line voltage (V_{rms})	1150	1150
Number of CSIs	2	2
Modulation scheme	SVM (SQ1)	Square-wave operation
Modulation index	1	1
Switching frequency (Hz)	540	60
Resistance (pu)	1	1
Inductance (pu)	0.1	0.1
Capacitance (pu)	0.3	0.5

The parameters are the same in each topology to promise the SC-CSIs in the three topologies operating under the same conditions except the filter capacitance, the modulation scheme, and the switching frequency in topology B since topology B operates with a switching frequency of 60 Hz. The SVM (SQ1) scheme is used in topology A and topology C. The square-wave operation is adopted in topology B.

The switching device employed in topology A and topology B is formed by using a 3300 V IGBT connected with a 3200 V diode in series. This switching device is also used on the first and last rows in topology C. Besides, A 6500 V IGBT connected with a 6500 V diode in series is employed as the inner switch for topology C due to the double voltage stress. The parameters of the employed IGBTs and diodes in topology A are shown in Table 2-2. The same components are used in topology B as well. The parameters of the employed IGBTs and diodes in topology C are shown in Table 2-3. The IGTBs and diodes are from different manufacturers since the diodes with the matching power ratings cannot be found in the same manufacturer. Considering a 50% margin of safety, the line-to-line voltage of the SC-CSIs and the DC-link current are set up as 1150 V and 500 A respectively. The simulation circuits of topology A, topology B, and topology C are shown in Figure 2-6, Figure 2-7, and Figure 2-8 respectively.

Table 2-2 Parameters of the employed IGBTs and diodes in topology A

Switch number	$\boldsymbol{S_{11}, S_{12}, S_{13}, S_{14}, S_{15}, S_{16}, S_{21}, S_{22}, S_{23}, S_{24}, S_{25}, S_{26}}$	
Part Number	5SNA1000N330300	D850N32T
Device type	IGBT	Diode
Manufacturer	ABB	Infineon
Voltage rating (V)	3300	3200
Current rating (A)	1000	850
V_{CE0}, V_{F0} (V)	1.3	0.84
R_C, R_D (mΩ)	1.96	0.49
E_{on} (J)	0.9	N/A
E_{off} (J)	1.23	N/A
Q_{rr} (mAs)	N/A	5

Table 2-3 Parameters of the employed IGBTs and diodes in topology C

Switch number	S_{11}, S_{12}, S_{13}, S_{31}, S_{32}, S_{33}		S_{21}, S_{22}, S_{23}	
Part Number	5SNA1000N 330300	D850N32T	5SNA1000G 650300	D711N68T
Device type	IGBT	Diode	IGBT	Diode
Manufacturer	ABB	Infineon	ABB	Infineon
Voltage rating (V)	3300	3200	6500	6500
Current rating (A)	1000	850	1000	770
V_{CE0}, V_{F0} (V)	1.3	0.84	2.14	0.84
R_C, R_D (mΩ)	1.96	0.49	2.29	0.87
E_{on} (J)	0.9	N/A	3.13	N/A
E_{off} (J)	1.23	N/A	3.13	N/A
Q_{rr} (mAs)	N/A	5	N/A	5.1

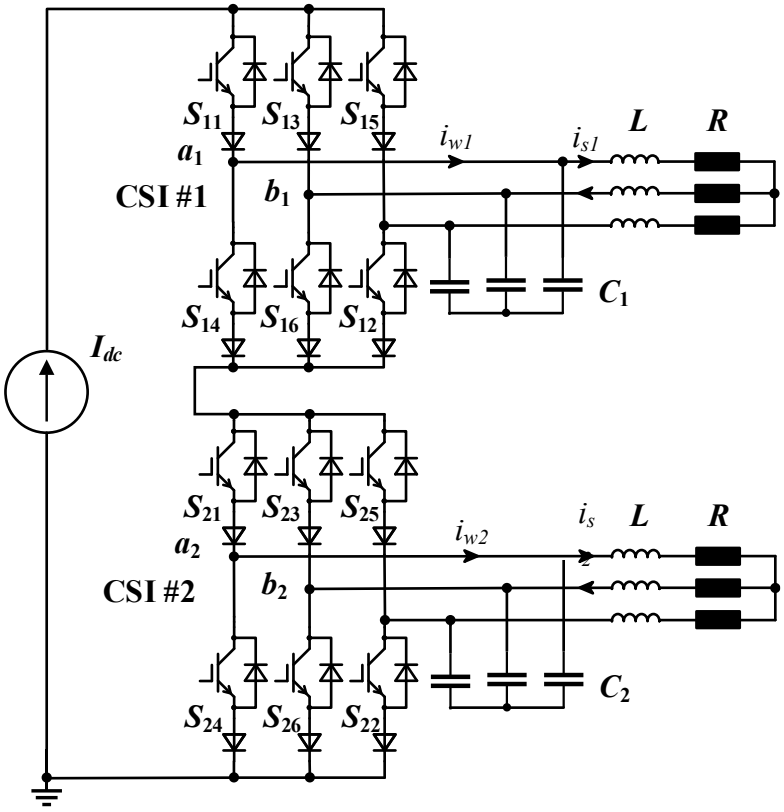

Figure 2-6 Simulation circuit of topology A.

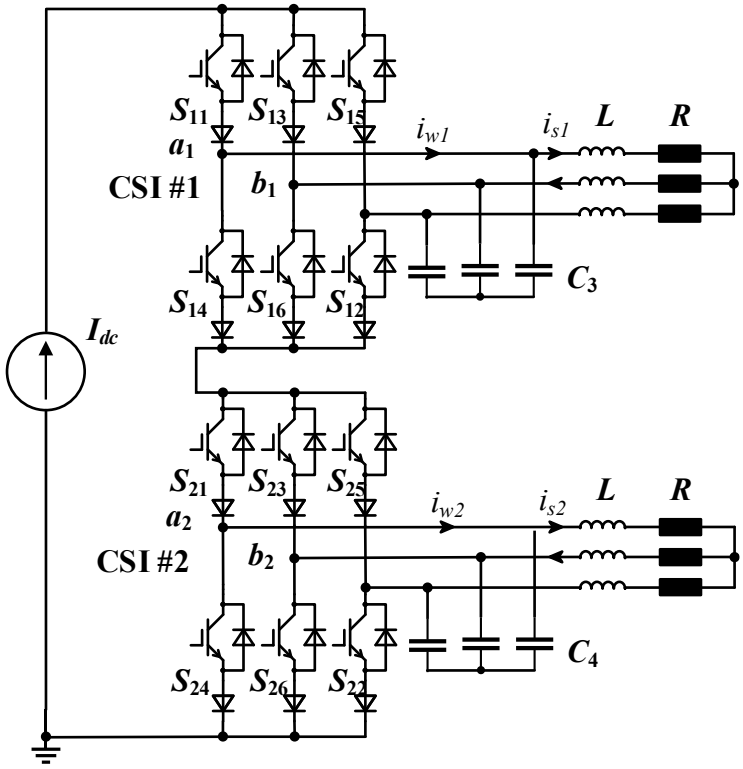

Figure 2-7 Simulation circuit of topology B.

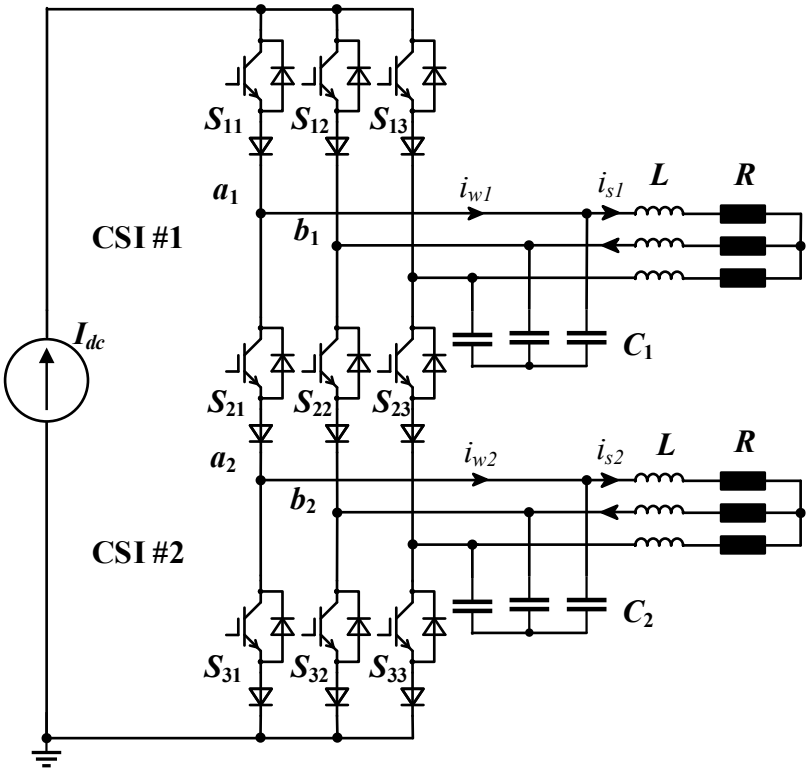

Figure 2-8 Simulation circuit of topology C.

2.4.1 Simulation results

(a) Topology A

The simulated input current I_{dc}, output PWM current i_w, and output current i_s of each CSI in topology A are shown in Figure 2-9. The top one presents the currents in CSI #1, and the bottom one shows the currents in CSI #2. It can be seen that the output currents of CSI #1 and CSI #2 are in phase. The input current I_{dc} is shown in blue which is 500A. The output PWM current i_w shown in green has nine pulses during each half cycle of the fundamental period since the SVM with SQ1 scheme with a switching frequency of 540 Hz is adopted. The output current i_s presented in red is the current after the filter. It is close to a sinusoidal wave with an amplitude of 500A since the modulation index is 1.

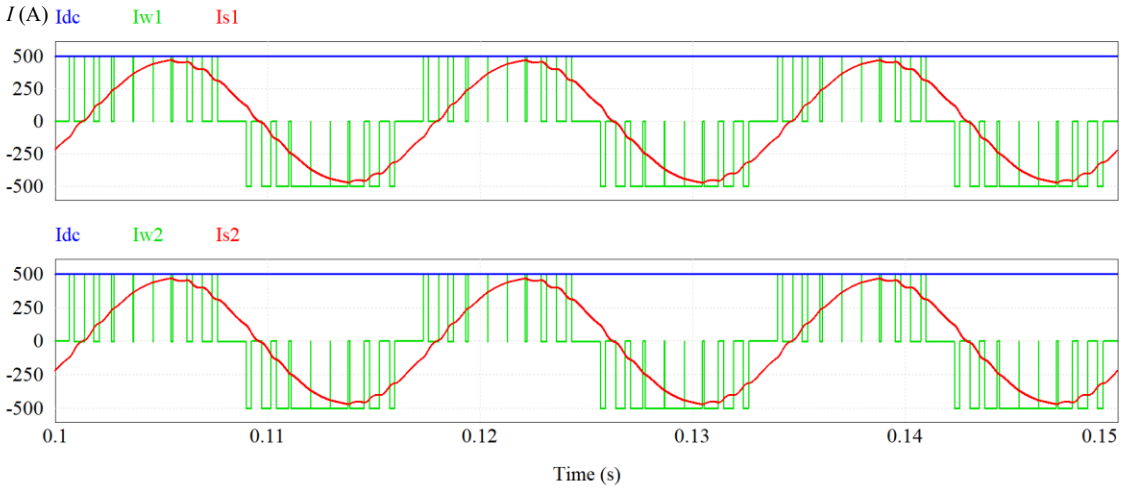

Figure 2-9 Simulated currents in topology A.

The simulated power losses of the switching device S_{11} in topology A are shown in Figure 2-10. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses are shown in blue, and the switching losses are shown in red. The simulated power losses of any other switching devices are the same as that of the switching device S_{11} in topology A. The result shows the conduction losses are the main losses in the IGBT, whereas the switching losses are the primary losses in the diode. The IGBT generates more losses than the diode.

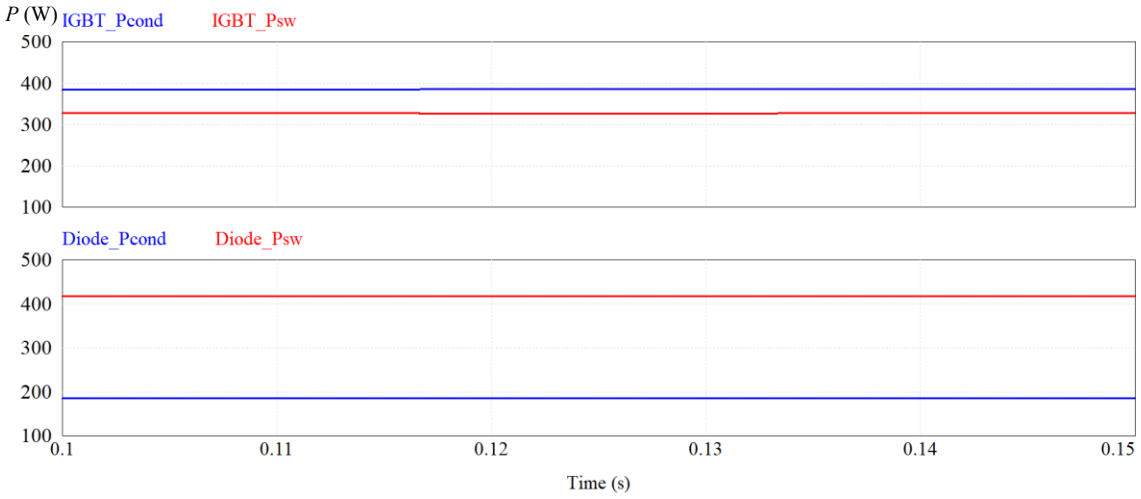

Figure 2-10 Simulated power losses of the switching devices in topology A.

The simulated conduction losses and switching losses of each switching component in topology A are shown in Table 2-4. The result shows that each switching device (an IGBT connected with a diode in series) has the same power losses leading to an even power loss distribution in topology A. Besides, IGBTs produce more losses than diodes in topology A. The power losses generated by IGBTs account for 52.8% of the total power losses in topology A. Furthermore, the switching losses are higher than the conduction losses in topology A. 58.5% of the total power losses in topology A are switching losses.

Table 2-4 Simulated power losses of the switching devices in topology A

Device		**Conduction losses (W)**	**Switching losses (W)**	**Power losses (W)**
S_{11}	IGBT	385.21	342.31	727.52
	Diode	186.00	463.83	649.83
S_{12}	IGBT	385.56	342.39	727.95
	Diode	186.16	463.98	650.14
S_{13}	IGBT	385.56	341.84	727.40
	Diode	186.16	463.16	649.32
S_{14}	IGBT	385.91	341.79	727.70
	Diode	186.33	464.34	650.67
S_{15}	IGBT	386.25	341.99	728.24
	Diode	186.50	464.50	651.00
S_{16}	IGBT	385.56	342.60	728.16

	Diode	186.16	463.79	649.95
S_{21}	IGBT	385.21	342.31	727.52
	Diode	186.00	463.78	649.78
S_{22}	IGBT	385.56	342.39	727.95
	Diode	186.16	463.92	650.08
S_{23}	IGBT	385.56	341.84	727.40
	Diode	186.16	463.11	649.27
S_{24}	IGBT	385.91	341.79	727.70
	Diode	186.33	464.29	650.62
S_{25}	IGBT	386.25	341.99	728.24
	Diode	186.50	464.45	650.95
S_{26}	IGBT	385.56	342.60	728.16
	Diode	186.16	463.73	649.89
Total		6862.72	9672.72	16535.44

(b) Topology B

The simulated currents in topology B are shown in Figure 2-11. The result shows that the output currents of CSI #1 and CSI #2 have a phase shift of 30° due to the phase-shifting modulation. The input current I_{dc} showed in blue is 500A. The output PWM current i_w shown in green is a three-level square wave with an amplitude of 500 A. The output current i_s is presented in red. It is close to a sinusoidal wave with an amplitude of 500A, but it is not as good as the i_s in topology A since the switching frequency is reduced to 60 Hz.

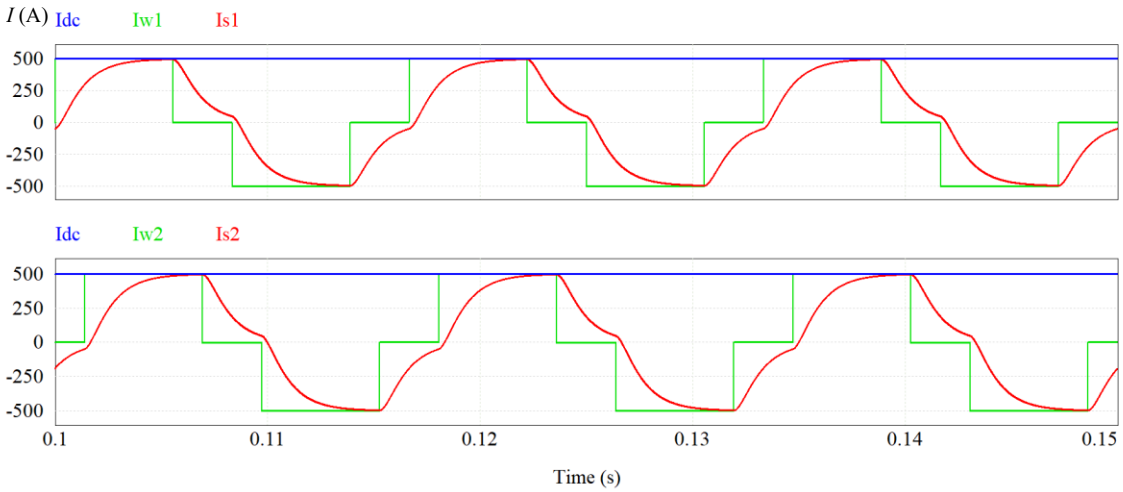

Figure 2-11 Simulated currents in topology B.

The simulated power losses of the switching device S_{11} in topology B are shown in Figure 2-12. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses are shown in blue, and the switching losses are shown in red. The simulated power losses of any other switching devices are the same as that of the switching device S_{11} in topology B. The result shows the switching losses are lower than the conduction losses in both the IGBT and the diode. The IGBT generates more losses than the diode.

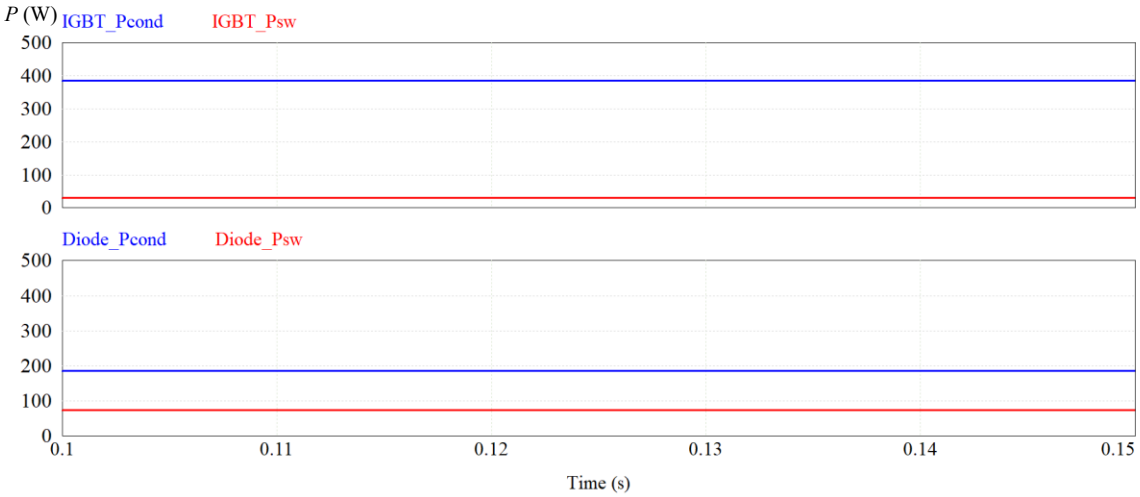

Figure 2-12 Simulated power losses of the switching devices in topology B.

The simulated conduction losses and switching losses of each switching component in topology B are shown in Table 2-5. The result shows that each switching device has the same power losses leading to an even power loss distribution in topology B. Besides, IGBTs have higher power losses than diodes in topology B. The power losses generated by IGBTs account for 61.6% of the total power losses in topology B. Furthermore, the switching losses are much lower than the conduction losses in topology B, which only account for 15.3% of the total power losses in topology B. Moreover, compared with topology A, topology B has the same conduction losses but fewer switching losses. This is because the switching frequency is reduced in topology B.

Table 2-5 Simulated power losses of the switching devices in topology B

Device		Conduction losses (W)	Switching losses (W)	Power losses (W)
S_{11}	IGBT	385.56	30.12	415.68
	Diode	186.16	73.32	259.48
S_{12}	IGBT	385.56	30.12	415.68
	Diode	186.16	73.08	259.24
S_{13}	IGBT	385.56	30.12	415.68
	Diode	186.16	73.38	259.54
S_{14}	IGBT	385.56	30.12	415.68
	Diode	186.16	73.14	259.30
S_{15}	IGBT	385.91	30.12	416.03
	Diode	186.33	72.90	259.23
S_{16}	IGBT	385.91	30.12	416.03
	Diode	186.33	73.02	259.35
S_{21}	IGBT	385.56	30.12	415.68
	Diode	186.16	73.20	259.36
S_{22}	IGBT	385.56	30.12	415.68
	Diode	186.16	72.96	259.12
S_{23}	IGBT	385.56	30.12	415.68
	Diode	186.16	73.26	259.42
S_{24}	IGBT	385.56	30.12	415.68
	Diode	186.16	73.02	259.18
S_{25}	IGBT	385.91	30.12	416.03
	Diode	186.33	73.14	259.47
S_{26}	IGBT	385.91	30.12	416.03
	Diode	186.33	72.90	259.23
Total		6862.72	1238.76	8101.48

(c) Topology C

The simulated input current I_{dc}, output PWM current i_w, and output current i_s of each CSI in topology C are shown in Figure 2-13. The result illustrates that the output currents of CSI #1 and CSI #2 have a phase shift of 180° due to the modified SVM scheme in topology C. The input current I_{dc} presented in blue is 500A. The output PWM current i_w shown in green

has nine pulses during each half cycle of the fundamental period. The output current i_s shown in red is close to a sinusoidal wave with an amplitude of 500A.

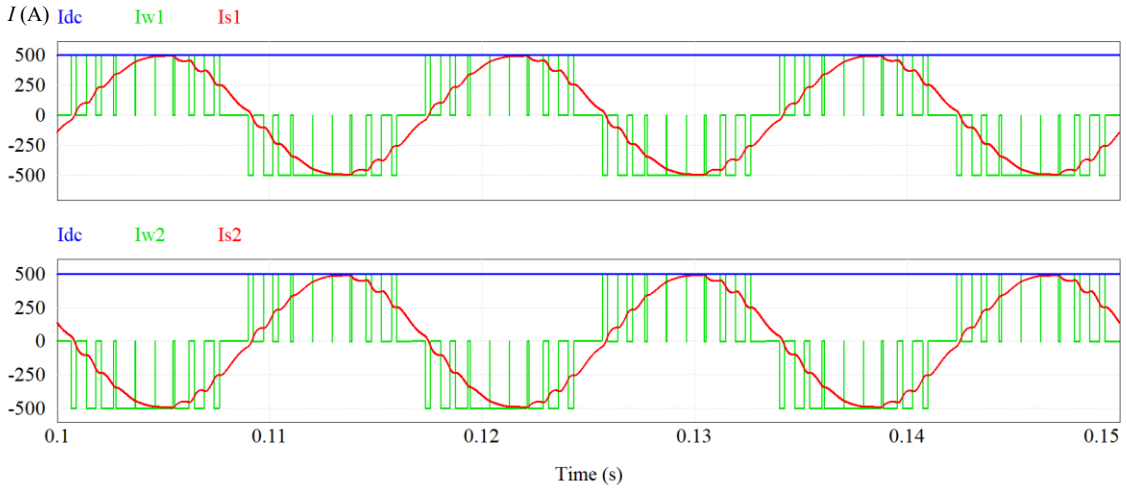

Figure 2-13 Simulated currents in topology C.

The simulated power losses of the switching devices S_{11} and S_{21} in topology C are shown in Figure 2-14. S_{11} is the switch on the first row and S_{21} is an inner switch in topology C. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses of the 3300 V device (S_{11}) and the 6500 V device (S_{21}) are shown in blue and green respectively. The switching losses of the 3300 V device and the 6500 V device are shown in red and pink respectively. As shown in Figure 2-14, the power losses of the 3300 V IGBT and the 6500 V IGBT are different. A similar result can be found in the diodes. The devices with a voltage rating of 6500 V are employed as the inner switches in topology C due to the double voltage stress. It can be seen from the simulated result that topology C has a different power loss distribution from topology A and topology B. Besides, the switching losses of the 6500 V IGBT are more than twice that of the 3300 V IGBT. And the conduction losses of the 6500 V IGBT are less than twice that of the 3300 V IGBT. These can also be found when comparing the power losses between the 6500 V diode and the 3300 V diode. These results are consistent with the analysis.

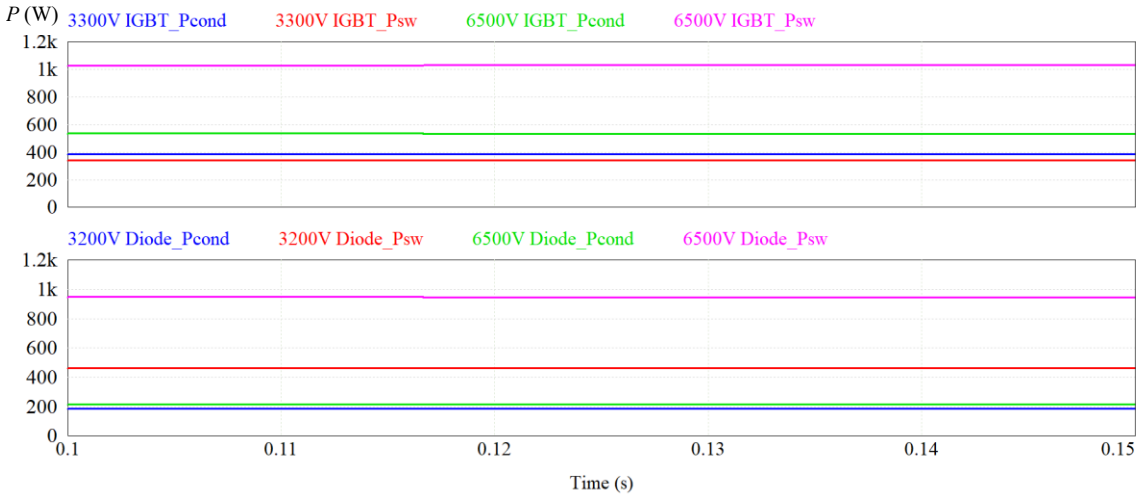

Figure 2-14 Simulated power losses of the switching devices in topology C.

The simulated conduction losses and switching losses of each switching component in topology C are shown in Table 2-6. The result shows that the power losses of each inner switch are higher than the power losses of any switches on the first and last rows. This results in an uneven power loss distribution in topology C. Besides, the power losses of IGBTs are higher than that of diodes in topology C. The power losses generated by IGBTs account for 55.1% of the total power losses in topology C. Furthermore, the switching losses are higher than the conduction losses in topology C, which account for 65.5% of the total power losses in topology C. Furthermore, compared with topology A, topology C has fewer conduction losses but more switching losses than topology A.

Table 2-6 Simulated power losses of the switching devices in topology C

Device		**Conduction losses (W)**	**Switching losses (W)**	**Power losses (W)**
S_{11}	IGBT	385.21	342.32	727.53
	Diode	185.99	463.72	649.71
S_{12}	IGBT	385.56	341.84	727.40
	Diode	186.16	463.04	649.20
S_{13}	IGBT	386.25	341.99	728.24
	Diode	186.50	464.39	650.89
S_{21}	IGBT	535.52	1029.92	1565.44
	Diode	216.15	948.68	1164.83
S_{22}	IGBT	535.04	1032.16	1567.20

	Diode	215.95	947.56	1163.51
S_{23}	IGBT	535.04	1031.45	1566.49
	Diode	215.95	947.86	1163.81
S_{31}	IGBT	385.21	342.32	727.53
	Diode	185.99	463.73	649.72
S_{32}	IGBT	385.56	341.84	727.40
	Diode	186.16	463.06	649.22
S_{33}	IGBT	386.25	341.99	728.24
	Diode	186.50	464.40	650.90
Total		5684.99	10772.27	16457.26

2.4.2 Comparison between simulated and calculated results

The simulated and calculated power losses of each topology are shown in Table 2-7. Among these three topologies, topology B has the fewest total power losses followed by topology C. Whereas Topology A has the most power losses. The total power loss difference between topology A and topology C is very small, which is only 78 W. Topology B has the highest efficiency, which is 99.45%. By contrast, topology A has the lowest efficiency, which is 98.80%. The efficiency of topology C is 98.81%, which is slightly higher than topology A.

Table 2-7 Simulated and calculated power losses of the SC-CSIs

Approach	**Losses**	**Topology A**	**Topology B**	**Topology C**
Calculation	Conduction losses (W)	6716.04	6716.04	5638.53
	Switching losses (W)	9640.02	1071.11	10661.04
	Power losses (W)	16356.24	7787.15	16299.57
	Efficiency	98.81%	99.48%	98.82%
Simulation	Conduction losses (W)	6862.72	6862.72	5684.99
	Switching losses (W)	9672.72	1238.76	10772.27
	Power losses (W)	16535.44	8101.48	16457.26
	Efficiency	98.80%	99.45%	98.81%
Error of the power losses between the calculation and simulation		1.08%	3.88%	0.96%

The comparison between the simulated power losses and calculated power losses in the three topologies is shown in Figure 2-15. The comparison shows that the calculated power losses are close to the simulated power losses, though it still has mismatching between them. The mismatch might be from 1) the reverse recovery energy of the diodes E_{rr} is not provided by the manufacturer. Although the reverse recovery charge Q_{rr} is provided, the value of the coefficient k_E in equation (2-8) is an assumed value, which may lead to the mismatch. 2) The switching losses of topology B are calculated from the switching losses of topology A divided by nine, however, the diodes used in topology A may not experience the reverse recovery process during every switching process, for example, when the voltage on the switch devices is positive during a switching process. Therefore, the calculated switching losses of topology B are fewer than the simulated result. And 3) the deviation between getting the data from datasheets for calculation and the data loaded in the simulation.

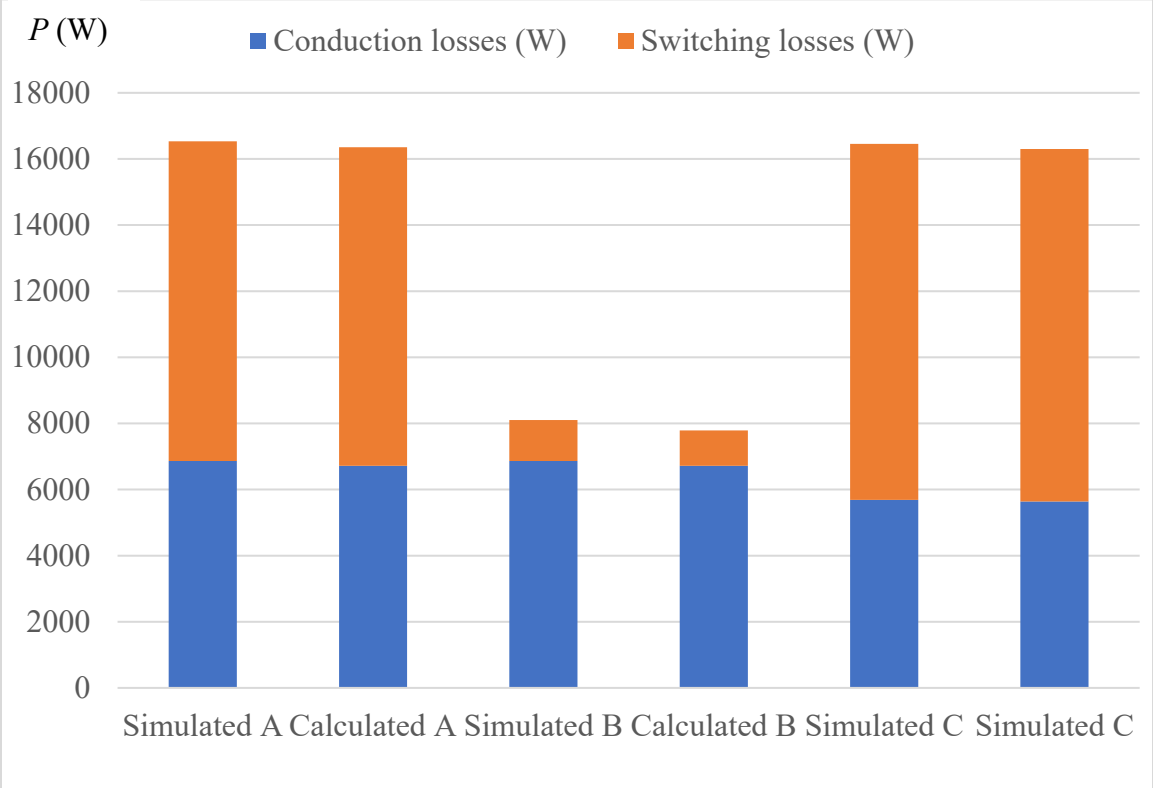

Figure 2-15 Comparison between the simulated and calculated power losses.

2.5 Summary

The factors related to the power losses are analyzed in detail in this chapter. The total power losses and the power loss distribution of SC-CSIs are investigated and compared. Firstly, topology A and topology B have the same power loss distribution, but topology C has a different power loss distribution. Every switch in topology A contributes the same power losses. The same result can be found in topology B. Whereas in topology C, every switch on the first and last rows has the same power losses as any switch in topology A, however, every inner switch in topology C contributes approximately double power losses.

Secondly, when SC-CSIs operate under the same conditions, topology A and topology C have almost the same total power losses, where the total power losses of topology A are slightly higher than that of topology C. Topology A has fewer switching losses but more conduction losses than topology C. The efficiency of topology C, 98.81% is slightly higher than that of topology A 98.8%, though the difference is very small. Among the three topologies, topology B has the fewest power losses with the highest efficiency of 99.45%.

Finally, the comparison among the three topologies is summarized in Table 2-8. The comparison in terms of efficiency is under the condition that using SVM with SQ1 scheme in topology A and topology C. The impact of different modulations on the power losses of SC-CSIs will be investigated in Chapter 3.

Table 2-8 Comparison among the three topologies

Item	**Topology A**	**Topology B**	**Topology C**
Efficiency	98.80%	99.45%	98.81%
Power loss distribution	Even	Even	Uneven
Number of switches	12	12	9
Complexity	High	High	Low

Chapter 3
Power Loss Investigation of Series-Connected Current Source Inverters with Different Modulation Schemes

The power losses of SC-CSIs in the three different topologies have been analyzed and compared in Chapter 2. The comparison is conducted with the typical modulation scheme SVM (SQ1) used in topology A and topology C. And the square-wave operation is adopted in topology B due to the switching frequency of 60 Hz. Modulation schemes can also influence the power losses of SC-CSIs. Adopting different modulation schemes in the same SC-CSIs may result in different power losses. Therefore, the objective of the investigation in this chapter is to analyze the influence of using different modulation schemes on the power losses of SC-CSIs.

This chapter starts with an introduction of three major modulation schemes for CSIs, including their principles and their performance, such as DC utilizing, dynamic performance, and harmonic performance. Then, the impacts of using different modulation schemes on the conduction losses and switching losses of SC-CSIs are analyzed. A simulated investigation of the power losses comparison using different modulation schemes is implemented. Finally, the power losses of SC-CSIs with different modulation schemes are compared. The topology and modulation scheme with the lowest power losses are recommended.

3.1 Modulation schemes for CSIs.

In general, two conditions must be satisfied in switching pattern design for CSIs. One is the DC current I_{dc} should be continuous. The other is the inverter PWM current i_w should be defined. These two conditions can be interpreted as a switching constraint: Only two switches, one in the top half of the bridge and the other in the bottom half can be on-state at any instant of time (excluding commutation intervals). Based on this, three typical

modulation schemes for CSIs operating with a switching frequency around 500Hz have been developed. They are the TPWM, SHE, and SVM.

3.1.1 TPWM

The diagram of a TPWM scheme with a switching frequency of 540 Hz is shown in Figure 3-1. The positive half-cycle of the output PWM current i_w is presented. The waveform of i_w is of half-wave symmetry. The gating signals are generated by comparing the modulating wave v_m with the carrier wave v_{cr}. The gating signal v_{g1} is generated when the magnitude of v_m is higher than v_{cr}. The modulating wave is a trapezoidal wave. The carrier wave is a triangle wave whose frequency is related to the switching frequency F_{sw}, but it equals zero in the middle $\pi/3$ interval of the positive half-cycle and the negative half-cycle of the inverter fundamental frequency. Such a design can make the switching pattern satisfy the switching constraint for CSIs. The gating signals of other switches can be obtained by shifting the gating signal v_{g1}. For example, gating signal v_{g2} can be obtained by shifting v_{g1} for a phase delay of 60º.

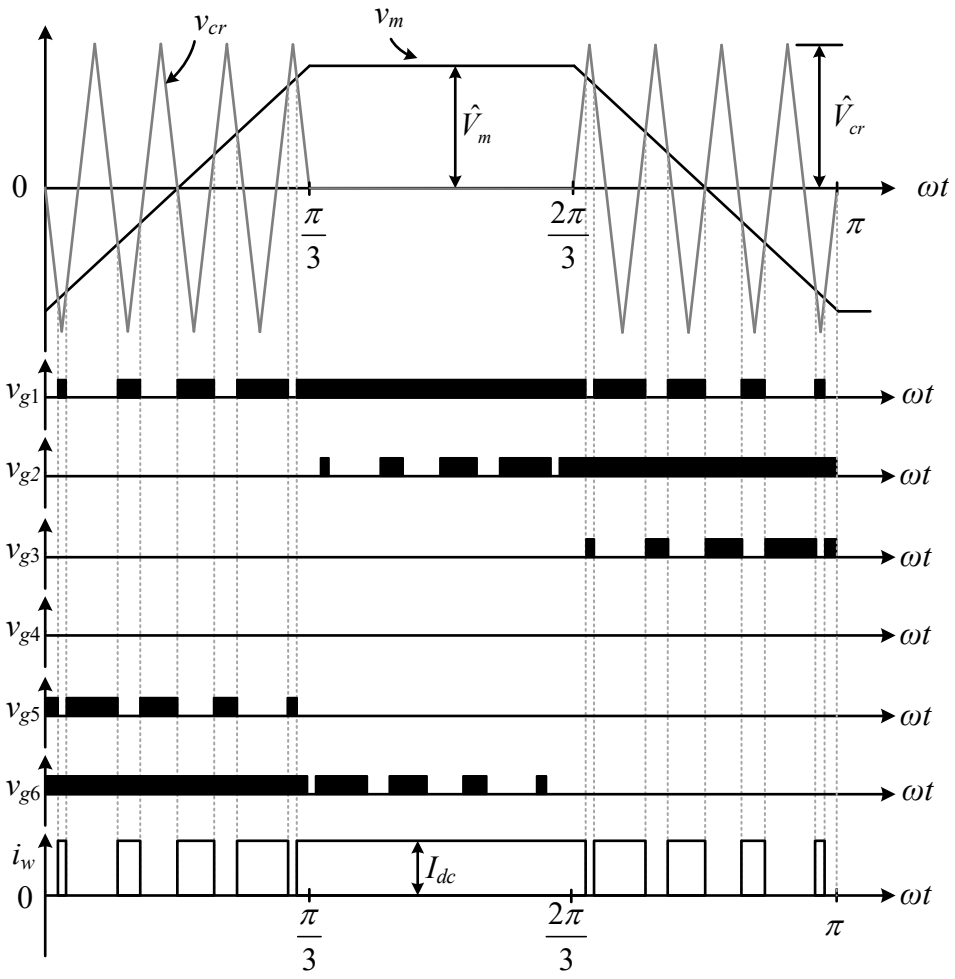

Figure 3-1 The TPWM scheme.

The switching frequency of switching devices can be calculated by

$$F_{sw} = F_1 \times N_p \tag{3-1}$$

where F_1 is the fundamental frequency and N_p is the number of pulses per half-cycle of the output PWM current i_w. As shown in Figure 3-1, there are 9 pulses per half-cycle of i_w, with a fundamental frequency of 60 Hz, the switching frequency can be calculated, which is 540 Hz.

In the TPWM scheme, the magnitude of the PWM output current i_w is equal to the DC current I_{dc}. While the rms value of the fundamental-frequency current i_{w1} can be regulated by adjusting the modulation index, in practice, it is normally controlled by adjusting the DC current I_{dc} through the rectifier. Its DC utilization varies from 0.66 to 0.74 when the

modulation index m_a changes from 0 to the maximum value of 1.0. In terms of the harmonic performance, two pairs of dominant harmonics I_{wn} can be found in the output PWM current with the TPWM scheme at

$$\begin{cases} n = 3\left(N_p - 1\right) \pm 1 \\ n = 3\left(N_p - 1\right) \pm 5 \end{cases} \tag{3-2}$$

Since the low-other harmonics are difficult to be fully eliminated, the TPWM scheme is hardly applied when N_p is less than seven [3].

3.1.2 SHE

Figure 3-2 presents a positive half-cycle i_w waveform of the SHE scheme with a switching frequency of 540 Hz. There are nine pulses with nine switching angles in the positive half-cycle in i_w. Among them, only four out of the nine switching angles, θ_1, θ_2, θ_3, and θ_4, are independent. Other switching angles can be calculated once known these four angles. These four switching angles provide four degrees of freedom, which can be used to eliminate four harmonics in the output PWM current i_w without modulation index control. Alternatively, it can eliminate three harmonics and provide an adjustable modulation index m_a. In practice, the regulation of the fundamental-frequency current i_{w1} is usually realized by adjusting the DC current I_{dc} instead of the modulation index m_a. Therefore, the former option is preferred. To eliminate a group of specific harmonics, the independent switching angles can be calculated by a few numerical methods, such as the Newton–Raphson iteration algorithm. Usually, the lowest order harmonics should be given the top priority to be eliminated.

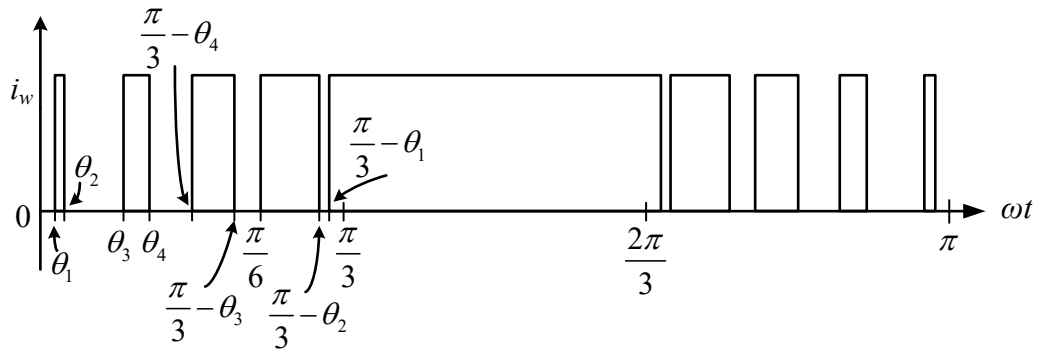

Figure 3-2 The SHE modulation scheme.

The DC current utilization of the SHE scheme ranges from 0.73 to 0.78. The SHE scheme has a great harmonic performance since several unwanted low-order harmonics in the output PWM current i_w can be eliminated by using the SHE scheme. However, it is complicated and may have no solution to eliminate more than four harmonics in i_w simultaneously [3]. The dynamic performance of the SHE scheme is limited since it is an offline modulation scheme. The switching angles used in SHE are pre-calculated due to the complex calculation process. After that, they are uploaded into a digital controller for implementation.

3.1.3 SVM

Based on the switching constraint, the CSI has a total of nine combinations of on-state switches with nine switching states, including three zero switching states and six active switching states. Each switching state has a corresponding space vector as shown in Table 3-1 [3], where $\vec{I}_1$ to $\vec{I}_6$ are the active vectors and $\vec{I}_0$ is the zero vector. They are also named stationary vectors since their positions are fixed in space.

The space vector diagram for CSIs is shown in Figure 3-3 [3], where $\vec{I}_{ref}$ represents the current reference vector and rotates at an angular velocity ω which is decided by the fundamental frequency of the inverter output current i_w, and θ is the angular displacement between $\vec{I}_{ref}$ and the α-axis of the α-β plane. With a certain position and length, the reference current $\vec{I}_{ref}$ can be synthesized from the three nearby stationary vectors. The switching state of the inverter can be selected according to the three vectors and gating

signals for the active switches can be generated. Different sets of switches will be turned on or off when $\vec{I}_{ref}$ rotates in the space. The magnitude of the output current is decided by the length of $\vec{I}_{ref}$, and the frequency of the output current depends on the rotating speed of the reference current $\vec{I}_{ref}$.

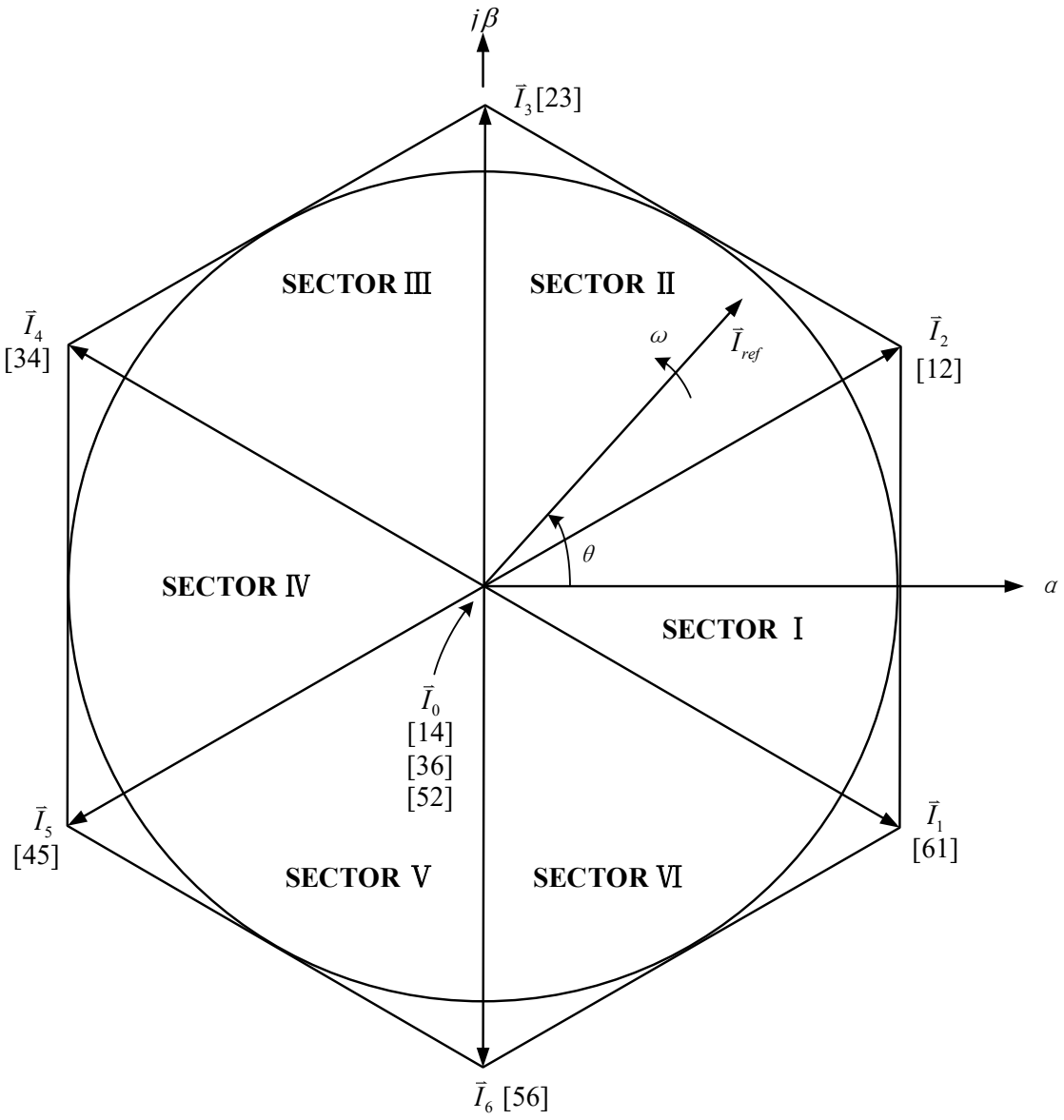

Figure 3-3 Space vector diagram for CSIs [3].

Table 3-1 Switching States and Space Vectors [3]

Type	Switching State	On-State Switches	Space Vector
Zero States	[14]	S_1, S_4	$\vec{I}_0$
	[36]	S_3, S_6	
	[52]	S_5, S_2	
Active States	[61]	S_6, S_1	$\vec{I}_1$
	[12]	S_1, S_2	$\vec{I}_2$
	[23]	S_2, S_3	$\vec{I}_3$
	[34]	S_3, S_4	$\vec{I}_4$
	[45]	S_4, S_5	$\vec{I}_5$
	[56]	S_5, S_6	$\vec{I}_6$

The dwell time calculation of the selected vectors in Sector I is shown in the equation (3-3) [3]. where m_a is the modulation index, T_s is the sampling period, T_1, T_2, and T_0 are the dwell time for vectors $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_0$ respectively.

$$\begin{cases} T_1 = m_a \sin(\pi/6 - \theta) T_s \\ T_2 = m_a \sin(\pi/6 + \theta) T_s \\ T_0 = T_s - T_1 - T \end{cases} \tag{3-3}$$

The switching sequence design for CSIs needs to meet two requirements to minimize the switching frequency: 1) Only two switches are involved during the transitions, one being switched on and the other switches off; and 2) the minimum number of switching is required when $\vec{I}_{ref}$ rotating from one sector to the next sector. Figure 3-4 shows six space vector sequences for CSIs studied in the literature [51]. Switching sequences can influence the switching losses due to different switching voltages and/or different switching frequencies. It is worth noting is that the switching frequency in SVM (SQ3) decreases from 540 Hz to 480 Hz since the last space vector in one sector and the first space vector in the next sector are the same. Besides, in SVM (SQ5), the last zero vector in the present sector is selected as the first zero vector in the next sector. Therefore, the switching frequency is reduced from 540 Hz to 480 Hz.

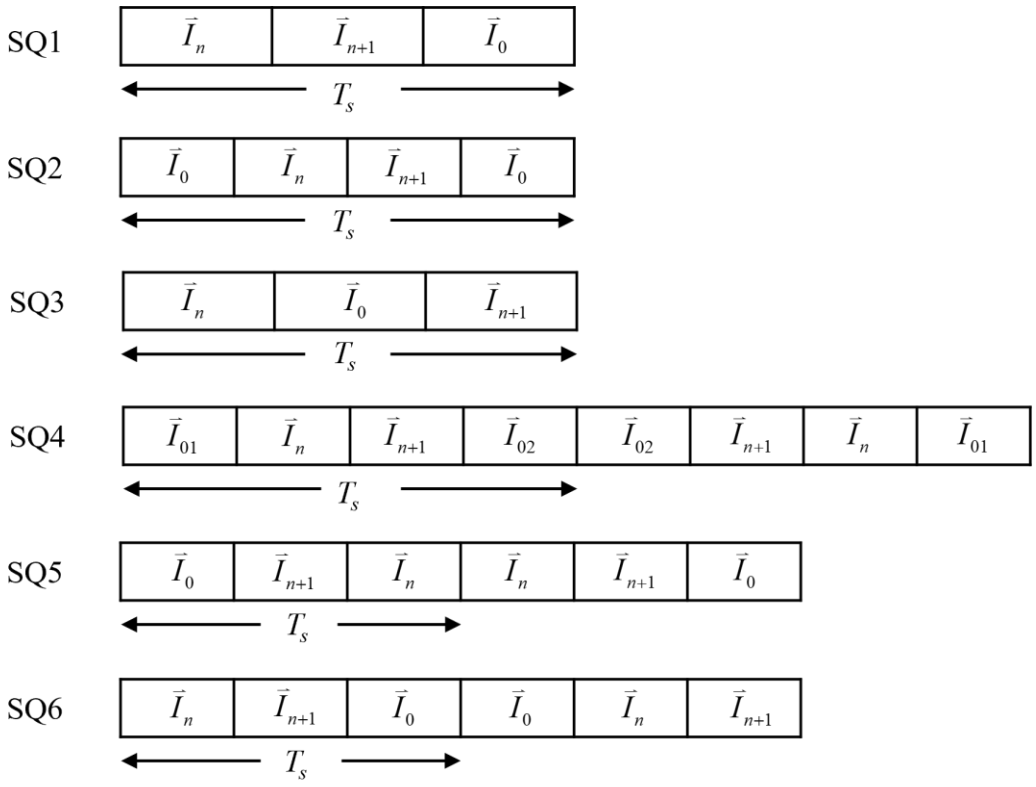

Figure 3-4 Switching sequences of the SVM for CSIs.

The maximum DC current utilization in SVM is 0.707 when the modulation index is at its maximum value of 1. It is comparatively low due to the bypass operation [3]. However, the SVM has the best dynamic performance. Because the modulation index can be changed within a sampling period to directly control the output PWM current i_w. The harmonic performance of SVM is ordinary. To reduce the low-order harmonics of SVM, a few developed SVM schemes have been proposed in the literature, for example, the natural sampling SVM (NS-SVM) [48].

3.2 Power losses with different modulation schemes

Different modulation schemes have different principles and generate different gating signals to control the switching device. They can influence the current and voltage waveforms of the switch, which may result in different power losses. However, the power loss distribution will not be influenced.

3.2.1 Conduction losses

As the analysis in Chapter 2, the conduction losses are decided by the conduction current, the saturation voltage of the switch, and the duty cycle of the switch, which is the on-state time during the whole cycle of the fundamental frequency. The conduction current and the saturation voltage of the switch do not change obviously. Thus, it is crucial to find out if the duty cycle *D* will change or not when using different modulation schemes.

(a) Duty cycle in the TPWM scheme

In the TPWM scheme, the on-state time of a switch is equal to its off-state time in the first and last π/3 section intervals of the positive half-cycle. This is because both the modulating wave and the carrier wave are of point symmetry at the center point of π/6 and 5π/6 in these two intervals. Besides, the switch is on-state in the center π/3 interval of the positive half-cycle and off-state in the entire negative half-cycle of the fundamental frequency. Therefore, the total on-state time of the switch accounts for 1/3 in the whole cycle of the fundamental frequency, which means the value of the duty cycle in the TPWM scheme D_{TPWM} is 1/3.

$$D_{TPWM} = \frac{(\frac{1}{2}\times\frac{\pi}{3}+\frac{\pi}{3}+\frac{1}{2}\times\frac{\pi}{3})}{2\pi} = \frac{1}{3} \tag{3-4}$$

(b) Duty cycle in the SHE scheme

In the SHE modulation scheme, the on-state time of a switch accounts for 1/2 in the first π/3 section interval of the positive half-cycle. For example, in Figure 3-2, the on-state time of a switch in the first π/3 section intervals of the positive half-cycle account for 1/2 of the interval.

$$\frac{(\theta_2-\theta_1)+(\theta_4-\theta_3)+[(\frac{\pi}{3}-\theta_4)-\frac{\pi}{6}]+[(\frac{\pi}{3}-\theta_2)-(\frac{\pi}{3}-\theta_3)]+[\frac{\pi}{3}-(\frac{\pi}{3}-\theta_1)]}{\frac{\pi}{3}} = \frac{1}{2} \tag{3-5}$$

Similarly, the on-state time also accounts for 1/2 in the last π/3 section intervals of the positive half-cycle. Besides, the switching is on-state during the entire center π/3 interval of

the positive half-cycle and off-state during the whole negative half-cycle. Therefore, the duty cycle in the SHE scheme D_{SHE} of the switch is also 1/3.

$$D_{SHE} = \frac{(\frac{1}{2}\times\frac{\pi}{3}+\frac{\pi}{3}+\frac{1}{2}\times\frac{\pi}{3})}{2\pi} = \frac{1}{3} \tag{3-6}$$

(c) Duty cycle in the SVM scheme

In the SVM modulation scheme, the value of duty cycle D is also 1/3. There are six sectors in the whole cycle of the fundamental frequency. The reference current $\vec{I}_{ref}$ in each sector can be synthesized by three space vectors. For instance, the $\vec{I}_{ref}$ is synthesized by space vectors $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_0$ in Sector I. The dwell time T_1, T_2, and T_0 of the space vectors $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_0$ can be calculated using equation (3-3). Assuming there are total N samples in each sector. The total exhibition time T_{t1}, T_{t2}, and T_{t0} of the space vectors $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_0$ in Sector I can be expressed as

$$\begin{cases} T_{t1} = \sum_{k=1}^{N} T_{k1} \\ T_{t2} = \sum_{k=1}^{N} T_{k2} \\ T_{t0} = \sum_{k=1}^{N} T_{k0} \end{cases} \tag{3-7}$$

where T_{k1}, T_{k2}, and T_{k0} are the dwell time of $\vec{I}_1$, $\vec{I}_2$, and $\vec{I}_0$ in the sample number k. Since the modulation index m_a and the sampling period T_s are fixed, also each sector contains the same number of samples. The dwell time T_{tn}, $T_{t(n+1)}$, and $T_{t0'}$ for space vectors $\vec{I}_n$, $\vec{I}_{(n+1)}$, and $\vec{I}_{0'}$ equal to T_{t1}, T_{t2}, and T_{t0} in other sectors.

$$\begin{cases} T_{tn} = T_{t1} \\ T_{t(n+1)} = T_{t2} \\ T_{t0'} = T_{t0} \end{cases} \tag{3-8}$$

During the whole cycle of the fundamental frequency, $\vec{I}_1$ (S_6 and S_1 are on-state) presents as the vector $\vec{I}_{(n+1)}$ in Sector VI and presents as the vector $\vec{I}_n$ in Sector I. $\vec{I}_2$ (S_1 and S_2 are on-state) presents as the vector $\vec{I}_{(n+1)}$ in Sector I and presents as the vector $\vec{I}_n$ in Sector II. And $\vec{I}_0$ (S_1 and S_4 are on) presents as the vector $\vec{I}_{0'}$ in Sector I and Sector IV. Therefore, the total on-state time T_{s1} of the switch S_1 during the whole cycle of the fundamental frequency is

$$T_{s1} = T_{t(n+1)} + T_{tn} + T_{t(n+1)} + T_{tn} + 2T_{t0'} = 2(T_{tn} + T_{t(n+1)} + T_{t0'}) \tag{3-9}$$

Thus, the duty cycle of the switch S_1 is

$$D_{s1} = \frac{2(T_{tn} + T_{t(n+1)} + T_{t0'})}{6(T_{tn} + T_{t(n+1)} + T_{t0'})} = \frac{1}{3} \tag{3-10}$$

Since each active space vector exhibits as the space vector $\vec{I}_n$ in one sector and exhibits as the space vector $\vec{I}_{(n+1)}$ in another sector, and each zero space vector exhibits as the space vector $\vec{I}_{0'}$ in two of six sectors. Moreover, every switch response for two of the active space vectors and one of the zero space vectors. Therefore, every switch has the same on-state time leading to the same duty cycle D_{SVM}.

$$D_{SVM} = D_{S1} = \frac{1}{3} \tag{3-11}$$

It can be seen that the switches in the TPWM, SHE, and SVM schemes have the same duty cycle from equations (3-4), (3-6), and (3-11). Besides, the duty cycle in square-wave operation is also 1/3. The duty cycles are the same in these modulation schemes and will not be affected by the modulation index m_a and switching frequencies. Since the conduction current, the saturation voltage, and the duty cycle remain the same in these modulation schemes, the conduction losses of SC-CSIs will not be influenced when using different modulation schemes.

3.2.2 Switching losses

The switching losses can be influenced by modulation schemes, modulation index m_a, and switching frequency F_{sw}. Different modulation schemes have different modulation principles to generate gating signals. Besides, the modulation index is a factor participating in the modulation process. Both of them can influence the gating signals. Different gating signals mean the moments of switching/conducting of the switch are changed. Consequently, the instant values of the voltage between the switching device during switching/conducting are different leading to different switching losses. The increase or decrease of the switching losses depends on the change of the switching voltages. Therefore, the same modulation index is adopted in these modulation schemes. Whereas, switching frequencies can directly affect switching losses.

When using different modulation schemes with the same switching frequency, the switching losses will be influenced by only different gating signals, which lead to the different switching voltages between the switching device when switching. However, when using different modulation schemes with different switching frequencies the switching losses will be influenced by two parts. 1) Different modulation principles generate different gating signals leading to the different switching voltages. 2) The switching frequency can directly influence the switching losses.

3.3 Simulation investigation

To investigate the influence of using different modulation schemes on the power losses of SC-CSIs and verify the analysis. A simulation investigation is carried out. The simulation models are built based on PSIM_2021a. The parameters of the SC-CSIs are presented in Table 3-2. These parameters are the same in each topology except the modulation schemes and the switching frequency since the objective is to find out the influence of the modulation scheme on the power losses. The inductors are employed as the leakage inductance from the transformers. Filter capacitors are employed at the output side of each inverter to assist the commutation of the switching devices and filter out harmonics.

Since SC-CSIs in topology B operates with a switching frequency of 60 Hz. The square-wave operation is adopted in topology B. The filter capacitance is larger in topology B due to the significant low-order harmonics. The TPWM, SHE, and SVM (SQ1 to SQ6) schemes are used in topology A and topology C. The adopted modulation schemes with the relative switching frequencies have been shown in Table 3-3.

Table 3- 2 Parameters of the SC-CSIs.

Parameters	**Topology A and topology C**	**Topology B**
DC link current (A)	500	500
Line voltage (V_{rms})	1150	1150
The number of CSI	2	2
Modulation index	1	1
Resistance (pu)	1	1
Inductance (pu)	0.1	0.1
Capacitance (pu)	0.3	0.5

Table 3-3 Switching frequency in each modulation scheme

Modulation scheme	**Switching frequency (Hz)**
TPWM	540
SHE	540
SVM (SQ1)	540
SVM (SQ2)	540
SVM (SQ3)	480
SVM (SQ4)	540
SVM (SQ5)	480
SVM (SQ6)	540
Square-wave operation	60

The simulation circuits of each topology are the same as the simulation circuits shown in Figure 2-6, Figure 2-7, and Figure 2-8 in Chapter 2. Each SC-CSIs are formed by two PWM CSIs. A three-phase balanced inductive load is applied at the output of each inverter. Filter capacitors are employed to assist the commutation of the switching devices and filter out harmonics. The parameters of the switching components are the same as the parameters presented in Table 2-2 and Table 2-3 in Chapter 2 since the components are not changed.

3.3.1 Simulation results

The simulated gating singles with the output PWM current i_w and output current i_s produced by using different modulation schemes will be shown. The simulated conduction losses, switching losses, and the total power losses of each topology with different modulation will be presented. The simulated power losses will be compared.

(a) Topology A

The simulated gating singles with the output PWM current i_w and output current i_s in topology A with the TPWM scheme are shown in Figure 3-5. The gating signals of the six switching devices in the CSI #1 are shown in blue. The output PWM current i_w and the output current i_s are presented in red. There are nine pulses per half cycle in the output PWM current i_w with a switching frequency of 540 Hz.

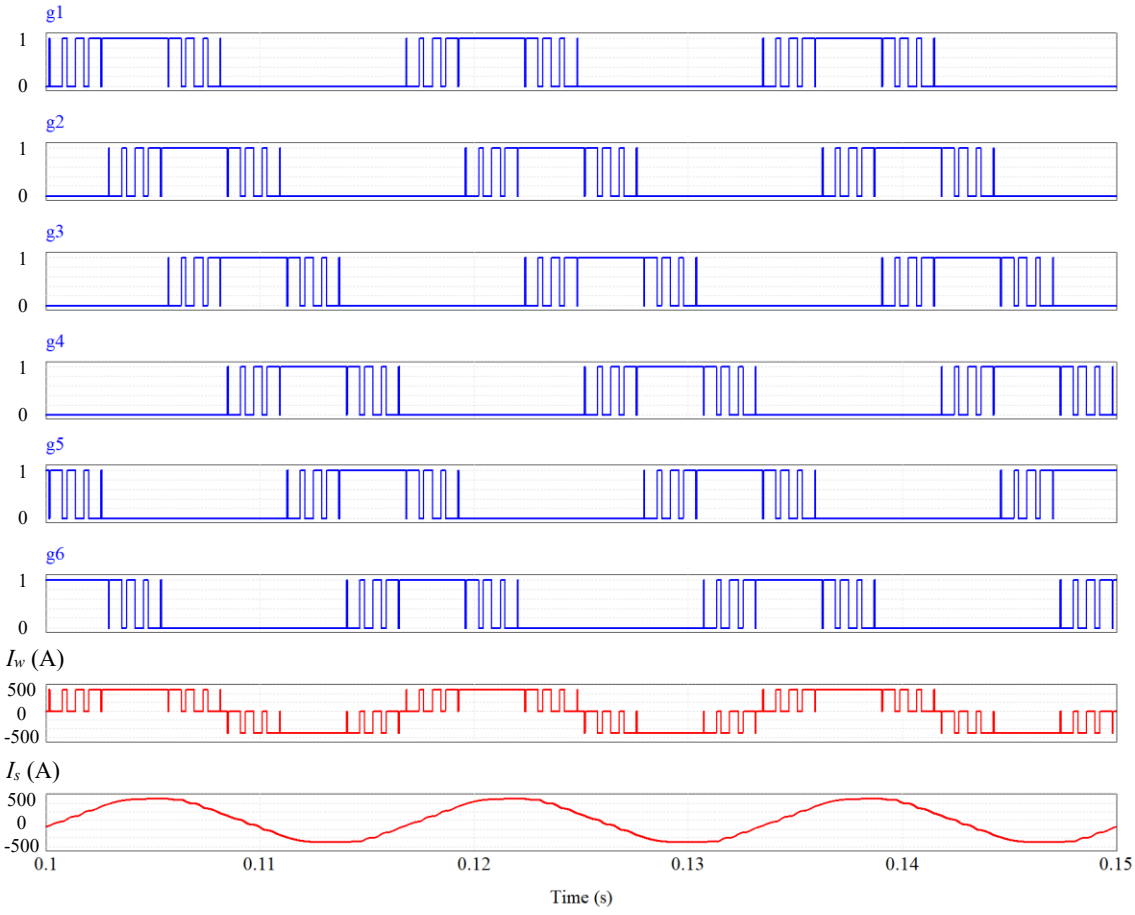

Figure 3-5 Simulated gating singles, i_w, and i_s in topology A with the TPWM scheme.

The simulated power losses of the switching device S_{11} in topology A with the TPWM scheme are shown in Figure 3-6. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses are shown in blue, and the switching losses are shown in red. The simulated power losses of any other switching devices are the same as that of the switching device S_{11} in topology A. This can be found in topology A with other modulation schemes. The result shows the conduction losses are the primary losses in the IGBT, whereas the switching losses are the main losses in the diode. The IGBT has more conduction losses but fewer switching losses than the diode. The IGBT generates more losses than the diode.

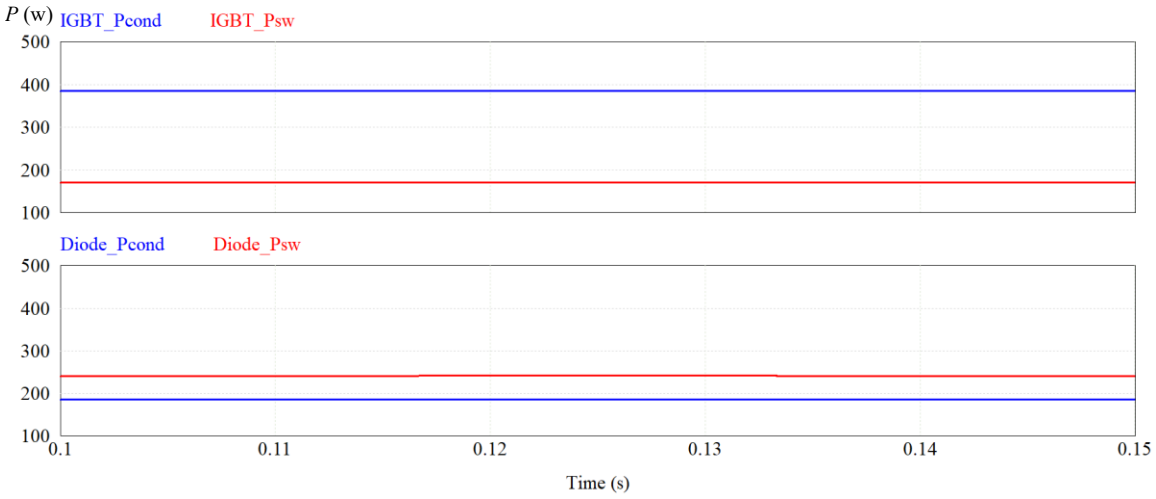

Figure 3-6 Simulated power losses of one switching device in topology A with the TPWM scheme.

The simulated gating singles with the output PWM current i_w and output current i_s in topology A with the SHE scheme are shown in Figure 3-7. The gating signals of the six switching devices in the CSI #1 are shown in blue. The output PWM current i_w and the output current i_s are presented in red. There are nine pulses per half cycle in the output PWM current i_w with a switching frequency of 540 Hz.

The simulated power losses of the switching device S_{11} in topology A with the SHE scheme are shown in Figure 3-8. The result shows the conduction losses are the primary losses in the IGBT, whereas the switching losses are the main losses in the diode. The IGBT has more conduction losses but fewer switching losses than the diode. The IGBT generates more losses than the diode.

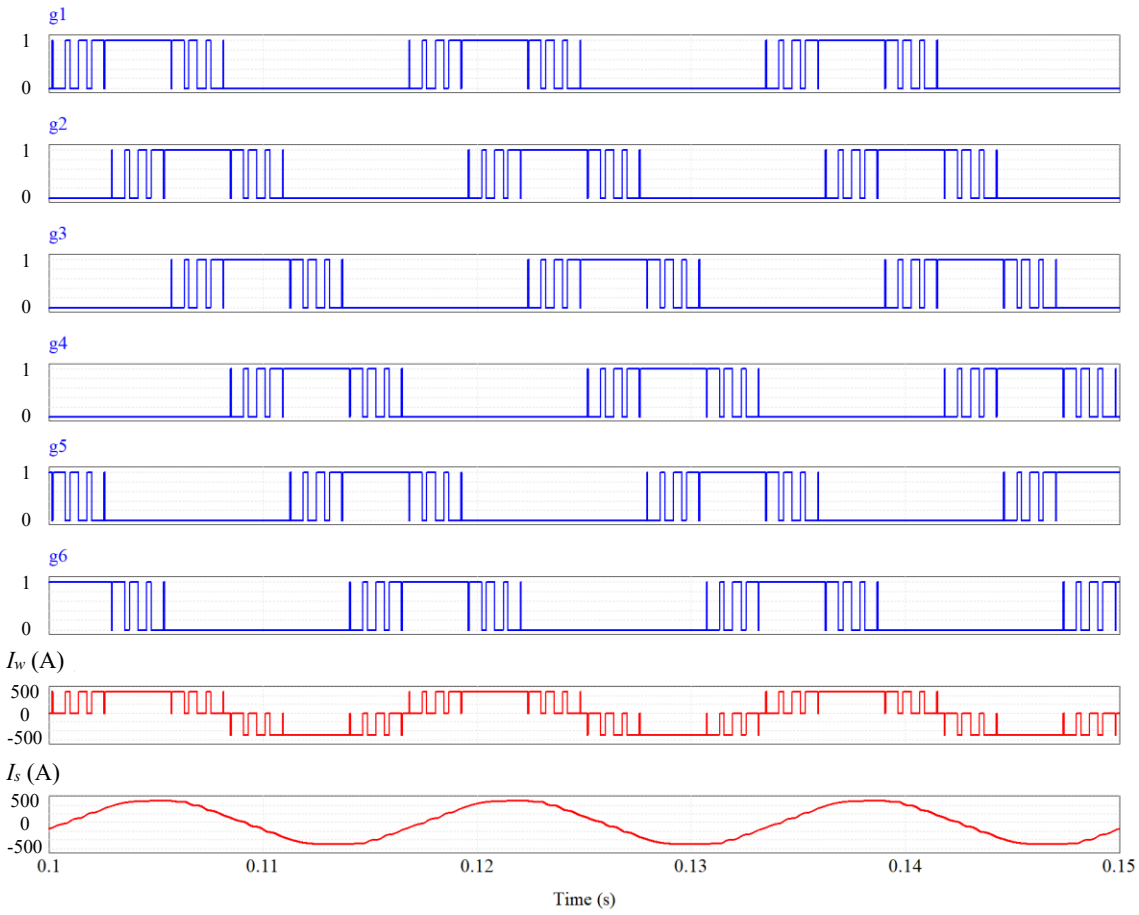

Figure 3-7 Simulated gating singles, i_w, and i_s in topology A with the SHE scheme.

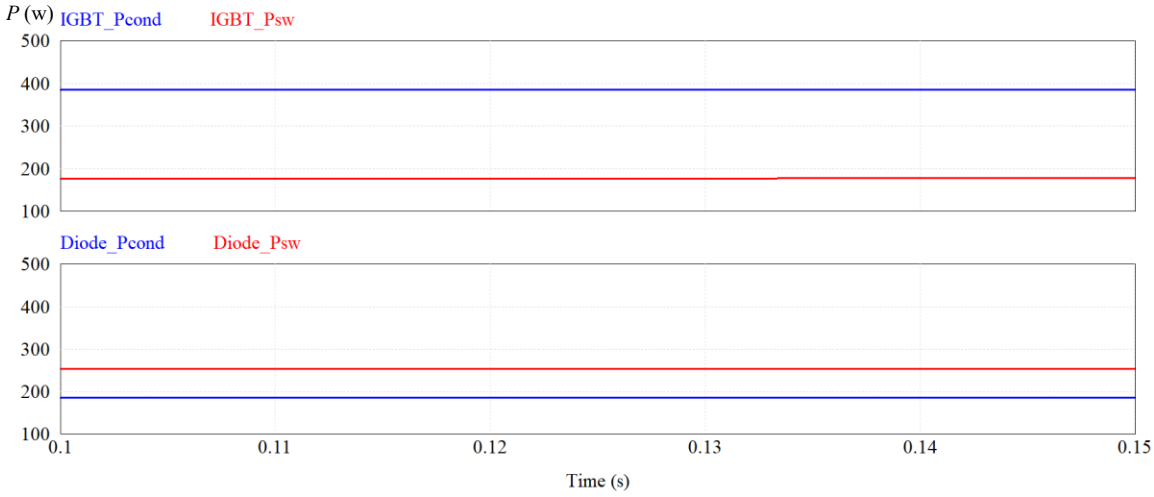

Figure 3-8 Simulated power losses of one switching device in topology A with the SHE scheme.

The simulated gating singles with the output PWM current i_w and output current i_s in topology A with the SVM (SQ1) scheme are shown in Figure 3-9. The gating signals of the six switching devices in the CSI #1 are shown in blue. The output PWM current i_w and the output current i_s are presented in red. There are nine pulses per half cycle in the output PWM current i_w with a switching frequency of 540 Hz.

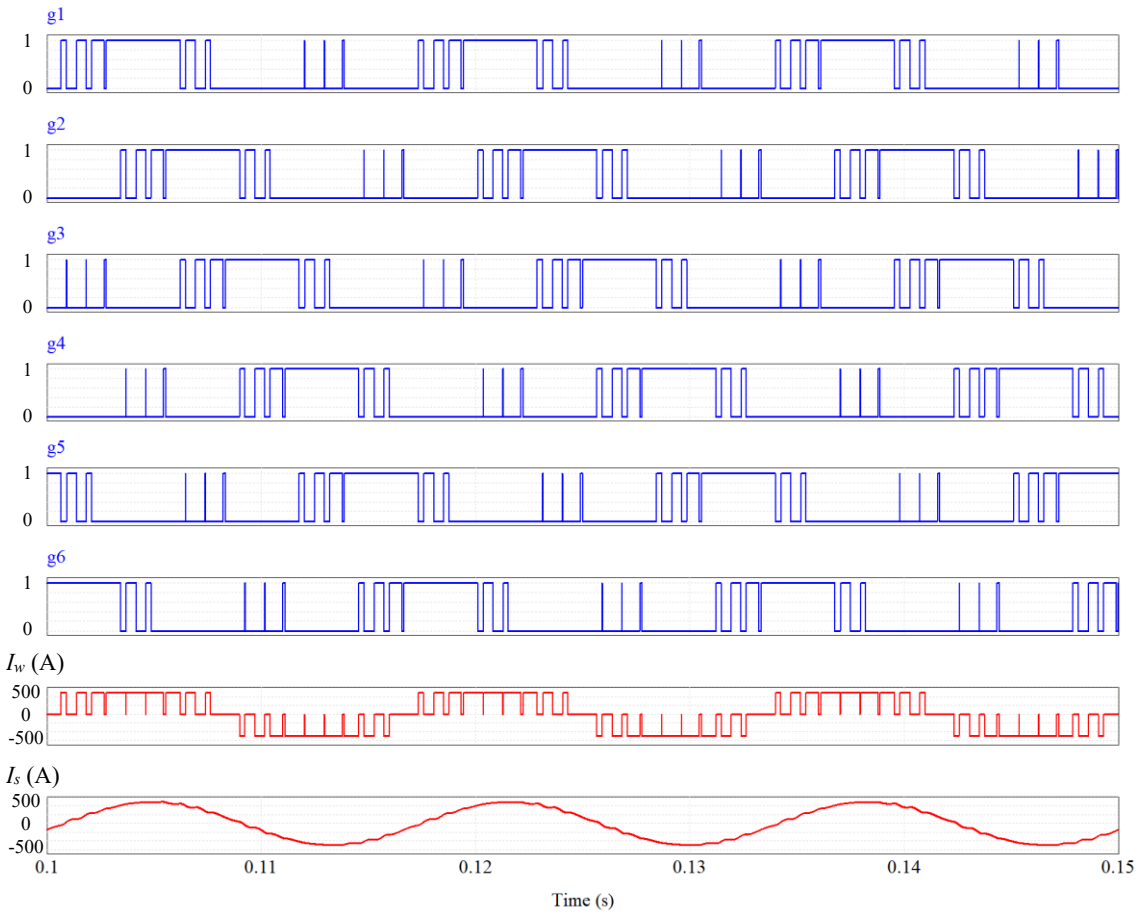

Figure 3-9 Simulated gating singles, i_w, and i_s in topology A with the SVM (SQ1) scheme.

The simulated power losses of the switching device S_{11} in topology A with the SVM (SQ1) scheme are shown in Figure 3-10. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses are shown in blue, and the switching losses are shown in red. The result shows the conduction losses are the main losses in the IGBT though the difference is not big, whereas the switching losses are the major losses in the diode and are much higher than the conduction losses. The IGBT has more conduction

losses but fewer switching losses than the diode. The IGBT generates more losses than the diode.

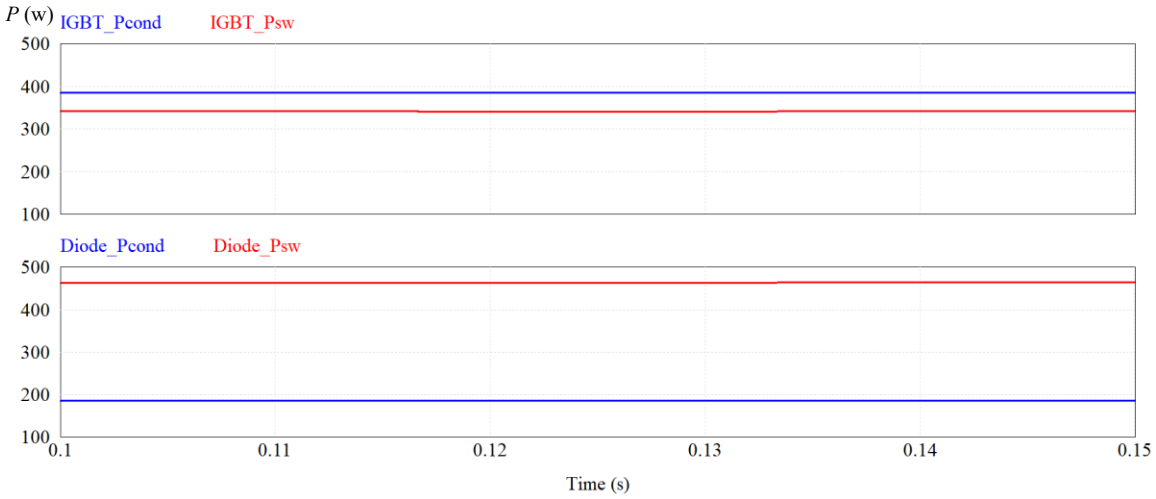

Figure 3-10 Simulated power losses of one switching device in topology A with the SVM (SQ1) scheme.

The simulated gating singles with the output PWM current i_w and output current i_s in topology A with the SVM (SQ2) scheme are shown in Figure 3-11. The gating signals of the six switching devices in the CSI #1 are shown in blue. The output PWM current i_w and the output current i_s are presented in red. There are nine pulses per half cycle in the output PWM current i_w with a switching frequency of 540 Hz.

The simulated power losses of the switching device S_{11} in topology A with the SVM (SQ2) scheme are shown in Figure 3-12. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses are shown in blue, and the switching losses are shown in red. The result shows the conduction losses are the main losses in the IGBT though the difference is not big, whereas the switching losses are the primary losses in the diode and are much higher than the conduction losses. The IGBT has more conduction losses but fewer switching losses than the diode. The IGBT generates more losses than the diode.

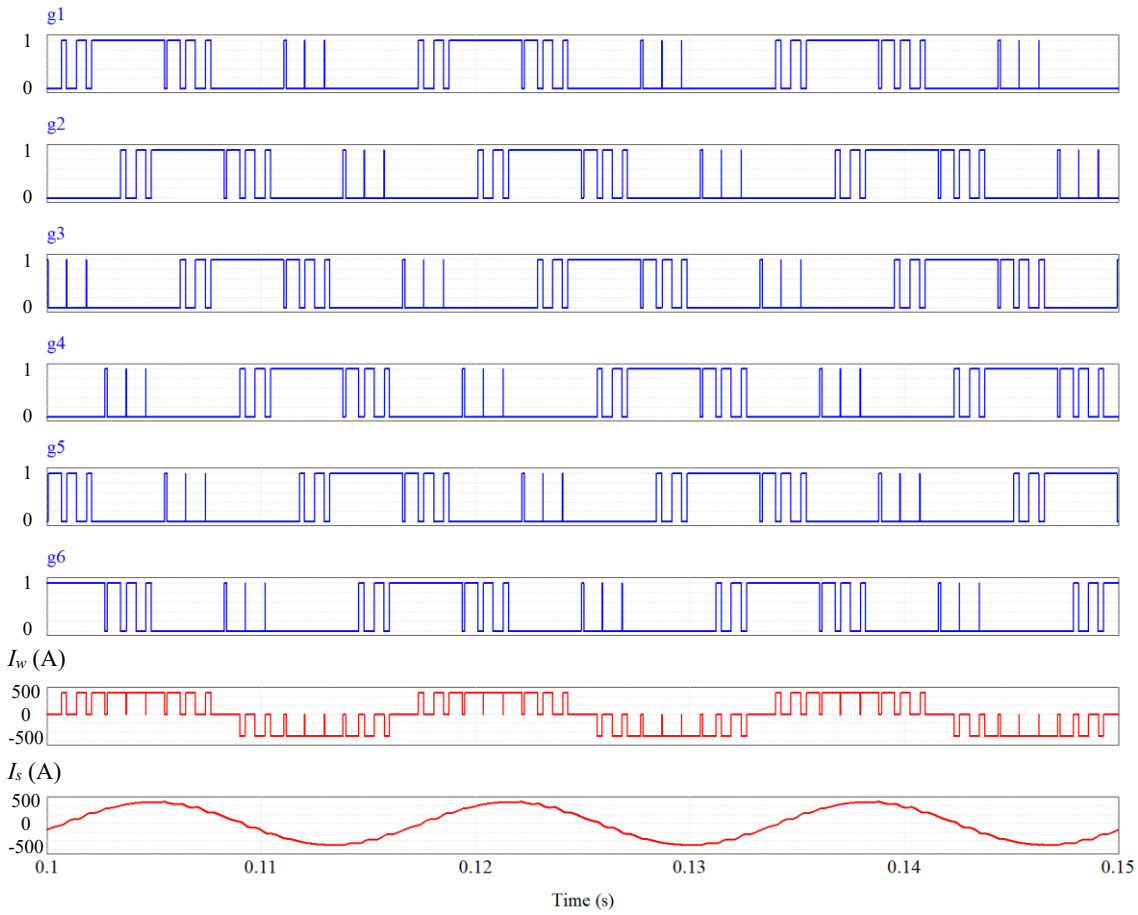

Figure 3-11 Simulated gating singles, i_w, and i_s in topology A with the SVM (SQ2) scheme.

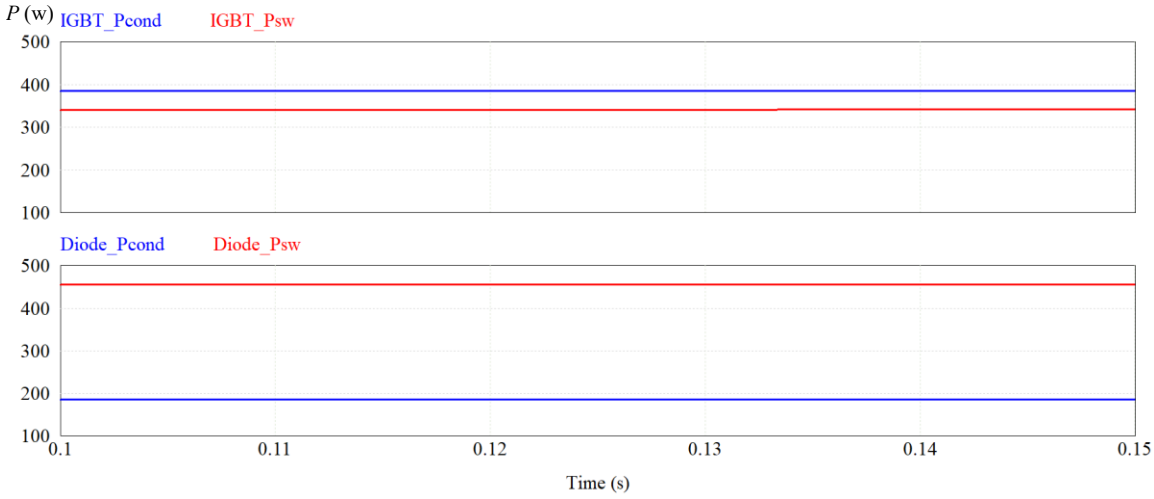

Figure 3-12 Simulated power losses of one switching device in topology A with the SVM (SQ2) scheme.

The simulated gating singles with the output PWM current i_w and output current i_s in topology A with the SVM (SQ3) scheme are shown in Figure 3-13. The gating signals of the six switching devices in the CSI #1 are shown in blue. The output PWM current i_w and the output current i_s are presented in red. There are eight pulses per half cycle in the output PWM current i_w with a switching frequency of 480 Hz.

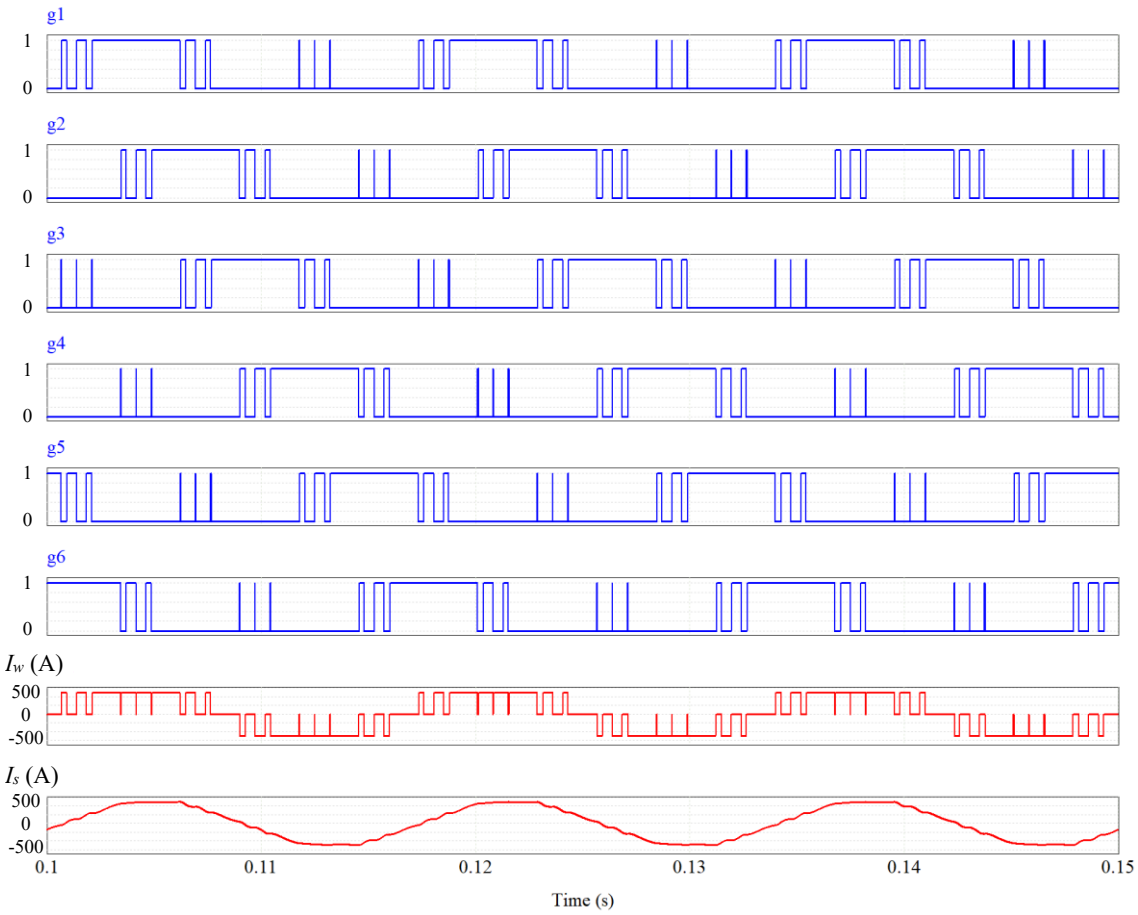

Figure 3-13 Simulated gating singles, i_w, and i_s in topology A with the SVM (SQ3) scheme.

The simulated power losses of the switching device S_{11} in topology A with the SVM (SQ3) scheme are shown in Figure 3-14. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses are shown in blue, and the switching losses are shown in red. The result shows the conduction losses are the main losses in the IGBT, whereas the switching losses are the primary losses in the diode and are much higher

than the conduction losses. The IGBT has more conduction losses but fewer switching losses than the diode. The IGBT generates more losses than the diode.

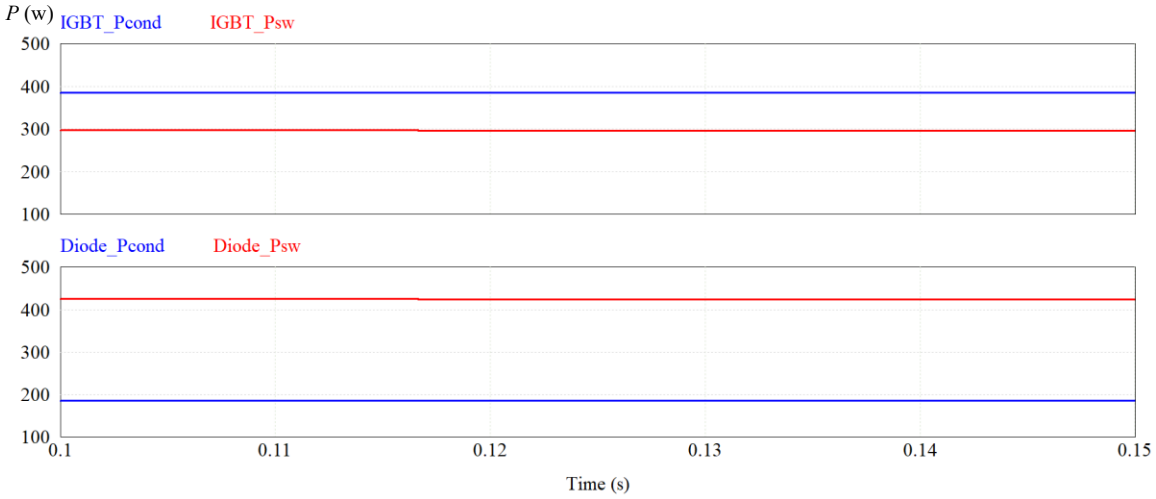

Figure 3-14 Simulated power losses of one switching device in topology A with the SVM (SQ3) scheme.

The simulated gating singles with the output PWM current i_w and output current i_s in topology A with the SVM (SQ4) scheme are shown in Figure 3-15. The gating signals of the six switching devices in the CSI #1 are shown in blue. The output PWM current i_w and the output current i_s are presented in red. There are nine pulses per half cycle in the output PWM current i_w with a switching frequency of 540 Hz.

The simulated power losses of the switching device S_{11} in topology A with the SVM (SQ4) scheme are shown in Figure 3-16. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses are shown in blue, and the switching losses are shown in red. The result shows the conduction losses are the main losses in the IGBT though the difference is not big, whereas the switching losses are the primary losses in the diode and are much higher than the conduction losses. The IGBT has more conduction losses but fewer switching losses than the diode. The IGBT generates more losses than the diode.

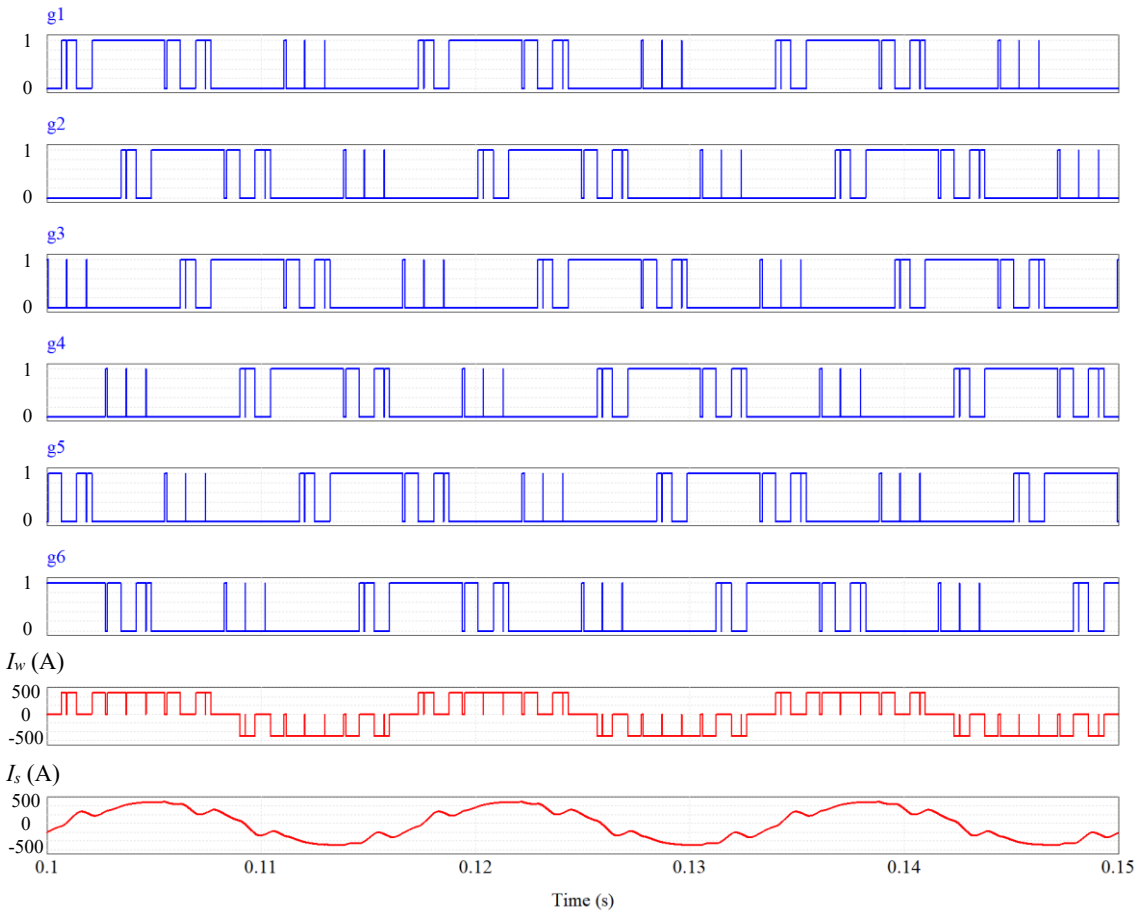

Figure 3-15 Simulated gating singles, i_w, and i_s in topology A with the SVM (SQ4) scheme.

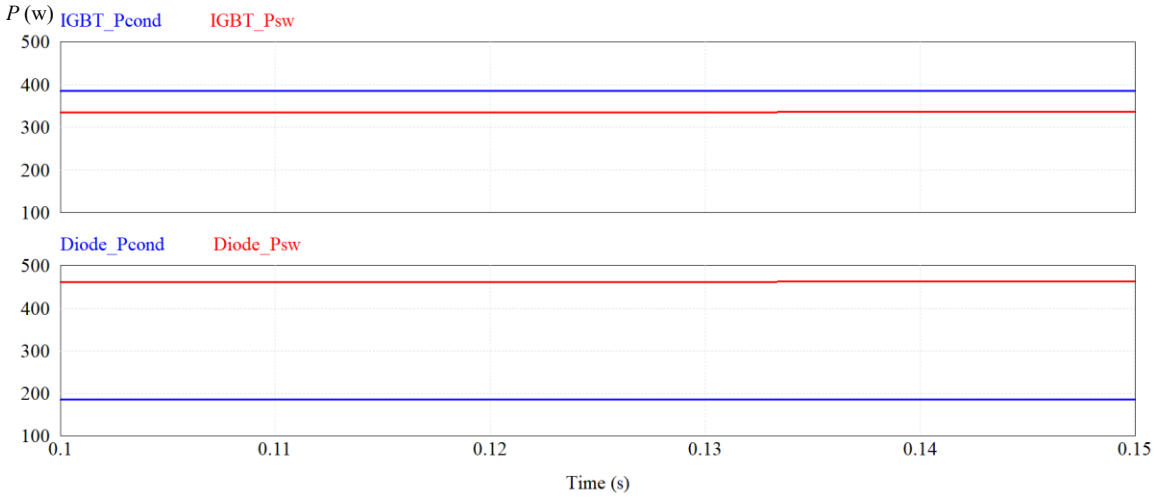

Figure 3-16 Simulated power losses of one switching device in topology A with the SVM (SQ4) scheme.

The simulated gating singles with the output PWM current i_w and output current i_s in topology A with the SVM (SQ5) scheme are shown in Figure 3-17. The gating signals of the six switching devices in the CSI #1 are shown in blue. The output PWM current i_w and the output current i_s are presented in red. There are eight pulses per half cycle in the output PWM current i_w with a switching frequency of 480 Hz.

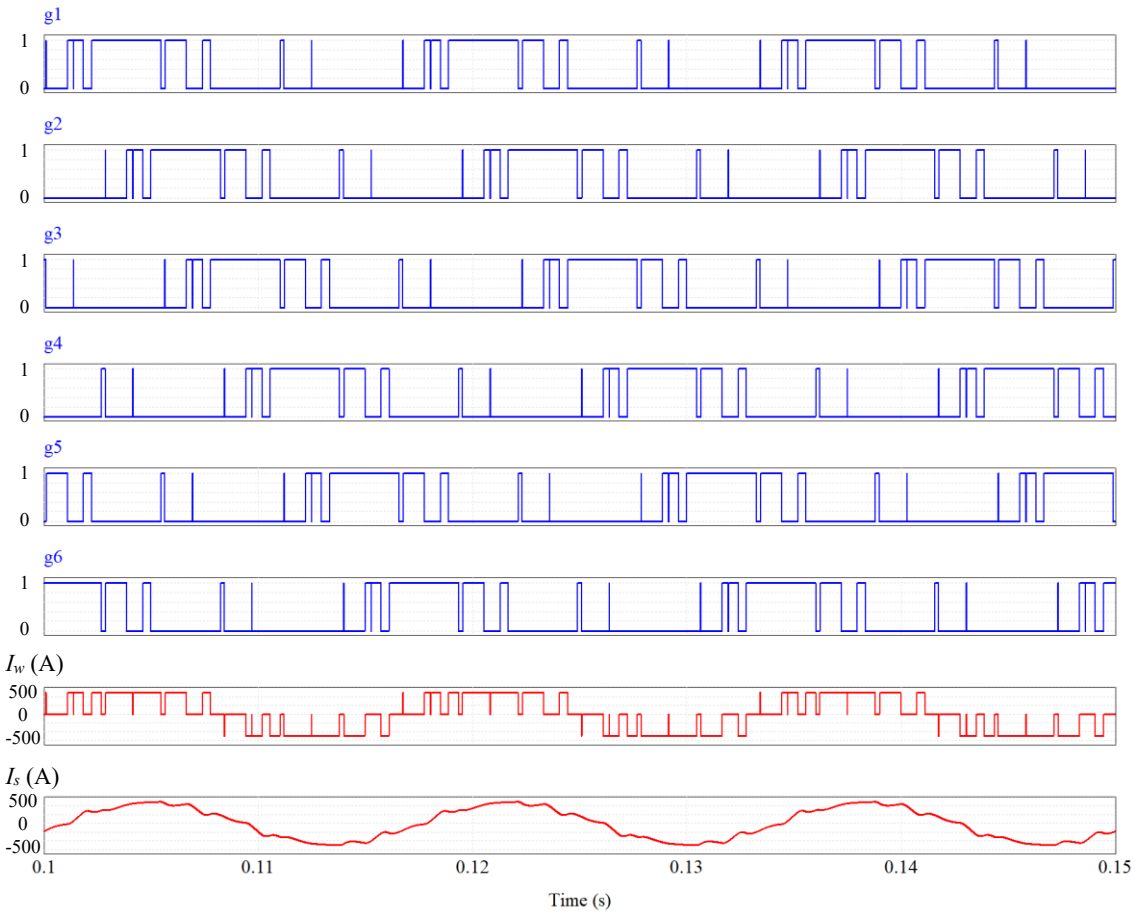

Figure 3-17 Simulated gating singles, i_w, and i_s in topology A with the SVM (SQ5) scheme.

The simulated power losses of the switching device S_{11} in topology A with the SVM (SQ5) scheme are shown in Figure 3-18. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses are shown in blue, and the switching losses are shown in red. The result shows the conduction losses are the primary losses in the IGBT, whereas the switching losses are the major losses in the diode. The IGBT has more

conduction losses but fewer switching losses than the diode. The IGBT generates more losses than the diode.

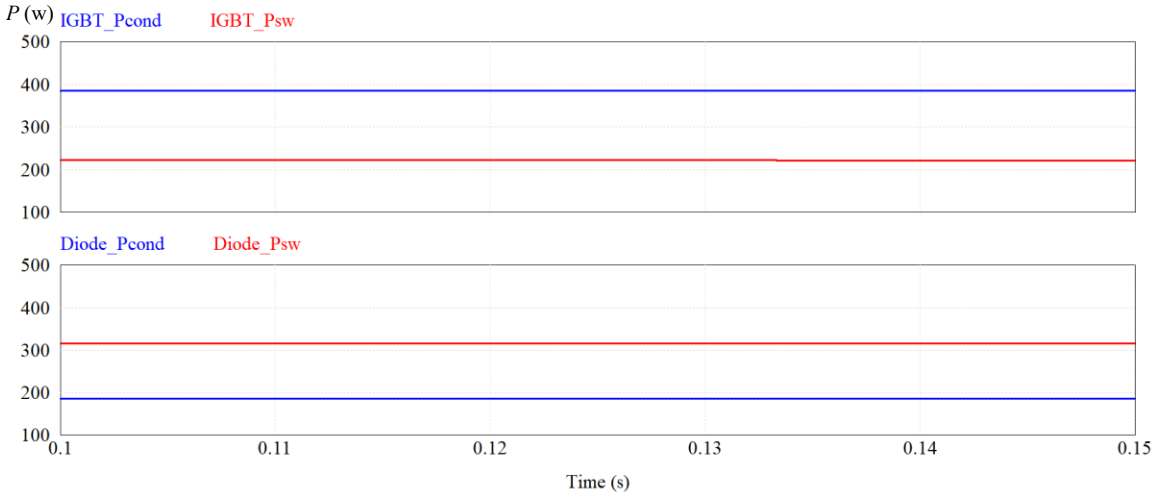

Figure 3-18 Simulated power losses of one switching device in topology A with the SVM (SQ5) scheme.

The simulated gating singles with the output PWM current i_w and output current i_s in topology A with the SVM (SQ6) scheme are shown in Figure 3-19. The gating signals of the six switching devices in the CSI #1 are shown in blue. The output PWM current i_w and the output current i_s are presented in red. There are nine pulses per half cycle in the output PWM current i_w with a switching frequency of 540 Hz.

The simulated power losses of the switching device S_{11} in topology A with the SVM (SQ6) scheme are shown in Figure 3-19. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses are shown in blue, and the switching losses are shown in red. The result shows the conduction losses are the main losses in the IGBT, whereas the switching losses are the primary losses in the diode. The IGBT has more conduction losses but fewer switching losses than the diode. The IGBT generates more losses than the diode.

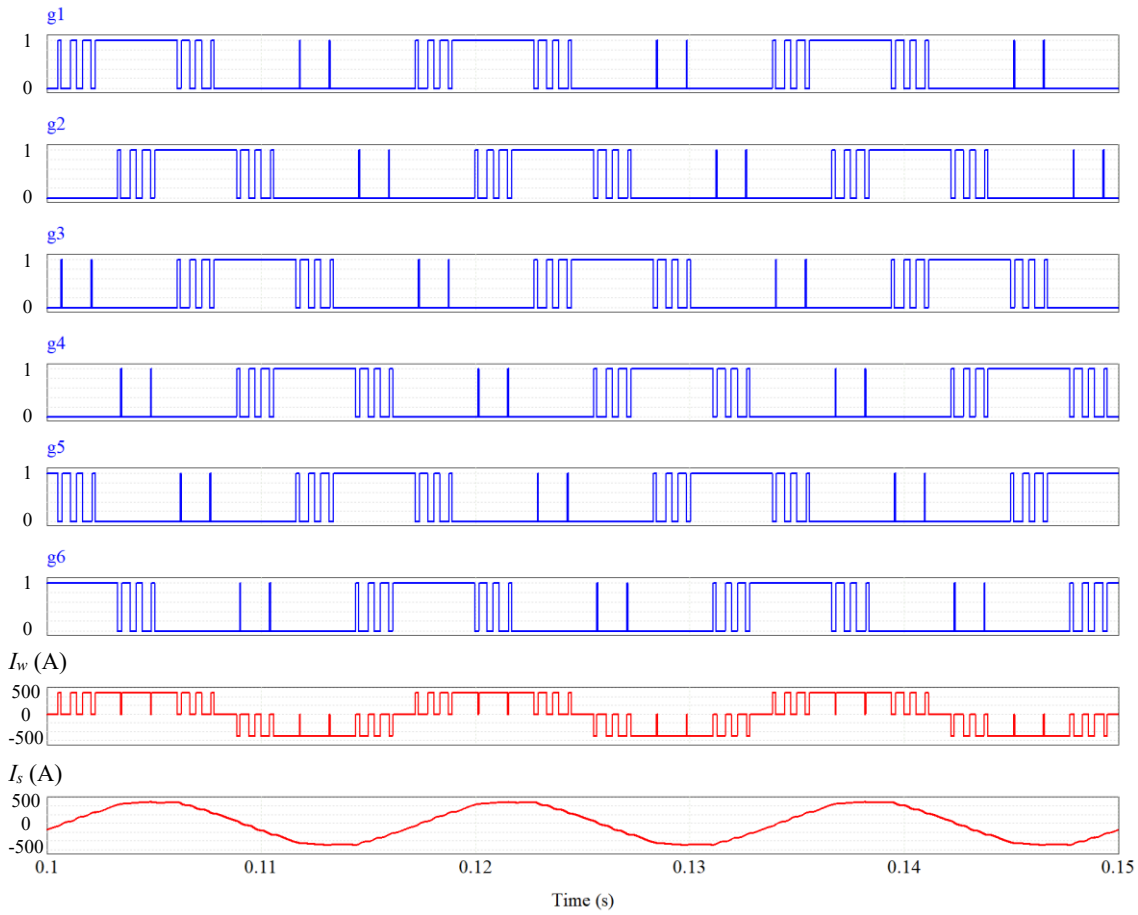

Figure 3-19 Simulated gating singles, i_w, and i_s in topology A with the SVM (SQ6) scheme.

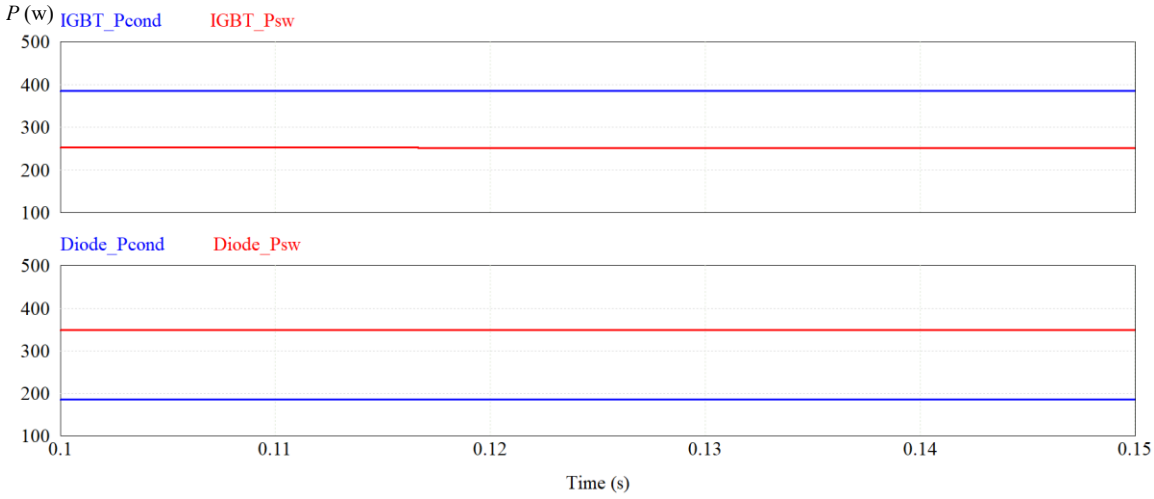

Figure 3-20 Simulated power losses of one switching device in topology A with the SVM (SQ6) scheme.

The simulated power losses of SC-CSIs in topology A with different modulation schemes are shown in Table 3-4. All the six switching sequences of the SVM scheme are included. The simulated power loss comparison among different modulation schemes in topology A is shown in Figure 3-21. The conduction losses are presented in blue. The switching losses are presented in orange.

Table 3-4 Simulated power losses in topology A

Modulation scheme	Conduction losses (W)	Switching losses (W)	Total power losses (W)	Efficiency
TPWM	6864.72	4950.96	11815.68	99.22%
SHE	6854.44	5174.88	12029.32	99.17%
SQ1	6860.60	9659.53	16520.14	98.80%
SQ2	6866.80	9573.34	16440.13	98.80%
SQ3	6858.62	8660.52	15519.14	98.94%
SQ4	6866.80	9571.92	16438.72	98.76%
SQ5	6860.62	6476.04	13336.66	99.00%
SQ6	6854.44	7211.18	14065.62	99.00%

The simulated results show the conduction losses are almost the same with different modulation schemes. However, the switching losses are different with different modulation schemes due to the different switching voltages. Note that the switching frequencies in SQ3 and SQ5 are 480 Hz. Switching frequencies can also influence the switching losses. The result shows the SVM (SQ1) results in the highest power losses in topology A, however, SVM (SQ4) leads to the lowest efficiency of 98.76%. Although the input current waves are the same in SC-CSIs with different modulation schemes, the input voltage waves have little difference due to the different switching states generated by different modulation schemes. Whereas using the TPWM scheme leads to the lowest power losses in topology A with the highest efficiency of 99.2%, followed by the SHE scheme.

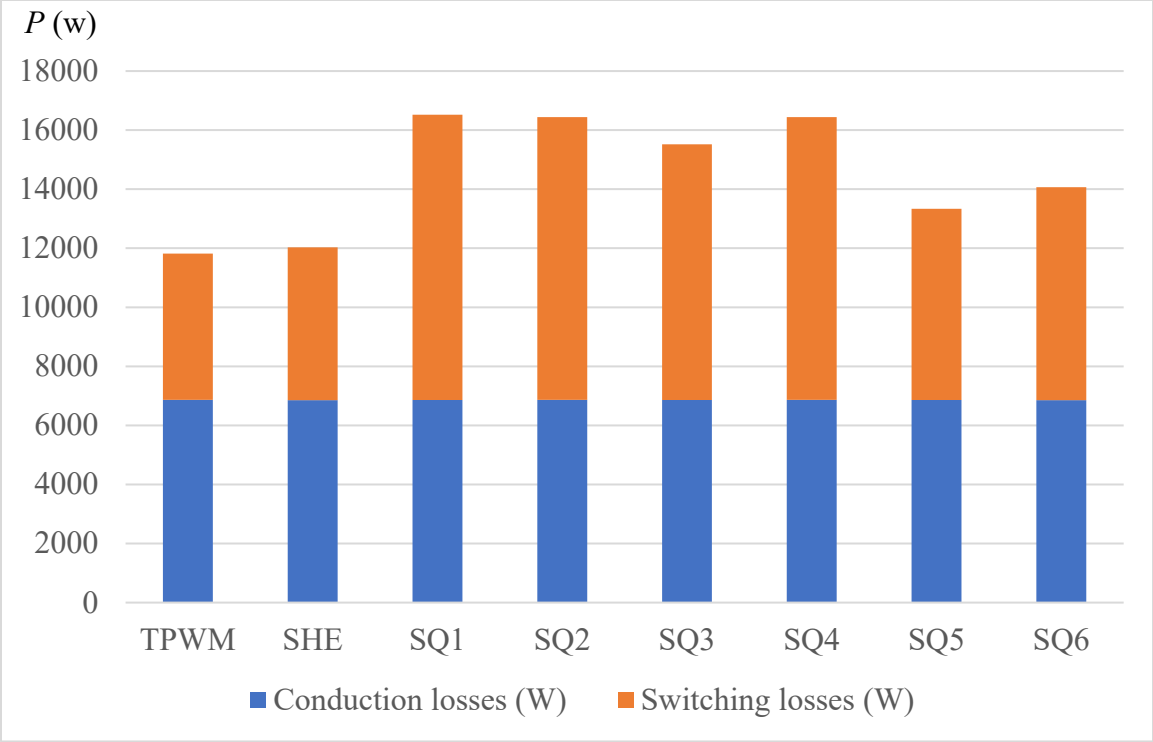

Figure 3-21 Simulated power losses in topology A with different modulation schemes.

(b) Topology B

The simulated gating singles with the output PWM current i_w and output current i_s in topology B with the square-wave operation are shown in Figure 3-22. The gating signals of the six switching devices in the CSI #1 are shown in blue. The output PWM current i_w and the output current i_s are presented in red. The output PWM current i_w is a three-level square wave current with a switching frequency of 60 Hz. The simulated results of the power losses of SC-CSIs in topology B are shown in Table 3-5. The switching losses are comparatively low due to the switching frequency of 60 Hz leading to high efficiency. The simulated power losses of one switching device in topology B have been shown in Figure 2-12 in Chapter 2, thus, will not be present here again.

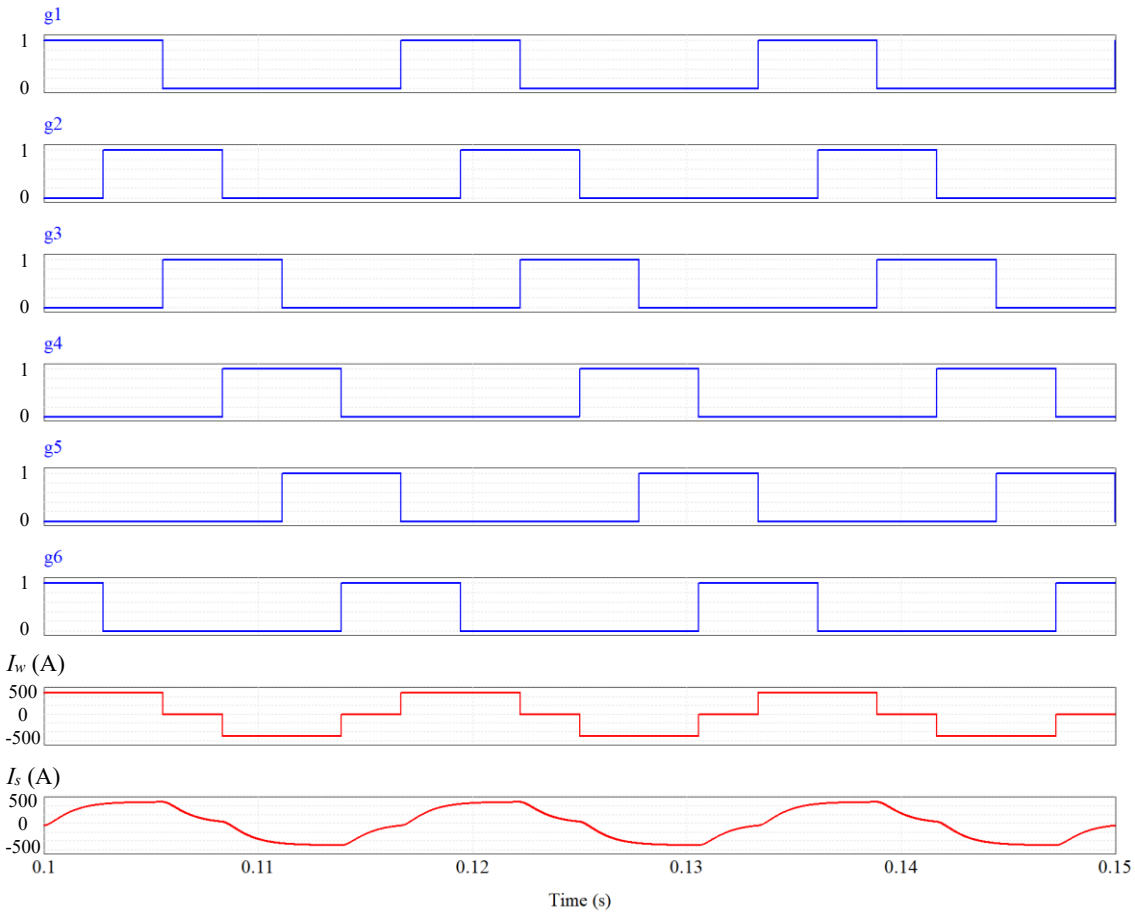

Figure 3-22 Simulated gating singles, i_w, and i_s in topology B with the square-wave operation.

Table 3-5 Simulated power losses in topology B

Modulation scheme	Conduction losses (W)	Switching losses (W)	Total power losses (W)	Efficiency
Square-wave operation	6862.72	1238.76	8101.48	99.45%

(c) Topology C

The simulated gating singles with the output PWM current i_w and output current i_s in the CSI #1 of topology C with different modulation are the same as those presented in topology A, thus, will not be shown again. The simulated power losses of the switching devices S_{11} and S_{21} in topology C with the TPWM, SHE, SVM (SQ1), SVM (SQ2), SVM (SQ3), SVM (SQ4), SVM (SQ5), and SVM (SQ6) schemes are shown from Figure 3-23 to Figure 3-30.

S_{11} is the switch on the first row and S_{21} is an inner switch in topology C. The top one shows the IGBT losses, and the bottom one presents the diode losses. The conduction losses of the 3300 V device (S_{11}) and the 6500 V device (S_{21}) are shown in blue and green respectively. The switching losses of the 3300 V device and the 6500 V device are shown in red and pink respectively.

As shown in Figure 3-23, the power losses of the 3300 V IGBT and the 6500 V IGBT are different. A similar result can be found in the diodes. The devices with a voltage rating of 6500 V are employed as the inner switches in topology C due to the double voltage stress. It can be seen from the simulated result that topology C has a different power loss distribution from topology A and topology B.

Besides, the switching losses of the 6500 V IGBT are more than twice that of the 3300 V IGBT. And the conduction losses of the 6500 V IGBT are less than twice that of the 3300 V IGBT. These can also be found when comparing the power losses between the 6500 V diode and the 3300 V diode. These are consistent with the analysis and can be found in other simulation results.

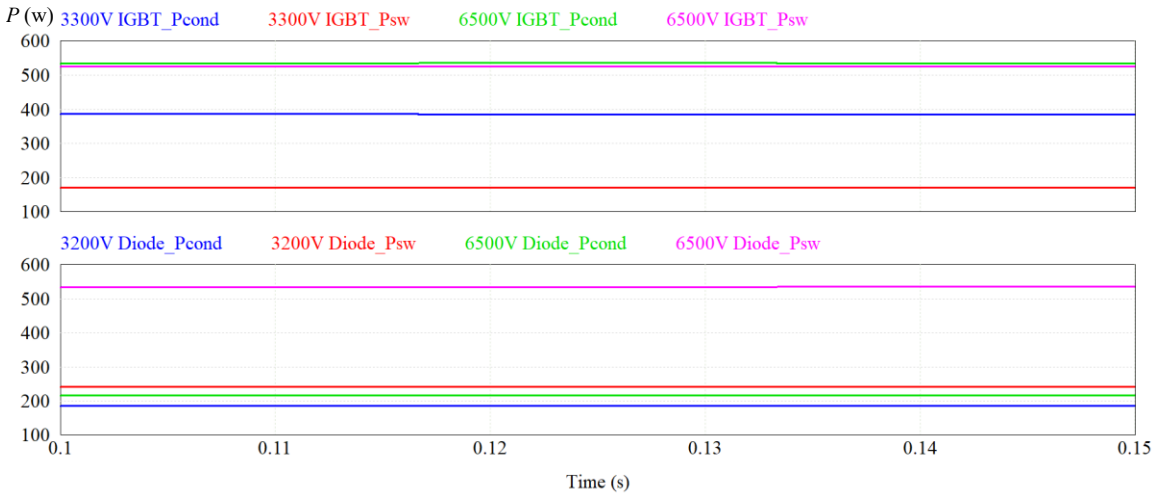

Figure 3-23 Simulated power losses of the switching devices in topology C with the TPWM scheme.

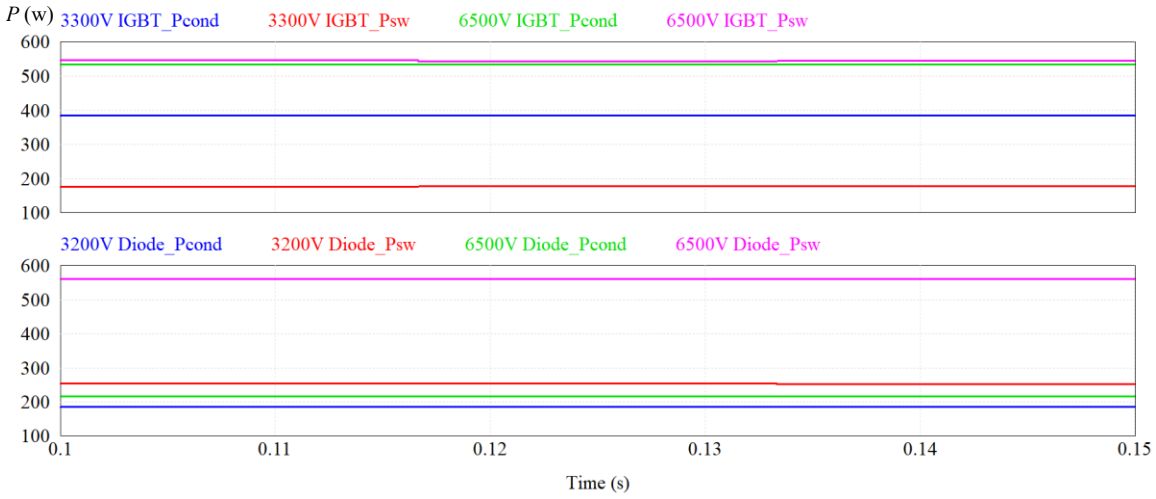

Figure 3-24 Simulated power losses of the switching devices in topology C with the SHE scheme.

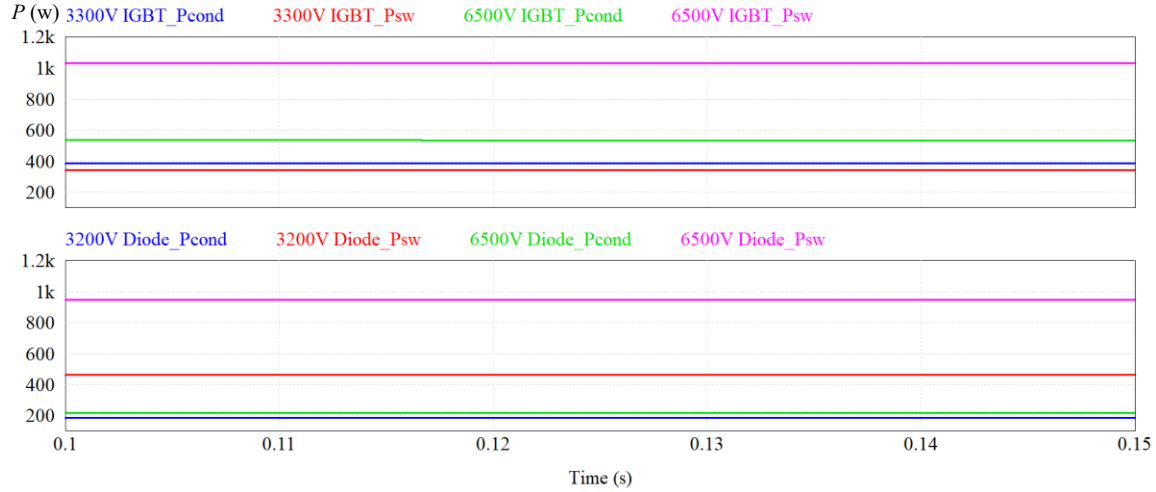

Figure 3-25 Simulated power losses of the switching devices in topology C with the SVM (SQ1) scheme.

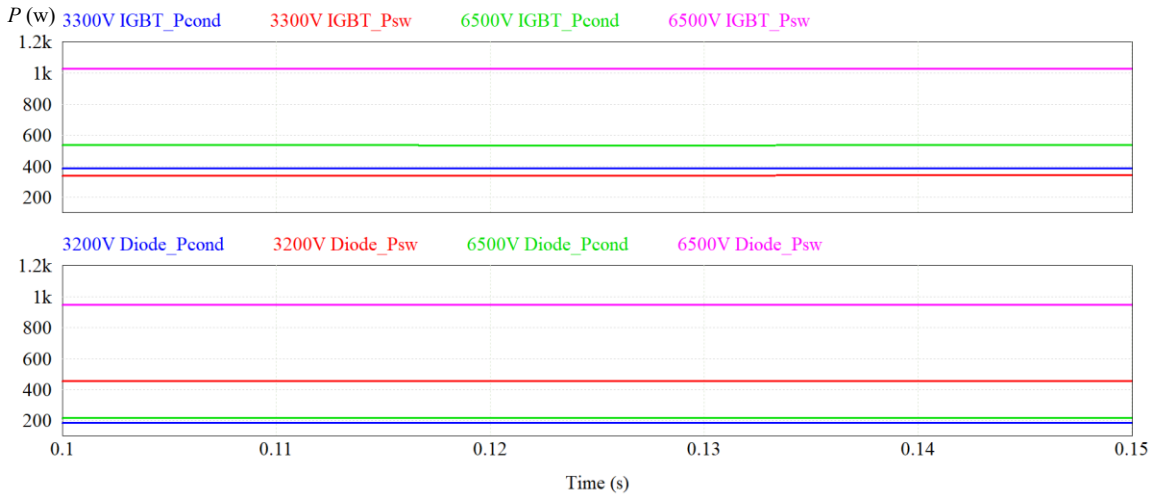

Figure 3-26 Simulated power losses of the switching devices in topology C with the SVM (SQ2) scheme.

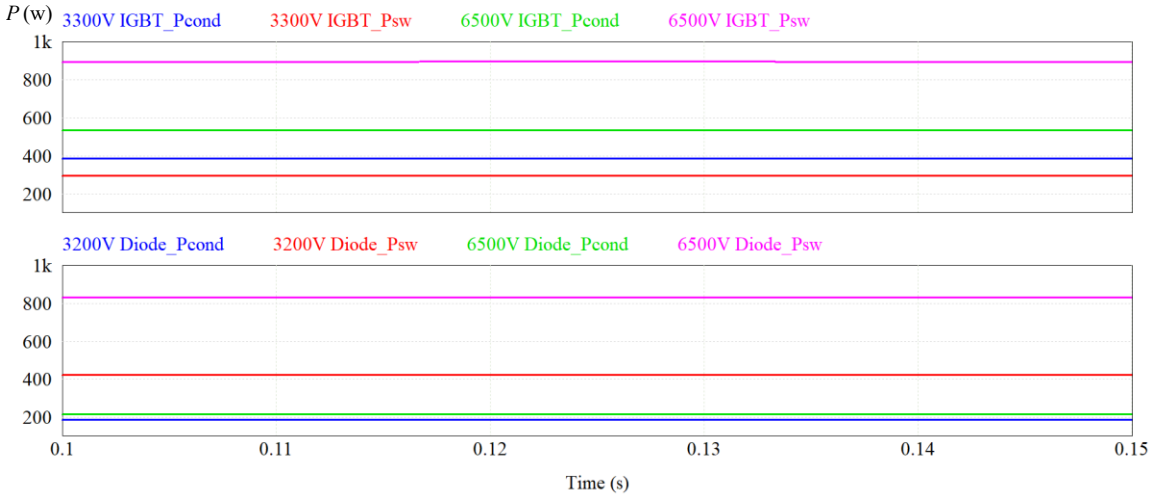

Figure 3-27 Simulated power losses of the switching devices in topology C with the SVM (SQ3) scheme.

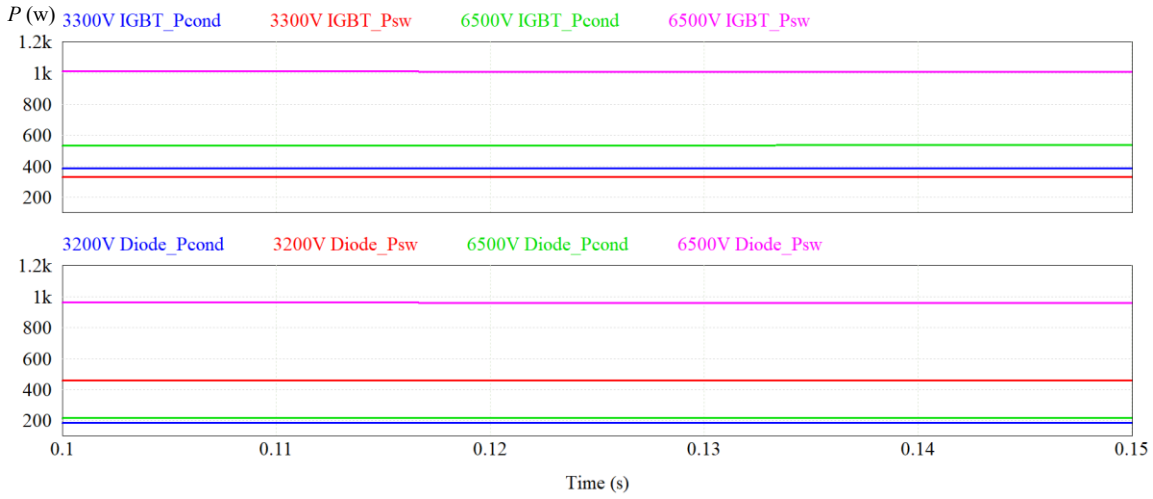

Figure 3-28 Simulated power losses of the switching devices in topology C with the SVM (SQ4) scheme.

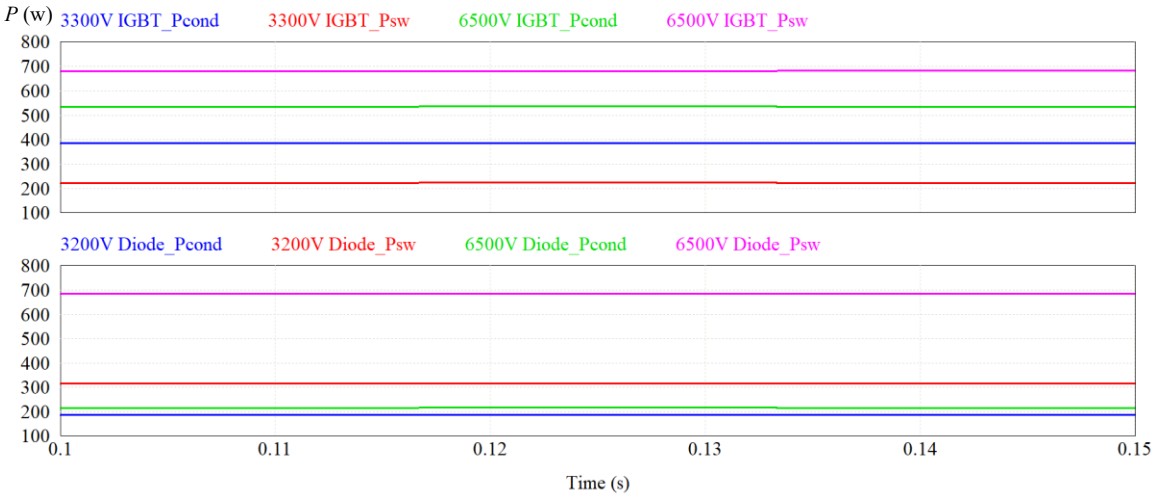

Figure 3-29 Simulated power losses of the switching devices in topology C with the SVM (SQ5) scheme.

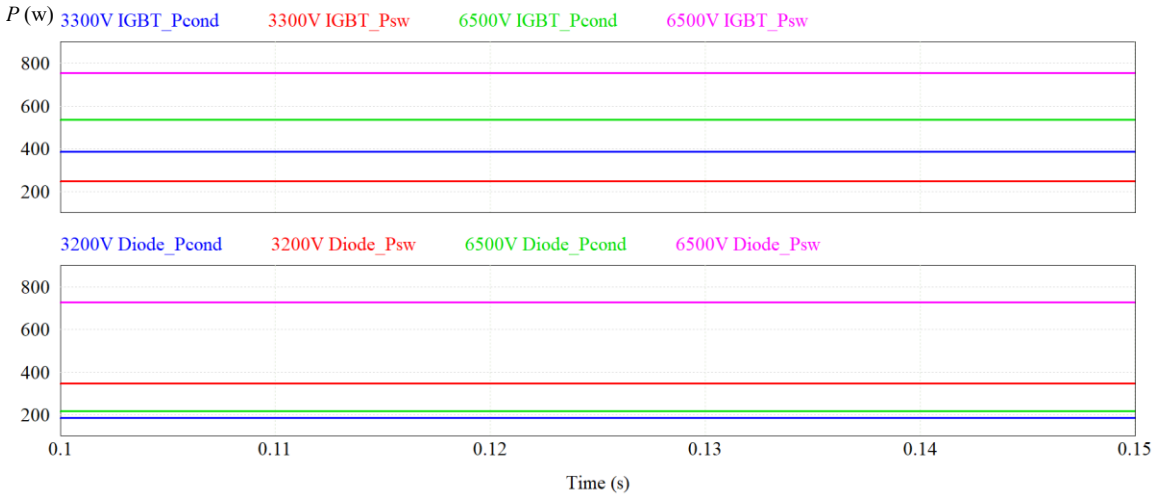

Figure 3-30 Simulated power losses of the switching devices in topology C with the SVM (SQ6) scheme.

The simulated power losses of SC-CSIs in topology C with different modulation schemes are shown in Table 3-6. The simulated power loss comparison among different modulation schemes in topology C is shown in Figure 3-31. The conduction losses are presented in blue. The switching losses are presented in orange.

Table 3-6 Simulated power losses in topology C

Modulation scheme	Conduction losses (W)	Switching losses (W)	Total power losses (W)	Efficiency
TPWM	5689.47	5650.83	11340.30	99.25%
SHE	5680.20	5909.95	11590.15	99.20%
SQ1	5681.26	10766.70	16447.96	98.81%
SQ2	5686.38	10702.33	16388.70	98.80%
SQ3	5683.29	9518.97	15202.26	98.96%
SQ4	5685.52	10752.78	16438.30	98.75%
SQ5	5686.41	7333.05	13019.46	99.01%
SQ6	5678.17	8088.29	13766.47	99.03%

The simulated results show using different modulation schemes does not influence the conduction losses, but it affects the switching losses due to the change of the switching voltages. The switching frequencies in SQ3 and SQ5 are 480 Hz. And switching frequencies can directly influence the switching losses. The comparison shows the SVM (SQ1) results

in the highest power losses. The SVM (SQ4) leads to the lowest efficiency of 98.75%. Whereas using the TPWM scheme leads to the lowest power losses in topology C with the highest efficiency of 99.25%, followed by the SWM scheme.

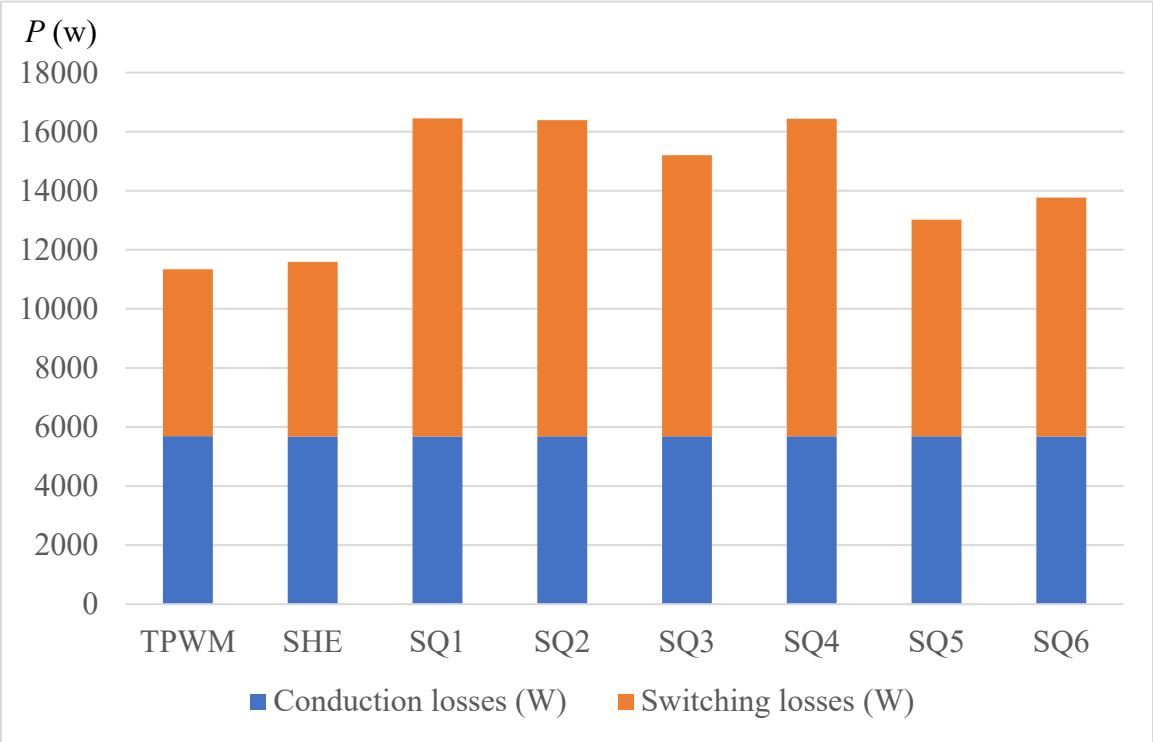

Figure 3-31 Simulated power losses in topology C with different modulation schemes.

3.3.2 Simulated power loss comparison

The simulated power loss comparison among topology A, topology B, and topology C with different modulation schemes are presented in Figure 3-32. The names under each bar have used the form (the modulation scheme – the topology). For example, TPWM-A presents the power losses of topology A using the TPWM scheme. The result shows among all the combinations, topology B with the square-wave operation has the lowest power losses with the highest efficiency of 99.45%, followed by topology C with the TPWM scheme with an efficiency of 99.25%. Whereas topology A with the SVM (SQ1) scheme has the highest power losses, and topology C with the SVM (SQ4) scheme has the lowest efficiency of 98.75%. The conduction losses are almost the same between topology A and topology B due to the same conduction current, duty cycle, switching device, and quantity.

Whereas topology C has lower conduction losses, which has been analyzed in Chapter 2. The SC-CSIs with different modulation schemes have different switching losses. This can be explained from two perspectives. The first part is from the switching voltages which are changed in different modulation schemes. The second part is from the switching frequency which might be different in different modulation schemes. For example, the switching frequency in the square-wave operation is 60 Hz. It becomes 480 Hz in the SWM (SQ3) and SWM (SQ5) schemes. And the switching frequency is 540 Hz in the rest modulation schemes.

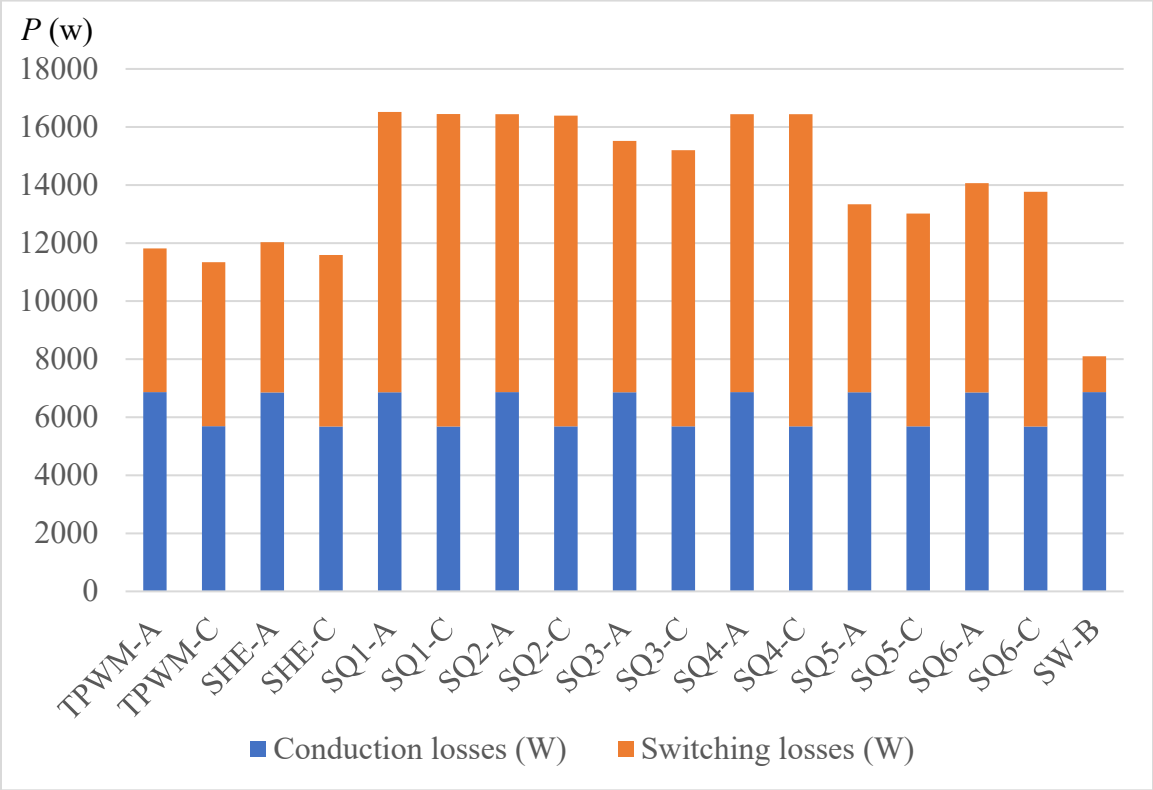

Figure 3-32 Simulated power loss comparison of SC-CSIs with different modulation schemes.

3.4 Summary

The power losses of SC-CSIs with different modulation schemes are investigated in this chapter. Firstly, the power losses of SC-CSIs can be affected by modulation schemes. The power loss distributing will not be influenced by using different modulation schemes.

Secondly, using different modulation schemes has no impact on the conduction losses of SC-CSIs. However, the switching losses can be influenced by modulations from two perspectives. The first part is from the switching voltages which can be changed by using different modulation schemes and/or modulation index. The second part is from the switching frequency which might be different in different modulation schemes. Finally, among all the combinations, topology B with the square-wave operation has the lowest power losses with the highest efficiency of 99.45%, followed by topology C with the TPWM scheme with an efficiency of 99.25%. Whereas topology A with the SVM (SQ1) scheme has the highest power losses, and topology C with the SVM (SQ4) scheme has the lowest efficiency of 98.75%.

Chapter 4
Conclusions

The power losses and the power loss distribution of SC-CSIs are investigated in this thesis. The factors that can influence the power losses of SC-CSIs are analyzed in detail. The power losses and power loss distribution of SC-CSIs in three topologies with the typical modulation scheme are analyzed in Chapter 2. The power losses and power loss distribution of SC-CSIs in three topologies with different modulation schemes are investigated in Chapter 3. The contributions and conclusion of the research and the future work are summarized in this chapter.

4.1 Contributions and conclusions

The main contributions and conclusions of this thesis are summarized as follows.

(1) Factors affecting the power losses of SC-CSIs are investigated and analyzed.

The conduction losses of the SC-CSIs can be influenced by the conduction current and the saturation voltage of the switching devices. The switching losses of the SC-CSIs can be affected by the modulation scheme, the modulation index, the switching frequency, the current and voltage of the switching device when switching, and the turn-on and turn-off energy losses of the switching devices. The higher values of these parameters, the higher the power losses of SC-CSIs.

(2) The power losses and power loss distribution of SC-SCIs with a typical modulation scheme are investigated.

When SC-CSIs operate under the same conditions, topology A and topology C have almost the same total power losses, where the total power losses of topology A are slightly higher than that of topology C. Topology A has fewer switching losses but more conduction losses than topology C. The efficiency of topology C, 98.81% is slightly higher than that of topology A 98.8%, though the difference is very small. Among the three topologies, topology B has the fewest power losses with the highest efficiency of 99.41%. Furthermore,

topology A and topology B have the same power loss distribution. Topology C has a different power loss distribution. Every switch in topology A contributes the same power losses. The same result can be found in topology B. Whereas in topology C, every switch on the first and last rows has the same power losses as any switch in topology A, however, every inner switch in topology C contributes more power losses.

(3) The power losses and power loss distribution of SC-CSIs with different modulation schemes are investigated.

The power loss distributing will not be influenced by using different modulation schemes. However, the power losses of SC-CSIs can be affected by modulation schemes. Using different modulation schemes has no impact on the conduction losses of SC-CSIs. But the switching losses can be influenced by modulations from two perspectives. The first part is from the switching voltages which are changed with modulation schemes. The second part is from the switching frequency which might be different in different modulation schemes.

(4) The best modulation for each topology is recommended.

Among all the combinations, topology B with the square-wave operation has the lowest power losses with the highest efficiency of 99.45%. Besides, in topology A and topology C, using the TPWM scheme leads to the lowest power losses with the highest efficiency, which is 99.22% and 99.25% respectively.

4.2 Future work

The following work is suggested for future research.

The power losses of SC-CSIs will influence the efficiency of the inverter and the whole system as well. Lowering the power losses of SC-CSIs can improve efficiency and save operation costs. Therefore, new topologies of SC-CSIs, new modulation schemes, and new advanced switching devices for SC-CSIs with lower power losses are expected and worth to be investigated.

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