Carrier-Based PWM Equivalent to Multilevel Multiphase Space Vector PWM Techniques

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Abstract—The space vector pulse width modulation (PWM) (SVPWM) techniques enhance the performance of multilevel multiphase inverters. With multilevel (three-phase) inverters and with (two-level) multiphase inverters, it is widely accepted that the typical SVPWM strategies have an equivalent carrier-based PWM (CBPWM) counterpart, which produces identical results. However, the conclusions reached in the papers that show these cannot be applied, nor even extended, to SVPWM techniques with more than two levels and three phases. This paper shows that the most widely accepted multilevel multiphase SVPWM techniques have a fully equivalent CBPWM counterpart, which consists of a phase disposition PWM (PDPWM) with an appropriate zero-sequence injection scheme. Closed-form expressions to calculate the zero sequences are provided. The proposed modulation techniques are simulated and then implemented in a field-programmable gate array (FPGA), showing that the equivalent CBPWM techniques produce identical results as the original SVPWM ones, but with a significant reduction of hardware requirements. The proposed methodology can be generalized to other multilevel multiphase SVPWM techniques.

Index Terms—carrier-based pulse width modulation (PWM) (CBPWM), field-programmable gate array (FPGA), multiphase drive, space vector PWM (SVPWM), voltage source inverter (VSI).

NOMENCLATURE

Vectors and matrices are printed in bold type while normal type is used for scalars. Lower case is used for normalized variables. Voltages are normalized with respect to the multilevel voltage source inverter (VSI) voltage step $V_{\rm dc}$ and times with respect to the switching period T. Variables related to reduced vectors, i.e., $(P-1)$-dimension ones, are written in Greek letters. Superscripts (k) denote the phase, i.e., the vector component, e.g., $v_r{}^k$ is the component (phase) k of vector $\mathbf{v}_r$. Numeric subscripts $(j$ or $m)$ are used to denote the position of vectors and indexes within a sequence. A hat $(\hat{\mathbf{v}})$ denotes a vector with its components sorted in descending order.

TABLE I
MULTILEVEL MULTIPHASE SVPWM TECHNIQUES UNDER STUDY

Multilevel multiphase SVPWM technique	Acronym
Thee-level five-phase d-q SVPWM in [9]	SVPWM-5A
Thee-level five-phase d-q SVPWM in [10]	SVPWM-5B
Thee-level six-phase d-q SVPWM in [11]	SVPWM-6
Thee-level seven-phase d-q SVPWM in [12]	SVPWM-7A
Thee-level seven-phase d-q SVPWM in [13]	SVPWM-7B
Basic multidimensional SVPWM [14]	SVPWM-B
Multidimensional SVPWM with redundancy [15]	SVPWM-R

I. INTRODUCTION

MULTIPHASE machines [1]–[3] have important benefits, which have been discussed in many excellent reviews published recently [4]–[7]. Multilevel multiphase drives combine such benefits with those well-known of the multilevel technology [8]. Application of space vector pulse width modulation (PWM) (SVPWM) to multilevel multiphase inverters permits to improve the overall drive performance. Available multilevel multiphase SVPWM are summarized in Table I and classified into d-q SVPWM techniques and multidimensional SVPWM techniques.

The d-q SVPWM techniques perform the calculation in the d-q subspaces of the multiphase machine, which offers an excellent insight into the behavior of the drive and facilitates developing high-performance PWM techniques [16]. Nevertheless, designing a PWM technique in the d-q frame is challenging because the selection of the switching vectors has to be made by considering all their components in every d-q subspace [16], with the additional inconveniences of their number growing exponentially [17], and their disposition into subspaces changing erratically with the phase number. These considerations make the adaptation of a particular d-q SVPWM algorithm to another case with a different number of phases or levels unfeasible. As a result, there is no general d-q SVPWM for any number of levels and phases. All the reported multilevel multiphase d-q SVPWM techniques, listed in Table I, are for particular cases of VSI levels and phases so far. The PWM techniques in this table intended for the same case differ basically in the use of the inverter switching state redundancy. The multidimensional SVPWM techniques avoid the d-q subspace decomposition and follow a more straightforward approach by formulating the problem in a multidimensional vector space, which permits to obtain very

general modulation algorithms at the expense of less insight into the behavior of the drive. The two multidimensional SVPWM in Table I can be applied to VSIs with any number of levels and phases. The SVPWM-R takes advantage of the switching vector redundancy to reduce the switching losses, and to support the accomplishment of complementary tasks like the equal distribution of power losses or the balancing of floating capacitors. Note that advanced modulation issues, like discontinuous modulation, random modulation or overmodulation methods, which have been addressed in multilevel three-phase SVPWM [18] and two-level multiphase SVPWM [1], [19], have not been studied in multilevel multiphase SVPWM applications so far. Despite the fact that all the SVPWM techniques in Table I are only defined in the linear region, the multidimensional ones can manage any number of levels, which permits to use the saturation of the output switching vectors as a basic overmodulation method.

The equivalence between the carrier-based PWM (CBPWM) and the SVPWM techniques has been studied just for the multilevel (three-phase) VSIs [20], [21] and for (two-level) VSIs [22], and the result of the studies cannot be generalized for the multilevel multiphase applications. For instance, the zero-sequence injection schemes for three-phase inverters in [20] and [21] cannot be extended to the five-phase SVPWM-R case because they are based on the well-known graphical two-dimensional space-vector diagrams of three-phase inverters, and the five-phase SVPWM-R is based on a very different four-dimensional algebraic approach, which has no graphical two-dimensional representation. The zero-sequence scheme for two-level five-phase inverters [22] cannot be extended for the three-level case in [9], [10] either, because the two-level space-vector diagram, with 31 vectors, is very different from the three-level one, which has 243 vectors. Comparisons between multilevel multiphase CBPWM and SVPWM are sparse, and the knowledge of this topic is very limited [5]. Just some performance similarities have been identified in the cases of the SVPWM-5B [12], the SVPWM-7B [13] and the SVPWM-6 [11], but there is no evidence to suggest that they produce identical results to a CBPWM technique. The SVPWM-5A and the SVPWM-7A relationships with the CBPWM have not been studied at all.

The contribution of this paper is to demonstrate that there is a CBPWM alternative equivalent to each of the high performance multilevel multiphase SVPWM techniques. The equivalent CBPWM techniques generate the same output voltages and make the same use of the switching vector redundancy, as a consequence of producing identical transistor trigger signals, but with the benefit of a significant reduction in the computation complexity. The equivalent CBPWM techniques consist of a phase disposition (PD) PWM (PDPWM) with appropriate zero sequence injection schemes. Closed-form expressions to calculate these zero-sequences are deduced throughout the paper. Simulations and experimental tests with an field-programmable gate array (FPGA) are carried out to validate the equivalent CBPWM techniques and to assess the reduction of the hardware requirements. The methodology followed in this paper and the general zero-sequence calculation equation deduced in this work can be applied to other

multilevel multiphase SVPWM techniques, provided they meet certain conditions.

The rest of the paper is organized as follows. The CBPWM techniques equivalent to the multidimensional SVPWM and the d-q SVPWM techniques are obtained in Sections II and III, respectively. Section IV validates the equivalent CBPWM techniques by simulation and experiments. Finally, Section V concludes the work.

II. CBPWM EQUIVALENT TO THE MULTIDIMENSIONAL SVPWM

The multilevel CBPWM alternatives are classified by the disposition of the carriers and the zero-sequence injection scheme. According to the carrier disposition the basic alternatives are the PDPWM, the phase opposition disposition PWM and the alternative phase opposition disposition PWM [18]. Regarding the the zero-sequence injection schemes, a widely used continuous modulation strategy is the one obtained with the double min-max zero-sequence injection scheme [10], [18], [23], [24], in which the zero sequence is

$$v_z = v_{z1} + v_{z2} \tag{1a}$$

where

$$v_{z1} = v_o - \frac{\min_k(v_r{}^k) + \max_k(v_r{}^k)}{2} \tag{1b}$$

$$v_{z2} = \frac{1}{2} - \frac{\min_k(v'_f{}^k) + \max_k(v'_f{}^k)}{2} \tag{1c}$$

$$v'_f{}^k = (v_r{}^k + v_{z1}) - \text{integ}(v_r{}^k + v_{z1}) \tag{1d}$$

and v_o is the normalized voltage of the dc-bus midpoint. Discontinuous modulation strategies are those that clamp an arbitrary phase k to a certain output level l during the whole switching period, in which the zero-sequence is [18], [25]

$$v_z = l - v_r{}^k \tag{2}$$

where $v_r{}^k$ is the normalized voltage reference for phase k. Application of (1) and (2) is possible for the wide range of multilevel topologies that produce equally-spaced (by V_{dc}) output-voltage levels, as is the case for diode clamped, flying capacitor and cascaded full-bridge multilevel inverters [18].

A. CBPWM Equivalent to the SVPWM-B

In the SVPWM-B technique, the normalized reference voltages are gathered in a P-dimensional vector, which is afterward decomposed into its integer and fractional parts: $\mathbf{v}_r = \mathbf{v}_i + \mathbf{v}_f$ [14]. Then, the fractional part $\mathbf{v}_f$ is modulated by using an inner two-level modulator to obtain a two-level displaced switching vector sequence $\{\mathbf{v}_{dj}\}$. Finally, the integer part is added to every element of the two-level vector sequence to obtain the multilevel multiphase switching vector sequence $\{\mathbf{v}_{sj}\} = \{\mathbf{v}_i + \mathbf{v}_{dj}\}$. The Matlab function used to implement the SVPWM-B algorithm, which makes use of a inner two-level SVPWM function to carry out the two-level modulator, is provided in the supplementary material of this paper.

Two-level multiphase SVPWM

	$\mathbf{v}_{d1}$	$\mathbf{v}_{d2}$	$\mathbf{v}_{d3}$	$\mathbf{v}_{d4}$	$\mathbf{v}_{d5}$	$\mathbf{v}_{d6}$
$v_f{}^a = \hat{v}_f{}^a$	0	1	1	1	1	1
$v_f{}^b = \hat{v}_f{}^b$	0	0	1	1	1	1
$v_f{}^c = \hat{v}_f{}^e$	0	0	0	0	0	1
$v_f{}^d = \hat{v}_f{}^d$	0	0	0	0	1	1
$v_f{}^e = \hat{v}_f{}^c$	0	0	0	1	1	1

$t_1 = 1 - \hat{v}_f{}^a$ $\quad$ $t_3 = \hat{v}_f{}^b - \hat{v}_f{}^c$ $\quad$ $t_5 = \hat{v}_f{}^d - \hat{v}_f{}^e$

$t_2 = \hat{v}_f{}^a - \hat{v}_f{}^b$ $\quad$ $t_4 = \hat{v}_f{}^c - \hat{v}_f{}^d$ $\quad$ $t_6 = \hat{v}_f{}^e$

Two-level CBPWM with leading-edge sawtooth carrier

Leading-edge sawtooth carrier

$v_f{}^a$, $v_f{}^b$, $v_f{}^e$, $v_f{}^d$, $v_f{}^c$

Same switching output voltage waveforms for both PWM

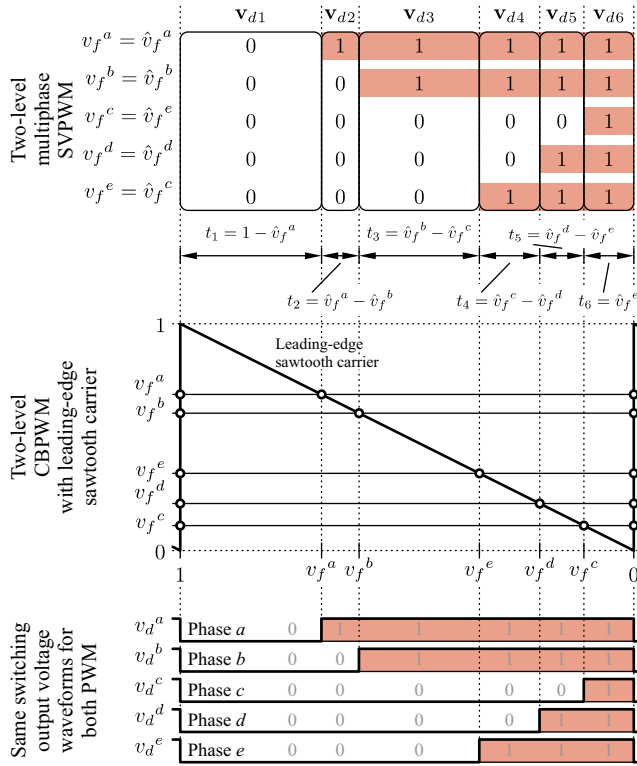|		v_{d1}	v_{d2}	v_{d3}	v_{d4}	v_{d5}	v_{d6}
$v_d{}^a$	Phase a	0	1	1	1	1	1
$v_d{}^b$	Phase b	0	0	1	1	1	1
$v_d{}^c$	Phase c	0	0	0	0	0	1
$v_d{}^d$	Phase d	0	0	0	0	1	1
$v_d{}^e$	Phase e	0	0	0	1	1	1

Fig. 1. Equivalence between the two-level multiphase SVPWM and the CBPWM with leading-edge sawtooth carrier. (Example considering $\mathbf{v}_f = [0.69, 0.60, 0.11, 0.21, 0.34]^T$ [26]).

The two-level modulator sorts $\mathbf{v}_f$ in descending order to obtain the vector $\hat{\mathbf{v}}_f$, and from it the sequence of $P + 1$ displaced switching vectors $\{\mathbf{v}_{dj}\}$ and their corresponding normalized dwell times $\{t_j\}$ are calculated [14]. The examination of the operations realized by this modulator reveals that all the displaced vector sequences always start with the zero vector $\mathbf{v}_{d1} = [0, 0, \ldots, 0]^T$, gradually increase each phase one by one and end with the vector of ones $\mathbf{v}_{d(P+1)} = [1, 1, \ldots, 1]^T$. The order in which these increases happen is determined by the aforementioned sorting operation. The dwell times are the result of subtracting two consecutive components of vector $\hat{\mathbf{v}}_f$. Fig. 1 illustrates the mathematical operations performed by the two-level SVPWM with a five-phase example in which $1 > v_f{}^a > v_f{}^b > v_f{}^e > v_f{}^d > v_f{}^c > 0$, and compares them with the operations carried out by the CBPWM with leading-edge sawtooth carrier. It is inferred that both techniques produce identical results. It is straightforward to extend this demonstration to reference vectors with their components sorted differently or with another phase number. For each extra phase, just an extra switching vector $\mathbf{v}_{dj}$ arises in the SVPWM sequence, and an extra reference signal $v_f{}^k$ needs to be compared with the sawtooth carrier.

The two-level modulators equivalence seen in Fig. 1 can be extended to the multilevel case since the displacement introduced by the integer part of the reference vector in the SVPWM-B algorithm is equivalent to the shifting of the reference signals to a common carrier band (two-level zone) performed in the practical implementation of the PDPWM [23], [24]. This analysis formally proves that the plain PDPWM with leading-edge sawtooth carriers produces identical results to those obtained with the SVPWM-B, and consequently, no zero-sequence injection scheme is needed in this case, regardless of the number of levels and phases:

$$v_z = 0. \tag{3}$$

Consequently, the PDPWM with triangular carriers is equivalent to the SVPWM-B with the usual symmetrical arrangement of the switching vectors within the switching period.

B. CBPWM Equivalent to the SVPWM-R

The SVPWM-R produces sorted sequences of adjacent switching vectors aiming to minimize the switching losses [15]. Such sequences are made of just P switching vectors, hence it is a discontinuous technique. In this technique, the modulation complementary tasks are managed by selecting a set of P consecutive integer numbers $\{q_m\}$. All the sets produce redundant switching vector sequences that differ just in their common-mode voltage (CMV). Since q_m is defined in [15] as the sum of the components of the mth switching vector of the sequence, the higher the value of the index q_m, the higher the CMV that is produced by that vector. Like the SVPWM-B, the SVPWM-R makes use of the inner two-level modulator seen in Fig. 1, but in this case operating with $(P-1)$-dimension vectors. The Matlab code provided in the supplementary material of this paper shows the implementation details of the SVPWM-R algorithm. The equivalence seen in Fig. 1 between the inner two-level modulator and CBPWM can be extended to the SVPWM-R to prove that it is also equivalent to a PDPWM with an appropriate zero-sequence injection that achieves discontinuous modulation. A detailed analysis of the operations performed with the $\{q_m\}$ indexes in the SVPWM-R algorithm leads to the conclusion that for an arbitrary index sequence $\{q_m\} = \{q_1, \ldots, q_P\}$ this technique clamps the phase

$$k = \begin{cases} x \text{ for which } \hat{\omega}_f{}^{j_P} = \omega_f{}^x & \text{if } j_P < P \\ P & \text{if } j_P = P \end{cases} \tag{4}$$

to the level

$$l = n_P - \operatorname{integ}(v_r{}^k - v_r{}^P) \tag{5}$$

where

$$n_P = \operatorname{integ}\left((q_P - q_i)/P\right) \tag{6a}$$
$$j_P = q_P - q_i - n_P P + 1 \tag{6b}$$

$\hat{\omega}_f{}^{j_P}$ is the j_P-th component of vector $\boldsymbol{\omega}_f$ sorted in descending order, and $\boldsymbol{\omega}_f$ and q_i can be calculated from $\mathbf{v}_r$ with the equations (36) and (50) given in [15], respectively. Then, by replacing (4) and (5) into (2) and with some manipulations, it results that the zero-sequence injection scheme that achieves a (discontinuous) PDPWM equivalent to the SVPWM-R is

$$v_z = \begin{cases} n_P - v_r{}^P - \hat{\omega}_f{}^{j_P} & \text{if } j_P < P \\ n_P - v_r{}^P & \text{if } j_P = P. \end{cases} \tag{7}$$

Note that this is a general expression, valid for any number of levels and phases, like the SVPWM-R technique.
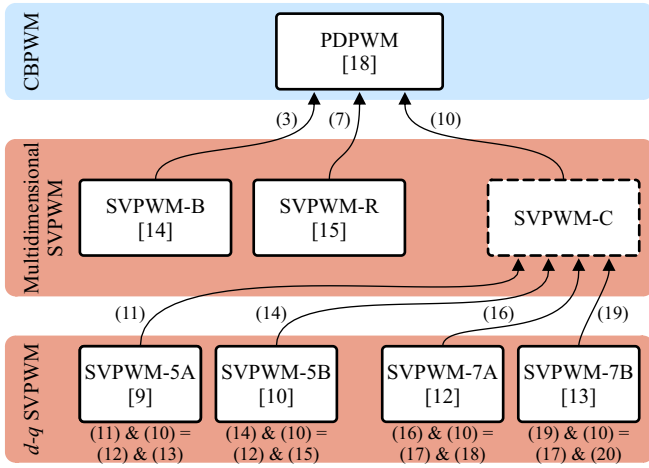
Fig. 2. Diagram of equivalences between the multilevel multiphase SVPWM techniques and the CBPWM, displaying the equations to calculate the corresponding zero-sequence injection scheme.

Fig. 3. Division of sector 1 into regions considered in SVPWM-5A [9].

The upper part of Fig. 2 summarizes the contributions of this paper up to this point. The equivalences between the multilevel d-q SVPWM techniques and the CBPWM one are quite difficult to demonstrate. In what follows, the demonstrations are addressed by means of an ancillary multidimensional SVPWM technique, which is referred to as SVPWM-C in Fig. 2. Such technique is a minor modification of the plain (discontinuous) SVPWM-R to achieve a continuous variant, like the d-q SVPWM techniques under study. It should be noted that the only purpose of this ancillary modulation algorithm is to facilitate the aforementioned demonstration, and not to propose a new standalone technique.

C. SVPWM-C Development and Equivalent CBPWM

A P-phase continuous SVPWM technique requires a sequence of at least $P + 1$ switching vectors. The plain SVPWM-R, as described in [15], produces a sequence of just P switching vectors, which correspond to the selected P consecutive q_m indexes. Therefore, a sequence of $P + 1$ switching vectors is readily obtained by using the SVPWM-R algorithm and selecting one additional consecutive index. The extra switching vector $\mathbf{v}_{s(P+1)}$ obtained in this way is redundant with the first one $\mathbf{v}_{s1}$:

$$\mathbf{v}_{s(P+1)} = \mathbf{v}_{s1} + [1, 1, \ldots, 1]^{\mathrm{T}}. \tag{8}$$

As a consequence, both switching vectors share their dwell times, which are calculated as

$$t_1 = t_{P+1} = \begin{cases} (\hat{\omega}_f{}^{j_P} - \hat{\omega}_f{}^{j_P+1})/2 & \text{if } j_P < P - 1 \\ \hat{\omega}_f{}^{P-1}/2 & \text{if } j_P = P - 1 \\ (1 - \hat{\omega}_f{}^1)/2 & \text{if } j_P = P. \end{cases} \tag{9}$$

From (8), it is inferred that the extra redundant switching vector in the sequence $\mathbf{v}_{s(P+1)}$ adds some CMV to the output, whose normalized value is equal to t_{P+1}. Hence, the zero-sequence injection required to obtain a PDPWM equivalent
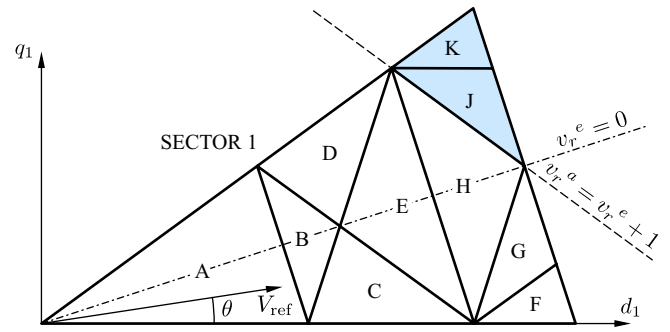
to the SVPWM-C can be calculated by increasing the value calculated with (7) by the amount of t_{P+1} in (9):

$$v_z = \begin{cases} n_P - v_r{}^P - (\hat{\omega}_f{}^{j_P} + \hat{\omega}_f{}^{j_P+1})/2 & \text{if } j_P < P - 1 \\ n_P - v_r{}^P - \hat{\omega}_f{}^{P-1}/2 & \text{if } j_P = P - 1 \\ n_P - v_r{}^P + (1 - \hat{\omega}_f{}^1)/2 & \text{if } j_P = P. \end{cases} \tag{10}$$

III. CBPWM Equivalent to the d-q SVPWM

In what follows, the equivalence between the d-q SVPWM techniques and the CBPWM one is established indirectly by means of the equivalence between the SVPWM-C and the PDPWM, as Fig. 2 shows.

A. CBPWM Equivalent to the SVPWM-5A

The SVPWM-5A is a three-level five-phase d-q SVPWM technique, which is based on the decomposition of the space vectors into two two-dimensional (2D) subspaces [9], namely, d_1-q_1 and d_2-q_2 planes. It divides the linear region of the d_1-q_1 plane into ten sectors, and each sector into ten regions (A–H, J and K), as shown in Fig. 3. The overmodulation region is ignored. The switching vector sequence is determined by identifying the region that the reference vector occupies. The sequences corresponding to every region are designed in [9] taking advantage of the switching vector redundancy to achieve a zero average voltage in the d_2-q_2 plane during each switching period, to minimize the number of switchings, and to improve the balancing of the capacitor voltages of a neutral point clamped VSI. For instance, the sequence that corresponds to the region A in sector 1 is $\{\mathbf{v}_{sj}\} = \{[1, 1, 0, 0, 1]^{\mathrm{T}}, [1, 1, 1, 0, 1]^{\mathrm{T}}, [1, 1, 1, 1, 1]^{\mathrm{T}}, [2, 1, 1, 1, 1]^{\mathrm{T}}, [2, 2, 1, 1, 1]^{\mathrm{T}}, [2, 2, 1, 1, 2]^{\mathrm{T}}\}$, which is made of six adjacent vectors, with the first and the last one being redundant. The same occurs with the sequences corresponding to the remaining regions, and therefore this d-q SVPWM technique is likely to be equivalent to the PDPWM. The switching vector sequences considered in the SVPWM-5A can be obtained by properly selecting the sequence of the $\{q_m\}$ indexes in the five-phase SVPWM-C. According to its definition, the q_m index associated with a certain switching vector is equal to the sum of all its components [15]. The application of this definition to the elements of the switching vector sequences given in Table II in [9] results in $\{q_m\} = \{3, 4, 5, 6, 7, 8\}$

for the regions A to H, and $\{q_m\} = \{2, 3, 4, 5, 6, 7\}$ for the regions J and K. Therefore, for the equivalent SVPWM-C algorithm, only the identification of the boundary between regions H and J is of concern (cf. Fig. 3). Region boundary equations are given in [9] in terms of the magnitude V_{ref} and the angle θ of the reference vector in the d_1-q_1 plane. Since the SVPWM-C and the CBPWM operate in the non-transformed vector space, the boundary equations are translated to such domain. This yields the expression $v_r{}^a = v_r{}^e + 1$ for the boundary between regions H and J. As a result, the switching vector sequences used by the SVPWM-5A are identical to the ones obtained by the SVPWM-C when the indexes are

$$\{q_m\} = \begin{cases} \{3, 4, \ldots, 8\} & \text{if } v_r{}^a < v_r{}^e + 1 \text{ (regions A–H)} \\ \{2, 3, \ldots, 7\} & \text{otherwise (regions J and K)} \end{cases}$$
(11)

provided the reference vector occupies the first sector. For the remaining nine sectors, similar expressions can be obtained, where only the region identification condition changes.

Considering the relationship between the SVPWM-C and the CBPWM seen in Section II-C, and by combining (10) with (11) and (6), it is concluded that the SVPWM-5A is fully equivalent to the PDPWM with the zero-sequence injection

$$v_z = \begin{cases} n_5 - v_r{}^5 - (\hat{\omega}_f{}^{j_5} + \hat{\omega}_f{}^{j_5+1})/2 & \text{if } j_5 < 4 \\ n_5 - v_r{}^5 - \hat{\omega}_f{}^4/2 & \text{if } j_5 = 4 \\ n_5 - v_r{}^5 + (1 - \hat{\omega}_f{}^1)/2 & \text{if } j_5 = 5 \end{cases}$$
(12)

where

$$n_5 = \begin{cases} \text{integ}\left((7 - q_i)/5\right) & \text{if } v_r{}^a < v_r{}^e + 1 \\ \text{integ}\left((6 - q_i)/5\right) & \text{otherwise} \end{cases}$$
(13a)

$$j_5 = \begin{cases} 8 - q_i - 5n_5 & \text{if } v_r{}^a < v_r{}^e + 1 \\ 7 - q_i - 5n_5 & \text{otherwise.} \end{cases}$$
(13b)

B. CBPWM Equivalent to the SVPWM-5B

The SVPWM-5B [10] is a modification of the SVPWM-5A that uses the switching vector redundancy to reduce the variations of the output CMV. This is achieved by halving every sector (see dash-dotted line in Fig. 3), which increases the number of regions per sector from 10 to 14, and by selecting an appropriate switching vector sequence for each region [10]. Following the same procedure as in Section III-A, the following is inferred. Firstly, the switching vector sequences proposed in [10] for all regions in the lower half sector have q_m indexes equal to $\{3, 4, \ldots, 8\}$, while those of the upper half sector are equal to $\{2, 3, \ldots, 7\}$. Secondly, the condition to evaluate if the region where the vector lies is in the lower half sector can be written as $v_r{}^e > 0$. Therefore, if the indexes

$$\{q_m\} = \begin{cases} \{3, 4, \ldots, 8\} & \text{if } v_r{}^e > 0 \text{ (lower half sector)} \\ \{2, 3, \ldots, 7\} & \text{otherwise (upper half sector)} \end{cases}$$
(14)

are selected within the SVPWM-C algorithm, the obtained switching vector sequences are identical to the ones obtained by the SVPWM-5B, provided the reference vector lies in the first sector. Similar expressions can be obtained for the remaining sectors.
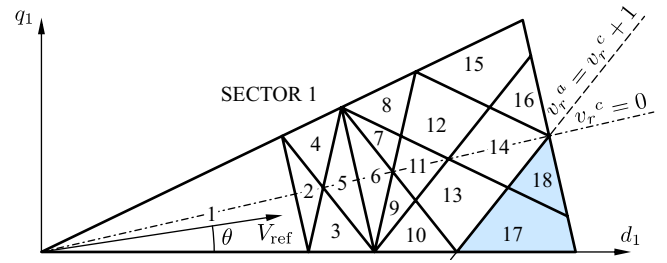

Fig. 4. Division of first sector into regions considered in SVPWM-7A [12].

The comparison of (14) with its counterpart (11) reveals that both expressions have the same form, and consequently, a PDPWM fully equivalent to the SVPWM-5B is obtained with the zero-sequence injection scheme given in (12) with

$$n_5 = \begin{cases} \text{integ}\left((7 - q_i)/5\right) & \text{if } v_r{}^e > 0 \\ \text{integ}\left((6 - q_i)/5\right) & \text{otherwise} \end{cases}$$
(15a)

$$j_5 = \begin{cases} 8 - q_i - 5n_5 & \text{if } v_r{}^e > 0 \\ 7 - q_i - 5n_5 & \text{otherwise.} \end{cases}$$
(15b)

Moreover, the zero sequence obtained by combining (12) with (15) is equal to the one obtained with (1) when $v_o = 1$, which also proves that the SVPWM-7B is fully equivalent to a PDPWM with double min-max zero-sequence injection.

C. CBPWM Equivalent to the SVPWM-7A

The SVPWM-7A [12] is the extension of the SVPWM-5A for seven-phase neutral point clamped VSIs, where the space vectors are decomposed into three planes: d_1-q_1, d_2-q_2 and d_3-q_3. The linear region of the d_1-q_1 plane is divided into 14 sectors, and then each sector into 18 regions, as shown in Fig. 4. The overmodulation region is ignored. The region where the reference vector lies determines the switching vector sequence, which is composed of eight adjacent vectors that produce zero voltage in the d_2-q_2 and d_3-q_3 planes on average during the switching period. Following the same procedure as in Section III-A, it is inferred that this PWM technique is also fully equivalent to the SVPWM-C when

$$\{q_m\} = \begin{cases} \{4, 5, \ldots, 11\} & \text{if } v_r{}^a < v_r{}^c + 1 \text{ (regions 1–16)} \\ \{3, 4, \ldots, 10\} & \text{otherwise (regions 17 and 18)} \end{cases}$$
(16)

provided the reference lies in the first sector. Similar expressions can be obtained for the remaining 13 sectors.

Considering the relationship between the SVPWM-C and CBPWM, and by combining (10) with (16), it is deduced that the SVPWM-7A is fully equivalent to the PDPWM with a zero-sequence injection calculated as

$$v_z = \begin{cases} n_7 - v_r{}^7 - (\hat{\omega}_f{}^{j_7} + \hat{\omega}_f{}^{j_7+1})/2 & \text{if } j_7 < 6 \\ n_7 - v_r{}^7 - \hat{\omega}_f{}^6/2 & \text{if } j_7 = 6 \\ n_7 - v_r{}^7 + (1 - \hat{\omega}_f{}^1)/2 & \text{if } j_7 = 7 \end{cases}$$
(17)

where

$$
n_7 = \begin{cases} \text{integ}\left((10 - q_i)/7\right) & \text{if } v_r{}^a < v_r{}^c + 1 \\ \text{integ}\left((9 - q_i)/7\right) & \text{otherwise} \end{cases} \tag{18a}
$$

$$
j_7 = \begin{cases} 11 - q_i - 7n_7 & \text{if } v_r{}^a < v_r{}^c + 1 \\ 10 - q_i - 7n_7 & \text{otherwise.} \end{cases} \tag{18b}
$$

D. CBPWM Equivalent to the SVPWM-7B

The SVPWM-7B [13] is a modification of the SVPWM-7A in which every sector is halved, analogously to its five-phase counterpart (i.e., SVPWM-5B). The application of the procedure in Section III-A leads to the conclusion that this technique is equivalent to the SVPWM-C when the following sequence of indexes is selected

$$
\{q_m\} = \begin{cases} \{3, 4, \ldots, 10\} & \text{if } v_r{}^c < 0 \text{ (lower half sector)} \\ \{4, 5, \ldots, 11\} & \text{otherwise (upper half sector)} \end{cases} \tag{19}
$$

provided the reference vector lies in the first sector. Similar expressions are obtained for the remaining 23 sectors. Once again, (19) is similar to its counterpart (16); and thus, the PDPWM with the zero sequence given in (17) with

$$
n_7 = \begin{cases} \text{integ}\left((9 - q_i)/7\right) & \text{if } v_r{}^c < 0 \\ \text{integ}\left((10 - q_i)/7\right) & \text{otherwise} \end{cases} \tag{20a}
$$

$$
j_7 = \begin{cases} 10 - q_i - 7n_7 & \text{if } v_r{}^c < 0 \\ 11 - q_i - 7n_7 & \text{otherwise} \end{cases} \tag{20b}
$$

is fully equivalent to the SVPWM-7B. Furthermore, the combination of (17) with (20) leads to (1) when $v_o = 1$. This also proves that the SVPWM-7B is equivalent to a PDPWM with double min-max zero-sequence injection.

E. Generalization to Other d-q SVPWM Techniques

Even though no general multilevel multiphase d-q SVPWM technique is available so far, the procedure developed in this section to obtain an equivalent PDPWM can be applied to other cases, provided the switching vector sequences used by the modulation technique are made of adjacent vectors sorted in ascending order of their magnitude. These are conditions usually fulfilled by the PWM techniques because the typical requirement of switching loss minimization leads to the consideration of this kind of switching vector sequences. In this case, the appropriate zero-sequence injection scheme can be calculated in general by means of (10), which is valid for any number of levels and phases. Its particularization for five ($P = 5$) and seven phases ($P = 7$) leads to (12) and (17), respectively. Note that, in all these expressions, the parameters n_P and j_P depend on $\{q_m\}$ [cf. (6)], which itself depends on the particular switching vector sequence assigned to each d-q region in the d-q SVPWM technique. No general expression can be provided to calculate n_P and j_P because there is no general methodology to perform the aforementioned assignation, since it is usually made to fulfill an arbitrary modulation complementary task by taking advantage of the switching redundancy in the VSI.

TABLE II
LIST OF SIMULATION AND EXPERIMENTAL TESTS

Test	SVPWM	Zero-sequence injection scheme
#1	SVPWM-B	Eq. (3)
#2	SVPWM-R	Eq. (7)
#3	SVPWM-5A	Eqs. (12) & (13)
#4	SVPWM-5B	Eqs. (12) & (15)
#5	SVPWM-7A	Eqs. (17) & (18)
#6	SVPWM-7B	Eqs. (17) & (20)

The algorithm in SVPWM-6 [11] meets the aforementioned conditions; thus, the proposed procedure can be applied to this technique as well. In this case, the result obtained is $v_z = 0$ (i.e., no zero-sequence injection scheme is required) for every d-q region, which leads to the conclusion that the SVPWM-6 produces identical results to a plain three-level six-phase PDPWM. This finding is in agreement with the experimental results obtained in [11].

Finally, the exact equivalence between SVPWM and CBPWM has the added value of permitting to apply the vast knowledge on the latter to the former. For the sake of example, the methodology presented in [18] can now be applied to the assessment of the switching harmonics produced by the multilevel multiphase SVPWM techniques. Additionally, it eases the comparison of SVPWM techniques among them, which now can be done by comparing the zero-sequence injection schemes corresponding to each one of them.

IV. SIMULATION AND EXPERIMENTAL RESULTS

The multilevel multiphase SVPWM techniques are compared by simulation and by experimental tests with the proposed CBPWM counterparts to verify the claimed equivalences. The arrows depicted in Fig. 2 may be used as a guide along this section. The six tests listed in Table II have been conducted to verify the proposed zero-sequence injection schemes that achieve PDPWM techniques equivalent to the multidimensional SVPWM and the d-q SVPWM techniques under study. For the multidimensional SVPWM tests, a five-level five-phase inverter is considered, which enters the overmodulation area for $m > 2.0$ p.u. in the case of the SVPWM-B (test #1) and for $m > 2.102$ p.u. in the case of the SVPWM-R (test #2).

A. Simulation Results

The simulations have been carried out in Matlab, taking into account the following considerations. A small ratio of the switching frequency to the fundamental frequency $m_f = 20$ is used to facilitate the comparison of the output voltage waveforms. Only half the fundamental cycle is plotted because of the half-wave symmetry obtained with integer m_f. Only phase a is shown since it is representative of the other phases.

1) Multidimensional SVPWM: A balanced five-phase sinusoidal reference with normalized amplitudes of $m = 1.6$ p.u., within the linear range, and $m = 2.3$, in the overmodulation range, is considered in the set of simulations shown in tests #1 and #2. The normalized output voltages obtained by the SVPWM-B and the PDPWM with the null zero-sequence
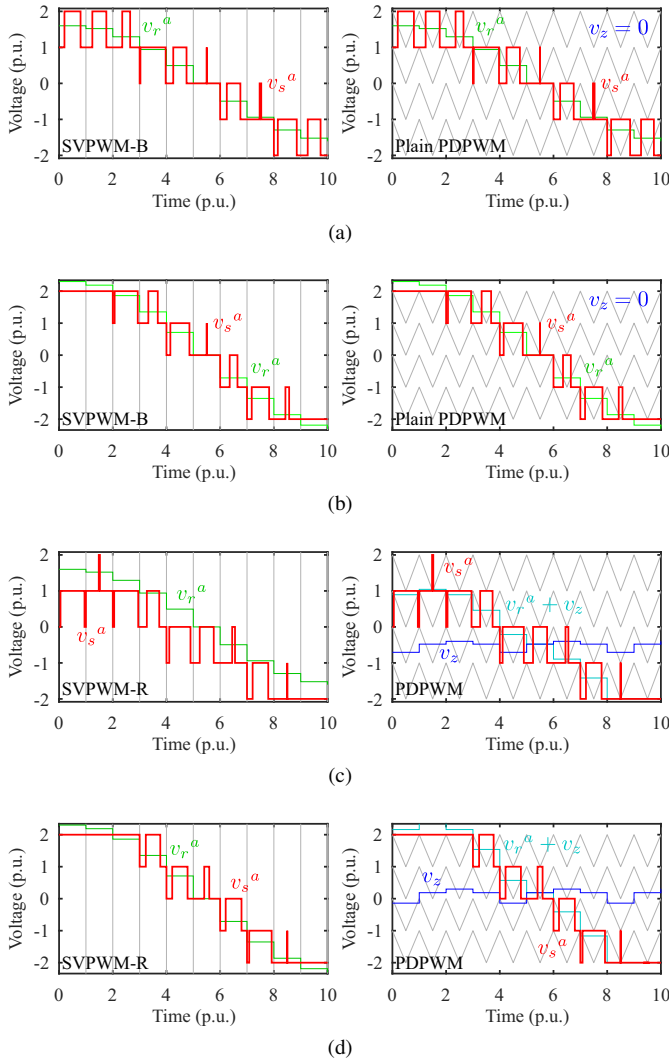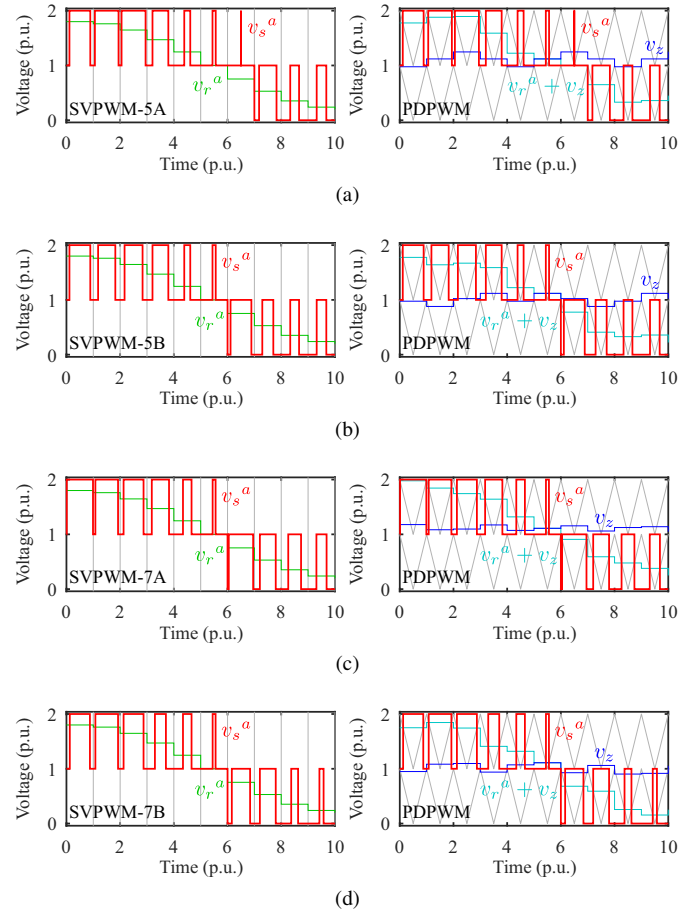
Fig. 5. Simulation comparison of the multidimensional SVPWM techniques with the PDPWM with the proposed zero-sequence injection schemes. (a) Test #1: SVPWM-B with $m = 1.6$ (linear region). (b) Test #1: SVPWM-B with $m = 2.3$ (overmodulation). (c) Test #2: SVPWM-R with $m = 1.6$ (linear region). (d) Test #2: SVPWM-R with $m = 2.3$ (overmodulation).

Fig. 6. Simulation comparison of the multilevel d-q SVPWM techniques with the PDPWM with the proposed zero-sequence injection schemes. (a) Test #3: SVPWM-5A. (b) Test #4: SVPWM-5B. (c) Test #5: SVPWM-7A. (d) Test #6: SVPWM-7B.

injection in (3) are plotted in Figs. 5(a) and 5(b). Figs. 5(c) and 5(d) compare the output obtained by means of the SVPWM-R with the output obtained by means of the PDPWM with the zero-sequence injection computed with (7). No differences between the SVPWM and the CBPWM techniques are noticeable, which validates the equivalence and the proposed zero-sequence injection schemes, nor in the linear nor in the overmodulation range.

2) d-q SVPWM: A balanced sinusoidal reference with a normalized amplitude of $m = 0.8$ p.u., within the linear range, is considered in the tests #3 to #6. The comparison in the overmodulation region is not feasible because all the d-q SVPWM techniques under study are undefined in such region. Fig. 6(a) plots the normalized outputs obtained in test #3 and shows that the output obtained by using the SVPWM-5A is identical to the one obtained by using the PDPWM with the zero-sequence injection calculated with (12) and (13). The same occurs in tests #4, #5 and #6 [cf. Figs. 6(b)

to 6(d)], in which the outputs produced by the d-q SVPWM techniques are identical to the ones produced by the PDPWM with the zero-sequence injection calculated with the equations indicated in Table II.

In order to quantify the differences between the PWM techniques under comparison, the variable δ is defined as the rms value of the differences between the normalized output voltages of every phase. Fig. 7 plots the figure δ against the normalized amplitude m of the sinusoidal voltage reference and against the frequency modulation index m_f. Results in the overmodulation region are highlighted for multidimensional SVPWM (i.e., tests #1 and #2). The d-q SVPWM techniques are simulated just in the linear range (i.e., $m \leq 1.051$ p.u. in tests #3 and #4, and $m \leq 1.026$ p.u. in tests #5 and #6). The frequency modulation index range includes integer and non integer values. In all cases, δ is less than 1.5×10^{-7} p.u., which leads to the conclusion that there are no practical differences between the compared techniques, even though such difference is non-zero, as it could have been expected, due to the usual rounding errors in numerical simulations. Extensive simulations for other phase numbers (not plotted) have been carried out rendering identical conclusions.
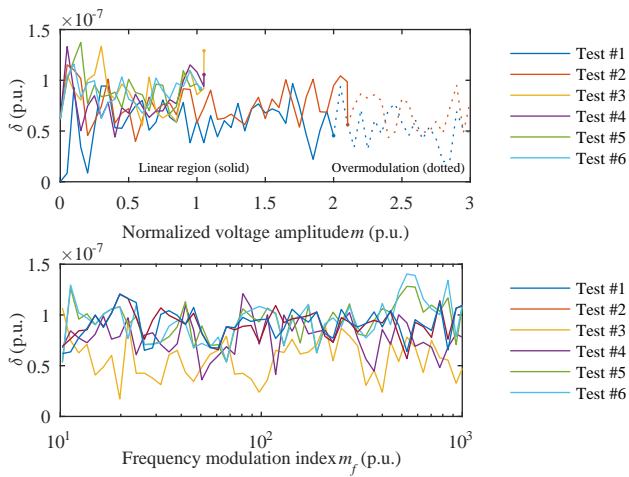
Fig. 7. Value of the rms difference between the output of the SVPWM and the equivalent PDPWM algorithms.
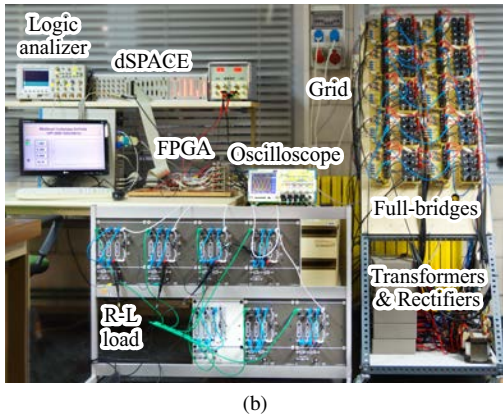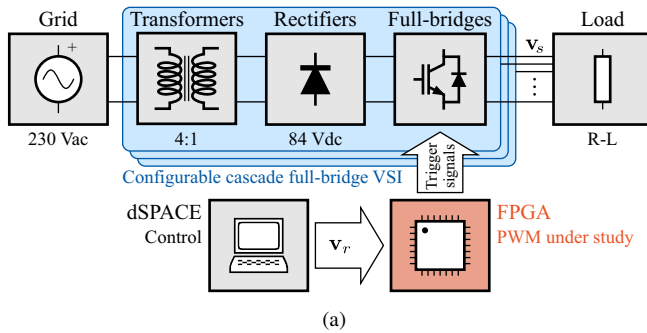

(a)

(b)

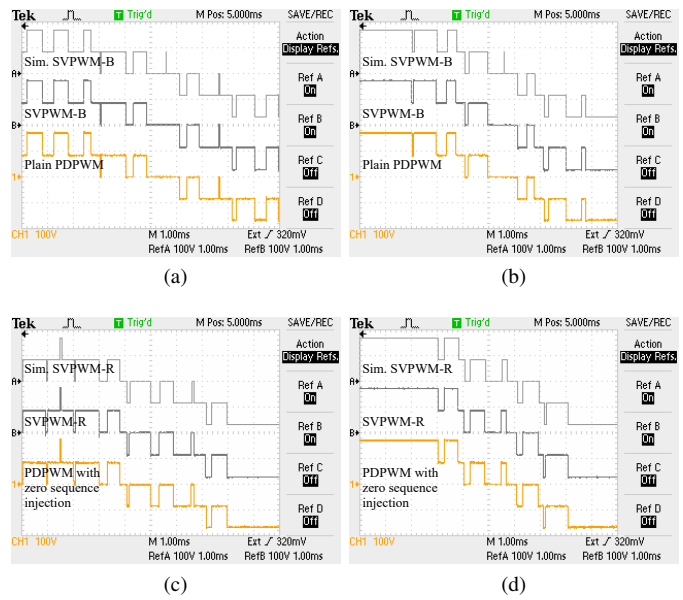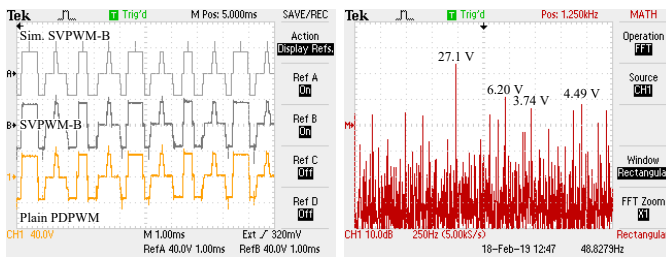Fig. 8. Experimental setup. (a) Block diagram. (b) Picture.

Fig. 9. Experimental comparison of the multidimensional SVPWM techniques with the PDPWM with the proposed zero-sequence injection schemes. `RefA`: simulated output voltage waveform. `RefB` and `CH1`: experimental output voltage waveforms. (a) Test #1: SVPWM-B ($m = 1.6$). (b) Test #1: SVPWM-B ($m = 2.3$). (c) Test #2: SVPWM-R ($m = 1.6$). (d) Test #2: SVPWM-R ($m = 2.3$).

B. Experimental Results

The CBPWM techniques and their equivalence with the SVPWM techniques are also verified in the laboratory with the experimental setup depicted in Fig. 8. The PWM techniques under study are implemented in a Spartan-3 XC3S200 FPGA from Xilinx, which generates the VSI trigger signals. The reference voltage signals to the FPGA are provided by a dSPACE DS1103 PPC Controller Board. A cascaded full-bridge topology has been used in the experiments because of its modular nature [27], which can be configured to make the VSIs with the different number of levels and phases required in the experiments. Two full-bridges are connected in series to configure each phase of the five-level inverter, and just one full-bridge is required for every phase of the three-level inverters. Each full-bridge module is composed of four IRGB6B60KD transistors fed from the utility grid with a 4:1 single-phase transformer and a full-bridge diode rectifier, which gives $V_{dc} = 84$ V. The switching frequency is 977 Hz. This particular value (close to 1 kHz) results from using 10-bit up-down counters connected to a 1-MHz clock in the FPGA to implement the carrier generators. No dead-time compensation scheme is used to alleviate the effects of the 4-μs dead time introduced by the transistor drivers. A balanced star-connected load with $R = 810\,\Omega$ in series with $L = 1.2$ H is considered.

All the simulation tests have been reproduced in the laboratory. Measurements of VSI output voltages and the instantaneous zero-sequence component have been made with a Tektronix TPS2014 digital oscilloscope. To facilitate the analysis of the experimental data, the simulation waveform corresponding to each test (cf. Figs. 5 and 6) was transferred to the reference memory waveform `RefA` of the oscilloscope by means of a comma-separated values file. Since the two PWM techniques under comparison cannot be run in parallel, the output waveform measured using the first one is stored in oscilloscope memory `RefB`, while the measurement made using the second one is displayed in channel `CH1`. Synchronization of all captures is achieved by using an external trigger signal generated by the dSPACE board.

Measurements of the output voltage of phase a and the zero-sequence component of the output voltage obtained in tests #1 and #2, which compare the multidimensional SVPWM techniques with their equivalent CBPWM counterparts, are shown in Figs. 9 and 10, respectively. Results obtained in tests #3 to #6, which compare each d-q SVPWM with its equivalent PDPWM
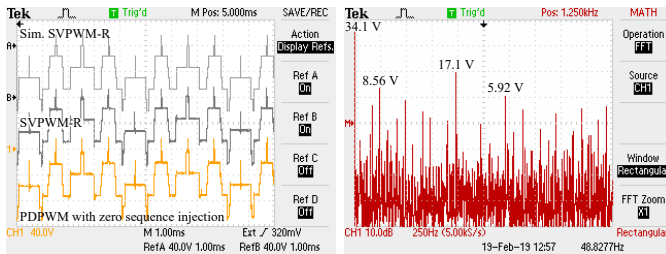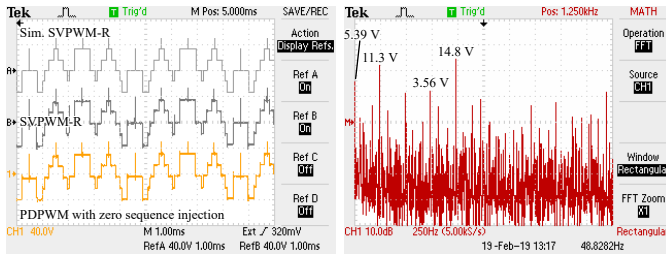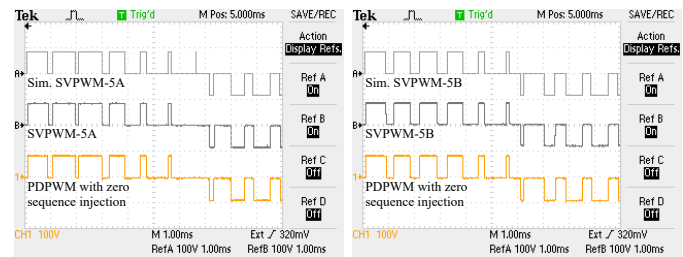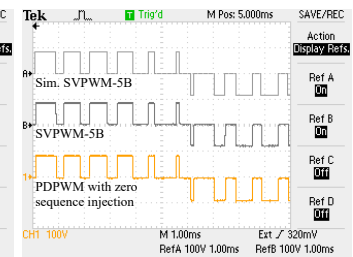
(a)
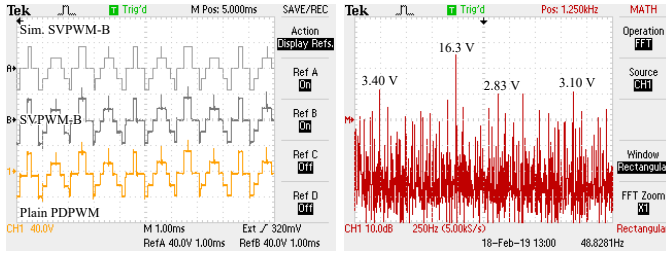
(b)

(c)

(d)

Fig. 10. Experimental comparison of the multidimensional SVPWM techniques with the PDPWM with the proposed zero-sequence injection schemes. `RefA`: simulated instantaneous zero-sequence waveform. `RefB` and `CH1`: experimental instantaneous zero-sequence waveforms. (a) Test #1: SVPWM-B with $m = 1.6$ (linear region). (b) Test #1: SVPWM-B with $m = 2.3$ (overmodulation). (c) Test #2: SVPWM-R with $m = 1.6$ (linear region). (d) Test #2: SVPWM-R with $m = 2.3$ (overmodulation).

(a)

(b)

(c)

(d)

Fig. 11. Experimental comparison of the multilevel d-q SVPWM techniques with the PDPWM with the proposed zero-sequence injection schemes. `RefA`: simulated output waveform. `RefB` and `CH1`: experimental output waveforms. (a) Test #3: SVPWM-5A. (b) Test #4: SVPWM-5B. (c) Test #5: SVPWM-7A. (d) Test #6: SVPWM-7B.
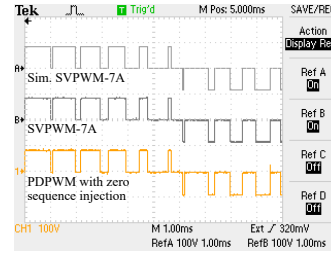
with proposed zero-sequence injection schemes are shown in Figs. 11 and 12. All the measurements in all the tests show similar results for the simulations (`RefA`) and the experimental waveforms (`RefB` & `CH1`), except for some short pulses that are lost because of dead times. More importantly, in all cases the differences between the two experimental measurements (i.e., `RefB` versus `CH1`) are negligible, which validates the equivalence between the multilevel multiphase SVPWM and the CBPWM techniques contributed in Fig. 2. For the case of multidimensional SVPWM techniques, the equivalence holds even in the overmodulation region. Oscilloscope captures
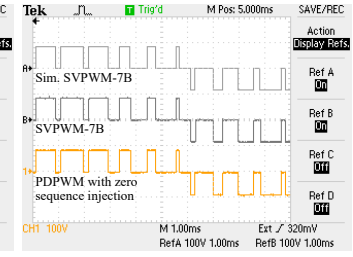
of the fast Fourier transforms (FFTs) of the instantaneous zero-sequence voltages obtained with the proposed CBPWM techniques are also included in Figs. 10 and 12. The FFTs obtained with the original SVPWM techniques are not shown because they are very similar, as it is expected, since the time-domain waveform counterparts have no significant differences. The minor differences in the time-domain waveforms and the FFTs are all attributed to measurement error.

Comparisons up to this point permit to validate the proposed equivalent CBPWM techniques from the load point of view. To validate the equivalence from the converter point of view, the transistor trigger signals are compared in Figs. 13 and 14. In the SVPWM techniques, these trigger signals are calculated from the switching vectors by means of some trigger logic, which depends on the converter topology and the desired modulation complementary tasks. The same trigger logic is used to calculate the trigger signals from the results of the arithmetic comparison between voltage reference and carriers in the equivalent CBPWM counterparts. No differences are noticed in Figs. 13 and 14 between the trigger signals obtained with the original SVPWM algorithm and those of the equivalent CBPWM. This reveals that the converter sees no difference between them, and consequently, all converter issues like switching losses, capacitor balancing, etc. do not change with the equivalent CBPWM techniques.

The only difference between the PWM techniques under comparison resides in the computational complexity. A simple inspection of the modulation techniques under consideration reveals that all the SVPWM algorithms are much more involved than their equivalent CBPWM counterparts. This is validated with the hardware resource comparison performed in Fig. 15, which shows that all the CBPWM algorithms use fewer slices than the SVPWM counterparts. The same
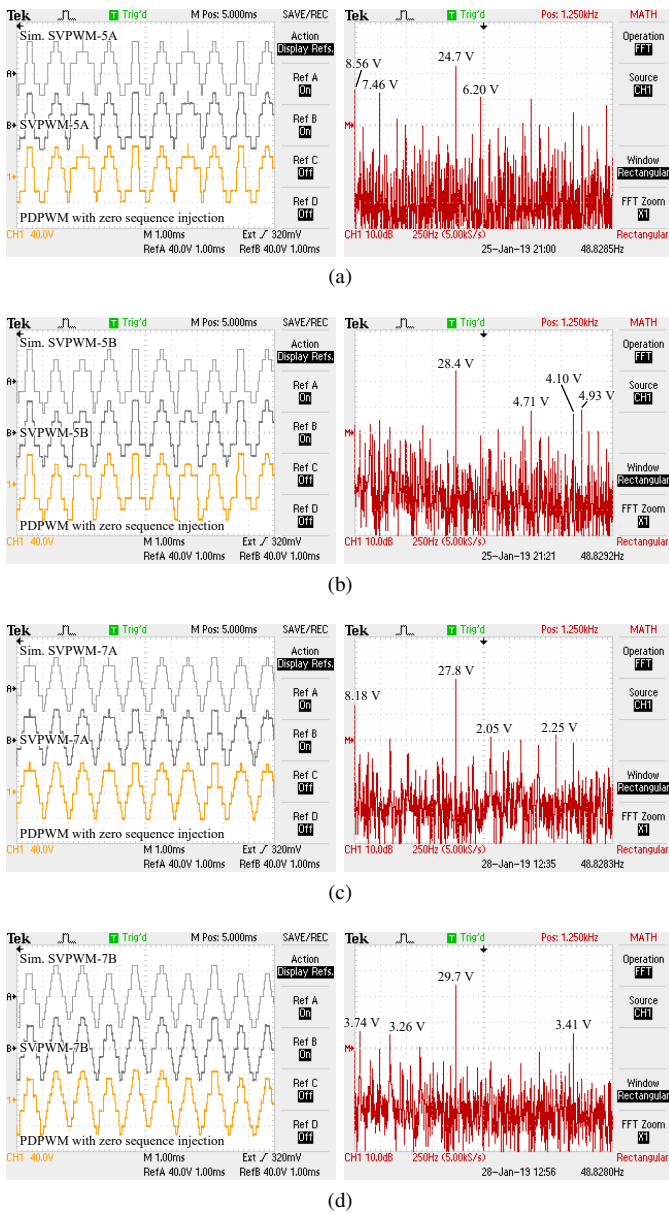
(a)

(b)

(c)

(d)

Fig. 12. Experimental comparison of the multilevel d-q SVPWM techniques with the PDPWM with the proposed zero-sequence injection schemes. `RefA`: simulated output waveform. `RefB` and `CH1`: experimental output waveforms. (a) Test #3: SVPWM-5A. (b) Test #4: SVPWM-5B. (c) Test #5: SVPWM-7A. (d) Test #6: SVPWM-7B.

(a)

(b)

(c)

(d)

Fig. 13. Trigger signal (phase a) comparison of the multidimensional SVPWM techniques with the PDPWM with the proposed zero-sequence injection schemes. T_{Rn}^a and $\bar{T}_{Ln}^a$ are the triggers of the upper-right and the lower-left transistors of the nth cascaded full-bridge of phase a, respectively. (a) Test #1: SVPWM-B ($m = 1.6$). (b) Test #1: SVPWM-B ($m = 2.3$). (c) Test #2: SVPWM-R ($m = 1.6$). (d) Test #2: SVPWM-R ($m = 2.3$).

(a)

(b)

(c)

(d)

Fig. 14. Trigger signal (phases a & b) comparison of the multilevel d-q SVPWM techniques with the PDPWM with the proposed zero-sequence injection schemes. T_{R1}^k and $\bar{T}_{L1}^k$ are the triggers of the upper-right and the lower-left transistors of the full-bridge of phase k, respectively. () Test #3: SVPWM-5A. () Test #4: SVPWM-5B. () Test #5: SVPWM-7A. () Test #6: SVPWM-7B.

occurs to the CBPWM processing time, which is lower as well. Despite the fact that all SVPWM algorithms easily fit in state-of-art FPGAs, the equivalent CBPWM counterparts are best suited for real-world applications because they are easier to implement and make a more efficient use of computing hardware.

V. CONCLUSION

In this paper, CBPWM techniques equivalent to the multilevel multiphase SVPWM techniques are proposed. Each of them consist of a PDPWM with a certain zero-sequence injection scheme. Closed-form mathematical expressions for the calculation of such zero-sequences are derived throughout the paper, which are valid for the same number of levels
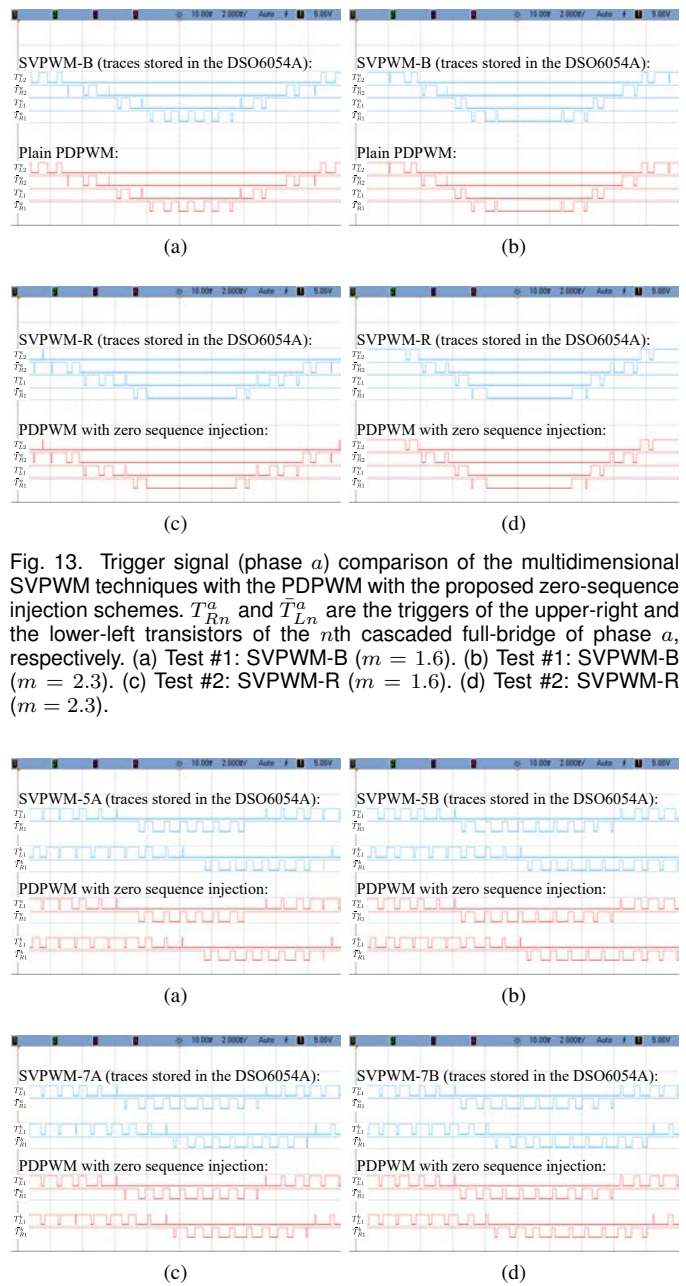
and phases of the original SVPWM, i.e, for any number of levels and phases in the case of the multidimensional SVPWM techniques and for particular level and phase numbers in the cases of the d-q SVPWM techniques. Nevertheless, the methodology followed in the paper can be generalized to other d-q SVPWM techniques with other number of levels or phases, provided they meet certain conditions.

It is shown that the equivalent CBPWM techniques produce identical results from both the converter and the load points of view, but with significant reduction of the computation complexity. The proposed equivalent CBPWM techniques are
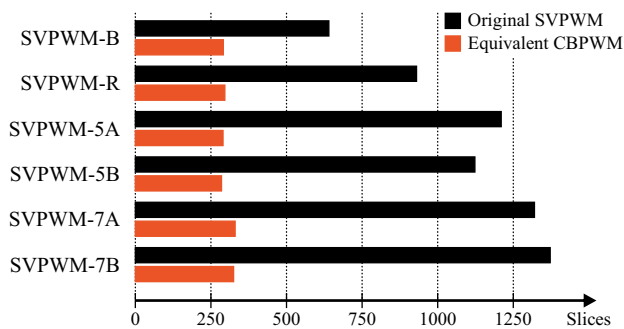
Fig. 15. Comparison of hardware resources used by the tested algorithms.

validated through extensive simulations and experimental tests. The equivalent CBPWM techniques use notably fewer hardware resources than the original SVPWM counterparts, which makes them the preferred choice in practical applications.

REFERENCES

[1] F. Bu, T. Pu, L. Zhu, and W. Huang, "Performance and evaluation of five-phase dual random SVPWM strategy with optimized probability density function," *IEEE Trans. Ind. Electron.*, vol. 66, no. 5, pp. 3323–3332, May. 2019.

[2] H. Lu, J. Li, R. Qu, D. Ye, and Y. Lu, "Fault-tolerant predictive control of six-phase PMSM drives based on pulse-width-modulation," *IEEE Trans. Ind. Electron.*, vol. 66, no. 7, pp. 4992–5003, Jul. 2019.

[3] A. S. Abdel-Khalik, A. M. Massoud, and S. Ahmed, "Application of standard three-phase stator frames in prime phase order multiphase machine construction," *IEEE Trans. Ind. Electron.*, vol. 66, no. 4, pp. 2506–2517, Apr. 2019.

[4] E. Levi, R. Bojoi, F. Profumo, H. A. Toliyat, and S. Williamson, "Multiphase induction motor drives—A technology status review," *IET Elec. Power Appl.*, vol. 1, pp. 489–516, Jul. 2007.

[5] E. Levi, N. Bodo, O. Dordevic, and M. Jones, "Recent advances in power electronic converter control for multiphase drive systems," in *Proc. IEEE Workshop Elec. Mach. Des., Control and Diagnosis WEMDCD*, pp. 158–167, Paris, France, 11–12 Mar. 2013.

[6] E. Levi, "Advances in converter control and innovative exploitation of additional degrees of freedom for multiphase machines," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 433–448, Jan. 2016.

[7] F. Barrero and M. J. Duran, "Recent advances in the design, modeling, and control of multiphase machines —Part I," *IEEE Trans. Ind. Electron.*, vol. 63, no. 1, pp. 449–458, Jan. 2016.

[8] H. Abu-Rub, S. Bayhan, S. Moinoddin, M. Malinowski, and J. Guzinski, "Medium-voltage drives: Challenges and existing technology," *IEEE Power Electronics Magazine*, vol. 3, no. 2, pp. 29–41, Jun. 2016.

[9] L. Gao and J. E. Fletcher, "A space vector switching strategy for three-level five-phase inverter drives," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2332–2343, Jul. 2010.

[10] O. Dordevic, M. Jones, and E. Levi, "A comparison of PWM techniques for three-level five-phase voltage source inverters," in *Proc. Eur. Conf. on Power Electron. and Appl. EPE*, Birmingham, UK, 2011.

[11] E. A. R. E. Ariff, O. Dordevic, and M. Jones, "A space vector PWM technique for a three-level symmetrical six-phase drive," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 8396–8405, Nov. 2017.

[12] O. Dordevic, M. Jones, and E. Levi, "A space vector PWM algorithm for a three-level seven-phase voltage source inverter," in *Proc. Eur. Conf. on Power Electron. and Appl. EPE*, Birmingham, UK, 2011.

[13] O. Dordevic, E. Levi, and M. Jones, "A vector space decomposition based space vector PWM algorithm for a three-level seven-phase voltage source inverter," *IEEE Trans. Power Electron.*, vol. 28, no. 2, pp. 637–649, Feb. 2013.

[14] O. López, J. Álvarez, J. Doval-Gandoy, and F. D. Freijedo, "Multilevel multiphase space vector PWM algorithm," *IEEE Trans. Ind. Electron.*, vol. 55, no. 5, pp. 1933–1942, May. 2008.

[15] O. López, J. Álvarez, J. Doval-Gandoy, and F. D. Freijedo, "Multilevel multiphase space vector PWM algorithm with switching state redundancy," *IEEE Trans. Ind. Electron.*, vol. 56, no. 3, pp. 792–804, Mar. 2009.

[16] H.-M. Ryu, J.-H. Kim, and S.-K. Sul, "Analysis of multiphase space vector pulse-width modulation based on multiple *d-q* spaces concept," *IEEE Trans. Power Electron.*, vol. 20, no. 6, pp. 1364–1371, Nov. 2005.

[17] O. López, E. Levi, F. D. Freijedo, and J. Doval-Gandoy, "Number of switching state vectors and space vectors in multilevel multiphase converters," *IET Electron. Lett.*, vol. 45, no. 10, pp. 524–525, May. 2009.

[18] D. G. Holmes and T. A. Lipo, *Pulse width modulation for power converters: principles and practice.* Wiley-IEEE press, 2003.

[19] G. Carrasco and C. A. Silva, "Space vector PWM method for five-phase two-level VSI with minimum harmonic injection in the overmodulation region," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 2042–2053, May. 2013.

[20] W. Yao, H. Hu, and Z. Lu, "Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 45–51, Jan. 2008.

[21] J. Chen, Y. He, S. U. Hasan, and J. Liu, "A comprehensive study on equivalent modulation waveforms of the SVM sequence for three-level inverters," *IEEE Trans. Power Electron.*, vol. 30, no. 12, pp. 7149–7158, Dec. 2015.

[22] A. Iqbal and S. Moinuddin, "Comprehensive relationship between carrier-based PWM and space vector PWM in a five-phase VSI," *IEEE Trans. Power Electron.*, vol. 24, no. 10, pp. 2379–2390, Oct. 2009.

[23] B. McGrath, D. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[24] O. Dordevic, M. Jones, and E. Levi, "A comparison of carrier-based and space vector PWM techniques for three-level five-phase voltage source inverters," *IEEE Trans. Ind. Informat.*, vol. 9, no. 2, pp. 609–619, May. 2013.

[25] J. Prieto, M. Jones, F. Barrero, E. Levi, and S. Toral, "Comparative analysis of discontinuous and continuous PWM techniques in VSI-fed five-phase induction motor," *IEEE Trans. Ind. Electron.*, vol. 58, no. 12, pp. 5324–5335, Dec. 2011.

[26] O. López, D. Dujic, M. Jones, F. D. Freijedo, J. Doval-Gandoy, and E. Levi, "Multidimensional two-level multiphase space vector PWM algorithm and its comparison with multifrequency space vector PWM method," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 465–475, Feb. 2011.

[27] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodríguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

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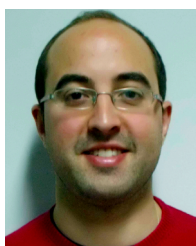
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