Distance measurement as a practical example of FPGA design

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***Abstract*— Digital design learning at the RT level requires practical examples and as learning progresses, the examples need to become more complex. FPGAs and development boards offer a very suitable platform for the implementation of these designs. However, classroom practice sessions usually last two hours, which does not allow the complexity of the designs be high enough. For this reason, interesting designs that can be made in several sessions are required In this paper, the construction of a distance measuring system is presented as a demonstrator. For this purpose, a distance measurement module based on ultrasound is available and the results are displayed in 7-segment displays on a Nexys4 board.**

Keywords— VHDL, digital system design, distance measuring module, FPGA.

I. INTRODUCTION

Digital design subjects in advanced electronic degree courses can use hardware description languages for the description of circuits. Besides, FPGA devices are used as a platform to experimentally test the behaviour of designed circuits. This methodology has many advantages. One of them is the use of a single CAD environment for the design, verification and programming of devices. In addition, this software is offered free of charge for educational use by FPGA manufacturers. Another advantage is the availability of development boards, which include the FPGA, displays and interface elements that allow to enter values to the inputs and see results on the outputs. For all these reasons, teaching digital design with the VHDL-FPGA tandem is an alternative at an acceptable cost and, above all, very practical and highly attractive for students.

This alternative is being applied in the course "Advanced Digital Design"[1], an elective in the fourth year of the Degree in Industrial Electronics at the Polytechnic School of the University of Seville. The aim of this course is for students to learn the most important concepts of digital design. The only prerequisites for this subject are the subjects "Industrial Electronics" and "Digital Electronics", both in the second year.

The subject "Industrial Electronics" is a subject of the common training block of the industrial branch, taught in the first term of the second year. It is the first subject that students have in this degree related to electronics. The contents of this subject [2] basically consist of an analogue and a digital block. In the digital block, the basic concepts of digital electronics are introduced, from switching algebra to the design of state machines, through the concepts of logic gates and bistables.

The subject "Digital Electronics" is a compulsory subject in the degree curriculum. It is taught in the second term of the second year. Its contents [3] develop those initiated in Industrial Electronics. They include the real features of logic gates and bistables, analysis and design of digital circuits (both combinational and sequential) and combinational and sequential subsystems. The latest topics in the course introduce concepts related to design at RT level (circuit structure based on control unit and data unit), ASM charts and basic microprocessor principles.

With this previous knowledge on the part of the students, in the course "Advanced Digital Design" they are taught the description of digital circuits using the VHDL hardware description language and the way to implement them on FPGA devices (in our case Xilinx). The subject is approached in a very practical way, so that the students design small circuits in the laboratory sessions. As the subject progresses, these laboratories increase in complexity, but in the time allotted to the laboratories (a maximum of two hours) there is no time to carry out designs that have a minimum complexity.

One solution to this problem is the realization of a design in several sessions. But for this solution to be interesting it must have several characteristics: on the one hand, each part must be self-contained (it must have a design objective that can be achieved in a laboratory session) and, on the other hand, it must involve a gradual construction of the functionality to be achieved.

In this communication we present as a demonstrator a set of four laboratory sessions to build a distance meter using an ultrasonic distance measuring device as a basis and the 7-segment displays as an element to show the result.

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The structure of this communication is as follows: the second section briefly explains the design to be carried out. Section III details the contents and objectives of each of the sessions into which the design has been divided, as well as the results to be obtained. Finally, some conclusions are drawn.

II. DESIGN TO BE DEVELOPED

The aim of the proposed set of laboratory sessions is to design a distance meter based on a commercial device. It is the HC-SR04[4] *("Fig. 1"*) which, by means of ultrasound, is capable of measuring distances within a given range and displaying these measurements in 7-segment displays.

The system must incorporate two operating modes: continuous mode and unitary mode. In continuous mode, the system will permanently activate the distance meter and display the measurements continuously. However, in unitary mode, the system will perform a single task each time the corresponding command is given.

The realization of the complete system involves the development of several additional elements such as code converters and a control unit that will be part of what will be the main module of the system.

In the block diagram of the measuring system, see *"Fig. 2"*, the connection between the HC-SR04 module, the main module and the 7-segment displays is shown. With respect to the external inputs of the system, in addition to the *reset* and *ck* signals, the *mode* signal is displayed, which allows the user to choose between the two operating modes (unitary and continuous) and the *mide* signal which activates the measurement operation in the unitary mode. As for the outputs, *data_valid* informs that the data shown on the displays already contains the measured distance and *alarm* is a signal that is activated when the distance to the obstacle is within a predefined range.

The HS-SR04 module interacts with the main module via two signals, one input to the distance meter (*trigger*) and one output (*echo*). After receiving a pulse at the *trigger* input, the distance meter emits an ultrasound signal and waits for the signal to be returned after hitting the obstacle. During this waiting time the distance meter generates a positive pulse in the *echo* output which will be proportional to the distance to be measured (*"Fig. 3"*). This distance is contained in a range between 2cm and 4m.

The main module is composed of a control unit, *maxsonar_control*, and a binary to 7-segments code converter. The control unit is in charge of supplying the *trigger* signal to the distance meter and evaluating the output *echo* to obtain the distance to the binary object as well as activating the *alarm* signal. The code converter receives the result of the distance and supplies it to the displays.

The complete system is designed by the students in four sessions. First, the unit *control_maxsonar* is designed and simulated (Lab1). Subsequently, in Lab2, the HC_SR04 meter is emulated by VHDL code. This makes it possible to have randomly timed *echo* signals and to simulate distance measurements. In Lab3, the entire system is brought to the board. To do this, the main module is finished by adding the converter and removing the emulator of the distance meter, since the main module can now interact with the real meter. Finally, in Lab4 the main module is completed with the *alarm* output that will be connected to a buzzer.

III. DEVELOPMENT OF LABORATORY SESSIONS

We will now go on to detail each of the sessions into which the design has been broken down.

A. Session 1 (Lab1)

In Lab1 the control unit, *control_maxsonar*, is created. It has the following inputs and outputs.

Regarding the inputs: a clock signal *ck* of 100Mhz coming from the development board, an asynchronous reset signal (*reset*), a distance measurement start signal (*start*) and the *echo* signal coming from the measuring module. As for the outputs: a *trigger* signal that activates each measurement and will be connected to the measuring module, an output bus that shows the value of the measured distance (*distance*) and a signal that indicates the validity of this measurement (*data_valid*) (see the "*control_maxsonar* block in *"Fig. 4"*).

The tasks to be performed by this module are as follows:

- Generate a pulse at the *trigger* output each time the *start* signal is activated. Since *trigger* will be connected to the measuring module, it must be ensured that it complies with the specifications of this module (it must be greater than 10μs) (*"Fig. 3"*).
- Measure the time the signal *echo* is 1. For this purpose, a frequency signal suitable for the accuracy of the measurement will be used, which in our case is 1cm. To this end, a Xilinx IP block is incorporated into the

Fig. 1 Distance meter HC-SR04

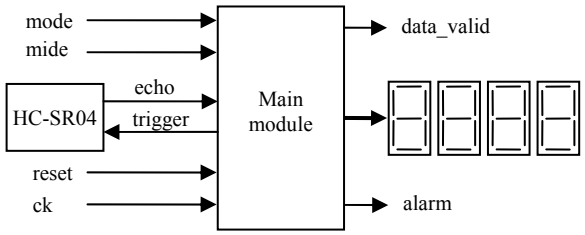

Fig. 2 Block diagram of the measuring system

design to divide the input frequency that is excessive. With the divided clock the number of cycles that the signal is 1 will be counted, being this the measure of the distance in centimeters.

- Activate the *data_valid* signal when the distance measurement process is completed.

The student must determine the number of bits required for the *distance* output according to the upper limit (4m).

The design must be carried out using a state machine complying with the synthesis restrictions. They also have to create a testbench to simulate the functionality of the designed module.

B. Session 2 (Lab2)

In Lab2 a functional model of the distance meter is designed. This will allow us to test the proper operation of the meter-*control_maxsonar* set by simulation before moving on to the test with the real meter and the board.

Once the simulation is successfully completed, the students can use the Nexys4 [5] development board along with the real distance meter to perform the experimental tests. For the connection between both of them it is established that the *trigger* output and the *echo* input of the control are connected to specific pins of the board. The *ck* signal must be connected to the 100 MHz clock of the board, the *reset* signal and the *start* signal to pushbuttons, the *distance* output to a set of leds and, finally, the *data_valid* signal also to another led.

To test the set, the student must activate the *reset* and then activate the *start* using the pushbuttons, wait for the led associated with *data_valid* to switch on and interpret in binary the value of the distance shown on the leds.

C. Session 3 (Lab3)

In Lab3 a block called *maxsonar_system* is designed. This contains the previously developed *maxsonar_control*, a binary to 7-segments converter for the output *distance* and an additional circuit that is simply a multiplexer (mux) to control the *start* signal depending on the *mode* and *mide* inputs.

For the converter we wanted to reuse a design that the student developed in a previous work consisting on a BCD/7-segment converter with 4-digits. Therefore, a new binary/BCD converter must be added to this module.

The block diagram of the *maxsonar_system* is shown in *"Fig. 4"*.

To test the operation of the system on the development board, the same pins used in Lab2 will be used for *echo* and *trigger* while the input *mide* and *mode* will be connected to a pushbutton and a switch respectively.

D. Session 4 (Lab4)

In Lab 4 the design is completed by adding the *alarm* output. The purpose of this output is to generate a sound signal that indicates the proximity to an object. To do this, there is a buzzer to which the *alarm* output is connected. The operating mode is as follows: for the buzzer to be off, the *alarm* output must be set to 1 and to be on, it must be set to 0.

Four cases will be considered depending on the distance to the object:

- If the distance to the object is between 100cm and 75cm, short but distant beeps will occur.
- If the distance value is between 75cm and 50cm the beeps will be slightly longer and less distant.
- If the distance to the object is between 50cm and 25cm, the beeps will be even less distant.
- Finally, if the distance is less than 10cm, the beep must be continuous.

To achieve these objectives, the student must modify the previous code, program the board and then check the operation of the entire system.

The *"Fig. 5, 6 and 7"* show images obtained in the laboratory. *"Fig. 5"* shows the modules that are connected to the development board: the HC_SR04 distance meter and the buzzer used to generate the sound signal. The other two images (*"Fig. 6"* and *"Fig. 7"*) correspond to photographs taken in the laboratory to illustrate the result achieved by the students after finishing the last sessions. Specifically, "Fig. 6" is the result of Lab3, where the distance to the object is shown in the four 7-segment displays and "Fig. 7" corresponds to the result obtained after the completion of Lab4 since the buzzer module is incorporated.

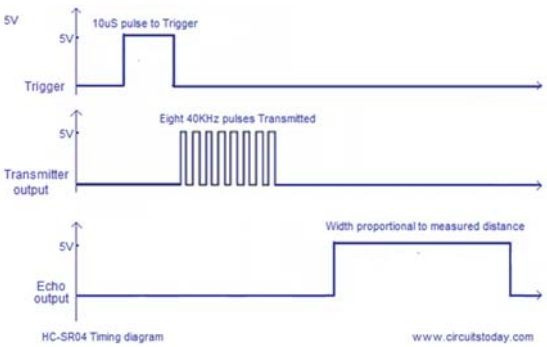

Fig. 3 Distance meter HC-SR04 operation

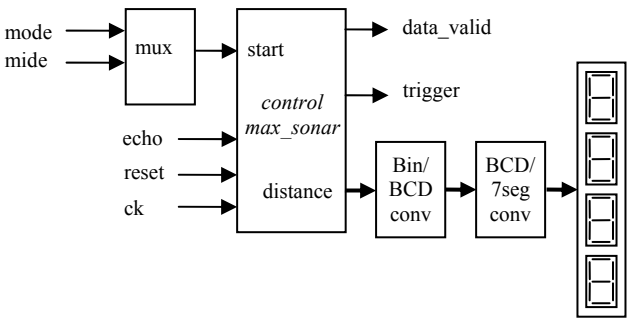

Fig. 4 Block diagram of *max_sonar* system

IV. Conclusions

With this set of laboratory sessions we have made the students face a design of a certain complexity by decomposing it into simpler designs. We have also achieved that each of the parts into which the design has been broken down corresponds to a single laboratory session. In addition, the complete design process is incorporated in each session, i.e. the writing of the VHDL code, debugging of errors, writing of the stimulus file (testbench) that allows functional simulation and, where appropriate, implementation on the board and experimental testing.

Acknowledgements

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References

[1] The teaching project can be consulted at the link: http://www.us.es/estudios/grados/plan_201/asignatura_2010034 (accessed in February 2018).

[2] The teaching project can be consulted at the following link: http://www.us.es/estudios/grados/plan_201/asignatura_2010011 (accessed February 2018).

[3] The teaching project can be consulted at the following link: http://www.us.es/estudios/grados/plan_201/asignatura_2010018 (accessed February 2018).

[4] The HC-SR04 meter specifications can be found at http://www.micropik.com/PDF/HCSR04.pdf

[5] The specifications of the Nexys4 development board can be found at: https://reference.digilentinc.com/reference/programmable-logic/nexys-4-ddr/reference-manual

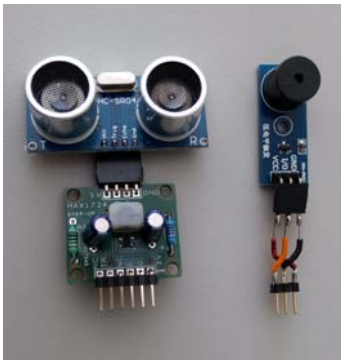

Fig 5 Distance meter (left) and buzzer (right)

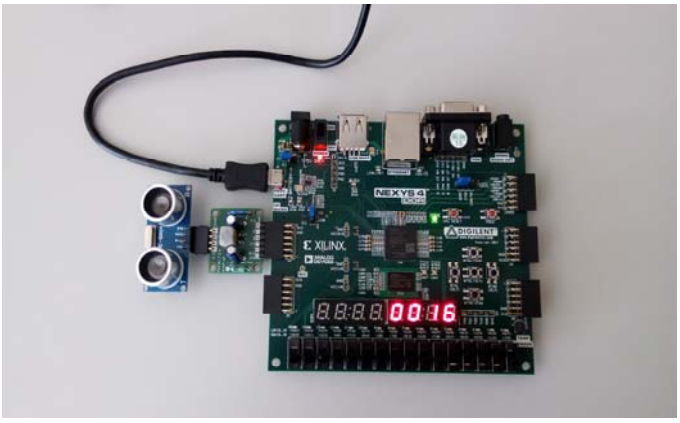

Fig. 6 Development board and meter. Results after Lab3

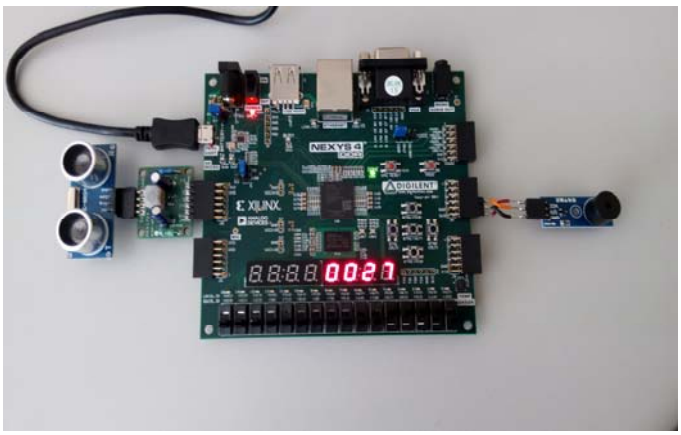

Fig. 7 Development board and meter. Results after Lab4