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# Analog CMOS Readout Channel for Time and Amplitude Measurements With Radiation Sensitivity Analysis for Gain-Boosting Amplifiers

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**ABSTRACT** The front-end readout channel consists of a charge sensitive amplifier (CSA) and two different unipolar-shaping circuits to generate pulses suitable for time and energy measurement. The signal processing chain of the single channel is built of two different parallel processing paths: a fast path with a peaking time of 30 ns to obtain the time of arrival for each particle impinging the detector; and a slow path with a peaking time of 400 ns dedicated for low noise amplitude measurements, which is formed by a pole-zero cancellation circuit and a 4th order complex shaper based on a bridged-T architecture. The tunability of the system is accomplished by the discharge time constant of the CSA in order to accommodate various event rates. The readout system has been implemented in a 180 nm CMOS technology with the size of 525 $\mu$m x 290 $\mu$m. The building blocks use compact gain-boosting techniques based on quasi-floating gate (QFG) transistors achieving accurate energy measurement with good resolution. The high impedance nodes of QFG transistors require a detailed study of sensitivity to single-effect transients (SET). After carrying out this study, this paper proposes a method to select the value of the QFG capacitors, minimizing the area occupancy while maintaining robustness to radiation. The nonlinearity of the CSA-slow-shaper has been found to be less than 1% over a 10-70 fC input charge. The power dissipation of the readout channel is 4.1 mW with a supply voltage of 1.8 V.

**INDEX TERMS** Low power sensor interface circuits, analog front-end electronics, semiconductor detectors, complex shaper, charge sensitive amplifier.

## I. INTRODUCTION

Front-end electronics (FEE) are a fundamental part in the signal processing systems of modern particle detectors. Regardless of the type of experiment and associated electronics, some basic principles are common: the electronic readout system has to acquire the signals from the sensor, digitizing and storing them for later analysis. The design of readout front-end channels finds great interest nowadays in applications where the sensor response to external physical stimulus is given in form of electrical charge, typically a short current pulse. Signal processing from radiation detectors for nuclear or particle physics, or medical imaging applications, are particular fields where FEE are widely used, with a trend towards complete system on chip design solutions [1]–[4].

In addition, in some of these scenarios the performance of analog circuits under radiation conditions is nowadays a main concern. This hostile environment, in which the FEE systems often operate, requires designs that take into consideration the harmful effect of radiation on some electronic components, especially those based on semiconductors, as this increases the probability of failure.

FEE refers to the closest electronics to the detector, and involves signal conditioning tasks related to charge to voltage conversion, amplification, pulse-shape conformation and analog-to-digital conversion. The operational amplifier

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(op-amp) is the most important building block for the analog part of a front-end system, whose performance limits most of the properties of the overall front-end channel. With the increasing demand for a higher number of channels, and given their high density of electronic components, the performance of sensors and sensor interface integrated circuits is increasingly important. Systems with low noise and low power consumption have become essential. In particular, the power efficiency of the analog building blocks must be improved.

An extensive discussion over the design of readout systems for semiconductor radiation detectors exists in literature [5]–[11], yet these systems require continuous improvement in order to keep up with the developments in modern detector systems. Furthermore, many of the available integrated readout circuits are implemented in modern CMOS technologies, where several trade-offs must be conciliated: power dissipation-bandwidth, low voltage-high gain, low voltage-high output swing, noise-power dissipation and high gain-small size transistors. In particular, the scaling properties of the VLSI processes have degraded some analog parameters of the transistors, and thus, they have also changed the design techniques used for CMOS analog circuits. In this way, the low output resistance of the transistors directly decreases the gain. Thus, for a proper closed-loop operation of the main circuits of a FEE, i.e., charge sensitive amplifiers (CSA) and shapers, the open-loop gain of their active elements (op-amps) must be high enough.

To this end, several approaches have been introduced [12]–[15]. One of the most extended techniques is the regulated cascode, based on the use of an extra amplifier to achieve a local negative feedback loop that further enhances the output resistance of the circuit [16]. The implementation of this extra amplifier determines the performance of the complete op-amp in terms of power consumption, bandwidth, chip area, and supply voltage.

This work addresses the low open-loop gain problem related to the degradation of the analog properties of transistors in modern CMOS technologies. A single stage telescopic amplifier is designed using a local feedback amplifier, resulting in an increased amplifier output resistance. The auxiliary amplifier is realized in a compact design based on the quasi-floating gate (QFG) technique, which has the effect of only a low increase in power consumption, making it suitable for low voltage applications [17], [18]. The properties of the telescopic amplifier have been exploited to design a front-end readout system for charged particle detection using silicon as detector material. Furthermore, as the proposed FEE is intended for radiation detection, these techniques should be validated assuming that the readout channel works in harsh environments, such as, particle accelerators or nuclear applications, where high levels of ionizing radiation interact with analog components, producing large voltage transients, which must be taken into account to ensure a proper functionality of the system.

In the particular case of the proposed circuit, the use of QFG transistors could compromise the behavior of the circuit due to the existence of very high impedance nodes. These nodes could cause the transient voltage variations due to an impact (single-event transient, SET) to lengthen over time, preventing the use of the circuit for harsh environments. In this paper, the effect of high-energy particles impacts on QFG transistors has been analyzed in detail and a methodology has been proposed that allows selecting a value of QFG capacitors to minimize the effect of radiation. This study and methodology are based on the use of an automatic tool to evaluate the sensitivity to single-event effects (SEE) [19].

The paper is organized as follows: Section II describes the basic architecture of the front-end readout channel and presents in detail the circuit schematics. Section III deals with the simulation results and analyzes the robustness to radiation of the front-end system, and in particular, of the QFG technique. Section IV deals with the measurement results of the system. Section V presents the noise performance. Finally, some conclusions are drawn in Section VI.

## II. FRONT-END READOUT CHANNEL

Fig. 1 shows a block diagram of the readout front-end system designed for semiconductor particle detectors. The ASIC consists of a single readout channel formed by a charge sensitive amplifier (CSA) with a capacitive feedback $C_F$ and a resistive feedback ($M_F$) connected in parallel, a pole-zero cancellation (PZC) network, a differentiator CR-stage, two second-order bridged-T filters connected in cascade (slow shaper) and a CR-RC filter (fast shaper). The internal bias-networks are not shown in the block diagram.

The input charge comes from the detector, which is a solid-state device made of silicon. The detector is an inversely biased *pn* junction built with two electrodes to which a high electrical potential is applied. The detector directly transforms the impinging radiation into an electrical signal. The radiation generates electron-hole pairs, which are put in motion by the influence of the electrical field, producing an electrical current. In nuclear and particle physics, the signals obtained are usually pulse signals.

### A. CHARGE SENSITIVE AMPLIFIER AND DESIGN CONSIDERATIONS

Since the charge $Q_{IN}$ delivered by the semiconductor detector is very small it is quite impractical for immediate signal processing. A proper amplification is required, and for this reason, preamplifiers are the first stage in the readout system. They are usually placed closest to the detector for noise minimization, since noise at this stage is critical. The preamplifier provides an output pulse whose amplitude is proportional to the charge released by the incident radiation.

A charge sensitive amplifier is adopted for the collection of the charges from the detector since this type of amplifier provides a charge-to-voltage conversion independent of the capacitance at the input node (both the detector capacitance and parasitic capacitances). Assuming at the input a delta-like current pulse a voltage step is obtained at the CSA output, which is proportional to the total charge carried by the

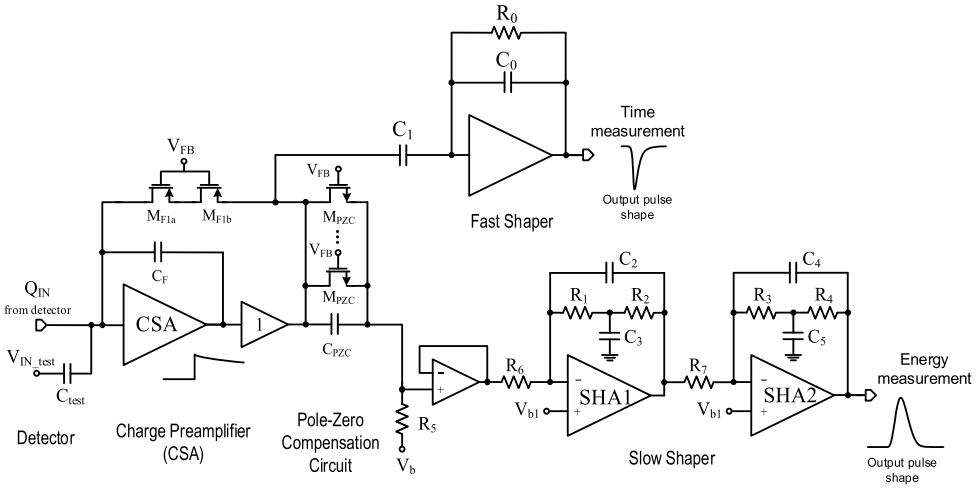


**FIGURE 1.** Simplified block diagram of the signal processing chain.

detector pulse, given by:

$$v_{out}(t) = -\frac{A}{(A+1)C_F + C_i} Q_{IN} \tag{1}$$

where $C_F$ is the feedback capacitor of the CSA and $C_i$ is the total capacitance at the input node. If the op-amp has a large open loop gain ($A \gg 1$), then the above equation can be simplified to $v_{out}(t) = -Q_{IN}/C_F$, and the conversion gain is determined by a well-controlled component, the feedback capacitor. Thus, this work is focused on achieving this high gain since for old CMOS technologies it is relatively easy to reach, but for modern CMOS processes additional gain enhancement techniques are needed.

The core of the preamplifier is a modified telescopic amplifier shown in Fig. 2. This topology uses cascode transistors that allow achieving quite large gain for a single stage due to the large impedance at the output node. This also requires that the current sources connected to the output nodes are realized using cascode current mirrors. The voltage gain can be written as $G_m \cdot R_{out}$, where $G_m \approx g_{m1}$ and

$$R_{out} = \{[1 + (g_{m2} + g_{mb2})r_{o2}]r_{o1} + r_{o2}\} \parallel \parallel \{[1 + (g_{m3} + g_{mb3})r_{o3}]r_{o4} + r_{o3}\} \tag{2}$$

For typical values, the voltage gain can be approximate as:

$$A_v \approx g_{m1}[(g_{m2}r_{o2}r_{o1})] \parallel [(g_{m3}r_{o3}r_{o4})] \tag{3}$$

A large bandwidth is also required to process the fast pulses from the detector. Usually, for the telescopic topology the high gain is obtained without any degradation in speed if a careful design is made.

The use of cascode transistors limits the output swing and if the gate bias voltages are chosen properly, the maximum output swing is equal to $V_{DD} - (|V_{OD1}| + |V_{OD2}| - V_{OD3} - V_{OD4})$, where $V_{ODi} = V_{GSi} - V_{THi}$ denotes the overdrive voltage of $M_i$. Nevertheless, for the charge sensitive amplifier it is possible to use cascode transistors since the output swings are only of several tens of millivolts.

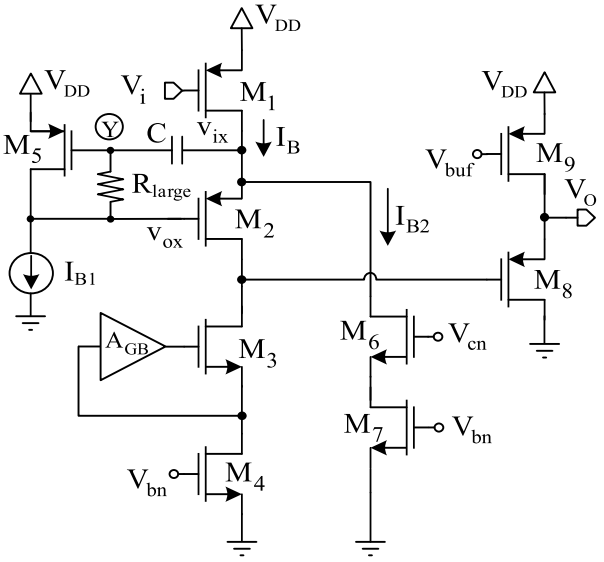


**FIGURE 2.** Schematic of the charge sensitive amplifier.

A pMOS has been chosen as input transistor ($M_1$) for its superior noise performance, since for modern CMOS technologies the flicker noise becomes more significant. The cascode transistor $M_2$ limits the voltage across the input transistor and minimizes short-channel effects.

As mentioned above, the open loop gain of the telescopic amplifier determines the performance of the feedback system, i.e., the accuracy of the charge-to-voltage conversion. In order to increase the gain, from eq. (3) we must increase the transconductance of the input transistor $g_{m1}$ or the output resistance of transistors $r_o$. In practice, noise requirements also require to increase $g_{m1}$ through the width and the bias current. With respect to $r_o$, its value is given by $1/(\lambda \cdot I_D)$, and $\lambda \propto 1/L$ yielding $r_o \propto L/I_D$. To increase $L$, since $M_1$ and $M_2$ appear in the path signal, it is desirable to keep their capacitances to a minimum, whilst $M_3$ and $M_4$ affect the

signal to a much lesser extent, have greater mobility and can therefore have larger dimensions, doubling the length and width. Note that, since in a conventional telescopic amplifier the same current flows through both transistors $M_4$ and $M_1$, it is difficult to decrease $I_D$, which makes it complicated to simultaneously obtain high transconductance $g_{m1}$ of input transistor $M_1$ and a high output resistance $r_{o4}(r_{o3})$ of transistor $M_4$ ($M_3$).

In this work, in addition to the design considerations described above, and taking into account that the intrinsic gain of transistors decreases continuously as sizes scale down, additional gain enhancement techniques are addressed [20], [21]. The telescopic amplifier in Fig. 2 includes two of them: (1) the regulated cascode approach based on a local negative feedback loop that increases the gain by a factor $A_{GB}$ [13]; and (2) an additional biasing branch formed by $M_6$ and $M_7$ that delivers most of the current of the input transistor $M_1$, overcoming the aforementioned $g_{m1}$-$I_D$ trade-off, and improving noise performance (as the input transistor carries out all the current) [22], [23]. A conventional source follower stage formed by $M_8$ and $M_9$, which acts as an output buffer, has been included to drive the load.

The regulated cascode technique does not compromise stability nor reduces headroom if it is used at low swing internal nodes. Different topologies to realize the local feedback (or auxiliary) amplifier, which enhances the effective gain of the cascode transistor, have been reported [24]–[28]. The proposed implementation in this work is based on a simple common-source amplifier ($M_5$ and $I_{B1}$) but combined with the QFG technique [18] to mainly overcome the limitation of low supply voltages. If the gate of transistor $M_5$ is directly connected to the drain of $M_1$, the maximum voltage at the drain of $M_1$ is given by $V_{DD}-(V_{TH5}+V_{DS,sat5})$, where $V_{DS,sat5}$ is the overdrive voltage for $M_5$ to remain in saturation.

However, the use of the QFG approach achieves that the gate of $M_5$ is connected to a DC biasing voltage through a large resistive element $R_{large}$, and it is AC coupled to signals by means of the small valued capacitor $C$. The gate of $M_5$ is decoupled in DC of the drain of $M_1$ (and thus, this node can operate at higher voltages), and transistor $M_5$ acts as a diode in DC, making $V_{GS}=V_{DS}$. $R_{large}$ is implemented using a series connection of diode-connected transistors [29]. The path for signals from the drain of $M_1$ is a high pass filter while for signals at the drain of $M_5$ is a low pass filter, both with corner frequency $f_c=1/(2\pi R_{large}C)$, typically of a few Hz. At frequencies higher than $f_c$ the drain of $M_5$ is no longer connected to the gate, whereas the coupling capacitor $C$ establishes a connection between the drain of $M_1$ and the gate of $M_5$. Thanks to the large value of $R_{large}$, the value of the capacitor $C$ is only limited by the parasitic capacitance at node $Y$ in order not to attenuate the voltage transferred from the drain of $M_1$ to the gate of $M_5$. A similar QFG scheme is applied to cascode transistor $M_3$. Finally, the QFG gain-boosting (GB) auxiliary amplifier does not introduce additional noise. Thus, the noise generated by the resistance $R_{large}$ is negligible since it is not a resistance due to the channel of the transistor, but the leakage resistance of a diode-connected transistor operating in the cutoff region.

Regarding the feedback network, the pMOS transistors $M_{F1a}$ and $M_{F1b}$ in Fig. 1 behave as an active resistance ($R_F$) connected in parallel to the feedback capacitor $C_F$ to avoid saturation of the CSA by continuously discharging the feedback capacitance. These transistors contribute to the parallel noise at the CSA input and their values were chosen to be high (nominal value of 1.5 MΩ, with transistor dimensions W/L of 0.5 $\mu$m/10 $\mu$m and $V_{FB}=100$ mV) as a trade-off between noise and counting rate. A high resistance value provides a slow pulse tail and minimizes the noise introduced, but a tail too slow can lead to pile-up effects resulting in the overlap between successive pulses in high rate experiments. The use of active feedback transistors instead of passive resistors saves area and reduces parasitic capacitances, and allows controlling the feedback resistance. The CSA pulse output decays exponentially with a relatively long discharge time constant $\tau_F = C_F \cdot R_F$. $C_F$ has been set to 500 fF.

### B. POLE-ZERO COMPENSATION CIRCUIT

The low frequency part of the CSA output pulse is removed by an RC differentiator stage (high pass section) formed by $C_{PZC}$ and $R_5$ in Fig. 1. The CSA feedback network together with the differentiator stage create an undershoot at the shaper output, which produces a baseline shift, and thus, a loss of the amplitude resolution of the system. The undershoot can be removed applying a pole-zero cancellation circuit by adding a resistor $M_{PZC}$ ($R_{PZC}$) in parallel to the capacitor $C_{PZC}$ [30]. This resistor has also been implemented by pMOS transistors and creates a zero that cancels the pole introduced by the feedback network of the CSA. The transfer function is given as:

$$H(s) = -Q_{IN} \cdot \frac{R_F}{1+sC_FR_F} \cdot \frac{1+sC_{PZC}R_{PZC}}{R_{PZC}} \qquad (4)$$

where $R_F$ and $R_{PZC}$ represent the equivalent small signal channel resistance of the $M_F$ and $M_{PZC}$ transistors, respectively. The correct cancellation requires that the condition $C_F \cdot R_F = C_{PZC} \cdot R_{PZC}$ is satisfied.

### C. PULSE SHAPERS

The CSA output is split into two different bandpass filters to process in parallel the incoming pulses for time and energy measurements. The fast path is a CR-RC shaper optimized to determine the input charge arrival time with a peaking time of 30 ns. The pulse peaking time is measured from 1% of the peak height to the center of the peak and is related to the time constant of the shaper. The slow path is a shaper consisting of two $(RC)^2$ filters in cascade shaper used for peak-amplitude measurement with a peaking time of 400 ns. The aim of the slow shaper is to optimize the overall signal to noise ratio by filtering the CSA output, limit the pulse width to reduce the possibility of pulse pile-up, and provide additional gain to the analog processing chain.

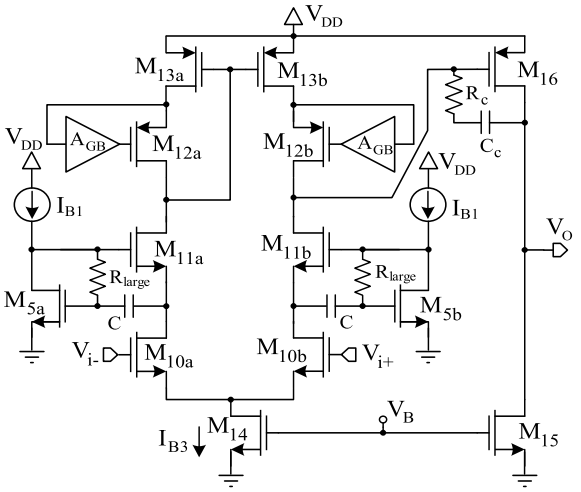


**FIGURE 3.** Schematic of gain-boosted rail-to-rail two-stage amplifier for the slow shaper.

The amplifier used as the core for the fast shaper has the same topology as that of the CSA, but the size and the power dissipation of the input transistor is lower because it has less influence on the noise performance of the entire system. However, for the slow shaper a different amplifier topology has been used. Thus, a two-stage op-amp has been designed as shown in Fig. 3. The input stage is based on the telescopic topology with QFG gain-boosting scheme equal to that of the CSA but scaled-down, and the output stage is a rail-to-rail common source scheme that maximizes the output swing. With a supply voltage of only 1.8 V, it is advisable to avoid using cascode transistors in the output branch of the slow shaper in order to enlarge the output voltage range that the front-end electronics can handle.

The choice of the filter type, order and its time constants strongly depends on the specified energy resolution of the readout system and its high-rate operation requirements. Two types of filters are often used: semi-Gaussian pulse shaper CR-$(RC)^n$ based on real poles, and quasi-Gaussian shaper. For the same filter order $n$, the quasi-Gaussian shaper is more suitable for low noise performance and high rate applications since it allows obtaining a shorter and symmetrical pulse. This satisfies the baseline return time requirement, which is a fraction of the average interarrival time, precluding the overlap between successive pulses.

A compact approach to obtain a quasi-Gaussian filter, which can be applicable in integrated circuits, uses a simple CR differentiator with a real pole followed by a limited number of active filter sections, which have complex poles obtained on the basis of frequency domain analysis.

The designed slow shaper is implemented with two second-order bridged-T filters connected in cascade, and optimized for low noise accurate peak-amplitude measurement. The transfer function of each second-order section shown in Fig. 1 is given as:

$$H(s) = -\frac{R_1 + R_2}{R_6} \frac{sC_3 \frac{R_1 R_2}{R_1 + R_2} + 1}{1 + sC_2(R_1 + R_2) + s^2 C_2 R_1 C_3 R_2} \quad (5)$$

The procedure used to design the quasi-Gaussian filter (or complex shaper) follows the direct synthesis method [31]. The simple CR differentiator formed by $R_5$ and $C_{PZC}$ in Fig. 1 realizes a real pole, which determines the time constant. The two complex conjugated poles obtained by the 4th order bridged-T topology are in the positions:

$$s_1 = \frac{R_1 + R_2}{2C_3 R_1 R_2} \left[ -1 \pm j \sqrt{\frac{4C_3 R_1 R_2}{C_2(R_1 + R_2)^2} - 1} \right] \quad (6)$$

The relation between the time constant of the differentiator and the real pole is given by $R_5 \cdot C_{PZC} = \sigma_0 \tau_x / A_0$, where $A_0 = 1.4766878$, $\sigma_0 = 1.0844$ and $\tau_x$ is the time constant of a CR-RC filter. For $\tau_x = 250$ ns, $R_5$ has been set to 91.5 kΩ yielding $C_{PZC} = 2$ pF. The complex pole pairs are $p_i = -A_i \pm W_i$, where $A_i$ and $W_i$ are the real and the imaginary parts, respectively. From (6), they are given by:

$$A_i = \frac{\sigma_0 \tau_x (R_1 + R_2)}{2C_3 R_1 R_2} \quad (7)$$

$$W_i = \frac{\sigma_0 \tau_x (R_1 + R_2)}{2C_3 R_1 R_2} \sqrt{\frac{4C_3 R_1 R_2}{C_2(R_1 + R_2)^2} - 1} \quad (8)$$

The coefficients $A_i$ and $W_i$ are provided in [31] for each second-order stage of the filter. In order to simplify the design, all resistances are set to the same value $R = R_1 = R_2 = R_3 = R_4 = 40$ kΩ. For the first stage: $A_1 = 1.4166647$, $W_1 = 0.5978596$, and for the second stage: $A_2 = 1.2036832$ and $W_2 = 1.2994843$. From (7), $C_3 = 4.78$ pF and $C_5 = 5.63$ pF. Applying the same procedure for the imaginary part in (8) yields $1+(W_i/A_i)^2 = C_3/C_2$. As result, $C_2 = 4.06$ pF and $C_4 = 2.6$ pF. For $\tau_x = 250$ ns the peaking time of this Gaussian filter is about $t_p = 400$ ns.

It can be noted in (5) that the gain can be varied by adjusting the resistance $R_6$, and this has no effect upon the location of the pole of the filter. This resistance has been set to $R_6 = R_7 = 20$ kΩ.

Regarding the fast shaper, the values have been set to: $C_0 = 650$ fF, $R_0 = 8$ kΩ, and $C_1 = 4$ pF, providing a peaking time of 30 ns.

## III. SINGLE EVENT EFFECTS RADIATION STUDY

The readout channel has been tested to analyze its robustness under irradiation conditions using a tool designed by some of the authors. The Analog FTU hardware debugging system, AFTU [19], is a software tool that allows circuit designers to evaluate the SEE sensitivity of analog/mixed signal circuits at transistor level. To this end, AFTU takes a Spectre-based netlist and automatically adds charge injection elements all over the circuit to emulate the effects of high-energy charged particle impacts without changing its functional behavior. The user can define a test campaign to simulate the influence of SEEs by means of three input configuration files. From them, AFTU creates an Ocean script-based file that manages a sensitivity analysis according to some predefined heuristics and parameters. The result of running the script is a file (.csv)

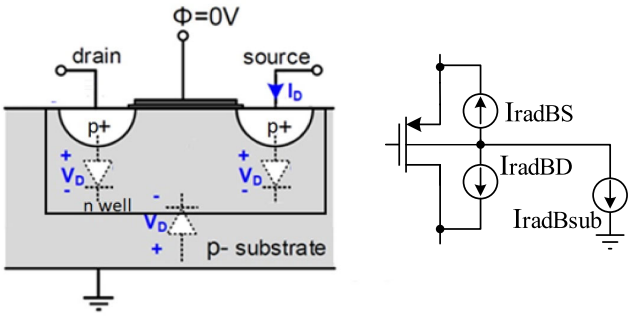


**FIGURE 4.** Model of a particle impact on a pMOS transistor.

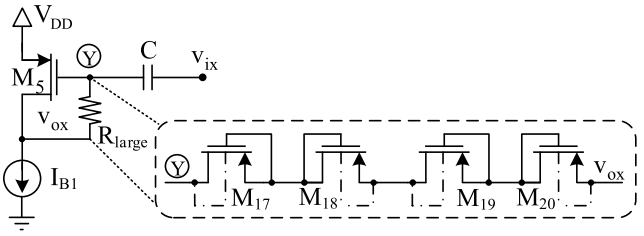


**FIGURE 5.** GB (Gain-Boosting) scheme for pMOS (GBP) transistors with $R_{large}$ implementation.

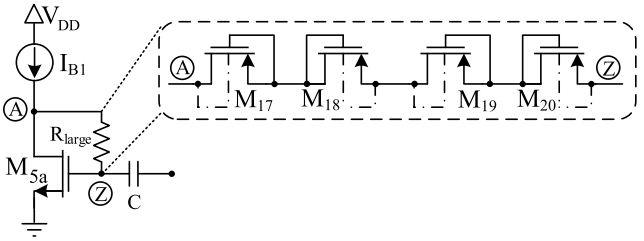


**FIGURE 6.** GB (Gain-Boosting) scheme for nMOS (GBN) transistors with $R_{large}$ implementation.

that contains all the results, classified following the applied criteria settled by the user.

Since there are no memory elements in this design, the study of SEE will be focused on the effect of Single Event Transients (SET). For the proposed circuit, an ''amplitude/pulse width'' analog metric has been settled to detect potentially dangerous transient pulses, determining its maximum voltage deviation (from non-irradiated signal values) and maximum recovery times. The current sources used as charge injection elements follow the double exponential model [32], [33]. Standard formulas (9) and (10) are applied:

$$Q = \mathrm{dLET}\frac{e\rho}{E_p} \tag{9}$$

$$I_{rad} = \frac{Q}{\tau_d - \tau_r}\left(e^{-\frac{t}{\tau_d}} - e^{-\frac{t}{\tau_r}}\right) \tag{10}$$

where $e$ is the electron charge, $\rho$ is the Si density, $E_p$ =3.6 eV is the e-h pair energy creation, *LET* is linear energy transfer, and $d = 2\ \mu$m is the recollection depth.

As previously stated, the impact of ionizing particles can generate charge injections into different nodes of the circuits, leading to the appearance of SET effects. The use of QFG has allowed the design of gain-boosting techniques in a very compact way. Nevertheless, the use of the QFG technique implies the existence of very high impedance nodes in which a transient effect can be particularly relevant, as it can last a large amount of time. Due to this situation, the study of these effects using AFTU to evaluate circuit robustness could be of great interest to ensure a proper functionality of the elements involved. Such a study to evaluate the effects of SETs over the QFG technique has not yet been performed, to our knowledge.

To this end, a representation of a pMOS transistor with its parasitic *pn* junctions, that can be affected by an impact of a particle, and all the possible current sources modelling charge injections [33] are shown in Fig. 4. For the case of an nMOS transistor, the model is similar but only sources that inject a current from drain/source to bulk are modelled.

Figs. 5 and 6 show the implementation of $R_{large}$ for both gain-boosting schemes.

There are several blocks in which the QFG technique is applied: two in the CSA amplifier and four in each slow shaper amplifier (SHA1, SHA2). Impact simulations have been carried out for each QFG block of the circuit. For the sake of clarity, the results obtained for the study of the CSA blocks will be explained in detail, while a qualitative discussion of the effects in the SHA blocks will be included taking into account the previous study in the CSA.

The procedure followed is based on evaluating the nominal performance of the system and comparing it with the results after an impact in a QFG block. In this way, we can observe the outputs of the circuit and classify the different SET effects depending on their influence into four possible classes:

I. Impacts with no influence at the output (Fig. 7a).
II. A transient effect with recovery times shorter than the time between impacts (5 $\mu$s) (Fig. 7b).
III. Impacts that generate large variations in the output voltage, affecting several consecutive impacts (Fig. 7c).
IV. Impacts that cause the system to completely stop functioning as a detector (Fig. 7d).

The most relevant results from the simulations are summarized in Table 1 for the CSA amplifier, where the voltage deviation at the output of the system is quantified for class III effects and circuit malfunctions as a detector (class IV) are marked as an X for every transistor in which the impact has been emulated. A value of charge of 0.3 pC has been used as a worst-case injection, based on estimations for a similar technology studied in [34] and the previous work carried out in similar studies using AFTU [19], [35], applying the formulas in (9) and (10). This corresponds to a LET of approximately 15 MeV-cm$^2$/mg, which is less than the maximum expected for radiation environments such as the

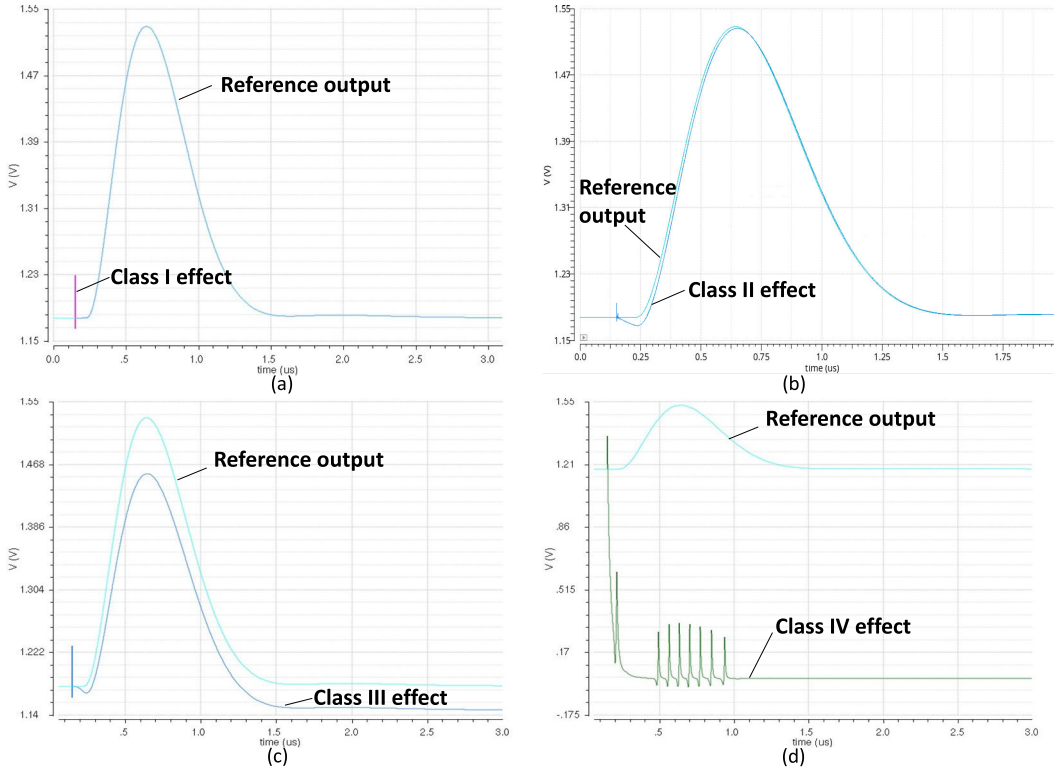


**FIGURE 7.** (a) Class I: no influence at the output. (b) Class II: influence during an impact cycle. (c) Class III: influence affecting several cycles. (d) Class IV: Impacts that cause a circuit malfunction.

**TABLE 1.** Effects of SET impacts on transistors implementing $R_{large}$ in the GBP (Fig. 5) and GBN (Fig. 6) blocks inside the CSA amplifier (Figs. 1 and 2).

| Block | Error class | ΔV [mV] at the output for impacts in transistor | | | |
|---|---|---|---|---|---|
| | | $M_{17}$ | $M_{18}$ | $M_{19}$ | $M_{20}$ |
| GBN | III | - | 29 | 29 | 29 |
| GBP | IV | X | X | X | - |

**TABLE 2.** Effects of SET impacts on transistors implementing $R_{large}$ in the two GBP (Fig. 5) and the two GBN (Fig. 6) blocks inside the SHA1 amplifier (Figs. 1 and 3).

| Block | Error class | ΔV [mV] at the output for impacts in transistor | | | |
|---|---|---|---|---|---|
| | | $M_{17}$ | $M_{18}$ | $M_{19}$ | $M_{20}$ |
| GBN1 | III | 3.5 | 160 | 160 | 187 |
| GBP1 | IV | X | X | X | - |
| GBN2 | III | 5 | 150 | 150 | 72 |
| GBP2 | IV | X | X | X | - |

High-Luminosity Large Hadron Collider tracker at ATLAS or CMS [35].

The results of the rest of the blocks in the SHA op-amps are also summarized in Tables 2 and 3.

From these results, it can be seen that the GBP block is more affected by impacts than the GBN scheme for every op-amp. A possible solution to this effect can be to increase the value of the capacitor in the GB scheme, to decrease the

**TABLE 3.** Effects of SET impacts on transistors implementing $R_{large}$ in the two GBP (Fig. 5) and two GBN (Fig. 6) blocks inside the SHA2 amplifier (Figs. 1 and 3).

| Block | Error class | ΔV [mV] at the output for impacts in transistor | | | |
|---|---|---|---|---|---|
| | | $M_{17}$ | $M_{18}$ | $M_{19}$ | $M_{20}$ |
| GBN1 | III | 1 | 49 | 49 | 53 |
| GBP1 | IV | X | X | X | - |
| GBN2 | III | 1 | 51 | 51 | 56 |
| GBP2 | IV | X | X | X | - |

voltage variation in the node which is affecting the circuit performance.

From simulations of impacts in the GBP block of first CSA amplifier (Table 1), it can be seen how the circuit performance can be corrected by using a higher value of the capacitor C (Fig. 5). As an illustrative case, Fig. 8 represents the effect of an impact that generates a malfunction with C= 200 fF (nominal design value) and C=1.2 pF.

In this way, the analysis using AFTU not only allows determining circuit vulnerabilities, but it can also be used to solve those vulnerabilities. By means of performing simulations for different sizes of the capacitor we can optimize the robustness of the GB blocks in the proposed scheme, determining an appropriate value. Of course, the larger the capacitor value, the more robust the circuit will be with respect to SET, at the cost of significantly increasing its area. The simulations carried out make it possible to select the minimum value of the

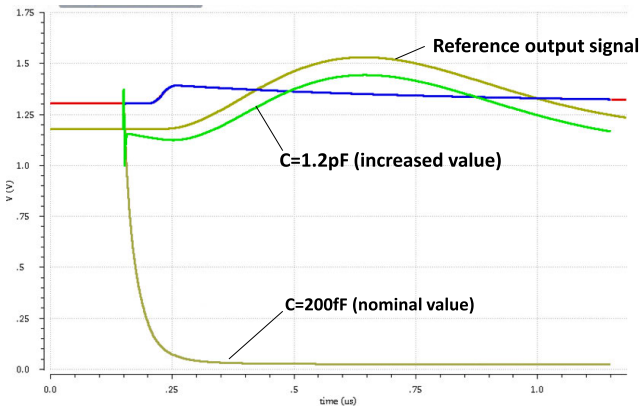


**FIGURE 8.** Possible correction to increase the circuit robustness.

**TABLE 4.** Effects of SETs on CSA amplifier (Figs. 1 and 2), evaluating the response of the output for different capacitor sizes for impacts in the GBP block (Fig. 5).

| Cap value [fF] | Error class | ΔV [mV] at the output for impacts in transistor | | | |
|---|---|---|---|---|---|
| | | $M_{17}$ | $M_{18}$ | $M_{19}$ | $M_{20}$ |
| 200 | IV | X | X | X | - |
| 500 | IV/III | X | 125 | 125 | - |
| 800 | III | 171 | 73 | 73 | - |
| 1200 | III | 97 | 46 | 46 | - |

**TABLE 5.** Effects of SETs on CSA amplifier (Figs.1 and 2), evaluating the response of the output for different capacitor sizes for impacts in the GBN block (Fig. 6).

| Cap value [fF] | Error class | ΔV [mV] at the output for impacts in transistor | | | |
|---|---|---|---|---|---|
| | | $M_{17}$ | $M_{18}$ | $M_{19}$ | $M_{20}$ |
| 200 | III | - | 29 | 29 | 29 |
| 500 | III | - | 25 | 25 | 29 |
| 800 | III | - | 18 | 18 | 27 |
| 1200 | III | - | 13 | 13 | 21 |

QFG capacitors while maintaining robustness to radiation. In Tables 4 and 5, the effect of increasing the capacitor size is summarized for the GB blocks in the CSA amplifier.

If we perform a similar analysis for the other two SHA op-amps, each one with four GB blocks, we can also adjust the capacitor to an optimum value. This effect is summarized in Tables 6, 7, 8 and 9. As it can be noticed, we can correct some class IV errors and convert them into class III errors, using AFTU to optimize the capacitor size for the most sensitive GB blocks.

As a result of the performed study, the values of the capacitors have been selected for every QFG block to ensure that the front-end readout channel works properly as a detector. In this way, we are ensuring that impacts will not generate any class IV error at the output of the circuit. The capacitor values have been selected considering a trade-off between robustness and area occupation, allowing a maximum error of 100 mV in the worst cases (GBP blocks), and 40 mV in the GBN schemes.

**TABLE 6.** Effects of SETs on SHA1 amplifier (Figs. 1 and 3), evaluating the response of the output for different capacitor sizes for impacts in the GBP block (Fig. 5).

| Cap value [fF] | Error class | ΔV [mV] at the output for impacts in transistor | | | |
|---|---|---|---|---|---|
| | | $M_{17}$ | $M_{18}$ | $M_{17bis}$ | $M_{18bis}$ |
| 200 | IV | X | X | X | X |
| 500 | IV | X | X | X | X |
| 800 | III | 49 | 80 | 173 | 152 |
| 1200 | III | 35 | 13 | 102 | 78 |

**TABLE 7.** Effects of SETs on SHA1 amplifier (Figs. 1 and 3), evaluating the response of the output for different capacitor sizes for impacts in the GBN block (Fig. 6).

| Cap value [fF] | Error class | ΔV [mV] at the output for impacts in transistor | | | |
|---|---|---|---|---|---|
| | | $M_{19}$ | $M_{20}$ | $M_{19bis}$ | $M_{20bis}$ |
| 200 | III | 161 | 178 | 157 | 175 |
| 300 | III | 52 | 76 | 42 | 67 |
| 500 | III | 24 | 40 | 13 | 34 |
| 800 | III | 13 | 29 | 2 | 19 |

**TABLE 8.** Effects of SETs on SHA2 amplifier (Fig. 1), evaluating the response of the output for different capacitor sizes for impacts in the GBP block (Fig. 5).

| Cap value [fF] | Error class | ΔV [mV] at the output for impacts in transistor | | | |
|---|---|---|---|---|---|
| | | $M_{17}$ | $M_{18}$ | $M_{17bis}$ | $M_{18bis}$ |
| 200 | IV | X | X | X | X |
| 500 | IV/III | X | 132 | X | 149 |
| 800 | III | 90 | 60 | 22 | 31 |
| 1200 | III | 54 | 44 | 10 | 18 |

**TABLE 9.** Effects of SETs on SHA2 amplifier (Fig. 1), evaluating the response of the output for different capacitor sizes for impacts in the GBN block (Fig. 6).

| Cap value [fF] | Error class | ΔV [mV] at the output for impacts in transistor | | | |
|---|---|---|---|---|---|
| | | $M_{19}$ | $M_{20}$ | $M_{19bis}$ | $M_{20bis}$ |
| 200 | III | 51 | 56 | 49 | 53 |
| 300 | III | 39 | 47 | 36 | 44 |
| 500 | III | 32 | 40 | 29 | 37 |
| 800 | III | 26 | 33 | 24 | 32 |

**TABLE 10.** Capacitor values for design optimization for every GB block (Figs. 5 and 6) inside the different amplifier blocks (Fig. 1).

| Op-amp block | Capacitor value [fF] | | | |
|---|---|---|---|---|
| | GBP1 | GBN1 | GBP2 | GBN2 |
| CSA | 1200 | 200 | - | - |
| SHA1 | 800 | 500 | 1200 | 500 |
| SHA2 | 800 | 500 | 800 | 500 |

The final values implemented are summarized in Table 10 for each GB block of the scheme.

In addition to these contributions, simulations to determine the minimum value of charge required to generate a voltage variation of at least 10 mV at the output have been performed, obtaining the results summarized in Table 11. As an example, if we consider the GBP block in the CSA amplifier for a

**TABLE 11. Minimum values of charge that generate a SEE (>10 mV) for every GB block (Figs. 5 and 6) inside the different amplifier blocks (Fig. 1) and different values of capacitors.**

| Op-amp | GB Block | Qcrit [pC] for different values of capacitors [fF] | | | |
|---|---|---|---|---|---|
| | | C=200 | C=500 | C=800 | C=1200 |
| CSA | GBN | 0.02 | 0.05 | 0.075 | 0.15 |
| | GBP | 0.01 | 0.02 | 0.03 | 0.05 |
| SHA1 | GBN1 | 0.02 | 0.02 | 0.02 | 0.05 |
| | GBP1 | 0.02 | 0.02 | 0.03 | 0.05 |
| | GBN2 | 0.02 | 0.02 | 0.02 | 0.05 |
| | GBP2 | 0.02 | 0.02 | 0.03 | 0.05 |
| SHA2 | GBN1 | 0.01 | 0.02 | 0.03 | 0.05 |
| | GBP1 | 0.02 | 0.03 | 0.05 | 0.05 |
| | GBN2 | 0.01 | 0.02 | 0.03 | 0.05 |
| | GBP2 | 0.02 | 0.03 | 0.05 | 0.05 |

**FIGURE 9.** Chip microphotograph.

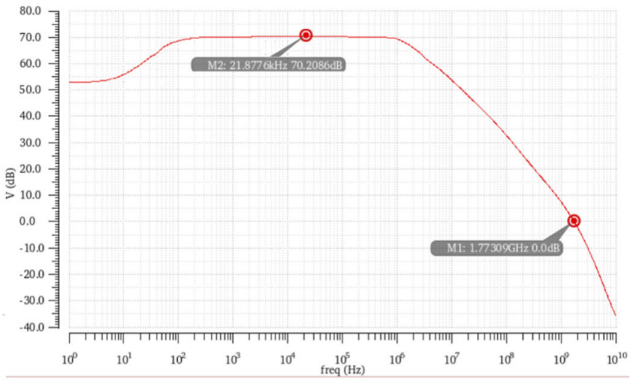


**FIGURE 10.** Simulated frequency response of the operational amplifier of the CSA.

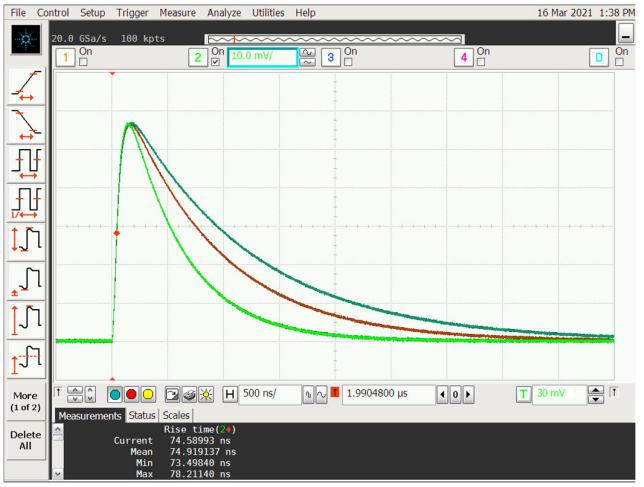


**FIGURE 11.** Transient response of the CSA for an input charge of 30 fC. Tunability of the decay time.

capacitor value of 500 fF, any charge below 0.02 pC will not generate a variation at the output bigger than 10 mV. In this way, we can have an estimation of the "critical charge" for every GB block in the circuit for different sizes of capacitors.

## IV. SIMULATION AND MEASUREMENTS

The front-end channel operates from a single supply voltage of 1.8 V. The microphotograph of the described circuit is shown in Fig. 9. The size of the channel is 525 $\mu$m x 290 $\mu$m, whereas the die size is 1.5 mm x 1.5 mm. The chip was manufactured via MOSIS service in IBM 180 nm CMOS technology. Due to the opaque passivation layer, only capacitors are visible.

The chip also includes a test injection circuit, consisting of a small test capacitor, $C_{test}$ in Fig. 1, that receives a controlled amplitude square voltage signal from a signal generator. A charge $Q_{in} = V_{test}xC_{test}$ is injected at the input of CSA by applying a voltage step through the test capacitor.

The dimensions W/L = 750 $\mu$m/0.18 $\mu$m for the pMOS input transistor $M_1$ of the CSA in Fig. 2 have been chosen according to the noise minimization guidelines for a detector capacitance of $C_{det} = 10$ pF [36]. This transistor is biased with a drain current of 1.125 mA, of which the additional biasing branch formed by $M_6$ and $M_7$ delivers 750 $\mu$A, and its transconductance $g_{m1}$ is 18.3 mA/V. The simulated parameters of the CSA core amplifier are open loop voltage gain $K_V = 3.2$ kV/V, GBW = 1.78 GHz (for a load capacitor of 1 pF) to meet the timing requirements, and current consumption 1.275 mA (2.3 mW) including the QFG gain-boosting schemes and the source follower stage. Note that in Figure 10 at very low frequencies the magnitude presents a first-order high-pass behavior due to the quasi-floating gate technique used for the local feedback amplifier of the regulated cascode, which has no influence on the behavior of the circuit.

Figures 11, 12 and 14 show the measured voltage output waveforms for the CSA, slow shaper and fast shaper, respectively.

The charge sensitive amplifier presents a charge gain of approximately 2 mV/fC due to the feedback capacitor $C_F = 500$ fF. It can be noted in Fig. 11 that the pulse height is about 57 mV, generated by an input test charge $Q_{in} = 30$ fC, which is injected into the CSA input, giving the CSA an

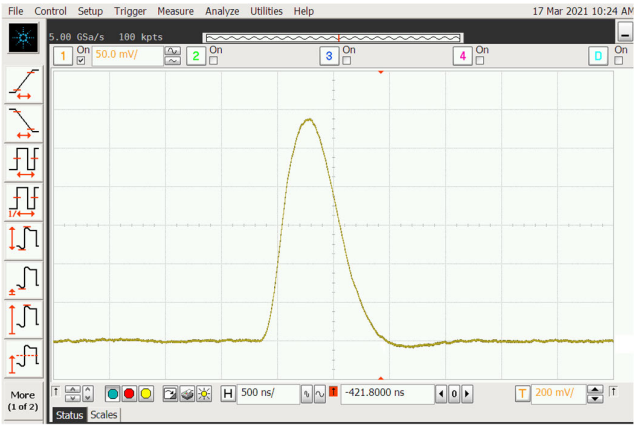


**FIGURE 12.** Measured time response at the slow shaper output.

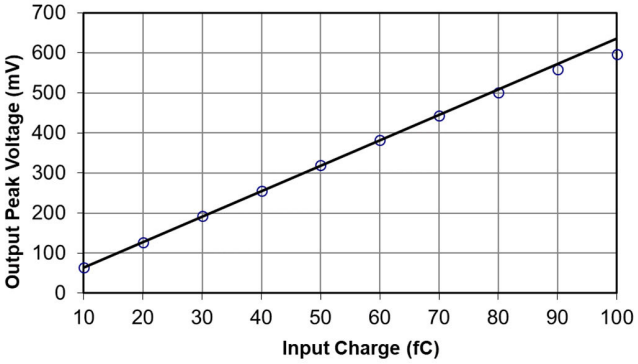


**FIGURE 13.** Output peak amplitude versus input charge.

accurate charge-to-voltage conversion. In addition, the decay time is five times the time constant $R_F \cdot C_F$ and its tunability is suitable in high rate experiments preventing the overlap of successive input pulses. Fig. 11 shows the programmability of the decay time for estimated values of the feedback resistance of 1 MΩ, 1.5 MΩ and 2 MΩ.

Fig. 12 shows the time response of the analog channel to a signal charge of 45 fC, showing a peak height about 290 mV. The peaking time, which is the time when the shaper output reaches the peak amplitude, is about 400 ns. A small undershoot can be observed due to mismatch between resistances in the pole-zero cancellation circuit. The gain pulse of the slow path is around 6.5 mV/fC.

The output voltage of the slow path must be linear for the charge range of the detector. Owing to the rail-to-rail output swing of the two-stage amplifier in Fig. 3, the dynamic range of the slow shaper is enhanced. Fig. 13 shows the energy response and the dynamic range obtained. The nonlinearity of the CSA-slow-shaper has been found to be less than 1% over a 10-70 fC input charge range.

Fig. 14 shows the measured time response of the fast path with a peaking time of around 30 ns.

## V. NOISE ANALYSIS

In order to analyze the noise characteristics of the design, the equivalent noise charge (ENC) is considered as it allows for


**FIGURE 14.** Measured response at the fast shaper output.

direct comparison with the number of electrons released in the detector at the input of the CSA.

Most of the noise in a well-designed front-end system has its origins in the detector, the CSA input transistor, or the feedback resistance of the CSA. For a generic front-end electronics channel, and considering a simplified noise model, the ENC is given by:

$$ENC^2 = \frac{1}{C_F^2}\left[\alpha t_p a_p + (C_{DET}+C_G+C_F)^2\left(\frac{\beta}{t_p}a_w + A_F a_f\right)\right] \tag{11}$$

In this expression, $\alpha$ encompasses the noise components corresponding to detector leakage current, detector bias resistance $R_{BIAS}$, and CSA feedback resistance, $R_F$; $a_p$ is the white current noise coefficient, $C_G$ represents the gate capacitance of the CSA input transistor, $\beta$ represents the CSA input transistor thermal noise component, $a_w$ is the white voltage noise coefficient, $A_F$ is the CSA input transistor *1/f* noise coefficient and $a_f$ represents the *1/f* voltage noise coefficient. The coefficients $a_p$, $a_w$, and $a_f$, related to the shaper transmittance function $H(s)$ and the CR-(RC)$^4$ complex filter are, respectively, 0.51, 0.91, and 0.53 [37]. Note that for $M_1$ in strong inversion the $\beta$ coefficient is proportional to $(8 \cdot k \cdot T)/3 \cdot g_{m1}$.

The characteristics of the CSA input transistor $M_1$ are crucial for achieving a good noise performance, thus special care must be taken when choosing its type, size, as well as biasing conditions. Thermal noise in the channel and flicker noise are the dominant noise contributors of $M_1$. Given that a high input pulse rate requires a short peaking time, the thermal noise of the input transistor dominates the total ENC noise of the slow processing path. Furthermore, the 1/f noise coefficient $A_F$ of the pMOS input transistor of the CSA is lower than that of a nMOS transistor. The contribution of the thermal noise is proportional to the value of the total input capacitance $C_T$, and inversely proportional to the square root of the transistor transconductance, $g_{m1}$. Therefore, the thermal noise can be reduced by increasing the input transistor transconductance, while considering low power and low occupied silicon area requirements. In this work the front-end electronics has been

optimized for detector capacitance of 10 pF. An equivalent noise charge of 466 electrons was measured for the slow path comprising a complex shaper.

## VI. CONCLUSION

A single front-end channel built of two different parallel processing paths for silicon detectors readout is presented. The readout channel includes a charge sensitive amplifier, bandpass filters, and a pole-zero cancellation circuit. The system, realized in 180 nm CMOS technology, is capable of both time and amplitude measurement of charge-pulses delivered by semiconductor detectors. A 4th order complex shaper improves the signal to noise ratio and minimizes the ratio of pulse width to peaking time. The amplifier cores have been designed with gain-boosting techniques based on quasi-floating gate transistors providing low noise, accurate amplitude measurements, and good resolution in the input pulse arrival time determination. Using an automatic SET simulation tool, the effect of possible impacts on the QFGs has been studied, proposing a method that allows selecting the design parameters of the QFGs to achieve a circuit resistant to radiation. The system has a large dynamic range and a power consumption of 4.1 mW, even though the single channel is built of two different parallel processing paths.

## REFERENCES

[1] M. Beikahmadi, S. Mirabbasi, and K. Iniewski, "Design and analysis of a low-power readout circuit for CdZnTe detectors in 0.13-$\mu$m CMOS," *IEEE Sensors J.*, vol. 16, no. 4, pp. 903–911, Oct. 2016.

[2] R. J. Aliaga, V. Herrero-Bosch, S. Capra, A. Pullia, J. A. Dueñas, L. Grassi, A. Triossi, C. Domingo-Pardo, R. Gadea, V. González, T. Hüyük, E. Sanchís, A. Gadea, and D. Mengoni, "Conceptual design of the TRACE detector readout using a compact, dead time-less analog memory ASIC," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 800, pp. 34–39, Nov. 2015.

[3] P. Kmon, G. Deptuch, F. Fahim, P. Grybos, P. Maj, R. Szczygiel, and T. Zimmerman, "Active feedback with leakage current compensation for charge sensitive amplifier used in hybrid pixel detector," *IEEE Trans. Nucl. Sci.*, vol. 66, no. 3, pp. 664–673, Mar. 2019.

[4] J. Galán, R. Lóez-Ahumada, T. Sánchez-Rodríguez, A. Torralba, R. G. Carvajal, and I. Martel, "Low voltage power efficient tunable shaper circuit with rail-to-rail output range for the HYDE detector at FAIR," *IEEE Trans. Nucl. Sci.*, vol. 61, no. 2, pp. 844–851, Apr. 2014.

[5] R. Kleczek and P. Kmon, "Comparative analysis of the readout front-end electronics implemented in deep submicron technologies," *J. Instrum.*, vol. 13, no. 11, Nov. 2018, Art. no. C11002.

[6] C. Peña, G. Deptuch, S. Xie, A. Apresyan, L. Narváez, and L. Ristori, "A simulation model of front-end electronics for high-precision timing measurements with low-gain avalanche detectors," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 940, pp. 119–124, Oct. 2019.

[7] F. Liu, Z. Deng, L. He, and Y. Liu, "Development of the full-chain cryogenic readout electronics for the point-contact HPGe detectors," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 947, Dec. 2019, Art. no. 162739.

[8] M. Sanchez-Raya, J. A. Gomez-Galan, E. Cojocaru, M. P. Carrasco, R. J. Naharro, F. M. Chavero, and I. M. Bravo, "Linear tunable analog front-end electronics for silicon charged-particle detectors," *IEEE Trans. Instrum. Meas.*, vol. 64, no. 2, pp. 418–426, Feb. 2015.

[9] H. Hamrita, E. Rauly, Y. Blumenfeld, B. Borderie, M. Chabot, P. Edelbruck, L. Lavergne, J. L. Bris, T. Legou, N. L. Neindre, and A. Richard, "Charge and current-sensitive preamplifiers for pulse shape discrimination techniques with silicon detectors," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 531, no. 3, pp. 607–615, Oct. 2004.

[10] W. M. C. Sansen and Z. Y. Chang, "Limits of low noise performance of detector readout front ends in CMOS technology," *IEEE Trans. Circuits Syst.*, vol. 37, no. 11, pp. 1375–1382, Nov. 1990.

[11] P. Kmon, L. A. Kadlubowski, and P. Kaczmarczyk, "Design of analog pixels front-end active feedback," *J. Instrum.*, vol. 13, no. 1, Jan. 2018, Art. no. P01018.

[12] R. Wang and R. Harjani, "Partial positive feedback for gain enhancement of low-power CMOS OTAs," *Anal. Integr. Circuits Signal Process.*, vol. 8, no. 1, pp. 21–35, 1995.

[13] M. M. Ahmadi, "A new modeling and optimization of gain-boosted cascode amplifier for high-speed and low-voltage applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 3, pp. 169–173, Mar. 2006.

[14] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th ed. New York, NY, USA: Wiley, 2009, pp. 212–214.

[15] J. Beloso-Legarra, C. A. D. L. Cruz-Blas, A. J. López-Martín, and J. Ramirez-Angulo, "Gain-boosted super class AB OTAs based on nested local feedback," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 9, pp. 3562–3573, Sep. 2021.

[16] A. Paul, J. Ramirez-Angulo, A. D. Sanchez, A. J. López-Martín, R. G. Carvajal, and F. X. Li, "Super-gain-boosted AB-AB fully differential Miller op-amp with 156 dB open-loop gain and 174 MV/V MHZ pF/$\mu$W figure of merit in 130 nm CMOS technology," *IEEE Access*, vol. 9, pp. 57603–57617, 2021.

[17] H. D. Rico-Aniles, J. Ramirez-Angulo, J. M. Rocha-Perez, A. J. López-Martín, and R. G. Carvajal, "Low-voltage 0.81 mW, 1–32 CMOS VGA with 5% bandwidth variations and −38 dB DC rejection," *IEEE Access*, vol. 8, pp. 106310–106321, 2020.

[18] J. Ramirez-Angulo, C. A. Urquidi, R. Gonzalez-Carvajal, A. Torralba, and A. López-Martín, "A new family of very low-voltage analog circuits based on quasi-floating-gate transistors," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 50, no. 5, pp. 214–220, May 2003.

[19] F. Márquez, F. Munoz, F. R. Palomo, L. Sanz, E. Lopez-Morillo, M. A. Aguirre, and A. Jiménez, "Automatic single event effects sensitivity analysis of a 13-bit successive approximation ADC," *IEEE Trans. Nucl. Sci.*, vol. 62, no. 4, pp. 1609–1616, Aug. 2015.

[20] P.-Y. Kuo and S.-D. Tsai, "An enhanced scheme of multi-stage amplifier with high-speed high-gain blocks and recycling frequency cascode circuitry to improve gain-bandwidth and slew rate," *IEEE Access*, vol. 7, pp. 130820–130829, 2019.

[21] T. Kishishita, G. Sato, H. Ikeda, T. Takahashi, T. Kiyuna, and Y. Mito, "Low-noise analog ASIC for silicon and CdTe sensors," *IEEE Trans. Nucl. Sci.*, vol. 57, no. 5, pp. 2971–2977, Oct. 2010.

[22] S. Robert, J.-F. Pratte, G. De Geronimo, P. O'Connor, S. Stoll, C. M. Pepin, R. Fontaine, and R. Lecomte, "Design and performance of 0.18-$\mu$m CMOS charge preamplifiers for APD-based PET scanners," in *Proc. IEEE Nucl. Sci. Symp. Conf. Rec.*, vol. 2, Oct. 2003, pp. 1242–1246.

[23] D. Moraes, J. Kaplon, and E. Nygard, "CERN_DxCTA counting mode chip," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 591, no. 1, pp. 167–170, Jun. 2008.

[24] E. Sackinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," *IEEE J. Solid-State Circuits*, vol. 25, pp. 289–297, 1990.

[25] M. H. Liu, H. C. Huang, W. Y. Ou, T. Y. Su, and S. I. Liu, "A low voltage-power 13-bit 16 MSPS CMOS pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 39, no. 5, pp. 834–836, May 2004.

[26] A. Torralba, R. G. Carvajal, J. Ramirez-Angulo, and F. Munoz, "Output stage for low supply voltage, high-performance CMOS current mirrors," *Electron. Lett.*, vol. 38, no. 24, pp. 1528–1529, 2002.

[27] P. Likittanapong, A. Worapishet, and C. Toumazou, "Linear CMOS triode transconductor for low-voltage applications," *Electron. Lett.*, vol. 34, no. 12, pp. 1224–1225, Jun. 1998.

[28] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, NY, USA: McGraw-Hill, 2001, ch. 9, pp. 311–312.

[29] R. R. Harrison and C. A. Cameron, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid State Circuits*, vol. 38, no. 6, pp. 958–964, Jun. 2003.

[30] G. De Geronimo, P. O'Connor, V. Radeka, and B. Yu, "Front-end electronics for imaging detectors," *Nucl. Instrum. Methods Phys. Res. A, Accel. Spectrom. Detect. Assoc. Equip.*, vol. 471, pp. 192–199, Sep. 2001.

[31] S. Ohkawa, M. Yoshizawa, and K. Husimi, "Direct synthesis of the Gaussian filter for nuclear pulse amplifiers," *Nucl. Instrum. Methods*, vol. 138, no. 1, pp. 85–92, Oct. 1976.

[32] G. C. Messenger, "Collection of charge on junction nodes from ion tracks," *IEEE Trans. Nucl. Sci.*, vol. NS-29, no. 6, pp. 2024–2031, Dec. 1982.
[33] G. I. Wirth, M. G. Vieira, and F. G. L. Kastensmidt, "Accurate and computer efficient modelling of single event transients in CMOS circuits," *IET Circuits, Devices Syst.*, vol. 1, no. 2, pp. 137–142, Apr. 2007.
[34] S. Lochner and H. Deppe, "Radiation studies on the UMC 180 nm CMOS process at GSI," in *Proc. Eur. Conf. Radiat. Effects Compon. Syst.*, Brugge, Belgium, Sep. 2009, pp. 614–616, doi: 10.1109/RADECS.2009.5994732.
[35] E. Lopez-Morillo, F. R. Palomo, F. Marquez, and F. Munoz, "Design of a radiation hardened power-ON-reset," *IEEE Trans. Nucl. Sci.*, vol. 65, no. 8, pp. 1943–1950, Aug. 2018.
[36] P. Grybos, "Front-end electronics for multichannel semiconductor detector systems," Editorial Series Accel. Sci., Inst. Electron. Syst., Warsaw Univ. Technol., Warszawa, Poland, 2010.
[37] R. Kleczek and P. Grybos, "FSDR16—Fast and low noise multichannel ASIC with 5th order complex shaping amplifier," *IEEE Trans. Nucl. Sci.*, vol. 60, no. 3, pp. 2188–2195, Jun. 2013.

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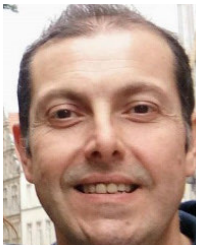

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