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Alternative Methods for Non-Linearity Estimation in High-Resolution Analog-to-Digital Converters

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Alternative Methods for Non-Linearity Estimation in High-Resolution Analog-to-Digital Converters

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Abstract

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Resumen

La medida de la característica de linealidad de un convertidor analógicodigital (ADC) de alta resolución mediante el método estándar del Histograma constituye un gran desafío debido los requisitos de alta pureza de la señal de entrada y del elevado número de datos de salida que deben adquirirse para obtener una precisión aceptable en la estimación. Estos requisitos encuentran importantes inconvenientes para su aplicación cuando las medidas deben realizarse dentro de largos flujos de pruebas, múltiples veces y en un gran número de piezas, y todo bajo un entorno industrial que busca reducir costes y plazos de entrega como es el caso del sector del Nuevo Espacio. Esta tesis introduce dos métodos alternativos que consiguen relajar los dos requisitos anteriores para la estimación de los parámetros de no linealidad en los ADCs. Los métodos se han evaluado estimando el patrón de No Linealidad Integral (INL) mediante simulación utilizando modelos realistas de ADC de alta resolución y experimentalmente aplicándolos en ADCs reales.

Inicialmente se analiza el reto que supone la aplicación del método estándar del Histograma para la evaluación de los parámetros estáticos en ADCs de alta resolución y cómo sus inconvenientes se acentúan en la industria del Nuevo Espacio, siendo un método altamente costoso para un entorno industrial donde se exige la reducción de costes y plazos de entrega. Se estudian métodos alternativos al Histograma estándar para la estimación de la No Linealidad Integral en ADCs de alta resolución. Como el número de trabajos es muy amplio y abordarlos todos es ya en sí un desafío, se han incluido aquellos más relevantes para el desarrollo de esta tesis. Se analizan especialmente los métodos basados en el procesamiento espectral para reducir el número de datos que necesitan ser adquiridos y los métodos basados en un doble histograma para poder utilizar generadores que no cumplen el requisito de precisión frente al ADC a medir.

En este trabajo se presentan dos novedosas aportaciones para la estimación de la No Linealidad Integral en ADCs, como posibles alternativas al método estándar del Histograma. El primer método, denominado SSA (Simple Spectral Approach), busca reducir el número de datos de salida que es necesario adquirir y se centra en la estimación de la INL mediante un algoritmo basado en el procesamiento del espectro de la señal de salida cuando se utiliza un estímulo de entrada sinusoidal. Este tipo de enfoque requiere un número mucho menor de muestras que el método estándar del Histograma, aunque la precisión de la estimación dependerá de lo suave o abrupto que sea el patrón de no-linealidad del ADC a medir. En general, este algoritmo no puede utilizarse para realizar una calibración del error de no linealidad del ADC, pero puede aplicarse para averiguar entre qué límites se encuentra y cuál es su forma aproximada. El segundo método, denominado SDH (Simplified Double Histogram) tiene como objetivo estimar la no linealidad del ADC utilizando un generador de baja pureza. El algoritmo utiliza dos histogramas, construidos a partir de dos conjuntos de datos de salida en respuesta a dos señales de entrada idénticas, excepto por un desplazamiento constante entre ellas. Utilizando un modelo simple de sumador, un enfoque ampliado denominado ESDH (Extended Simplified Double Histogram) aborda y corrige las posibles derivas temporales durante las dos adquisiciones de datos, de modo que puede aplicarse con éxito en un entorno de prueba no estacionario. De acuerdo con los resultados experimentales obtenidos, el algoritmo propuesto alcanza una alta precisión de estimación.

Ambas contribuciones han sido probadas en ADCs de alta resolución con experimentos tanto simulados como reales en laboratorio, estos últimos utilizando un ADC comercial con una resolución de 14 bits y una tasa de muestreo de 65Msps (AD6644 de Analog Devices).

Abstract

The evaluation of the linearity performance of a high resolution Analog-to-Digital Converter (ADC) by the Standard Histogram method is an outstanding challenge due to the requirement of high purity of the input signal and the high number of output data that must be acquired to obtain an acceptable accuracy on the estimation. These requirements become major application drawbacks when the measures have to be performed multiple times within long test flows and for many parts, and under an industrial environment that seeks to reduce costs and lead times as is the case in the New Space sector. This thesis introduces two alternative methods that succeed in relaxing the two previous requirements for the estimation of the Integral Nonlinearity (INL) parameter in ADCs. The methods have been evaluated by estimating the Integral Non-Linearity pattern by simulation using realistic high-resolution ADC models and experimentally by applying them to real high performance ADCs.

First, the challenge of applying the Standard Histogram method for the evaluation of static parameters in high resolution ADCs and how the drawbacks are accentuated in the New Space industry is analysed, being a highly expensive method for an industrial environment where cost and lead time reduction is demanded. Several alternative methods to the Standard Histogram for estimating Integral Nonlinearity in high resolution ADCs are reviewed and studied. As the number of existing works in the literature is very large and addressing all of them is a challenge in itself, only those most relevant to the development of this thesis have been included. Methods based on spectral processing to reduce the number of data acquired for the linearity test and methods based on a double histogram to be able to use generators that do not meet the the purity requirement against the ADC to be tested are further analysed.

Two novel contributions are presented in this work for the estimation of the Integral Nonlinearity in ADCs, as possible alternatives to the Standard Histogram method. The first method, referred to as SSA (Simple Spectral Approach), seeks to reduce the number of output data that need to be acquired and focuses on INL estimation using an algorithm based on processing the spectrum of the output signal when a sinusoidal input stimulus is used. This type of approach requires a much smaller number of samples than the Standard Histogram method, although the estimation accuracy will depend on how smooth or abrupt the ADC nonlinearity pattern is. In general, this algorithm cannot be used to perform a calibration of the ADC nonlinearity error, but it can be applied to find out between which limits it lies and what its approximate shape is. The second method, named SDH (Simplified Double Histogram)aims to estimate the Non-Linearity of the ADC using a poor linearity generator. The approach uses two histograms constructed from the two set of output data in response to two identical input signals except for a dc offset between them. Using a simple adder model, an extended approach named ESDH (Extended Simplified Double Histogram) addresses and corrects for possible time drifts during the two data acquisitions, so that it can be successfully applied in a non-stationary test environment. According to the experimental results obtained, the proposed algorithm achieves high estimation accuracy.

Both contributions have been successfully tested in high-resolution ADCs with both simulated and real laboratory experiments, the latter using a commercial ADC with 14-bit resolution and 65Msps sampling rate (AD6644 from Analog Devices).

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Contents

Ał	Abstract iii			
Acknowledgements vi				vii
1	Intro	oductio	on	1
	1.1	Motiv	ation	1
	1.2	Struct	ure and contents of the dissertation	3
	1.3	Appli	cation of the Standard Histogram Method in high reso-	
		lution	Analog-to-Digital converters	5
		1.3.1	Drawbacks of the application of the Standard Histogram	
			Method in the high resolution ADCs industrial testing	8
			ADCs COTS Qualification for New Space	10
	1.4	Alterr	native methods to the Standard Histogram Method	16
		1.4.1	Alternative Integral Non-Linearity estimation using the	
			spectral approach	17
		1.4.2	Integral Non-Linearity estimation using double histogram	n
			based methods	22
		1.4.3	Other INL estimation techniques	30
2	INL	estima	tion using a Spectral Processing based method	33
	2.1	Introd	luction	33
	2.2	A Sim	ple Spectral Approach to estimate the INL in ADCs: SSA	
		metho	od	34
		2.2.1	A proposal for modelling the Integral Non-Linearity	35
		2.2.2	Inclusion of the Integral Non-Linearity model in the	
			spectral approach	40
		2.2.3	Method for spectral processing and calculation of spec-	
			tral parameters	45
			Estimation of the harmonic parameters under a coher-	
			ence sampling test	46
			Estimation of the harmonic parameters under a non-	
			coherence sampling test	48

		2.2.4	Simulated experiments	49
			Experiment 1: ADC_1 under a low-density DC sweep .	50
			Experiment 2: ADC_1 under a sine-wave input	52
			Experiment 3: ADC_2 under a sine-wave input	57
		2.2.5	Application of the method to a real ADC Pipeline	62
3	INL	estima	ation based on the Double Histogram method	65
	3.1	Introc	luction	65
	3.2	A pro	posal for the Non-Linearity estimation based on the Dou-	
		ble Hi	istogram method	66
		3.2.1	Adaptation to a non-stationary test environment	71
		3.2.2	Proposal for the histogram normalisation and the eval- uation of the two set of virtual transition levels in Dou-	
			ble Histogram methods	73
		3.2.3	Enhanced DH method: Application of the generalised Double Histogram model under a non-stationary test	
			environment by obtaining the non-intearity 1 of the	70
	2.2	A Circ	non-linear generator	70
	5.5	A 5111	SDU A Simplified algorithm based on the Double Histogram method	00
		5.5.1	togram method applied on a stationary set up	80
		3.3.2	Extended SDH method: Generalisation of the SDH metho	ou od
			in a non-stationary test environment	87
		3.3.3	Simulated Experiments	92
			Experiment 1: Application of SDH method under a sta-	
			tionary test environment	92
			Simulated Experiment 2: Application of ESDH under a	
			non-stationary test environment	98
			Experiment 3: Application of the Enhanced DH method	
			under a non-stationary test environment	103
4	Exp	erimen	tal application of the proposed methods on a commercia	1
	higl	n-resol	ution Analog-to-Digital Converter	107
	4.1	Descr	iption of the measurement set-up	109
	4.2	Descr	iption of the experiment test flow	111
	4.3	Stand	ard Histogram test settings	112
			Coherent Sampling Compliance	113
			Amplitude setting	115

			Setting of the number of samples per record and the	
			number of records	115
	4.4	Evaluation of the INL reference pattern using the TTE high		
		qualit	y band-pass filter: Pure Sine input signal	117
	4.5	Estima	ation of the INL pattern using the SSA method: Pure Sine	
		input	signal	121
	4.6	Estima	ation of the INL using methods based on the DH: Non-	
	1.0	pure input signals		
		461	Estimation of the INIL pattern using the LPB-15 low-	120
		1.0.1	pass filter: Non-pure sine input signal	126
		162	Estimation of the INI pattern using the I PB 5 low pass	120
		4.0.2	filter: Non pure triangular input signal	122
				155
5	Con	onclusions and Future Work 13		
	5.1	Concl	usions	139
	5.2	Future	e Work	143
Α	Eval	valuation of the static parameters of an ADC by the Standard His-		
	togr	gram Method 14		
	A.1	An ov	erview of the ADC static parameters	145
		A.1.1	INL corrected for gain and offset contributions	147
	A.2	The St	andard Histogram Method	149
B	Stin	uulus F	rror Identification and Removal: SFIR method	153
D	R 1	Intogr	al Non-Linearity definition	153
	D.1	R 1 1	Input signal poplingarity modeling	155
		D.1.1	Input Signal Hormiteanty modeling	154
		D.1.2	Integral Non-Linearity evaluation	155
	В.2	IINL es	stimation using two nonlinear stimuli	157
Bi	bliog	raphy		161

List of Figures

1.1	Transfer function of a 3-bit ADC	6
1.2	A scheme of a typical test flow for COTS based on ECSS-Q-ST-	
	60-13C	12
1.3	Standard Histogram method drawbacks and alternative meth-	
	ods	16
1.4	Test procedure using a spectral processing method	18
1.5	Test protocols using SSA method	21
1.6	Test procedure using the DH method	23
2.1	SSA theoretical deduction flow	34
2.2	N-bit ADC transfer function	36
2.3	Low density sampling	37
2.4	High-order and Low-order transfer function approximation .	38
2.5	First-order Taylor series	39
2.6	Spectrums	41
2.7	Visual relations between τ_k and l_k	43
2.8	Estimated INL and error by the transfer function approxima-	
	tion in a low-sampling test	51
2.9	Typical spectrum for ADC_1	53
2.10	ADC_1 estimated INL and error using the SSA method	55
2.11	Histogram estimation using 4 records of 4096 samples for ADC_1	56
2.12	Typical spectrum for ADC_2	57
2.13	ADC ₂ INL pattern estimated by SSA method and including	
	gain effect	58
2.14	ADC_2 INL pattern estimated by SSA method $\ldots \ldots \ldots$	59
2.15	SSA application using 2 records of 32768 samples for ADC_2 .	61
2.16	Histogram estimation using 2 records of 32768 samples for ADC_2	62
2.17	Prototype ADC: Spectrum for SSA method application	63
2.18	Prototype ADC: INL estimated by the Standard Histogram	
	method and by the SSA method	63
3.1	Non-Linear AWG model	67

3.2	Global ADC model	68
3.3	Actual and Estimated Transfer Curves	69
3.4	Doble Histogram method Set-up	70
3.5	Two Virtual Transition levels sets	70
3.6	Non-stationary Non-Lineal AWG model	72
3.7	Adopted INL pattern	78
3.8	SDH theoretical deduction flow	81
3.9	Geometrical relationships in SDH	82
3.10	Derivatives from the Finite difference approximation	84
3.11	ESDH theoretical deduction flow	87
3.12	Geometrical relationships in ESDH	88
3.13	Simulated Experiment 1 input signal	94
3.14	Simulated Experiment 1: INL estimated by the Standard His-	
	togram method	95
3.15	Simulated Experiment 1: Results estimated by the SDH	96
3.16	Simulated Experiment 1: RMS error evolution	97
3.17	Simulated Experiment 2: Gain and offset evolution	100
3.18	Simulated Experiment 2: Resuls comparinson between SDH,	
	ESDH and interleaved SDH methods	101
3.19	Simulated Experiment 2: Thue-Morse series	103
3.20	Simulated Experiment 3: Gain and offset evolution	105
3.21	Simulated Experiment 3: Resuls comparinson between DH	
	and EDH	106
4.1	AD6644: Picture of the Evaluation Board	107
4.2	AD6644: Measurement set-up	109
4.3	AD6644: Measurement set-up for the INL reference pattern	117
4.4	AD6644: Picture of the set-up for the INL reference pattern	
	evaluation	117
4.5	AD6644: Output data spectrum from the pure sinusoidal input	
	signal	118
4.6	Number of Records versus Noise	119
4.7	AD6644 INL and DNL reference pattern	120
4.8	AD6644: Measurement set-up for the INL estimation by the	
	SSA method	121
4.9	AD6644: Output data spectrum from the pure sinusoidal input	
	signal	122
4.10	AD6644: Output data spectrum from the pure sinusoidal input	
	signal	123

4.11	AD6644: Estimated INL from the SSA method	124
4.12	AD6644: Estimated INL from the SSA method and the his-	
	togram method using 32686 samples	124
4.13	AD6644: Set-up for the SDH, Extended SDH and Enhanced	
	DH methods using a non-pure sine-wave input	127
4.14	AD6644: Picture of the set-up for the SDH, Extended SDH and	
	Enhanced DH methods using a non-pure sine-wave input	127
4.15	AD6644 output data spectrum from the non-pure sinusoidal	
	input signal	128
4.16	Evaluation of the system noise by DC histograms	128
4.17	Offset evolution in SDH method	129
4.18	AD6644: Thue-Morse SDH method offset evolution	130
4.19	AD6644: Non-pure sinusoidal INL patterns	131
4.20	AD6644: INL patterns from SDH and Morse DH methods us-	
	ing a sinusoidal input signal	132
4.21	AD6644: INL patterns from ESDH and EDH methods	132
4.22	AD6644: Set-up for the SDH, Extended SDH and Enhanced	
	DH methods using a non-pure triangular-wave input	133
4.23	AD6644: Raw output data from the non-pure triangular input	
	signal	134
4.24	AD6644: Equivalent-time output data from the non-pure tri-	
	angular input signal	134
4.25	AD6644: Non-pure triangular INL patterns	136
4.26	AD6644: INL patterns from SDH and Morse DH methods us-	
	ing a triangular input signal	137
4.27	AD6644: INL patterns from ESDH and EDH methods using a	
	triangular signal	137

List of Tables

2.1	In order of harmonic magnitude, first six amplitudes and phases	
	estimated from the ADC_1 output data spectrum $\ldots \ldots$	54
3.1	Relations between signal waveform and its amplitude cumu-	
	lative probability distribution	73

List of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converters
ATE	Automatic Test Equipment
AWG	Arbitrary Waveform Generator
BIST	Built In Self Test
BP	Band Pass filter
COTS	Commercial Off The Shelf
DC	Direct Current
DH	Double Histogram
DFT	Discrete Fourier Transform
DNL	Differential Non Linearity
ECSS	European Cooperation for Space Standardization
EEE	Electrical Electronic Electromechanical
ENOB	Effective Number Of Bits
ESA	European Space Agency
ESDH	Extended Simplified Double Histogram
ESCC	European Space Components Coordination
FERARI	Fundamental Identification and Replacement
FFT	Fast Fourier Transform
FIRE	Fundamental EstimationRemoval And Residue Interpolation
FOM	Figure Of Merit
GCF	Greatest Common Factor
GE	Gain Error
HCF	High Code Frequency component
INL	Integral Non Linearity
LCF	Low Code Frequency component
LP	Low Pass filter
LS	Least Squares method
LSB	Least Significant Bit
NASA	National Aeronautics and Space Administration
OFFE	OFFset Error
RMS	Root Mean Square
RVT	Radiation Verification Test
SDH	Simplified Double Histogram
SEIR	Stimulus Error Identification and Removal
SSA	Simple Spectral Algorithm
THD	Total Harmonic Distortion

TID Total Ionizing Dose

To my family

Chapter 1

Introduction

1.1 Motivation

In this decade, more than 9,000 new satellites are expected to be launched. New Space missions such as constellations or nano and small satellites are growing significantly in recent years. New Space is a commercial space sector for the development of satellite communication solutions far away from the classic concept of satellites in geostationary orbit. Some constellations already have their own name, such as *Oneweb*, *Starlink* or *Kuiper*. The sector is continuously requiring higher performance systems while at the same time demanding lower overall costs. For this reason, there is currently an emerging demand for solutions that allow for fast, high volume supply and easy qualification and adaptation of Electrical, Electronic and Electromechanical (EEE) parts to achieve the maximum technological performance. As a consequence, the trend towards the use of Commercial-of-the Shelf (COTS) devices is strongly growing, but because of their target market, in their origin they do not require the levels of confidence and reliability that space systems ask, leading to their having to be subjected to extensive and time consuming adhoc qualification schemes, (European Cooperation For Space Standardization, 2013). Since time and cost are key elements in everything surrounding megaconstellations and New Space, the sector is demanding for new testing approachs as alternative to the standard techniques traditionally used.

One of the most demanded COTS devices is the Analogue-to-Digital Converter (ADC), a key and ever-present device as part of the mixed-signal systems, as it is the communication bridge between the analog and the digital world. The linearity test of an ADC is of great importance to guarantee the functionality of the device in a given application (Linnenbrink et al., 2006), being the Integral Non Linearity (INL) parameter one of the most demanded specifications to be measured by the space industry when qualifying these components. The Standard Histogram method is the traditional method used by the industry to perform the linearity test on an ADC. As technology progresses and the digital domain increases in performance, higher resolution ADCs are required. The application of the histogram method in high resolution ADCs is very expensive and cost time consuming due to the high linearity requirements of the excitation signal generators and the long test times caused by the need to acquire a large number of data.

In this context, the present thesis project aims to develop alternative lowcost methods to the traditional histogram method for the estimation of the Integral Nonlinearity in high resolution ADCs, for future application in the space industry. The alternative methods focus on relaxing the linearity requirement of the test input signal generator and relaxing the requirement of a high density data acquisition. The work has been executed within the framework of *Finantial support for the trainning of PhDs in companies :Industrial Doctorates* of the "Ministerio de Ciencias, Innovación y Universidades" of the Government of Spain and under the project: *Definición de técnicas de ensayo de bajo coste de conertidores analógicos-digitales* with Reference DI-16-08912 assigned to ALTER TECHNOLOGY TUV NORD company.

1.2 Structure and contents of the dissertation

The dissertation is divided into five chapters and the appendices. Chapter 1 is the introduction to the work developed in the thesis, where the challenge of applying the Standard Histogram method for the evaluation of static parameters in high resolution ADCs is exposed. It is analysed how the drawbacks of its application in high resolution ADCs are accentuated in the New Space industry, and makes it an unsuitable and highly costly test method for an industrial environment where the reduction in costs and delivery times is demanded. This chapter also introduces alternative methods to the Standard Histogram to estimate the Integral Non-Linearity in high resolution ADCs, devised to relax the requirements of purity of the test input signal or the high number of samples that have to be acquired for its application. The bibliography presented is especially focused on methods based on spectral processing to reduce the number of data acquired for the linearity test and on methods based on a double histogram to be able use generators that do not meet the linearity requirement against the ADC to be tested.

Chapter 2 and Chapter 3 are the core of the dissertation. They present two novel methods developed during this research work for the estimation of the Integral Non-Linearity in ADCs, as possible alternatives to the Standard Histogram method. Both chapters follow the same structure to describe the work developed: a summary of the existing literature on the subject, our contribution with the algorithms previously discussed, the mathematical formulation of our proposal and its implementation to obtain a estimate of the Integral Non-Linearity and the simulation results.

Chapter 2 focuses on the estimation of the INL using an algorithm based on the processing of the output signal spectrum when a sinusoidal input stimulus is used. This type of approach requires a much smaller number of samples than the Standard Histogram method, although its estimation accuracy will depend on how smooth or abrupt the Integral Non-Linearity pattern of the ADC is. This algorithm cannot be used to perform a calibration of the nonlinearity errors of the ADC, but it can be used to know between which limits it lies and what its approximate shape is.

The algorithms described in Chapter 3 aim to estimate the Integral Non-Linearity of the ADC using a poor linearity generator. The approaches use a double histogram, constructed from the two set of output data in response to two identical input signals except for a DC offset between them. Using a simple adder model, our approach addresses and corrects for possible time drifts during the two data acquisitions, so that it can be successfully applied in a non-stationary test environment. According to the experimental results obtained, the proposed algorithm achieves high estimation accuracy.

Chapter 4 describes the experiments carried out at the laboratory to apply the proposed methods in Chapter 2 and Chapter 3 for the estimation of the INL of a high-performance commercial ADC: AD6644 from Ananlog Devices. The chapter details how to perform a linearity test for ADCs according to the Standard Histogram method, a non-trivial task. The structure of the chapter is as follows: obtaining the reference INL by applying the Standard Histogram method, estimating the INL by the alternative methods proposed and comparing them with the reference INL. The experimental results obtained evidence the successful application of the different methods proposed as an alternative to the Standard Histogram according to the objectives to be achieved, emphasising that the device under test is a high-resolution (14 bits) and high-speed (65 Msps) ADC.

Chapter 5 includes the Conclusions and Future Work. The appendices are divided into: Appendix (A) where a review of the static parameters of the ADC and their evaluation using the histogram method is provided and Appendix (B) where a description of the SEIR method is presented.

1.3 Application of the Standard Histogram Method in high resolution Analog-to-Digital converters

The Standard Histogram method (Measurement and Technical, 2011; Linnenbrink et al., 2006) is one of the methods used to estimate the transition levels of an ADC and to evaluate the static parameters that characterise its transfer function. An overview of the static parameters and how to perform the histogram method is described in Appendix(A). The work presented in this thesis is focused on the evaluation of the static parameter Integral Non Linearity (INL), which measures the deviation of the real transition levels of the tested actual ADC, hereafter designated as the set { t_k }, with respect to the ideal transition levels of the ideal ADC, hereafter designed as the set { l_k }. Its mathematical expression is:

$$INL_k = \frac{t_k - l_k}{q}, \quad \forall k \in [z_{min} + 1, z_{max}]$$
(1.1)

where *q* is the quantum or LSB (Least Significant Bit) of the ideal ADC, t_k and l_k are the transition levels where the output changes from code k - 1 to code *k* in the actual ADC and the ideal ADC respectively, z_{min} is the minimum code or lower saturating code and z_{max} is the maximum code or upper saturating code of the actual ADC. Equation (1.1) is expressed in quantum or LSB units. Figure 1.1 shows in blue line a hypothetical transfer function of a 3-bit ADC and in black line the transfer function of its associated ideal ADC. The analog input domain is bipolar in [-R, R] and the ideal quantum is $q = 2 \cdot R/2^3$. As an example, in the figure the INL error of the code k = 2 and Differential Non linearity (DNL) error of the code k = 4 are represented. The DNL measures how much the width of each code of the actual ADC, w_k , deviates from the quantum or LSB of the ideal ADC, in LSB units:

$$DNL_{k} = \frac{w_{k} - q}{q} = \frac{t_{k+1} - t_{k}}{q} - 1 = INL_{k+1} - INL_{k}, \quad \forall k \in [z_{min} + 1, z_{max} - 1]$$
(1.2)

By definition, the set $\{INL_k\}$ is affected by the offset and gain errors introduced by the test input signal and the ADC. In the work presented in this





FIGURE 1.1: Transfer function of a 3-bit ADC showing the INL and DNL error parameters

thesis the final objective is to obtain a INL pattern of the ADC under test corrected for these offset and gain contributions.

In order to evaluate the transition levels of the ADC under test, the Standard Histogram method performs a statistical procedure based on the construction of the histogram of the output codes of the ADC, in response to an input signal with a given waveform whose statistical distribution is known. On the one hand, the probability of occurrence of each output code is obtained from the histogram of the output codes. On the other hand, the probability distribution that the ADC output will follow is known, which is a function of the transition levels and the input parameters. From this information the transition levels are obtained.

Advantages of the Standard Histogram method:

• It achieves high accuracy regardless of the shape of the transfer function of the ADC.

• For its application, any signal waveform with a known amplitude probability distribution can be used as an input signal to test the ADC.

Requirements for the Standard Histogram method application (Measurement and Technical, 2011):

- Purity of the input signal to the ADC: nolinearities in the input signal result in errors in the estimation of transition levels. An input signal at least 3 bits higher than the expected accuracy of the ADC under test is required.
- Number of samples versus accuracy: there is a dependence between the accuracy of the obtained ADC transfer function and the number of output codes or samples computed by the histogram: the larger the number, the lower the uncertainty. To achive a given confidence, the number of samples per code that must be computed by the histogram depends on the noise level of the input signal and the ADC under test. As the standard (Measurement and Technical, 2011) indicates, the uncertainty in LSB units in the estimate of a transition level due to noise is approximated by:

$$\varepsilon \approx \sqrt{\frac{\sigma}{H}}$$
 (1.3)

Where σ is the standard deviation of the noise in LSB units and *H* is the average number of histogram samples adquired in each of the code bins that share the given transition level. Since for a N-bit resolution ADC the number of different codes is 2^N , the number of samples required to performed the Standard Histogram method with a certain accuracy increases as a power of two with the resolution *N* of the ADC under test.

Synchronisation between the input signal and the ADC sampling frequency. The input signal should be generated in synchronisation with the sampling clock. Since the histogram method is based on estimating the transition levels from the probability of occurrence of each code according to the ADC excitation signal, it is important that this probability is not altered because some codes are more excited than others due to a non-uniform distribution of data caused by poor synchronisation, giving them a different probability to the one that corresponds to them according to the input signal waveform.

In a periodical wave testing, the ratio between the input frequency, f_0 , and the sampling frequency, f_s , must be such that there must be an integer number of cycles, J, in the acquired data record and that number of cycles must be relatively prime to the number M of samples in the record. Mathematically it means that J and M do not have common factors, that is the Greatest Common Factor is equal one: GCF(J, M) = 1. This guarantees that the samples in each record are uniformly distributed in phase from 0 to 2π . An input frequency that meets the above is the one that follows the expression:

$$f_0 = f_s \frac{J}{M} \tag{1.4}$$

with J an odd integer and M a power of 2.

1.3.1 Drawbacks of the application of the Standard Histogram Method in the high resolution ADCs industrial testing

The requirements of applying the Standard Histogram method to high-resolution ADCs entails a high cost in terms of expensive measurement instrumentations, as well as high time cost in terms of measurement setup design and data acquisition:

1. The requirement to use a more linear input signal than the ADC under test implies the need to be generated by high linearity generators or Arbitrary Wave Generators (AWGs). For example, to evaluate the INL pattern of a 16-bit effective resolution ADC, an AWG of at least 19-bit resolution is required. As technology advances and ADCs increase in resolution, meeting the requirement for linearity of the estimulus signal is a great challenge and one of the factors that increase the cost of test. In an industrial test environment, the use of expensive Automated Test Equipments (ATEs) suitable for mixed-signal testing facilitates the process of measuring the performance of ADCs, integrating high-performance AWGs, precise clock generators, control and data acquisition systems into its instrumentation, and allowing via these instrumentations a full synchronisation between signal generation, sampling of the ADC under test and data capture. High linearity AWG generators use as important elements Digital to Analog Converters (DACs) structures to achieve the required high resolution, usually at the expense of other performance factors such as speed, stability or signal

settling: (1) The frequency limitations of the AWG can make it difficult to achieve this full synchronisation between the generated signal, its sampling and the capture of the output data. (2) If the application of the Standard Histogram method requires the acquisition of a large number of output samples, the input signal to the ADC under test has to remain stationary during data capture, thus requiring the use of very low time drift generators. A solution is taking several records of fewer output samples and construsct the histogram with them, but the test time could be increased by waiting times between the data records acquired. Waiting times may be due to the uniform sampling observance of the Standard Histogram method or due to the capture system itself.(3) Long settling times on the input signal increase the test run time and therefore test time cost.

The implementation of the Standard Histogram method using a sinusoidal input signal to the ADC under test is widespread because it is possible to purify or linearise the signal by applying a filter in the path signal. Obviously, the degree of linearity achieved will depend on the type of filtering (low pass filter or band pass filter), the frequency and bandwidth of the filter and the quality (distortion introduced, frequency selectivity...) of the filter. For high resolution ADCs, the introduction of high quality filters is a new constraint, as it is necessary to resort to expensive custom-made high quality bandpass filters specially manufactured for a given frequency and so increasing the test cost.

Another source of cost-increase in industrial test comes from the fact that the fast advance in technology makes generators obsolete in a few years for the test of the State-of-the-art ADCs, requiring constant investment in new expensive generators or expensive ATEs. In fact, future test instrumentation will be powered by the new generation of mixedsignal components, so that progress in measurement instrumentation will lag behind the progress of the new generation to be measured.

2. The requirement on the number of samples acquired for a desired accuracy under a test system noise level can lead in high resolution ADCs to the need to capture a very large number of samples, strongly increasing the test time cost. For example, in a sine waveform testing that meets (1.4), for an ideal ADC and in absence of random noise, the minimum

number of adquired data that ensures a sample of every code bin is $M = \pi \cdot 2^N$ (Measurement and Technical, 2011). Assuming a 16-bit ADC and a noise standard deviation of 1LSB, according to (1.3) if 10 samples per code bin are acquired, the uncertainty due to noise will be about 0.32LSB. 10 samples per code bin implies a minimum number of samples of $10 \cdot \pi \cdot 2^N \approx 2.058.874$, being $M = 2^{21} = 2.097.152$ the closest power of 2 number of samples.

Capturing a data record with a very large number of samples implies some drawbacks as: (1) As discussed above, a very low time drift generator is needed, so that the input signal to the ADC remains stationary during data capture. The longer the data record, the longer it will take the record adquisition and the greater time drift errors. (2) For sinusoidal signals testing, with larger number of samples per record higher accuracy will be required of the signal frequency (Measurement and Technical, 2011). (3) Possible limitations due to the memory of the capture system. The solution is to take several records under the same conditions with a smaller number of samples, and construct the histogram with all of them. This will increase time test, due to the input signal settling time, the adaptation of the capture system for the acquisition of the next record (e.g. resetting the data memory) and the uniformity in the distribution of the acquired samples, that has to be fulfilled when integrating all records. In a sine wave testing, the records have to be evenly phase distributed between 0 and 2π .

ADCs COTS Qualification for New Space

New Space is a private initiative area of space industry driven mostly for commercial purposes, a fact that is leading to the evolution of the space industry towards a new model that is different from the traditional one. High costs due to custom-made designs and long development times are being replaced by much lower costs and time solutions, while maintaining high performance requirements. One of the sectors most affected by the New Space approach is that of communication satellites, where the start-up of medium and low orbit megaconstellations such as *Oneweb* or *Starlink* is already a reality.

One of the solutions to reduce costs and lead times is the use of commercial components that meet the design and performance requirements. These are the so-called Commercial-of-the Shelf (COTS) devices. The use of COTS in space systems provides for rapid and high volume procurement of components that meet design performance requirements. But COTS are devices that were not designed and manufactured for use in space flight. For this reason they have to be subjected to a series of tests to qualify them for safe use in the conditions of the Space environment which, for example, will cause large temperature fluctuations in the in-flight systems as well as their exposure to space radiation. Evidence of the space industry's growing commitment to the use of COTS is the increasing acceptance of conferences papers where their qualification results are presented (Jalon-Victori, Carranza-Gonzalez, and Ricca-Soaje, 2021; Vargas-sierra et al., 2018), and even the recent emergence of workshops where they are exclusively addressed, such as ACCEDE (ESA, Alter Technology, 2019), supported by the European Space Agengy (ESA) and companies of the sector such as Alter Technology company. Tests to evaluate and qualify the use of COTS in Space can be performed, for example, in accordance with ECSS-Q-ST-60-13C (from the European Space Agency ESA) (European Cooperation For Space Standardization, 2013) or EEE-INST-002 (from the National Aeronautics and Space Administration NASA) (Sahu, Leidecker, and Lakins, 2003), which should be used in conjunction with PEM-INST-001 (Lakins, 2003) for additional and specific product assurance requirements for plastic components. These standards are guidelines that can be tailored to each part and mission. Focusing on the European guide, the Standard ECSS-Q-ST-60-13C is the European Cooperation for Space Standardization (ECSS) standard intended to the commercial Electrical, Electronic and Electromechanical (EEE) components management, engineering and product assurance in space projects and applications. The standard indicates three levels of components classification based on a tradeoff between assurance and risk. Class 1 is the highest assurance and lowest risk and Class 3 is the lowest assurance and highest risk.

Another possible adaptation required by COTS for use in space applications is the re-tinning of their leads. The commercial components comply with the RoHS hazardous substances regulation, so the use of lead (Pb) in manufacturing is limited, leaving essentially pure tin (Sn) plating. Tin whiskers are microscopic metal conductive fibers that may cause electrical short-circuits and grow spontaneously from pure-tinned surfaces (Galyon,



FIGURE 1.2: A scheme of a possible test flow for COTS based on ECSS-Q-ST-60-13C

2004). In order to mitigate the growth of these whiskers, a risk mitigation plan shall be released. One mitigation strategy is, if possible, the re-tinning of the COTS leads using a tin-lead alloy.

Let's focus on tests involving electrical measurements. If, for example, a commercial component wants to be classified as Class 1, Evaluation and Screening test flows are established customised for part and mission (Alter Technology, 2021). Figure 1.2 shows a possible test flow based on the ECSS-Q-ST-60-13C standard. In the hypothetical test chart depicted, all parts except those to be subjected to the RVT Evaluation have been re-tinned. The Evaluation and Screening flows require electrical measurements at three temperatures: at room temperature of 25°C and at a maximum and minimum temperature depending on the manufacturer and the future space application. Each includes environmental testing, where the electrical measurements are performed before, after and even in between specific tests regulated by the bias device configuration, the test environment temperature and the time required for the test execution. The screening flow is performed on 100% of the parts in the lot, which in some cases may consist of hundreds of samples. These test flows also include the Radiation Verification Test (RVT), with Total Ionizing Dose (TID) being one of the tests to be performed. The European Space Components Coordination (ESCC) Basic Specification 22900 (European Space Agency, 2016) defines the basic requirements applicable to the steady-state irradiation testing of integrated circuits and discrete semiconductors suitable for space applications. Apart from the initial and the final electrical measurements at the test, the total ionizing dose is reached by at
least three intermediate exposure steps that require control electrical measurements, to evaluate the response of the component to the accumulated irradiation dose up to that moment. These measurements have the drawback that they must be performed within two hours, since a maximum of two hours between consecutive irradiation exposures is allowed so that the component does not initiate a recovery.

In general, the electrical measurements of a COTS are compared with the ranges of possible values of the measured parameter which have been established by the manufacturers and indicated in the datasheet of the component. This may establish a pass/fail criterion. In general, the parameter electrical measurement test conditions are also set by the conditions indicated in the manufacturer's datasheet, although they may also be customised to the demands of the design in which it will be integrated.

Assuming that the COTS to be qualified for space application are highresolution commercial ADCs whose parameter to be measured is INL. ADCs are key parts in systems developed for space applications and need the highest assurance and lowest risk standarization requirements, so they are usually test under Class 1 classification. Suppose, for example, that a batch of 100 pieces is screened. Screening involves performing an environmental test with initial electrical measurements at room temperature and final measurements at room temperature, high temperature and low temperature, that is, the INL has been measured four times for each part. In other words, the screening part of the batch alone would involve applying the Standard Histogram method 400 times. According to the above qualification schemes, the application of the Standard Histogram method is a handicap to meet the low cost and time considerations targeted by the New Space. Consequently, alternative test solutions are needed to enable fast and low-cost test procedures in line with the demands of this sector of the space industry:

1. Signal generator linearity requirements. In view of the drawback explained in section 1.3.1 about this issue, for the measurement of a specific ADC, the relaxation of the linearity requirement of the signal generator increases the number of generators available to perform the linearity test. This allows a faster adaptation between the needs of the input signal to perform the test with high accuracy and synchronisation, the rest of the instrumentation and the ADC to be measured. It should

be remembered that tests have to be performed by setting specific measurement conditions that have to be fulfilled with almost no degree of freedom. Since a space mission may involve more than one COTS ADC to be qualified, the advantage of having more than one generator is amplified, and the choice can be optimised according to the test needs, the availability of generators and the devices to be measured.

The ability to drive the ADC under test with low-purity sinusoidal signals also eliminates the need for expensive custom-made filters at the input signal path of the ADC. If the test requires filters in the input signal path to reduce the noise level, its requirements will no longer be as demanding, making it possible to use cheap commercial filters.

Therefore, the relaxation of generator linearity requirements is a clear advantage that can strongly reduce production test costs, both by using less expensive instrumentation and by speeding up the design and assembly of the setup. Obviously, because of the demand for instrumentation, is a major advantage when there are qualification test flows of high-resolution COTS ADCs running in parallel.

2. Large number of samples. Alternative methods that relax the number of samples acquired for the linearity test would overcome the high time consuming data acquisition. This drawback is strongly accentuated in the space industry: (1) by all the times that the same part or sample has to be measured electrically during its qualification for space. (2) The test flow has to be performed on a large number of parts. (3) The time constraints during the Evaluation TID test. The TID test is usually performed on a set of parts that are biased (called ON parts) and another set of parts whose connections are grounded (called OFF parts) during the radiation exposure. Generally, the number of parts that are subjected to this test is 10 (plus a Control sample). The time limitation between each exposure step of two hours maximum means that these parts have to be measured within that time. If the electrical measurement testing time of each part is so long, additional actions may have to be taken for the strict timing comply and also to enable a handling time in case problems arise during the measure. A solution is to divide the TID test into two TID tests (ON parts and OFF parts) but complicating the test procedure and its execution. (4) For issues arising if the parts are re-tinned. Re-tinned parts may have poor contact with the measuring socket due to the loss of coplanarity by the re-tinning process. The test result under these conditions may be a failure and/or false and the part must be repositioned to retest the electrical measurement. In these cases, a quick test that requires a short data acquisition but with a reliable result would allow to evaluate if the test is running under proper conditions, without having to wait for a long run time to get the results of the histogram method.

1.4 Alternative methods to the Standard Histogram Method



FIGURE 1.3: Standard Histogram method drawbacks and alternative methods

In section 1.3 it has been exposed the challenge that in general implies the application of the Standard Histogram method for the estimation of the set of transition levels in high resolution ADCs (set that will allow us to obtain the parameters of nolinearity) and how it may become a handicap in the industrial test and in particular for the New Space industry.

Over the last few years, a large number of papers have been published looking at alternative methods to the Standard Histogram method to reduce test time and/or the cost of demanding expensive test instrumentation. The proposals presented in this thesis are based on two approaches depicted in the Figure 1.3: (1) spectral processing to obtain an INL signature acquiring a lower number of samples than required by the Standard Histogram method and (2) using the redundant information from two histograms obtained from the output data in response to the ADC excitation with two signals, with lower accuracy than the Standard Histogram method required, identical to each other except for a constant offset between them. In the dissertation, this method is called Double Histogram (DH) method. Subsections 1.4.1 and 1.4.2 on this section are intended to show different existing works on these subjects that have contributed to the development of this thesis. Other alternative methods to the Standard Histogram method which do not use a spectral processing or double histograms as the main test procedure and therefore do not susceptible to appear in these subsections are introduced in subsection 1.4.3.

1.4.1 Alternative Integral Non-Linearity estimation using the spectral approach

Alternative methods based on a spectrum processing of the output signal aim to obtain an estimate of the Integral Nonlinearity INL of the ADC under test without having to resort the capture of a large number of samples, as required by the Standard Histogram method. In general, the application of these methods involve the execution of the following steps:

1. Suitable modelling of the INL. Using an INL expression that can be related to the harmonics of the spectrum:

$$INL_k \approx f(k; \alpha_1, \alpha_2, ..., \alpha_n) \tag{1.5}$$

Where α_i are coefficients to be determined that depend on the type of function *f* that expresses the INL.

- 2. ADC under test excitation with a sinusoidal signal.
- 3. Calculation of the spectrum of the output data.
- 4. Processing and obtaining the harmonics information needed to evaluate (1.5).
- 5. Evaluation of (1.5).

Figure 1.4 shows the procedure indicated in the previous points for the evaluation of the INL using a spectral approach.

Papers (Adamo, Attivissimo, and Giaquinto, 2002; Adamo et al., 2002; Attivissimo, Giaquinto, and Kale, 2004; Serra et al., 2004; Janik and Fresnaud, 2007; Kerzérho et al., 2006a; Kerzérho et al., 2006b) deal with obtaining f and evaluating the accuracy obtained depending on how sharp the actual INL curve of the ADC is and the approximation used to express it mathematically:

Approximation of the INL by a polynomial function of degree n . In this case the accuracy of the approximation depends strongly on the degree of the polynomial function. The result is a smooth curve with which



FIGURE 1.4: Test procedure using a spectral processing method

it is not possible to describe patterns with steep and sharp transitions. Among this type of polynomial approximations is the *Chebyshev test* ((Adamo, Attivissimo, and Giaquinto, 2002; Adamo et al., 2002; Attivissimo, Giaquinto, and Kale, 2004). In this test the INL is expressed as a sum of Chebyshev polynomials, whose coefficients are extracted from the spectral processing of the ADC response to a sinusoidal signal. In (Adamo, Attivissimo, and Giaquinto, 2002; Adamo et al., 2002) the coefficients of the Chebyshev polynomials can be directly related to the Fast Fourier Transform (FFT) of the ADC output. This fact implies the fulfillment of coherent sampling between the input signal and the sampling frequency. In (Attivissimo, Giaquinto, and Kale, 2004) a dedicated spectral processing is introduced to eliminate the coherent sampling condition. In order to estimate a non-smooth INL pattern with discontinuities, in (Serra et al., 2004) the INL is modeled as the sum of a Low Code Frequency component (LCF) and a High Code Frequency component (HCF). The LCF component corresponds to the smooth part of the INL pattern and is modeled by a polynomial approximation. The HCF component corresponds to the discontinuities of the INL pattern and is estimated using a narrow band histogram test.

Approximation of the INL based on the Discrete Fourier Series . (Janik and Fresnaud, 2007; Kerzérho et al., 2006a; Kerzérho et al., 2006b). This approach apply the Fourier series expansion to develop the INL expression. The INL curve must be periodic to be expressed with a Discrete Fourier Series, so a mathematical technique is used consisting of defining a periodic INL function and using from it only the interval of interest. According to the authors, this technique may work well even for the estimation of a sharp INL curve with steep transitions.

Our proposal presented in (Peralias and Jalon, 2007; Peralias, Jalon, and Rueda, 2007; Peralias, Jalon, and Rueda, 2008) consists of obtaining an expression of the INL by analysing the local behaviour of the transfer function at the ideal transition levels. The local variation of the transfer function at ideal transition leves will be obtained by means of the Taylor series approximation using the derivatives of the function at that point. This work uses a first-order Taylor series expansion. The transfer function thus written and evaluated at the real transition levels will allow it to be related to the INL:

$$INL_k \approx \frac{k - Z(l_k)}{q \cdot \partial_x Z(l_k)}$$
(1.6)

where $Z(l_k)$ and $\partial_x Z(l_k)$ are the ADC transfer function Z(x) and its derivative evaluated at the k^{th} ideal transition level.

Obviously, an estimation of the INL as in (1.6) requires that the transfer function Z(x) complies:

- It is a smooth, continuous and derivable function with respect to the input signal *x* over the full input range of the ADC.
- It is a strictly increasing function and, therefore, with derivative always non-zero over the full input range of the ADC.

When the input signal to the ADC is an analogue sinusoidal signal, its response will be a sinusoidal coded signal, but including the errors introduced by the ADC. This is modeled as the sum of a main tone corresponding to the pure excitation sinusoidal signal plus the harmonics of the main tone frequency. This description of the ADC response to a sinusoidal signal will allow to relate the INL in (1.6) to the amplitude, frequency and phase parameters of the harmonic superposition. The complete information and the development of our novel proposed algorithm, refered in the thesis as Simple Spectral Approach or SSA, can be found in 2 of this dissertation. As major contributions of the algorithm SSA proposed in this thesis are:

- The modelling of INL is simple and is obtained from the direct application of its traditional definition. No resorting to a polynomial series parametrisation or approximations based on Discrete Fourier Series are required. The final INL expression depends directly on the amplitude, frequency and phase parameters of the harmonics of the output signal spectrum. This simplifies its application as an INL estimation method compared to other techniques based on spectral processing.
- Simulation and experimental results show that the SSA algorithm obtains accurate results even with non-smooth and sharp INL patterns. Abrupt INL patterns are typical of ADCs with Successive Approximation Register (SAR), pipeline or algorithmic topologies. This makes SSA a generalised technique independent of the type of topology the ADC is designed with.

The SSA simulation and experimental results show that it is a very suitable method in an industrial test environment with a test protocol where a very precise estimation of the shape of the INL pattern is not required but just to evaluate the maximum and minimum values in which it lies, in order to compare them with the range established by the manufacturer as valid. It is a trade-off between accuracy and cost. Particularly for the New Space industry and the estimation of the INL in COTS, the SSA method implies great advantages in terms of test time reduction (1.3.1):

- 1. Because of the large number of times the parameter has to be evaluated for the same sample during the test flows and because of the large number of samples involved.
- 2. Because of the time constraints of the radiation TID test.

But it can also be very useful if is included in a test protocol to quickly evaluate if the test is not running under correct measurement setup conditions such as poor contact with the measurement socket, which is very common in retinned parts, or temperature settling problems during high and low temperature tests. The final test result would be obtained by the Standard Histogram method if required by customer conditions, but introducing the SSA method as an initial check test. This is depicted in Figure 1.5 where the



FIGURE 1.5: Test protocols using SSA method: On the left side as a direct INL estimation method, on the right side as an initial check test

SSA method is applied either to estimate INL directly or as an initial check test.

In general, methods based on spectral processing must comply with the recommendations of the EEE Standard (Measurement and Technical, 2011) to ensure a robust test procedure:

- The sinusoidal input signal must be at least 3 or 4 bits purer or more accurate than de the ADC under test.
- Coherent sampling compliance. Coherent sampling means that the relationship between the input frequency to the ADC and the sampling frequency is such that the captured data record contains an integer number of cycles of the signal.
- Sinusoidal input signal should be within the ADC's analogue input domain, in order to avoid output clipping.
- A stationary test environment must be observed.
- The ADC must be driven by a low-jitter sampling clock.

Currently there are methods to relax the requirements of the IEEE standard, as the ones introduced by (Zhuang and Chen, 2018; Sudani et al., 2015), since compliance with these requirements increases the time and cost of the test. Sampling coherence compliance in high-resolution ADCs is one of the biggest challenges, and involves the use of high-resolution and highaccuracy frequency signal generators and full synchronisation of the test system with low jitter clocks. In INL estimation, the sinusoidal signal must span the maximum range of the ADC's analogue input domain, to obtain its evaluation by covering the maximum possible range of the ADC output code domain. In order to meet this condition, the range of the input signal must be slightly lower than the input range of the ADC, demanding a high stability of the amplitude input signal for not causing the ADC saturation.

In (Sudani et al., 2015) a comparative study is presented of four State-ofthe-Art application methods for relaxing the coherence sampling and/or the stability of the amplitude input signal. Windowing (relaxes coherent sampling) is one of the most used methods and is included in(Measurement and Technical, 2011), but as the resolution of the ADC increases, it becomes more difficult to find a suitable window function. The Fundamental Identification and Replacement (FIRE)(Sudani and Chen, 2013) and the Fundamental Estimation, Removal and Residue Interpolation (FERARI)(Sudani, Xu, and Chen, 2013; Xu, Sudani, and Chen, 2014) are more novel methods that provide accurate and robust spectral results by an accurately estimate of the non-coherent fundamental and its removing from original data. The FER-ARI method has the advantage that it can be used even when the input signal range exceeds the input domain of the ADC and amplitude clipping occurs, also relaxing the stability of the amplitude input signal requirement.

1.4.2 Integral Non-Linearity estimation using double histogram based methods

This subseccion is focused on alternative methods based on a double histogram obtained by the displacement of an input signal, to estimate the Integral Non-linearity by relaxing the linearity requirements of the generator used to excite the ADC under test. The method will be referred to in this dissertation as DH method (Double Histogram method). Figure 1.6 depicts the DH procedure for the evaluation of the INL using two identical poor accuracy inputs signal, one shifted a constant offset from the other.



FIGURE 1.6: Test procedure using the DH method

The work presented in (Jin et al., 2005a) is our starting point and is based on the idea of using two input signals of low accuracy with respect to the ADC under test ¹, identical except for a constant offset or displacement between them, to identify and remove the non-linearity component introduced by the generator from the INL calculation. The algorithm is called SEIR (Stimulus Error Identification and Removal) by its authors. A more detailed description of the method can be found at Appendix (B). The following considerations are made in (Jin et al., 2005a):

• The algorithm is developed for the particular case of ramp-type input signals. The real ramp signal is modeled as a function of time that follows the expression:

$$x(t) = x_{os} + \eta t + F(t)$$
 (1.7)

where x_{os} is the offset voltage and η the slope of the straight line that defines the linear component of the ramp, and F(t) represents its non-linear component.

¹notice that to test the linearity performance of an ADC, the Standard Histogram method requires the accuracy of the input signal to be 3 or 4 bits higher than that of the ADC under test

The function *F*(*t*) is modeled as a finite series expansion of basis functions {*F_i*(*t*), *j* = 1, 2, 3, ...} in the form:

$$F(t) = \sum_{j=1}^{Mp} a_j F_j(t) + e(t)$$
(1.8)

where $\{a_j\}$ con j = 1, 2, 3, ..., Mp is the set of Mp coefficients of the finite series expansion using Mp basis functions and e(t) represents the residual due to the unmodeled part of the approximation in Mp terms. And according to (Jin et al., 2005a) there will always be a number Mp sufficiently large for the residual to be negligible, obtaining:

$$F(t) \approx \sum_{j=1}^{Mp} a_j F_j(t)$$
(1.9)

Once the set of basis functions has been chosen $\{F_j(t)\}$, the algorithm needs to estimate the set of coefficients $\{a_j\}$ in order to identify the non-linearity introduced by the input signal.

- The method is particularised for a ramp-type input signal, since the transitions are estimated in time by counting the number of times each code appears (histogram), making a cumulative sum up to each code and multiplying it by the time elapsed from sample to sample (or sampling period). To make the method independent of time ranges, a timing normalisation in [0, 1] is performed. This will establish boundary conditions for F(t) to define the parameters of the input signal and develop its algorithm, and will establish the domain of definition for the basis functions used to approximate F(t).
- The obtaining of the coefficients {a_j} is performed by applying the DH and establishing a relation for each code between both data sets through the true Integral Nonlinearity of the converter under test, resulting in an overconstrained equation system which is solved by the Least Squared method (LS). The algorithm is applied under the assumption that the two input signals used are identical except for the constant offset, and this condition is very difficult to meet in a real measurement setup, with a non-stationary environment, where there are time drifts that will introduce variations between the first and the second signal generated as well as in the value of the offset applied,

causing systematic errors in the estimates obtained. As a partial solution to this problem a test strategy is proposed by interleaving the two excitation signals following a "common-centroid" distribution sequence according to the Thue-Morse series, information which is expanded in (Jin et al., 2005b).

Based on the work of (Jin et al., 2005a) a large number of extensions and improved techniques have been developed and summarising them all is a challenge in itself. Of great interest to help getting to know much of the existing bibliography on the subject, it is the paper (Schat, 2018) in which a survey up to the date of publication can be found. Because of the method developed in this thesis, we will focus on those works that apply a double histogram and that have most influenced the proposed solutions of some of its drawbacks.

The algorithm introduced in (Korhonen and Kostamovaara, 2007) is based on the idea presented in (Jin et al., 2005a) but with a less complex computation process focused on a Built-In-Self-Test (BIST) solution, without the need to perform a parametrisation of the non-linear component of the excitation signal and without using the LS optimisation method as it is costly in hardware resources. The proposed algorithm studies how the slope of the nonlinear input ramp is related to the code widths estimated by the histogram. The two-point difference forfulae is used for the derivative evaluation, obtaining the slope and hence the code width, from which the DNL and INL are evaluated. (Korhonen and Kostamovaara, 2007) still assumes that the test takes place in a stationary environment, where the two generated ramps are identical except for the constant offset, so the test strategy of interleaving the two signals following the "common centroid" sequence is adopted to reduce errors due to time drifts in the offset.

(Korhonen and Kostamovaara, 2008) presents an adaptation of (Korhonen and Kostamovaara, 2007) but to the case of non-pure sinusoidal input signals, being necessary to improve the initial algorithm to detect higher degree derivatives. According to (Korhonen and Kostamovaara, 2008), it is required the use of four (and not two) sinusoidal input signals identical to each other except for the constant offsets that move them, resorting to the application of Lagrange polynomials to generate a derivative formula based on four points, and not two. (Korhonen and Kostamovaara, 2009; Korhonen and Kostamovaara, 2011) address the on-chip generation of the constant offset for the application of the DH method.

In (Vasan, Chen, and Geiger, 2010) the SEIR algorithm is adapted to the use of non-pure sinusoidal signals. Previously in (Jin et al., 2004) the SEIR algorithm was used for this type of stimulus, but one signal was an attenuated version of the other. In (Vasan, Chen, and Geiger, 2010) the authors also adapt the algorithm proposed in (Korhonen and Kostamovaara, 2007) for its use with sinusoidal signals without considering the changes in (Korhonen and Kostamovaara, 2008), by modifying the histogram data obtained from the two signals and applying it directly to the equations set out in the method.

In (Jin, Chen, and Geiger, 2007) an improved version of the (Jin et al., 2005a) SEIR algorithm is shown, to reduce errors when is applied in a nonstationary test environment. The proposal is to decompose the input ramp signals into multiple smaller triangular waves and then order them following a Center Symmetric Interleaving (CSI) pattern. (Zhuang et al., 2015) focuses on the effect of flicker noise in SEIR with ramps and (Zhuang et al., 2016) concludes that the use of sinusoidal signals makes the SEIR method more robust to flicker noise.

In the work presented in (Jalon, Rueda, and Peralias, 2009) we proposed the Enhanced Double Histogram test (EDH), an algorithm for applying a double histogram method that:

- Makes no assumptions about the waveform of the input signal.
- Estimates the two sets of transition levels directly from the application of the histogram on its output data, performing a normalisation process that allows the two transition sets to be related.

The EDH method is based on a procedure similar to SEIR, and uses a parameterisation of the generator non-linearity for its description. The EDH algorithm works in non-stationary test environments but not being required any time-interleaved technique: it is based under the hypothesis that time drifts in the input signals can be modeled with an effective offset and an effective gain introduced by the signal path adder, being different values between the first and second data acquisition to construct the two histograms. The estimation of the INL pattern is obtained by applying two interlaced Least Squares methods, one to obtain the parameterisation parameters of the function describing the non-linearity of the generator and the other to correct the time drift effects by minimising with respect to the variation of the gain. The contributions of our proposal are:

- The algorithm itself considers and corrects for possible effects arising from time drifts of the generator and setup parameters during both histogram testing, with no time-interleaved procedure. The integration of a L-times Thue-Morse series in the test procedure increases the test time by L-2 times, as well as increases the difficulty of the set-up programming to manage the process implementation
- The transition levels are obtained from a direct application of the histogram method on each data set acquired for the double histogram. This gives the advantage that it can be applied with any type of input as long as its amplitude probability distribution function is known. The use of input signals other than a ramp type does not require any correction terms of higher derivatives.

In (Jalon and Peralias, 2009; Jalon and Peralias, 2010) we introduced the Simplified Double Histogram method (SDH), a simple novel proposal based on a double histogram, but without resorting to a parameterisation of the generator non-linearity for its description. Our method performs a local study for each ADC code of how the non-linearity of the generator affects the evaluated code width (called virtual code width), obtaining how much it deviates from the real code width of the ADC. As we are dealing with high resolution ADCs, each code width is assumed to be very small, so that within it and for each code it is possible to locally study how the non-lineal generator function evolves and affects the virtual code widths by means of its derivative approximated with the three-point formula. Obtaining two sets of evaluated transition levels (called virtual transition levels) from two equal input signals except for a constant offset displacement between them, it will allow estimating the actual code widths of the ADC through an expression that only depends on the two sets of evaluated transition levels and the applied constant offset. Our SDH proposal estimates the two sets of transition levels by using the same EDH approximation based on the Standard Histogram method. In the SDH method it is assumed that the two input signals and the offset for the application of the method are generated in a stationary test environment, so no input signals and offset time drifts are considered.

The work presented in (Jalon and Peralias, 2010) also addresses the problem of non-stationarity during the application of the method introducing the Extended Simplified Double Histogram method (ESDH). The ESDH method applies the proposal of EDH in (Jalon, Rueda, and Peralias, 2009) to a nonstationary test environment but adapted to the SDH new algorithm. The contributions of our proposal are:

- The algorithm does not perform a parameterisation of the generator non-linearity by a finite series expansion of basis functions, so the accuracy of the SDH and ESDH method does not depend on the number *Mp* of series elements chosen to model the generator non-linearity. This is important to emphasise as it is not a trivial task to choose the right number of *Mp* elements of the series to perform a fit to a function for which, a priori, everything is unknown. The pattern of INL estimated by SEIR will depend on the number of *Mp* basis functions selected for the fitting, and both under-selection (underestimation)and overselection (overestimation) will result in an erroneous estimate of INL. Proper fitting of the non-linear generator function is achieved when the estimated INL accurately matches the true INL signature, but which is unknown a priori since precisely the objective of this method is to obtain it.
- As in EDH, the algorithm itself considers and corrects for possible effects arising from time drifts of generator and setup parameters during both histogram testing, with no time-interleaved procedure.
- As in EDH, the transition levels are obtained from a direct application of the histogram method on each data set acquired for the double histogram. This gives the advantage that it can be applied with any type of input as long as its distribution function is known. The use of input signals other than a ramp type does not require any correction terms of higher derivatives. In (Jalon and Peralias, 2010) is explained the simple way of evaluating transition levels by the Standard Histogram method while keeping the full code range of the converter under test.

The EDH, SDH and ESDH methods are part and are fully described in this thesis work. The high accuracy of both simulation and experimental INL estimation results show that our proposals are applicable as alternative test methods to the Standard Histogram test when the available generators do not meet the linearity requirements for the ADC to be tested.

The work presented in (Gines et al., 2016) introduces a self-testable BIST test strategy based on the use of double histogram techniques. It uses an iterfacing solution for on-chip ramp generator design, based on a buffer topology that allows an offset injection for a double histogram test. The strategy was verified by simulation by applying our SDH technique.

In this section it is imperative to mention the existence of techniques developed from the SEIR method but which do not apply a double histogram as such. The methods are intended to relax the requirement for linearity of the test input signal but also reducing test time. In (Jin, Chen, and Geiger, 2009) is introduced a histogram SEIR based technique that uses the architecture property of high resolution pipelined and cyclic ADCs to only use a single nonlinear stimulus signal for linearity testing. The Ultrafast Stimulus Error Removal and Segmented Model Identification of Linearity Errors (USER-SMILE method) (Chen and Chen, 2015; Chen et al., 2018) uses the SEIR concept of applying the two nonlinear signals related by the constant offset to stimulus error removal combined with a segmented model identification of linearity errors (Yu and Chen, 2012) (see subsection 1.4.3). Although the original proposal of (Yu and Chen, 2012) uses a pure sine wave as input signal, since the expected code (which the code actually obtained is compared with) is obtained through the application of the Fast Fourier Transform (FFT), the acquisition of the two output sets removes the linearity and wave type constraints of the input signal. No histogram evaluation is required and is limited to ADCs with segmented architecture such as SAR, pipeline and cyclic ADCs. In (Chen et al., 2020) is addressed the implementation of a BIST solution for a signal generator with voltage shift generation for USER-SMILE application.

The authors of the adaptative procedure presented in (Gines Arteaga, Peralias, and Rueda, 2011) (see subsection 1.4.3) indicate as a method of relaxation of the input digital representation accuracy requirement the adaptation of the DH technique to the adaptive estimation method.

1.4.3 Other INL estimation techniques

The work presented in (Gines Arteaga, Peralias, and Rueda, 2011) proposed an adaptive no-histogram evaluation procedure of the INL applicable with any type of input signal as it does not require prototype waveforms such as a ramp or a sine. It is possible to implemented by using a low-cost digital logic. The adaptive algorithm still requires a digital representation of the input signal of at least one or two bits more accurate than the ADC under test.

The authors in (Yu and Chen, 2012) introduce an algorithm to accurate estimates nolinearity parameters dramatically reducing data acquisition. The method performs a more efficient noise averaging than the histogram method, by making a proper use of the input signal information. Knowing the pure input signal, the ideal expected output code is known and can be compared to the actual output code to obtain error terms. The method uses the fact that, in high resolution ADCs, the number of truly independent error sources contributing to linearity errors is significantly smaller than the number of codes to be tested. In (Yu and Chen, 2012) the ADC INL pattern is modeled with a three-level segmented non-parametric model and the expected output codes are evaluated via a Fast Fourier Transform of the actual output data. Therefore the method is only applicable to ADCs with segmented INL structures, such as pineline, SAR and cyclic ADCs and with pure sinusoidal input signals. As the method requires FFT of the output data signal to obtain the expected codes, INL estimates covering nearly the full input domain of the ADC will require very careful control of the amplitude of the input signal. A customised version of this test procedure was applied for the evaluation of the static parameters of the COTS 18-bit SAR AD7982 from Analog Devices during the TID qualification test campaign (Vargas-sierra et al., 2018). The work was carried out by the mixed-signal group of the Alter Technology company, to which the PhD student of this thesis belongs, in collaboration with Dr. Eduardo Peralías Macías, from the Institute of Microelectronics of Seville (IMSE-CSIC). The results were compared with those of the Standard Histogram method, showing excellent accuracy while greatly reducing the number of data acquired for its application.

Other methods extend the procedure of the Standard Histogram method: the standard histogram method, due to its high accuracy on results, is a conventional method used to calibrate the nonlinearity errors of ADCs (INLbased calibration). Recently, some studies (Gines, Peralias, and Rueda, 2017; Gines, Leger, and Peralias, 2021) have shown that its application in ADCs with a redundant codification (used in pipeline and SAR ADCs) is not appropriate, since due to its data processing procedure, is not capable of correctly estimate the INL in the multivalued regions. Notice that the Standard Histogram method will always result in a monotonic representation of the transfer function of the ADC. In (Gines, Peralias, and Rueda, 2017) the authors introduce a digital foreground INL-based calibration using a INL-based additive code, called Redundant Integral NonLinearity (INL_R) . The INL_R is obtained using the redundant information from the multivalued codes and it is experimental estimate applying the no-histogram based adaptive algorithm presented in (Gines Arteaga, Peralias, and Rueda, 2011). The INL_R information is then stored in a Look-Up-Table LUT) to be used during calibration process. In (Gines, Leger, and Peralias, 2021) an improved INL-based calibration using LUT approach is presented. The method is based on a digital post-processing of the INL estimated by the Standard histogram method, but replacing in the LUT the standarized values of INL in the multivalued regions by the INL values obtained by an extrapolation process.

Chapter 2

INL estimation using a Spectral Processing based method

2.1 Introduction

This chapter will introduce a simple method to estimate the Integral Non-Linearity (INL) parameter based on spectral processing and will show how its application in high resolution ADCs can obtain more than satisfactory results while significantly relaxing the number of samples acquired for its application compared to the Standard Histogram method (Measurement and Technical, 2011). The method is based on the idea of expressing the INL in such a way that it is possible to relate it to the spectrum of the ADC response when it is excited by a pure sinusoidal signal.

Algorithms based on spectral processing for ADC static parameter estimation, such as INL, have shown that they can obtain a more than enough description to evidence ADC high level out-of-specification. This estimation produces a partial description of the static behavior of the ADC and, for example, cannot be used for a non-linearity calibration. But from the point of view of a test in which the aim is to evaluate whether the INL parameter is within the established margins indicated by an acceptance criteria, given for example by the manufacturer, this partial description can be a valid approach.

Obtaining the INL using the ADC output signal spectrum information requires expressing the Integral Non-Linearity by a mathematical function and then relating it to the spectral harmonics:

$$INL_k \approx f_{INL}(k; \bar{h_1}, \bar{h_2}, \dots, \bar{h_n})$$

$$(2.1)$$

Where $\{\bar{h}_i\}$ is the set of complex harmonics of the output waveform.

A summary of works related to the spectral processing approach can be found in Chapter 1, section 1.4.1 of this thesis dissertation.

2.2 A Simple Spectral Approach to estimate the INL in ADCs: SSA method



FIGURE 2.1: Theoretical deduction flow to establish the SSA test procedure

Based on the previously section, the objective is to find a mathematical expression of the INL that can be related to the spectrum of the ADC output data in response to a sinusoidal input. The contributions of the new technique presented here, referred to as SSA from now on, are:

- Simplification: a study of the local variation of the ADC transfer function around each ideal transition is made under the hypotheses of continuity and derivability, obtaining a mathematical expression that can easily be related to the standard mathematical definition of the Integral Non-Linearity, not requiring to express it as a sum of polynomials or as a series expansion.
- Generalization: possibility of applying the method even to ADCs with an abrupt and sharp INL pattern.

The work developed in this chapter has been presented in the papers (Peralias and Jalon, 2007; Peralias, Jalon, and Rueda, 2007; Peralias, Jalon, and Rueda, 2008).

Figure 2.1 shows the theoretical deduction flow to establish the SSA test procedure. This seccion is devided in five subsections. The first one shows the application conditions of the technique and how to obtain a mathematical model of the INL. The second and the third sections will adapt this model so that it can be evaluated by a spectral processing of the ADC response to a sinusoidal input. These three sections are depicted and summarised at Figure 2.1. In the fourth section the SSA method will be tested by simulation. In the fith section its application to a real prototype ADC will be shown.

2.2.1 A proposal for modelling the Integral Non-Linearity

Let start from the standard mathematical definition of the INL ((Measurement and Technical, 2011) and Appendix (A)):

$$INL_k = (t_k - l_k)/q \tag{2.2}$$

where t_k is the actual transition level in which the ADC output code changes from k - 1 to k, l_k is the ideal transition level and q is the quantum or LSB of the ADC.

The aim is to link (2.2) to the transfer function of the ADC. The transfer function of an ADC relates the ADC input signal *x* to the ADC output code *Z*. As an example, Figure 2.2 shows a hypothetical ADC of *N* bits of resolution and input range [-R, +R], assuming without any loss of generalization that the ADC input range is bipolar and centered at zero and the output code range is bipolar. On the same Z(x) versus *x* graph is plotted the ideal transfer function and the assumed actual transfer function of the example ADC. An enlargement of the plot is shown in the colored shaded area. The ideal transfer function is the representation of the set of of ideal transitions, $l_k = q \cdot k$ in the example, versus the set of output codes $k \in [z_{min} + 1, z_{max}] \subset [-2^{N-1}, 2^{N-1} - 1]$, where $q = (2 \cdot R)/2^N$ is the quantum or LSB of the ADC. Without loss of generality, from now on $z_{min} = -2^{N-1}$ and $z_{max} = 2^{N-1} - 1$ will be considered as saturating codes.

The SSA proposes an approach to the Integral Non-Linearity based on two hypotheses about the transfer function:

• It is a smooth, continuous and derivable function with respect to the input signal *x* over the full input range of the ADC.



FIGURE 2.2: Example N-bit ADC transfer function: the blue line plots the ideal transfer function and the black line plots the actual transfer fuction of the example ADC

• It is a strictly increasing function and, therefore, with derivative always non-zero over the full input range of the ADC.

When the transfer function continuity assumption is made, it is presumming that the resolution of the ADC is high enough so that the quantization error is embedded in the rest of the noise contributions.

Let Z(x) be the transfer function of the ADC satisfying the above two conditions, then mathematically it can be written:

$$z = Z(x) + \varepsilon(x), \quad \exists \partial_x Z \neq 0, \quad \forall x \in [-R, +R]$$
 (2.3)

where the error function $\varepsilon(x)$ is considered of the same order as the quantization error and [-R, +R] represents the input range of the ADC.

For a better understanding of the mathematical process to be developed, the transfer function example illustrated above will be used. Consider Figure 2.3. Focusing on the actual transfer function of the example ADC, let us assume that the blades in red represent the codes obtained when performing an output data acquisition with a low density of samples per code. Then the Z(x) function can be obtained as a fit to this low-density sampling of the



FIGURE 2.3: Low density sampling of the actual transfer function of the example ADC

actual transfer function. Figure 2.4 shows a high-order (upper figure) and a low-order (bottom figure) fitting to the example actual transfer function.

For this purpose, and under the fulfilment of the two conditions indicated above for the transfer function, the local variation of the transfer function around each ideal transition level will be studied: for values of x close to each ideal transition level l_k it is possible to estimate the value of Z(x) knowing how this function varies over this small range $(x - l_k)$. This local variantion can be obtained by a Taylor series approximation. The approach here presented for the SSA method considers a low-order differentiable transfer curve using a first-order Taylor expansion around each ideal transition l_k (as is illustrated in Figure 2.5):

$$Z(x) \approx Z(l_k) + \partial_x Z(l_k) \cdot (x - l_k), \quad \forall x \approx l_k$$
(2.4)

For each ideal transition l_k , (2.4) is evaluated in the corresponding actual transition level, $x = t_k$, obtaining:

$$Z(t_k) \approx Z(l_k) + \partial_x Z(l_k) \cdot (t_k - l_k)$$
(2.5)

The value of Z(x) evaluated for $x = t_k$ roughly matches the code k for



FIGURE 2.4: High-order (up) and Low-order (bottom) transfer function approximation

that transition, $k \approx Z(t_k)$. And the term $(t_k - l_k)$ is easily related to the Integral Non-Linearity using the standard definition given in expression (2.2). Substituting in (2.5) is obtained:

$$k \approx Z(l_k) + \partial_x Z(l_k) \cdot q \cdot INL_k \tag{2.6}$$

Solving for the INL term from (2.6), the desired INL approximation is:

$$\hookrightarrow \quad INL_k \approx \frac{k - Z(l_k)}{q \cdot \partial_x Z(l_k)} \tag{2.7}$$

Obviously the INL pattern of an ADC can be evaluated from the previous expression if the first derivative of the function Z(x) exists.

A first-order Taylor expansion approximation is considered since the nonlinearity of the ADC is assumed very small. For high resolution ADCs we



FIGURE 2.5: The first-order Taylor expansion of the transfer function Z(x) around an ideal transition level l_k

can mathematically limit its value to $max_k |INL_k| < 2^{N-10}$ with N > 10. In the case that a second-order Taylor expansion is required and the second derivative of the function Z(x) exists, it is possible to obtain an alternative INL approximation to the one proposed in (2.7). The second-order Taylor expansion around each ideal transition l_k is:

$$Z(x) \approx Z(l_k) + \partial_x Z(l_k) \cdot (x - l_k) + \frac{1}{2} \partial_x^2 Z(l_k) \cdot (x - l_k)^2, \quad \forall x \approx l_k$$
(2.8)

Evaluating at each transition level *t_k*:

$$Z(t_k) \approx Z(l_k) + \partial_x Z(l_k) \cdot (t_k - l_k) + \frac{1}{2} \partial_x^2 Z(l_k) \cdot (t_k - l_k)^2$$
(2.9)

Using $k \approx Z(t_k)$ and relating (2.9) to the INL using its definition (2.2):

$$k \approx Z(l_k) + \partial_x Z(l_k) \cdot q \cdot INL_k + \frac{1}{2} \partial_x^2 Z(l_k) \cdot q^2 \cdot INL_k^2$$
(2.10)

Solving this quadratic equation in *INL*_k:

$$INL_k \approx \frac{\sqrt{2(k - Z(l_k)) \cdot \partial_x^2 Z(l_k) + (\partial_x Z(l_k))^2} - \partial_x Z(l_k)}{q \cdot \partial_x^2 Z(l_k)}$$
(2.11)

2.2.2 Inclusion of the Integral Non-Linearity model in the spectral approach

The aim of this seccion is to show how to evaluate the expression (2.7) through the spectrum of the ADC response to a sinusoidal excitation. This will be achieved by obtaining an expression for the transfer function Z(x) of the ADC when it is excited by a sinusoidal signal.

Let therefore start from the ADC that is excited by a sinusoidal input signal whose mathematical expression is:

$$x(t) = A\cos(w_x t + \varphi_x) + B \tag{2.12}$$

Where *A* is the amplitude, *B* is the offset, w_x the frequency and φ_x the phase of the sinusoidal input signal.

Considering that the objective is to estimate the static parameter INL_k for all code k, the sinusoidal signal must meet the following two requirements:

- It has to excite the full input range of the converter to cover the entire range of codes but without saturating the ADC; following the example in Figure 2.2, *A* ≈ *R* y *B* ≈ 0.
- The input frequency must be low enough so that the dynamic effects during the test are negligible. This requirement is analogous to the one in (Measurement and Technical, 2011) for the choice of a test input frequency for the evaluation of the static parameters by the histogram method using a sinusoidal input.

As the ADC is a linear system, the response of the ADC to the above sinusoidal input in (2.12) is a sinusoidal signal that contains the static errors (as indicated above, the dynamic errors have been considered negligible) introduced by the ADC and so can be described as a superposition of harmonics of the excitation frequency, whose mathematical expression is:

$$Z(x(t)) = C_0 + \sum_{n \ge 1} C_n \cos(w_n t + \varphi_n), \quad w_n = nw_1$$
 (2.13)

where w_1 and φ_1 are respectively the frequency and phase of the fundamental harmonic.



FIGURE 2.6: Application of the spectral approach to relate the input signal and the output signal parameters for a sinusoidal input

Remember that the aim is to evaluate the Integral Non-Linearity using the expression (2.7) and for this it is required to obtain the derivative of the transfer function of the ADC. The derivative of the transfer function $\partial_x Z(x)$ is calculated as:

$$\partial_x Z(x) = \frac{\partial_t Z(x(t))}{\partial_t x(t)} = \frac{\sum_{n \ge 1} w_n C_n \sin(w_n t + \varphi_n)}{w_x A \sin(w_x t + \varphi_x)}$$
(2.14)

Expression (2.13) can be evaluated finding a relationship between the parameters of the sinusoidal input signal and the parameters of $Z(x(t) \text{ as Figure 2.6 shows: since the ADC is a linear system and its response is a sinusoidal signal, the fundamental harmonic is dominant and in a first approximation it is possible to discriminate from (2.13) the remaining harmonics (<math>n > 1$) to obtain a relationship between the parameters and coefficients of the main harmonic and the expression (2.12) of the analog input signal. Thus:

$$Z(x(t)) \approx C_0 + C_1 \cos(w_1 t + \varphi_1)$$
(2.15)

 $w_1 \approx w_x$ and $\varphi_1 \approx \varphi_x$ are the frequency and phase of the fundamental harmonic and they have been identified with the frequency and phase of the input signal. On the other hand, the ADC is a linear system whose function is approximate to (Measurement and Technical, 2011):

$$Z(x) \approx \frac{g \cdot x}{q} + z_{os} \tag{2.16}$$

where *g* represents the gain and z_{os} the offset of the ADC.

From (2.15) and (2.16) the following relations are obtained:

$$C_1 \approx \frac{g \cdot A}{q}, \quad C_0 \approx \frac{g \cdot B}{q} + z_{os}, \quad w_1 \approx w_x, \quad \varphi_1 \approx \varphi_x$$
 (2.17)

A more approximate but more expensive expression can be obtained if the ADC output signal is fitted by means of Least Squares method to a sinusoidal signal expressed as $\hat{z}(t) = C_B + C_A \cos(w_z t + \varphi_z)$, where C_A, C_B, w_z, φ_z are the parameters obtained from the adjustment. In relation (2.17) these parameters would replace the coefficients, frequency and phase of the main harmonic.

Continuing with our more simplified model, including the relations (2.17) in (2.14):

$$\partial_x Z(x) \approx \frac{g}{q} [1 + \frac{\sum_{n \ge 2} C_n n \sin(nw_1 t + \varphi_n)}{C_1 \sin(w_1 t + \varphi_1)}]$$
 (2.18)

Both (2.13) and (2.18) are functions expressed in the time domain but that need to be evaluated at each ideal transition level l_k as they appear in (2.7). This will be possible knowing the time instants $t = \tau_k$ in which the input signal crosses the ideal transition levels and, from the perspective of the output data, knowing the phases $nw_1t + \varphi_n$ of the output harmonics for $t = \tau_k$. Then $Z(l_k) = Z(\tau_k)$ and $\partial_x Z(l_k) = \partial_x Z(\tau_k)$ in (2.7). For a better understanding, Figure 2.7 shows a sinusoidal excitation signal that covers the full input range of the example ADC but without producing saturation: during its travel there will be certain time instants τ_k in which the signal will reach the voltage values corresponding to the ideal transition levels l_k of the ADC, being easily related using the mathematical expression of the input wave, $x(\tau_k) = l_k$. It can then be written that:

$$l_k = A\cos(w_x\tau_k + \varphi_x) + B \tag{2.19}$$

Clearing the cosine argument $w_x \tau_k + \varphi_x$:

$$w_x \tau_k + \varphi_x = \arccos(\frac{l_k - B}{A}) \Rightarrow w_x \tau_k = -\varphi_x \arccos(\frac{l_k - B}{A})$$
 (2.20)

Equation (2.20) is expressed in terms of the parameters of the sinusoidal input signal. To express it in terms of the spectral harmonic parameters and



FIGURE 2.7: Time instants τ_k when the input signal crosses the ideal transition levels l_k

coefficients of the response, the relations of (2.17) are used:

$$\hookrightarrow \quad \delta_k = w_1 \cdot \tau_k \approx -\varphi_1 \arccos(\frac{g \cdot k + z_{os} - C_0}{C_1}) \tag{2.21}$$

where l_k has been replaced by its value $l_k = q \cdot k$.

Replacing (2.21) into the phases of the expressions (2.13) and (2.18):

$$nw_1t + \varphi_n|_{t=\tau_k} = nw_1\tau_k + \varphi_n = n\delta_k + \varphi_n \tag{2.22}$$

Applying (2.22) and (2.21) into (2.13) and (2.18) both evaluated for $t = \tau_k$, and replacing in (2.7):

Equation (2.23) provides an approximation of the Integral Non-Linearity evaluable through the amplitudes of the response harmonics $\{C_n\}$, their phase shifts $\{\varphi_n\}$, and the gain g and offset z_{os} of the ADC. All of them, in principle, can be estimated by the spectral processing of the ADC output data. Some considerations must be indicated:

Gain and offset : To obtain the gain g and offset z_{os} of the ADC it is necessary to know the exact amplitude A and offset B values of the input sinusoidal signal. This is the case, for example, if the evaluation of the gain eg and offset eos errors of the ADC is required. In general, canceling the offset z_{os} of the ADC is equivalent to a possible compensation with the offset of the input signal. Concerning to the gain, is assumed that the ADC gain is close to unity. Errors in the amplitude and offset values of the input signals do not induce errors in the INL parameter because they only induce gain and offset errors (Measurement and Technical, 2011), so the Integral Non-Linearity wanted is the one obtained after correcting the $\{INL_k\}$ vector from offset and gain contributions. In (Measurement and Technical, 2011), this is achieved by performing a fit of the set of actual transition levels t_k to the equation of a straight line, either by the Least Squares method or by the method of passing through the extreme points, for then removing the obtained line from the INL computation. This is equivalent to performing a normalization process considering g = 1 and $z_{os} = 0$ in (2.21) to evaluate (2.23):

$$\mathbf{INL}_{\mathbf{k}} \approx f_{INL}(k; C_n, \varphi_n, 1, 0), \quad \forall k \in [-2^{N-1} + 1, 2^{N-1} - 1]$$
(2.24)

where the INL in (2.24) represents the Integral Non-Linearity without the offset and gain information of the ADC.

Number of harmonics selected : The number of harmonics selected for the evaluation of (2.23) depends on the mathematical method used to obtain the harmonics parameters $\{C_n\}$ and $\{\varphi_n\}$, and on the spectral discrimination allowed by the noise floor. The work presented is based on the Discrete Time Fourier Transform (or DTFT) to obtain the spectrum of the ADC output data and, concerning to the selection of harmonics, a conservative criterion has been chosen of including those whose amplitude is at least 10dB over the noise floor.

This will be discussed in the next section.

2.2.3 Method for spectral processing and calculation of spectral parameters

In the previous section, a mathematical expression of the INL has been obtained as a function of spectral parameters calculated by the spectral processing of the ADC output signal in response to a sinusoidal excitation. In Analog-to-Digital Converters, where the output signal is obtained by sampling the input signal with a constant period Ts (where fs = 1/Ts is the sampling frequency of the ADC), many of the mathematical methods applied for the evaluation of spectral harmonics are based on the Discrete Time Fourier Transform (DTFT). In a test environment where records with a limited number of samples or output codes are acquired, the mathematical calculation can be simplified by using the Discrete Fourier Transform (DFT) (Measurement and Technical, 2011), under the assumption that a record corresponds to a single period of the input signal extending infinitely. If the record does not contain an integer number of complete cycles of the input signal, spectral leakage arises. The requirement for coherence sampling appears. This condition implies the use of high accuracy frequency signal generators and the use of a low jitter master clock that synchronises the input signal and the ADC clock signals.

Output data spectral processing based on DFT is a time-consuming challenging task for high performance ADC. The work (Sudani et al., 2015) summarizes four methods to relax some of these test requirements, as the coherent sampling or the use of an input amplitude that does not produce output signal clipping. The four methods presented are: (1) Windowing, (2) The four-parameter sine-fit, (3) Fundamental Identification and Replacement (FIRE) (Sudani and Chen, 2013) and (4) Fundamental Estimation, Removal And Residue Interpolation (FERARI) (Sudani, Xu, and Chen, 2013; Xu, Sudani, and Chen, 2014).

Estimation of the harmonic parameters under a coherence sampling test

In our test conditions, it is assumed the need to acquire a register of M output samples $\{z_i\}_{i=1}^{M}$. Coherent sampling occurs if the frequency of the sinusoidal input signal to the ADC f_x is related to the ADC sampling frequency f_s such that in the output data record there is an integer number of cycles of the input signal converted by the ADC, i.e., if it is verified (Measurement and Technical, 2011):

$$f_x = f_s \cdot \frac{J}{M} \tag{2.25}$$

where *J* is the number of complete cycles contained in the data register. The Fast Fourier Transform or FFT is a powerful and very efficient algorithm that allows to calculate the DFT. This algorithm increases its effectiveness if the number of samples stored in the register *M* is a power of two.

In addition, as is indicated in (Measurement and Technical, 2011), the condition (2.25) is also used to guarantee that the ADC samples the input signal such that M different values are sampled, being this possible if the relationship between f_x and f_s is such that there are M different input signal phases that are uniformly distributed between 0 and 2π . This condition meets when M and J do not have common factors or, what is the same, its greatest common factor is one. If the number of samples captured is a power of two, any odd integer for J satisfies the condition.

Regarding the contribution of noise, it is assumed a random, additive and white noise model, and with a background noise level allowing to make a clear discrimination of harmonics in the obtained spectrum.

Thus, let $\{\varsigma_j\} = FFT(\{z_i\})$ be the data set resulting from applying the DFT to the output data record under the above test conditions. From this new data set it will be estimated the spectral parameters of the *H* harmonics $\{\varsigma_{j_n}\}_{n=1}^{H}$ used in the calculation of the INL in (??) following the criteria: (1) They are dominant and clearly noticeable against the background noise. A very restrictive selection criterion is to consider those harmonics with aplitudes at least 10*dB* above the noise floor level. (2) Identifying the source of

other notable spectral lines in the spectrum is important, as they may be due to higher order harmonics $w_n > w_s/2$ that are folded into the spectrum represented within the Nyquist frequency or the Nyquist band; if these harmonics are part of the INL computation, a correction factor have to be introduced.

Under all these above considerations, the applicable expressions in (??) are:

$$w_1 = 2\pi f_s J/M \tag{2.26}$$

$$w_n = nw_1 \tag{2.27}$$

.- - - .

$$C_0 = mean_i\{z_i\}$$
(2.28)

$$C_n = (2/M) \cdot \|\varsigma_{j_n}\| \tag{2.29}$$

$$\varphi_n = (-1)^{p_n} \cdot Arg(\varsigma_{j_n}) \tag{2.30}$$

$$g = q \cdot rms\{z_i\} / rms\{x(t)\}$$
(2.31)

where for $k \ge 0$:

$$p_n = \{ \begin{array}{ll} 0 & w_n/w_s \in [k, (2k+1)/2[\\ 1 & w_n/w_s \in [(2k+1)/2, (k+1)[\end{array} \} \} \}$$

 p_n is the function that corrects the inversion phase in the case of folded harmonics in the spectrum.

Although the gain and offset contributions are eliminated from (2.23) by taking g = 1 and $z_{os} = 0$, in (2.26) is indicated a simple way to evaluate the gain g by calculating the Root Mean Square of the input signal $RMS\{x(t)\}$, which is easily measurable with a wattmeter. Under the assumption of a low distortion ADC, the difference between the gain measured in this way and that evaluated by standard methods such as fitting the set of transition leves to a straight line and matching the gain with the slope (Measurement and Technical, 2011), is usually less than 0.5%.

If, when calculating the output signal spectrum, a noise averaging is required on the acquisition of R records of M samples length, these records must be consecutive captured since the phase information is necessary and cannot be lost. A single record of $R \cdot M$ samples must be captured to this end and where the coherent sampling requirement apply to *M* samples. Spectrum averaging is performed by applying the FFT to the data of each of the R records, obtaining the modulus and argument of data of each new data set, and using them to obtain averaged modulus and argument:

$$\{\varsigma_j^{(m)}\}_{m=1}^R = FFT\{z_i^{(m)}\}$$
(2.32)

$$\|\hat{\varsigma}_{j}\| = \sqrt{mean_{m=1,\dots,R}} \{ \|\varsigma_{j}^{(m)}\|^{2} \}$$
(2.33)

$$Ar\hat{g}(\varsigma_j) = mean_{m=1,\dots,R} \{ Arg(\varsigma_j^{(m)}) \}$$
(2.34)

where $\|\hat{\varsigma}_j\|$ is the averaged modulus and $Arg(\varsigma_j)$ is the averaged argument. (2.26) to (2.32) will continue to be valid expressions but considering the averaging in *R* records.

An alternative approach to obtain an averaged spectrum is to address the problem from the time domain signal, this is a Time-Avaraged Spectrum. It consists of averaging the raw data over the *R* records of *M* samples to obtain an averaged signal:

$$\{\hat{z}_i\} = mean_{m=1,\dots,R}\{z_i^{(m)}\}$$
(2.35)

and then calculating the FFT:

$$\{\varsigma_j\} = FFT(\{\hat{z}_i\}) \tag{2.36}$$

Time-Avaraged Spectrum is very useful in the SSA method as it overaverages the spectral noise and can allow discerning a larger number of spectral lines embedded in the noise floor.

Estimation of the harmonic parameters under a non-coherence sampling test

If the sinusoidal input frequency and the sampling frequency are not accurately known and controlled leading to the coherent sampling condition is not met, the DFT application causes spectral leakage. Windowing or to apply a window function to the output data is proposed in (Measurement and
Technical, 2011) to reduce spectral leakage. For the case of a spectrum averaging, the window function is applied to each sub-record *R*:

$$\{\varsigma_i^{(m)}\}_{m=1}^R = FFT\{w_i z_i^{(m)}\}$$
(2.37)

where $\{w_i\}_{i=1}^M$ is the convolution window. In this case the coefficients in (2.26) have to be corrected by a factor that depends on the applied window.

If the test input frequency is such that there are high-order harmonics above the Nyquist frequency and folded into the Nyquist band, when windowing is used it is not only necessary take care with the proper selection of harmonics, but also a fine adjustment on the input frequency considering that there are no overlaps between the lobes of the harmonics taken for the INL evaluation with (2.23).

2.2.4 Simulated experiments

In order to test the SSA method, simulated experiments for the estimation of the Integral Non-Linearity have been performed on two ADCs with very different signatures of this parameter:

- ADC_1 : high-level model of a Sigma-Delta ADC with 14-bits of resolution and $f_s = 100ksps$ of sampling frequency. The ADC works in unipolar configuration with reference voltages $R^- = 0.0V$ and $R^+ = +5.0V$ and a useful input range [+0.5V, +4.5V]. The model: (1) includes offset and non-linearity effects considering a very regular transfer function affected by +7.3LSB of offset and whose nonlinearity is described by a smooth curve, (2) models a frequency behavior to simulate dynamic effects and (3) also considers the noise introduced by both the ADC and the input treated as a 2LSB RMS white noise referred to the input.
- ADC_2 : high-level model of a pipeline ADC with 16-bit of resolution and a sampling frequency up to $f_s = 5Msps$. The ADC works in bipolar configuration with reference voltages $R^- = -2.0V$ and $R^+ = +2.0V$. The model: (1) considers a non-monotonic transfer characteristic and whose non-linearity presents strong and sharp discontinuities, (2) models a frequency behavior to simulate dynamic effects, (3) the noise introduced by both the ADC and the input is modeled as a 1*LSB* RMS white noise referred to the input.

For each of the above ADCs the Integral Non-Linearity evaluated by the Standard Histogram method (Measurement and Technical, 2011) is taken as the real INL reference pattern. In order to this, the histogram method is performed under the same test conditions as for the application of the SSA method, but with the amplitude of the sinusoidal signal that slightly saturates the ADC under test and with a number of captured samples suitable for the application of the method: in a sinusoidal wave test, the minimum record size ensuring a sample of every code is $M = \pi \cdot 2^N$, in the case of the ideal ADC transfer function in the absence of random noise. The section has been divided into three parts or experiments:

- Experiment 1: a direct application of the approximation (2.7) to the *ADC*₁ model will be performed.
- Experiment 2: Application of the SSA spectral algorithm to estimate the INL pattern of the *ADC*₁ model.
- Experiment 3: Application of the SSA spectral algorithm to estimate the INL pattern of the *ADC*₂ model.

The simulated experiments have been presented in the papers (Peralias and Jalon, 2007; Peralias, Jalon, and Rueda, 2007; Peralias, Jalon, and Rueda, 2008).

Experiment 1: *ADC*₁ **under a low-density DC sweep**

In order to show an immediate application of the INL modeled as (2.7), an experiment has been devised using the ADC_1 model as the ADC under test. The aim is to find an expression Z(x) that describes the transfer function of the ADC under test and satisfies the assumptions of continuity, derivability and growth already listed above. To do so, the idea is to perform a low-density sampling by means of a DC sweep, obtain for each input value \bar{x}_i a record of output codes or samples to compute and associate to it the average code \bar{z}_i . On the set $[(\bar{x}_i, \bar{z}_i)]$ a best-fit polynomial of degree Mp, $Z_{Mp}(x)$, will be constructed. This polynomial can be directly replaced into (2.7).

Firstly, the excitation signal has been constructed to perform a DC sweep of about 4000 points covering the input range [+0.7V, +4.3V]. Each of these points excites the ADC under test model, registering for each input value 50 points or output codes. Secondly, on each register of 50 stored codes, an



FIGURE 2.8: a)INL estimation and b) difference or error for the ADC_1 approximating Z(x) in a low-sampling test and using a DC sweep: in thick black line the one obtained by (2.7), in thin blue line the INL reference pattern evaluated by the Histogram method.

average code is calculated, being in this experiment inside the range $I_k = [-5792, 5801]$. Now, each input level with which the ADC has been excited has a corresponding output code associated with it. Thirdly, a polynomial fit has been applied to the above input-code data set. In this experiment, the Chebyshev polynomials of the first class Tn in its trigonometric definition have been chosen as the basis function. The choice of the degree of the polynomial was adjusted according to the number of significant harmonics found in the spectrum of Simulated Experiment 2, being Mp = 32. This idea will be discussed later.

It has been already defined the function $Z_{32}(x)$ which models the transfer function of the simulated ADC and its derivative. Under these conditions, it is possible to obtain for each $k \in I_k = [-5792, 5801]$ code the value of $Z_{32}(l_k)$ and $\partial_x Z_{32}(l_k)$ to evaluate INL_k according to (2.7). In order to obtain a reference curve of the INL of ADC_1 with which to compare the results, the application of the Standard Histogram method has also been simulated using a sinusoidal waveform as the excitation signal and taking R = 64 records of $M = 500 + 2^{12} = (500 + 4096)samp/reg$. The number of 500 samples are recorded at the beginning of ech register to reduce setting errors by removing them from the final computation: the total number of output samples computed for the histogram is $Mtotal = 64 \cdot 2^{12} = 262144$ samples. The amplitude of the input signal saturates the input range of the ADC under test and the input frequency has been set in the order of 83 times lower than the sampling frequency (to avoid dynamic effects on the measurement) and observing coherent sampling over the 4096 samples, being $f_x = 1.1962KHz$. The phases of the records have been evenly distributed between $[0, 2\pi]$.

Figure 2.8 a) shows in black line the INL estimated by (2.7) and in blue line the reference INL pattern obtained by the Standard Histogram method. Both pattern shapes match but with a displacement of about 0.5LSB, showing the high accuracy achieved by the method in a smoothy INL pattern. It should be mentioned that the curves depicted in Figure 2.8 a) are shifted by about -6LSB respect to 0LSB due to no offset correction has been made to remove its contribution from the INL: practically the offset from which the ADC_1 transfer function is affected is shown. Figure 2.8 b) depicts the difference between both estimations, showing the systematic 0.5LSB error commented above. This difference comes since (2.5) and (2.6) are evaluated from the transitions levels instead of the code centers. As the INL desired is the one without offset contribution, it must be eliminated from the final INL calculus, in this case correcting it by means of the its mean value. When the expressions (2.23) and (2.21) are used through the spectral processing, no offset correction is needed since the offset contribution is eliminated considering $z_{os} = 0$.

Experiment 2: *ADC*₁ **under a sine-wave input**

This simulated experiment will show the result of the application of the SSA method, estimating the INL of the ADC_1 using (2.23). To carry out the experiment, it is necessary to generate a sine wave to excite to the ADC under test and to construct the spectrum of the response signal. The choice of parameters defining the sinusoidal input signal are as follows:



FIGURE 2.9: Typical spectrum for the *ADC*₁ averaging 4 records of 4096 samples

- Amplitude *A* of about –3*dBFS* to cover the same input range as the previous experiment and with an offset *B* in the range of 100*LSB* from mid-range at 2.5*V*.
- Input frequency of value well lower than the sampling frequency in order to not introduce dynamic effects in the measurement. In this experiment, a value approximately 83 times below, *f_x* ≈ *f_s*/83 = 1.2048*kHz*, has been selected. The input frequency value has also been set to emulate an experiment where coherent sampling is not achieved with the accuracy required.
- The input signal phase was uniformly distributed within the range [-π, +π] by the repetition of 35 simulated experiments.

The equivalent noise referred to the input will now be included as 1*LSB* RMS white noise.

Addressing data capture for the SSA method application, R = 4 consecutive output records of $M = 2^{12} = 4096 samp/reg$ are acquired. Added to these data, 500 samples are recorded at the beginning of the acquisition to reduce settling error effects by removing them from the final computation. The

Index n	Amplitude (dBFS) C _n	Phase (degree) φ_n
1	-3.0	177.9
3	-70.3	-6.7
2	-85.2	175.3
5	-90.2	169.1
6	-90.2	-12.2
22	-93.9	134.4

TABLE 2.1: In order of harmonic magnitude, first six amplitudes and phases estimated from the ADC_1 output data spectrum

total number of samples captured are $500 + (4 \cdot 4096) = 500 + 16384$ samples. As the INL pattern reference was estimated (in the previous simulated experiment) taking 262144 samples, the number of samples used for the SSA application is 1/16 times the number of samples required for the histogram method.

Finally, the FFT is applied to each set of 4096 samples and an averaged spectrum over the 4 records is calculated. Figure 2.9 depicts the typical magnitude spectrum obtained. In this experiment a window function application is needed to avoid spectral leakage due to non-coherent sampling. The selection of an appropriate window function and the extraction of the spectral parameters corrected for the effect of its application have been treated according to the works presented in (Belega, Ciugudean, and Stoiciu, 2007; Zhu et al., 2007), chosing a 4-term cosine window for output data windowing and a linear phase regression algorithm for the {*C_n*}, {*w_n*} and {*φ_n*} spectral parameters extraction. The DC component have been evaluated by means of the weighted mean of the samples, using as weight function the convolution window:

$$C_{0} = mean_{m=1,\dots,R} \{ \frac{\sum_{i} (w_{i} \cdot z_{i}^{(m)})}{\sum_{i} w_{i}} \}$$
(2.38)

As Figure 2.9 shows, the background noise is approximately -112dBFS. Following the very restrictive selection criterion of choosing harmonics with amplitudes at least 10dB above the noise level, those with amplitudes higher than -102dBFS will be chosen as possible harmonics to compute (2.23). In addition, among these harmonics, only those whose estimated frequency does not deviate from a multiple of the fundamental frequency by more than



FIGURE 2.10: a)Black thick line: estimation of the INL of the ADC_1 using SSA method. Blue thin line: reference INL obtained by the Standard Histogram method b) Difference between the SSA INL estimation and the one estimated by the standard histogram method, c) Differences obtained for all of the SSA experiments performed in ADC_1

2.25 times the spectral resolution $\Delta f = f_s/4096$, that is $|f_n - h \cdot f_1| \leq 2.25 \cdot \Delta f$ with h an integer, have been selected to compute (2.23). This criterion allows to accurately discriminate true harmonics from other spurious lines, even if they are high frequency harmonics folded into the Nyquist band of the spectrum. The typical selection detects about 17 harmonics with orders up to 30^{th} . Table 2.1 indicates, in order of magnitude, the estimated amplitude and phase values of the first six harmonics selected from the spectrum of this experiment. Amplitude values are given in *dBFS* unit. Remark that the estimated amplitude of -3dBFS matches the amplitude value of the input sinusoidal signal used in this experiment, which is consistent with the unity gain of this ADC model.



FIGURE 2.11: Histogram estimation using 4 records of 4096 samples and its comparison with the standard histogram method

Figure 2.10 a) plots in black line the typical INL result obtained for one of the 35 expreriments when the SSA method is applied and in blue line the INL pattern reference corrected from the offset effect. In this case the INL curves are completely overlapping since the offset contributions are corrected from both estimations, the SSA method by considering $z_{os} = 0$. The INL reference pattern covers approximately the range of $\pm 4LSB$. Figure 2.10 b) plots the difference or error between the two INL patterns, that lies between $\pm 0, 3LSB$. Figure 2.10 c) shows the differences between the INL estimating by each of the 35 experiments and the INL pattern reference, showing that the error always lies within the range $\pm 0, 4LSB$.

The application of the histogram method with only 4 records of 4096 samples each would lead to large errors in the estimation of the INL pattern. This is depicted in Figure 2.11, where the blue line plots the INL obtained by the histogram method using a $4 \cdot 4096$ samples, resulting in a INL pattern within the $\pm 10LSB$ range.

By applying the SSA method and using only 16384 samples, a number 1/16 times the number of samples used for the Standard Histogram method (or the 6.25%), it has been possible to accurately estimate the INL of the ADC_1 , with a smooth pattern and $INL_{max} = 4LSB$, fully matching its shape,

being in the same range of values and with a maximum error of 0.4LSB. In contrast, the application of the histogram method using the same 16384 number of samples leads to an inaccurate INL estimation that is not able to estimate the actual shape of the INL curve and that duplicates the range of values in which it moves.





FIGURE 2.12: Typical spectrum for the *ADC*₂ averaging 8 records of 32768 samples

In this section, a simulated experiment is carried out for the application of the SSA method in the ADC model ADC_2 , with a higher resolution and higher speed than the previous one and with a non-smooth and sharp INL signature.

The experiment operates the ADC at a sampling frequency of $f_s = 1Msps$ and the sinusoidal input signal is programmed as:

- The generated sinusoidal input signal will cover practically the full input range of the ADC under test, by setting -0.2dBFS of amplitude *A*. The signal offset *B* is in the range of 10LSB.
- The input frequency is well lower than the sampling frequency in order to not introduce dynamic effects in the measurement. In this experiment, a value of approximately 223 times below, $f_x \approx f_s/223$, has



FIGURE 2.13: a)Black thick line: estimation result of the INL of the ADC_2 using SSA method and including gain effect. Blue thin line: reference INL obtained by the standard histogram method and including gain effect, b) Difference between the SSA INL estimation and the one estimated by the standard histogram method

been selected. The input frequency value has been set to emulate a coherent sampling experiment. The number of samples per record selected on which the coherent sampling has been established is $M = 2^{15} = 32768 samp/reg$, being the coherent sampling met for J = 147 and $f_x = f_s \cdot (147/32768) = 4.4843 kHz$.

 The input signal phase was uniformly distributed within the range [-π, +π] by the repetition of 35 simulated experiments.

In order to obtain a reference pattern of the INL of ADC_2 with which to compare the results, the application of the Standard Histogram method has also been simulated using a sinusoidal waveform as the excitation signal and taking R = 64 records of $M = 500 + 2^{15} = (500 + 32768)samp/reg$. The number of 500 samples are recorded at the beginning of ech register to reduce setting errors by removing them from the final computation: the total number of output samples computed for the histogram is $Mtotal = 64 \cdot 2^{15} = 2097576$ samples. The amplitude of the input signal saturates the input range of the



FIGURE 2.14: a)Black thick line: estimation result of the INL of the ADC_2 using SSA method with g = 1. Blue thin line: reference INL obtained by the standard histogram method and including gain effect, b) Both estimations corrected by gain and offset contributions

ADC under test and the input frequency has been set in the order of 223 times lower than the sampling frequency (to avoid dynamic effects on the measurement) and observing coherent sampling over the 32768 samples, being $f_x = 4.4843kHz$. The phases of the records have been evenly distributed between $[0, 2\pi]$.

Addressing data capture for the SSA method application, R = 8 consecutive output records of $M = 2^{15} = 32768samp/reg$ are acquired. Added to this data, 500 samples are recorded at the beginning of the acquisition to reduce settling error effects by removing them from the final computation. The total number of samples captured are $500 + (8 \cdot 32768) = 500 + 262144$ samples. As the INL pattern reference was estimated computing 2097576 samples, the number of samples used for the SSA application is 1/8 times the number of samples required for the histogram method.

The FFT is applied to each record of 32768 samples and a spectrum averaged over the 8 records is calculated. Figure 2.12 depicts the typical magnitude spectrum obtained, observing how the sharp shape of the INL results in a large number of harmonics in the spectrum. The background noise is approximately -130dBFS. Following the very restrictive selection criterion of choosing harmonics with aplitudes at least 10dB above the noise level, those with amplitudes higher than -120dBFS will be chosen as possible harmonics to compute (2.23). The so irregular structure with sharp discontinuities of the INL of this ADC leads to the typical selection detects about 165 harmonics with orders up to 680^{th} .

First of all, the SSA method is applied without any normalisation of the gain g in the expression (2.21), obtaining its value through the proposal in (2.26). In order to be able to compare the result with the reference INL, the pattern obtained with the standard histogram method has not been corrected for the effect of gain. Figure 2.13 a) depicts in black line the INL estimated by SSA method and in blue line the reference INL estimated by the histogram method. It shows that even for such sharp INL pattern of the ADC_2 , the SSA method estimation absolutely follows (obviously with a smoothing effect) the reference curve processing 262144 samples, a number 8 times fewer than the one used by the histogram method. The result also evidences the high accuracy in the measurement of the gain from the AC power relation between the output and input signals through (2.26). Figure 2.13 b) plots the difference between both estimates: the main differences or errors occur in the areas where the discontinuities of the transfer function are more abrupt, where the smoothing effect of the curve due to the limited number of harmonics that have been selected is more evident.

As the INL required is the one corrected by gain and offset effects, measuring the gain value is not necessary since for the SSA method this is simply achieved in this example by taking now g = 1. Figure 2.14 a) depicts in black line the INL estimated by SSA using g = 1 and in blue line the reference INL including the gain effect. Figure 2.14 b) plots the same INL estimations as in a) but now with both pattern corrected by gain and offset contributions by means of the substraction of the best-fitting line.

The experiment has been replicated on the same ADC model but acquiring only two consecutive records, R = 2, of M = 32768 samp/reg. The FFT



FIGURE 2.15: SSA application using 2 records of 32768 samples and its comparison with the standard histogram method

is applied to each record of 32768 samples and a spectrum averaged over the 2 records is calculated. In this case, the typical selection detects about 150 harmonics with orders up to 600th. The INL pattern obtained when the SSA method is applied is analogous to the previous one. Figure 2.15 plots in black line the INL estimated by the SSA method and in blue line the INL reference pattern, both corrected by gain and offset contributions by means of the sub-straction of the best-fitting line.

The application of the histogram method with only 2 records of 32768 samples each would lead to large errors in the estimation of the INL pattern. This is depicted in Figure 2.16, where the blue line plots the INL obtained by the histogram method using $2 \cdot 32768$ samples, resulting in a INL pattern within the $\pm 25LSB$ range.

Application of the SSA method acquiring only 65536 samples, that is a number 1/32 times the number of samples acquired by the Standard Histogram method (or 3, 125% of the required by the histogram) it has been possible to estimate the INL of the ADC_2 , with a transfer function with sharp discontinuities and $INL_{max} = 4LSB$, fully adapted to its actual shape and being in the same range of values. In contrast, the application of the histogram method using the same 65536 number of samples leads to an inaccurate INL estimation that is not able to estimate the actual shape of the INL curve and that increases the range of values in which it moves to $\pm 25LSB$.

With the results of the three simulated experiments above, the feasibility



FIGURE 2.16: Histogram estimation using 2 records of 32768 samples and its comparison with the standard histogram method

of the SSA method has been demonstrated by simulation in a low-cost test environment where test time reduction is critical. This may be the situation in New Space industry, where minimising measurement time costs is critical: (1) with a massive number of COTS devices to be tested (2) the same component is evaluated several times (3) under a Pass/Fail criterion given by a range or limits in which the evaluated device parameter must be inside.

2.2.5 Application of the method to a real ADC Pipeline

As an example of application of the SSA method, this section shows the results of a laboratory experiment to estimate the INL pattern of a pipeline prototype ADC of 12-bit of resolution, using the SSA method. The experiment was introduced in the paper (Peralias, Jalon, and Rueda, 2008) to present an SSA application and its results on a real ADC with an abrupt INL pattern. The ADC under test is fully differential prototype in a 120 nm CMOS technology with reference voltages $R^- = -1V$ and $R^+ = +1V$.

The input signals driven to the ADC under test are AC-coupled and generated by the Agilent N8241A AWG generator. The experiment has been performed at an input frequency of $f_x \approx 500kHz$, with the ADC under test operating at a sampling frequency of $f_s = 20MHz$, and always under coherent sampling compliance.



FIGURE 2.17: Prototype ADC: Output spectrum for the SSA method application showing selected harmonics



FIGURE 2.18: INL estimated by the Standard Histogram method and by the SSA method

First, the SSA method has been applied using a single record of M = 4090 samples. No windowing or spectral averaging is required. The input frequency is $f_x \approx 503 KHz$. The input amplitude is A = -0.1 dBFS. Figure 2.17 depicts the magnitude spectrum of the output data of the acquired record, with a floor noise at about -100 dBFS. The harmonics selected have been those with the amplitude higher than -90 dBFS, taking the typical selection about 45 harmonics with orders up to 150^{th} .

In order to obtain a INL reference pattern with which to compare the results of the estimation using the SSA method, a Standard Histogram test has been performed. This test has been carried out with an input amplitude saturating the ADC under test and acquiring 262144 samples, a much larger number of output data than for the application of the SSA method.

Figure 2.18 shows the INL pattern estimated by the SSA method (black line) versus the INL reference pattern (indicated as Real INL in the picture and depicted in blue line). Remark that the INL obtained by the spectral method reproduces the shape of the reference pattern even at large steps, and both are within the same INL values. The SSA method has required 1.56% of the number of samples required by the Histogram method.

Chapter 3

INL estimation based on the Double Histogram method

3.1 Introduction

Methods based on a double histogram aim to perform the linearity test on high-resolution ADCs by relaxing the linearity requirement of the excitation signal generator. This is achieved by applying two identical signals shifted one from each other by a constant offset, constructing two histograms of the two sets of output data and relating the two sets to the input signal nonlinearity.

These appraches have shown that they can achieve high accuracy results in the INL estimation using low-accuracy input signals versus the accuracy of the ADC under test, being methods potentially applicable in low-cost test environments. But they are very sensitive to time drifts of the input signal and the applied offset between the first and the second data acquisition. This information can be found at subsection 1.4.2 of Chapter 1.

3.2 A proposal for the Non-Linearity estimation based on the Double Histogram method

This section describe our DH-based proposal for the estimation of Non-Linearity in high resolution ADCs by using generators less linear than the converter under test. The contributions of the developed algorithm can be summarised in the following points:

Simplification of the method:

- As a major innovation, it uses very simple relationships through the two related input signals. It does not require to express the non-linearity of the generator as a series expansion of basis functions whose coefficients must be estimated by solving a system of non-linear equations.
- The method provides a simple way of evaluating transition levels by the Standard Histogram method while keeping the full code range of the converter under test.

Generalisation of the method:

- It is a black box method. It treats the ADC as a black box, it makes no assumptions about its internal architecture.
- It works with any type of input waveform. No assumptions have to be made about the waveform of the input signal, as the transition levels are evaluated by the Standard Histogram method. It does not require any correction terms of higher derivatives.
- As a major innovation, the method is adapted to a non-stationary measurement set-up, and the algorithm itself considers and corrects the possible time drifts during the test of each histogram. No alternative procedure is required to compensate for the possible errors generated.

Firstly, the use of the Standard Histogram method (Measurement and Technical, 2011) will be discussed. The basic block diagram of the measurement set-up for the estimation of the non-linearity parameters of a ADC by means of a generator that is less linear than the converter under test, is shown in the Figure 3.1. The figure, without loss of generality, depicts an N-bit ADC (ADC under test or ADCUT in the picture) with input range $[R^-, R^+]$ and

3.2. A proposal for the Non-Linearity estimation based on the Double Histogram method



FIGURE 3.1: Non-Linear AWG model for an ADC stationary test set-up

with transition levels $\{t_k\}, \forall k \in [1, 2^N - 1]$. From now on, and without loss of generality, the lower saturating code is considered to be 0 and the upper saturating code is considered to be $2^N - 1$. The non-linear generator, block named NL - AWG in the figure, is modeled as an ideal voltage source called Virtual Source (*VS*) that supplies the ideal signal x(t), to which a non-linear component $\Psi(\cdot)$ is added, being the final input signal that excites the ADC $u(t) = x(t) + \Psi(x(t))$. According to this, the probability distribution of the amplitude of the signal driving the ADC is not known with accuracy, so the ADC under test is not in a suitable condition for the application of the Standard Histogram method for the evaluation of its real transition levels, $\{t_k\}$.

Consider now the Figure 3.2, where the non-linear part of the generator $\Psi(\cdot)$ is associated to the ADC; this group can be considered as a new virtual ADC, named Global ADC (*GADC*) and with virtual transitions { τ_k }, which is in the appropriate conditions for the application of the Standard Histogram method, since it is excited by the ideal signal given by the ideal virtual generator *VS* and which amplitude probability distribution is a priori known. Therefore, the application of the Sandard Histogram method in the test set-up under discussion does not allow to directly estimate the real transition levels of the ADC under test { t_k }, but virtual transition levels modified by the non-linearity of the non-linear generator { τ_k }, as represented in Figure 3.2.



FIGURE 3.2: New ADC stationary test set-up with a Global ADC

However, the virtual transition levels of the *GADC* and the real transition levels of the ADC under test are univocally related through the *NL* – *AWG* generator non-linear function, denoted as f(x) and mathematically expressed as $f(x) = x + \Psi(x)$. This is depicted in Figure 3.3, that shows if this function is evaluated at the instants when the virtual signal x(t) passes through the *GADC* virtual transition levels, $x = \tau_k$, this matches to the instants when the distorted signal u(t) passes through the real transition levels of the ADC under test. Mathematically:

$$u(x = \tau_k) = t_k = f(\tau_k) = \tau_k + \Psi(\tau_k), \quad \forall k \in [1, 2^N - 1]$$
 (3.1)

The expression (3.1) provides a relation between the set of actual transition levels that are not directly evaluable by the Standard Histogram method and the set of virtual transition levels evaluable by the Standard Histogram method. Since the virtual converter *GADC* now contains the non-linearity of the NL - AWG generator, its virtual transition levels $\{\tau_k\}$ are modified by $\Psi(\cdot)$ with respect to those of the original ADC under test, $\{t_k\}$.

The model for the application of the DH method is depicted in Figure 3.4, where $v(t) = x(t) + \Psi(x(t))$ is the signal generated by NL - AWG and the aim of the adder, named as d, is to introduce a modification in the NL - AWG function by adding a constant offset between the two distorted signals that will excite the ADC under test, to build the two histograms that allow to establish a set of relations to obtain the non-linearity parameters of the ADC

3.2. A proposal for the Non-Linearity estimation based on the Double Histogram method



FIGURE 3.3: Details on the relationship between the actual and the measured transition leves

under test. Thus, the input signal to obtain a Histogram 1, from now on designated as H1, can be expressed as:

$$u(t) = v(t) + d_1 (3.2)$$

And for a Histogram 2, from now on designed as H2:

$$u(t) = v(t) + d_2 (3.3)$$

Where $d = d_1 - d_2$ is the offset applied between the input signals. The criteria for the choice of the *d* value is that it has to be large enough to discern it from the quantization noise and small enough to avoid an excessive loss of the converter input range when the input signal is shifted for the construction of the second histogram.

Proceeding with the test set-up model proposed in Figure 3.2, from H1 is obtained a set of virtual transition levels $\{\tau_k^{(1)}\}$ corresponding to a virtual



FIGURE 3.5: Example of the DH method application using a sine-wave input signal

converter $GADC_1$, and from H2 is obtained a set of virtual transition levels $\{\tau_k^{(2)}\}\$ corresponding to a virtual converter $GADC_2$, since the introduccion of the offset has modified the non-linear function of the NL-AWG. Figure 3.5 depicts an example of the DH method application using a sine-wave input signal, showing the two histograms constructed from each output data and the two set of virtual transition levels evaluated from them. Applying (3.1) to the excitation signals (3.2) and (3.3) of the DH method:

$$u(x = \tau_k^{(1)}) = t_k = f(\tau_k^{(1)}) + d_1$$
(3.4)

$$u(x = \tau_k^{(2)}) = t_k = f(\tau_k^{(2)}) + d_2$$
(3.5)

Matching (3.4) to (3.5) through the actual transition levels t_k of the ADC under test:

$$t_k = f(\tau_k^{(1)}) + d_1 = f(\tau_k^{(2)}) + d_2$$
(3.6)

applicable in $\forall k \in [k_{min}, k_{max}] \subseteq [1, 2^N - 1]$, indicating the code range $[k_{min}, k_{max}]$ the result of a possible loss of input range when applying the signal shift, leading to a reduction of the code range in which the method is applicable and, consequently, to a loss of information of the Integral Non-linearity of the ADC under test in those codes lost. Our proposal for the calculation of the virtual transition levels so that the application of the method covers the full input range of the ADC under test will be shown below, in the section 3.2.2.

3.2.1 Adaptation to a non-stationary test environment

The expression (3.6) assumes that during data capture for H1 and H2 there are no time drifts in the measurement set-up or that data capture is so fast that such drifts are negligible during acquisition. But the application of (3.6) in a non-stationary test environment and in which the data capture is slow enough to be affected by its time drifts will lead to systematic estimation errors in the transition levels and thus in the estimation of the static non-linearity parameters of the ADC under test. It is impossible to guarantee that time variations do not exist in a real test environment. Careful design of the measurement set-up can minimise such time drifts and their effects, but never completely eliminate them. In addition, design can be difficult and costly, requiring time-consuming and expensive test equipments.

Our proposal is a solution using a general DH-based algorithm that includes and corrects for the above possible effects. The starting hypothesis is based on the assumption that, during the test for H1 and the test for H2, the output signal of the non-linear generator NL - AWG, v(t), is affected in each case by an effective gain α_i and offset β_i with i = 1 to 2 whose values depend on the offset d_i applied in each standard histogram H1 and H2 and whose ideal values are the unity gain and the offset values d_i applied for each data set, i.e. those of a test environment without time drifts. That is, the inclusion of the adder d in the nonlinear generator signal path introduces effective variations in the offset and gain of the generated signal, depending on the offset applied by the adder. A schematic of our proposed model is depicted in Figure 3.6. Mathematically it is expressed as:



FIGURE 3.6: Non-Linear AWG model for an ADC nonstationary test set-up

$$u(t) = \alpha_i \cdot v(t) + \beta_i \tag{3.7}$$

with $\alpha_i \approx 1$ and $\beta_i \approx d_i$.

If the ADC under test is now excited with a signal of the form written in (3.7) and the Double Histogram method is applied, using the expression (3.1) the following relations are obtained:

$$u(x = \tau_k^{(1)}) = t_k = \alpha_1 \cdot f(\tau_k^{(1)}) + \beta_1 = \alpha_1(\tau_k^{(1)} + \Psi(\tau_k^{(1)})) + \beta_1$$
(3.8)

$$u(x = \tau_k^{(2)}) = t_k = \alpha_2 \cdot f(\tau_k^{(2)}) + \beta_2 = \alpha_2(\tau_k^{(2)} + \Psi(\tau_k^{(2)})) + \beta_2$$
(3.9)

$$t_k = \alpha_1 \cdot f(\tau_k^{(1)}) + \beta_1 = \alpha_2 \cdot f(\tau_k^{(2)}) + \beta_2$$
(3.10)

$$t_k = \alpha_1(\tau_k^{(1)} + \Psi(\tau_k^{(1)})) + \beta_1 = \alpha_2(\tau_k^{(2)} + \Psi(\tau_k^{(2)})) + \beta_2$$
(3.11)

 $\forall k \in [k_{min}, k_{max}] \subseteq [1, 2^N - 1].$

Signal Waveform	$Q_k = h(\tau_k; A, C)$	$\tau_k = h^{-1}(Q_k; A, C)$
Ramp	$\frac{\tau_k - C}{2A}$	$C + 2A \cdot Q_k$
Triangular	$\frac{\tau_k - (C-A)}{2A}$	$C - A \cdot (1 - 2Q_k)$
Sinusoidal	$1 - \frac{1}{\pi} \arccos(\frac{\tau_k - C}{A})$	$C - A \cdot \cos(\pi Q_k)$
Exponential	$\frac{1}{(T/Tau)} ln(\frac{2A/1 - e^{-(T/Tau)}}{(C-A) + 2A/1 - e^{-(T/Tau)} - \tau_k})$	$(C-A) + 2A \cdot (\frac{1-e^{-(T/Tau)Q_k}}{1-e^{-(T/Tau)}})$

 TABLE 3.1: Relations between signal waveform and its amplitude cumulative probability distribution.

3.2.2 Proposal for the histogram normalisation and the evaluation of the two set of virtual transition levels in Double Histogram methods

Obtaining each set of virtual transition levels $\{\tau_k^{(1)}\}\$ and $\{\tau_k^{(2)}\}\$ is done by applying the Standard Histogram Method to the histograms of the output data H1 and H2 respectively, where the evaluation of the transitions is based on the calculation of the cumulative probability distribution of each output code, henceforth denoted as Q_k . The function defining the cumulative probability distribution per code is set by the waveform of the excitation signal to the ADC. In addition, this function for each code depends on the transition level of the code and the offset and amplitude parameters of the input signal. Mathematically for the *GADC*:

$$Q_k = h(\tau_k; A, C), \quad \forall k \in [1, 2^N - 1]$$
 (3.12)

where h(x; A, C) is the function defining the cumulative probability distribution for an assumed ideal waveform, *A* is its peak amplitude and *C* its DC voltage offset.

Isolating from (3.12) the virtual transition levels:

$$\tau_k = h^{-1}(Q_k; A, C), \quad \forall k \in [1, 2^N - 1]$$
(3.13)

Table 3.1 shows the expression to obtain the transitions leves by the cumulative probability distribution for some signal waveforms.

On the other hand, the cumulative probability distribution per code is calculated through the histogram of the output codes:

$$Q_k = \sum_{i=0}^{k-1} p_i, \quad \forall k \in [0, Mcod]$$
(3.14)

where $Mcod = 2^N - 1$ is the maximum code, $p_i \approx H_i/H_c$ is the estimation of the occurrence probability of code *i*, H_i is the number of collected samples of code *i* and $H_c = \Sigma_i H_i$ is the total number of collected data.

So that the virtual transition levels can be calculated from (3.13) if the amplitude *A* and the offset *C* are known. Our proposal for obtaining the virtual transition levels is based on the following two points:

• Test in a saturated state of the ADC: The amplitude and offset values of the input signal and the offset value *d* must be such that, both for the construction of the histogram H1 and for the construction of the histogram H2, the ADC is always saturated. This ensures that the full input range of the converter is covered, running through its entire set of transition levels and hence $[k_{min}, k_{max}] = [1, 2^N - 1]$.

If the offset *d* to be applied is such that it is not possible to cause saturation at one of the extremes of the code range of the ADC under test, then it is necessary to impose a fictitious saturation on the output data.

• Normalisation of the Standard Histogram Method (Measurement and Technical, 2011): Knowledge of the amplitude and offset parameters is necessary to evaluate (3.13). According to our model, the virtual transition levels correspond to those of the virtual converter *GADC* and are obtained through the application of the virtual signal generated by the virtual source *VS*, not accessible to us and, therefore, without the possibility of measuring exactly the parameters that define it. To overcome this problem, a normalisation process is used in the range of the virtual transition levels.

The proposed process is as follows:

First, the ADC is excited with a signal that saturates its input range and from output data the histogram H1 is constructed. From (3.14) the set $Q_k^{(1)}$ is obtained. In order to evaluate the virtual transition levels from (3.13) it is necessary to know the amplitude and offset values of the signal generated by the virtual source *VS*, which are respectively called A_{VS} and C_{VS} :

$$\tau_k^{(1)} = h^{-1}(Q_k^{(1)}; A_{VS}, C_{VS}), \quad \forall k \in [1, 2^N - 1]$$
(3.15)

In (3.15) is where the normalisation process will be carried out, moving the set of virtual transition levels $\{\tau_k^{(1)}\} \subseteq [\tau_1^{(1)}, \tau_{Mcod}^{(1)}]$ to, for example, a fixed normalised range by assigning $\tau_1^{(1)} = -1$ and $\tau_{Mcod}^{(1)} = 1$. Then $\{\tau_k^{(1)}\} \subseteq [-1, 1] \quad \forall k \in [1, 2^N - 1].$

Under these conditions, it is possible to calculate a normalised amplitude $\overline{A_{VS}}$ and offset $\overline{C_{VS}}$ by solving the two equations with two unknowns system obtained from (3.13), evaluated at the extreme normalised virtual transition levels:

$$-1 = h^{-1}(Q_1^{(1)}; \overline{A_{VS}}, \overline{C_{VS}})$$

$$1 = h^{-1}(Q_{Mcod}^{(1)}; \overline{A_{VS}}, \overline{C_{VS}})$$
(3.16)

And using these $\overline{A_{VS}}$ and $\overline{C_{VS}}$ values, the rest of the normalised virtual transition levels $\{\tau_k^{(1)}\}$ from H1:

$$\tau_k^{(1)} = h^{-1}(Q_k^{(1)}; \overline{A_{VS}}, \overline{C_{VS}}), \quad \forall k \in [2, 2^N - 2]$$
(3.17)

Secondly, the H2 histogram is constructed by exciting the ADC with the same signal as for the H1 histogram but adding the offset *d* and always keeping the saturation condition for the ADC. As the amplitude and offset parameters of the virtual signal given by the virtual generator *VS* have not changed from one test to the other, the new virtual transition levels $\{\tau_k^{(2)}\}$ are calculated using the values $\overline{A_{VS}}$ and $\overline{C_{VS}}$ evaluated from (3.16):

$$\tau_k^{(2)} = h^{-1}(Q_k^{(2)}; \overline{A_{VS}}, \overline{C_{VS}}), \quad \forall k \in [1, 2^N - 1]$$
(3.18)

where $Q_k^{(2)}$ is the accumulated probability distribution for H2 and has been obtained from the second set of output data by applying (3.14).

3.2.3 Enhanced DH method: Application of the generalised Double Histogram model under a non-stationary test environment by obtaining the non-linearity Ψ of the non-linear generator

The aim of this section is to show how to calculate the set of actual transition levels of the ADC under test, $\{t_k\}$, from the solution of the set of relations (3.11) obtained from our set-up model under a non-stationary test environment and considering the non-linearity function $\Psi(\cdot)$ of the non-linear generator NL - AWG as an unknown of the system. That is, the estimation of the set of real transitions will be handled from the initial proposal of (Jin et al., 2005a), where the construction of the two histograms H1 and H2 and their subsequent processing will allow to evaluate the nonlinearity $\Psi(\cdot)$ of the generator, to remove its contribution from the estimated actual transition levels. This procedure, called SEIR (Stimulus Error Identification and Removal) by its authors, is described in detail in Appendix (B).

The algorithm developed in this section was presented in the paper (Jalon, Rueda, and Peralias, 2009).

First of all, expression (3.11) is rewritten as follows:

$$\tau_{k}^{(1)} + \Psi(\tau_{k}^{(1)}) = \gamma(\tau_{k}^{(2)} + \Psi(\tau_{k}^{(2)})) + \beta, \quad \forall k \in [k_{min}, k_{max}] \subset [1, 2^{N} - 1]$$
(3.19)
Being $\gamma = \alpha_{2}/\alpha_{1}$ y $\beta = (\beta_{2} - \beta_{1})/\alpha_{1}$.

The virtual transition levels $\{\tau_k^{(1)}\}$ and $\{\tau_k^{(2)}\}$ are estimated as explained in section 3.2.2 by using the Standard histogram method to H1 applying (3.17) and to H2 applying (3.18) respectively, so they are known values of the system of equations. In addition, if the input signals always saturate the input range of the ADC, the application code range is $\forall k \in [k_{min}, k_{max}] =$ $[1, 2^N - 1]$

Regarding the non-linearity of the NL - AWG generator $\Psi(\cdot)$, is followed the proposal of (Jin et al., 2005a) to express it as a finite series of Mp + 1 basis functions { $\psi_i(x)$ } and coefficients { a_j } with j = 0, 1, 2, ..., Mp in the form of:

$$\Psi(x) = \sum_{j=0}^{Mp} a_j \psi_j(x) + e(x)$$
(3.20)

where e(x) represents the part not modeled by the finite parametrisation of Mp + 1 terms. The greater the number Mp of summation terms in the series that constructs the function $\Psi(x)$, the smaller the error e(x) made, so in the developments it is assumed that Mp has been chosen so that e(x) is negligible (Jin et al., 2005a). Replacing (3.20) into (3.19), it is possible to express the latter as a matrix equation of the form:

$$\tilde{\lambda}(\gamma) = [\widehat{\Gamma}(\gamma) \quad \mathbf{1}]\tilde{\mathbf{a}}$$
 (3.21)

where:

$$(\tilde{\lambda})_{k} = \tau_{k}^{(1)} - \gamma \tau_{k}^{(2)}$$

$$(\widehat{\Gamma})_{kj} = \gamma \psi_{j}(\tau_{k}^{(2)}) - \psi_{j}(\tau_{k}^{(1)}), \quad \tilde{\mathbf{a}} = (a_{0}, a_{1}, ..., a_{Mp}, \beta)^{t}$$
(3.22)

Expression (3.21) is a nonlinear system of equations, with $k_{max} - k_{min}$ equations and Mp + 3 unknowns: Mp + 1 unknowns corresponding to the coefficients a_j that parameterise the function $\Psi(\cdot)$ and the unknowns γ and β . Our work proposed a solution by means of two meshed Least Squares methods:

- **Step 1** : Let γ_0 be a fixed value for the parameter γ , from which to start. Since γ represents the gain change between the first data acquisition for H1 and the second data acquisition for H2, a suitable option is to choose $\gamma_0 = 1$, which is its ideal value when there has been no gain change between the two data acquisitions. Substituting γ_0 in (3.21) and solving by Least Squares method, the set of parameters $\tilde{a}(\gamma_0)$ is obtained.
- **Step 2** : Using the coefficients $\{a_j(\gamma_0)\}$, a set of transitions levels $\{\tilde{t}_k(\gamma_0)\}$ is calculated from (3.11):

$$\tilde{t}_{k}(\gamma_{0}) = \tau_{k}^{(1)} + \sum_{j=0}^{Mp} a_{j}(\gamma_{0})\psi_{j}(\tau_{k}^{(1)})$$
(3.23)

Then, the Integral Non-Linearity set $INL_k^{(UC)}(\gamma_0)$ is estimated from its definition:

$$INL_{k}^{(UC)}(\gamma_{0}) = (\tilde{t}_{k}(\gamma_{0}) - l_{k})/q$$
(3.24)

where the super-index UC (Un-Corrected) indicates that INL has not yet been corrected for gain and offset contributions, $q = (R^+ - R^-)/2^N$



FIGURE 3.7: Example of the INL norm evolution versus γ

is the quantum or LSB of the ADC under test and $\{l_k\} = \{R^- + qk\}$ is the set of ideal transition levels.

- **Step 3** : An offset and gain correction process of the vector $INL_k^{(UC)}(\gamma_0)$ is done, to remove linear contributions from our calculations ((Measurement and Technical, 2011) and Appendix A). This process allow to cancel the errors introduced by the use of an non-accurate offset value. The new vector is designed as $INL_k^{(C)}(\gamma_0)$, indicating the super-index C that the INL is corrected for gain and offset contributions.
- Step 4 : Finally, the above step-by-step procedure is repeated for different values of γ . The second Least Squares process consists of minimising with respect to the γ parameter the norm of the $INL_k^{(C)}(\gamma)$ vector. The Integral Non-Linearity vector resulting from this minimisation is the final adopted estimate for the INL of the ADC under test (see Figure 3.7):

$$INL_{k} = INL_{k}^{C}(\gamma^{*}), \quad \gamma^{*} = min_{\gamma}[\parallel INL_{k}^{C}(\gamma) \parallel]$$
(3.25)

The following section will explain and develop a simple proposal based on the DH method, called Simplified Double Histogram or SDH method. The expression (3.6) is of great importance for this, because it will allow to establish geometric relations between real transition levels $\{t_k\}$ and virtual transition levels $\{\tau_k^{(1)}\}$ and $\{\tau_k^{(2)}\}$. Later, the method will be generalised to a non-stationary test environment and will be referred to as Extended SHD or ESHD.

3.3 A Simplified algorithm based on the Double Histogram method

This section presents a simple approach to estimate the Integral Non-Linearity in high resolution ADCs based on the Double Histogram that was introduced in the papers (Jalon and Peralias, 2009; Jalon and Peralias, 2010). It is divided into a first part where the algorithm is developed under stationary test conditions and a second part where the algorithm is developed under time drifts in the input signal parameters assuming an adder model that takes them into account.

3.3.1 SDH: A Simplified algorithm based on the Double Histogram method applied on a stationary set-up

The simplified algorithm that will be developed in this section to estimate the Integral Non-Linearity parameter of high resolution ADCs, and referred to as Simplified DH or SDH from now on, was presented in (Jalon and Peralias, 2009; Jalon and Peralias, 2010) and is based on the two-histogram test with the typical set-up that has already been shown in Figure 3.4. Starting from the expression (3.6), as an innovation, the algorithm proposed here obtains a local geometric relation between the virtual transition levels τ_k , τ_{k+1} and the code width of the ADC under test $w_k = t_{k+1} - t_k$, through the derivative of the curve f(x) and its approximation to the slope of this curve. Once the set $\{w_k\}$ is known, it is possible to evaluate the Differential Non-Linearity (DNL) parameter of the ADC under test through the expression ((Measurement and Technical, 2011) and Appendix A):

$$DNL_k = \frac{w_k}{q} - 1, \quad \forall k \in [1, 2^N - 2]$$
 (3.26)

And the INL parameter using the relationship:

$$INL_k = \sum_{j=1}^{k-1} DNL_j, \quad \forall k \in [1, 2^N - 1]$$
 (3.27)

where $q = (R^+ - R^-)/2^N$ is the quantum or LSB of the ADC under test.

Figure **??** shows the theoretical deduction flow to establish the SDH test procedure.



FIGURE 3.8: Theoretical deduction flow to establish the SDH test procedure

The INL evaluated from (3.27) contains in its value, apart from the nonlinearity component of the ADC, a linear contribution due to gain and offset errors. The linear contribution is obtained by fitting the vector or set $\{INL_k\}$ to the equation of a straight line. This fitting can be performed by (Measurement and Technical, 2011):

- The best-fit line method, using a least-squares fit technique.
- The terminal-based method, where the straight line is the one joining the two values of INL at the extreme codes.

The final INL is the one corrected from offset and gain contributions (Measurement and Technical, 2011). In the later examples of both simulated and experimental applications, it will be always represented as the INL the one corrected using its best-fit line by the least squares method.



FIGURE 3.9: Geometrical relationships between the k-th code width, the two sets of virtual transition levels and the offset *d*

Consider first Figure 3.9, which shows the geometric relationships between the real transition levels of the ADC under test $\{t_k\}$ and the virtual transition levels obtained by the histogram H1 and the histogram H2, $\{\tau_k^{(1)}\}$ and $\{\tau_k^{(2)}\}$ respectively. Remember that the histograms H1 and H2 have been obtained by modifying the non-linear function of the NL-AWG generator, f(x), by adding the offset d at the output of the generator, satisfying (3.6) $\forall k \in [k_{min}, k_{max}] \subset [0, 2^N - 1]$. Without loss of generality, in Figure 3.9 the shifted function has been represented as g(x) = f(x) + d. Notice that the derivatives of the functions f(x) and g(x) coincide, since they differ in a constant d. Focusing on the functions f(x) and g(x) at each interval of the virtual transition levels $[\tau_k^{(i)}, \tau_{k+1}^{(i)}]$, intervals that are univocally related to the interval $[t_k, t_{k+1}]$ and in a high resolution converter will be very small, it is possible to apply the three-point formula to approximate a function derivative from two evaluations of that function:

$$f'(c) \approx \frac{f(x+h) - f(x-h)}{2h}$$
 (3.28)

Defining $\xi_k^{(i)}$ as the central point of each interval of the virtual transition levels in the code *k*, evaluating (3.28) at this central point (P1, P2 and P3 in Figure 3.9) we obtain for each histogram test H1 and H2 respectively:

$$f'(\xi_k^{(1)}) \approx \frac{f(\tau_{k+1}^{(1)}) - f(\tau_k^{(1)})}{\tau_{k+1}^{(1)} - \tau_k^{(1)}} = \frac{t_{k+1}^{(1)} - t_k^{(1)}}{\tau_{k+1}^{(1)} - \tau_k^{(1)}}$$
(3.29)

$$g'(\xi_k^{(2)}) = f'(\xi_k^{(2)}) \approx \frac{f(\tau_{k+1}^{(2)}) - f(\tau_k^{(2)})}{\tau_{k+1}^{(2)} - \tau_k^{(2)}} = \frac{t_{k+1}^{(2)} - t_k^{(2)}}{\tau_{k+1}^{(2)} - \tau_k^{(2)}}$$
(3.30)

 $\forall k \in [k_{min}, k_{max}] \subset [1, 2^N - 2] \text{ and where } \xi_k^{(i)} = (\tau_{k+1}^{(i)} + \tau_k^{(i)})/2.$

Replacing in the above expressions by the code width $w_k = t_{k+1} - t_k$, $\forall k \in [k_{min}, k_{max}] \subset [1, 2^N - 2]$ is obtained:

$$f'(\xi_k^{(1)}) \approx \frac{w_k}{\Omega_k^{(1)}}$$
 (3.31)

for H1 and where $\Omega_k^{(1)} = \tau_{k+1}^{(1)} - \tau_k^{(1)}$ is the virtual code width for the virtual ADC *GADC*₁.

$$f'(\xi_k^{(2)}) \approx \frac{w_k}{\Omega_k^{(1)}}$$
 (3.32)

for H2 and where $\Omega_k^{(2)} = \tau_{k+1}^{(2)} - \tau_k^{(2)}$ is the virtual code width for the virtual ADC *GADC*₂.

Isolating the code width from (3.31) and (3.32):

$$w_k \approx f'(\xi_k^{(1)}) \cdot \Omega_k^{(1)} \tag{3.33}$$

$$w_k \approx f'(\xi_k^{(2)}) \cdot \Omega_k^{(2)} \tag{3.34}$$

Up to now the derivatives have been obtained with the sets derived from the histograms. Now they will be related to the *d* displacement of the input. For this purpose consider now the Figure 3.10. The derivatives (3.31) and (3.32) can be evaluated through the slope traced at the points $f(\xi_k^{(1)})$ and $f(\xi_k^{(2)})$ respectively, using the relationship between these two nearby points on the curve f(x) and the displacement *d*. For this purpose, a finite difference will be applied as an approximation to the derivatives. In the case of the slope at $f(\xi_k^{(1)})$ (P1 in Figure 3.10), the Backward-Difference formula is applied:



FIGURE 3.10: Errors in the incremental derivatives at two close points

$$f'(x) \approx \lim_{h \to 0} \frac{f(x) - f(x - h)}{h}$$
 (3.35)

where $x = \xi_k^{(1)}$ and $h = \xi_k^{(1)} - \xi_k^{(2)}$.

And in the case of the slope at $f(\xi_k^{(2)})$ (P3 in Figure 3.10), the Forward-Difference formula is applied:

$$f'(x) \approx \lim_{h \to 0} \frac{f(x+h) - f(x)}{h}$$
 (3.36)
where $x = \xi_k^{(2)}$ and $h = \xi_k^{(1)} - \xi_k^{(2)}$.

In both cases, the obtained approximation is the same value:

 $f'(\xi_k^{(1)}) \approx f'(\xi_k^{(2)}) \approx \frac{d}{\delta_k}$ (3.37) being $\delta_k = \xi_k^{(1)} - \xi_k^{(2)}$.

If the error term ε_k is introduced into the Backward-Difference formula and the error term e_k is introduced into the Forward-Difference formula to improve the approximation of the derivatives, neglecting second and higher order terms in the error, then (3.37) becomes:
$$f'(\xi_k^{(1)}) \approx \frac{d}{\delta_k - \varepsilon_k} \approx \frac{d}{\delta_k} (1 + \frac{\varepsilon_k}{\delta_k})$$
 (3.38)

$$f'(\xi_k^{(2)}) \approx \frac{d - e_k}{\delta_k} \approx \frac{d}{\delta_k} (1 - \frac{e_k}{\delta_k})$$
 (3.39)

Replacing (3.38) in (3.33) and replacing (3.39) in (3.34):

$$w_k \approx \frac{d \cdot \Omega_k^{(1)}}{\delta_k} (1 + \frac{\varepsilon_k}{\delta_k})$$
 (3.40)

$$w_k \approx \frac{d \cdot \Omega_k^{(2)}}{\delta_k} (1 - \frac{e_k}{\delta_k})$$
 (3.41)

As the distance between the curves gets closer, which is equivalent to a smaller offset d, the points $\xi_k^{(1)}$ and $\xi_k^{(2)}$ will get closer together and the differences between the derivatives (3.38) and (3.39) will decrease. This means if the distance between the curves, d, is small enough to assume the change in its curvature negligible when moving from the point $\xi_k^{(1)}$ to the point $\xi_k^{(2)}$, then it is possible to consider, in a first-order approximation, $\varepsilon_k \approx e_k$. So that the offset must be low enough to avoid errors due to the difference between the derivatives on the two points, but must be high enough to obtain a noticeable distance between the curves for method application. Under this conditions:

$$w_k \approx \frac{d \cdot \Omega_k^{(1)}}{\delta_k} (1 + \frac{\varepsilon_k}{\delta_k}) = w_k^{(1)}$$
(3.42)

$$w_k \approx \frac{d \cdot \Omega_k^{(2)}}{\delta_k} (1 - \frac{\varepsilon_k}{\delta_k}) = w_k^{(2)}$$
(3.43)

Where $w_k^{(1)}$ is the expression obtained for the code width from the Backward-Difference formula and $w_k^{(2)}$ is the expression obtained from the Forward-Difference formula. The mean value of the two available approaches is:

$$\hookrightarrow \quad w_k^* = \frac{w_k^{(1)} + w_k^{(2)}}{2} \approx \frac{d \cdot (\Omega_k^{(1)} + \Omega_k^{(2)})}{2\delta_k}, \quad \forall k \in [k_{\min}, k_{\max}] \subset [1, 2^N - 2]$$
(3.44)

where the errors from (3.42) and (3.43) in a first-order approximation are compensated:

$$w_k^* = \frac{w_k^{(1)} + w_k^{(2)}}{2} \approx \frac{w_k(1 - \varepsilon_k/\delta_k) + w_k(1 + \varepsilon_k/\delta_k)}{2} = w_k$$
(3.45)

The expression (3.44) is a very simple formula to calculate the code width set $\{w_k\}$ of the ADC under test and is fully known once the virtual transition levels have been estimated through the histograms H1 and H2 as explained in section 3.2.2, by using the Standard histogram method to H1 applying (3.17) and to H2 applying (3.18) respectively. In addition, if the input signals always saturate the input range of the ADC, the application code range is $\forall k \in [k_{min}, k_{max}] = [1, 2^N - 1]$. Applying (3.44) to the calculation of the DNL by means of (3.26) and this later to the calculation of the INL by means of (3.27), the integral non-linearity desired is the one obtained after correcting the $\{INL_k\}$ vector from offset and gain contributions. Errors in the amplitude and offset values of the input signals do not induce errors. So, in the gain and offset correction last process, are cancelled the errors introduced by the use of a non-accurate *d* offset value.

It is also important to highlight that the model proposed here makes no assumptions about the type of waveform that excites the ADC under test, as the two sets of virtual transition levels are estimated using the Standard Histogram Method in each case. This degree of freedom in the choice of the type of test input waveform is a great advantage when designing a measurement set-up. Traditionally, the standard histogram test uses the ramp or sine-wave signal as stimulus signals to the ADC under test (Measurement and Technical, 2011), but it is possible to apply the method to other waveforms as long as their accumulated probability function is known. This will be explained in the next section and illustrated by the simulated experiments shown in the Simulation Experiments Resuls section.

3.3.2 Extended SDH method: Generalisation of the SDH method in a non-stationary test environment



FIGURE 3.11: Theoretical deduction flow to establish the ESDH test procedure

Figure 3.11 shows the theoretical deduction flow to establish the SDH test procedure. As explained in the section on the Simplified Double Histogram or SDH algorithm, the objective is to find the geometric relations that relate the set of real transition levels of the ADC under test $\{t_k\}$ and the two sets of virtual transition levels corresponding to the virtual converters $GADC_1$ and $GADC_2$, $\{\tau_k^{(1)}\}$ and $\{\tau_k^{(2)}\}$ respectively. As is well known, the virtual transition levels are estimated as explained in section 3.2.2 being known values for the estimation process. In addition, if the input signals always saturate the input range of the ADC, the application code range is $\forall k \in [k_{min}, k_{max}] = [1, 2^N - 1]$ This will be done on the basis of the expression (3.10). The Figure 3.12 is an analogous figure to Figure 3.9, but now the



FIGURE 3.12: Geometrical relationships between the k-th code width, the two sets of virtual transition levels and the offset d_k using an effective change of gain and offset model

function f(x) of the non-linear generator NL-AWG is affected by a different effective gain and offset between the first data acquisition to obtain H1 and the second data acquisition to obtain H2:

$$g_1(x) = \alpha_1 \cdot f(\tau_k^{(1)}) + \beta_1 \tag{3.46}$$

$$g_2(x) = \alpha_2 \cdot f(\tau_k^{(2)}) + \beta_2 \tag{3.47}$$

Isolating f(x) from (3.46) and replacing in (3.47) :

$$g_2(x) = \gamma \cdot g_1(x) + (\beta_2 - \gamma \cdot \beta_1) \tag{3.48}$$

where $\gamma = \alpha_2 / \alpha_1$.

The mathematical process that now continues is analogous to the one developed earlier in SDH, since it is again possible to apply (3.28) and similarly obtain the relationships in the centre of virtual intervals $\{\xi_k^{(i)}\}$:

$$g_{1}'(\xi_{k}^{(1)}) \approx \frac{f(\tau_{k+1}^{(1)}) - f(\tau_{k}^{(1)})}{\tau_{k+1}^{(1)} - \tau_{k}^{(1)}} = \frac{t_{k+1}^{(1)} - t_{k}^{(1)}}{\tau_{k+1}^{(1)} - \tau_{k}^{(1)}}$$
(3.49)

$$g_{2}'(\xi_{k}^{(2)}) \approx \frac{f(\tau_{k+1}^{(2)}) - f(\tau_{k}^{(2)})}{\tau_{k+1}^{(2)} - \tau_{k}^{(2)}} = \frac{t_{k+1}^{(2)} - t_{k}^{(2)}}{\tau_{k+1}^{(2)} - \tau_{k}^{(2)}}$$
(3.50)

where $\xi_k^{(i)} = (\tau_{k+1}^{(i)} + \tau_k^{(i)})/2$. Substituting by code width of the ADC under test w_k and by the virtual code widths $\Omega_k^{(i)}$:

$$g'_1(\xi_k^{(1)}) \approx \frac{w_k}{\Omega_k^{(1)}}$$
 (3.51)

$$g'_{2}(\xi_{k}^{(2)}) \approx \frac{w_{k}}{\Omega_{k}^{(2)}}$$
 (3.52)

Calculating the derivative of the expression (3.48):

$$g'_{2}(x) = \gamma \cdot g'_{1}(x)$$
 (3.53)

Both derivatives (3.51) and (3.52) are related by:

$$g'_{2}(\xi_{k}^{(2)}) = \gamma \cdot g'_{1}(\xi_{k}^{(2)})$$
 (3.54)

Replacing (3.54) in (3.52) and isolating w_k :

$$w_k \approx g_1'(\xi_k^{(1)}) \cdot \Omega_k^{(1)}$$
 (3.55)

$$w_k \approx \gamma \cdot g_1'(\xi_k^{(2)}) \cdot \Omega_k^{(2)}$$
(3.56)

On the other hand, as it was done in the SDH algorithm under a stationary test shown in Figure 3.10, it is possible to evaluate the previous derivatives $g'_1(\xi_k^{(1)})$ and $g'_1(\xi_k^{(2)})$ by applying 3.31 and 3.32 under the assumption of two very close points of the curve, now being the applied offset designated as d_k since its value will depend on the code k on which the calculation is being performed, due to the effective changes in gain and offset produced between the first and the second data capture. The new relationships obtained are:

$$w_k \approx \frac{d_k \cdot \Omega_k^{(1)}}{\delta_k} (1 + \frac{\varepsilon_k}{\delta_k}) = w_k^{(1)}$$
(3.57)

$$w_k \approx \gamma \cdot \frac{d_k \cdot \Omega_k^{(2)}}{\delta_k} (1 - \frac{\varepsilon_k}{\delta_k}) = w_k^{(2)}$$
 (3.58)

As in (3.44) and (3.45), it is possible to calculate the code width as the mean value of the two previous ones:

$$\hookrightarrow \quad w_k(\gamma) \approx w_k^* = \frac{w_k^{(1)} + w_k^{(2)}}{2} = \frac{d_k \cdot (\Omega_k^{(1)} + \gamma \cdot \Omega_k^{(2)})}{2\delta_k}$$
(3.59)
$$\forall k \in [k_{min}, k_{max}] \subset [1, 2^N - 1] \text{ and where } d_k = g_1(\xi_k^{(1)}) - g_1(\xi_k^{(2)}).$$

The equation (3.59) is analogous to that obtained in SDH but now depends on the γ factor and the displacement d_k that depends on the code k in which it is being calculated. So, in order to solve (3.59) and obtain the set of code widths of the ADC under test, it is necessary to rewrite the displacement d_k by evaluating $g_1(\xi_k^{(1)})$ and $g_1(\xi_k^{(2)})$:

On one hand:

$$g_1(\xi_k^{(1)}) = c_k = t_k + (w_k/2)$$
(3.60)

where c_k is the midpoint of the interval $[t_k, t_{k+1}]$ of the ADC under test.

On the other hand, using (3.48) is obtained:

$$g_1(\xi_k^{(2)}) = (1/\gamma) \cdot (g_2(\xi_k^{(2)}) - (\beta_2 - \gamma \cdot \beta_1))$$
(3.61)
where $g_2(\xi_k^{(2)}) = c_k = t_k + (w_k/2).$

Finally the displacement d_k is rewritten as:

$$\hookrightarrow \quad d_k = a \cdot t_k + b + a \cdot (w_k/2) \tag{3.62}$$

where $a = 1 - 1/\gamma$ and $b = (1/\gamma) \cdot \beta_2 - \beta_1$.

Replacing (3.62) in (3.59):

$$\hookrightarrow \quad w_k(\gamma) \approx (a(\gamma) \cdot t_k + b(\gamma)) \cdot \frac{F_k(\gamma)}{1 - ((a(\gamma)/2) \cdot F_k(\gamma))} \tag{3.63}$$

$$\forall k \in [k_{min}, k_{max}] = [1, 2^N - 1], \text{ where } F_k(\gamma) = (\Omega_k^{(1)} + \gamma \cdot \Omega_k^{(2)})/2\delta_k$$

In order to solve (3.63), an iteration process will be applied in which the definition of Integral Non-Linearity will be used, expressed by its definition:

$$INL_k = (t_k - l_k)/q \tag{3.64}$$

where $q = (R^+ - R^-)/2^N$ is the quantum or LSB of the ADC under test and $\{l_k\} = \{R^- + qk\}$ is the set of ideal transition levels.

The following steps show the post-processing procedure adopted to obtain the INL:

- **Step 1** : The effective offsets β_1 and β_2 will be assigned their ideal values, d_1 and d_2 respectively, being $b = (1/\gamma) \cdot d_2 d_1$. Indeed, since $\gamma \approx 1$, it is possible to assume $b \approx d$ as a constant value. These assumptions will not be a source of error in the final estimate, as the INL wanted will be offset and gain corrected.
- Step 2 : Considering a fixed $\gamma = \gamma_0$ value, an iterative process is applied for t_k and w_k in (3.63) starting with the first code and calculating at each iteration step the Integral Non-Linearity INL_k per code from (3.64): The process starts by assigning to the first transition level t_1 its ideal value $l_1 = R^- + q$, which implies $INL_1 = 0$. From (3.63), w_1 is obtained and from this and $t_{k+1} = t_k + w_k$, the second transition level t_2 . Using the value of the second transition level, INL_2 and w_2 are evaluated. So on and so forth until the process is completed in the last code. The result is a vector for the chosen value of γ : $INL_k^{(UC)}(\gamma_0)$.
- **Step 3** : An offset and gain correction process of the vector $INL_k^{(UC)}(\gamma_0)$ is done, to remove linear contributions from our calculations. This process allows to cancel the errors introduced by the use of a non-accurate *b* value. The new vector is designed as $INL_k^{(C)}(\gamma_0)$.
- **Step 4** : Finally, the above is repeated for different values of γ , obtaining different vectors $INL_k^{(C)}(\gamma)$. The Integral Non-Linearity pattern adopted is the one that presents the minimum norm versus γ (Figure 3.7):

$$INL_{k} = INL_{k}^{(C)}(\gamma^{*}), \quad \gamma^{*} = min_{\gamma}[\parallel INL_{k}^{(C)}(\gamma) \parallel]$$
(3.65)

3.3.3 Simulated Experiments

In order to validate the proposed algorithms for estimating the Integral Non-Linearity using non-linear generators, this section shows the results obtained in three different simulated experiments:

- Experiment 1: In this simulated experiment the SHD method will be applied under a stationary test environment.
- Experiment 2: In this simulated experiment the ESHD method will be applied under a non-stationary test environment.
- Experiment 3: In this simulated experiment, the proposed generalised DH solution by obtaining the non-linearity Ψ of the NL-AWG generator will be applied for a non-stationary test environment.

In each of them, the *INL* calculated by the Standard Histogram Method using a pure excitation signal (Measurement and Technical, 2011) will be taken as the reference pattern of the ADC under test. A reference pattern obtained with the same frequency and number of samples as the histograms of the proposed alternative methods is desired, in order to compare them each other.

Experiment 1: Application of SDH method under a stationary test environment

This simulated experiment was presented in the research papers (Jalon and Peralias, 2009; Jalon and Peralias, 2010). The purpose of this experiment is to evaluate by simulation the application of the Simplified Double Histogram (SDH) method to obtain the INL of the ADC under test, using a less linear generator than the converter under test and with the assumption that it is operated in a stationary test environment. To this end, the different blocks of the DH typical set-up shown in Figure 3.4 have been modeled as:

• ADC under test model: it is high-level model of a fully differential Pipeline ADC with 16-bit of resolution, $f_s = 100ksps$ of sampling rate and bipolar input range $[R^-, R^+] = [-0.5V, 0.5V]$, being the Full-Scale value FS = 1V and its $LSB = 1/2^{16} \approx 15.3\mu V$. The ADC model has

such a transfer function that it results in strong discontinuities in the INL pattern. The noise due to both the input signal and the ADC itself, referred to the input, is modeled as an additive white noise of value 2LSB rms.

- Non-linear generator NL-AWG: According to the generator block model in Figure 3.4, the generated input signal by the NL-AWG is the sum of a pure signal *x*(*t*) given by the virtual generator VS and of the non-linear function Ψ(*x*):
 - The pure signal x(t) given by VS has been modeled as the exponentialpulse train shown in Figure 3.13 a), of frequency $f_0 \approx 3.87kHz$. The frequency chosen to perform the simulated experiment is low enough with respect to the sampling frequency f_s of the ADC under test so as not to introduce dynamic effects in the measurements (Measurement and Technical, 2011): $f_0 \ll f_s$. The amplitude and offset parameters has been set to $A_{VS} \approx 0.5V + 5\%$ and $C_{VS} \approx 0.0V$. The time constant of the exponential waveform has been taken twice the *T* period of the signal, $Tau \approx 2T = 2/f_0$, in order to have enough time to capture the unsaturated-zone output codes in each period of the signal.
 - The non-linear function Ψ(x) has been modeled as shown in Figure 3.13 b), a 38th-order polynomial with a range of non-linearity covering 800*LSB* peak-to-peak.

The first histogram H1 is obtained from the output data captured using as excitation signal the exponential waveform given by the non-linear generator above. The second histogram H2 is obtained from the output data captured using the same signal as for H1 but with an added offset of $d = 5.0mV \pm 0.25mV \equiv 328LSB \pm 17LSB$. As 5mV is equivalent to 1% of 0.5V, both histograms have been obtained with the ADC under test saturated. From the histogram H1, applying (3.16) and (3.17), it is obtained the set of virtual transition levels $\{\tau_k^{(1)}\}$ and the amplitude and offset values of the ADC input signal, $\overline{A_{VS}}$, $\overline{C_{VS}}$ normalised to the range [-1, +1]. According to the exponential waveform of the experiment, the function relating such transition levels and the accumulated probability per code is (see Table 3.1):

$$\tau_{k}^{(1)} = h^{-1}(Q_{k}^{(1)}; \overline{A_{VS}}, \overline{C_{VS}}) = (\overline{C_{VS}} - \overline{A_{VS}}) + 2\overline{A_{VS}} \cdot (\frac{1 - e^{-(T/Tau)Q_{k}^{(1)}}}{1 - e^{-(T/Tau)}})$$
(3.66)



FIGURE 3.13: a) Exponential waveform used in the simulated example. b) Non-Linearity function $\Psi(x)$ of the NL-AWG generator

The above set of transition leves results, applying (3.64), in the Integral Non-Linearity pattern shown in Figure 3.14 which, following our model shown in Figure 3.2, is the INL pattern of the *GADC*. This figure plots the vector $\{INL_k\}$ versus the vector of codes $\{k\} \in [1, 2^N - 1]$, and clearly shows that the estimate is essentially the non-linearity of the NL-AWG generator. This means that the use of a single histogram with the above non-linear generator model leads to large errors in the estimation of the Integral Non-Linearity of the ADC under test, since the application of a single Standard Histogram Method practically obtains the non-linearity of the generator, being the non-linearity of the ADC under test embedded in it. This is what can be noticed in Figure 3.14.

From the histogram H2, applying (3.18) and using the same $\overline{A_{VS}}$ and $\overline{C_{VS}}$ values as in (3.66), it is obtained the set of virtual transition levels $\{\tau_k^{(2)}\}$:



FIGURE 3.14: INL estimated by the Standard Histogram method

$$\tau_k^{(2)} = h^{-1}(Q_k^{(2)}; \overline{A_{VS}}, \overline{C_{VS}}) = (\overline{C_{VS}} - \overline{A_{VS}}) + 2\overline{A_{VS}} \cdot (\frac{1 - e^{-(T/Tau)^{(2)}}}{1 - e^{-(T/Tau)}})$$
(3.67)

From the set of virtual transition levels $\{\tau_k^{(1)}\}\$ and the set of virtual transition levels $\{\tau_k^{(2)}\}\$ are calculated the set of virtual code width $\{\Omega_k^{(1)}\}\$, the set of virtual code width $\{\Omega_k^{(2)}\}\$ and δ_k . These are the data required to evaluate, from the SDH equation (3.44), the set of code widths of the ADC under test.

The result obtained from calculating the $\{INL_k\}$ vector using the SDH approach is plotted with a red line in Figure 3.15 a). The black line shows the actual INL of the ADC under test. Figure 3.15 b) shows the error per code for the SDH estimated INL, by the difference between both curves. The maximum error is approximately 0.75*LSB*, being the RMS error 0.2*LSBrms*.

In conclusion, in this simulated experiment it has been possible to estimate accurately, by applying the SDH method which only requires knowledge of the virtual transition levels that have been estimated through the histograms H1 and H2, the Integral Non-Linearity of a 16-bit ADC using a much less linear generator than the device under test, in contrast to the application of a single histogram which leads to erroneous estimates of about 400LSB.

Using the same ADC model and the same non-linear generator model, a new simulated test has been performed by using a sine wave as the input signal to the ADC under test. The pure sine signal x(t) given by the virtual generator VS maintains the previous frequency $f_0 \approx 3.87 kHz$, amplitude



FIGURE 3.15: a) Comparison between the INL estimated by the SDH method using d = 328LSB (red line) and the actual INL (black line). b) Estimated error per code

 $A_{VS} \approx 0.5V + 5\%$ and offset $C_{VS} \approx 0.0V$ conditions. The non-linear function of the generator $\Psi(x)$ remains as described above and shown in Figure 3.13 b). The SDH method will be performed 10 times by sweeping the value of the offset *d* from 50LSB to 500LSB with each step increasing by 50LSB. The purpose of this simulated test is to verify the following:

- The no dependency between the results estimated by the SDH method and test input waveform: using a sinusoidal waveform input, results with an accuracy analogous to that of the previous test are achieved.
- How the error in the INL estimation depends on the offset value *d* applied in the SDH method.

Virtual transition levels are now obtained from the expression:

$$\tau_k = h^{-1}(Q_k; \overline{A_{VS}}, \overline{C_{VS}}) = \overline{C_{VS}} - \overline{A_{VS}}cos(\pi Q_k)$$
(3.68)

Figure 3.16 depicts the rms value of the INL error estimation versus the offset d in LSBs from the previous 10 SDH application. Notice that the accuracy of the estimation is of the order of that of the exponential-pulse train signal. The evolution of the INL estimation error with respect to the value of the offset d is in accordance with the approximations applied in the mathematical development of the SDH algorithm: with a minimum rms error that



FIGURE 3.16: RMS error of the estimated INL versus the offset d (in LSB)

occurs for an offset of $d_{min} \approx 150LSB$, as the value of d increases from this minimum (in the figure we move to the right of 150LSB), difference between the derivatives of the two point (3.38) and (3.39) increases, and estimation errors increase. As the value of d decreases from this minimum (in the figure we move to the left of 150LSB), the points are so close that the displacement between the curves is not noticeable by the SDH method, and estimation errors increase.

Simulated Experiment 2: Application of ESDH under a non-stationary test environment

The purpose of this experiment also introduced in (Jalon and Peralias, 2009; Jalon and Peralias, 2010) is to evaluate by simulation the application of the Extended Simplified Double Histogram ESHD method to obtain the INL of the ADC under test, using a less linear generator than the converter under test and with the assumption that it is operated in a non-stationary test environment. Now, in this simulated experiment, it will be assumed that offset and gain time drifts occur during the first and second collection data. To this end, the different blocks of the DH typical set-up shown in Figure 3.6 have been modeled as:

- ADC under test model: it is high-level model of a fully differential Pipeline ADC with 16-bit of resolution, $f_s = 1Msps$ of sampling rate and bipolar input range $[R^-, R^+] = [-1.0V, 1.0V]$, being the Full-Scale value FS = 2V and its $LSB = 2/2^{16} \approx 30.5\mu V$. This ADC model has such a transfer function that it results in strong discontinuities in the INL pattern and a large number of missing codes. The noise due to both the input signal and the ADC itself, referred to the input, is modeled as an additive white noise of value 2LSB rms.
- Non-linear generator NL-AWG: According to the generator block model in Figure 3.6, the generated input signal by the NL-AWG is the sum of a pure signal *x*(*t*) given by the virtual generator VS and of the nonlinear function Ψ(*x*), but including offset and gain errors because of the adder:
 - The pure signal x(t) given by VS has been modeled as a sine-wave signal, of frequency $f_0 \approx 3.87 kHz$. The frequency chosen to perform the simulated experiment is low enough with respect to the sampling frequency f_s of the ADC under test so as not to introduce dynamic effects in the measurements (Measurement and Technical, 2011): $f_0 \ll f_s$. The amplitude and offset parameters has been set to $A_{VS} \approx 1V + 5\%$ and $C_{VS} \approx 0.0V$.
 - The non-linear function Ψ(x) has been modeled as shown in Figure 3.13 b), a 38th-order polynomial with a range of non-linearity covering 800*LSB* peak-to-peak.
 - The adder has been modeled as a block that introduces a gain factor *α*(*t*) and and offset value *β*(*t*) that varies in time according to

the expressions:

$$\alpha(t) = \alpha_0 \cdot (1 + b_{\alpha}t + c_{\alpha}\hat{u}(t - t_{H2}) + n_{\alpha B}(t))$$
(3.69)

$$\beta(t) = \beta_0 + b_{\beta}t + c_{\beta}\hat{u}(t - t_{H2}) + n_{\beta B}(t)$$
(3.70)

Each of the above expressions consists of a term that varies linearly with time $b_x t$, a term that introduces the finite increment c_x at the instant t_{H2} when the offset is applied by the $\hat{u}(\cdot)$ the Unit Step function, and an unbounded Brownian noise $n_{xB}(t)$, where $x \equiv \alpha$ or β . The following coefficients have been chosen for the simulation: $\alpha_0 = 0.99$, $b_\alpha = 10.7 ppm/s$, $c_\alpha = 1000 ppm$, a standard deviation of $\sigma_{\alpha B} = 10^{-4} ppm$ for each time-step of the α – *Brownian* noise, $\beta_0 = -110 LSB$, $b_\beta = -3 \mu V/s$, $c_\beta = 200 LSB \pm 20 LSB$ and a standard deviation of $\sigma_{\beta B} = 3.10 \mu V$ for each time-step of the β – *Brownian* noise. Figure 3.17 depicts in detail the time evolution of these models during the simulation test, that lasts about 9s and where $t_{H2} \approx 4.5s$.

The first histogram H1 is obtained from the output data captured using as excitation signal the sine-wave v(t) given by the non-linear generator above. During the execution of this part of the test, the time evolution of the gain and offset that the adder has applied to the signal is the one shown in Figure 3.17 for $t < t_{H2}$. The second histogram H2 is obtained from the output data captured using the same signal v(t) as for H1 but now,during the execution of this part of the test, the evolution in time of the gain and offset that the adder has applied to the signal is the one shown in Figure 3.17 for $t < t_{H2}$. In both histograms the saturation of the input range of the ADC under test has been preserved.

From the histogram H1, applying (3.16) and (3.17), it is obtained the set of virtual transition levels $\{\tau_k^{(1)}\}$ and the amplitude and offset values of the ADC input signal, $\overline{A_{VS}}$, $\overline{C_{VS}}$ normalised to the range [-1, +1]. According to the sine waveform of the experiment, the function relating such transition levels and the accumulated probability per code is (see Table 3.1):

$$\tau_k^{(1)} = h^{-1}(Q_k^{(1)}; \overline{A_{VS}}, \overline{C_{VS}}) = \overline{C_{VS}} - \overline{A_{VS}}cos(\pi Q_k^{(1)})$$
(3.71)

From the histogram H2, applying (3.18) and using the same $\overline{A_{VS}}$ and $\overline{C_{VS}}$ values as in (3.66), it is obtained the set of virtual transition levels $\{\tau_k^{(2)}\}$:



FIGURE 3.17: a) Offset and b) relative gain time evolution during the running of the entire example test

$$\tau_k^{(2)} = h^{-1}(Q_k^{(2)}; \overline{A_{VS}}, \overline{C_{VS}}) = \overline{C_{VS}} - \overline{A_{VS}}cos(\pi Q_k^{(2)})$$
(3.72)

From the set of virtual transition levels $\{\tau_k^{(1)}\}\$ and the set of virtual transition levels $\{\tau_k^{(2)}\}\$ are calculated the set of virtual code width $\{\Omega_k^{(1)}\}\$, the set of virtual code width $\{\Omega_k^{(2)}\}\$ and δ_k .

Figure 3.18 a) shows the actual sharp INL pattern and Figure 3.18 b) shows the actual DNL pattern of the ADC under test. Notice the large number of missing codes that exist (DNL = -1). If the SDH method is applied in a first approach, using a fixed offset of d = 200LSB, the INL pattern estimated for the ADC under test is the one shown in Figure 3.18 c). This INL pattern is within the range of approximately +1000*LSB* and -1900*LSB*. That is, the use of the SDH method in the non-stationary test environment here



FIGURE 3.18: a) Actual INL pattern b) Actual DNL pattern of the ADC under test. Non-stationary set-up: Resuls comparinson between c) SDH, d) ESDH and e) interleaved SDH methods

presented leads to large errors in the estimation of the INL pattern.

If the ESDH method is applied, the expression to be computed is (3.63) and within the iterative process developed and explained in the corresponding section above:

- 1. The coefficient $b(\gamma)$ is assumed to be the constant value $b(\gamma) = d = 200LSB$.
- 2. A γ value is set, i. e. $\gamma = 1$.
- 3. The following iterative algorithm is applied:

$$t_1 = 1$$

FOR k = 1 to $2^N - 2$ $INL_k^{(UC)} = t_k - k$ w_k from formula (3.63) $t_{k+1} = t_k + w_k$ ENDFOR $INL_{2^N-1}^{(UC)} = t_{2^N-2} - (2^N - 2)$ where the quantities have been inserted directly in LSBs units.

- 4. The vector $INL_k^{(UC)}$ is gain and offset corrected, obtaining $INL_k^{(C)}$.
- 5. Going back to step 2, the process is repeated by varying the coefficient γ using values close to the unity.
- 6. The norm is calculated for all the vectors $INL_k^{(C)}$ obtained during the above process, adopting as the INL pattern of the ADC under test the one with the minimum norm.

Figure 3.18 d) plots the error per code obtained when the ESDH method is used, calculated as the difference between the actual and the estimated INL patterns. The error is within the range $\pm 0.5LSB$.

So, by applying the ESDH method which only requires knowledge of the virtual transition levels that have been estimated through the histograms H1 and H2, it has been possible to estimate accurately the Integral Non-Linearity of a 16-bit ADC using a much less linear generator than the device under test and in the more real non-stationary test envarionment. Even with an INL pattern as sharp as that of the simulated example ADC and containing a large number of missing codes.

In this simulated experiment, the solution to the set-up time drift problem has also been addressed using the approach proposed in (Jin et al., 2005a; Jin et al., 2005b). In it the two input signals used for the Double Histogram method are L times interleaved following a "common-centroid" distribution sequence according to the Thue-Morse series, as is depicted in Figure 3.19. This process increases the time needed to collect the data by L-2 times, as well as increases the difficulty of the set-up programming to manage the process implementation. The simulation has required L = 128 time slots to obtain the error per code of the same order as the ESDH, and is shown in Figure 3.18 e). In conclusion, the ESDH method, which requires only 2 time slots, has achieved an INL estimation with an accuracy analogous to the proposal in (Jin et al., 2005b), which requires 128 time slots.



FIGURE 3.19: SDH test using L-interleaved Thue-Morse series

Experiment 3: Application of the Enhanced DH method under a non-stationary test environment

The aim of this simulated experiment is to evaluate in a non-stationary test environment the application of the Enhanced DH method from the approximation of (Jin et al., 2005a), where the non-linear contribution of the nonlinear generator is estimated by a parameterisation and then removed from the ADC under test INL calculation (SEIR approach). The simulated experiment was presented in (Jalon, Rueda, and Peralias, 2009). To this end, the different blocks of the DH typical set-up shown in Figure 3.6 have been modeled as:

• ADC under test model: it is high-level model of a fully differential Pipeline ADC with 16-bit of resolution, $f_s = 100ksps$ of sampling rate and bipolar input range $[R^-, R^+] = [-1.0V, 1.0V]$, being the Full-Scale value FS = 2V and its $LSB = 2/2^{16}V$. The actual INL pattern is the same as that of the ADC model chosen for the Simulated Experiment 1.

The noise due to both the input signal and the ADC itself, referred to the input, is modeled as an additive white noise of value 2LSB rms.

- Non-linear generator NL-AWG: According to the generator block model in Figure 3.6, the generated input signal by the NL-AWG is the sum of a pure signal *x*(*t*) given by the virtual generator VS and of the nonlinear function Ψ(*x*), but including offset and gain errors because of the adder:
 - The pure signal x(t) given by VS has been modeled as a sine-wave signal, of frequency $f_0 \approx 3.87 kHz$. The frequency chosen to perform the simulated experiment is low enough with respect to the sampling frequency f_s of the ADC under test so as not to introduce dynamic effects in the measurements (Measurement and Technical, 2011): $f_0 \ll f_s$. The amplitude and offset parameters has been set to $A_{VS} \approx 1V + 5\%$ and $C_{VS} \approx 0.0V$.
 - The non-linear function $\Psi(x)$ has been modeled as shown in Figure 3.13 b), a 38^{th} -order polynomial with a range of non-linearity covering 800LSB peak-to-peak. For the application of the proposed estimation method, the $\Psi(x)$ function has been parametrised using as basis function the set $\{sin(j\pi x)\}$ up to the order Mp = 100.
 - The adder has been modeled as a block that introduces a gain factor *α*(*t*) and and offset value *β*(*t*) that varies in time according to the expressions:

$$\alpha(t) = \alpha_0 \cdot (1 + b_{\alpha}t + c_{\alpha}\hat{u}(t - t_{H2}) + n_{\alpha B}(t))$$
(3.73)

$$\beta(t) = b_{\beta}t + c_{\beta}\hat{u}(t - t_{H2}) + n_{\beta B}(t)$$
(3.74)

Each of the above expressions consists of a term that varies linearly with time $b_x t$, a term that introduces the finite increment c_x at the instant t_{H2} when the offset is applied by the $\hat{u}(\cdot)$ the Unit Step function, and an unbounded Brownian noise $n_{xB}(t)$, where $x \equiv \alpha$ or β . The following coefficients have been chosen for the simulation: $\alpha_0 = 0.99$, $b_\alpha = 1.75ppm/s$, $c_\alpha = 1000ppm$, an accumulated standard deviation of $\sigma_{\alpha B} = 0.9940ppm\sqrt{s}$ for the α – Brownian noise, $b_\beta = -3\mu V/s$, $c_\beta = 200LSB \pm 20LSB$ and an accumulated standard deviation of $\sigma_{\beta B} = 3.10\mu V\sqrt{s}$ for the β – Brownian noise. Figure 3.20 depicts in detail the time evolution of these



FIGURE 3.20: a) Offset and b) relative gain time evolution during the running of the entire example test

models during the simulation test, that lasts about 100*s* and where $t_{H2} \approx 50s$.

The first histogram H1 is obtained from the output data captured using as excitation signal the sine-wave v(t) given by the non-linear generator above. During the execution of this part of the test, the time evolution of the gain and offset that the adder has applied to the signal is the one shown in Figure 3.20 for $t < t_{H2}$. The second histogram H2 is obtained from the output data captured using the same signal v(t) as for H1 but now,during the execution of this part of the test, the time evolution of the gain and offset that the adder has applied to the signal is the one shown in Figure 3.20 for $t < t_{H2}$. In both histograms the saturation of the input range of the ADC under test has been preserved. The virtual transition levels are calculated as already explained in the Experiment 2.



FIGURE 3.21: Non-stationary set-up:a) Estimated INL from DH method approaching the non-linearity generator with Mp=100.b) and c) Comparison between the True INL (red line) and the estimated INL (black line) by applying the proposed Enhanced DH method

If an approach is applied where time drifts are not taken into account, the result of the INL estimation has large errors as shown Figure 3.21 a). In this case the system of equations (3.21) has been solved by only considering $\gamma = 1$. The wrong estimate INL pattern is within the range of approximately +1200*LSB* and -2350*LSB*.

If our proposed solution in subsection 3.2.1 for a non-stationary test environment is applied, the errors in the estimation of the INL pattern are dramatically reduced, as shown Figure 3.21 b) and Figure 3.21 c). The actual and the estimated INL patterns match very closely, with the difference between them being in the range of $\pm 1LSB$.

Chapter 4

Experimental application of the proposed methods on a commercial high-resolution Analog-to-Digital Converter



FIGURE 4.1: AD6644: Picture of the evaluation board including the input signal (BNC connector), the clock signal (SMA connector) and the Logic Analyser connections

The objetive of this chapter is to evaluate the application of the SSA method (based on a spectral approach) and the SDH, ESDH and EDH methods (based on a double histogram approach) for the Integral Non-Linearity estimation of a high-resolution commercial ADC. The device under test is the highperformance 14-bit, 65Msps AD6644 from Analog Devices (Devices, 2007). To simplify the design and the assembly of the measurement set-up, the AD6644 converter has been measured on its evaluation board, also from Analog Devices. A picture of the evaluation board is shown in Figure 4.1. The schematic of the evaluation board can also be found in the datasheet of the device (Devices, 2007).

4.1 Description of the measurement set-up

The schematic of the measurement set-up used during the experiments is depicted in Figure 4.2:



FIGURE 4.2: AD6644: General measurement set-up

- **AD6644** This commercial ADC from Analog Devices has a resolution of 14 bits, nominally operates at a sampling frequency of 65Msps, has a fully-differential input with a Full-Scale of FS = 2.0V and parallel digital outputs. It requires an analogue bias of $AV_{cc} = 5.0V$ typical and a digital bias of $DV_{cc} = 3.3V$ typical. A $V_{REF} = 2.4V$ reference voltage is on-chip generated to give the Common Mode level to the input signals driving the AD6644. It is clocked differentialy via ENCODE and \overline{ENCODE} signals.
- **AD6644 Eval-Board** The AD6644 evaluation board contains all the elements necessary to operate the converter quickly and easily:
 - All the required bias-voltages on the evaluation board are driven from two power supplies of +5*V* and +3.3*V*, including the ADC analog and digital biasing.
 - The differential conversion clock of the ADC can be ac-coupled driven from a board-included fixed 65*Msps* frequency clock oscillator, the MX045-65 from CTS Reeves, or from an externally clock generator via a BNC or SMA connector. As the AD6644 must be clocked differentially, the clock signal is ac-coupled into the *ENCODE* and *ENCODE* pins via a board-included transformer.

• A single-to-differential input conditioning circuit: the DC-coupled analog input circuit buffers the single-ended input of the evaluation board to the differential inputs of the ADC under test. The DC-coupled circuit is a resistive inverter that uses the low-distortion fully-differential output AD8138 Operational Amplifier from Analog Devices. This amplifier has an input pin that gives the required Common Mode level to each of the output signals driving the ADC. This pin is driven by the output pin $V_{REF} = 2.4V$ given by the AD6644.

It should be noted that the signal conditioning circuit driving the AD6644 will be integrated in the system to be measured, introducing a non-linearity contribution that may be significant in the INL estimated by the different evaluation methods. This is why, as shown in Figure 4.2, from now on the ADC under test will be the system formed by the conditioning circuit plus the AD6644 ADC.

- **Tek AFG3102 Function/AWG Input Signal Generator** The AFG3102 is a conventional inexpensive generator. This generator does not meet the linearity requirements necessary to estimate the INL of the ADC under test. In our experiment the input signals have been generated using the basic-prestored standard generator functions.
- Filter During the experiments, three different signal filters are used according to the desired purity and the waveform of the input signal that will drive the ADC under test: (1) An expensive high quality custom-made band-pass filter designed for a frequency of 1.42*MHz* to achieve a high spectral purity sinusoidal signal. It is the Q56TR from TTE filter, a 8pole elliptical function anti-aliasing filter with a Total Harmonic Distortion of THD = -90 dBc dedicated for ADCs. This filter also lowers the noise level due to the input signal. (2) A conventional cheap 15MHz low-pass filter to filter out part of the noise introduced by the input signal. It is the BLP-15 filter from Minicircuit. This filter is used only to filter out the noise from the signal supplied by the generator to perform a double histogram test with a sinusoidal type signal. (3) A conventional cheap 5MHz low-pass filter to filter out part of the noise introduced by the input signal. It is the BLP-5 filter from Minicircuit. This filter is used only to filter out the noise from the signal supplied by the generator to perform a double histogram test with a triangular type signal.

- **SRSCG635 Clock Generator** A low jitter high accuracy clock generator is used to generate the ADC conversion clock at approximately 65*Msps*.
- **HP 53131A Frequency Counter** The frequency counter is used to achieve a high accuracy coherent sampling.
- **Agilent 16823A Logic Analyzer** Data acquisition is performed using a logic analyser.
- **HP E3631A Power Supply** For +3.3*V* and +5.0*V* biasing.

4.2 Description of the experiment test flow

Experimental tests have been carried out as follows:

- 1. Evaluation of the INL reference pattern using the Standard Histogram method. The excitation signal is a high spectral purity sine-wave obtained with the conventional generator and the inclussion of the TTE high quality bandpass filter in the signal path. The use of this filter imposes that the frequency of the sinusoidal signal is $f_0 \approx 1.42MHz$. This frequency is much lower than the sampling frequency of the converter, $f_s \approx 65Msps$.
- 2. Application of the SSA method using a pure sine-wave input signal. The pure signal is also obtained by filtering the sinusoidal signal generated by the conventional generator with the TTE high quality bandpass filter. The use of this filter imposes that the frequency of the sinusoidal signal is $f_0 \approx 1.42 MHz$.
- 3. Application of the SDH, the Extended SDH and the Enhanced DH methods using as the non-pure input signal the sine-wave generated by the conventional generator filtered by the conventional commercial BLP-15 low pass filter. The filter is used to lower the input noise level allowing to relax the number of captured samples. If the filter introduces distortion into the input signal, the applied method will include it as embedded in the non-linearity of the generator. In order to compare results, this test will be performed using the same input frequency of $f_0 \approx 1.42MHz$.
- 4. Application of the SDH the Extended SDH and the Enhanced DH methods using as the non-pure input signal a triangular-wave generated

by the conventional generator filtered by the conventional commercial BLP-5 low pass filter. This test has been performed at a frequency of $f_0 \approx 14.1 kHz$.

The following criteria have been considered when comparing the INL patterns obtained from the different methods versus the reference one:

- Comparison of the maximum and minimum values of the INL patterns.
- Comparison according to how the shape and margins comprising the two INL patterns match.
- Comparison of similarity between INL patterns. The similarity between patterns has been evaluated by calculating the Fréchet distance (Alt and Godau, 1995; Efrat et al., 2002; Buchin, Buchin, and Wenk, 2008). The Fréchet distance is a Figure Of Merit (FOM) that will allow a mathematical evaluation of the performance of the proposed methods by measuring the similarity between the INL patterns evaluated by the different approaches respect to the INL reference pattern, as it measures the distance between their points taking into account the flow of the two curves being compared. The larger the Fréchet distance the lower the similarity between the curves. A Fréchet distance of zero indicates that the curves match completely.

4.3 Standard Histogram test settings

The evaluation of the INL patterns requires test settings for performing a standardised histogram test (Measurement and Technical, 2011) according to: (1) Coherent sampling compliance and (2) Number of data records required. In general, the test setting procedure consists of the following steps:

- 1. Analysis of the output noise level, by means of a DC histogram. This analysis can also be performed using a low frequency sine wave as input signal and obtaining the sine of best fit to the output signal. The difference between the real output data and the best-fit signal gives us the residual or error which, due to the low frequency, can be assumed only as noise contribution.
- 2. Obtaining the number of samples and records required for the noise level of the system previously evaluated and according to the accuracy desired.

- (a) The number of samples per record is decided by the memory depth of the hardware available for the test and by the ability to establish a level of perfection in the coherence compliance between the sampling signal and the input signal. It should be observed that the longer the record, the more accuracy is required for the frequencies, as indicated in (Measurement and Technical, 2011).
- (b) The number of records is determined by the conditions indicated in the standard (Measurement and Technical, 2011).
- (c) The input signal and its conditions are set according to the available filtering capacity.
- 3. Assessment of whether it is necessary to reduce the noise level to reduce the number of records required. As the Standard Histogram method requires a uniform distribution of the samples over $[0, 2\pi]$, the different records should have their initial phases uniformly distributed over $[0, 2\pi]$. If this adjustment is done by software, it is necessary to leave a sufficient number of samples in each record to choose as the first sample of the record the one with the required initial phase. The number of samples per record is therefore also limited by the number of records to be acquired.
- 4. The saturation level to the ADC will depend on the noise level of our system and should be set according to the standard, but also according to the offset level to be used to perform the double histogram method, as the saturation should always be maintained.
- 5. The offset between the input signals used for the double histogram should be:
 - A value large enough so that the noise levels between the constructed histograms do not overlap.
 - A value small enough so that the saturation condition is not lost and the local variations of the generator non-linearity are slight enough to allow the derivative to be approximated by a finite first order difference.

Coherent Sampling Compliance

The experimental procedure followed to achieve a coherent sampling in a data record has been as follows:

1. Coherent sampling is guaranteed if it is complied with:

$$f_0 = f_s \frac{J}{M} \tag{4.1}$$

where f_0 is the input frequency, f_s is the sampling frequency, J is the number of cycles per record and M is the number of samples per record on which coherent sampling is established, being J and integer relatively prime to M.

- 2. The ideal values considered for the input frequency and the sampling frequency are the starting point. The use of the bandpass filter at 1.42 MHz fixes the frequency of the input signal, so in this experiment the sampling frequency has been more flexible in adjusting the coherence, although always considering that the ADC is working at its maximum frequency.
- 3. The input signal is programmed into the signal generator with the ideal required frequency value and by means of the frequency counter its value is accurately measured, obtaining f_0 . It is also possible to fine tune the frequency of the signal generator to the required frequency by means of the frequency counter.
- 4. A record length is set by selecting the number of samples M to be captured. When choosing the number of samples per record, it should be observed that the longer the record, the more accuracy is required for the frequencies, as indicated in (Measurement and Technical, 2011). Using the accurate value of the input signal f_0 and the ideal value to the sampling frequency (in our case 65MHz), from (4.1) a number of cycles is obtained. The number of samples M and the number of cycles J are then set to relatively prime integers.
- 5. From (4.1), using f_0 , M and J the precise value for the sampling frequency that achieves coherence is obtained, being f_s .
- 6. The value obtained for the sampling frequency is programmed to the highest possible accuracy supported by the clock generator and by means of the frequency counter its value is accurately measured.
- 7. A very fine coherence adjustment is possible by varying the frequency of the clock generator in very small steps until the frequency counter meets the obtained value sampling frequency f_s .

Amplitude setting

For fine tuning of the input signal amplitude, a calibration process of this parameter has been carried out, by correcting the experimental measured gain between the amplitude programmed in the generator and that measured with the output data. The amplitude of the input signal saturating the ADC under test has been programmed to provide an already corrected amplitude of 0.1dBFS.

Setting of the number of samples per record and the number of records

The memory depth of our capture system has been limited to a maximum number of samples per record of $Mmax = 2^{16} = 65536$. To optimise memory resources, for each record we have fully utilised the available memory depth, but reserving a number of samples to eliminate effects from signal settling (removing first samples from the histogram computation) and to software adjust the phase of each record to ensure a uniformly distributed sampling between 0 and 2π . If M = 65304samp/reg is considered, this gives a margin of 65536 - 65304 = 232 samples to perform the phase shift.

Once the number of samples *M* per record is set, the number of records required to achieve the desired confidence level must be determined. The standard ((Measurement and Technical, 2011)) provides an equation to calculate it:

$$R = \left(\frac{2^{(N-1)}K_u}{B}\right)^2 \cdot \left(\frac{c\pi}{M}\right) \cdot \left\{1.13\left[\frac{\sigma}{V} + \frac{c\sigma_{\Phi}}{2}\right] + 0.25\left(\frac{c\pi}{M}\right)\right\}$$
(4.2)

where *R* is the minimum required number of records, *M* is the number of samples per record, *c* is equal to $1 + 2(V_0/V)$, *V* is the full-scale range of the ADC under test, V_0 is the input overdrive, σ is the rms random noise effects, σ_{Φ} is the rms random phase error of the input signal relative to the sampling frequency, *N* the number of bits of the ADC under test, *B* the desired test tolerance and k_u is obtained from the Table 2 of ((Measurement and Technical, 2011)) for the specified confidence. The following approximations on the standard expression has been used in our test:

- Since the high resolution of the ADC under test, V_0/V is very small, considering $c \approx 1$.
- Phase noise is assumed to be white noise and embedded within the total random noise.

$$R \approx \left(\frac{2^{(N-1)}K_u}{B}\right)^2 \cdot \left(\frac{\pi}{M}\right) \cdot \left\{1.13\frac{\sigma}{V} + 0.25(\frac{\pi}{M})\right\}$$
(4.3)

4.4 Evaluation of the INL reference pattern using the TTE high quality band-pass filter: Pure Sine input signal



FIGURE 4.3: AD6644: Measurement set-up for the evaluation of the INL reference pattern



FIGURE 4.4: AD6644: Picture of the set-up for the evaluation of the INL reference pattern

The pure sinusoidal input signal of frequency $f_0 = 1.42MHz$ has been generated using the TTE high quality custom-made Band-Pass filter (BP filter), as shown the schematic of the set-up in Figure 4.3 to evaluate the INL



FIGURE 4.5: AD6644: Output data spectrum from the pure sinusoidal input signal

reference pattern by the Standard Histogram method. The figure also reports the attenuation factors in the input signal path due to the filtering stage and the input conditioning circuit. It should be mentioned that the TTE Band-Pass filter removes the DC component of the generator signal (AC coupling). Figure 4.4 shows a picture of the set-up at the laboratory, with the TTE filter placed after the signal generator. In order to show the spectrum of the output data when this filter is used, Figure 4.5 is plotted. This figure has been obtained with a peak-to-peak amplitude of -1dBFS not to saturate the ADC and by averaging spectra over R = 16 records of M = 16343 samples each and taken in a continually way. The records have been acquired in compliance with the requirement of coherent sampling, being de sampling frequency $f_s \approx 65 Msps$. As the input signal is a high purity sine, the harmonic distortion observed in the spectrum of the output signal is produced by the non-linearity of the ADC under test. Taking the contribution of the 100 most influential harmonics of the spectrum, the Total Harmonic Distortion (THD) obtained translates into an effective number of bits of 13.3 bits, i.e. the non-linearity results in a loss of approximately 0.7 bits respect to the ideal ADC resolution. The Effective Number Of Bits (ENOB) is 11.2 bits, i.e. adding the noise contribution the loss is approximately 2.8 bits.

In order to have an experimental estimation of the noise level of our system, the histogram of a DC level has been analysed. The histogram shows a bell-shaped Gaussian distribution centred at the DC level and $\sigma \approx 2LSB$.



FIGURE 4.6: Number of Records versus Noise for M = 65325 samples

To estimate the INL reference pattern, the peak-to-peak amplitude of the pure sinusoidal input signal has been set to A = +0.1 dBFS, maintaining the input frequency to 1.42*MHz*. The DC component of this signal is the nominal one, and will be filtered by the TTE bandpass filter. The selected amplitude causes both upper and lower saturation of about 100*LSB*. Following the coherent sampling compliance search process, the sampling frequency has been set to 65.00*Msps* and the selected number of samples per record to M = 65325. This number of samples gives 211 samples to perform the registers phase shift to cover uniformly $[0, 2\pi]$. Figure 4.6 plots the number of records required versus the noise level of the system for a M = 65325samp/reg, for test tolerances from 0.2*LSB* to 1*LSB*, considering a 95% confidence level. The number of total samples collected has been 3070275.

The noise sigma value in Figure 4.6 allows to choose the number of records according to the desired tolerance for the test. The choice is a trade-off between accuracy and time cost. In this experiment, R = 47 records has been acquired for histogram test, corresponding to a estimation tolerance of about 0.5*LSB*.

Figure 4.7 shows the INL reference pattern obtained from the Standard Histogram method, using the pure sine input signal. The figure also plots the DNL. A typical INL saw-pattern is estimated, being the maximum INL





FIGURE 4.7: AD6644 INL and DNL reference pattern

value about 3*LSB*. The figure shows that the INL is practically in the range of $\pm 1.5LSB$, except in the more extreme lower codes where there is a curvature rising to about 3*LSB*. Note the third order behaviour in the shape of the evaluated pattern, which is consistent with the spectrum shown in Figure 4.5 where, excluding the main harmonic, the third harmonic predominates over the rest of the spectral components. From now on it will be considered as the true INL pattern of the ADC under test and will be called INL reference pattern.
4.5 Estimation of the INL pattern using the SSA method: Pure Sine input signal



FIGURE 4.8: AD6644: Measurement set-up for the evaluation of the INL pattern by the SSA method

The objective of this section is to show the estimated INL pattern when the SSA method is applied to the ADC under test and its comparison with the reference pattern evaluated by the Standard Histogram method.

For this purpose, the ADC under test has been excited with a high spectral purity sinusoidal signal obtained by filtering with the TTE BP filter the sinusoidal signal of frequency $f_0 = 1.42MHz$ generated by the generator. The schematic of the measurement set-up is as shown in the Figure 4.8, the same as for the INL reference pattern estimation by the Standard Histogram method, but with the conditions of the input siganl and the data acquisition adapted to the SSA spectral test, as will be detailed in this section. The SSA method has been applied with a much smaller number of samples than the Standard Histogram method. In this experiment, the coherence of each record has been established on M = 16343 samples. Taking a smaller number of samples per record speeds up the process of searching for coherent sampling, since as indicated above, the larger the data record the more precision is required in the frequencies involved. In the spectral processing, a coherent sampling search process has been performed together with a fine tuning of frequencies to avoid that high frequency harmonics (above the Nyquist frequency) when folding within the Nyquist band overlap or lie closely to



FIGURE 4.9: AD6644: Output data spectrum from the pure sinusoidal input signal by averaging 4 registers of 16343 samples per register

harmonics of lower frequencies within the Nyquist spectrum. To perform spectrum averaging, R = 4 records have been acquired continuously. It is worth remembering that the records have to be taken continuously in order not to lose the phase information of the sinusoidal signal. The total number of samples taken is 65372, practically filling the available memory depth. It should be noted that the total number of samples acquired in this esperiment is the 2.13% of the total number of samples collected to evaluate the INL reference pattern from the Standard Histogram method.

Concerning the input signal amplitude, it has been set to a peak-to-peak amplitude of -0.2dBFS to ensure that the signal does not saturate the ADC under test. This peak-to-peak amplitude is about 180*LSB* lower than the full-scale of the ADC under test.

When obtaining an averaged spectrum, it is possible to address it in two different ways: (1) Averaged Spectrum: one approach is to calculate the spectrum over each of the M sample records and then perform the averaging. (2) Time-Averaged Spectrum: another approach is a raw-data averaging over the R records of M samples and calculate the spectrum of the averaged signal obtained. Figure 4.9 shows the spectrum obtained from the first approach: the FFT of each record of M = 16343 samples has been calculated and then the four spectra obtained have been averaged. Figure 4.10 shows the spectrum obtained with the second approach: the data of the four records have

4.5. Estimation of the INL pattern using the SSA method: Pure Sine input signal



FIGURE 4.10: AD6644: Output data spectrum from the pure sinusoidal input signal by time-averaging 4 registers of 16343 samples per register

been time-averaged, obtaining an averaged data record. The FFT has been calculated on the data of this new record. Comparing both pictures, it can be observed that the Time-Averaged approximation eliminates part of the noise and allows discriminating harmonics that in the first approximation are embedded in the spectrum background noise. Although time averaging underestimates the spectral noise, it is well suited for the application of the SSA method, as it is helpful in discerning a larger number of harmonics compared to spectral averaging. This is clearly observable in the THD parameter: using the Averaged Spectrum approach it has been calculated on 100 harmonics while in the Time-Averaged approach it has been possible to estimate it on 300 harmonics. Although the contribution of harmonic distortion to the effective number of bits when taking 100 harmonics (about 12.7 bits) or 300 harmonics (about 12.5 bits) has not changed much, discerning more harmonics in the SSA method allows a more accurate estimation of the shape of the INL pattern.

Finally, based on the spectrum of the figure 4.10, the amplitude, frequency and phase parameters of the 300 harmonics with the highest amplitude have been evaluated and the SSA method has been applied. Figure 4.11 shows the INL estimated by the SSA method in maroon line and the reference pattern in grey line. The estimated INL pattern is a smooth version of the INL reference pattern, but follows its shape perfectly and within the margins set by the reference pattern.



Chapter 4. Experimental application of the proposed methods on a commercial high-resolution Analog-to-Digital Converter





FIGURE 4.12: Estimated INL from the SSA method using 300 harmonics and its comparison to the estimated INL from the histogram method using 32686 samples

Figure 4.12 overlaps both the INL estimated by the SSA method using the spectrum parameters from the 300 harmonics obtained via the Time-Averaged spectrum with R = 4 records (65372 total number of samples) and the INL obtained by the histogram method with the same number of records (cyan line). The figure shows how the number of samples is insufficient for the histogram method for a noise averaging to obtain an accurate INL estimate, as some errors are of the order of 2*LSB*. Although the SSA method does not provide the detail of the typical INL saw pattern, it does accurately follow the shape of the reference INL pattern. For a mathematical comparison between pattern similarities, the Fréchet distance to the INL reference pattern has been calculated for both estimates. The Fréchet distance using the SSA method is $FOM_{FD} = 48.5$ and using the histogram method is $FOM_{FD} = 82.4$.

4.6 Estimation of the INL using methods based on the DH: Non-pure input signals

Next step has consisted of carrying out the experiments for the application and evaluation of the proposed SDH, Extended SDH and Enhanced DH methods based on the DH approach.

4.6.1 Estimation of the INL pattern using the LPB-15 lowpass filter: Non-pure sine input signal

In this test, the sinusoidal signal generated by the generator is filtered by the low-cost LPB-15 low-pass filter, as shown the set-up figure 4.13. This is the non-pure sine input signal. Figure 4.14 shows a picture of the set-up in the laboratory, with the LPB-15 filter placed after the signal generator. Figure 4.15 shows the spectrum of the ADC signal response to this excitation. It should be noted that now the THD obtained with the 100 most influential harmonics of the spectrum corresponds to an effective number of bits of 9.9 bits, being of the same order as the ENOB obtained with the total contribution of noise and distortion. That is, the non-linearity of the input signal in this experiment is conditioning the non-linearity measured through the output signal and its contribution is overestimating the non-linearity of the ADC under test. This is clearly shown by the THD, which estimates a loss of 4.1 bits respect to the nominal ADC resolution. Obviously, the application of the histogram method using this input signal will lead to an erroneous estimation of the Integral Non-Linearity of the ADC under test.

In order to have an experimental estimation of the new noise level of our system, the histogram of the output data of a DC level input has been analysed. The histogram shows a Gaussian distribution with a sigma of about 2*LSB*. In the DH method, this test not only helps to establish the minimum number of registers to perform the histogram tests with a certain tolerance, but also to establish the minimum difference between the DC or offset values of the input signals so that there is no overlap between them in the queue of the Gaussian, to be clearly discernible when applying the method. This is shown in Figure 4.16, where the histograms of three DC values in LSB units have been plotted: nominal DC value, +15LSB offset from DC nominal, and -15LSB offset from DC nominal. Considering that in the Gaussian distribution approximately 99% of the distribution is contained within

4.6. Estimation of the INL using methods based on the DH: Non-pure input signals



FIGURE 4.13: AD6644: Set-up for the application of the SDH, Extended SDH and Enhanced DH methods using a non-pure sine-wave input



FIGURE 4.14: AD6644: A picture of the set-up for the application of the SDH, Extended SDH and Enhanced DH methods using a non-pure sine-wave input

 $\pm 3\sigma$ with respect to the central value, the separation between the DC values of each excitation signal must be about 15*LSB*. Finally, the following test conditions have been set: (1) the computing of M = 65416samp/reg and R = 47 records for each histogram test (that is, each histogram has been performed on a total of 3.1 million of samples), corresponding to a estimation





FIGURE 4.15: AD6644 output data spectrum from the non-pure sinusoidal input signal



FIGURE 4.16: Evaluation of the system noise by DC histograms

tolerance of about 0.5*LSB*, (2) the displacement of a $\pm 15LSB$ respect to the nominal DC value to generate the two non-pure sinusoidal input signals for the SDH and ESDH methods. Therefore, the offset or displacement between the two non-pure sinusoidal signals to apply a double histogram has been about 30LSB = 3.7mV.





FIGURE 4.17: Offset evolution during the test process in SDH method

Considering M = 65416samp/reg, the number of cycles per record is J = 1429cycles/reg. Each displacement from one sample to the next corresponds to a phase shift of $360^{\circ} \cdot (1429/65416) = 7.86^{\circ}/samp$. The 120 samples to perform the phase shifts gives a coverage of $7.86^{\circ}/samp \cdot 120 = 943^{\circ}$, more than enough to cover the phase shifting between 0 and 2π .

The histogram H1 has been obtained from the 47 records of output data acquired using as excitation signal the non-pure sine-wave with a $os_1 = +15LSB$ offset. The histogram H2 has been obtained from the 47 records of output data acquired using as excitation signal the non-pure sine-wave with a $os_2 = -15LSB$ offset. From each set of histograms H1 and H2 the virtual transition levels have been estimated. The offset is required remaining constant over time. Figure 4.17 is intended, as an example, to show the evolution of the offset values os_1 and os_2 during the test run, plotting the offset estimated with the data set for each of the first 40 records captured for the construction of the H1 and the H2 histograms. Performing a linear fit to the set of 40 offset values calculated for each histogram, it is concluded that for the H1 histogram the offset has followed an evolution with effective gain $g_1 = +3.37mLSB/reg$ and for the H2 histogram the offset has followed an evolution with effective gain $g_2 = -5.12mLSB/reg$. Temporal offset drifts will lead to errors in the estimation of the INL pattern.

In order to address the offset time drifts as the solution proposed in (Jin et al., 2005a; Jin et al., 2005b), the data collection has been repeated but switching the offset of each sinusoidal input signal for each record following a Thue-Morse series distribution. These records have then been reordered



FIGURE 4.18: Offset evolution during the test process in an Thue-Morse interleaved SDH method

by software to construct two histograms: the one containing the output data with offset +15LSB and denoted as H1Morse and the one containing the output data with offset -15LSB and denoted as H2Morse. Figure 4.18 shows the time evolution of the offset values os_1 and os_2 , plotting the offset value estimated for each of the first 80 registers when the 94 registers are interleaved following the Thue-Morse series. From the linear fit performed to the set of 40 offset values calculated for H1Morse and to the set of 40 offset values calculated for H1Morse and to the set of 40 offset values calculated for H1Morse and $g_2 = +0.54mLSB/reg$. The effective gains have been reduced but not completely eliminated, so there will still be errors in the INL estimation due to offset drifts.

Figure 4.19 plots the non-linearity patterns obtained by each of the simple histograms, H1, H2, H1Morse and H2Morse. That is, the INL curves obtained by comparing the ideal transition levels of the ADC under test with the virtual transition levels obtained from the histogram H1 (INL in red line), from the histogram H2 (INL in magenta line), from the histogram H1Morse (INL in blue line) and from the histogram H2Morse (INL in green line) are depicted. The grey line plots the INL reference pattern. The four INL patterns obtained from the non-pure sine signals practically match each other and lie within $\pm 12LSB$. By visual comparison with the reference INL, it is possible to conclude that the generator in its sinusoidal function is more linear in the central regions of the sine waveform than in the extreme regions. The Fréchet distance reports (indicated as FOM_{FD} in the picture), as expected, that all four INL patterns have practically the same low similarity to the reference INL pattern, a value of about 400.

4.6. Estimation of the INL using methods based on the DH: Non-pure input signals



FIGURE 4.19: AD6644 INL patterns estimated from the simple histograms of the non-pure sinusoidal signals

Using the H1 and H2 histograms, the SDH method has been applied. The H1Morse and H2Morse sets have been used to apply the Double Histogram but with a parameterisation of Mp = 51 coefficients of the non-linearity of the generator, as explained in the Enhanced DH method but not yet applying our time drift correction strategy. Figure 4.20 shows the results obtained in both cases and their comparison with the INL reference pattern. Time drifts in the measurement set-up during the tests leads to an erroneous estimation of the INL of the ADC under test. Even the strategy of interleaving the 94 records according to the Thue-Morse series was not sufficient to improve the result. The Fréchet distance informs that Thue-Morse strategy has improved the result ($FOM_{FD} = 302.7$), but is still far away from the reference pattern.

Finally, the Extended SDH method has been applied using the H1 and H2 sets. The Enhanced DH method has been applied using the H1Morse and H2Morse sets (hereinafter referred to as Enhanced Morse DH). Figure 4.21 shows the results obtained from both methods and their comparison to the INL reference pattern. The upper picture shows in maroon line the INL pattern estimated with the Enhanced Morse DH method. The bottom picture shows in pink line the INL pattern estimated with the Extended SDH method. It is noteworthy how the patterns evaluated with these algorithms closely matches with the reference pattern, with the typical INL saw-pattern,



FIGURE 4.20: AD6644: INL patterns estimated by SDH and Morse DH methods using a sinusoidal input signal

and how the Figure of Merit has improved to values below 70. The INL estimated by the Extended SDH method obtains a Fréchet distance of 68.7 and a maximum INL of *3LSB*. The INL estimated by the Enhanced DH method and introducing the offsets interleaving strategy obtains a Fréchet distance of 66.7 and a maximum INL of about 2.5*LSB*.



FIGURE 4.21: AD6644: INL patterns estimated by the Extended SDH and the Enhanced DH methods

4.6.2 Estimation of the INL pattern using the LPB-5 low-pass filter: Non-pure triangular input signal



FIGURE 4.22: AD6644: Set-up for the SDH, Extended SDH and Enhanced DH methods using a non-pure triangular-wave as input signal

In order to show the independence of the results of the proposed methods with the type of input signal wave driven to estimate the INL of the ADC under test, the experiment has been repeated but with a low-purity triangular-wave signal generated by the same non-linear generator. Figure 4.22 shows the set-up. Now the signal generated by the triangular function of the generator is filtered by the low-cost LPB-5 low-pass filter. This is the non-pure triangular input signal.

The noise level obtained from the histogram of the output data of a DC level input has been analogous to that of the previous experiments, being again a Gaussian distribution with a sigma of about 2*LSB*. This leads to conclude that in all of the introduced filtered cases it is the noise level of the ADC under test that is dominating the total noise level of the system.

As in the previous experiments, the test conditions have been set according to the coherent sampling compliance and the number of data per record and the number of records to obtain an estimation accuracy of about 0.5*LSB* considering 2*LSB* noise level. The number of samples per register over which the coherent sampling is established, *M*, is still conditioned by the memory





FIGURE 4.23: Raw output data from the non-pure triangular input signal



FIGURE 4.24: Equivalent-time output data from the non-pure triangular input signal

depth of Mmax = 65536 samples and by the need to have a sufficient number of samples available to perform the sample shift at the beginning of each record so that the uniform distribution is met. Finally, the following conditions have been set: $f_0 = 14.1kHz$, $f_s = 65.20MHz$, M = 60237samp/reg, J = 13cycles/reg and R = 47 registers. That is, each histogram has been performed on a total of 2.8 million of samples. Regarding the saturation level, it has remained around 100LSB. According to the measured noise level, the offset shift between the non-pure triangular-wave input signals to perform the proposed double histogram methods has been kept at 30LSB.

4.6. Estimation of the INL using methods based on the DH: Non-pure input signals

The histogram H1 has been obtained from the 47 records of output data acquired using as excitation signal the non-pure triangle input signal with a $os_1 = +15LSB$ offset. The histogram H2 has been obtained from the 47 records of output data acquired using as excitation signal the non-pure triangle-wave with a $os_2 = -15LSB$ offset. Figure 4.23 shows one of the coherent sampling compliance record of the ADC under test output data in response to the non-pure triangular signal used to compute the histogram H1. The figure depicts the output codes encoded in bipolar output range versus time. Figure 4.24 plots the equivalent-time output data, where the data of the thirteen cycles have been depicted in a single period of the signal, being $T_s = 1/f_s = 70.9\mu s$ the period of the signal. The saturation is clearly visible in this graph.

As in the non-pure sinusoidal input signal experiment, the data collection has been repeated switching the offset of each triangle input signal for each record following the Thue-Morse series distribution. These records also have been reordered by software to obtain two histograms: the one containing the output data with offset +15LSB and denoted as H1Morse and the one containing the output data with offset -15LSB and denoted as H2Morse.

Figure 4.25 plots the non-linearity patterns obtained by each of the simple histograms, H1, H2, H1Morse and H2Morse. That is, the INL curves obtained by comparing the ideal transition levels of the ADC under test with the virtual transition levels obtained from the histogram H1 (INL in red line), from the histogram H2 (INL in magenta line), from the histogram H1Morse (INL in blue line) and from the histogram H2Morse (INL in green line) are depicted. The grey line plots the INL reference pattern. The four INL patterns obtained from the non-pure triangular signals practically match each other and lie within the range [-6LSB, +2LSB]. The Fréchet distance has been calculated in each estimation and included in the figure, reporting, as expected, that all four INL patterns have practically the same low similarity to the reference INL pattern, a value of about 150. Comparing with the INL results of the simple histograms of the sinusoidal experiment, it can be concluded that the non-linearity of the generator in its triangular function is lower than that of the sinusoidal function.

Figure 4.26 shows the results obtained when the SDH method (in green



FIGURE 4.25: AD6644 INL patterns estimated from the simple histograms of the non-pure triangular signals

line) and the Thue-Morse strategy of offset interleaving (in yellow line) have been performed, and their comparison with the INL reference pattern (in grey line). As for the sinusoidal experiment, the non-linearity of the generator has been parameterized by Mp = 51 coefficients. The time drift in the measurement set-up during the tests leads to an erroneous estimation of the INL of the ADC under test when the SDH method is applied. The resulting INL pattern is analogous to that of the experiment with sinusoidal input signal, obtaining a Fréchet distance of 418.3. But, on the other hand, the strategy of interleaving the 94 records according to the Thue-Morse series has been able to improve the result, obtaining a Fréchet distance of 66.5 and a maximum INL of about 2*LSB*, results very similar to those obtained with the sine-wave Enhanced DH method.

Finally, the Extended SDH method has been applied using the H1 and H2 sets. The Enhanced DH method has been applied using the H1Morse and H2Morse sets. Figure 4.27 shows the results obtained from both methods and their comparison to the INL reference pattern. The upper picture shows in maroon line the INL pattern estimated using the Enhanced Morse DH method. The bottom picture shows in pink line the INL pattern evaluated by the Extended SDH method. The INL estimated by the Enhanced Morse DH method (Enhanced DH introducing the offsets interleaving strategy) obtains a Fréchet distance of $FOM_{FD} = 62.5$ and a maximum INL of about 2*LSB*.



4.6. Estimation of the INL using methods based on the DH: Non-pure input signals

FIGURE 4.27: AD6644: INL patterns estimated by the Extended SDH and the Enhanced DH methods using a triangular signal

For the INL pattern estimated by the Extended SDH method, the Fréchet distance is $FOM_{FD} = 89.1$ and lies approximately within a range of $\pm 1LSB$. It is noteworthy that both estimates obtain a very similar behaviour in the lower codes, approximately below code -7168, which does not match the reference pattern. This phenomenon, combined with what is shown by Figure 4.25 in those same codes, leads to suspect that probably the INL of the ADC under test has modified its behaviour especially in those codes during the test with the triangular input signal due to the influence of the DC-coupled input conditioning circuit part of the ADC under test.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

Knowledge of the parameters that characterise the transfer function of an Analog-to-Digital converter (ADC) is of major importance to ensure the correct operation of an ADC in a given application. One of the most widely used standardised methods for estimating these parameters is the Standard Histogram method. Its application in high resolution ADCs is highly expensive and time consuming, especially in industrial sectors such as the so-called New Space, where large amounts of parts have to be tested several times in long test flows.

This dissertation has focused on the development of two alternative methods to the Standard Histogram method (Measurement and Technical, 2011) for the estimation of the non-linearity parameters of high resolution ADCs.

- 1. The first contribution introduced a method based on a spectral processing and it has been named Simple Spectral Approach (SSA):
 - (a) The method is intended to estimate the Integral Non-Linearity (INL) parameter acquiring much smaller number of output samples than required by the Standard Histogram. It uses a pure sinusoidal input signal. It is a black-box method as it makes no assumptions about the ADC design topology.
 - (b) It assumes and applies a continuous and derivable transfer function model of the ADC under test.
 - (c) The method performs a local study of the ADC transfer function by means of a first-order Taylor series which is related to the ADC non-linearity parameters by means of the mathematical definition of the INL.

- (d) The Integral Non-Linearity is estimated by the evaluation of the harmonic amplitudes and the phase-shifts obtained from the spectrum of the ADC output.
- (e) The SSA method has been applied by simulation in realistic ADC models with different design topology and non-linearity patterns: some ADC models emulate smooth INL patterns and some ADC models emulate saw-tooth INL patterns. In both cases, accurate estimates of the INL pattern were obtained.
- (f) The SSA method has been applied in laboratory experiments to estimate the INL of two real ADCs: a 12-bit resolution Pipeline prototype ADC and a 14-bit resolution 65*Msps* commercial Pipeline ADC, both with sharp INL patterns. The results show an INL pattern that follows the shape of the reference one (evaluated by the Standard Histogram method), reproducing the typical large steps, and always complying with the INL margins established by the reference INL
- (g) The SSA method can be useful in industrial test protocols where a very precise estimation of the shape of the INL pattern is not required but just to evaluate the maximum and minimum values in which it lies, in order to compare them with the range established by the manufacturer as valid. It is a trade-off between accuracy and cost. Introducing the SSA method as an initial check test, it can also be useful to quickly assess whether a long, highly accurate test process is running under the right conditions by comparing the shape of the estimated pattern with the one actually expected. This will allow a fast decision on whether to continue or abort the full test.
- 2. The second contribution introduced methods based on the collection of two sets of output data to construct two histograms (Double Histogram). The methods have been referred to as Enhanced Double Histogram (Enhanced DH or EDH), Simplified Double Histogram (Simplified DH or SDH) and Extended Simplified Double Histogram (Extended SDH or ESDH):
 - (a) The methods are intended to relax the requirements on the purity of the signal driving the ADC under test. They use the transition levels evaluated from the two histograms constructed from

the collection of two sets of output data in response to two identical non-pure input signals except for a constant DC level between them. The ADC is handled as a black-box model as no assumption is made about its design topology.

- (b) A proposal for the estimation of the sets of transition levels using the two histograms constructed is presented. No assumption is made about the type of input waveform used.
- (c) A solution for the application of the method in a non-stationary test environment has also be addressed. A general algorithm has been developed under the hypothesis that time drifts in the input signals can be modeled with an effective offset and an effective gain introduced by the signal path adder, being different effective values for the first and the second data acquisition to construct the two histograms.
- (d) The method named Enhanced Double Histogram (EDH) is based on performing a parameterisation of the non-linearity of the generator by means of a serial expansion of basis functions, as was done in the SEIR algorithm presented in (Jin et al., 2005a) but it is adapted for using in a non-stationary test environment.
- (e) The Simplified Double Histogram method (SDH) is a simple novel proposal that performs a local study of the non-linearity of the generator by means of its derivative approximated with the threepoint formula, obtaining a simple relation with the actual code width of the ADC under test. The two sets of transition levels evaluated from the two histograms (called virtual transition levels) allow to estimate the actual code widths of the ADC under test through an expression that only depends on the two sets of virtual transition levels and the applied constant offset.
- (f) The Extended Simplified Simplified Double Histogram (ESDH) method uses the derivative-based approach presented in the SDH method, but adapted for use in a non-stationary test environment.
- (g) The methods has been applied by simulation in realistic Pipeline ADC models with the typical saw-tooth non-linearity patterns. The Simplified DH method has been applied in simulated experiments using different input waveform signals. The Extended SDH and Enhanced DH methods have been applied by simulation emulating a non-stationary test environment using an adder model with

time drifts in gain and offset parameters. In all cases, accurate estimates of the INL pattern were obtained.

- (h) The methods have been applied in laboratory experiments to estimate the INL of a 14-bit resolution 65*Msps* commercial Pipeline ADC. A conventional cheap generator has been used in its standard waveform generation function and including low-cost filters in the signal path for noise filtering of the input signals. Experimental tests have been carried out using in one case a low-purity input sine waveform and in another case a low-purity input triangular waveform. The results have shown that it is possible to accurately estimate the INL of a high performance ADC using a low-cost generator and applying the proposed DH-based methods.
- (i) In the industrial sector, the proposed methods can be very useful allowing to perform linearity testing on high-resolution ADCs overcoming the handicap of using expensive high-linearity signal generators (including Arbitrary Waveform Generators, AWGs, and those integrated in Automatic Test Equipments, ATEs). As examples, some advantages resulting from their application would be: (1) extending the test laboratory resources available to carry out the test, (2) speeding up the design and assembly of the measurement set-up by adapting the different resources available to the different ADCs to be measured, (3) taking advantage of resources that are obsolete versus the new generations of ADCs.

5.2 Future Work

- Integration of the alternative methods into industrial test protocols. Enhancing the application in the industrial sector of the methods developed in this research work to perform linearity tests on ADCs is a non-trivial task that remains to be done. As shown in the introductory chapter of the thesis, there is a large literature on alternative methods to the histogram test, but their application in the test industry is not widespread. Focusing on test companies in the space industry, promoting the use of these methods implies a full customer confidence in them, and this is achieved by assuring their reliability throughout the several test flows. A future action plan could consist of applying the proposed methods in parallel with the Standard Histogram method in ADC COTS qualification projects, to have a broad set of results to support the method for future customers.
- Integration of state-of-the-art spectral processing techniques into the SSA method. The SSA method is a fast approach for INL estimation in high-resolution ADCs, but compliance with coherent sampling is one of the most challenging constraints that needs further work. On the other hand, the application of the SSA method using saturated output sine waves would allow to cover the full output code range of the ADC and relax the requirements on signal amplitude control. The inclusion of a technique similar to that the FERARI (Fundamental Estimation, Removal And Residue Interpolation) (Sudani, Xu, and Chen, 2013; Xu, Sudani, and Chen, 2014) in the SSA method is future work to address both of the above issues.
- Setting an upper limit on the value of the offset applied between the input signals for the application of the Simplified Double Histogram method. As a pending task is to formulate an expression to define a maximum value for the offset up to which a description with the first derivative and its approximation by means of the finite difference is valid.
- Adaptation of the Double Histogram method for application using ACcoupled signals. The development of the Double Histogram method based on the variation of the amplitude value of the input signals is one possibility to address the issue.

- Adaptation of the algorithm used by the Simplified Double Histogram method to a procedure in which transition levels are not evaluated by the Standard Histogram method.
- Optimisation of the procedure of the Double Simple Histogram method to generators with a linearity behaviour that varies according to the evolution of the generated signal. This behaviour can be evident in the generation of signals that change abruptly, as the saw-tooth or the triangular waveform signals.

Appendix A

Evaluation of the static parameters of an ADC by the Standard Histogram Method

A.1 An overview of the ADC static parameters

An Analog-to-Digital Converter, hereafter referred to as ADC, is a device that converts an analog signal x(t) to a digital signal, represented as an ADC output code k. Under stationary conditions, the relationship between the analog input signal and the ADC output codes is a staircase function, known as the transfer function of the ADC. This transfer function is characterised by: (1) the analog conversion domain of the ADC, which is the $[R^-, R^+]$ range of analogue input signal values in which the ADC operates, being R^- the lower limit of the conversion domain and R^+ the upper limit of the conversion domain and conversion domain where the function changes value or code in a stepwise way, and called code transition levels or simply transition levels.

In the case of an ideal ADC, the analog conversion domain is divided into uniform intervals of value $q = FS/2^n$ called quantum or LSB of the ADC, where $FS = R^+ - R^-$ is the Full Scale or length of the domain and n is the number of bits or the resolution of the ADC. The output code is represented in binary base by n digits. Without loss of generality it has been assumed that the codes are coded in unsigned decimal values. The transfer function of the ADC is not a linear function, but it is considered to be linear if the transition levels are linearly related to the output code. This is the case of the ideal ADC, whose transition levels fulfil the following linear relationship:

$$l_k = R^- + q \cdot k, \quad \forall k \in [1, 2^n - 1]$$
(A.1)

where the set $\{l_k\}$ represents the input signal values where the output code of the ideal ADC changes from k - 1 to k, that is, the ideal transition levels. In the ideal ADC, the minimum code or lower saturating code is 0 and the maximum code or upper saturating code is $2^n - 1$, being $[0, 2^n - 1]$ the output conversion domain.

In the real ADC, the output conversion domain may be less than that of the ideal ADC. Therefore, the minimum code or lower saturating code is denoted as $z_{min} \ge 0$ and the maximum code or upper saturating code as $z_{max} \le 2^n - 1$, being $[z_{min}, z_{max}]$ the output conversion domain of the real ADC.

An ADC is designed to meet the behaviour of the ideal ADC. The differences between the set of real transition levels of the real ADC, hereafter designated as $\{t_k\}$, and the set of ideal transition levels $\{l_k\}$ report how much the transfer function of the real ADC deviates from the transfer function of the ideal ADC. These are the static parameters and include the following:

INL Integral Non Linearity. It measures the difference between the set $\{t_k\}$ and the set $\{l_k\}$ in quantum or LSB units:

$$INL_k = \frac{t_k - l_k}{q}, \quad \forall k \in [z_{min} + 1, z_{max}]$$
(A.2)

It has to be corrected from offset and gain contributions, as indicated by (Measurement and Technical, 2011).

DNL Differential Non Linearity. It measures how much the width of each code of the actual ADC, $w_k = t_{k+1} - t_k$, deviates from the quantum or LSB of the ideal ADC, in LSB units:

$$DNL_{k} = \frac{w_{k}}{q} - 1 = \frac{t_{k+1} - t_{k}}{q} - 1 = INL_{k+1} - INL_{k}, \quad \forall k \in [z_{min} + 1, z_{max} - 1]$$
(A.3)

A code *k* is defined as missing code if $DNL_k \leq -0.9$.

GE Gain Error. It measures the variation rate of the real analog conversion domain with respect to the ideal one:

$$GE_{v} = (t_{z_{max}} - t_{z_{min}+1}) - (l_{z_{max}} - l_{z_{min}+1})$$
(A.4)

Expressed in LSB units, it is related to INL as:

$$GE_{LSB} = \frac{GE_v}{q} = INL_{z_{max}} - INL_{z_{min}+1}$$
(A.5)

It is usually expressed as a percentage of Full Scale:

$$GE_{\%FS} = \frac{GE_v}{FS} \cdot 100 \tag{A.6}$$

OFFE Offset Error. It measures the difference between the beginning of the actual ADC analog conversion domain and the beginning of the ideal ADC analog conversion domain:

$$OFFE_v = t_{z_{min}+1} - l_{z_{min}+1} \tag{A.7}$$

Expressed in LSB units, it is related to INL as:

$$OFFE_{LSB} = \frac{OFFE_v}{q} = INL_{z_{min}+1}$$
 (A.8)

ZE Zero Error. It measures the difference between the central position of the real ADC transfer function and the central position of ideal ADC transfer function. The central position is given for the ideal transition level of the central code of the ideal ADC output conversion domain, which is $z_c = 2^{n-1}$:

$$ZE_v = l_{z_c} - t_{z_c} \tag{A.9}$$

Expressed in LSB units, it is related to INL as:

$$ZE_{LSB} = \frac{ZE_v}{q} = -INL_{z_c} \tag{A.10}$$

A.1.1 INL corrected for gain and offset contributions

If the real ADC is affected by gain and offset errors, the INL obtained from the expression (A.2) contains a linear contribution that has to be corrected as indicated by the standard (Measurement and Technical, 2011). The linear contribution is performed by fitting the set of real transition levels $\{t_k\}$ to a straight line, obtaining a new set of effective transition levels $\{\tilde{t}_k\}$ that follows the lineal law:

$$\tilde{t}_k = b + a \cdot (k - z_{min}), \quad \forall k \in [z_{min} + 1, z_{max}]$$
(A.11)

The parameters *a* and *b* are calculated by two standardised adjustments (Measurement and Technical, 2011): (1) Best-Fit Line: obtaining the line of best fit by the Least Squares method or (2) End-Line: obtaining the line that crosses the extreme or terminal real transition levels, $t_{z_{min}+1}$ and $t_{z_{max}}$.

This process corresponds to comparing the real ADC not with the ideal ADC but with the ADC whose transfer function best approximates, as indicated above, the real transfer function. Therefore, by comparison with the ideal ADC law (A.1), the parameter *a* corresponds to the quantum or LSB of the best approximate ADC, designated as the effective quantum or LSB q_e , and the parameter *b* corresponds to the lower reference of the best approximate ADC, designated as the effective R_e⁻.

The corrected Integral Non Linearity is:

$$INL_k = \frac{t_k - \tilde{t_k}}{q_e}, \quad \forall k \in [z_{min} + 1, z_{max}]$$
(A.12)

where:

$$\tilde{t}_k = R_e^- + q_e \cdot (k - z_{min}), \quad \forall k \in [z_{min} + 1, z_{max}]$$
(A.13)

From (A.12), the Differential Non Linearity is:

$$DNL_{k} = INL_{k+1} - INL_{k} = \frac{t_{k+1} - t_{k}}{q_{e}} - 1, \quad \forall k \in [z_{min} + 1, z_{max}]$$
(A.14)

The Gain Error and Offset Error parameters can be obtained respectively from:

$$GE_{dimensionless} = \frac{q}{q_e} - 1 \tag{A.15}$$

where $g = q/q_e$ is the gain of the real ADC.

$$z_{os} = \frac{R^-}{q} - \frac{R_e^-}{q_e} \tag{A.16}$$

where z_{os} is in LSB units.

A.2 The Standard Histogram Method

The histogram method is a statistical procedure developed by Joey Doernberg et al. (Doernberg, Hae-Seung, and Hodges, 1984) to obtain the set of transition levels of an ADC and is standardised according to (Measurement and Technical, 2011). It is based on the construction of the histogram of the output codes of an ADC, in response to an input signal with a given waveform whose amplitude probability statistical distribution is known. On the one hand, the probability of occurrence of each output code is obtained from the histogram of the output codes. On the other hand, the probability distribution that the ADC output will follow is known, which is a function of the transitions and the input parameters. From this information the transition levels are obtained.

It is important to highlight that the histogram does not report the location of where the codes are appearing within the ADC analogue domain, only the number of times each code appears, so the set of transition levels obtained is monotonic non-decreasing. This condition of the histogram method produces erroneous results in ADCs with non-monotonic behaviour, since the histogram method will always assign a set of monotonic transition levels to the ADC under test. From now on it is assumed that the ADC is monotonic non-decreasing, being the worst-case behaviour the missing code.

Suppose the histogram method is to be performed to obtain the static parameters of an ADC. For this purpose, an ideal, noise-free, continuous analogue signal x is applied to excite the ADC under test. Consider the peak amplitude of the input signal is A and its DC or offset value is C, being the range of excitation amplitudes of the input signal $x \in [C - A, C + A]$. It is assumed that this range covers the analogue conversion domain of the ADC, causing upper and lower saturation of the ADC output.

The data or codes in response to the previous analogue signal will be captured. Assuming that are acquired M output codes or samples, the code set $\{z_j\}_{j=1toM}$ is obtained. On it, the histogram of codes is calculated by counting the number of times S_z each code z appears in the acquired data set, being the histogram represented as the set $H = \{z, S_z\}_{z \in [z_{min}, z_{max}]}$. It is obvious that M meets:

$$M = \sum_{k=z_{min}}^{z_{max}} S_z \tag{A.17}$$

From the histogram is estimated the probability of occurrence of each code $k \in [z_{min}, z_{max}]$:

$$P_k = \frac{S_k}{M} \tag{A.18}$$

And the probability of occurrence of an output code, z, being less than a given $k \in [z_{min} + 1, z_{max}]$:

$$Q_k = P_{(z < k)} = \sum_{z = z_{min}}^{k-1} P_z,$$
(A.19)

The set $H_P = \{z, P_z\}_{z \in [z_{min}, z_{max}]}$ is called a probability histogram, and the set $H_Q = \{z, Q_z\}_{z \in [z_{min}, z_{max}]}$ is called a cumulative probability histogram.

On the other hand, as it is assume that the distribution function of the ADC input signal is known, $f_x(x; A, C)$, then it is possible to obtain the probability cumulative distribution function followed by the output signal, by means of the transition levels and the amplitude *A* and offset *C* of the input signal:

$$Q_k = P_{(z < k)} = \int_{\infty}^{t_k} f_x(x; A, C) dx = h(t_k; A, C), \quad \forall k \in [z_{min} + 1, z_{max}]$$
(A.20)

Isolating t_k from (A.20) and using the cumulative probability histogram previously computed in (A.19):

$$t_k = h^{-1}(Q_k; A, C), \quad \forall k \in [z_{min} + 1, z_{max}]$$
 (A.21)

Although it is possible to use any waveform whose statistical distribution is known, typically, the histogram method is performed using pure triangular or sinusoidal waveforms as input signals to the ADC under test as they are easily implemented in the laboratory. So, if a triangular or ramp waveform is used as input signal:

$$h(u; A, C) = \frac{(A+C) - u}{2A}$$
 (A.22)

and therefore by (A.21):

$$t_k = C - A \cdot (1 - 2Q_k), \quad \forall k \in [z_{min} + 1, z_{max}]$$
 (A.23)

If a sinusoidal waveform is used as input signal:

$$h(u; A, C) = 1 - \frac{1}{\pi} \arccos(\frac{u - C}{A})$$
(A.24)

and from (A.21):

$$t_k = C - A\cos(\pi Q_k), \quad \forall k \in [z_{min} + 1, z_{max}]$$
(A.25)

When the peak amplitude A and the offset C parameters are known with high accuracy, the transition levels are estimated directly from (A.21) using the suitable expression to the input waveform used. In the case where the input signal parameters are unknown or known with low accuracy, it is possible to obtain them if two widely separated transitions are measured very accurately by an alternative method, solving then the following system of equations with the two unknowns A and C:

$$t_{z_l} = h^{-1}(Q_{z_l}; A, C) \tag{A.26}$$

$$t_{z_h} = h^{-1}(Q_{z_h}; A, C) \tag{A.27}$$

where $z_l > z_{min}$ and $z_h \le z_{max}$ are the codes whose transitions t_{z_l} and t_{z_h} are known. As an example, if the triangular or ramp waveform is used as input signal:

$$A = \frac{1}{2} \cdot \frac{t_{z_h} - t_{z_l}}{Q_{z_h} - Q_{z_l}}$$
(A.28)

$$C = t_{z_h} + A \cdot (1 - 2Q_{z_h})$$
 (A.29)

And if a sinusoidal waveform is used as input signal:

$$A = \frac{t_{z_h} - t_{z_l}}{\cos(\pi Q_{z_h}) - \cos(piQ_{z_l})}$$
(A.30)

$$C = t_{z_h} + A\cos(\pi Q_{z_h}) \tag{A.31}$$

Once the parameters of the input signal are obtained, the rest of the transition levels are estimated from (A.21) using the suitable expression to the input waveform used.

Once the transition levels of the ADC under test are known, the static parameters that characterise its transfer function are evaluated from the expressions given in section (A.1).

In the case where the peak amplitude A and offset C of the input signal cannot be accurately known, an erroneous estimate of the static parameters of the ADC will be obtained, except for those corrected for the gain and offset contribution: the results from expressions (A.12) and (A.14) are independent of the value assumed for the input signal parameters. Thus, when the gain and offset errors are not required and only the non-linearity parameters corrected for their contributions want to be evaluated, it is possible to perform a normalisation process assuming in (A.21) the values A = 1 and C = 0, to obtain the set of transition levels with which to evaluate (A.12) and/or (A.14). The results of this evaluation are identical to those obtained with any other value of A and C.

Appendix **B**

Stimulus Error Identification and Removal: SEIR method

The SEIR algorithm is a method presented in (Jin et al., 2005a) to accurately estimate the Integral Non Linearity pattern of a high resolution ADC using a low linearity generator. The method is based on the use of a Double Histogram, by exciting the ADC under test with two identical low linearity ramp signals but one shifted with respect to the other by a constant offset. The two ADC output data sets contain the information of the ADC transition levels plus the nonlinearity contribution from the generator. Matching the transition levels of the ADC under test from both sets, a system of equations related to the nonlinearity of the generator is obtained. The nonlinearity of the input signal is then parameterized using a set of basis function, whose parameterization coefficients are obtained solving by the Least Square (LS) method the previous set of equations. Once the generator nonlinearity is identified, it is removed from the ADC output data and the nonlinearity of the ADC is accurately estimated.

B.1 Integral Non-Linearity definition

Consider an ADC of *n*-bit of resolution and $N = 2^n$ output codes. The set of transition leves is denoted as T_k with k = 1, 2, ..., N - 1. It is assumed that the ADC is monotonic and with no missing codes.

The INL expression used by (Jin et al., 2005a) is specific to the case where offset and gain correction is performed by means of the terminal-based (or end-line) definition. The transition levels of the linear ADC that fit the transition levels of the ADC under test matching their extreme transitions T_1 and T_{N-1} follow the linear equation:

$$I_k = T_1 + Q_e \cdot (k-1), \quad k = 1, ..., N-1$$
 (B.1)

The slope of the line is $Qe = (T_{N-1} - T_1)/(N-2)$, the effective quantum or Least Significant Bit (LSB) of the fitted linear ADC.

The terminal-based INL expression used is:

$$INL_{k} = \frac{T_{k} - I_{k}}{Qe} = \frac{T_{k} - T_{1}}{T_{N-1} - T_{1}} \cdot (N-2) - (k-1), \quad k = 1, 2, ..., N-1$$
(B.2)

The aim is to calculate de transition levels and obtain the INL, but if the input signal is not pure the transition levels cannot be estimated directly from the output data using the histogram method.

B.1.1 Input signal nonlinearity modeling

In (Jin et al., 2005a) the real linear ramp is modeled in time *t* as:

$$x(t) = x_{os} + \eta t + F(t) \tag{B.3}$$

where x_{os} is the dc offset voltage, ηt is the linear part of the ramp signal and F(t) represents its nonlinear component.

Defining the transition time t_k the time at which the ramp signal is equal to the k^{th} transition level of the ADC, is obtained:

$$T_k = x(t_k), \quad k = 1, ..., N - 1$$
 (B.4)

The input signal is assumed monotonic. In order to make the algorithm independent of the time range in which the test is performed, the authors carry out a normalisation process by considering $t_1 = 0$ and $t_{N-1} = 1$. Considering that the nonlinearity of the input signal is zero at t = 0 and t = 1, that is F(0) = F(1) = 0, (B.3) is expressed as:

$$x(t) = T_1 + (T_{N-1} - T_1)t + F(t), \quad 0 \le t \le 1$$
(B.5)

As the signal input nonlinearity is assumed unknown, in order to identify it F(t) is parameterized as a series expansion over a set of basis function $\{F_j(t), j = 1, 2, 3, ...\}$. In (Jin et al., 2005a) is chosen the trigonometric functions as the set of basis function, resulting on the interval [0, 1]:

$$F(t) = \sum_{j=1}^{M} A_j \sin(j\pi t) + e(t), \quad 0 \le t \le 1$$
(B.6)

where only the first M basis function are included for the series expansion, and e(t) represents the residual due to the unmodeled part of the approximation in M terms. According to the authors, M can always be appropiately chosen so that the residue is small to any desired level. In general, the input nolinearity function can be parameterized as:

$$F(t) \approx \sum_{j=1}^{M} A_j F_j(t), \quad 0 \le t \le 1$$
(B.7)

where $\{A_j\}$ with j = 1, 2, 3, ..., M is the set of M coefficients of the finite series expansion using M basis functions, and satisfying each element of the set that $F_j(0) = F_j(1) = 0$. The term e(t) has been neglected from this expression.

The input signal in (B.5) can be written as:

$$x(t) \approx T_0 + (T_{N-2} - T_0)t + \sum_{j=1}^M a_j F_j(t), \quad 0 \le t \le 1$$
 (B.8)

B.1.2 Integral Non-Linearity evaluation

Once the model of the input signal in time has been obtained, the ADC transition levels are estimated by means of (B.4) and using (B.8):

$$T_k \approx T_1 + (T_{N-1} - T_1)t_k + \sum_{j=1}^M A_j F_j(t), \quad 0 \le t_k \le 1$$
 (B.9)

Replacing (B.9) in (B.2):

$$INL_k \approx (N-2)t_k + \sum_{j=1}^M a_j F_j(t_k) - (k-1), \quad k = 1, 2, ..., N-1$$
 (B.10)

where now the coefficients $a_j = A_j/Q$ are in LSB units. Expression (B.10) gives the ADC nonlinearity per code as a function of the associated transition time and the coefficients of the nonlinearity input. An approximation of the transition times can be estimated using the histogram of the output data: let C_k with k = 0, 1, ..., N - 1 the bin counts obtained in the histogram test for each code. As the ADC samples with a constant period, the time taken

to take a sample is proportional to the number of samples taken up to it. Thus, taking t = 0 as the origin, if C_1 is the number of samples that have been counted from code 1, as the input signal is a ramp, it is possible to evaluate the instant of time at which the last sample with code 1 was taken, as C_1 times the sampling period. Similarly, the last sample of the code 2 was taken at instant $C_1 + C_2$ times the sampling period. In general:

$$\hat{t}_k = T_c \sum_{i=1}^k C_i, \quad k = 1, 2, ..., N - 1$$
 (B.11)

With:

$$T_c = \frac{1}{\sum_{i=1}^{N-2} C_i}$$
(B.12)

where T_c is a scaling factor to set the \hat{t}_k time instants into the normalisation range [0, 1].

As is assumed that the input signal is monotonically increasing, the actual time instant at which the value of the input signal matches one transition level lies between the histogram time instant estimate and the histogram instant time estimate plus one sampling period:

$$\hat{t_k} \le t_k < \hat{t_k} + T_c \tag{B.13}$$

Assuming that the number of samples acquired for the histogram is large enough to make *Tc* very small, the \hat{t}_k time instant will be very close to t_k , being possible the following approximation:

$$t_k \approx \hat{t_k}$$
 (B.14)

And using this approximation in (B.10), the INL_k is:

$$I\hat{N}L_k \approx (N-2)\hat{t_k} + \sum_{j=1}^M a_j F_j(\hat{t_k}) - (k-1), \quad k = 1, 2, ..., N-1$$
 (B.15)

with $\hat{t_1} = 0$ and $\hat{t_{N-1}} = 1$.

Since the unknowns in the expression (B.15) are the coefficients $\{a_j\}$, SEIR approach considers two different histograms to use (B.15) and establish a set of linear equations to solve.
B.2 INL estimation using two nonlinear stimuli

The SEIR approach to testing ADC nolinearity involves using two input signals identical except for a fixed offset between them, to deal with identifying the nolinearity of the ADC input signal and then removing it from the INL calculation. Consider α the constant offset between the two input ramp signals, using the input signal modeling of (B.5) they can be written as:

$$x_1(t) = T_1 + (T_{N-1} - T_1)t + F(t)$$
(B.16)

$$x_2(t) = T_1 + (T_{N-1} - T_1)t + F(t) - \alpha, (\alpha > 0)$$
(B.17)

Input signal x_1 will reach the transition levels of the ADC under test at time instants $t_k^{(1)}$ and input signal x_2 will reach them at time instants $t_k^{(2)}$. So, the set of transition levels of the ADC under test can be evaluated from:

$$T_k = x_1(t_k^{(1)}) \tag{B.18}$$

$$T_k = x_2(t_k^{(2)}) \tag{B.19}$$

Assuming that the offset between the input signals is positive, $\alpha > 0$, it will take a longer time for the second signal to reach a transition level than it will take for the first signal: $t_k^{(1)} < t_k^{(2)}$. Let $C_k^{(1)}$ and $C_k^{(2)}$ with k = 0, 1, ..., N - 1 the bin counts obtained in the histogram test using x_1 and x_2 respectively as the input signals to the ADC under test. Using the histogram data information, transition times can be estimated following a similar procedure to that of (B.11). In this case, in order to perform the normalisation process in time and as two sets of time transitions are available, the time origin will be taken at $t_1^{(1)} = 0$ and the unit time at $t_{N-1}^{(1)} = 1$, being an approximation of the transition times for the first signal:

$$t_{k}^{(1)} = \frac{\sum_{i=1}^{k} C_{i}^{(1)}}{\sum_{i=1}^{N-2} C_{i}^{(1)}}, \quad k = 1, 2, ..., N-1$$
(B.20)

In order to have the same units, the transition times of the second signal must be scaled by the same scaling factor but shifted the offset amount in time generated by the offset α :

$$t_{k}^{(2)} = \frac{\sum_{i=1}^{k} C_{i}^{(2)} - (C_{0}^{(1)} - C_{0}^{(2)})}{\sum_{i=1}^{N-2} C_{i}^{(1)}}, \quad k = 1, 2, ..., N-1$$
(B.21)

Assuming a large number of samples taken for each histogram, INL can be estimated by operating similar as for (B.15):

$$\hat{INL}_{k}^{(1)} = (N-2)t_{k}^{(1)} + \sum_{j=1}^{M} a_{j}F_{j}(t_{k}^{(1)}) - (k-1), \quad k = 2, ..., N-2$$
(B.22)

$$\hat{INL}_{k}^{(2)} = (N-2)t_{k}^{(2)} + \sum_{j=1}^{M} a_{j}F_{j}(t_{k}^{(2)}) - \alpha - (k-1), \quad k = 2, ..., N-2, \quad t_{k}^{(2)} \le 1$$
(B.23)

Only INL_k estimates for which the corresponding transition times are within the domain of the definition for the basis functions are included in (B.22) and in (B.23). As a result of this, the total number of equations available for (B.23) is $N - 3 - \alpha$.

Since $INL_k^{(1)}$ and $INL_k^{(2)}$ are estimates for the INL of the same ADC, they must match code to code. Their respectively expressions (B.22) and (B.23) can be equated to obtain a set of equations involving only the input non-linearity:

$$(N-2)(t_k^{(\hat{2})} - t_k^{(\hat{1})}) = \sum_{j=1}^M a_j(F_j(t_k^{(\hat{1})}) - F_j(t_k^{(\hat{2})})) + \alpha, \quad k = 2, ..., N-2, \quad t_k^{(\hat{2})} \le 1$$
(B.24)

It is possible to express the latter as a matrix equation of the form:

$$\tilde{\lambda}(\gamma) = [\widehat{\Gamma}(\gamma) \quad 1]\tilde{\mathbf{a}}$$
(B.25)

where:

$$(\tilde{\lambda})_{k} = (N-2)(t_{k}^{(2)} - t_{k}^{(1)})$$

$$(\widehat{\Gamma})_{kj} = F_{j}(t_{k}^{(1)}) - F_{j}(t_{k}^{(2)}), \quad \tilde{\mathbf{a}} = (a_{0}, a_{1}, ..., a_{Mp}, \alpha)^{t}$$
(B.26)

The number of equations in (B.24) is $N - 3 - \alpha$ and the number of unknowns is M + 1 (M from the a_j parameters plus the offset α). For high resolutions ADCs, typical values of M and α are much smaller than N. When the number of equations is larger than the number of unknowns, this system of equations is overconstrained and is solved by the Least Square method:

$$\tilde{\mathbf{a}} = \tilde{\lambda}(\gamma) \begin{bmatrix} \widehat{\Gamma}(\gamma) & \mathbf{1} \end{bmatrix}$$
(B.27)

Considering than the solution is given by the parameters and the offset $\{\hat{a}_1, \hat{a}_2, ..., \hat{a}_M, \hat{\alpha}\}$, the esimate of the *INL*_k of the ADC under test can be obtained replacing them, for example, in (B.22):

$$\hat{INL}_{k}^{(1)} = (N-2)t_{k}^{(1)} + \sum_{j=1}^{M} \hat{a}_{j}F_{j}(t_{k}^{(1)}) - (k-1), \quad k = 2, ..., N-2$$
(B.28)

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