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Citation: Journal of Applied Physics **121**, 205302 (2017); doi: 10.1063/1.4984051
View online: http://dx.doi.org/10.1063/1.4984051
View Table of Contents: http://aip.scitation.org/toc/jap/121/20
Published by the American Institute of Physics

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JOURNAL OF APPLIED PHYSICS 121, 205302 (2017)

Modeling of the multilevel conduction characteristics and fatigue profile of $Ag/La_{1/3}Ca_{2/3}MnO_3/Pt$ structures using a compact memristive approach

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(Received 7 March 2017; accepted 10 May 2017; published online 24 May 2017)

The hysteretic conduction characteristics and fatigue profile of $La_{1/3}Ca_{2/3}MnO_3$ (LCMO)-based memristive devices were investigated. The oxide films were grown by pulsed laser deposition (PLD) and sandwiched between Ag and Pt electrodes. The devices exhibit bipolar resistive switching (RS) effect with well-defined intermediate conduction states that arise from partial SET and RESET events. The current-voltage curves are modeled and simulated using a compact memristive approach. Two equations are considered: one for the electron transport based on the double-diode equation and the other for the memory state of the device driven by the play operator with logistic ridge functions. An expression that accounts for the remnant resistance of the device is obtained after simplifying the model equations in the low-voltage limit. The role played by the power dissipation in the LCMO reset dynamics as well as the asymmetrical reduction of the resistance window caused by long trains of switching pulses are discussed. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4984051]

I. INTRODUCTION

Electron transport in rare earth-doped perovskite manganites such as $La_{1-x}Ca_xMnO_3$ (LCMO) has been intensively investigated in the last decade. This material not only exhibits remarkable magnetoresistance properties and intrinsic phase separation effects[1] but also excellent resistive switching (RS) capability when sandwiched between a variety of metal electrodes.[2] Multilevel conduction in LCMO can be achieved by the so-called "electric-pulse-induced reversible" (EPIR) resistance change, which consists of the application of voltage or current pulses with the appropriate polarity with the aim of modulating the conductance of the structure in the selected direction.[3] The EPIR effect can be used for multibit storage in nonvolatile memory devices, and it is a desirable feature for analog computing and neuromorphic circuits as well.[4,5] Within this context, the fatigue effect in LCMO associated with encored EPIR, i.e., the progressive modification of the resistance window caused by electrical stress, is an issue that has deserved special attention because of its connection with lifetime operation.[6] The electron transport in LCMO has been ascribed to a variety of physical mechanisms: Pool-Frenkel or charge emission from traps,[6,7] space-charge limited conduction with exponential trap distribution,[6–9] filling and emptying of microscopic domains,[6,10–12] Schottky conduction,[2,12] polaronic hopping with band bending at the interfaces,[14] and more recently, single or multiple conducting paths with transmission properties modulated by the oxygen concentration at the metal/oxide interfaces.[2,4,15–18] However, most of the reports concerning the electron transport in LCMO focuses the analysis on the microscopic material properties exclusively or on the current-voltage (I-V) characteristics behaviour at the lowest and highest achievable conduction states. To our knowledge, modeling of the current flow in LCMO for arbitrary input signals following a memristive approach has not received much attention. However, this is a fundamental issue for the developement of a compact conduction model suitable for circuit simulators.

As many other RS materials, LCMO-based devices exhibit two extreme conduction states which are referred to as high (HRS) and low (LRS) resistance states. The passages from HRS to LRS and viceversa have been largely attributed to the electric field-induced drift of oxygen vacancies to and from the contact region with the metal electrode, where these species are supposed to modulate the height of the interfacial barrier.[8,19,20] In Ref. 21, the EPIR mechanism is ascribed to the formation of transition layers in the insulating material close to the interfaces as a consequence of the occurrence of redox-type reactions. According to some authors,[22] this phenomenon is ruled by the Gibbs free energy of the metal formation, which implies that there can be different RS mechanisms for the same material with different electrode/material interface structures. All these mechanisms are compatible with the formation of preferred pathways for conduction spanning the oxide film.[2] The transition events from one state to the other are called SET and RESET and they can be abrupt or gradual. They can also occur for applied biases of equal (unipolar RS) or opposite (bipolar RS) polarity. In particular, our devices exhibit bipolar RS with abrupt SET and gradual RESET transitions. The devices were subjected to positive and negative voltages alternately in order to modify

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the oxide conductance in a controlled manner, and the resistance of the structure measured at a low positive bias (remnant resistance). Remarkably, the investigated devices not only present a major *I-V* loop associated with the maximum positive and negative voltage excursions allowed (without introducing irreversible damage) but also well-defined intermediate conduction states arising from partial SET and RESET events. In terms of hysteretic modeling, these intermediate states are called minor I-V loops, which have also been reported in literature for LCMO.[3,23]

In this work, in order to account for the hysteresis phenomenon in the *I-V* curves, we consider a compact memristive approach[24] consisting of two coupled equations, one for the electron transport given by the double-diode equation with series resistance and the other for the memory state of the device driven by the solution of the generalized logistic differential equation (extended Verhulst equation[25]). As will be shown, this latest equation expresses the generation and annihilation of conducting paths in the dielectric film or equivalently the increase and decrease of the effective conducting area. In addition, the reduction of the resistance window, i.e., the difference between LRS and HRS, caused by the fatigue of the material when subjected to long trains of pulses plays a major role in the system dynamics that cannot be overlooked. In this regard, the fatigue effect needs to be phenomenologically characterized since it has important implications for the possible application of these memristive structures in the field of nonvolatile memories. This paper is organized as follows: in Sec. II, the devices and the experimental setup used to switch their conduction states are described. Modeling and simulation results for the I-V characteristics using the compact memristive approach and the fatigue effects associated with EPIR are reported in Sec. III. Finally, in Sec. IV, general conclusions are presented.

II. DEVICE AND MEASUREMENT DETAILS

LCMO thin films with composition $x = 2/3$ were grown by the Pulsed Laser Deposition (PLD) technique on top of commercial Pt/Ti/SiO_2/Si substrates. The temperature and oxygen growth pressure were fixed at 850 °C and 0.13 mbar, respectively. The X-ray (Cu source) diffraction pattern in Fig. 1(a) shows that LCMO grows polycrystalline without evidence of secondary phases. Both the surface and the cross-section of the films were visualized by scanning electron microscopy (SEM). In the latest case, a small volume of material was physically removed with a focused ion beam. The SEM image in Fig. 1(b) shows a dense network of well connected nanograins without the presence of particulates on the surface. The cross section in Fig. 1(c) shows that the Pt, which acts as a bottom electrode, and LCMO layers are 100 and 88 nm thick, respectively. The silver top electrode was fabricated according to the sketch shown in the inset of Fig. 1(c). Silver pillars with areas ranging from 1 μm × 1 μm to 10 μm × 10 μm, embedded in an insulating SiO_2 matrix, were fabricated by a combination of standard electronic lithography, sputtering (for the SiO_2), thermal evaporation (for the silver), and ion etching. The top of the pillars end in macroscopic pads for the electrical contact with standard

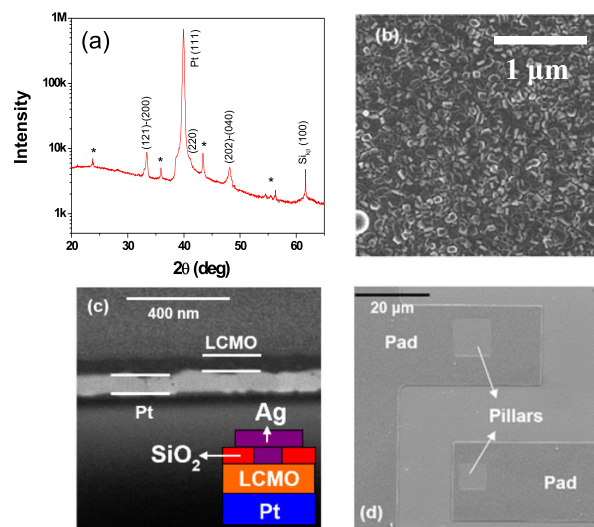

FIG. 1. (a) X-ray diffraction pattern of the LCMO film. Peaks marked with an asterisk correspond to a small amount of crystalline SiO_x—buried below the bottom Pt electrode—that it is formed during the substrate heating during the LCMO deposition. (b) Scanning electron microscopy image of the deposited material. (c) Cross-section scanning electron microscopy image of the device and sketch showing the silver pillar through the SiO_2 film. (d) Scanning electron microscopy image of the structures including electrical pads and pillars.

probe station tips. Figure 1(d) shows a top view of the final device, where both pillars and pads are clearly seen.

The devices were characterized using pulsed *I-V* measurements at room temperature with a Keithley 2612 source-meter. This means that positive and negative pulses of increasing or decreasing magnitude were applied to the structure in order to generate major and minor *I-V* loops. Figure 2 illustrates typical examples of cyclical major *I-V* loops. Figures 2(a) and 2(b) were obtained using current compliances of I_C=5 mA and I_C=10 mA during the SET process, respectively. The electrical stimulus was applied to the top electrode with the bottom electrode grounded. The time width of the applied pulses was 1 ms. After the application of each pulse, a small reading voltage V_M of 0.1 mV or 0.15 mV is applied across the structure, and the current measured. This information is used to calculate the remnant resistance R_M of the structure, which in turn is used to evaluate the fatigue profile for both HRS and LRS. The remnant resistances are shown as insets in Figs. 2(a) and 2(b). Notice that if the damage caused to the device is under control (lower I_C), the R_M loop does not change too much as the number of cycles increases. However, if the maximum allowed current for the SET process is higher, the resistance window shrinks because of a reduction of the switching capability of the structure. No electroforming step is required to activate the switching property of our samples.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Modeling and simulation of the I-V characteristics

In order to model the hysteretic *I-V* characteristic (see Fig. 3), we assume that electronic transport takes place along multiple conducting pathways spanning the oxide layer with their resistance dominated by potential barriers present at

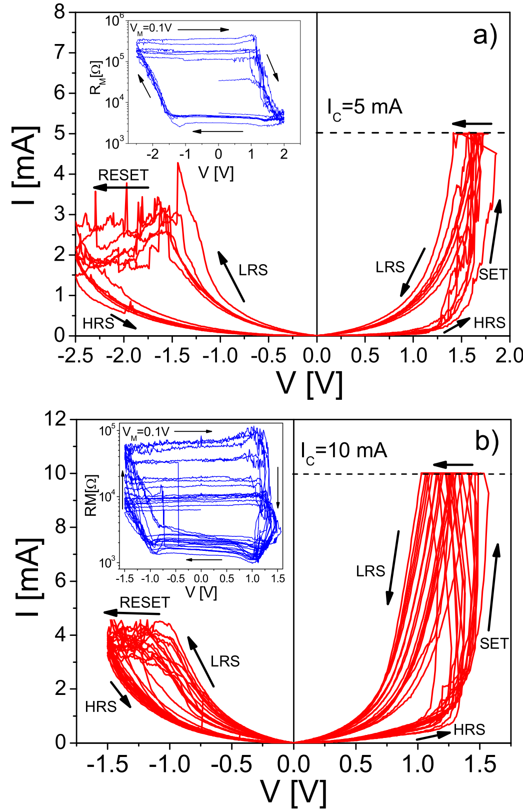

FIG. 2. (a) Experimental *I-V* characteristics obtained with a current compliance of 5 mA. (b) Experimental *I-V* characteristics obtained with a current compliance of 10 mA. In both cases, the insets show the corresponding remnant resistance loop. Notice that both LRS and HRS exhibit nonlinear dependence with the applied voltage.

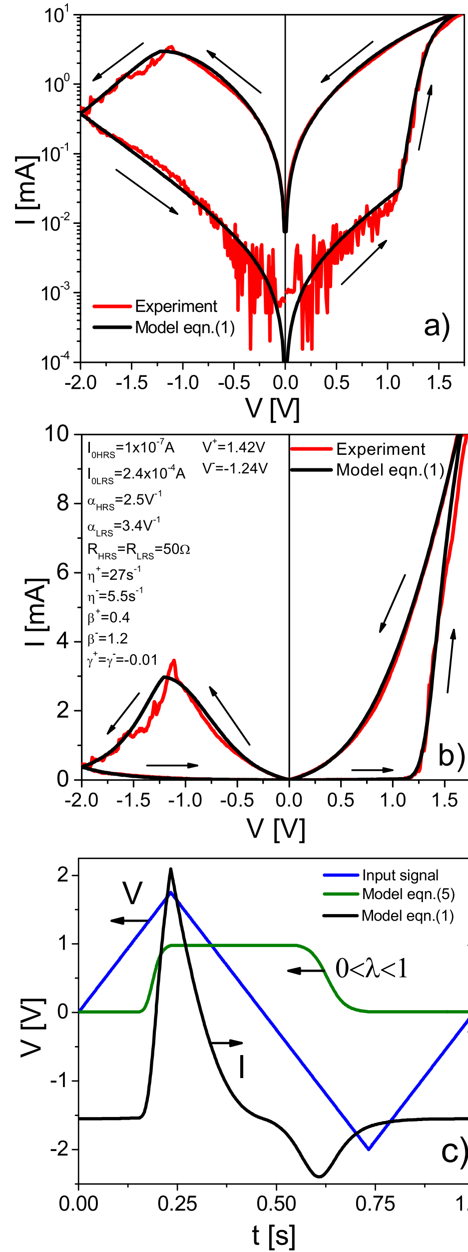

FIG. 3. (a) Experimental and model results for a typical major *I-V* loop in log-linear axes. (b) Same experimental and model results shown in (a) but in linear-linear axes. Notice the excellent agreement in both representations. The model parameters used in expressions (1) and (4) are shown in (b). Figure (c) illustrate the evolution of the current and memory state.

one or at both metal-oxide interfaces.[13,14,16] The height of these barriers is modulated by the oxygen vacancies concentration at the interface, which can be modified by the external field. According to a number of publications, these barriers are not spatially uniform so that the formation probability of conducting paths would be higher in those zones where the barriers are lower and would increase with the magnitude of the external electrical stress.[4,8,26] Interestingly, Jooss *et al.*[14] have demonstrated that for some electrode materials, upbending of the manganite conduction band at both oxide interfaces can occur. In this case, the band structure of the device resembles two opposite Schottky contacts. This would be consistent with the independence of the EPIR effect on the oxide thickness as reported in Ref. 4. For our devices, both LRS and HRS currents are almost symmetrical for positive and negative biases which is likely associated with the presence of a single barrier, presumably located at the Ag/LCMO interface.[16] We recall that the Pt/manganite interface was reported as ohmic due to the large work function of Pt (5.65 eV).[27] This implies that in our samples, the manganite/Pt interface does not contribute to the EPIR effect. Following this observation, and for the sake of simplicity, it will be assumed that the device exhibits nonrectifying diode-like behaviour.[11] In this case, the *I-V* curve can be expressed in terms of the double-diode equation[28] as

$$I = \mathrm{sgn}(V)\left[(\alpha R)^{-1} W\{\alpha R I_0 \exp\left[\alpha(|V| + R I_0)\right]\} - I_0\right], \quad (1)$$

where I_0 and α are model parameters related to the effective conducting area and to the particular features of the potential barrier, respectively, R a series resistance associated with the non-switchable region of the device,[29,30] *sgn* the sign function, and W the Lambert function.[31] A model parameters vector of the form $\Omega = (I_0, \alpha, R)$ is defined as $\Omega = \Omega_{HRS} + \lambda(\Omega_{LRS} - \Omega_{HRS})$, where $\Omega_{HRS} = (I_{0HRS}, \alpha_{HRS}, R_{HRS})$ and $\Omega_{LRS} = (I_{0LRS}, \alpha_{LRS}, R_{LRS})$ are the two ends of the vector Ω. $0 < \lambda < 1$ is the memory state variable of memristive systems and within this framework can be thought of as the fraction of activated conducting paths at a given applied voltage.[28] Equation (1) also yields a pinched I-V characteristic [$I(V = 0) = 0$], as required by memristive systems. From

Eq. (1), R_M can be simply calculated as the device resistance at low applied bias, i.e.,

$$R_M = \frac{V}{I} \approx R + \frac{1}{\alpha I_0} \approx \lambda^{-1}, \quad (2)$$

which, at first order, is proportional to λ^{-1} as long as $R \ll (\alpha I_0)^{-1}$. This condition is always met by our devices since R is in the range 1–50 Ω, α in the range 2–3 V^{-1}, and I_0 in the range 10^{-7}–10^{-4} A. Next, it is assumed in a first approximation that the generation and annihilation of conducting paths are described by the logistic function

$$L^{\pm}(V) = \left\{1 + \exp\left[-\eta^{\pm}V\right]\right\}^{-1}, \quad (3)$$

where $\eta^{\pm}$ is a constant related to the voltage transition rate from one state to the other. The signs + and – denote the generation and destruction of conducting paths, respectively, associated with the intensity and polarity of the external stimulus. From (3), $L^{\pm}(V \to \infty) = 1$ and $L^{\pm}(V \to -\infty) = 0$, which means that for large positive and negative voltages all the conducting paths are activated or disrupted, respectively. Importantly, as illustrated in Fig. 4, this case corresponds approximately to the progressive generation/destruction of conducting paths according to gaussian-distributed activation/deactivation voltages.[28] Since we are pursuing a compact approach, in order to improve the fitting results, it is worth using a generalised version of Eq. (3). To this end, the ridge functions $\Lambda^{\pm}$ are defined as

$$\Lambda^{\pm}(V) = \left\{1 + \left[\left(2^{\beta^{\pm}} - 1\right)^{\gamma^{\pm}} - \eta^{\pm}\gamma^{\pm}\beta^{\pm}V\right]^{\frac{1}{\gamma^{\pm}}}\right\}^{-\frac{1}{\beta^{\pm}}}, \quad (4)$$

where $\eta^{\pm}$, $\beta^{\pm}$, and $\gamma^{\pm}$ are the shape parameters. Expression (4) is the solution of the generalised logistic differential equation.[25] Remarkably, for $\beta^{\pm} = 1$ and $\gamma^{\pm} \to 0$, Eq. (4) reduces to the standard logistic function Eq. (3), i.e., $\Lambda^{\pm}(V) \to L^{\pm}(V)$. The effect of considering different $\beta^{\pm}$ and $\gamma^{\pm}$ values is to modify the tails of the distributions with the aim of capturing the shape of the experimental *I-V* curve during the transitions HRS ↔ LRS. $\gamma^{\pm} < 0$ yields distributions skewed to the right, whereas $\beta^{\pm} > 1$ yields distributions skewed to the left (see Fig. 4). The extension of these tails can be physically linked to the presence of the series resistance at the largest biases or to a change of the switching mechanism at low currents.[32] As mentioned above, $\eta^{\pm}$ gives the voltage transition rate and is mathematically related to the dispersion of the distributions.

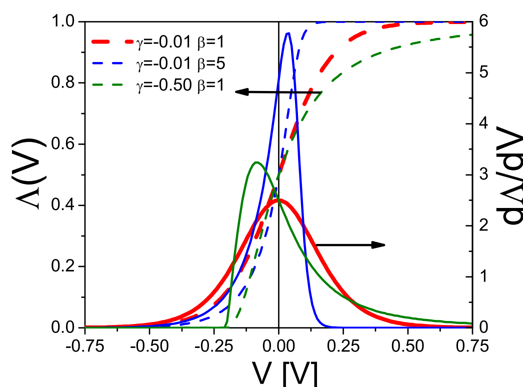

FIG. 4. Plot of the ridge functions Λ (dashed lines) and their derivatives dΛ/dV (solid lines) for different combinations of shape parameters. Notice the skewness of the distributions. The ridge functions describe the creation and annihilation of conducting paths in the oxide material. These functions are used to construct the recursive operator that controls the current magnitude.

In addition, since we are dealing with a hysteretic phenomenon, the evolutionary behaviour of the device needs to be taken into account. To model the memory state of the device, the *play* operator proposed in Ref. 33 is considered

$$\lambda(V) = \min\{\Lambda^{-}(V - V^{-}), \max[\lambda(V - \Delta V) + \kappa(V, I, \lambda)\Delta t, \Lambda^{+}(V - V^{+})]\}, \quad (5)$$

where V is the applied voltage, min(x,y) and max(x,y) are the minimum and maximum of x and y, respectively, $\kappa = d\lambda/dt$ is a function that describes the evolution of λ for a constant input signal, and V^{+} and V^{-} describe the voltage location of the SET and RESET distributions. $\Delta V > 0$ and $\Delta t > 0$ are the voltage and time steps used for the simulation. Equation (5) is a recursive expression that yields the state of the system at time t as a function of the state of the system at time $t - \Delta t$. Notice that Eq. (5) represents the memory state equation of memristive systems.[34] Remarkably, (5) is not expressed in the usual way, i.e., as a differential equation, because the threshold functions $\Lambda^{\pm}(V)$ are already integrated functions. $\lambda(V)$ is used to calculate the vector Ω required for the model parameters in the *I-V* expression (1). The simplest hysteresis dynamics is achieved with $\kappa = 0$ in Eq. (5), which corresponds to a flat response of the memory state for $\Lambda^{-}(V - V^{-}) \leq \lambda(V) \leq \Lambda^{+}(V - V^{+})$. In this case, Eqs. (1) and (5) are decoupled and the time step does not play any role, implying that no drift or accumulation effect is involved in the calculation of the memory state. From the viewpoint of hysteretic systems, this is called a rate-independent process with a wiping-out property.[33] Model results for a typical major *I-V* loop obtained with Eqs. (1), (4), and (5) are illustrated in Figs. 3(a) and 3(b). Notice the good agreement between the experimental and model curves both in log-linear and linear-linear scales. For the sake of clarity, Fig. 3(c) shows the input signal V, the memory state λ [Eq. (5)], and the current I [Eq. (1)] as function of time. Contrary to what is commonly observed in many RS materials, the LRS *I-V* curve in LCMO is not linear, which allows discarding the formation of metallic filaments bridging both electrodes (an ohmic-type dependence should be expected in that case). This observed behaviour is instead consistent with the presence of some kind of potential barrier at the ends or within the conducting paths. In order to shed light on the role played by the main parameters of the model, Fig. 5 illustrates the effects of (a) minimum (I_{0HRS}) and maximum (I_{0LRS}) diode current amplitudes, (b) slopes of the HRS and LRS *I-V* characteristics (α_{HRS} and α_{LRS}), and (c) series resistances (R_{HRS} and R_{LRS}) for both conduction modes. This is the minimum number of parameters required to simulate the magnitude and shape of the two stable states, HRS and LRS. Notice that R_{HRS} and R_{LRS} determine whether the *I-V* curves follow a linear or an exponential dependence on the applied voltage.

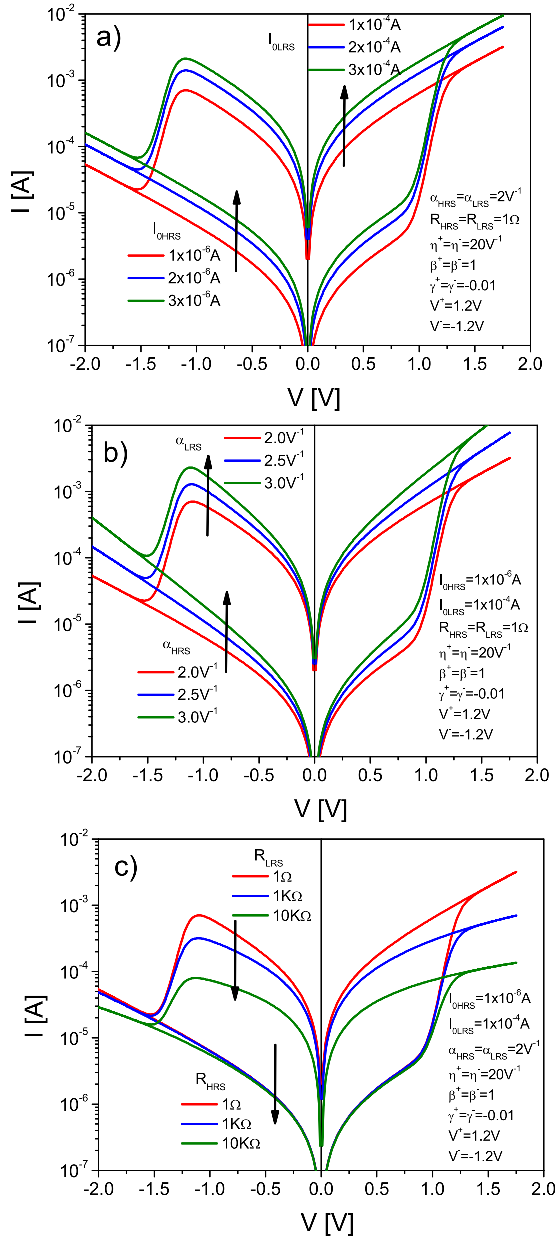

FIG. 5. Effects of the diode model parameters [Eq. (1)] on the *I*-*V* curves: (a) diode current amplitude I_0, (b) slope α, and (c) series resistance R. The rest of parameters are indicated in the figures.

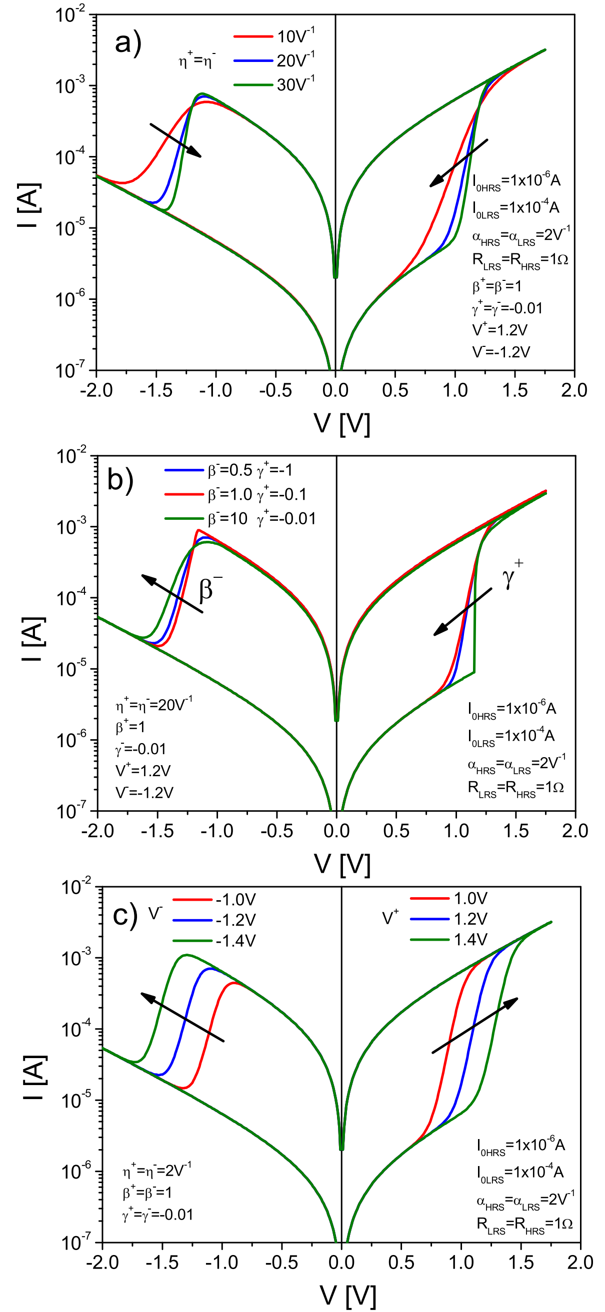

FIG. 6. Effects of the transition parameters [Eq. (4)] on the *I*-*V* curves: (a) general slope η, (b) shape parameters β and γ, and (c) location of SET and RESET voltages (V^+ and V^-). The rest of parameters are indicated in the figures.

To complete the picture, Fig. 6 illustrates the role played by the rest of model parameters, in this case, those corresponding to the transition profiles: effect of (a) transition rate parameter (η), (b) type of outset for the SET and RESET transitions (smooth or sharp) given by the generalized logistic equation (β and γ), and (c) location of the SET and RESET transition voltages (V^+ and V^-). In all cases, the plots were obtained considering $\kappa = 0$ in Eq. (5). In some cases, the parameters for the HRS and LRS *I*-*V* curves are the same.

With the aim of improving the simulation results for the minor *I*-*V* loops corresponding to arbitrary positive and negative voltage pulse sequences [Fig. 7(a)], a correction function of the form $\kappa(I) = -AI^B$, where $B = 2$ and $A > 0$ is a fitting constant, is introduced into Eq. (5). This additional term only applies for the RESET dynamics and with increasing voltages. The negative sign in κ means that the current induces a reduction of the memory state λ. This particular dependence of κ on I arises from our own observations and from the results reported in Ref. 2 concerning the Joule heating effect in manganite-based RS devices. According to that study, the power dissipated in LRS increases the local temperature of the conducting path which in turn raises its resistance by favouring the migration of oxygen vacancies towards the device interface. The change in the resistance $\Delta R \sim I^2$ has been experimentally confirmed by Lee *et al.*[35] Similar arguments for the annihilation of conducting paths

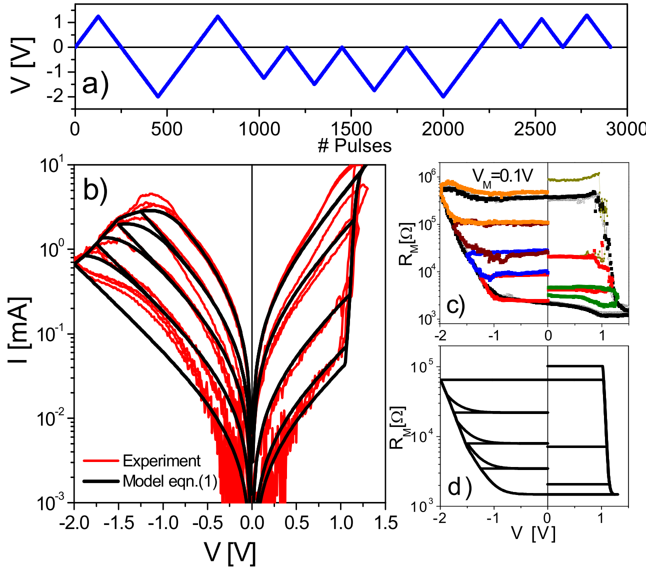

FIG. 7. (a) Sequence of positive and negative voltage pulses required to generate major and minor *I-V* loops. Major loops consist in sweeping pulses of amplitudes in the range −2 V to +1.5 V. Minor loops are attained by increasing the negative maximum limit from −1 V to −2 V. (b) Experimental and simulated *I-V* characteristics. (c) Experimental remnant resistance loops corresponding to the curves shown in (b). (d) Model results for the remnant resistance calculated using Eq. (2). The evolutionary function $\kappa(I) = -10^6 I^2$, $\Delta V = 0.01$ V, and $\Delta t = 0.01$ s were considered in Eq. (5).

during the RESET process were invoked in Ref. 15. The simulated *I-V* curves using the correction term mentioned above are illustrated in Fig. 7(b). Interestingly, since $\lambda \sim R_M^{-1}$ from Eq. (2), the remnant resistance provides complete information about the shape of the memory loop λ vs V. The sigmoidal curves associated with the ridge functions $\Lambda^{\pm}$ and the minor remnant resistance loops are shown in Figs. 7(c) and 7(d) for the experimental and simulated curves, respectively. Notice the effect of including $\kappa(I) \sim -I^2$ in Eq. (5). This appears as an upward bending of R_M in the RESET quadrant. The difference between experiments and simulations for R_M in HRS can be ascribed to the noisy behavior of the measured current at so low reading voltage ($V_M = 0.1$ V). Similar R_M vs V curves can be found in Ref. 35. Interestingly, the formation of minor *I-V* loops was also investigated in connection with the electroforming behaviour of silver-manganite interfaces.[36]

As an additional test for the proposed compact model, experimental and simulation results corresponding to the application of short trains of pulses of increasing negative magnitude [see Fig. 8(a)] are shown in Fig. 8(b). This figure shows experimental (symbols) and model (solid lines) results for a RESET pulse sequence with voltage amplitudes: −1, −1.25, −1.5, −1.75, and −2 V. In this particular case, simulations were performed using $\kappa = 0$ in Eq. (5) since no drift effects were observed in λ for short-term degradation. The initial memory state of the device is $\lambda(0) = 1$, which means that all the conducting paths are in the SET condition at the outset of the RESET process. Figure 8(c) shows again experimental and simulation results for the repetitive application of the already mentioned pulse pattern. Multilevel conduction with a high degree of repeatability in PLD-grown LCMO-based RS devices is thus demonstrated using EPIR.

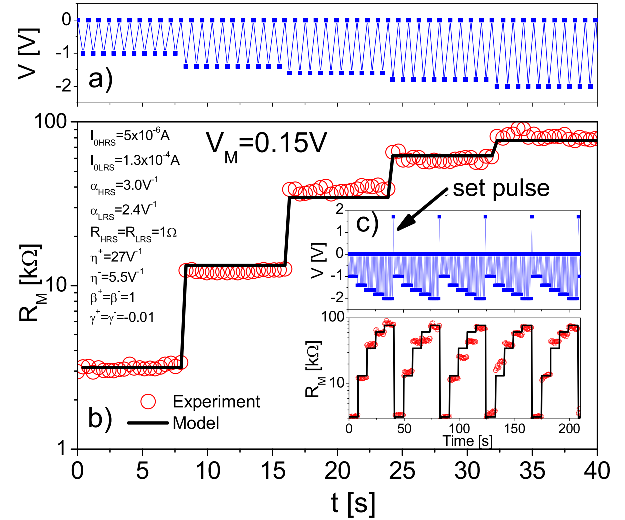

FIG. 8. (a) Sequence of RESET pulses with negative amplitude. (b) Increase of the device resistance caused by the RESET pulses. Symbols and lines are experimental and simulation results, respectively. Model parameters are indicated in the figure. (c) Repetition of the pulse sequence shown in (a). The positive pulse is used to SET the device before each RESET pulse sequence.

Similar results are obtained for an arbitrary sequence of positive and negative pulses as those shown in Fig. 9(a). In this case, the device is progressively reset by an increasing sequence of negative pulses, set by a single positive pulse and again reset by an increasing sequence of negative pulses but with different ramp rates [see Fig. 9(b)]. Subsequently, the remnant resistance of the device is measured without changing its memory state, and finally, a new sequence of SET pulses with increasing voltage is applied in order to progressively reduce the resistance of the device. The evolution of λ is also illustrated in Fig. 9(b). Notice that λ does not start from zero since the initial state of the device is LRS. Within the reproducibility limits, both the experimental and simulated results show good agreement, demonstrating once again the versatility of the proposed approach.

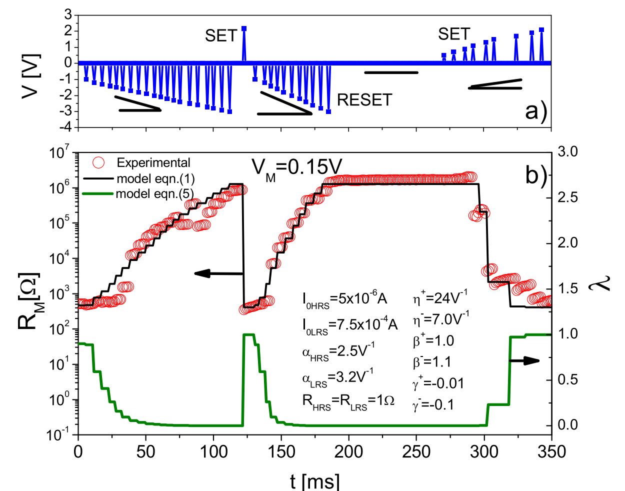

FIG. 9. (a) Arbitrary sequence of SET and RESET pulses with different ramp rates. (b) Evolution of the current for the pulse sequence illustrated in (a). The evolution of the memory state is also represented in the same plot.

B. Characterization and simulation of the fatigue profile

After presenting the hysteretic model that accounts for multilevel conduction in Ag/LCMO/Pt structures, it is worth focusing the attention on the transient effects related to the stabilization of the switching dynamics. In this case, pulses of opposite or similar polarities are applied, leading the device to the SET and RESET conditions alternately. As in Sec. III A, the remnant resistance R_M is always measured at a low positive bias. In general, the transient effects in LRS and HRS are dissimilar and can last several hundreds of cycles. The phenomenon is often called the fatigue effect and has been reported many times in the past for LCMO.[5,12,13,37] In terms of the model discussed in Sec. III A, the modifications in LRS and HRS can be straightforwardly linked to modifications of the model parameters I_{0LRS} and I_{0HRS}, i.e., the maximum and minimum diode current amplitudes in Eq. (1), respectively. Simulated effects of the I-V and R_M-V characteristics are illustrated in Figs. 10(a) and 10(b), respectively.

Here, a simple expression for the evolution of LRS and HRS as a function of the number of switching pulses is proposed. The expression not only covers the asymmetric fatigue profile of both resistance states but can also be used to characterize the EPIR ratio of the device,[6] a relevant figure of merit when dealing with bistable nonvolatile memory structures. Figure 11(a) illustrates the effect of positive and negative voltage pulses on the resistance state measured at 150 mV. It can be seen that, before stabilization, there is a remarkable reduction of the resistance window at the beginning of the cycling experiment. Both HRS and LRS can be described by a first order fitting profile of the form

$$R(n) = R(0) + \big(R(\infty) - R(0)\big)\exp(-n/\tau), \tag{6}$$

where n is the pulse number, $R(n)$ the resistance, $R(0)$ the initial resistance, and $R(\infty)$ the long-run resistance. τ is a characteristic number of pulses associated with the transient effect. Expression (6) is typical of a self-saturation process.[20] As shown in Fig. 11(a), the resistance window not only decreases but there is also an asymmetry in the fatigue profile since τ is larger for LRS ($\tau = 550$) than for HRS ($\tau = 33$). This behavior can be likely attributed to a reaccommodation of the defects or vacancies that modulate the conductive path resistances rather than to a global increase of the conducting area. The same trend has been previously reported for LCMO layers,[13,22] including the distinctive behaviours for HRS and LRS.[38] In addition, the EPIR ratio is defined as

$$EPIR(n) = \frac{R_{HRS}(n) - R_{LRS}(n)}{R_{LRS}(n)}, \tag{7}$$

which expresses the relative change of resistances as the degradation proceeds. According to Fig. 11(b), the EPIR ratio reduces from 10^4 to 10^1, which indicates that while the structure always exhibits a well-defined bistable behavior, the fatigue effect cannot be overlooked for long-run device operation. Figure 9 reveals that the resistance profile given by Eq. (6) can be applied to describe the evolution of the unfolded remnant resistance loop as well. In this case, the unfolded data correspond to the resistance loops shown in Fig. 12(a). Notice that the value $\tau \approx 10^3$ is radically different from what was found in the previous experiment. This occurs because, here, n represents the number of pulses required for achieving complete I-V loops instead of alternately conducting states. The same data are also shown in log-log [Fig. 12(b)] and log-linear axes [Fig. 12(c)]. The asymmetry in the

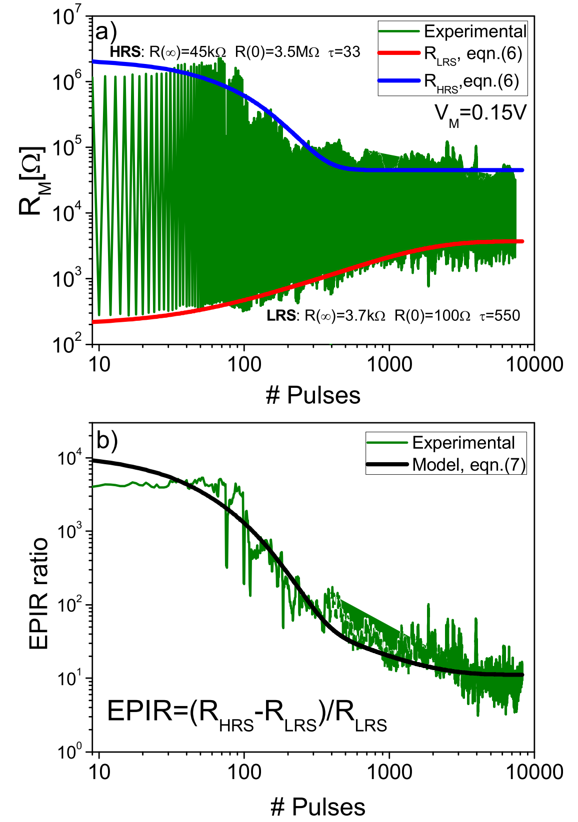

FIG. 11. (a) Experimental and simulated fatigue profile (remnant resistance) for LCMO under switching pulses. The upper and lower envelope functions were obtained using expression (6). (b) EPIR ratio calculated from the data shown in (a) using Eq. (7). Notice that the EPIR ratio also follows a sigmoidal curve.

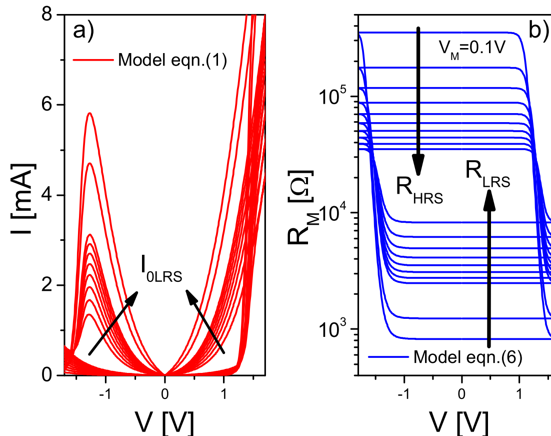

FIG. 10. (a) Simulated I-V curves taking into account a reduction of the maximum (I_{0LRS}) and minimum (I_{0HRS}) current parameters. (b) Effect of the reduction of I_{0LRS} and I_{0HRS} on the remnant resistance R_M. For the sake of simplicity, a symmetrical reduction of the resistance window was considered in this case.

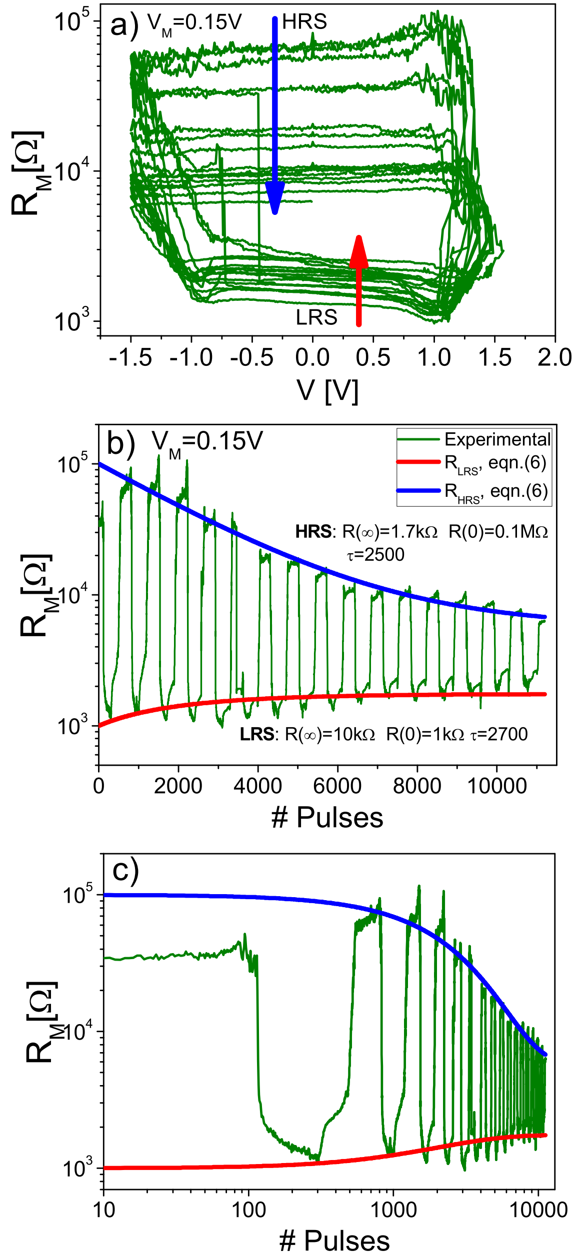

FIG. 12. (a) Remnant resistance loop showing fatigue effects. The blue and red arrows point out the reduction and increase of the HRS and LRS states, respectively. (b) Unfolded remnant resistance loop obtained from (a) as a function of the number of pulses. Notice the reduction of the resistance window as the degradation proceeds. (c) Same results of (b) but in log-log axes. Fitting parameters are shown in the figures.

resistance values asssociated with the stable states is still visible so that, comparing with the results shown in Fig. 11, it can be stated that either in the case of voltage increasing/decreasing switching pulses or in the case of switching pulses with opposite polarity, the fatigue effect is related to a reduced trajectory within the memory map of the device. Importantly, in order to increase the endurance of similar devices, a protocol based on a proper selection of the pulse amplitudes has been proposed in Ref. 39.

To conclude this section, Fig. 13(a) illustrates the effect of stressing the device at a constant negative voltage. The different remnant resistance curves correspond to different bias conditions (from 1 V to 1.4 V). Clearly, the transition

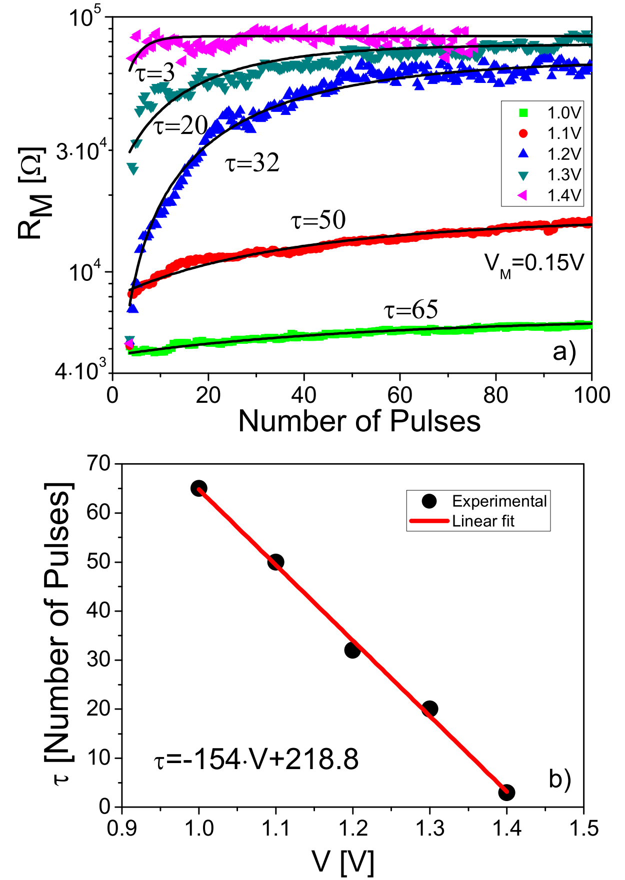

FIG. 13. (a) Evolution of the remnant resistance as a function of the number of pulses. Each curve corresponds to a different negative applied voltage. All the curves start in LRS and evolve toward HRS. (b) Characteristic number of pulses (transient effect) for each applied voltage. Notice that T follows a linear relationship with V.

from LRS to HRS takes a shorter time for a higher applied bias. Again, the RESET profile under this circumstance can be described by Eq. (6), which seems to express the exhaustion of conducting paths or equivalently the progressive reduction of the effective conducting area for long-term stresses. Remarkably, the transient time (in terms of the pulse number) follows a well-defined relationship with the applied voltage ($\tau = -154 \cdot V + 218.8$ [#Pulses]). This result is reported in Fig. 13(b), which indicates that the transition is almost instantaneous ($\tau \approx 0$) for applied voltages larger than 1.42 V.

IV. CONCLUSIONS

A compact memristive model for the hysteretic conduction characteristics of LCMO films with metal electrodes was presented. The formation of conducting paths with transmission properties modulated by the presence of a local potential barrier is assumed for the electron transport. The model parameters are controlled by sigmoidal curves that represent the activation and deactivation of these paths. The exponential behaviour of both the HRS and LRS I-V characteristic seems to indicate that this potential barrier, presumably located at the Ag/LCMO interface, is always present regardless of the conduction state. The memory state variable that accounts for the history of the device is described

using a recursive operator with voltage thresholds. Contrary to previous approaches for the low and high conduction states, the reported model can deal with arbitrary input signals. This is of utmost importance in compact modeling for circuit simulators. In addition, the transient fatigue effect detected in our samples indicates that a large number of the involved conducting paths are not able to withstand a long-term switching process. To our understanding, the main point for LCMO as functional oxide is the possibility of a continuous modulation of the electron transport transmission properties, a crucial feature for analog computing and neuromorphic applications. We suggest that the proposed model could bridge the gap between basic material research and specific applications such as multilevel conduction in non-volatile memory devices or electrical synapses.

ACKNOWLEDGMENTS

We acknowledge financial support from CONICET (Project No. PIP 291), CIC-Bs. As. and ANPCyT (PICT2013 0788). E.M. aknowledges the César Milstein-Raíces Program from Ministerio de Ciencia, Tecnología e Innovación Productiva, Argentina, PANACHE-ENIAC Joint Undertaking, and DURSI of the Generalitat de Catalunya 2014SGR384. The authors also thank J. Lecourt for the preparation of the LCMO target, F. G. Marlasca for technical assistance during the electrical measurements, and F. Golmar for the use of the SEM-FIB facility.

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