Design, Fabrication, and Testing of Silicon-integrated Li-ion Secondary Micro Batteries with Interdigital Electrodes

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Abstract. This paper reports the design, fabrication, and testing of silicon-integrated lithium ion secondary micro batteries with a side-by-side electrode setup. Cavities separated by narrow silicon spacers served as containments for two interdigitally arranged electrodes and were etched into <110>-Si by wet chemical etching. The etched silicon battery containments were passivated by a layer of SiO_x/Si_xN_y. Al current collectors were applied by sputtering and back etching. A volumetric micro dispenser served to fill the cavities with slurries of the active materials - lithium cobalt manganese oxide ($Li_y(Ni_{1/2}Co_{1/5}Mn_{3/10})O_2$) as the cathode and lithium titanate ($Li_4Ti_5O_{12}$) as the anode material. Filling with electrolyte, encapsulation, and electrochemical characterization of the finished cells took place in an Ar-filled glove box. The fabricated batteries with IDE show considerably lower impedances than cells with single side by side electrodes and are capable of constant current loads up to 10 C. A linear capacity loss rate of <0.1 % per cycle was observed over 30 full cycles at 0.2C.

1. Introduction

The fabrication of silicon integrated micro batteries appears to be of interest for applications where a small volume, high capacity energy supply is needed. Examples are small energy autarkic sensors, e.g. implantable sensors for medical applications [1][2], miniaturized sensor networks [3], active smart labels, or MEMS. Such applications cannot be supplied by state of the art solid state batteries due to their limited specific capacity per area which usually accounts for values of around 100 µAh/cm² only [1][3]. As the size of the battery decreases, the amount of passive packaging material in proportion to active material will increase. For very small systems this is reducing the energy density significantly. Therefore, the direct integration of the battery into the chip or package is crucial for highly miniaturized applications.

2. Design

Previously, we investigated a battery design with two electrodes lying side by side, separated by a silicon spacer (figure 1a) [4]. As compared to a conventional setup with stacked electrodes [5], such a setup facilitates assembly and encapsulation considerably since no polymer separator is needed and

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both electrodes can be contacted from downside. However, because of the comparatively high cell impedance due to the long paths of Li-ion movement, the fabricated cells have shown a rate capability that was limited to < 5C. In this study we therefore developed the side-by-side electrode concept further to a design with narrower and interdigitally arranged electrodes (figure 1b).

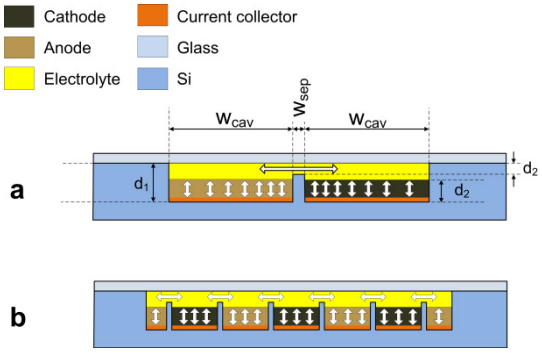

Figure 1. Schematic profiles of battery cells with a side-by-side electrode setup **a**: previous design, **b**: design with IDE (arrows indicate paths of Li-ion movement)

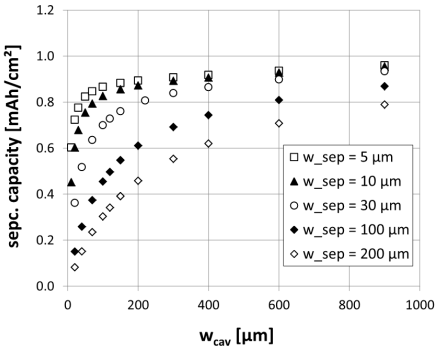

Figure 2. Specific capacity of microbatteries with IDE as function w_{cav} and w_{sep} (d_3~160 µm; reference area is footprint of IDE without package; capacities extrapolated from practically achieved values)

In an IDE setup the width of the separator (w_{sep}) must be minimized to limit losses in specific capacity per area, especially if the cavities are very narrow (figure 2). However, since the active electrode materials undergo volume changes during cycling, the feasible aspect ratio of w_{sep} : (d_1-d_2) is limited to provide for sufficient mechanical stability. Furthermore, the dimension of w_{sep} and d_2 determine the shape of the separator tip, which in turn influences the process of dispensing the electrode materials. Separators that have flattened tips are beneficial for a reliable separation of the electrodes (see section 3.2). Based on these findings and a preliminary investigation on the etch behavior at the separator (see section 3.3), we chose to fabricate IDE with cavities of 600 and 900 µm in width and 100 µm wide silicon spacers. The clearance above the silicon spacer was set to 80 µm.

3. Fabrication

3.1. Fabrication of the electrode containments

Silicon chips structured as shown in figure 1b were fabricated from a p(B) <110>-silicon substrate by applying two steps of wet chemical etching. In the first etching step, two cavities separated by a Si-spacer of full height are formed, whereas the second etching step gives rise to a clearance above the Si-spacer as well as a tapering of its edges. The substrates were passivated by a double layer of SiO_x/Si_xN_y. A 1 µm thin film of Al was applied by sputtering and structured by back etching to serve as current collector for the cathode and the anode, respectively. A more detailed description of the single processing steps can be found in [4]. Figure 3a shows electrode containments ready for dispensing the active electrode materials.

3.2. Deposition of active materials and encapsulation

The active materials for cathode and anode were prepared from slurries of commercially available powders. Lithium cobalt manganese oxide ($Li_y(Ni_{1/2}Co_{1/5}Mn_{3/10})O_2$, NCM) was used as the cathode and lithium titanate ($Li_4Ti_5O_{12}$, LTO) as the anode active material (both from MTI Corp.), polyvinylidene difluoride (PVDF) as a binder, N-methyl-2-pyrrolidone (NMP) as a solvent, and carbon black as a conductive agent. The slurries were applied to the cavities by two proceeding steps of volumetric micro dispensing (Ultimus IV, Nordson) and the solvent removed by appropriate heat treatment. Depending on their individual consistency, the electrode slurries are likely to ascend the

walls of the etched cavities due to capillary action during dispensing, especially at the slanted edges of the tips of the silicon spacers that feature a rough, disintegrated surface. The separation of the electrode slurries is mainly based on edge effects. Thus, for a reliable separation of the electrodes, separators that have flattened tips (four edges) are necessary (figure 4).

The battery containments with the applied electrodes were introduced into an Ar-filled glove box and sealed and filled with electrolyte as described in [4]. The bond interface adds up some 20 µm to the final dimension of d_2. We used 1M $LiPF_6$ dissolved in a mixture of ethylene carbonate and dimethylcarbonate (EC:DMC, 1:1wt%) as the electrolyte.

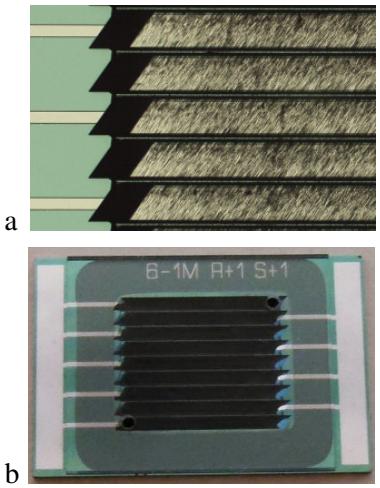

Figure 3. a: Electrode containment (w_{cav} 600 µm, w_{sep} 100 µm; d_1 300 µm, d_2 80 µm) **b:** after encapsulation (chip size 10x15 mm²).

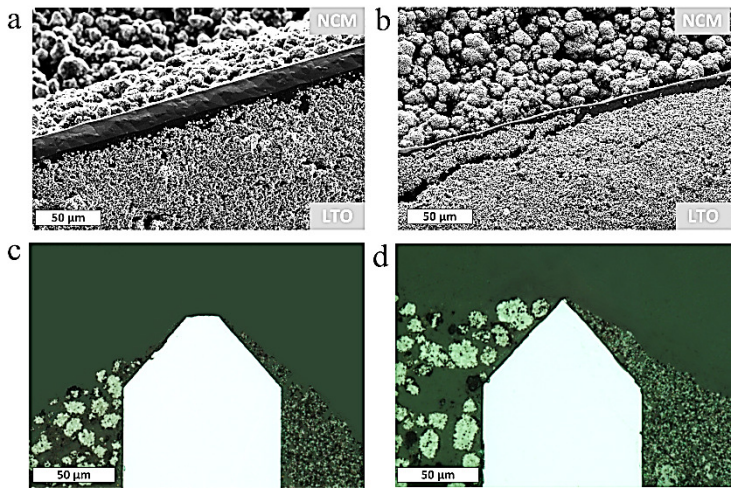

Figure 4. Separator region of cells with applied electrodes and w_{sep} = 100 µm (top: SEM picture, bottom: cross section polish). **a,c:** separator with flattened tip ($w_{plateau}$=20 µm). **b,d:** sharp separator tip.

3.3. Deduction of design rules for shaping the separator tip

As discussed above, it is crucial to precisely control the shape of the separator. The unmasked exposure of convex edges to KOH etching solution is known to result in a rounding of these edges. We simulated and observed this effect in our previous study [4]. The sloped edges at the separator tip form an angle α of around 40° with the vertical {111} side walls of the cavities. Depending on the etch time, there is a critical minimum separator width below which these sloped edges will run into each other and separator tips with acute angles be formed. This process results in a growth of the clearance d_2 above the separator tip.

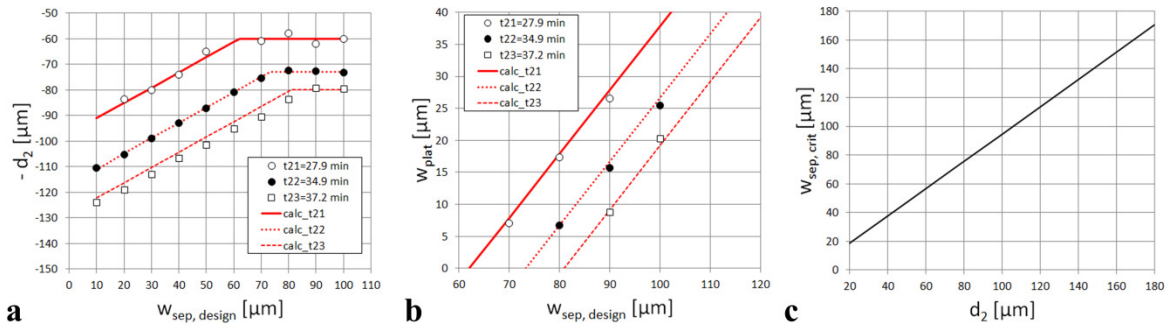

Figure 5. Etching characteristics at the separator tip. **a:** dimension of clearance d_2 as function of separator width w_{sep} and duration t_2 of the second KOH etch step **b:** width of the plateau at the separator tip (w_{plat}) as function of w_{sep} (markers: measurement, lines: calculation using equation 1 and an etch rate of 0.77 µm/min at the separator edges). **c:** critical dimension of w_{sep} as function of d_2.

We measured d_2 in dependence on w_{sep} and the duration of the second KOH etch step by using a profilometer. For wider separators, a plateau parallel to the wafer surface is still visible on the topside of the separator. In this case, the dimension of d_2 is consistent with the expected etch rate of <110>-Si. For smaller w_{sep}, however, d_2 was found to nearly linearly increase with a decrease in w_{sep} (figure 5a).

The orientation of the tapered edges at the separator tips does not correspond to a specific high-index crystal plane. However, a macroscopic etch rate for an etch attack perpendicular to the disintegrated slopes at the separator edges could be determined using geometrical data of separators with a distinct plateau, as given in figure 5b. We found this rate to account for some 0.77 µm/min for our etching conditions (80°C, 33% KOH). Using this rate and the observed angle α the slanted edges of the separator form with the {111} planes of the cavity side walls, a theoretically expected clearance d_2 can be calculated according to equation (1).

$$d_2 = \tan(90-\alpha)\ \frac{w_{sep}}{2} - \frac{d_{etch\perp slope}}{\sin(90-\alpha)} \quad (1)$$

The output of equation 1 is in very good agreement with the measured data for the first two immersion times (t_{21}, t_{22}) during etch step 2. For the longest time, t_{23}, however, we measured slightly higher values of d_2 than expected by calculation (figure 5). This difference can be explained by an increased etch rate at the acute angles of the separator tips, giving rise to a rounding of the newly formed convex edges. As an important output, the critical separator width, $w_{sep,crit}$, from which on acute angles are formed can be calculated in dependence on the desired clearance d_2 above the separator tip (equation 2, figure 5c).

$$w_{sep,crit} = 2\, r_{etch,slope}\, t_2 (\sin(90-\alpha))^{-1} \quad (2)$$

4. Testing and Evaluation

We tested the fabricated batteries using a multichannel battery test system (CTS-LAB, Basytech GmbH). To investigate the rate capability the fabricated cells were cycled between 2.0 and 2.9 V with CC/CV-charge steps at a rate of 0.2C and increasing discharge rates ranging from 0.2 to 10 C. For each discharge rate six complete cycles were run through. The reference capacity for calculating the C-rates was determined during the first cycle after formation at a discharge rate of 0.2C. At this rate the value basically equaled the nominal capacity of the cathode material (~130 mAh/g) as measured with standard laboratory test cells in EC:DMC (1:1wt) / 1M $LiPF_6$ vs. Li(0).

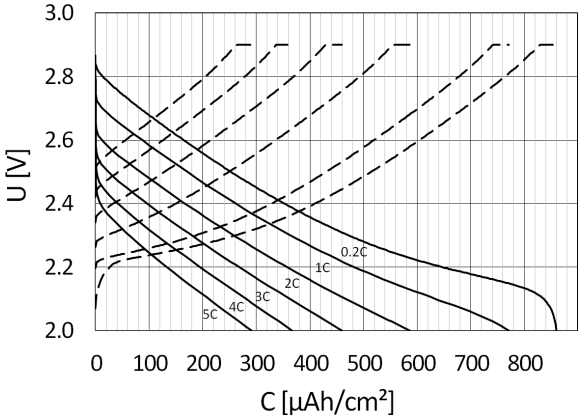

Figure 6. Cell voltage as function of extracted / inserted capacity per active area for micro battery with IDE during CC discharge at different loads and CC-CV charge at 0.2C (w_{cav}: 600 µm, w_{sep}: 100 µm, d_1: 300 µm, d_2: 100 µm, d_3: 180µm)

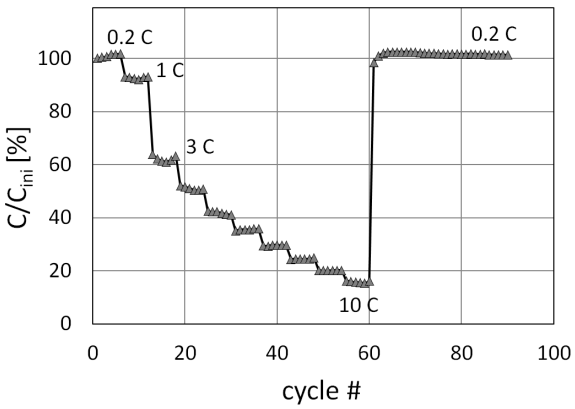

Figure 7. Capacity retention as function of cycle number and C-rate (rate capability test 0.2C to 10C followed by cycling performance test with 30 additional full cycles at 0.2C) (w_{cav}: 600 µm, w_{sep}: 100 µm, d_1: 300 µm, d_3: 170µm)

Figure 6 shows the discharge characteristics of a micro battery with 600 µm wide IDE digits at different CC loads until 5C. Cells of this geometry were capable of constant current loads of 10 C at some 15% capacity retention (figure 7). A comparison between micro batteries with single side-by-side electrodes and micro batteries with IDE of the same geometry (w_{cav}, w_{sep}, d_1, d_2,d_3) shows that by implementing an IDE design the rate capability can be improved significantly (figure 8). To evaluate the cycling stability each rate capability test was directly followed by 30 full cycles at a charge and discharge rate of 0.2C, respectively. The linear capacity loss rate over these 30 cycles accounted for < 0.1 % per cycle for all investigated IDE cells.

Yoshima et al. recently proposed a similar micro battery design with interdigitally arranged side-by-side electrodes (20 µm digits, 20 µm spacers) structured by micro injection of electrode slurries into dry film resist channels and subsequent lift-off of the resist [6]. The cells were capable a rate of 20 C at 60 % capacity retention. For the present micro batteries, some 60% of the discharge capacity at 0.2 C could be retained only at much lower rates of about 2 to 3C. However, the feasible specific capacity of the present cells (up to 850 µAh/cm², figure 6) is much higher than for the cells in [6]. That means, in terms of current and capacity per area, the present battery even outperforms [6] for moderate current loads, whereas for higher current loads a design as proposed in [6] is favorable (figure 9).

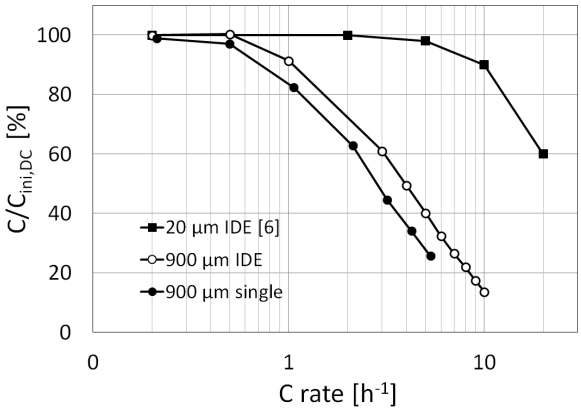

Figure 8. Capacity retention vs. discharge rate

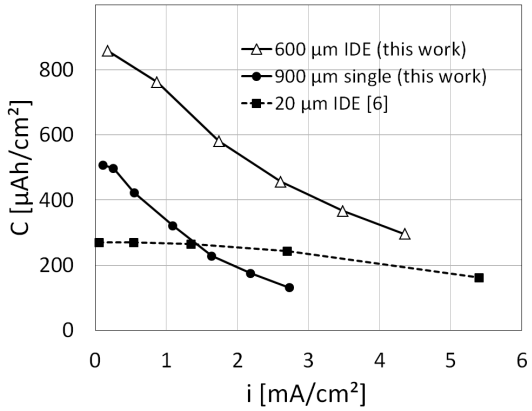

Figure 9. Capacity density vs. current density

5. Conclusion

The present micro battery concept combines state-of-the-art lithium ion battery materials and Si-processing. We hereby seek to overcome the limitations of thin film and 3D micro batteries considering specific capacity per area and cost. For packaging reasons it is of high advantage to have a co-planar arrangement of both electrodes. The fabricated micro batteries with IDE are capable of higher current loads than cells with single side-by-side electrodes [4]. The feasible specific capacity of the present cells is in the range of 600 to 900 µAh/cm² (0.2C) and hence considerably higher than for thin film batteries. The choice of the dimension of the separator width is crucial not only for realizing a high specific capacity per area but also for the reliable separation of the electrode slurries. The critical separator width, $w_{sep,crit}$, from which on acute angles are formed and the necessary etch time to generate a certain clearance d_2 can be calculated based on equation 1 and 2, respectively. A linear capacity loss rate of <0.1 % per cycle was observed over 30 full cycles at 0.2C CC-CV charge and CC discharge, respectively.

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