Analysis of Improvement for Turn on/off Performance of the MOSFET Gate Drive Waveform

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Abstract

This thesis shows that the gate waveform of a power MOSFET driven by a specialized driver chip used in industry is imperfect and induces increased power loss in the MOSFET and lowers overall efficiency. The accurate measurements and analysis of the RLC parameters for the transmission line connecting the driver to the MOSFET are presented and a mathematical model for the line is developed based on ABCD parameters. The transmission line is characterized by experimentally measuring the frequency response of the line and extracting the parameters of the line using the mathematical model. Spice simulations and experimental results confirm the results of the extraction process. The simplified Spice model of the power MOSFET driver is developed in conjunction with the transmission line model and simulated with power source circuitry to match the experimental results. Length of the transmission line is changed in Spice simulation to confirm the dependency of length of the line with the performance of the driver. Finally, the slew rate of the gate waveform is shown to improve by inserting a capacitor to split up the transmission line in half. The result is confirmed experimentally.

Acknowledgements

I would like to express my gratitude to my supervisor Dr. K. Natarajan for his helpful support and guidance, to my parents who support me, and to my friend T. Tang who always stood by me. Dr. K. Natarajan gave me kind encouragement and useful instructions all through my writing. Thank you very much.

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1 Introduction

1.1 Introduction to the MOSFET driver performance

As the feature size of electronic circuits continue to shrink and the operational frequency applied to drive the circuits continue to increase in today's power electronic industry, many designers have become aware of the problems with driving a precisely shaped pulse to the gate of the MOSFET. For instance, in Figure1.1, when we use a frequency of 1.2 MHz square wave input to drive the MOSFET circuit, we see overshoots, undershoots, and ringing at the waveform on the gate of the MOSFET, These imperfections that occur during signal transitions from low to high and high to low are shown in Figure 1.2.

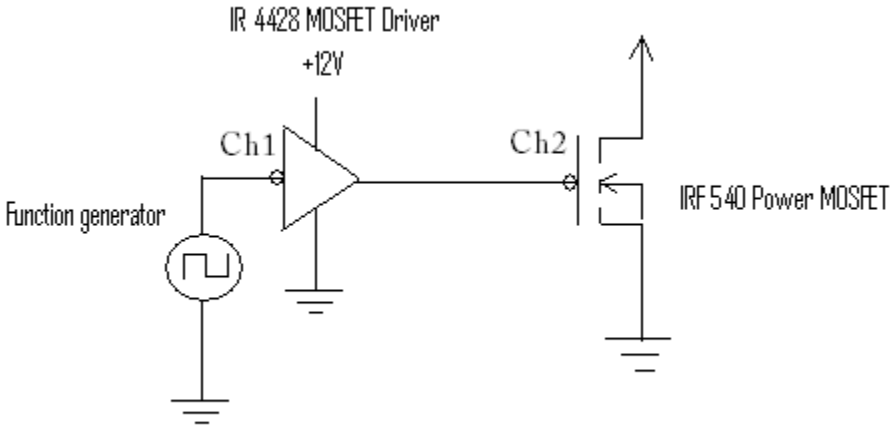
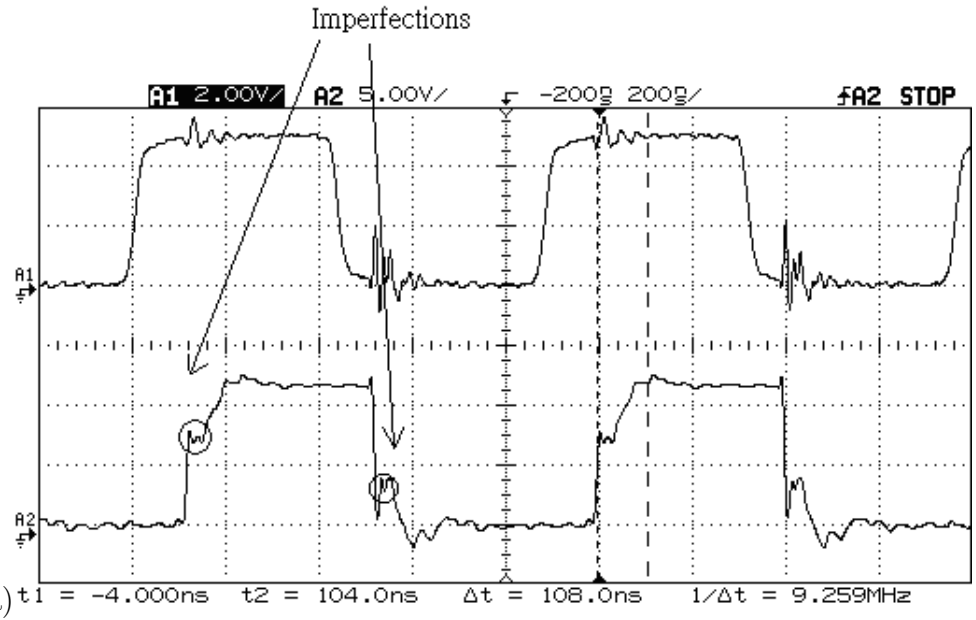


Figure 1.1: A square wave used to drive the MOSFET circuit.

Since we know that higher slew rate means better performance by turning MOSFET on quickly, we will calculate the slew rate of the MOSFET at the gate of the MOSFET:



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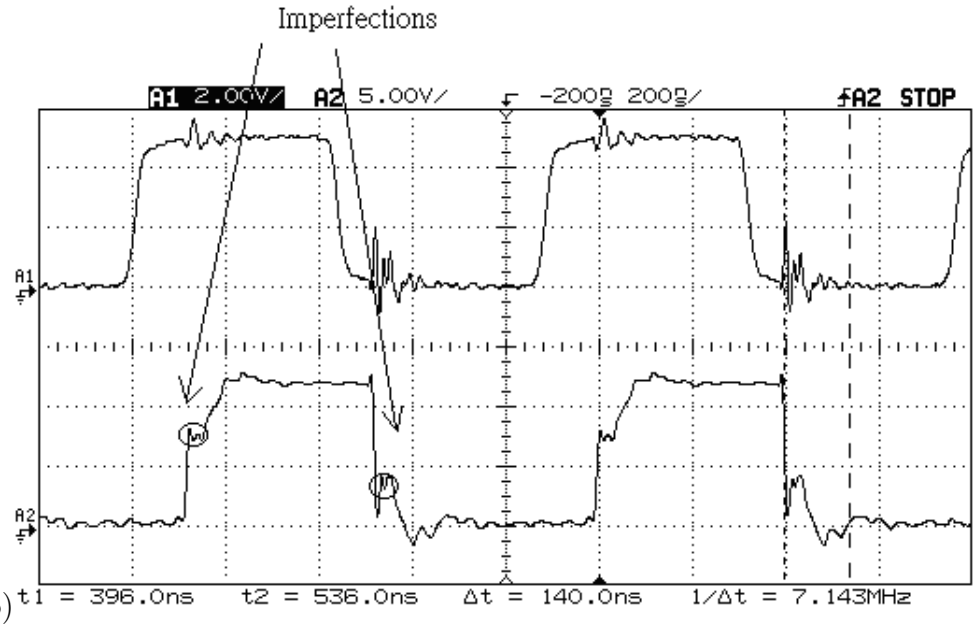


(b)

Figure 1.2: (a) Rise time ,and (b) fall time at the gate of the MOSFET with a 1.2 MHz square wave input. Channel A1 is the output from function generator and Channel A2 is the output at the gate of the MOSFET.

The rise time is 108 ns to reach 10 volts at which level the MOSFET is fully on, so the slew rate is equal to 92.6 V/µs ; the fall time is 140 ns, so the slew rate is equal to 71.4 V/µs. Furthermore, the propagation delay at the gate waveform as seen on the Channel 2 in Figure 1.3 is 124 ns (turn-on) and 88 ns (turn-off). The propagation delay will be used for comparison in later improvements.

It is known from specification sheets that power MOSFET can be turned on in 45 ns and turned off in 25 ns; therefore, if a slew rate could be improved here, the MOSFET can be turned on and off at this speed. Further the dynamic power consumption, caused by MOSFET turn-on, turn-off, contributes to the total power efficiency of the power electronic circuit[1]. From Figure 1.2 and 1.3, it is observed that the imperfections in signal transition at the gate of the MOSFET will increase the rise/fall time of the waveform and, as a result, increase the dynamic power consumption of the circuit and lower the power conversion efficiency.

1.2 A simple solution to improve the performance of the driver

There is a simple solution to improve the performance of the driver as shown in Figure 1.4. We can add a series resistor between the output of the driver chip and the MOSFET. This limits the instantaneous current to slow down the turn on/off time of the MOSFET and reduces the ringing, voltage spikes, and imperfections. The waveform becomes smoother in signal transition at the gate of the MOSFET and appears to improve the performance of the driver; however, it will increase the power loss of the circuit by slowing down MOSFET

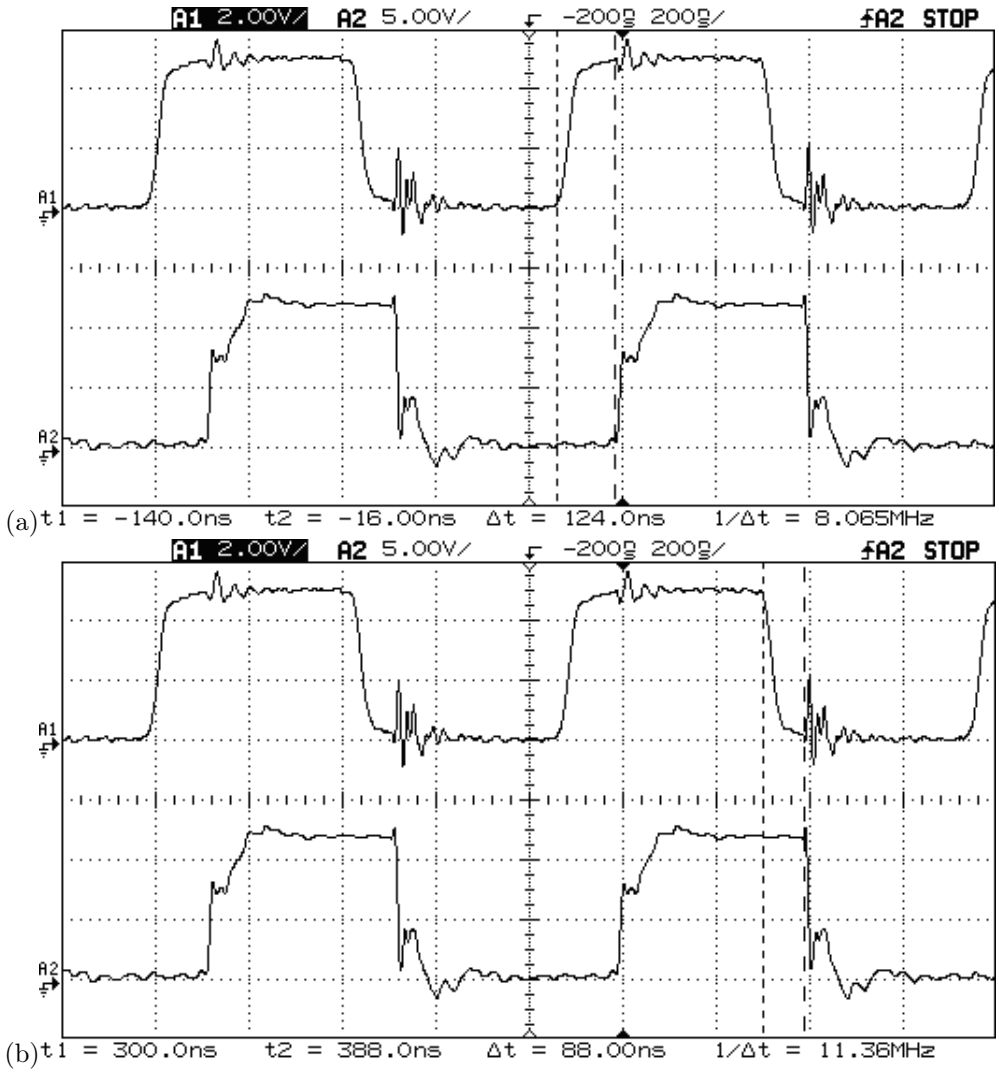


Figure 1.3: (a) Turn on, and (b) turn off delay time measured during signal transition at the gate of the MOSFET with a 1.2 MHz square wave input. Channel A1 is the output at function generator and Channel A2 is the output from the gate of the MOSFET.

turn on/off time as the rise/fall time is considerably increased and this is a major concern for today's power electronic circuits. Therefore, adding a gate resistor is not an ideal solution to resolve the issue of imperfections in gate waveform.

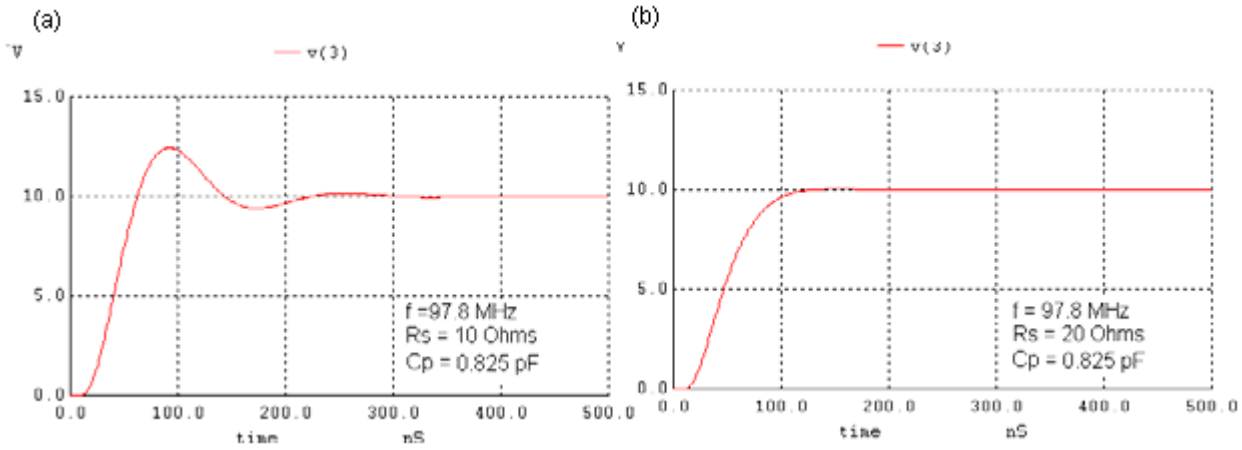


Figure 1.4: Spice simulation results (a) before adding a series resistor between the MOSFET driver and the MOSFET, and (b) after adding a series resistor between the MOSFET driver and the MOSFET.

1.3 The possible causes of the poor driver performance

Imperfections in the driver output waveform at the gate of the MOSFET slows down the signal transition and results in slower signal transition at the gate output. The effect will become more severe when we use a higher frequency input to the power MOSFET driver. According to the literature review from Section 2.1 distributed, line inductance effects could play an important role in the poor performance and the transmission line effects between the driver and the MOSFET could possibly cause the imperfections at the gate of the MOSFET. Authors in [2] shows that ringing, overshoots, and undershoots

could be caused by transmission line effects of interconnect. There are coupling effects, capacitive and inductive between the traces of circuits[3]. The power MOSFET can carry large currents in the drain source and magnetic coupling effects can also occur from these currents into the gate drive circuit. To sum up, modeling these effects on the driver gate circuit will provide better understanding of the power MOSFET drive waveforms and help reduce the imperfections.

1.4 Thesis Outline

This thesis is organized as follows. The background information, literature review on measuring the performance of the power MOSFET driver and modeling interconnect is introduced in Chapter 2. The measurement results of the power MOSFET driver are presented and discussed in Chapter 3. In Chapter 4, an analysis of the distributed RLC transmission line connecting the driver to the MOSFET is presented and a mathematical model for the line is developed, The frequency response of the line after extracting RLC parameters is computed and shown to match experimental results of the circuit. Spice simulation results of the RLC transmission line confirms the match with the experimental results provided later in this chapter. Spice simulation of the power MOSFET driver with the power source circuitry is completed and the model is used to improve the performance of the MOSFET driver in Chapter 5. Three different methods to improve performance are proposed and Spice simulations are performed to evaluate improvements in the gate waveform and slew rate. The thesis concludes with a practical solution to improve the

gate waveform performance and provides a good power MOSFET driver model for future driver optimization.

2 Background

2.1 Review of literature

A review of literature on MOSFET gate waveform and driver performance did not provide any literature expect the application notes from manufacturers of the driver chips. However, in today's semiconductor technologies, the VLSI circuits continue to operate in several giga-hertz clock frequencies and with the scaling of technology, the cross-sectional area of wires has been scaled down and interconnect lengths have increased. Besides, line resistances have been further reduced because of the shrinking size of the circuits in industry. Inductive effects have therefore become significantly important in modeling interconnect transmission lines due to higher signal frequencies and longer wire lengths[4]. Traditional lumped and distributed RC models of interconnects are no longer accurate as they predict delay and crosstalk with substantial errors[2, 5]. Therefore, an accurate resistance-inductance-capacitance (RLC) interconnect model is critical in the design of high-performance integrated circuits and much recent effort has been dedicated towards this. This literature was reviewed for understanding the modeling of printed circuit board trace inductances.

Line inductance can affect the circuit performance in two distinct ways[6]. Firstly, it can slow down the rise and fall time (slew rate) and cause signal delay throughout interconnects. This will deteriorate the performance of the circuit and lower the overall efficiency. Secondly, since VLSI interconnects can be viewed as CMOS gates driving lossy transmission lines, line inductance may give rise to reflections when input impedance of the load is not necessarily matched with the output impedance of the circuit and result in

overshoots and undershoots in voltage waveforms. These issues are similar to the observed phenomenon in Chapter 1 when driving power MOSFET gates. Voltage overshoots may cause glitches to increase the power dissipation, or in the worst case, the MOSFET can be damaged, thus leading to failure. Voltage undershoots may cause the false transitions and increase the dynamic power dissipation.

Wire inductances are sensitive to even distant variations in the interconnect topology[7]. Being able to optimize the insertion length of interconnect will help minimize the overall time delay for a long interconnect line[8] and the ideas from this literature therefore can help provide ideas for improving MOSFET gate driver performance. The interconnect transmission line can have a tremendous effect on the performance of MOSFET driver. The dependency of length of the transmission line interconnect becomes important and worth studying further.

2.2 A CMOS gate driving an uniformly distributed RLC transmission line

A CMOS gate driving a distributed RLC transmission line representation of an interconnect line is shown in Figure 2.1. The total length of the interconnect is H. The driven transmission line consists of resistance, inductance, and capacitance per unit length of r, l, and c, respectively, with a small unit length Δx. The RLC parameters are, therefore, given by $R_t = rH$, $L_t = lH$, and $C_t = cH$, where R_t, L_t, and C_t are the total resistances, total inductances, and total capacitances. The interconnect is driven by a MOSFET driver

with a voltage source V_{in}, consisting of the output impedance(resistor) R_s and the output parasitic capacitance C_P, and it is terminated by a power MOSFET with the equivalent input capacitance C_L. V_{out} is the output voltage at the end of the interconnect section.

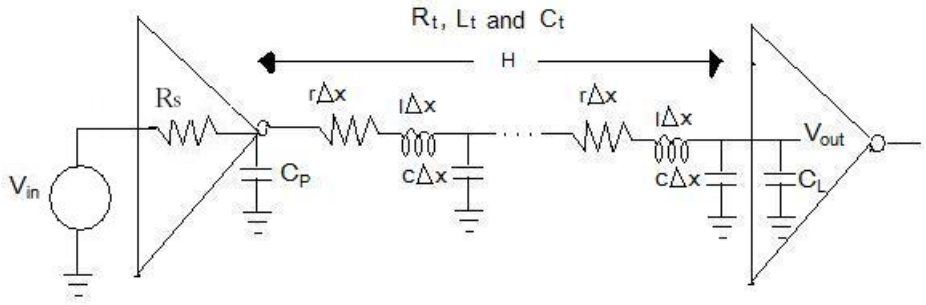


Figure 2.1: The equivalent circuit of a source driving a distributed RLC transmission line with load adapted from[9].

2.3 Typical gate driving configurations for MOSFET driver

To improve the MOSFET overall efficiencies, and size of power electronic equipment, higher frequencies are used to drive the power MOSFET in power electronic circuits. As seen in Chapter 1 within, high peak currents going through the power MOSFET driver and the fast rise/fall time of the gate drive voltage can result in failure to drive an accurate input. As the circuit becomes more complicated, there are also a large number of longer copper traces so that the transmission line effects become significant to the driver. As a result,

many power MOSFET drivers need to run with additional clamp circuitry to improve the overshoots/undershoots in the driver performance.

There are many circuit configurations that MOSFET drivers can be used in[10]. The most ideal MOSFET driver circuit is shown in Figure 2.2. Good rise/fall time of the MOSFET gate voltage can be achieved by adding appropriate bias voltage bypass capacitors (C_p) as shown in Figure 2.2. Moreover, this capacitor can be used to limit the instantaneous current flowing through the driver and prevent damage to driver. It is also important that the grounding of the MOSFET driver and the MOSFET source be the same. Adding a series gate driving resistor R_s, as shown in Figure 2.2 which unfortunately often leads to slower performance. Most of the time the rapid turn-on and turn-off of the MOSFET gate voltage can lead to increased EMI noise. Adding a series gate driving resistor can limit the peak gate driving current in order to slow down the rise of the gate voltage and is justified to reduce EMI; however, with other shielding techniques this justification is no longer valid.

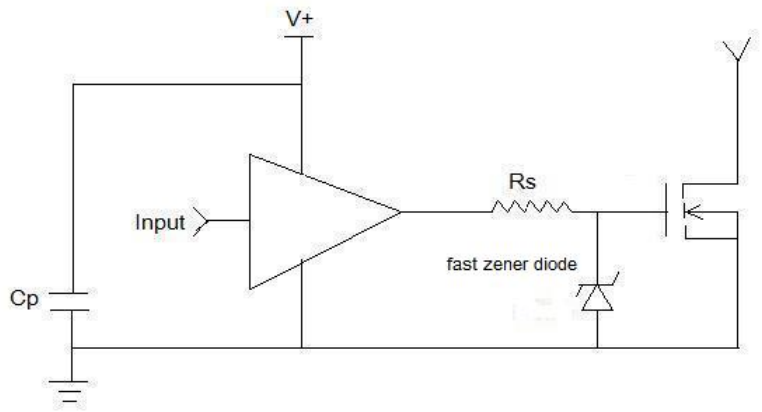


Figure 2.2: Typical MOSFET driver configuration.

Ideally, the MOSFET should be placed as close as possible to the driver. There are inductance effects between the output of the driver and the gate of the MOSFET (transmission line effects). This can result in the gate voltage of the MOSFET ringing above the Vdd and below the ground. If the peak voltage exceeds the maximum rated gate voltage of the MOSFET, the MOSFET can be damaged and lead to failure. The gate voltage can be clamped down by adding a fast zener diode from the gate to the source of the MOSFET as shown in Figure 5. However, there has always been a trade-off between the limiting of the performance of the MOSFET driver, and additional power dissipation resulting from the additional circuitry and the placement of the MOSFET in the circuit.

2.4 Frequency spectrum for square wave

Since experimental measurements are processed digitally. a few facts of frequency spectra are collected in this section.

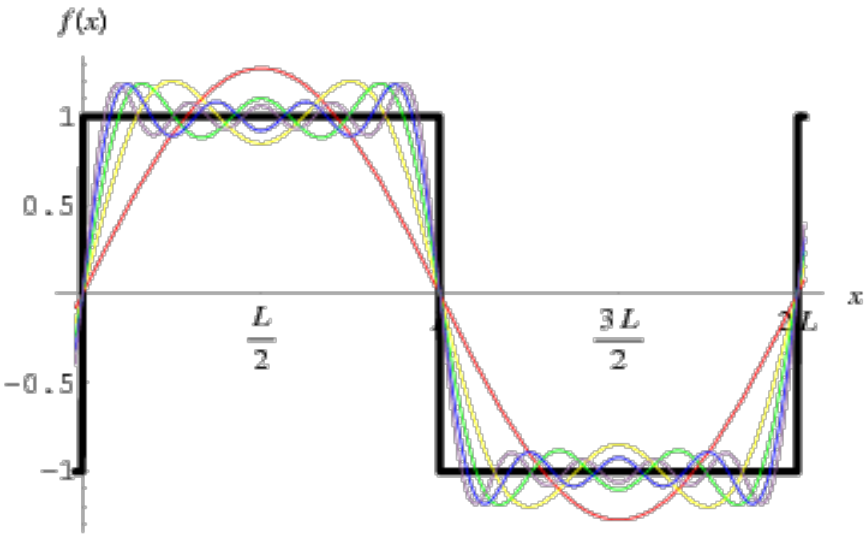


Figure 2.3: a square wave of period 2L

According to Fourier series, a square wave representation can be constructed by adding many sine waves with frequencies equal to multiples of the "fundamental" frequency of the square wave. this square wave can be obtained by summing up an infinite number of odd harmonics

$$f(x) = \frac{4}{\pi} \sum_{n=1,3,5\ldots}^{\infty} \frac{1}{n} \sin\left(\frac{n\pi x}{L}\right) \tag{2.1}$$

where, period is 2L.

The amplitude of the N^{th} harmonic is $\frac{1}{N}$ of the amplitude of the fundamental compo-

nent. If we decompose a square wave into its sinusoidal components using the FFT (Fast Fourier Transform), we should get a spectrum of sampled signal consisting of the fundamental and the odd harmonics of the square wave frequency[11]. The spectrum should have the amplitudes in the ratios 1, $\frac{1}{3}$, $\frac{1}{5}$, $\frac{1}{7}$, $\frac{1}{9}$, ... respectively and contain components at odd harmonics of the fundamental frequency(1, 3, 5, 7...). To abide by Nyquist sampling theorem, the sampling frequency should be at least twice larger than the folding frequency to satisfy the equation $f_N \leq \frac{f_s}{2}$, where f_N is the highest frequency that is to be accepted in the original signal. In other words, if we don't use sampling rate high enough to sample the signal, the aliasing effect that causes high frequency different signals to become indistinguishable from low frequency will occur in the frequency spectrum.

2.5 Network Analyzer with scattering parameters

While dealing with circuits operating at low frequencies, one is able to measure voltages and currents involving the magnitudes and phases of a wave traveling in a given direction since most circuits can be treated as an interconnection of lumped-equivalent components with unique voltages and currents defined at any point in the circuit[12]. In contrast, at higher or microwave frequencies the direct measurement of voltages and currents becomes difficult or incorrect due to the distributed nature of the circuits. The network analyzer is used to measure the scattering parameters of an N-port network in such a case and this is reviewed in this section.

The scattering parameters measured from the network analyzer can provide a complete

description of the network with magnitudes and phases in a matrix form. The scattering matrix describing the two-port network needed in the thesis is:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \tag{2.2}$$

where a_1, a_2 are incident waves, b_1, b_2 are reflected waves, and

S_{11} = Input reflection from port 1.

S_{12} = Reverse transmission gain with energy from port 2 towards port1.

S_{21} = Forward transmission gain with energy from port1 towards port2.

S_{22} = Output reflection from port 2.

In this thesis, S_{11}, S_{12}, S_{21}, and S_{22} values in magnitudes and phase are measured and converted into ABCD parameters using Matlab. Then the ABCD parameters are used to model the transfer function of the circuit and decide "optimizing values" of per unit length - resistance, inductance, and capacitance for the transmission line between the driver and the MOSFET.

Since ABCD parameters are used in the thesis, basic definition of these parameter is provided below:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \tag{2.3}$$

where V_1, V_2 are input and output voltages, I_1, I_2 are input and output currents, respec-

tively and

$A = \frac{V_1}{V_2}$, when $I_2 = 0$.

$B = \frac{V_1}{I_2}$, when $V_2 = 0$.

$C = \frac{I_1}{V_2}$, when $I_2 = 0$.

$D = \frac{I_1}{I_2}$, when $V_2 = 0$.

3 MOSFET Driver Circuit Board Design and Performance

3.1 MOSFET driver configuration

A MOSFET driver circuit is designed on a PCB (printed circuit board) to initially test the MOSFET driver. The complete design of the MOSFET driver board primarily consists of a MOSFET driver chip (dual low side driver IR4428), 6 cm long copper trace (transmission line), and a NMOS transistor (power MOSFET IRF540). The circuit configuration is presented in Figure 3.1.

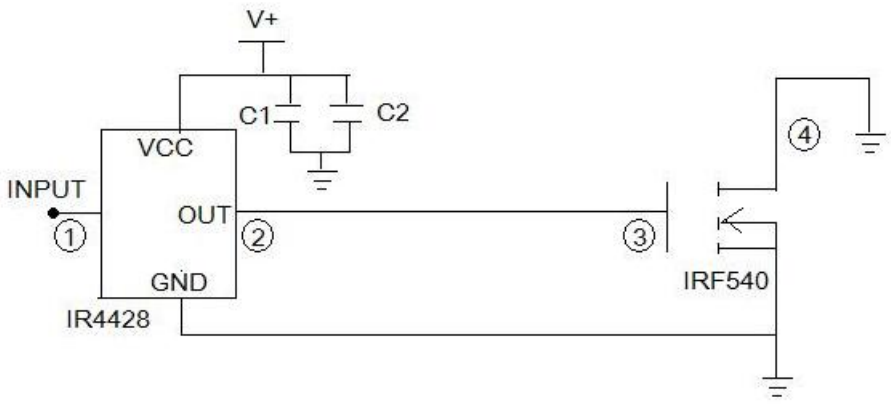


Figure 3.1: MOSFET driver circuit board configuration.

A tantalum capacitor C_2 and a regular bypass capacitor C_1 are placed between the power supply of the MOSFET driver and the ground. These capacitors are used to absorb spikes on the driver because of the sudden interruption of flow of current from the driver which leads to a sharp rise/fall in voltage and may cause damage or slow performance of

the driver; therefore, the addition of these bypass capacitors can stabilize the power supply of the circuit. The tantalum capacitor here is particularly used to handle high frequency components to improve the MOSFET driver performance.

A clean square wave signal with 5 V peak to peak and 2.5 V offset from the function generator and a 10 V power supply is connected to the MOSFET driver. The driver chip and the source of NMOS transistor are grounded on the same node to get rid of ground noise. The square wave input frequency is varied and the square waveforms are observed on oscilloscope. We can verify that the outputs of the function generator are consistent with the outputs of the MOSFET driver board. We will optimize the square waveforms by carefully designing the additional circuitry in the driver board.

3.2 Behaviour of the MOSFET driver at different frequencies

The first goal is to observe the behaviour of the MOSFET driver. At the beginning, the square waves at different frequencies are used to drive the NMOS transistor (IRF540). Figures 3.2 and 3.3 show the behaviour of the driver performance between using a 780 kHz square wave and a 1560 kHz square wave.

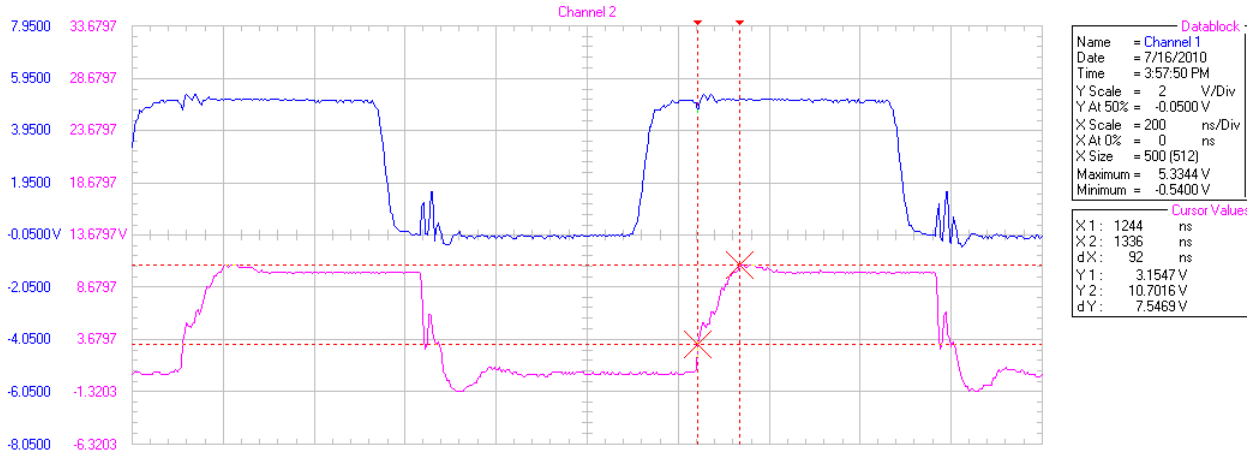


Figure 3.2: The result from Fluke PM3370B oscilloscope when using a 780 kHz square wave input

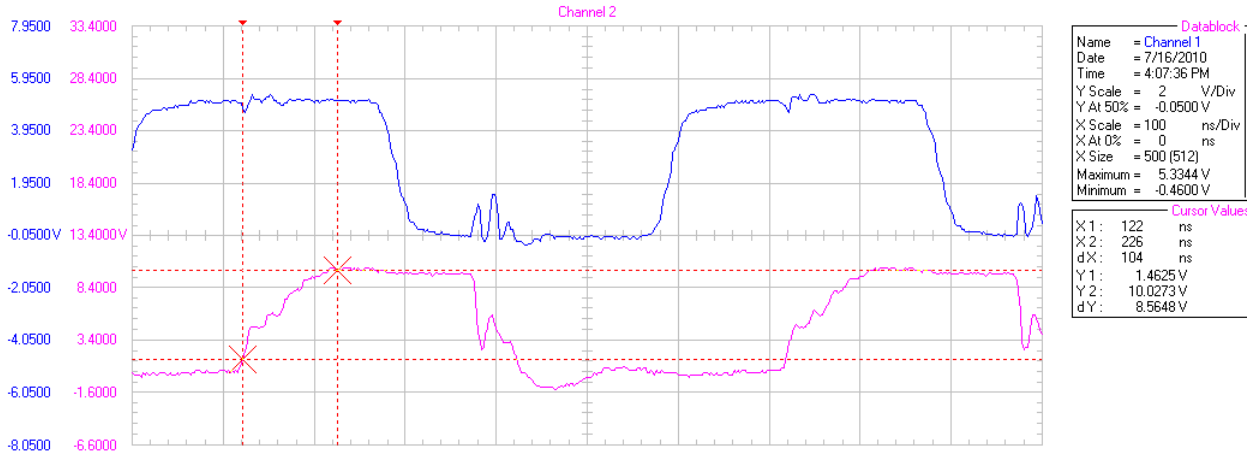


Figure 3.3: The result from Fluke PM3370B oscilloscope when using a 1560 kHz square wave input

Channel 1 represents the results taken from the oscilloscope at the output of the function generator (labeled No. 1 in Figure 3.1), and Channel 2 represents the results at the output of the gate of the MOSFET (labeled node 3 in Figure 3.1). The two 15 pf passive probes we have used to measure the performance of the MOSFET driver are connected to the Fluke PM3370B oscilloscope. As we compare the results in Figure 3.2 and 3.3, they show

slower rise and fall time which occur during the signal transitions in the waveform when we use a frequency at 1560 kHz square wave to drive the MOSFET than from a 780 kHz square wave. The square waveforms at both frequencies start to form humps at the rising and falling edges and the humps become more easier to see when we use higher frequency square wave. More importantly, the imperfections which exist in the signal transition are the main reasons slowing down the slew rate of the waveform. At higher frequency, we are seeing more severe delays occur during the signal transitions and the waveforms disfigure due to the slow slew rate. As a result, the rise and fall time measured at the output of the MOSFET driver have further increased. The power dissipation has increased in the power electronic circuit and the slow signal transition may cause an unreliable performance of the MOSFET driver, in the worse case, driving an inaccurate input waveform. To improve the imperfections of the waveform and to drive the MOSFET more efficiently, we need to measure the frequency response of the MOSFET driver and furthermore understand the behaviour of the transmission line effects between the driver and the MOSFET.

3.3 The spectra of the frequency response of the MOSFET driver

To study the performance of the MOSFET driver including the behaviour of transmission line effects, we will study the frequency spectra of the MOSFET driver using FFT analysis. We use the function generator to drive the MOSFET with a clean square wave and then collect the raw data using a Fluke PM3370B oscilloscope. Probe 1 is connected to the output of the function generator and probe 2 is connected to the gate of the NMOS

transistor. After collecting the raw data from the oscilloscope, we use Matlab to compute the FFT on the data.

The raw data from the oscilloscope were sampled $N = 512$ times with a time interval of t_s= 5 ns; therefore, the total sampling duration is

$$T_s = Nt_s = 512 \cdot \left(5 \times 10^{-9}\right) = 2.56\,\mu\text{s} \tag{3.1}$$

and the spectral resolution is

$$f_s = \frac{1}{T_s} = \frac{1}{Nt_s} = \frac{1}{512 \cdot (5 \times 10^{-9})} \approxeq 390\,\text{kHz} \tag{3.2}$$

We know by Fourier series Section 2.4, the frequency spectrum of the square waveform should only contain the fundamental frequency and the odd harmonics, and the magnitudes should come in the ratios 1, $\frac{1}{3}$, $\frac{1}{5}$, $\frac{1}{7}$, $\frac{1}{9}$, ... respectively. To perform the analysis of the frequency spectrum, we have taken away the DC component from the frequency response by removing the mean from the waveforms. Therefore, we are supposed to see the first data point of the graph at zero Hz has 0 magnitude with position $n = 1$ (since Matlab automatically starts with the position 1 in its index). The second data point represents the spectrum of the frequency response at 390 kHz since we know the frequency spectral resolution is equal to 390 kHz from Equation 3.2, and the third data point represents 780 kHz which is the fundamental spectrum of the frequency response at $n = 3$. If we

The order of the odd harmonics take place in the spectrum	$780\,kHz$ (weight =2)	$1560\,kHz$ (weight =4)	$2340\,kHz$ (weight =6)
1^{st}	$(2 \times 1)+1 = 3$	5	7
3^{rd}	$(2 \times 3)+1 = 7$	13	19
5^{th}	$(2 \times 5) + 1 = 11$	21	31
7^{th}	$(2 \times 7) + 1 = 15$	29	43
9^{th}	$(2 \times 9) + 1 = 19$	37	55

Table 3.1: Table shows how the frequency spectrum at odd harmonics of a square wave input should appear in Matlab FFT plots.

continue to count the position of the data points occurs in the manner, then the next odd harmonic will occur on the position $n = 7$ in the graph which stands for 2340 kHz frequency spectrum. Table 3.1 gives us a summary of the positions that the order of the odd harmonics would occur in the spectrum of frequency response. On the other hand, the magnitude of the spectrum at $n = 3$ (the fundamental) would be 3 times larger than the magnitude of the spectrum at $n = 7$ (the third harmonic) and 5 times larger than the magnitude of the spectrum at $n = 11$(the fifth harmonic).

The initial test is conducted by using a 780 kHz square wave input to drive the MOSFET. Figure 3.4 shows, after we compute the FFT, the frequency spectrum results as measured at the input from the function generator and the output from the gate of the power MOSFET. We are able to see the expected responses from the input frequency spectrum; however, when we look at the output frequency spectrum from the gate of the transistor, we see significant energy spectra are also at even harmonics which occur on the $5^{th}((2 \times 2)+1 = 5)$, 9^{th}, and 13^{th} place in the plot of the frequency spectrum. This contradicts the expectation

that we are supposed to see the energy spectra only at odd harmonics. Thus the driver and load effectively distort the signal from the ideal expectation.

With the square wave input at 1560 kHz, the results are seen in Figure 3.5. We are again able to see clear results of the frequency spectrum. The results tell us that the energy spectra are at odd harmonics from the input, but apparently exist both at odd and even harmonics at the output.

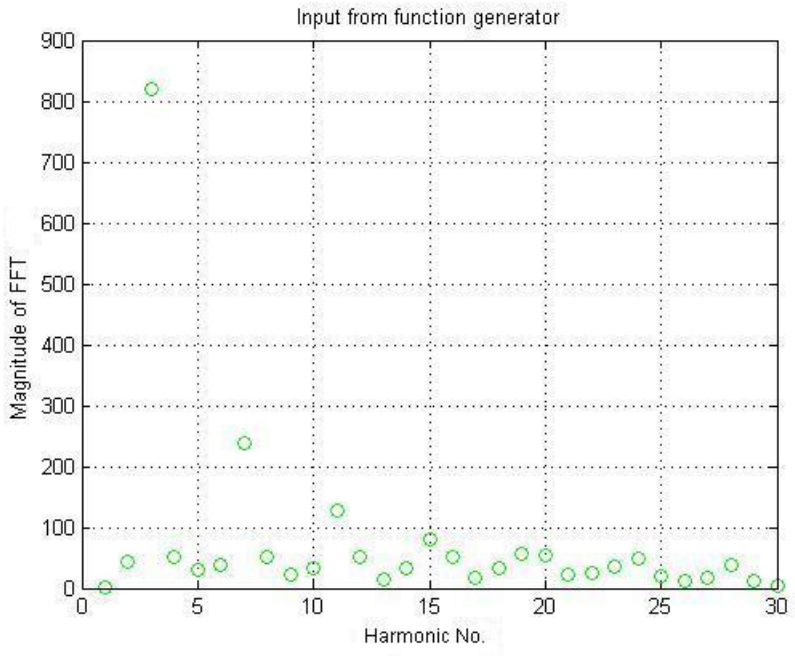
Given the experimental results, we would argue that the energy in the even spectra in the output at the gate of the transistor could be caused by the combined effects from components on the MOSFET driver as well as the transmission line load of the PCB trace or the power MOSFET. We try to find the cause of the even frequency spectra in the next section.

3.4 Determining the cause of even harmonics in the square wave spectra

Different approaches are taken to determine what causes the frequency spectra at even harmonics to exist in the output at the gate of the MOSFET.

3.4.1 Measure with higher spectral resolution oscilloscope

By Nyquist sampling theorem, we realize that the frequency spectra at even harmonics could be the result of aliasing effects that cause the unwanted higher frequency signals to



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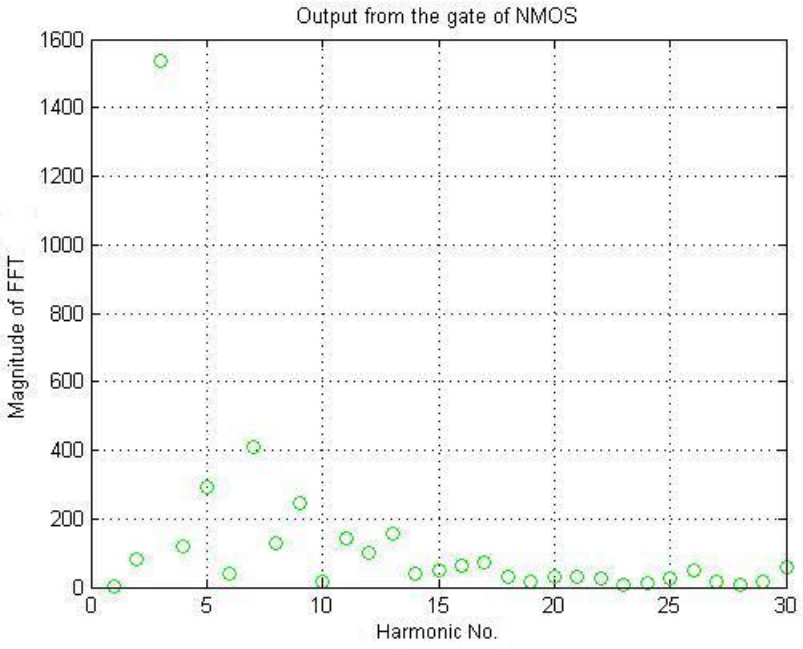
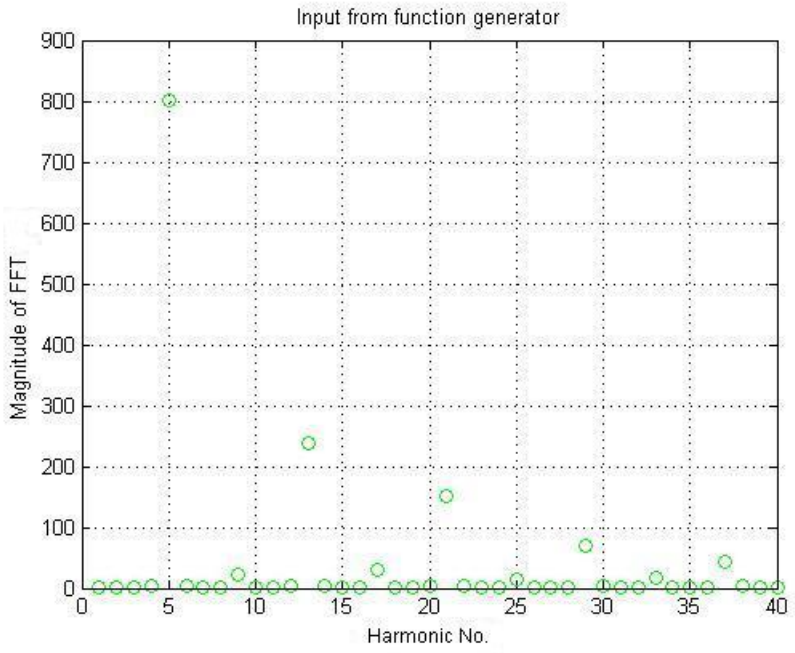
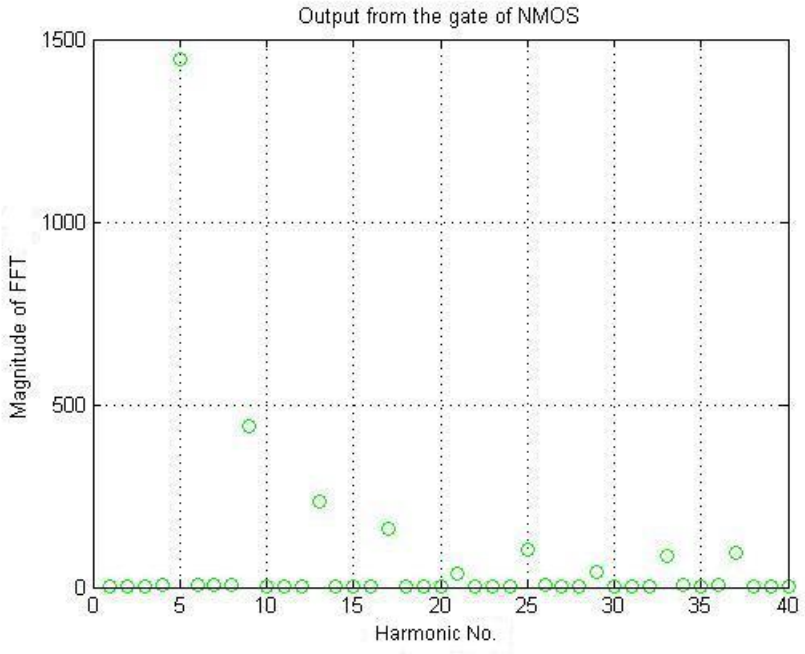


(b)

Figure 3.4: Frequency spectra (a)from the function generator with the square wave input at 780 kHz. (b)from the gate of the NMOS transistor. The raw data are sampled with the Fluke PM3370B.



(a)



(b)

Figure 3.5: Frequency spectra (a)from the function generator with the square wave input at 1560 kHz. (b)from the gate of the NMOS transistor. The raw data are sampled with the Fluke PM3370B.

fold back into the desired frequency band where they could appear as a desired signal. We might be able to avoid the aliasing effects by increasing the sampling frequency. The Fluke PM3370B oscilloscope was replaced with Agilent HP 54645D oscilloscope. The Agilent HP 54645D has higher spectral resolution as it can take up to 2000 samples instead of 512 samples from Fluke oscilloscope. With 2000 samples sampled at 2.5×10^{-9} seconds, the spectral resolution of the FFT becomes

$$\frac{1}{Nt_s} = \frac{1}{2000 \cdot (2.5 \times 10^{-9})} = 200\,\text{kHz} \tag{3.3}$$

This approach doubles the spectral resolution. Compared to the results from the Fluke PM3370B oscilloscope, it gives us 1000 harmonics in the frequency spectrum. With the Agilent oscilloscope, the same measurements with the square waves at the different frequencies was performed. The even harmonics persist at the output of the gate of the transistor and therefore the spectra are not caused by the oscilloscope aliasing effect.

3.4.2 Enclose the MOSFET driver in the metal box

Since the external signals coming from the lab environment could affect the driver's behaviour and possibly cause the unexpected energy spectra in the output, we use a metal box to shield the MOSFET driver circuit board. We have the I/O connectors firmly mounted on the metal box along with the MOSFET driver circuit board inside the box to avoid the interference from the noise. In this approach the surface of the metal box is grounded;

however, even harmonic spectra persist at the gate of the MOSFET.

3.4.3 Repeat the experiment by removing the driver chip

Both the MOSFET driver chip and the transmission line could have influences in the results at the output of the gate transistor. We repeat the experiment by removing the MOSFET driver chip to see if this changes the result. We use the function generator to generate a square wave input directly into the trace of the driver load fed by the output of the driver and terminate the line by an equivalent capacitor. We obtain different results after removing the driver chip from the MOSFET driver circuit. The even harmonics spectra are no longer present at the output the gate capacitive load. The capacitor load is replaced by the power MOSFET gate as load and similar conclusion is obtained: Thus, we conclude that the frequency spectra at even harmonics are primarily caused by the MOSFET driver chip.

3.5 Conclusion

A simple design of a MOSFET driver circuit board has been introduced at the beginning of the Chapter. A clean square wave input is used to drive a NMOS power MOSFET through this circuit board at different frequencies. The results of the performance are measured both using PM3370B and Agilent HP 54645D oscilloscopes. The behaviour of

the MOSFET driver circuit board has shown that the imperfections which occur during the signal transition of the waveform become more severe at higher frequency square wave inputs. The frequency spectra at even harmonics are found in the output of the MOSFET driver in the MOSFET driver circuit board when we compute the FFT of the waveform. Additional experiments were conducted to find out the primary reason which causes the existence of spectra at even harmonics. Based on these experiments, it is concluded that the driver chip introduces the even harmonics.

To model the performance of the MOSFET driver board, we remove the MOSFET driver chip from the circuit and study the behaviour of the interconnect from the driver chip output to the gate of the power MOSFET . We will then derive a mathematical model and extract the values of per unit length - resistance (r), inductance (l), and capacitance(c) for the line. Thereafter, Spice simulations will be used to verify the results and predict the behaviour of the MOSFET driver when the driver is inserted back into the board.

4 Modeling the Transmission Line of the MOSFET Driver Circuit Board

4.1 Performance of the transmission line excited by square wave

In Chapter 3, we tried to model the behaviour of the MOSFET driver when the driver chip is in the board and realized the driver chip causes unexpected energy spectrum at the output on the MOSFET power transistor gate.Therefore, we test the circuit without the driver chip and model the transmission line of the circuit to extract r, l, and c values of the line. We remove the MOSFET driver chip and replace the NMOS transistor on the PCB with a equivalent capacitor which has a capacitive load of 1000 pf corresponding to the IRF540 transistor datasheet. A square wave input is used to drive the interconnect at 1 MHz. The result is shown in Figure 4.1: Channel 1 is at the beginning of the interconnect to measure the input signal and Channel 2 is measured at the load end of the interconnect. We have seen that the smooth square waveforms contain small ringing and small humps form on the rising and falling edge of the waveforms.

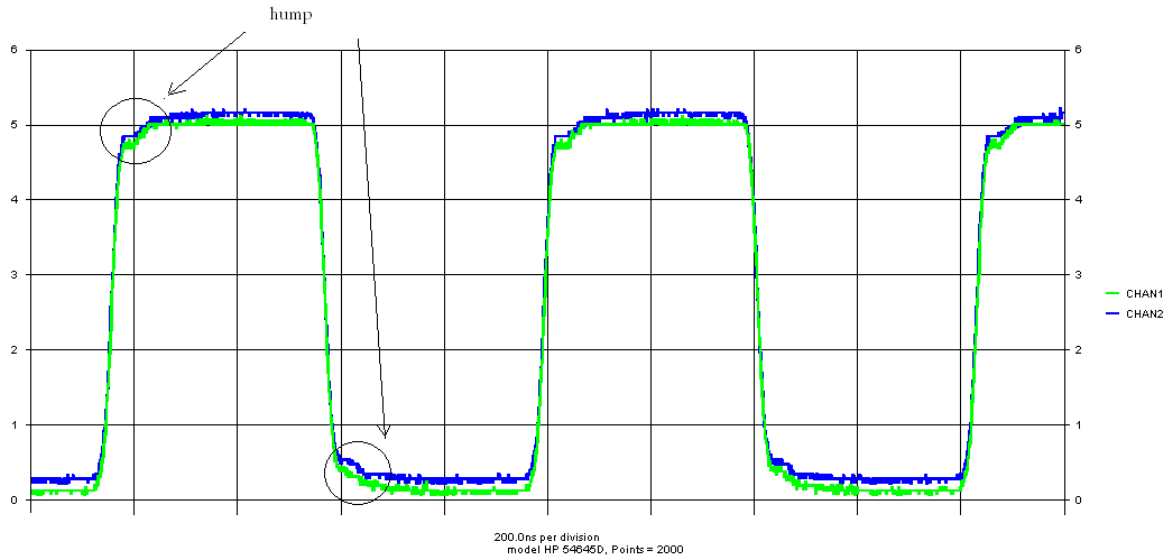


Figure 4.1: Experimental result of the transmission line with square wave input at 1200 kHz: Channel 1 is at the beginning of the interconnect and Channel 2 is measured at the load of the interconnect.

The ultimate goal for us is to model the r, l, and c parameters of the transmission line so that we can compute the Spice simulation of the circuit to match with the experimental result in Figure 4.1. The ABCD parameters model of the transmission line along with the capacitors in the circuit is going to be developed in the next section.

4.2 ABCD parameters of the circuit without the MOSFET driver chip

The ABCD parameters model introduced in Section 2.5 for the interconnect is constructed primarily to compute the frequency response of the circuit. The ABCD parameters of

the simple elements in the distributed network and the ABCD parameters for a RLC transmission line length L (the derivation is shown in Appendix A.1) are used to developed the ABCD parameters model of the interconnect. Since the ABCD parameters of a cascade of two linear systems is the product of ABCD parameters of the individual systems, we can represent the ABCD parameters of the circuit including the gate load and capacitances at the input as

$$\begin{aligned}
&\begin{bmatrix} A & B \\ C & D \end{bmatrix} \\
&= \begin{bmatrix} 1 & 0 \\ sC_P & 1 \end{bmatrix} \begin{bmatrix} \cosh(\theta L) & Z_o \sinh(\theta L) \\ \frac{1}{Z_o} \sinh(\theta L) & \cosh(\theta L) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC_L & 1 \end{bmatrix} \\
&= \begin{bmatrix} \cosh(\theta L) & Z_o \sinh(\theta L) \\ sC_P \cosh(\theta L) + \frac{1}{Z_o} \sinh(\theta L) & sC_P Z_o \sinh(\theta L) + \cosh(\theta L) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ sC_L & 1 \end{bmatrix}
\end{aligned} \tag{4.1}$$

The capacitance C_P at the driver chip location is the 15 pF scope probe capacitance. The transmission line is terminated by the equivalent input capacitance which consists of a 15 pF scope probe capacitance and a 1000 pF capacitor which is used to simulate the IRF 540 gate capacitance.

Since the output port of the circuit is open-circuited with output current $i_2 = 0$, the transfer function of the circuit is obtained from Equation 4.1

$$H(s) = \frac{V_2}{V_1} = \frac{1}{A} = \frac{1}{\cosh(\theta L) + Z_o \sinh(\theta L)\, sC_L} \tag{4.2}$$

Here $Z_o = \sqrt{\frac{r+sl}{sc}}$, $\theta = \sqrt{(r+sl)\,sc}$, L is the total length, and then s is the complex frequency(jw). The transfer function could be used to predict the frequency response of the circuit, and this is computed by Matlab for a given r, l, and c (see Appendix C.1.1). On the other hand, the *fminsearch* function in Matlab and the experimental results from frequency responses are used to determine the r, l, and c values of the transmission line.

4.3 Optimize the RLC parameters with 'fminsearch' in Matlab

The transfer function obtained in Equation 4.2 is used to compute the frequency response of the circuit. We use the *fminsearch* function in Matlab to determine the r, l, and c values of the line. We collect the raw data from the scope and compute the FFT to obtain the frequency responses at these frequencies. To compute with the *fminsearch* function, the initial values of resistance $init\_r$, inductance $init\_l$, and capacitance $init\_c$ are used for the optimization.

The *fminsearch* function tries to match the frequency response obtained by adjusting r, l, and c values in Equation 4.2. The function is provided the measured frequency responses at different frequencies. The larger number of frequency response data used in this process, the more accurate results of r, l, and c parameters can be expected. The *fminsearch* function will return values of r, l, and c and these values are used in the transfer function (Equation 4.2) to compute the frequency response of the line in Matlab. This result is compared with the experimental frequency response to see how well they are

matched.

4.4 Experimental frequency responses from the oscilloscope

Two different methods are used to input the data of frequency response of the circuit from the experimental results. The two methods are compared to see which one is the better match to the frequency response from the transfer function in Equation 4.2.

4.4.1 Collect the raw data at single frequency

The first method collects set of raw data from the oscilloscope with certain frequency square wave input and computes as many harmonics as possible the frequency response. We will use a frequency of 1.2 MHz to compute this frequency response. Since we have $\frac{2000}{2} = 1000$ points in the FFT within the Agilent scope, we can compute up to 80 points in the frequency response. The odd harmonics take place at 7, 19, 31 . . . 943, 955, accordingly. Figure 4.2 shows the computational result of frequency responses at 1.2 MHz:

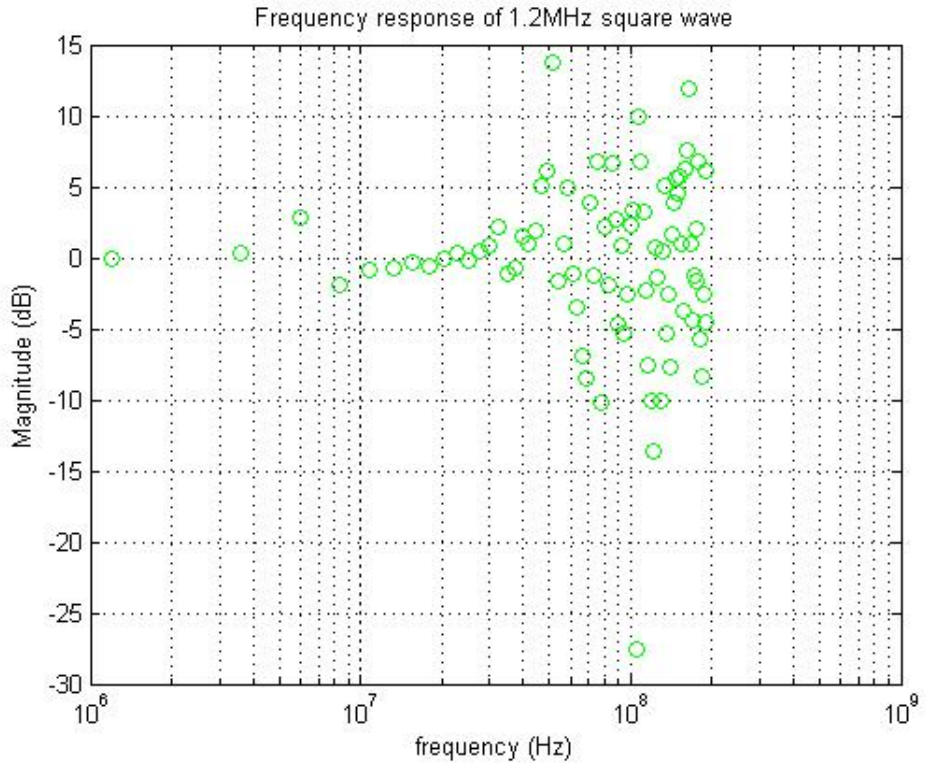


Figure 4.2: Frequency responses of the transfer function at harmonics of 1.2 MHz.

We can see the tremendous scatter in the frequency responses beyond 80 MHz. Since the later harmonics in the raw data has weaker, the trend of the response seems to be inconclusive and no good parameters extraction or match of the frequency response could be obtained.

4.4.2 Collect the raw data at different frequencies

To try to improve the results by more precise measurement of frequency response, we collect several sets of raw data at different square wave frequencies and compute the frequency

response for each frequency. The first five harmonics at each frequency are taken into account and plotted in the frequency responses respectively. We use 600 kHz, 1200 kHz, and 2400 kHz square wave inputs with the total fifteen harmonics to complete the frequency response of the circuit as seen in Figure 4.3. If there is an overlap frequency responses point coming from the different frequency inputs, they are averaged in the results at these harmonics.

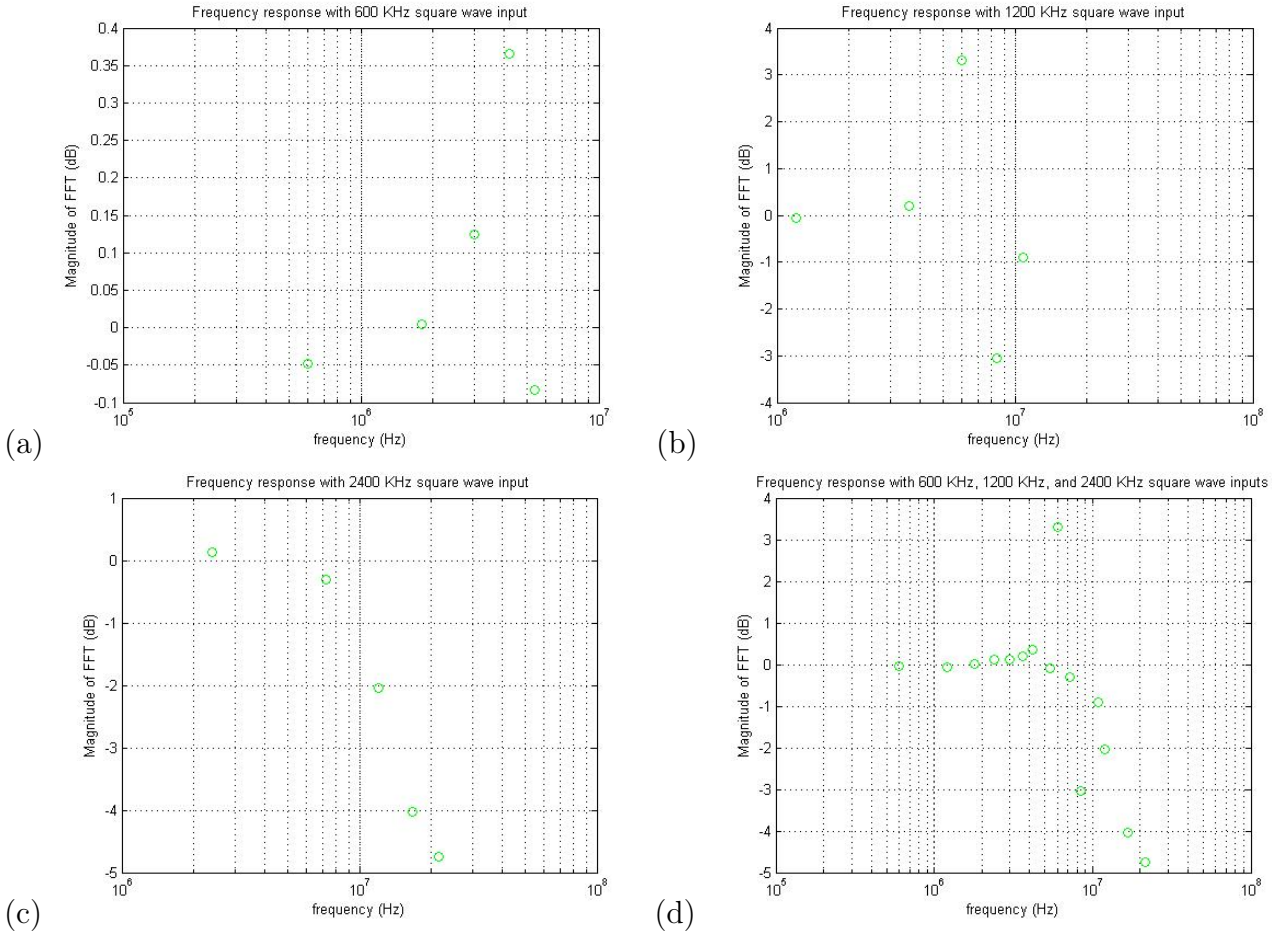


Figure 4.3: Frequency responses at frequency (a) 600 kHz. (b) 1200 kHz. (c) 2400 kHz. (d) the combination of the threes.

The second method provides a more complete frequency response of the circuit as shown in Figure 4.4. Based on the frequency response, we are able to determine the values of r, l, and c for the transmission line computationally to match the frequency response with the *fminsearch* function used in Matlab and the resultant frequency response from transfer function is shown in the Figure 4.4. The solid line shows the frequency response of the transfer function with extracted parameters $r = 1.8 \times 10^{-1}$ Ω/mm, $l = 8.1 \times 10^{-9}$ H/mm, and $c = 7.2 \times 10^{-13}$ F/mm extracted from the computation with *fminsearch* function in Matlab; however, this method would not characterize the frequency response of the circuit since the range of the frequency response that can be measured with generator, is limited by the function generator to 15 MHz (input) .

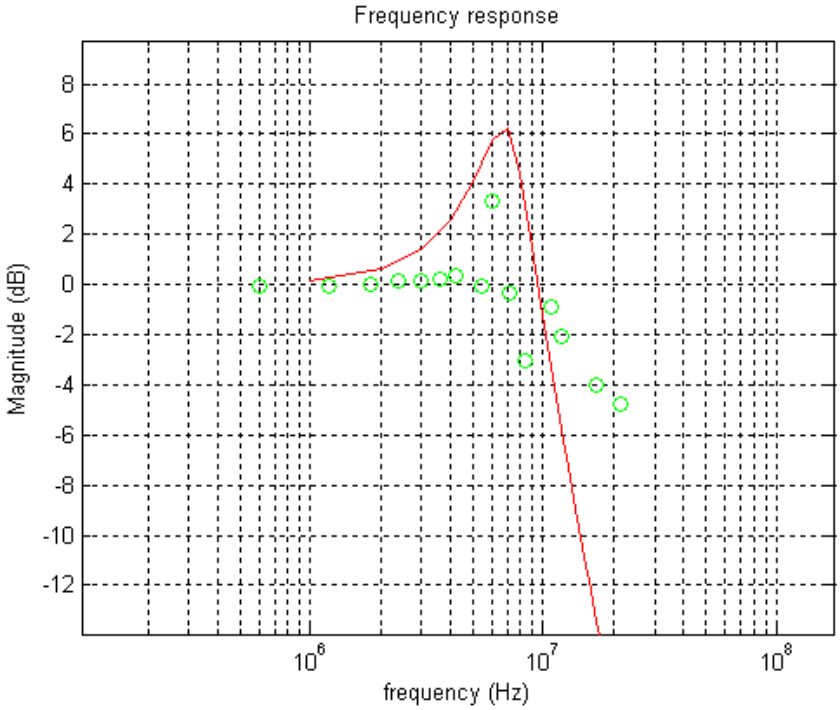


Figure 4.4: The solid line shows computational result from transfer function with $r = 1.8 \times 10^{-1}$ Ω/mm, $l = 8.1 \times 10^{-9}$ H/mm, and $c = 7.2 \times 10^{-13}$ F/mm, the bubbles show the experimental result.

Since the function generator used in the experiment could only generate a square wave input signal up to 15 MHz, the behaviour of the frequency response could be studied only up to $9 \times 15 = 135$ MHz using this method. However, the frequencies above this also play a role in the performance of the board. In addition, the oscilloscope sampling matters: A large number of samples could help improve the spectral resolutions with better fit on the frequency response. To complete the frequency response at higher frequencies, a network analyzer is used to measure the scattering parameters and is discussed in the next section.

4.5 Modeling the transmission line using network analyzer

Since we require the frequency response at much higher frequencies to determine more precise r, l, and c parameters for the transmission line, the network analyzer is used to measure the scattering parameters with magnitude and phase. Before connecting the BNC adapters to the transmission line circuit, we meticulously calibrate the network analyzer following the calibration method described in Appendix B.2. The measurement is performed with circuit in a shielded metal box with two BNC adapters firmly mounted on the input and output of the transmission line. The scattering parameters measured with network analyzer are converted into ABCD parameters using '$s2abcd$' function in Matlab provided in the Appendix C.1.2. The result from the network analyzer on the circuit are more reliable since we are able to measure the scattering parameters in a frequency range between 300 kHz and 1300 MHz. The same method is used to extract the r, l, and c values of the transmission line from transfer function with search technique using Matlab (*fmin-*

search function see Appendix C.1.3) . As a result, we have seen a more accurate matching frequency response between the transfer function with extracted r, l, c performance and experimental data with the r, l, and c values of $r = 2.8 \times 10^{-3}$ Ω/mm, $l = 2.9 \times 10^{-11}$ H/mm, and $c = 1.6 \times 10^{-11}$ F/mm is obtained and shown in Figure 4.5.

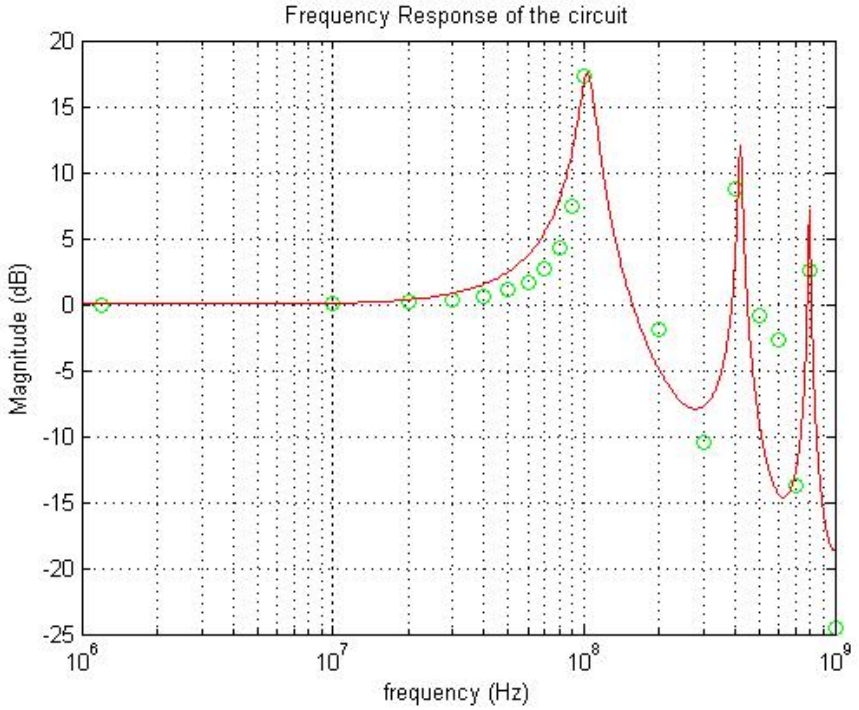


Figure 4.5: The solid line represents computational result from transfer function with $r = 2.8 \times 10^{-3}$ Ω/mm, $l = 2.9 \times 10^{-11}$ H/mm, and $c = 1.6 \times 10^{-11}$ F/mm, and the bubbles represent the experimental results from network analyzer.

4.6 Spice simulation of the RLC circuit without the MOSFET driver chip

The interconnect circuit is simulated with Spice circuit simulator with the r, l, and c

values of the transmission line determined in the previous circuit. We use the fact that the function generator has a 50 Ω output impedance in this simulation. There are two 15 pF capacitance from the scope probes and the transmission line terminating by an equivalent capacitor used to replace the NMOS transistor on the line. In addition, the transmission line is split into sixty small segments for simulation in Spice. Figure 4.6 shows the circuit configuration used to compute the simulation and two simulation results: One is from the input of the transmission line and the other is from the output.

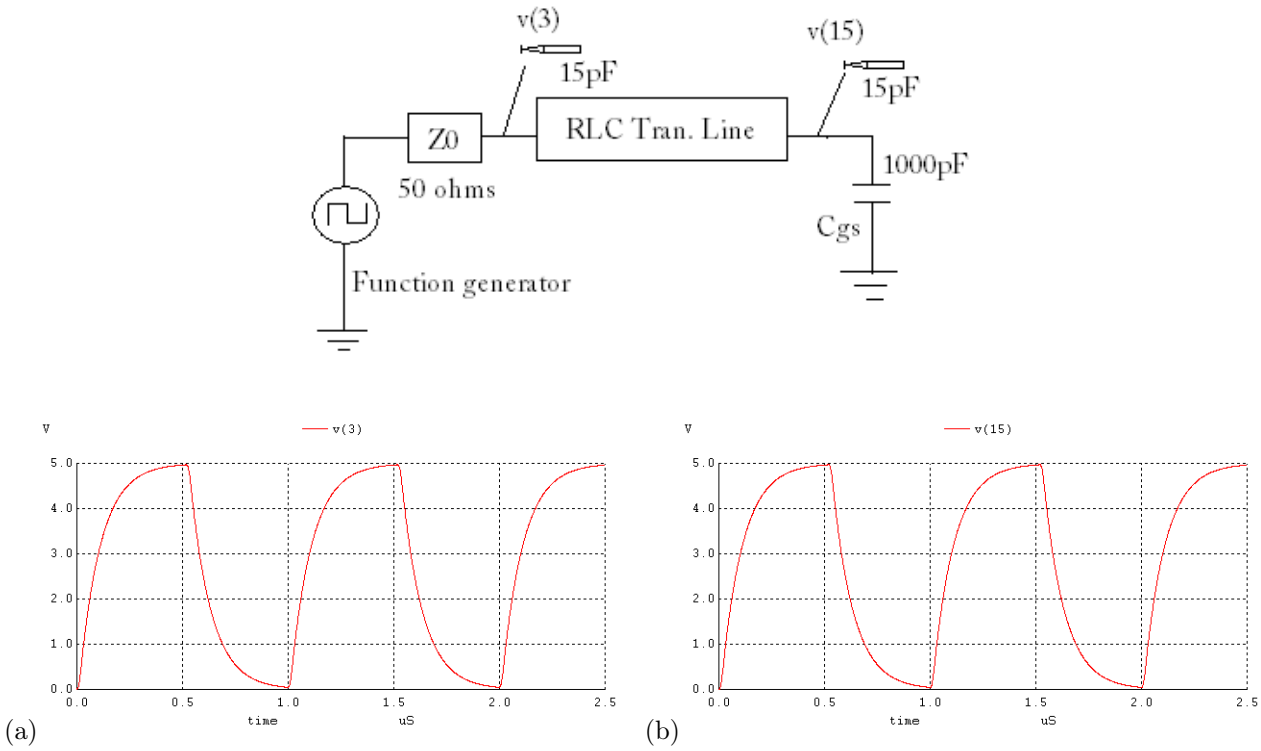


Figure 4.6: Spice simulation results without the driver chip (a) output voltage in the beginning of the interconnect. (b) output voltage at the load of the interconnect.

Comparing these results with the experimental results of Section 4.1, we see close behaviour from the simulation results. We thus conclude that the extracted values of r, l,

and c for the transmission line are reasonably precise and the model can be used to study the circuit with the MOSFET driver and power MOSFET in place.

4.7 Conclusion

The MOSFET driver board is studied without the MOSFET driver chip and tested throughout this chapter. The transmission line terminated with a equivalent capacitor is used to construct the ABCD parameters and decide the transfer function parameters. The transfer function frequency response is used to model the r, l, and c parameters of the transmission line and the search function *fminsearch* in Matlab is used to optimize the r, l, and c values to match experimental data.

Two methods are introduced to compute the frequency response of the circuit from function generator based on experimental results and compared with the computational result of frequency response from transfer function with determined r, l, and c values. Furthermore, the network analyzer is used to measure the scattering parameters of the circuit which are converted to ABCD parameters in Matlab. Based on the measurement result from network analyzer, the final r, l, and c values are $r = 2.8 \times 10^{-3}$ Ω/mm, $l = 2.9 \times 10^{-11}$ H/mm, and $c = 1.6 \times 10^{-11}$ F/mm for the transmission line circuit without the driver chip. This model is set up for further study in the next chapter.

5 Spice Simulation of the MOSFET Driver Board and Improvement

5.1 Spice simulation of the MOSFET driver

After completing the analysis of the transmission line of the circuit and realizing the r, l, and c values for the transmission line, in the chapter we model the MOSFET driver board by simulation of the circuit using Spice. From the experimental point of view we replace the driver chip back into the MOSFET driver board and replace the equivalent capacitor with the MOSFET power transistor (IRF540). The experimental result is shown in Figure 5.1 with the same probes measuring at the same locations of the circuit (Figure 4.6).

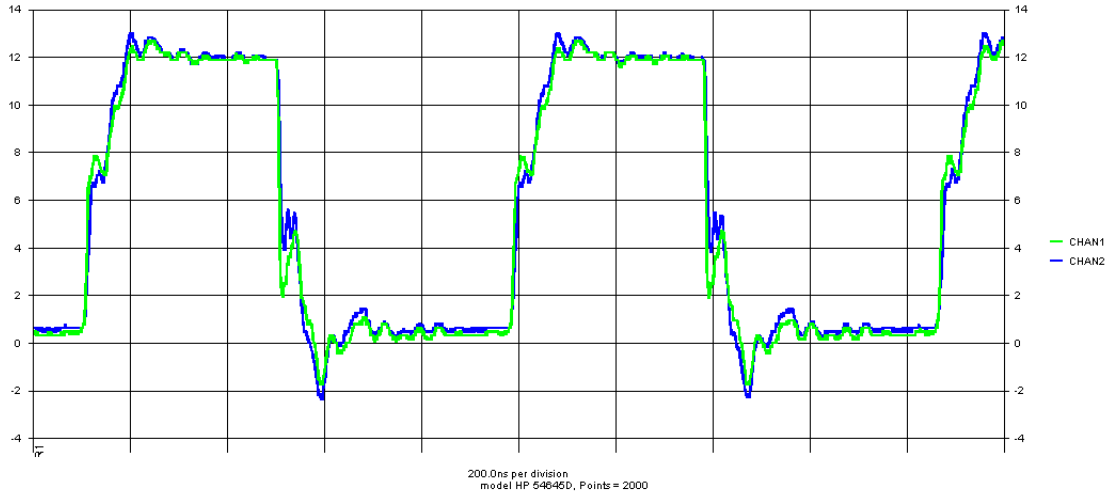


Figure 5.1: Experimental result of the MOSFET driver with square wave input at 1200 kHz: Channel 1 is measured from the beginning of the interconnect and Channel 2 is measured at the gate of the MOSFET.

To accomplish the simulation of the MOSFET driver with Spice circuit simulator, a simple circuit is designed to represent the MOSFET driver chip. As shown in Figure 5.2,

a series 7 Ω resistance and a CMOS inverter are used along with the transmission line and the MOSFET power transistor for this simulation. The CMOS transistor parameters are chosen so that 4.7 amps current is available to charge the load through PMOS and discharge the load through NMOS transistor in the CMOS circuit. The process parameter is calculated as per:

$$I_{DS} = \frac{K_p}{2} \cdot \frac{W}{L} (V_{GS} - V_{TN})$$

$$\therefore K_p = \frac{2I_{DS}}{(V_{GS} - V_{TN})^2} \frac{L}{W}$$

$$= \frac{2 \times 4.7A}{(10V - 0.5V)^2} \cdot \frac{1u}{12u} = 8.68 \times 10^{-3} \tag{5.1}$$

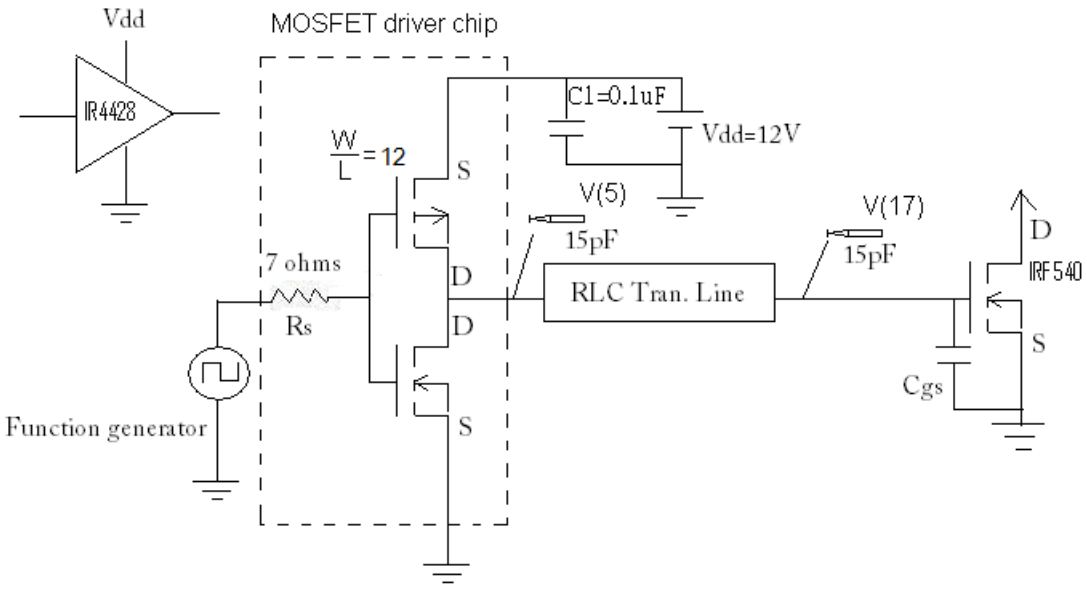
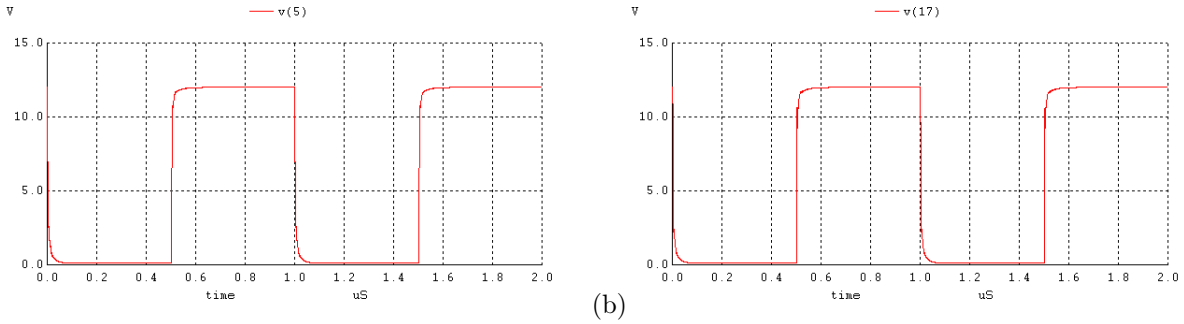


Figure 5.2: Configuration of the MOSFET driver in Spice simulation.

The simulation results are shown in Figure 5.3. From the output, during the rise and the fall time in both results, the imperfections are not significant and the ringing on the rising and the falling edge of the waveform is not clearly observable. Different parameters of the CMOS inverter are implemented along with different values of the input resistance in the design of the MOSFET driver chip. In all cases, we are not able to produce a match with what has been seen in the experiment shown in Figure 5.1.



(a) (b)

Figure 5.3: Spice simulation of the MOSFET driver (a) input voltage at the beginning of the interconnect. (b) output voltage at the gate of the MOSFET.

5.2 Spice simulation of the MOSFET driver with power supply

We know the wires connecting the power source to the MOSFET driver chip carry large current so that it could have significant inductive coupling effects on the MOSFET driver. The inductive effects coming from the entire power supply circuitry is often neglected in practice; however, it may not be negligible given the rise and fall time that we have dealt with. We add an equivalent power supply circuitry to the Spice simulation which represents the power source along with the wires as seen in Figure 5.4. The inductances are estimated

using the inductances of the straight wire formulae to be within 0.3 nH to 1.2 nH using E.B. Rosa's Formulae[13].

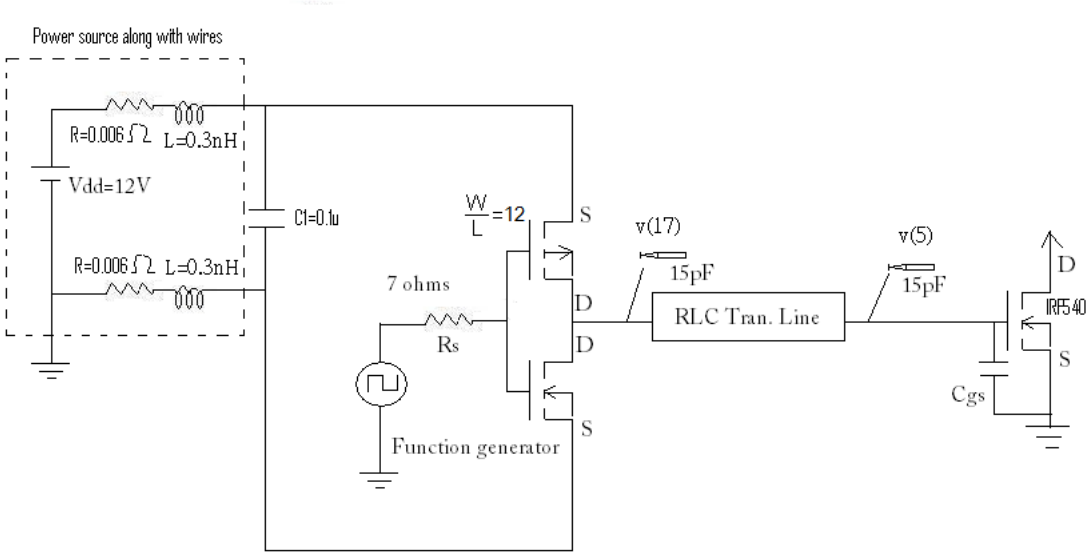
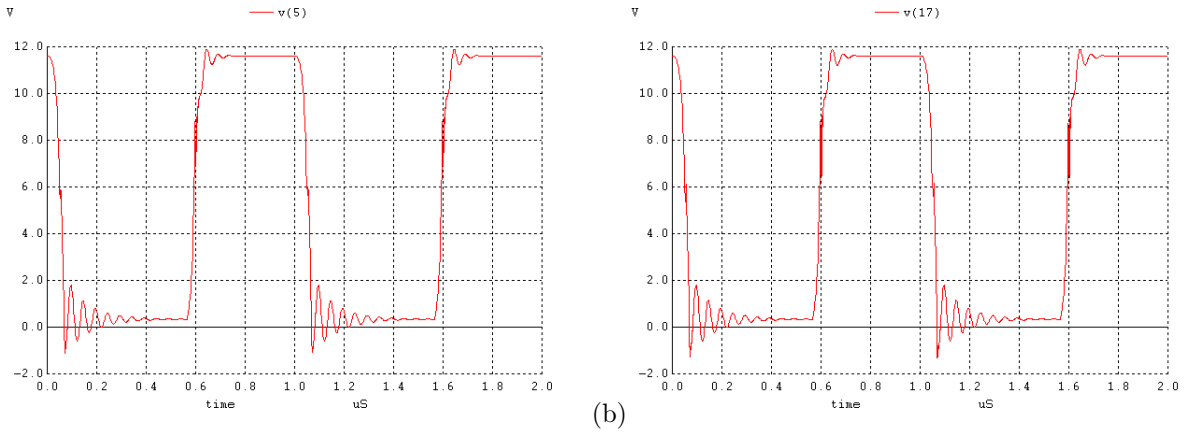


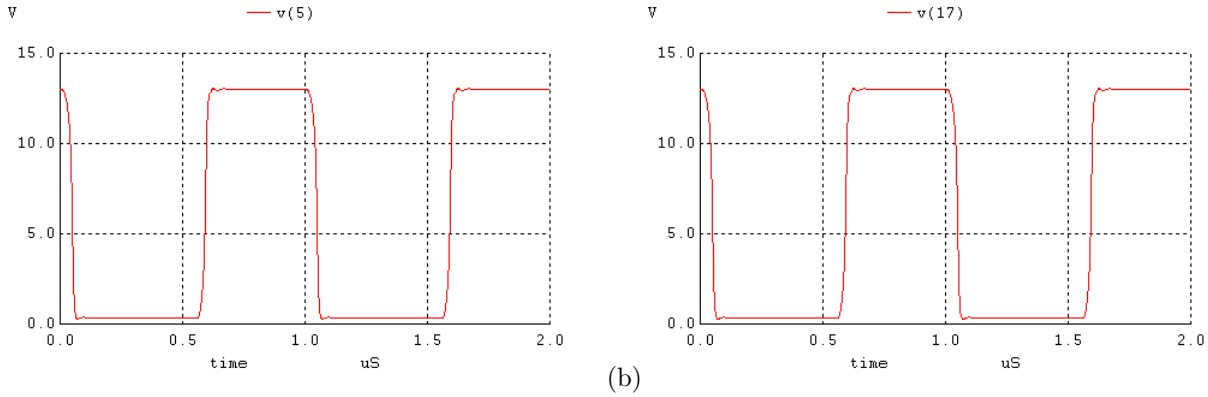
Figure 5.4: Configuration of the MOSFET driver with power supply in Spice simulation.

With the power to the circuit the imperfections during the signal transition and the ringing on the rising and the falling edge of the waveform are clearly seen in the results of this simulation in Figure 5.5. The simulation results are now reasonably matched with what was observed in the experiment. Furthermore, to see if the distributed r, l, c circuit line really affects these results, we replace it by a r, c transmission line in the MOSFET driver board for the simulation to see if the inductive effects from the transmission line is negligible compared to the effect of the power source. These simulation results are shown in Figure 5.6. The simulation results indicate that inductive effects from the transmission line and the wires connected to the power source are both considerable, and neither can be ignored in the result of the imperfections occurring in signal transition.



(a) (b)

Figure 5.5: Spice simulation of the MOSFET driver with power supply(a) input voltage at the beginning of the interconnect. (b) output voltage at the gate of the MOSFET.



(a) (b)

Figure 5.6: Spice simulation of the MOSFET driver with power supply using only r, c line(a) input voltage at the beginning of the interconnect. (b) output voltage at the gate of the MOSFET.

5.3 Spice simulation of the MOSFET driver board for improvement of waveform

Three different approaches are tried by simulation for the purpose of reducing the imperfections occurring at the MOSFET gate waveform and improving the slew rate of this waveform.

5.3.1 Decrease the distance between the MOSFET driver chip and the MOSFET

Shortening the length of the transmission line in the Spice simulation was initially attempted to see if the imperfection size will become smaller and the slew rate will improve. Shortening the length will result in reducing the inductive effects coming from the transmission line of the MOSFET driver board as recommended from power MOSFET and driver chip manufacturers[10]. The rising and the falling signal waveforms in the end of the transmission line where the output voltage occurs at the gate of the transistor will be focused upon. We attempt to shorten the lengths of the transmission line with 1/2, 1/10, and 1/20 of 6 cm and observe the results with Spice simulation since the MOSFET driver board model has been clarified in previous section to represent the circuit. From the simulation results in Figure 5.7, the imperfection is not improved when we shorten the length of the transmission line to 1/10 of 6 cm, but with further decrease of the length to 1/20 of 6 cm, we see small improvement on the imperfections in the waveform. While this shows that the effect of imperfections at the gate of transistor has a dependency on the length of the transmission line in a MOSFET driver circuit, it does not alleviate it.

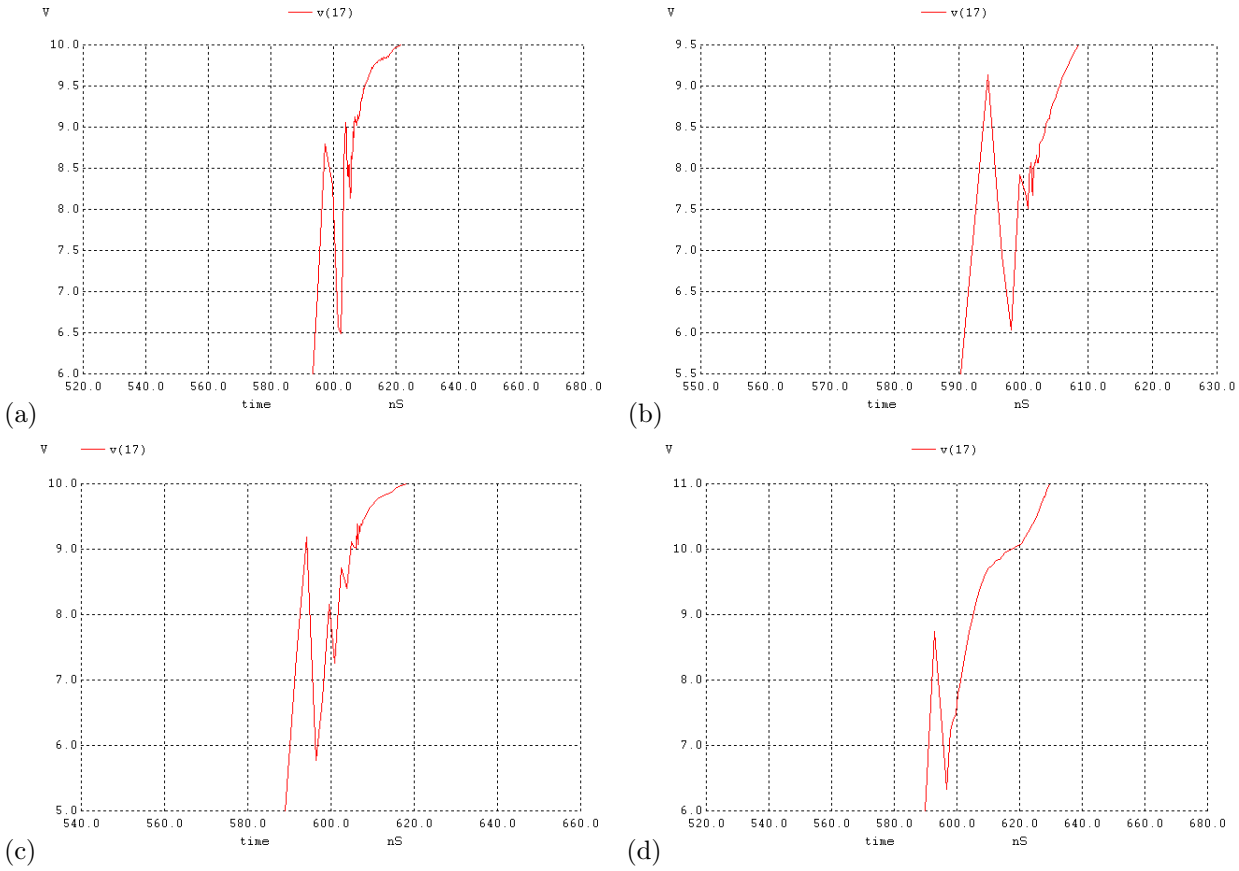


Figure 5.7: Magnified simulation results of imperfection at the gate of transistor when the length of the transmission line is (a)6 cm. (b)1/2 of 6 cm. (c)1/10 of 6 cm. (d)1/20 of 6 cm.

5.3.2 Model the power supply circuitry of the MOSFET driver

Since the inductive effects coming from the wires used to connect the power source with the MOSFET driver has a big influence on the circuit, the second attempt is to adjust the capacitor C1 value in the power supply circuitry to see if we could reduce the effects from the wires. The capacitor with the value of 0.01 µF, 0.1 µF, 1 µF, and 10 µF are used to complete the comparisons in the Spice simulation according to the Figure 5.8. However,

we are not able to see any significant improvement in these simulation results.

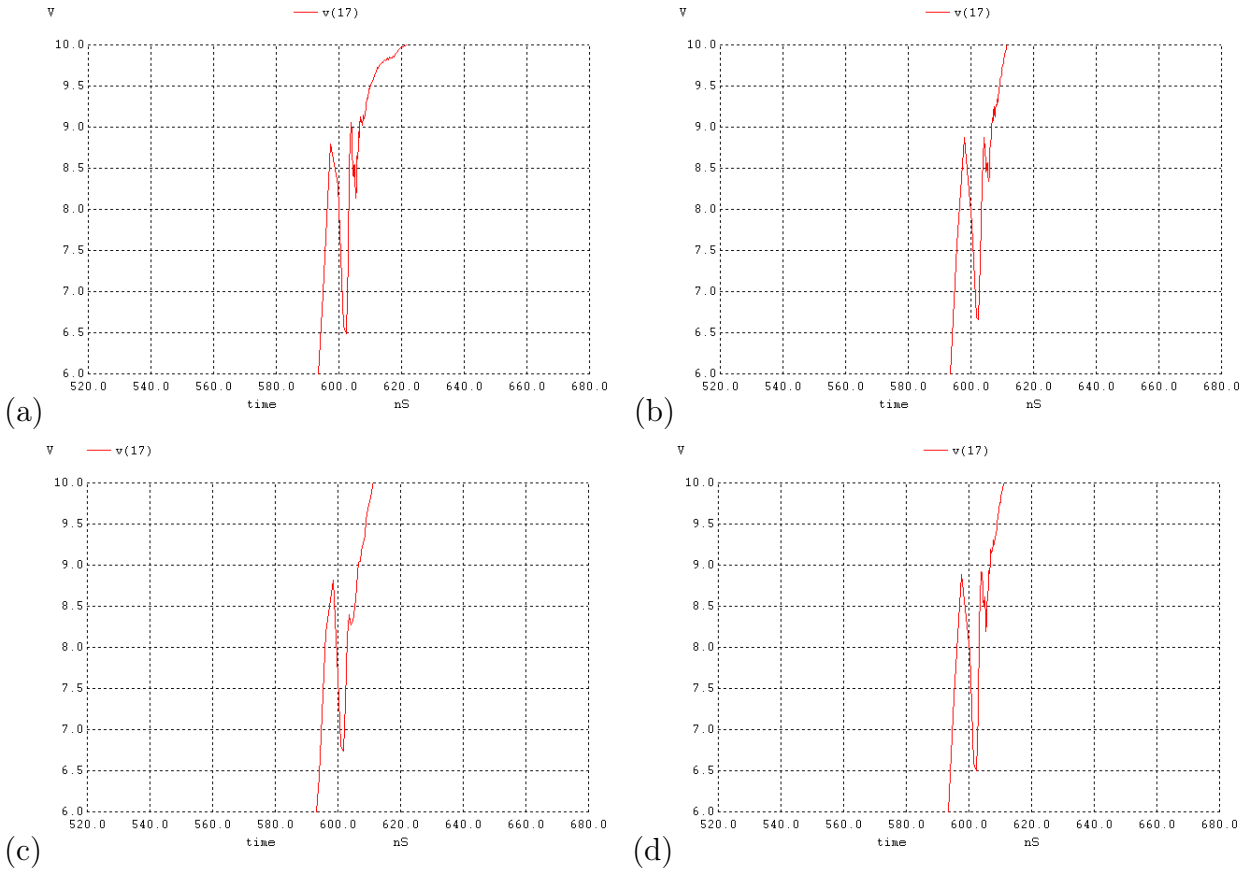


Figure 5.8: Magnified simulation results showing imperfection at the gate of transistor when the (a) 0.01 µF (b) 0.1 µF (c) 1 µF (d) 10 µF capacitor is used in the power supply circuitry.

5.3.3 Insert a capacitor to split up transmission line of the MOSFET driver

We then attempted to add different values of capacitor in the middle of the transmission line to break it into 2 segment with 3 cm line each as shown in Figure 5.9. A capacitor value

of 0.01 µF is first used to test the idea. The experimental result at the gate of transistor shows that the waveform looks distorted and the MOSFET driver will not deliver the square waveform even after a long period. After several attempts, a 1 nF capacitor is finalized to implement in the circuit as it provides for improvement of the imperfection of the waveform at the gate of the MOSFET. In the simulation results as shown in Figure 5.10, we see that the size of imperfection shrinks down to a range of 0.5 volt from 2.5 volt when we use a 1 nF capacitor to split up the transmission line in half with 30 segments on the right and 30 segments on the left.

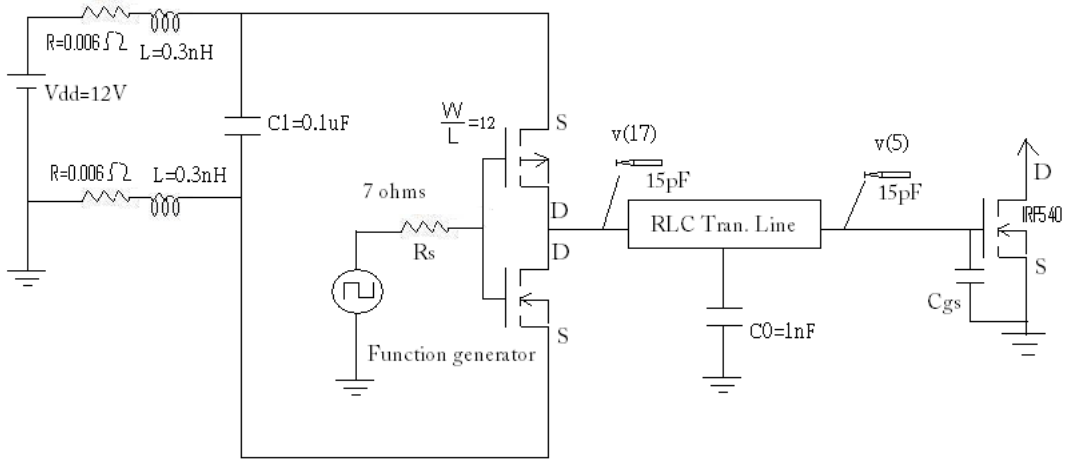


Figure 5.9: Configuration of the MOSFET driver board by adding a capacitor in the middle of the transmission line.

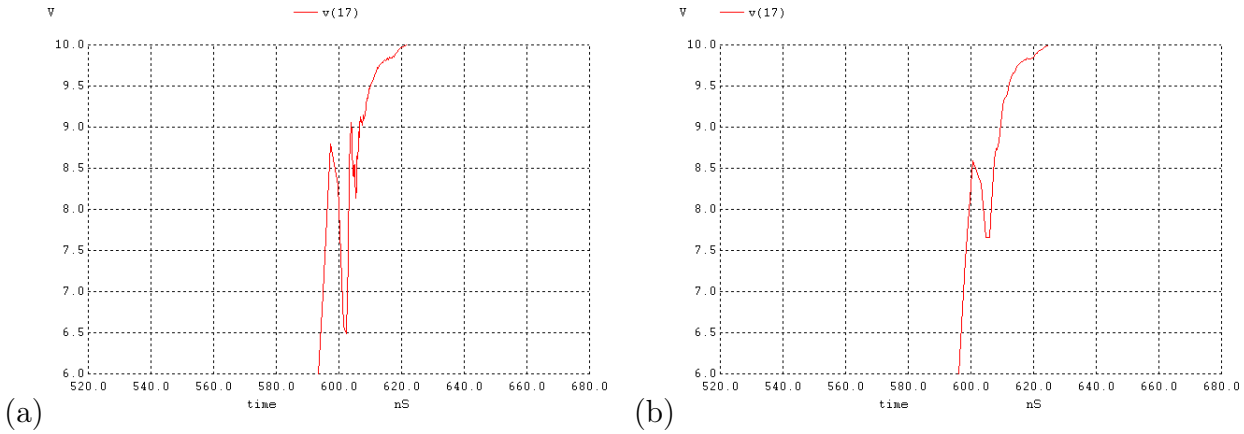


Figure 5.10: Imperfections size comparison in Spice simulation of the MOSFET driver (a) without the capacitor to split it in half. (b) with a 1 nF capacitor.

Furthermore, the experimental results are shown in Figure 5.11 with a capacitor splitting up the transmission line in half, the size of the imperfections has become smaller. As a result, the rise and fall time during the signal transition at the gate of the MOSFET are fairly reduced. The rise time has reduced to 96 ns from 108 ns as measured from 0 to 10 V at which level the MOSFET is fully turned on, so the slew rate becomes $\frac{10V}{0.096\mu s} = 104.2$ V/µs. the fall time has also reduced to 136 ns from 140 ns as measured from 10 to 0 V at which level the MOSFET is fully turned off, so the slew rate becomes $\frac{10V}{0.136\mu s} = 73.5$ V/µs. We see that the slew rates have slightly been improved compared with the ones in Section 1.1(as shown in Figure 1.2). Thus, we have shown that adding a capacitor in the middle of the transmission line will improve the slew rate of the waveform in signal transition in the power MOSFET.

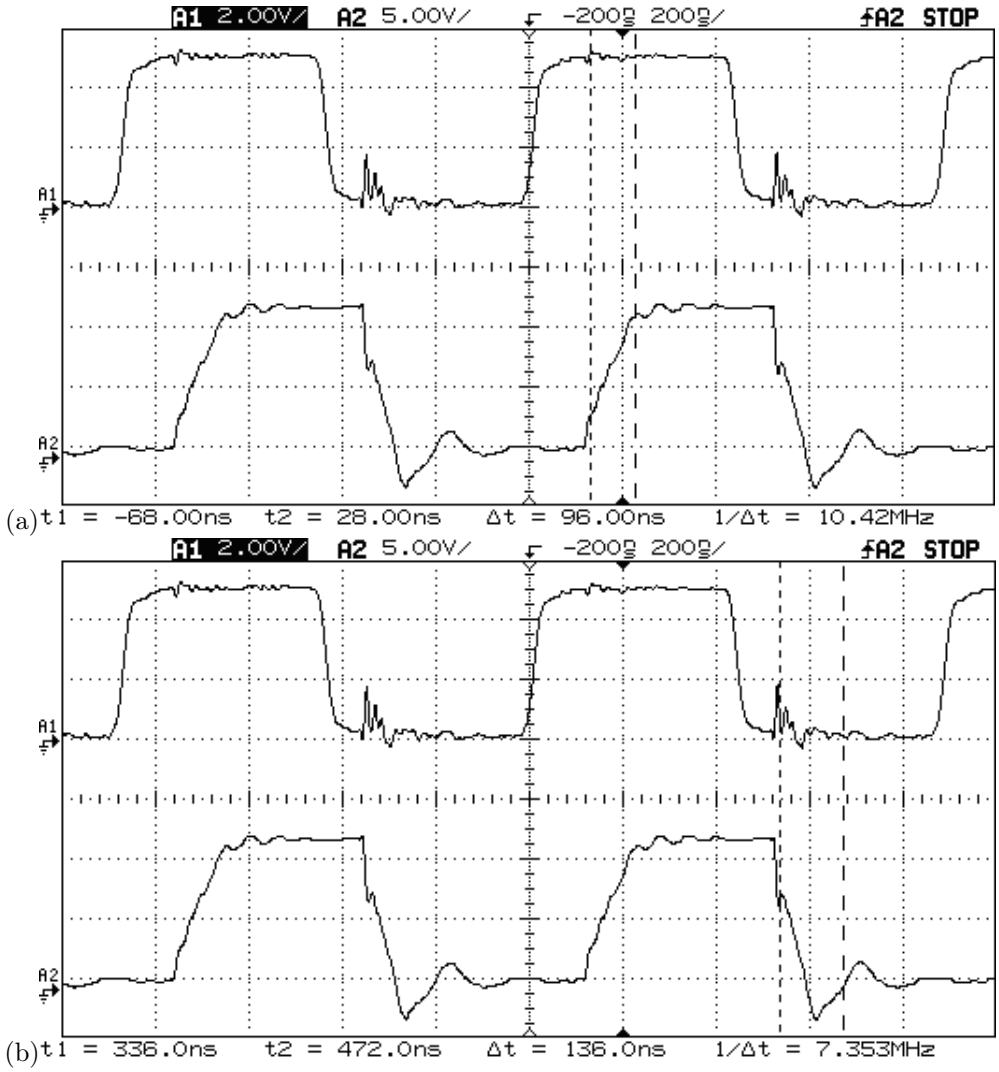


Figure 5.11: (a) Rise time, and (b) fall time measured at the gate transistor when a 1 nF capacitor is used to split the transmission line in half. Channel A1 is the output from function generator and Channel A2 is the output from the gate of the MOSFET.

We know that adding a capacitor in the middle of the transmission line could provide a buffer against imperfections. However, this could delay turn on/off time of the gate signal. From Figure 5.12, the propagation delays for the rise and the fall time are measured. The turn on/off delay time are longer with 140 ns and 100 ns respectively, compared to the

one measured in Figure 1.3 which shows the propagation delays are 124 ns and 88 ns. In conclusion, adding a capacitor in the middle of the transmission line will improve the slew rate of the waveform at the gate transistor but prolong propagation delays.

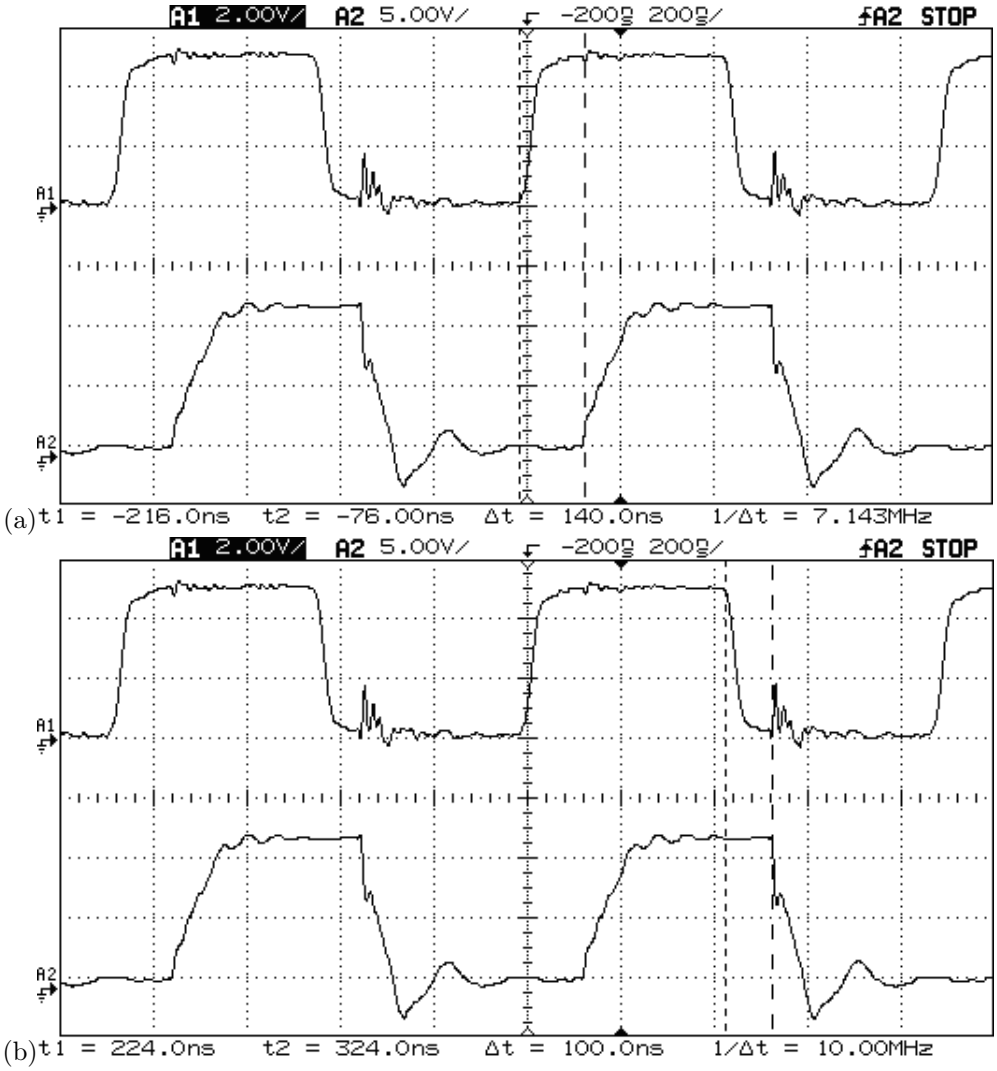


Figure 5.12: (a) Turn on, and (b) turn off delay time measured at the gate of the MOSFET when a 1 nF capacitor is used to split the transmission line in half. Channel A1 is the output from function generator and Channel A2 is the output from the gate of the MOSFET.

5.4 Future improvement

Since we realize that the imperfections during the signal transition at the gate transistor are sensitive to the distance variations of the transmission line between the MOSFET driver chip and the MOSFET, it is worth studying what would happen when we extend the length of the line for experiments. Another choice is to change the thickness of the line which would lead to different values of r, l, and c per unit length. Besides using a single small value of capacitor in the middle of the transmission line to improve the MOSFET driver performance, we could consider creating more than one capacitor to split up the transmission line. However, this may slow down the signal transition and the value of the capacitor has to be carefully chosen because the MOSFET driver may be unable to drive the resultant circuit.

5.5 Conclusion

We have completed the Spice simulation of the MOSFET driver board and the simulation results match in experimental results. An additional capacitance is designed in the simulation and implemented in experiments to verify the simulation results. Three different attempts to improve the imperfections at the gate of the power transistor were simulated with Spice and the results show that adding a capacitor in the middle of the transmission line between the MOSFET driver chip and the MOSFET can possibly reduce the imperfection size and improve the slew rate; however, the propagation delays are increased.

Moreover, it has been shown that the dependency of length of the transmission line can have an impact on the imperfection in signal transition at the gate transistor. By changing the length of the line one can minimize the transmission line effect to the power MOSFET and optimize the performance of the MOSFET driver. However, the power supply source inductances play a major role.

The thesis has also shown two methods of obtaining the transmission line r, l, and c parameters; one is by collecting the raw data from a scope and computing the frequency response and extracting parameters from the transfer function by search technique, the other approach is by measuring the scattering parameters using network analyzer. By modeling the transmission line parameters, we are able to show complete analysis of the MOSFET driver board. Spice simulation is used to verify the experimental results and later provides the possible predictions for optimizing the MOSFET driver's performance.

Finally, the thesis has provided a model of the MOSFET driver board for Spice simulation for further development and improvement of the driver's performance. The methods used to obtain the transmission line parameters can help designers for driver analysis.

A APPENDIX

A.1 ABCD parameters for a uniform RLC transmission line

ABCD transmission line parameters are the transfer function of the 2-port network with the form

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{A.1}$$

where v_1, v_2 are input and output voltage. i_1, i_2 are input and output current.

The advantage of ABCD transmission parameters are that they are useful for obtaining the characteristics of n cascaded 2-port network. The following ABCD parameters for a section of the line are developed from[6]. We consider a uniform distributed transmission line which consists of a small section of length Δx with resistance, inductance, and capacitance per unit length *r, l,* and c shown in Figure A.1.

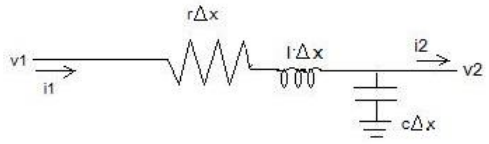


Figure A.1: A small segment of a uniform RLC transmission line

We can obtain two equations from the figure A.1

$$v_1 = v_2 + i_2 (r + sl) \Delta x \tag{A.2}$$

$$i_1 = i_2 + v_2 sc \Delta x \tag{A.3}$$

and put them in the matrix form

$$\begin{bmatrix} v_1 \\ i_1 \end{bmatrix} = \begin{bmatrix} 1 & (r+sl)\triangle x \\ sc \triangle x & 1 \end{bmatrix} \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} = E \begin{bmatrix} v_2 \\ i_2 \end{bmatrix} \tag{A.4}$$

Since a cascade of two linear systems is the product of ABCD parameter matrices of the individual systems, we can express an RLC transmission line of Length H with n of each section of length $\triangle x$ as a ABCD parameter matrix

$$E^n = \begin{bmatrix} 1 & (r+sl)\triangle x \\ sc \triangle x & 1 \end{bmatrix}^n \tag{A.5}$$

where, $n = \frac{H}{\triangle x}$.

To find the limit of the above matrix as $n \to \infty$, we will let E be diagonally decomposed as $E = W \bigwedge W^{-1}$, where $\bigwedge$ is a diagonal matrix of eigenvalues of E, and W is the eigenvector matrix. The matrix E can be diagonalized as

$$\begin{bmatrix} 1 & a \\ b & 1 \end{bmatrix} = \frac{1}{\sqrt{a+b}} \begin{bmatrix} \sqrt{a} & \sqrt{a} \\ \sqrt{b} & -\sqrt{b} \end{bmatrix} \begin{bmatrix} 1+\sqrt{ab} & 0 \\ 0 & 1-\sqrt{ab} \end{bmatrix} . \frac{\sqrt{a+b}}{2\sqrt{ab}} \begin{bmatrix} \sqrt{b} & \sqrt{a} \\ \sqrt{b} & -\sqrt{a} \end{bmatrix} \tag{A.6}$$

where

$$a = (r + sl) \triangle x$$

$$b = sc \triangle x.$$

We can solve for $E^n = W \bigwedge^n W^{-1}$, and obtain

$$\begin{bmatrix} 1 & a \\ b & 1 \end{bmatrix}^n$$

$$= \frac{1}{2} \begin{bmatrix} \left(1+\sqrt{ab}\right)^n + \left(1-\sqrt{ab}\right)^n & \sqrt{\frac{a}{b}} \left(\left(1+\sqrt{ab}\right)^n - \left(1-\sqrt{ab}\right)^n\right) \\ \sqrt{\frac{b}{a}} \left(\left(1+\sqrt{ab}\right)^n - \left(1-\sqrt{ab}\right)^n\right) & \left(1+\sqrt{ab}\right)^n + \left(1-\sqrt{ab}\right)^n \end{bmatrix} \quad \text{(A.7)}$$

Let

$$Z_o = \sqrt{\frac{a}{b}} = \sqrt{\frac{r+sl}{sc}}$$

$$\theta = \sqrt{(r + sl)\, sc} = \frac{\sqrt{ab}}{\triangle x} = \frac{\sqrt{ab}}{\frac{H}{n}}$$

Substituting them back to Equation A.7 for E^n, the expression becomes

$$E^n = \frac{1}{2} \begin{bmatrix} \left(1+\theta\frac{H}{n}\right)^n + \left(1-\theta\frac{H}{n}\right)^n & Z_o \left(\left(1+\theta\frac{H}{n}\right)^n - \left(1-\theta\frac{H}{n}\right)^n\right) \\ \frac{1}{Z_o} \left(\left(1+\theta\frac{H}{n}\right)^n - \left(1-\theta\frac{H}{n}\right)^n\right) & \left(1+\theta\frac{H}{n}\right)^n + \left(1-\theta\frac{H}{n}\right)^n \end{bmatrix} \quad \text{(A.8)}$$

By using the identity

$$\lim_{n\to\infty} \left(1 + \frac{x}{n}\right)^n = \exp(x) \quad \text{(A.9)}$$

The ABCD parameter matrix for a distributed RLC transmission line of length H is given by

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\theta H) & Z_o \sinh(\theta H) \\ \frac{1}{Z_o} \sinh(\theta H) & \cosh(\theta H) \end{bmatrix} \tag{A.10}$$

B APPENDIX

B.1 Search function $'fminsearch'$

The *fminsearch* function is used to optimize the parameters throughout the thesis. This optimization method is used to estimate more accurate values of per unit length - resistance, inductance, and capacitance of interconnect. The *fminsearch* function can be performed using Matlab with the syntax

$$[x, fval] = fminsearch('function', init\_x)$$

It starts at the initial point $init\_x$ and finds a local minimum x of the function described in $'function'$. $init\_x$ can be a scalar, vector, or matrix. The $'function'$ function can contain several variables$(x_1, x_2, x_3, \ldots)$. The *fminsearch* function minimizes with the optimization parameters specified in $init\_x$ and returns in $fval$ the minimum value of $'function'$ function. The function can often handle discontinuity, particularly if it does not occur near the solution and can only minimize over the real numbers.

B.2 Network analyzer and calibration method

The HP 8712ES Network Analyzer used in the lab allows us to characterize a 2-port network system in the frequency domain. It introduces a sinusoidal wave into each port of the device under test (DUT) and measuring the transmitted and reflected waves over a large frequency range from 300 kHz to 1300 MHz. The network analyzer measures characteristic impedance, S-parameters, magnitude, and phase and shows them on the Smith chart.

Before starting to measure the S-parameters for the DUT, we need to first calibrate the network analyzer. According to the user manual guide, the circuit board is an non-insertable device. Thus, we will need to follow the non-insertable device calibration method: We connect the test cable with type-N(m) connectors to the network analyzers port 1 and port 2, and then connect the three standards(open, short, and load) to the BNC at the end of the both test cable following the screen prompts commands. The network analyzer internally measures each standard and computes the proper calibration coefficients. After we see the "Calibration complete" message, we remove the three standard connectors and now connect the analyzer to the load. We measure the magnitude and phase of the scattering parameters of the load.

C APPENDIX

C.1 Matlab functions

C.1.1 computation of the transfer function of the MOSFET driver without driver chip

```
function f = f_run(x)
freq = 1e6:1e6:1e9;          % frequency range %
r= x(1);         % resistance %
l= x(2);         % inductance %
c= x(3);         % capacitance %
L = 6.0e1;         % length L %
i=sqrt(-1);         % i %
Cl= 1.015e-9;          % equivalent output capacitance %
s=2*pi*freq*i;          % s = jw %
theta=((r+s*l).*(s*c)).^(1/2);
Zo=((r+s*l) ./ (s*c)).^(1/2);
Q = cosh(theta*L) + Zo.*sinh(theta*L).*s*Cl;          %inverse of the transfer function %
Q = Q';
H = 1./ Q;
figure;semilogx(freq,20*log10(abs(H)), 'r');grid
```

C.1.2 Network analyzer

```
i=sqrt(-1); % i %
s_12k =[2.594e-3 74.65; 993.7e-3 -2.347; 1.000 -543.6e-3; 3.157e-3 65.73];
s_10m =[21.11e-3 86.58; 999.9e-3 -4.093; 999.3e-3 -4.946; 20.97e-3 77.86];
s_20m =[40.85e-3 86.89; 995.5e-3 -8.686; 998.3e-3 -8.959; 41.09e-3 70.77];
s_30m =[61.39e-3 87.96; 993.4e-3 -13.50; 989.9e-3 -12.89; 60.40e-3 63.51];
s_40m =[81.38e-3 88.62; 994.8e-3 -17.54; 993.2e-3 -18.68; 79.28e-3 53.53];
s_50m =[100.7e-3 90.00; 986.6e-3 -23.58; 982.5e-3 -22.75; 95.92e-3 42.11];
s_60m =[119.7e-3 93.41; 985.3e-3 -28.21; 985.4e-3 -28.88; 111.7e-3 28.53];
s_70m =[142.2e-3 98.92; 977.8e-3 -34.57; 974.8e-3 -34.44; 127.4e-3 10.84];
s_80m =[176.3e-3 105.7; 966.5e-3 -41.64; 966.6e-3 -41.84; 149.2e-3 -13.40];
s_90m =[236.9e-3 113.8; 942.9e-3 -51.46; 941.9e-3 -50.45; 194.1e-3 -43.76];
s_100m =[362.4e-3 116.6; 884.1e-3 -63.57; 887.4e-3 -63.95; 293.9e-3 -81.85];
s_200m =[695.4e-3 18.39; 714.4e-3 -49.81; 710.5e-3 -48.95; 673.9e-3 60.68];
s_300m =[852.0e-3 33.81; 201.7e-3 -18.89; 203.1e-3 -20.12; 628.3e-3 47.78];
s_400m =[775.2e-3 -27.79; 591.4e-3 -107.7; 599.0e-3 -105.5; 761.8e-3 -12.78];
s_500m =[831.1e-3 -52.02; 471.3e-3 -129.2; 481.6e-3 -128.8; 780.3e-3 -35.15];
s_600m =[631.9e-3 -136.8; 336.3e-3 -73.64; 341.0e-3 -74.57; 705.3e-3 -114.8];
s_700m =[178.4e-3 -51.61; 119.4e-3 19.17; 119.3e-3 16.75; 816.2e-3 69.34];
```

```
s_800m =[222.5e-3 72.14; 893.3e-3 147.7; 886.0e-3 147.8; 274.3e-3 20.80];
s_1000m=[858.1e-3 -82.32; 44.63e-3 161.5; 47.94e-3 161.4; 895.7e-3 -68.13];
z0 = 50;
%Define a matrix of S-parameters
s11_12k = s_12k(1,1)*exp(j*s_12k(1,2)/180*pi);
s21_12k = s_12k(2,1)*exp(j*s_12k(2,2)/180*pi);
s12_12k= s_12k(3,1)*exp(j*s_12k(3,2)/180*pi);
s22_12k= s_12k(4,1)*exp(j*s_12k(4,2)/180*pi);
s_params_12k = [s11_12k s12_12k; s21_12k s22_12k];
abcd_params_12k = s2abcd(s_params_12k, z0);
s11_10m = s_10m(1,1)*exp(j*s_10m(1,2)/180*pi);
s21_10m = s_10m(2,1)*exp(j*s_10m(2,2)/180*pi);
s12_10m= s_10m(3,1)*exp(j*s_10m(3,2)/180*pi);
s22_10m= s_10m(4,1)*exp(j*s_10m(4,2)/180*pi);
s_params_10m = [s11_10m s12_10m; s21_10m s22_10m];
abcd_params_10m = s2abcd(s_params_10m, z0);
s11_20m = s_20m(1,1)*exp(j*s_20m(1,2)/180*pi);
s21_20m = s_20m(2,1)*exp(j*s_20m(2,2)/180*pi);
s12_20m= s_20m(3,1)*exp(j*s_20m(3,2)/180*pi);
s22_20m= s_20m(4,1)*exp(j*s_20m(4,2)/180*pi);
s_params_20m = [s11_20m s12_20m; s21_20m s22_20m];
abcd_params_20m = s2abcd(s_params_20m, z0);
s11_30m = s_30m(1,1)*exp(j*s_30m(1,2)/180*pi);
s21_30m = s_30m(2,1)*exp(j*s_30m(2,2)/180*pi);
s12_30m= s_30m(3,1)*exp(j*s_30m(3,2)/180*pi);
s22_30m= s_30m(4,1)*exp(j*s_30m(4,2)/180*pi);
s_params_30m = [s11_30m s12_30m; s21_30m s22_30m];
abcd_params_30m = s2abcd(s_params_30m, z0);
s11_40m = s_40m(1,1)*exp(j*s_40m(1,2)/180*pi);
s21_40m = s_40m(2,1)*exp(j*s_40m(2,2)/180*pi);
s12_40m= s_40m(3,1)*exp(j*s_40m(3,2)/180*pi);
s22_40m= s_40m(4,1)*exp(j*s_40m(4,2)/180*pi);
s_params_40m = [s11_40m s12_40m; s21_40m s22_40m];
abcd_params_40m = s2abcd(s_params_40m, z0);
s11_50m = s_50m(1,1)*exp(j*s_50m(1,2)/180*pi);
s21_50m = s_50m(2,1)*exp(j*s_50m(2,2)/180*pi);
s12_50m= s_50m(3,1)*exp(j*s_50m(3,2)/180*pi);
s22_50m= s_50m(4,1)*exp(j*s_50m(4,2)/180*pi);
s_params_50m = [s11_50m s12_50m; s21_50m s22_50m];
abcd_params_50m = s2abcd(s_params_50m, z0);
s11_60m = s_60m(1,1)*exp(j*s_60m(1,2)/180*pi);
s21_60m = s_60m(2,1)*exp(j*s_60m(2,2)/180*pi);
s12_60m= s_60m(3,1)*exp(j*s_60m(3,2)/180*pi);
s22_60m= s_60m(4,1)*exp(j*s_60m(4,2)/180*pi);
s_params_60m = [s11_60m s12_60m; s21_60m s22_60m];
abcd_params_60m = s2abcd(s_params_60m, z0);
s11_70m = s_70m(1,1)*exp(j*s_70m(1,2)/180*pi);
s21_70m = s_70m(2,1)*exp(j*s_70m(2,2)/180*pi);
s12_70m= s_70m(3,1)*exp(j*s_70m(3,2)/180*pi);
s22_70m= s_70m(4,1)*exp(j*s_70m(4,2)/180*pi);
s_params_70m = [s11_70m s12_70m; s21_70m s22_70m];
abcd_params_70m = s2abcd(s_params_70m, z0);
s11_80m = s_80m(1,1)*exp(j*s_80m(1,2)/180*pi);
s21_80m = s_80m(2,1)*exp(j*s_80m(2,2)/180*pi);
s12_80m= s_80m(3,1)*exp(j*s_80m(3,2)/180*pi);
s22_80m= s_80m(4,1)*exp(j*s_80m(4,2)/180*pi);
s_params_80m = [s11_80m s12_80m; s21_80m s22_80m];
abcd_params_80m = s2abcd(s_params_80m, z0);
```

```
s11_90m = s_90m(1,1)*exp(j*s_90m(1,2)/180*pi);
s21_90m = s_90m(2,1)*exp(j*s_90m(2,2)/180*pi);
s12_90m= s_90m(3,1)*exp(j*s_90m(3,2)/180*pi);
s22_90m= s_90m(4,1)*exp(j*s_90m(4,2)/180*pi);
s_params_90m = [s11_90m s12_90m; s21_90m s22_90m];
abcd_params_90m = s2abcd(s_params_90m, z0);
s11_100m = s_100m(1,1)*exp(j*s_100m(1,2)/180*pi);
s21_100m = s_100m(2,1)*exp(j*s_100m(2,2)/180*pi);
s12_100m= s_100m(3,1)*exp(j*s_100m(3,2)/180*pi);
s22_100m= s_100m(4,1)*exp(j*s_100m(4,2)/180*pi);
s_params_100m = [s11_100m s12_100m; s21_100m s22_100m];
abcd_params_100m = s2abcd(s_params_100m, z0);
s11_200m = s_200m(1,1)*exp(j*s_200m(1,2)/180*pi);
s21_200m = s_200m(2,1)*exp(j*s_200m(2,2)/180*pi);
s12_200m= s_200m(3,1)*exp(j*s_200m(3,2)/180*pi);
s22_200m= s_200m(4,1)*exp(j*s_200m(4,2)/180*pi);
s_params_200m = [s11_200m s12_200m; s21_200m s22_200m];
abcd_params_200m = s2abcd(s_params_200m, z0);
s11_300m = s_300m(1,1)*exp(j*s_300m(1,2)/180*pi);
s21_300m = s_300m(2,1)*exp(j*s_300m(2,2)/180*pi);
s12_300m= s_300m(3,1)*exp(j*s_300m(3,2)/180*pi);
s22_300m= s_300m(4,1)*exp(j*s_300m(4,2)/180*pi);
s_params_300m = [s11_300m s12_300m; s21_300m s22_300m];
abcd_params_300m = s2abcd(s_params_300m, z0);
s11_400m = s_400m(1,1)*exp(j*s_400m(1,2)/180*pi);
s21_400m = s_400m(2,1)*exp(j*s_400m(2,2)/180*pi);
s12_400m= s_400m(3,1)*exp(j*s_400m(3,2)/180*pi);
s22_400m= s_400m(4,1)*exp(j*s_400m(4,2)/180*pi);
s_params_400m = [s11_400m s12_400m; s21_400m s22_400m];
abcd_params_400m = s2abcd(s_params_400m, z0);
s11_500m = s_500m(1,1)*exp(j*s_500m(1,2)/180*pi);
s21_500m = s_500m(2,1)*exp(j*s_500m(2,2)/180*pi);
s12_500m= s_500m(3,1)*exp(j*s_500m(3,2)/180*pi);
s22_500m= s_500m(4,1)*exp(j*s_500m(4,2)/180*pi);
s_params_500m = [s11_500m s12_500m; s21_500m s22_500m];
abcd_params_500m = s2abcd(s_params_500m, z0);
s11_600m = s_600m(1,1)*exp(j*s_600m(1,2)/180*pi);
s21_600m = s_600m(2,1)*exp(j*s_600m(2,2)/180*pi);
s12_600m= s_600m(3,1)*exp(j*s_600m(3,2)/180*pi);
s22_600m= s_600m(4,1)*exp(j*s_600m(4,2)/180*pi);
s_params_600m = [s11_600m s12_600m; s21_600m s22_600m];
abcd_params_600m = s2abcd(s_params_600m, z0);
s11_700m = s_700m(1,1)*exp(j*s_700m(1,2)/180*pi);
s21_700m = s_700m(2,1)*exp(j*s_700m(2,2)/180*pi);
s12_700m= s_700m(3,1)*exp(j*s_700m(3,2)/180*pi);
s22_700m= s_700m(4,1)*exp(j*s_700m(4,2)/180*pi);
s_params_700m = [s11_700m s12_700m; s21_700m s22_700m];
abcd_params_700m = s2abcd(s_params_700m, z0);
s11_800m = s_800m(1,1)*exp(j*s_800m(1,2)/180*pi);
s21_800m = s_800m(2,1)*exp(j*s_800m(2,2)/180*pi);
s12_800m= s_800m(3,1)*exp(j*s_800m(3,2)/180*pi);
s22_800m= s_800m(4,1)*exp(j*s_800m(4,2)/180*pi);
s_params_800m = [s11_800m s12_800m; s21_800m s22_800m];
abcd_params_800m = s2abcd(s_params_800m, z0);
s11_1000m = s_1000m(1,1)*exp(j*s_1000m(1,2)/180*pi);
s21_1000m = s_1000m(2,1)*exp(j*s_1000m(2,2)/180*pi);
s12_1000m= s_1000m(3,1)*exp(j*s_1000m(3,2)/180*pi);
s22_1000m= s_1000m(4,1)*exp(j*s_1000m(4,2)/180*pi);
```

```
s_params_1000m = [s11_1000m s12_1000m; s21_1000m s22_1000m];
abcd_params_1000m = s2abcd(s_params_1000m, z0);
F = 1e6*[1.2, 10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 200, 300, 400, 500, 600, 700, 800, 1000];
A = [1/abcd_params_12k(1,1),
1/abcd_params_10m(1,1),
1/abcd_params_20m(1,1),
1/abcd_params_30m(1,1),
1/abcd_params_40m(1,1),
1/abcd_params_50m(1,1),
1/abcd_params_60m(1,1),
1/abcd_params_70m(1,1),
1/abcd_params_80m(1,1),
1/abcd_params_90m(1,1),
1/abcd_params_100m(1,1),
1/abcd_params_200m(1,1),
1/abcd_params_300m(1,1),
1/abcd_params_400m(1,1),
1/abcd_params_500m(1,1),
1/abcd_params_600m(1,1),
1/abcd_params_700m(1,1),
1/abcd_params_800m(1,1),
%1/abcd_params_900m(1,1),
1/abcd_params_1000m(1,1)
];
figure;semilogx(F, 20*log10(abs(A)),'+g');grid
```

C.1.3 $'fminsearch'$ function

```
function f = fmin_fun(x)
freq = 1e6*[1.2, 3.6, 6.0, 8.4, 10.8, 13.2, 15.6, 18.0, 20.4, 22.8, 25.2, 27.6, 30, 40, 50, 60, 70, 80, 90, 100, 140, 160, 200, 300, 400, 500, 600, 800, 1000];
L = 6.0e1;        % length L %
i=sqrt(-1);        % i %
Q=[1.0039 - 0.0198i, 0.9699 - 0.0558i, 0.6870 - 0.0365i, 1.2363 - 0.1419i, 1.0973 - 0.1867i, 1.0705 - 0.1961i, 1.0363 - 0.2099i, 1.0242 - 0.2785i, 0.9705 - 0.3158i, 0.9326 - 0.2955i, 0.9594 - 0.3027i, 0.8937 - 0.3445i, 0.9607 + 0.0073i, 0.9284 - 0.0071i, 0.8815 + 0.0132i, 0.8216 + 0.0029i, 0.7348 + 0.0155i, 0.6113 + 0.0243i, 0.4195 + 0.0490i, 0.0925 + 0.0997i, 3.0475 + 0.3784i, 1.8320 + 0.0637i, 1.2367 + 0.0215i, 0.4361 + 0.0230i, -0.3611 + 0.0604i, -1.0783 + 0.2078i, 0.7610 + 1.1377i, -0.7444 - 0.0330i, -14.1449 - 8.9693i];        % the value of the inverse of the transfer function %
Cl = 1.015e-9;          % equivalent output capacitance %
s = 2*pi*freq*i;
r= x(1);        % resistance %
l= x(2);        % inductance %
c= x(3);        % capacitance %
theta=((r+s*l).*(s*c)).^(1/2);
Zo=((r+s*l)./ (s*c)).^(1/2);
% ff1 = cosh(theta*L) + Zo*sinh(theta*L)*s*Cl - Q;
part1=cosh(theta*L);
part2=Zo.*sinh(theta*L).*s*Cl;
f=part1+part2-Q;
f=abs(f);f=sum(f);
% To call this function: %
```

%> fmin_fun([0.01, 1e-11 1e-11]) %
%To use fminsearch function: %
%> [x,fval] = fminsearch('fmin_fun',[1e-2, 1e-10, 1e-14]) %

C.1.4 Spice simulation of the transmission line

```
* Transmission line without CMOS INVERTER
VIN 2 0 pulse (0 5 0 20n 20n 5e-07 1e-06)
R 2 3 50 Cp 3 0 15p
X1 3 4 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X2 4 5 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X3 5 6 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X4 6 7 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X5 7 8 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X6 8 9 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X7 9 10 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X8 10 11 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X9 11 12 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X10 12 13 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X11 13 14 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X12 14 15 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
Cl 15 0 1015p
.SUBCKT lumped5 1 11 50
R1 1 2 {RR}
L1 2 3 {LL}
C1 3 50 {CC}
R3 3 4 {RR}
L2 4 5 {LL}
C2 5 50 {CC}
R5 5 6 {RR}
L3 6 7 {LL}
C3 7 50 {CC}
R7 7 8 {RR}
L4 8 9 {LL}
C4 9 50 {CC}
R9 9 10 {RR}
L5 10 11 {LL}
C5 11 50 {CC}
.ENDS
.tran 1n 2.5u .plot tran V(3) .plot tran V(15)
*.plot DC V(15) *.print DC V(15)
**************************** **** Node 0(ground), 1(Vdd), 2(Vin), 3(Vout)****** **********************
```

C.1.5 Spice simulation of the MOSFET driver with power supply

```
* Transmission line with CMOS INVERTER
La 1 20 0.3n Ra 21 20 0.006
VDD 21 0 DC 13V
VIN 3 0 pulse (0 10 0 64n 64n 5e-07 1e-06)
R1 3 4 7
C1 1 2 0.1u
Lb 2 30 0.3n Rb 0 30 0.006
M1 5 4 1 1 PMOS L=1u W=12u
M2 5 4 2 2 NMOS L=1u W=12u
Cp 5 0 15p
X1 5 6 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X2 6 7 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X3 7 8 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X4 8 9 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X5 9 10 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X6 10 11 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X7 11 12 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X8 12 13 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X9 13 14 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X10 14 15 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X11 15 16 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
X12 16 17 0 lumped5 {RR=2.8e-3 LL=2.9e-11 CC=1.6e-11}
Cl 17 0 15p
X13 1 17 0 irf540n
.SUBCKT lumped5 1 11 50
R1 1 2 {RR}
L1 2 3 {LL}
C1 3 50 {CC}
R3 3 4 {RR}
L2 4 5 {LL}
C2 5 50 {CC}
R5 5 6 {RR}
L3 6 7 {LL}
C3 7 50 {CC}
R7 7 8 {RR}
L4 8 9 {LL}
C4 9 50 {CC}
R9 9 10 {RR}
L5 10 11 {LL}
C5 11 50 {CC}
.ENDS
.tran 2.5n 2u .plot tran V(5) .plot tran V(17)
****************************** **** Node 0(ground), 1(Vdd), 2(Vin), 3(Vout)****** *************
.MODEL NMOS NMOS (LEVEL=2 VTO=0.5 GAMMA=0 KP=8.64E-03)
.MODEL PMOS PMOS (LEVEL=2 VTO=-0.5 GAMMA=0 KP=8.64E-03)
.SUBCKT irf540n 1 2 3 * SPICE3 MODEL WITH THERMAL RC NETWORK **********************************
Model Generated by MODPEX * *Copyright(c) Symmetry Design Systems* * All Rights Reserved * * UNPUBLISHED LICENSED SOFTWARE * * Contains Proprietary Information * * Which is The Property of * * SYMMETRY OR ITS LICENSORS * *Commercial Use or Resale Restricted * * by Symmetry License Agreement * ********************************
Model generated on Sep 5, 01 * MODEL FORMAT: SPICE3 * Symmetry POWER MOS Model (Version 1.0) * External Node Designations * Node 1 -> Drain * Node 2 -> Gate * Node 3 -> Source M1 9 7 8 8 MM L=100u W=100u .MODEL MM NMOS LEVEL=1 IS=1e-32 +VTO=3.58173 LAMBDA=0.00806114 KP=112.25 +CGSO=1.896e-05 CGDO=1e-11 RS 8 3 0.025918 D1 3 1 MD .MODEL MD D IS=1.565e-11 RS=0.006486 N=1.1328 BV=100 +IBV=0.00025 EG=1.2 XTI=3.32496
```

TT=0 +CJO=1.16e-09 VJ=3.16363 M=0.840542 FC=0.5 RDS 3 1 1e+06 RD 9 1 0.0130608 RG 2 7 6.45271 D2 4 5 MD1 * Default values used in MD1: * RS=0 EG=1.11 XTI=3.0 TT=0 * BV=infinite IBV=1mA .MODEL MD1 D IS=1e-32 N=50 +CJO=1.30485e-09 VJ=0.899032 M=0.9 FC=1e-08 D3 0 5 MD2 * Default values used in MD2: * EG=1.11 XTI=3.0 TT=0 CJO=0 * BV=infinite IBV=1mA .MODEL MD2 D IS=1e-10 N=0.4 RS=3e-06 RL 5 10 1 FI2 7 9 VFI2 -1 VFI2 4 0 0 EV16 10 0 9 7 1 CAP 11 10 2.35428e-09 FI1 7 9 VFI1 -1 VFI1 11 6 0 RCAP 6 10 1 D4 0 6 MD3 * Default values used in MD3: * EG=1.11 XTI=3.0 TT=0 CJO=0 * RS=0 BV=infinite IBV=1mA .MODEL MD3 D IS=1e-10 N=0.4 .ENDS irf540n

*SPICE Thermal Model Subcircuit .SUBCKT irf540nt 3 0

R_RTHERM1 2 3 0.158 R_RTHERM2 1 2 0.274 R_RTHERM3 0 1 0.29 C_CTHERM1 2 3 0.00131 C_CTHERM2 1 2 0.001686 C_CTHERM3 0 1 0.022562

.ENDS irf540nt

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