One Dimensional Feed-Forward Modulation of a Cascaded H-Bridge Multi-Level Converter including Capacitor Balancing with Reduced Switching Frequency

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Abstract

Multi-level converters are well suited to medium and high power applications where the priority is for high quality a.c. currents with low harmonic content and for low switching losses. Suitable modulation schemes must find a good compromise between these two conflicting aims.

This paper relates one-dimensional feed-forward modulation (1DFFM) to carrier based modulation. 1DFFM can produce high quality currents despite d.c. capacitor voltage ripple by accounting for measured capacitor voltages in the modulation process and can balance capacitor voltages by eliminating states that cause the capacitor voltages to diverge. It is shown in this paper that this method increases the device switching frequency compared to carrier-based modulation with the same sampling rate.

An alternative modulation method is presented which balances the capacitor voltages by assigning commutations to bridges during each sampling period. This approach is less likely to cause two bridges to commutate at the same time so produces a lower device switching frequency than 1DFFM. It is shown experimentally that the two methods produce similar a.c. current distortion and both effectively balance the capacitor voltages.

Introduction

Multi-level converters are a variety of power converter that produce stepped voltage waveforms from different methods of summing voltages of capacitive storage elements and are advantageous for a diverse range of applications requiring good quality output waveforms at high power ratings [1]-[3]. The output waveforms contain lower step changes in voltage than a two level converter of the same rating and approximate a reference signal more closely, thus reducing harmonic emissions. Furthermore, multi-level topologies allow high power converters to be constructed using devices with lower voltage ratings.

Numerous topologies have been discussed in the literature, the main three being the diode clamped converter, the flying capacitor converter and the cascaded H-bridge converter. The cascaded H-bridge (Fig. 1) has received attention primarily because it has a modular construction, which reduces the costs of construction and maintenance. It also requires fewer power electronic devices than other topologies to achieve the same number of output voltage levels [4]. The two-cell case, depicted in Fig. 1, requires four switching signals to control a total of eight devices as the pairs of devices in each leg are operated in a complementary fashion. The naming convention for the states of single H-bridge is given in Table I, where $x \in \{1, 2\}$. States for the complete phase-leg are denoted with the notation $(s_{11} - s_{12}, s_{21} - s_{22})$.
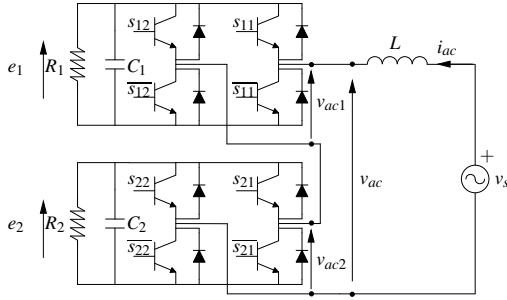
Figure 1: Two-Cell Cascaded H-bridge rectifier.

Table I: Naming convention of H-bridge states.

state	s_{x2}	s_{x1}	v_{acx}
-1	1	0	$-e_x$
0	0	0	0
	1	1	
1	0	1	e_x

The d.c. links in Fig. 1 can be supplied by single phase rectifiers or isolated converters in a back-to-back arrangement [5]. The cascaded H-bridge topology is particularly well suited for use in STATCOM applications, in which case only capacitors are required in the d.c. links making the topology very compact [1]. The results presented in later sections of this paper are performed with each bridge loaded by a resistor as shown in Fig. 1. The total capacitor voltage is controlled in closed-loop to draw active power from the supply.

Many modulation schemes that allow the converters to produce high quality a.c. waveforms have been presented in the literature. Carrier based methods have been studied in great detail [6][7], as have space-vector methods [8]-[10] and programmed modulation schemes. Most modulation schemes have been developed assuming ideal constant and equal d.c. link voltages, which introduces the concept of state redundancy. Multiple switching states produce identical output voltages allowing for further optimization of the modulation scheme [8][10][11].

In practice, the d.c. link capacitor voltages are not constant as the phase legs of a cascaded H-bridge are single phase converters and are subject to power pulsations at twice the a.c. side fundamental frequency. Furthermore, as each bridge spends different periods of time in different switching states and may experience different loads or internal losses, the d.c. voltages are not always equal. Modulation techniques which compensate for the variation in d.c. link capacitor voltages are known as *feed-forward* techniques [12]-[15].

Throughout the paper the capacitor voltages $e_{1,2}$ are considered to be time varying and are not assumed to be exactly equal.

One-Dimensional Modulation

One-dimensional modulation (1DM), which was first presented in [16], is a single-phase modulation scheme which relies on knowledge of the position of every switching state in a one-dimensional control region. Since being developed, 1DM has been shown to be a basis for simplified implementation of space-vector modulation [17].

For one-dimensional feed-forward modulation (1DFFM) the position of each state is calculated at each sampling instant using measured d.c.-link capacitor voltages [14][18]. An example of a control region with un-balanced capacitor voltages is shown in Fig. 2. The two states nearest to the reference voltage are used to modulate and the proportion of the sampling time to apply each state is given by (1)

$$d_{S_1} = \frac{V(S_2) - v^*}{|V(S_2) - V(S_1)|} \qquad\qquad d_{S_2} = 1 - d_{S_1} \qquad\qquad (1)$$

where

- S_1 and S_2 are the first and second states to apply
- $V(S_x)$ is the calculated output voltage of the xth state
- v^* is the sampled reference voltage.

To balance the capacitor voltages to the desired voltage ratio, switching states that cause the capacitor voltages to diverge are rejected at each sampling instant. Of the permitted states, the two closest to the sample are used to reproduce the reference voltage.

The key advantages of 1DFFM are

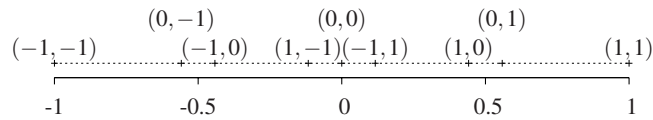- straightforward digital implementation,

(0,−1) (0,0) (0,1)

(−1,−1) (−1,0) (1,−1)(−1,1) (1,0) (1,1)

-1 -0.5 0 0.5 1

Figure 2: Control region with un-balanced capacitor voltages

Voltage (p.u.)

2

1

0

−1

−2

carrier

reference

sampled reference

Voltage (p.u.)

2

1

0

−1

−2

A B C

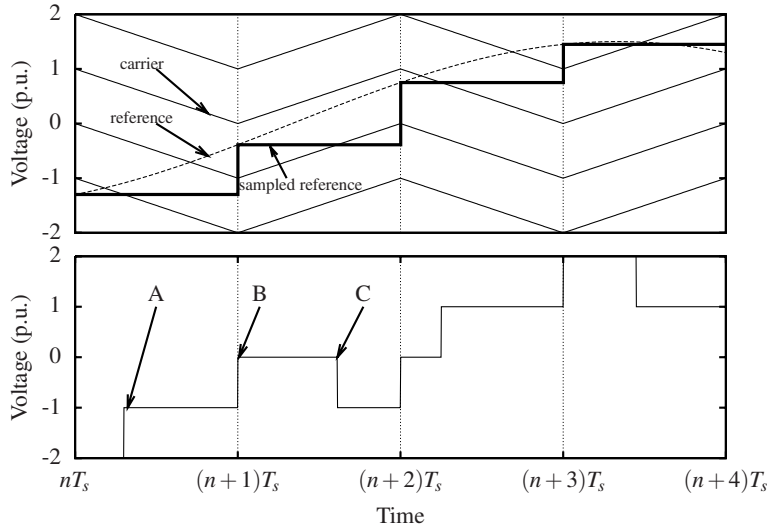nT_s $(n+1)T_s$ $(n+2)T_s$ $(n+3)T_s$ $(n+4)T_s$

Time

Figure 3: Asymmetrical regularly sampled level-shifted carrier modulation.

- balancing of capacitor voltages and
- good quality a.c. waveforms even when the capacitor voltages are not at their target values.

This paper analyses 1DM to show that it is very closely related to regularly-sampled carrier-based modulation. It goes on to show that eliminating certain states for balancing of the capacitor voltages tends to cause the converter to perform multiple simultaneous commutations, which increases the total device switching frequency.

An alternative method of choosing states is proposed, which assigns commutations to suitable bridges in order to equalize the capacitor voltages without introducing extra commutations. The proposed method is then verified experimentally in terms of its total device switching frequency, balancing capability and a.c. side harmonic emissions.

1DFFM Compared with Carrier Modulation

An example of regularly-sampled, level-shifted carrier (LSC) modulation (also known as phase-disposition or PD modulation) is shown in Fig. 3. The reference signal is sampled at twice the carrier frequency and the switching state changes every time the sampled reference crosses one of the carrier signals. Because of the alternating gradients of the carrier signal, alternate sampling periods produce voltage steps in opposite directions (edges A and C), with extra commutations (edge B) sometimes occurring at the sampling instants.

Fig. 4 shows a representation of 1DFFM with arbitrary capacitor voltages. Segments of equivalent carrier signals have been constructed for the two states nearest to the reference and the resulting gate signals are plotted beneath. The carrier signal represents the calculation of duty times of (1) for the chosen states. When the capacitor voltages are equal the equivalent carrier signals are the same as for LSC modulation.

Literature regarding 1D modulation does not specify in which order the chosen states should be applied. If the modulation is programmed to produce edges in opposite directions in consecutive sampling periods then the effective carrier signals mimic the shape of triangular carrier modulation, as depicted in Fig. 4. Thus the 1DFFM modulation produces a.c. voltage waveforms equivalent to asymmetrically sampled, LSC modulation when the capacitor voltages are equal.
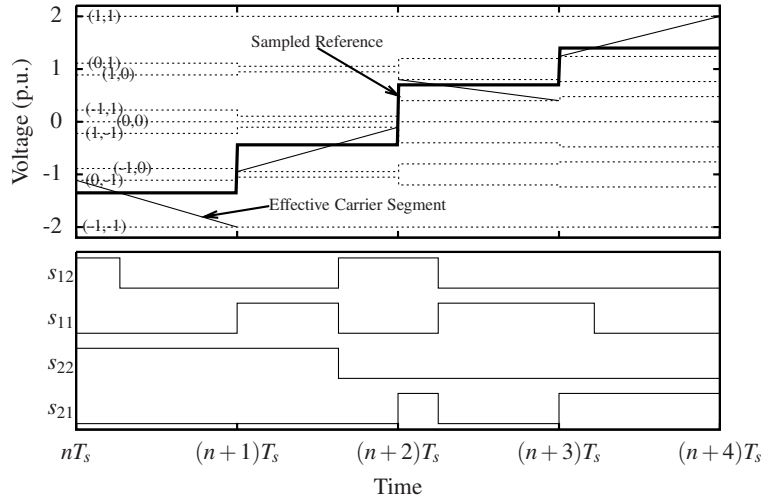
Figure 4: An equivalent carrier signal and associated gate signal for 1DFFM allowing all the states.
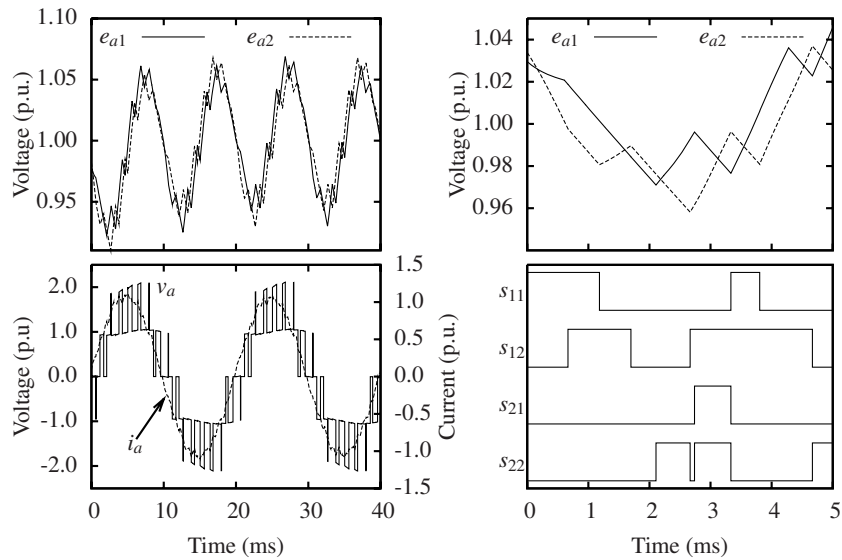

Figure 5: Simulation of 1DFFM with capacitor voltage balancing

A key difference between the 1D modulation and LSC modulation is the interpretation of the carrier signals. For LSC modulation each carrier signal represents a complementary pair of devices so when the reference crosses a carrier only one commutation is performed. 1DFFM considers all the switching states and the effective carrier signals extend between adjacent states. In some cases multiple simultaneous commutations are required to step between adjacent states even if the reference has crossed only one carrier.

Fig. 4 shows an example of how the selection of switching states can affect the total device switching frequency. When the reference is towards the centre of the range where there are most states, multiple commutations are needed to step between the states closest to the reference, for example during the second and third sampling period shown.

Multiple simultaneous commutations are also produced when 1DFFM is used to balance capacitor voltages (Fig. 5.) Each time the capacitor voltages cross the set of permitted states changes. It is common for the state at the end of one sampling period to be forbidden during the next sampling period and multiple commutations are often required to change to the next permitted switching state. This is the cause of the simultaneous commutations at various intervals in Fig. 5, which shows two cycles of simulated wave-forms for one phase of a three-phase converter and a close-up view of the d.c. voltages and switching signals. The simulated converter has two cells per phase and is simulated in rectifying configuration with equal resistive loads on each cell.
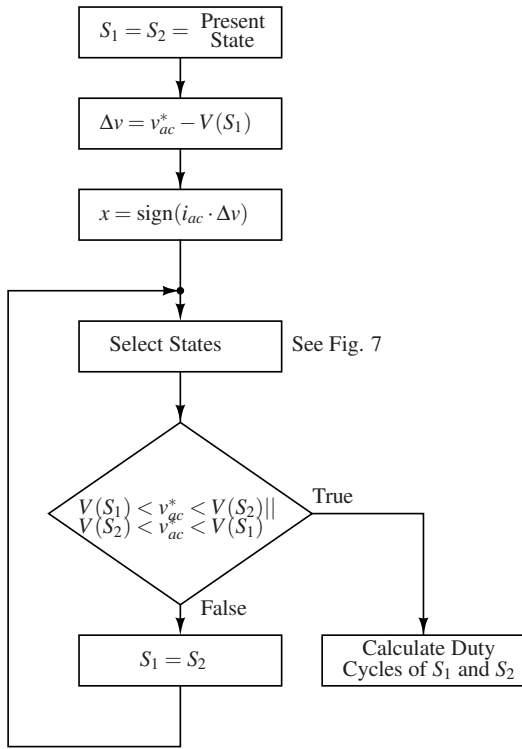
Figure 6 flowchart:

$S_1 = S_2 = $ Present State

$\Delta v = v_{ac}^* - V(S_1)$

$x = \text{sign}(i_{ac} \cdot \Delta v)$

Select States — See Fig. 7

$V(S_1) < v_{ac}^* < V(S_2) \,||\, V(S_2) < v_{ac}^* < V(S_1)$

True → Calculate Duty Cycles of S_1 and S_2

False → $S_1 = S_2$

Figure 6: Outer loop ensures that chosen states can produce desired reference

Figure 7 flowchart:

$x > 0$

True → $n = 1$

False → $n = N$

$n += x$

$|S_2.s_n + \text{sign}(\Delta v)| <= 1$

False → $n += x$
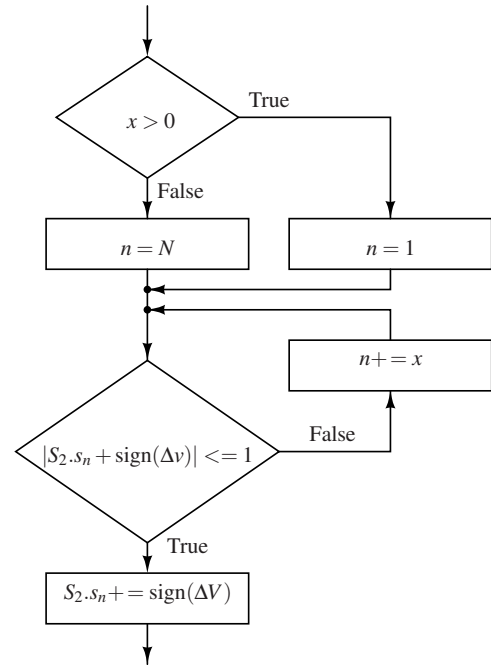
True → $S_2.s_n += \text{sign}(\Delta V)$

Figure 7: Inner loop chooses most suitable bridge to commutate.

Choosing states to reduce switching frequency

This section proposes an alternative method of choosing switching states to balance capacitor voltages without introducing simultaneous commutations. Capacitor balancing is achieved by applying each demanded commutation to the appropriate bridge. In the proposed scheme, states are chosen by considering the effect of each demanded commutation and choosing the best bridge to perform it.

The Effect of Commutations on Capacitor Voltages

When current is flowing into the converter from the a.c. side, a positive voltage step from a single bridge causes that bridge to charge if stepping from 0 to 1, or to stop discharging if stepping from -1 to 0. In both these cases the best bridge to commutate is the one with the lowest capacitor voltage. For other combinations the product $\Delta v i_{ac}$ (where Δv is the required voltage step direction) defines the best bridge to commutate: the bridge with the lowest capacitor voltage for positive values and the bridge with the highest voltage for a negative values. If the chosen bridge cannot produce a step in the desired direction, for example if a positive step is demanded but the bridge is already in the +1 state, then the modulator must fall back to the other, less ideal, bridge.

Proposed Modulation Scheme

A complete feed-forward modulation scheme based on assigning commutations to the most appropriate bridge is defined by the flow charts in Figs. 6 and 7.

The modulation scheme comprises two loops. Starting from the state at the end of the half-carrier period, the outer loop (Fig. 6) determines the required voltage step direction and the inner loop Fig. 7 selects which bridge should commutate to produce such a step. In Fig. 7 the two states being considered, S_1 and S_2, are broken down in terms of the states of the individual bridges. For a two-cell converter $S_x.s_1$ and $S_x.s_2$ are the states of the bridge with the lowest and highest capacitor voltages respectively. The sign

function is defined as follows:

$$\text{sign}(x) = \begin{cases} 1 & \text{if } x > 0 \\ -1 & \text{otherwise.} \end{cases} \tag{2}$$

Once a bridge is chosen to commutate, the outer loop calculates the expected output voltage of the new states from the measured capacitor voltages. If the two chosen states do not straddle the reference voltage another step is required, which is again assigned to the appropriate bridge by the inner loop. The combined effect of the two loops is a step-by-step search through the control region, starting with the converter state at the end of the previous sampling period. For moderate steps in reference voltage and reasonably balanced capacitor voltages, this method tends to produce single commutations.

The proposed method can be made to mimic LSC modulation in the same way as 1DFFM by demanding alternate positive and negative edges. Any resulting extra commutations at the sampling instants are distributed between the bridges using the same algorithm described.
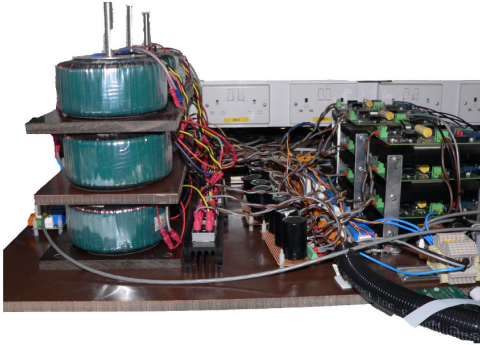
Experimental Results

Figure 8: Experimental Converter

Table II: Operating conditions for experimental converter

Parameter	Value
Supply Voltage (peak)	190V
Capacitor Voltage Reference	100V
DC-Link Capacitance	1mF
AC-Side Inductance	11mH
Modulation Sampling Frequency	1500Hz

The proposed modulation scheme has been tested experimentally at low voltage using the three-phase converter shown in Fig. 8. The experimental converter has three cells per phase but one cell has been disabled per phase as this paper discusses the two-cell case. The converter was operated under the conditions listed in Table II. The supply was fed from the lab supply with a variable autotransformer set to give a convenient d.c. voltage value with high modulation index. The presented results are normalized to a mean capacitor voltage of 1V and are from phase a of the three-phase converter.

Balanced Loads

For balanced loads, $R_1 = R_2 = 57\Omega$, 1DFFM and the proposed method are compared in Fig. 9. The a.c. side waveforms are indistinguishable but switching functions of the individual bridges show that the proposed method produces fewer commutations than 1DFF modulation. Table III shows an 18% reduction in commutations at this sampling rate using the new method. The higher rate of commutation allows 1DFFM to balance the capacitor voltages slightly better, but without any observable difference in the current.

Table III: Switching rate with balanced loads

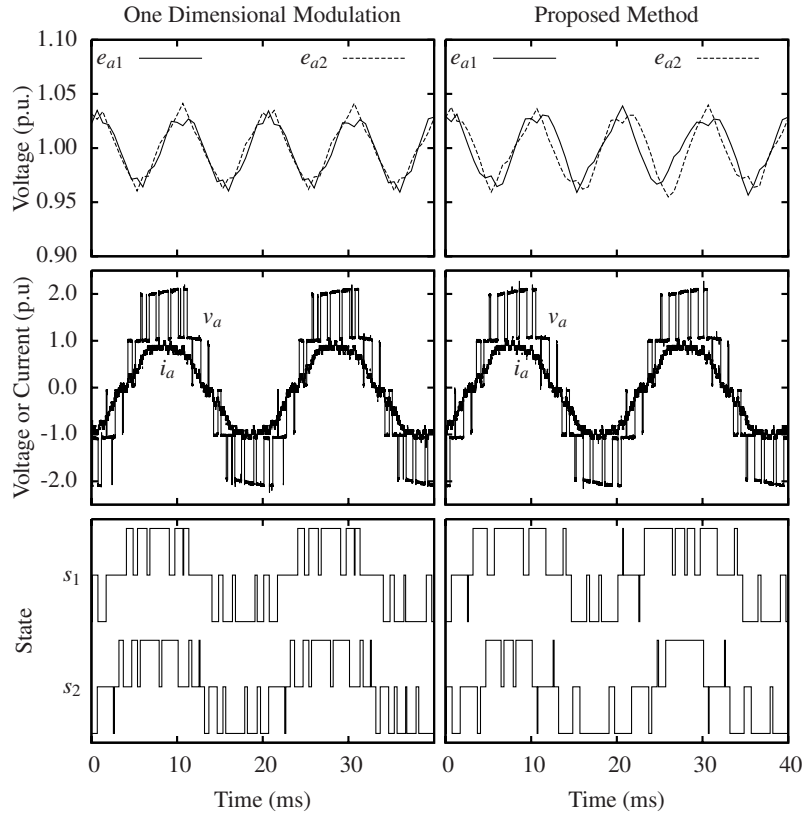|	Commutations per cycle		
	s_1	s_2	total
1DFFM	20	25	44
Proposed Method	18	18	36

Figure 9: 1DFFM and the proposed method with balanced d.c.-side loads.

Unbalanced loads

The proposed method has been tested for two cases with unbalanced loads, which are compared side-by-side in Fig. 10. The loads in each case are given in Table IV.

In the first case, the d.c. links are loaded according to *Case 1* in Table IV and the proposed modulation method is able to keep the capacitor voltages close to equal. In order to increase the power flow in the more heavily loaded bridge, the commutations are not shared equally between the two bridges (Table V) but the total number of commutations remains the same.

Table IV: Resistive loads for unbalanced operation

	R_1	R_2
Case 1	39Ω	57Ω
Case 2	25Ω	57Ω

Table V: Switching rate with unbalanced loads

	Commutations per cycle		
	s_1	s_2	total
Case 1	12	24	36
Case 2	4	32	36

In the second case, the modulation of the heavily loaded bridge is saturated to the minimum commutation rate of four commutations per cycle and the capacitor voltages cannot be kept equal. The capacitor voltage of the over-loaded bridge drops by ten percent and the other voltage increases because the voltage controller acts on the sum of capacitor voltages.

The line voltage spectrum produced by both imbalanced cases is shown in Fig. 11 as well as the line voltage spectrum from a simulation of regularly sampled LSC modulation with constant and equal d.c. sources at the same modulation index. Despite the capacitor voltage ripple in the practical converter and the unequal capacitor voltages in *Case 2* both methods produce a similar voltage spectrum to the ideal modulator, confirming the relationship between the proposed method and LSC modulation and suggesting that the feed-forward element of the modulation is effective.
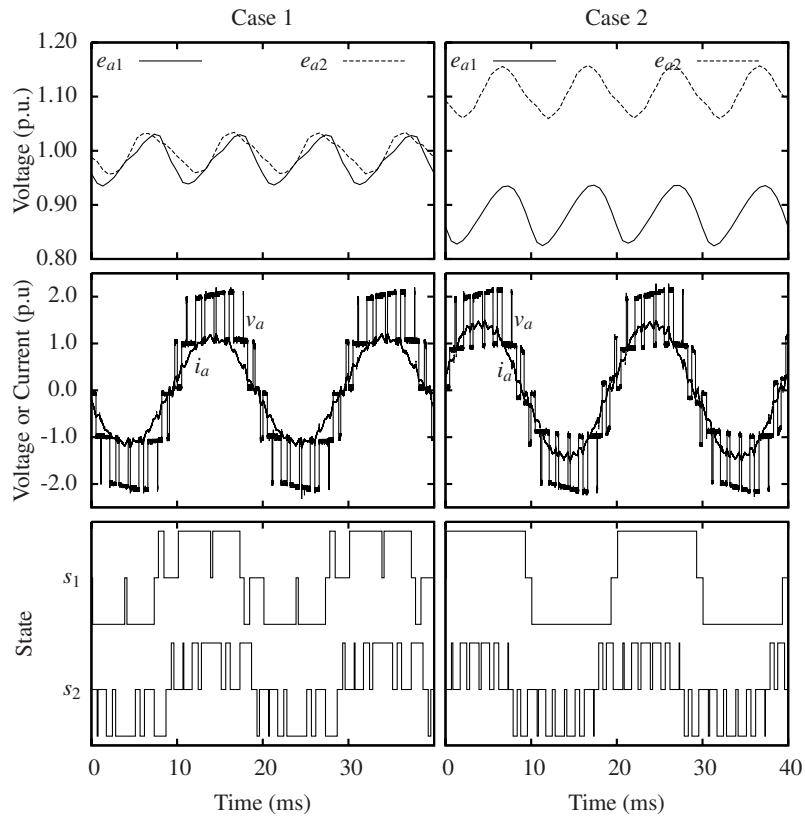
Case 1   Case 2

Figure 10: Proposed method operating with unbalanced loads
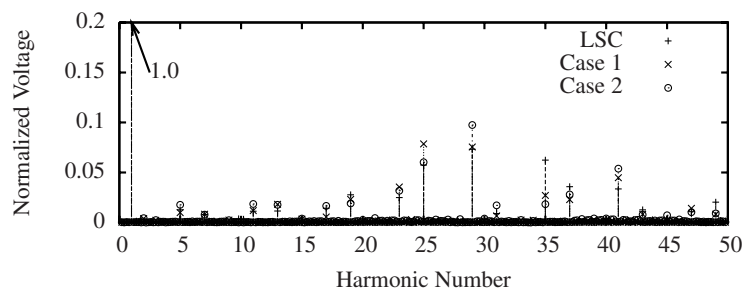

Figure 11: Line voltage spectrum of proposed method in comparison with level-shifted carrier modulation.

Conclusion

One-dimensional, feed-forward modulation has been analysed in terms of carrier-based modulation and it has been shown that the choice of switching states employed for capacitor voltage balancing has a tendency to increase the total device switching frequency. An alternative method of choosing states has been presented which allocates single commutations between bridges and so has lower device switching frequency. The proposed method has been verified experimentally at low voltage with balanced and unbalanced loads for a two-cell converter. The proposed modulation scheme, as defined in Figs. 6 and 7, is general and not specific to a two-cell converter. There is therefore scope for further work to study the behaviour and performance of the proposed modulation method when applied to converters with a greater number of cells.

References

[1] F. Z. Peng, W. Qian, and D. Cao, "Recent advances in multilevel converter/inverter topologies and applications," in *Int. Power Electron. Conf*, Jun. 2010, pp. 492–501.

[2] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 8, pp. 2553–2580, 2010.

[3] J. Rodriguez, L. G. Franquelo, S. Kouro, J. I. Leon, R. C. Portillo, M. A. M. Prats, and M. A. Perez, "Multilevel converters: An enabling technology for high-power applications," *Proc. IEEE*, vol. 97, no. 11, pp. 1786 –1817, 2009.

[4] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[5] J. Rodriguez, J. Pontt, E. Silva, J. Espinoza, and M. Perez, "Topologies for regenerative cascaded multilevel inverters," in *IEEE 34th Annual Power Electron. Specialist Conf. PESC 03*, vol. 2, Jun. 2003, pp. 519 – 524.

[6] B. P. McGrath and D. G. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 858–867, Aug. 2002.

[7] D. G. Holmes and B. P. McGrath, "Opportunities for harmonic cancellation with carrier-based pwm for a two-level and multilevel cascaded inverters," *IEEE Trans. Ind. Electron.*, vol. 37, no. 2, pp. 574 –582, Mar. 2001.

[8] B. P. McGrath, D. G. Holmes, and T. Lipo, "Optimized space vector switching sequences for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 18, no. 6, pp. 1293–1301, Nov. 2003.

[9] A. R. Beig, G. Narayanan, and V. T. Ranganathan, "Modified SVPWM algorithm for three level VSI with synchronized and symmetrical waveforms," *IEEE Trans. Ind. Electron.*, vol. 54, no. 1, pp. 486–494, Feb. 2007.

[10] A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1672 –1681, 2007.

[11] B. P. McGrath, T. Meynard, G. Gateau, and D. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 508–516, Mar. 2007.

[12] S. Kouro, P. Lezana, M. Angulo, and J. Rodriguez, "Multicarrier PWM with DC-Link ripple feedforward compensation for multilevel inverters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 52–59, Jan. 2008.

[13] J. I. Leon, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, P. W. Wheeler, and A. J. Watson, "Three-dimensional feedforward space vector modulation applied to multilevel diode-clamped converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 1, pp. 101–109, Jan. 2009.

[14] J. I. Leon, S. Vazquez, A. J. Watson, L. G. Franquelo, P. W. Wheeler, and J. M. Carrasco, "Feed-forward space vector modulation for single-phase multilevel cascaded converters with any DC voltage ratio," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, pp. 315–325, Feb. 2009.

[15] J. I. Leon, S. Kouro, S. Vazquez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Multidimensional modulation technique for cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 58, no. 2, pp. 412 –420, Feb. 2011.

[16] J. I. Leon, R. Portillo, L. G. Franquelo, S. Vazquez, J. M. Carrasco, and E. Dominguez, "New space vector modulation technique for single-phase multilevel converters," in *IEEE Int. Symp. on Ind. Electron. ISIE*, Jun. 2007, pp. 617 –622.

[17] J. I. Leon, S. Vazquez, J. A. Sanchez, R. Portillo, L. G. Franquelo, J. M. Carrasco, and E. Dominguez, "Conventional space-vector modulation techniques versus the single-phase modulator for multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2473–2482, Jul. 2010.

[18] J. I. Leon, S. Vazquez, S. Kouro, L. G. Franquelo, J. M. Carrasco, and J. Rodriguez, "Unidimensional modulation technique for cascaded multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 56, no. 8, pp. 2981–2986, 2009.